Abstract—A CMOS op-amp input and gain stage suitable for low voltage operation are introduced. The input stage operates in strong inversion and has common-mode range beyond rail-to-rail. It uses two complementary differential pairs connected in parallel. The common-mode dependent current biasing employs only four transistors, does not require additional voltage references, current switches and/or current mirrors and does not increase the minimum required supply voltage. The variation of the net transconductance is approximately 15% over the entire common-mode range. The gain-stage has constant output resistance. In addition it reduces the variation of the net transconductance due to variations in $\mu_n/\mu_p$ ratio.

I. INTRODUCTION

A widely used technique for obtaining a rail-to-rail input range, when designing low-voltage op-amps, is to connect two complementary differential pairs in parallel as shown in Fig. 1(a). In this way one guarantees that for any common-mode input voltage at least one of the differential pairs will operate properly. This simple topology is rarely used, however, because its net transconductance $g_{mT}$ varies by a factor of two over the common-mode input range. In mid-supply range, where both pairs operate, the net transconductance is given by:

$$g_{mT} = g_{m1} + g_{m2}$$

However, when the input common-mode voltage approaches the positive (negative) rail $g_{mT}$ reduces to $g_{m1}$ ($g_{m2}$) respectively. This variation does not allow optimal frequency compensation of multi-stage op-amps and also increases their distortion.

Since the individual differential-pair transconductances $g_{m1}$ and $g_{m2}$ are well-defined functions of the of the tail currents $I_n$ and $I_p$, respectively, a general method for obtaining common-mode-independent net transconductance is to employ common-mode-dependent current biasing. In other words, we balance the reduction in $g_{m1}$ ($g_{m2}$) (caused by the reduction of $I_n$ ($I_p$) when $V_{inCM}$ approaches $V_{ds}$ ($V_{dd}$)) by increasing $I_p$ ($I_n$) (e.g. Fig. 1(b)).

In the case of an input stage using BJT's or MOS transistors in weak inversion the requirement that $g_{mT}$ be independent of $V_{inCM}$ translates into the following, simple to implement, current-biasing requirement:

$$I_n + I_p = \text{const.}$$

If MOS transistors in strong inversion are to be used in such a rail-to-rail input stage the current biasing requirement is:

$$\sqrt{I_n} + \sqrt{I_p} = \text{const.} \quad \text{for } \beta_n = \beta_p$$

and, more general:

$$\sqrt{(2/\beta_n)I_n} + \sqrt{(2/\beta_p)I_p} = \text{const.} \quad \text{for } \beta_n \neq \beta_p$$

The main differences between various rail-to-rail input stage topologies reported in the literature is the employed biasing scheme. Those schemes targeting the MOS-strong inversion case can loosely be classified as either exact or approximate. All schemes realizing equations (3) or (4) [1], [2], [3] are considered exact, because under ideal conditions (perfect matching and no second order effects) they result in a constant net transconductance. The approximate schemes are based on the assumption that the tail currents $I_n$, $I_p$ take either their nominal value or are completely turned off. Those schemes are usually implemented by use of a simple 1:3 current mirrors [3], [4] and can reduce the $g_{mT}$-variation to within 15%. Unfortunately, most of the reported strong inversion biasing circuits have high complexity.

In Section II we present a simple approximate scheme which requires only four additional transistors and has a $g_{mT}$ variation of approximately 15%. In Section III a gain stage which has constant output resistance is introduced. Also, it reduces the variations of the effective net transconductance caused by variations in the mobility ratio $\mu_n/\mu_p$.

II. THE PROPOSED RAIL-TO-RAIL INPUT STAGE

The input stage, shown in Fig. 2(a), is topologically identical to that reported in [5]. However, the aspect ratios of the four additional transistors in the Fig. 2(a) circuit is three times that of the corresponding differential-pair transistors. The nominal value of the tail currents $I_{5a}$ and...
is 4I₀ and must be selected sufficiently large to ensure
strong-inversion operation. The aspect ratios of the n and
p-channel transistors are selected such that \( \beta_n = \beta_p = \beta \).
Under this conditions the Fig. 2(a) circuit guarantees rail-to-rail operation with a 15\% variation in \( g_{mT} \). To show this
let us first consider the operation of the \( M_5 - M_8 \) quartet.
As discussed in [5] if a CMOS current source (\( M_5 - M_6 \)) is
connected in series with a current sink (\( M_7 - M_8 \)), the
pair which must carry the higher current is forced into the
triode region and thus the smaller of the two currents is
conducted. For our case:

\[
I_e = \min \left( \frac{3}{4} I_{S_n}, \frac{3}{4} I_{p} \right) = \frac{3}{4} \min(I_{S_n}, I_{p}) \tag{5}
\]

Hence, the current \( I_e \) and the currents \( I_p = I_{S_n} - I_e \)
\((I_n = I_{S_n} - I_e)\) conducted by the differential-pair tran-
sistors \( M_{1,2}(M_{3,4}) \) of the Fig. 2(a) stage are,

1) \( V_{\text{inCM}} \) close to \( V_{ss} \):
\[
\begin{align*}
I_e &= 3/4I_{S_n} = 0 \\
I_n &= 1/4I_{S_n} = 0 \\
I_p &= I_{S_n} - I_e = 4I_0 - I_e = 4I_0
\end{align*}
\]

2) \( V_{\text{inCM}} \) near mid-supply:
\[
\begin{align*}
I_e &= 3I_0 \\
I_n &= I_{S_n} - I_e = 4I_0 - 3I_0 = I_0 \\
I_p &= I_{S_n} - I_e = 4I_0 - 3I_0 = I_0
\end{align*}
\]

3) \( V_{\text{inCM}} \) close to \( V_{dd} \):
\[
\begin{align*}
I_e &= 3/4I_{S_n} = 0 \\
I_n &= I_{S_n} - I_e = 4I_0 \\
I_p &= 1/4I_{p} = 0
\end{align*}
\]

Thus for the above three regions of operation, where the
tail currents \( I_{S_n}, I_{p} \) have their nominal (4I₀) value or have
zero value, the total transconductance (see equation (1)) is
the same and given by:

\[
g_{mT} = 2\sqrt{(2/\beta)I_0} \quad \text{when} \quad \beta_n = \beta_p = \beta \tag{6}
\]

For the transition regions, where \( 0 < I_{S_n, p} < 4I_0 \), \( g_{mT} \)
is not constant and slightly higher than the above value.
The maximum \( g_{mT} \) deviation can be calculated and is ap-
proximately 15\%.

The Fig. 2(a) rail-to-rail input stage was simulated using
HSPICE and BSIM2 (level 13) models for MOSIS 2-micron
ORBIT Analog Process. The size of the transistors and the
value of the constant bias current 4I₀ were as indicated on
the schematic. Fig. 2(b) shows the variation of \( I_n \) and \( I_p \)
bias currents as the \( V_{\text{inCM}} \) is swept from \( V_{ss} \) to \( V_{dd} \). The
three regions (near-\( V_{ss} \), mid-supply and near-\( V_{dd} \)) where
\( I_n \) and \( I_p \) must remain constant are evident. The non-zero
slope of those regions is due to the finite output resistance
of the used transistors. In Fig. 2(c) the simulated individ-
ual (\( g_{m_n}, g_{m_p} \)) and net transconductance (\( g_{mT} \)) are plotted
v.s. the input common-mode voltage. As expected, there are
two "bumps" in the \( g_{mT} \) plot corresponding to the two
transition regions. The small "glitch" present within each
"bump" can not be predicted if the simple square-law re-
lation is used to model the voltage-current behavior of the
MOS transistor. Since "glitches" occur when one of the
bias currents (\( I_n \) or \( I_p \)) has relatively low value, they are
most likely due to one of the differential pairs entering mod-
erate and then weak inversion region of operation.
Because of finite \( r_o \) effects, \( I_n \) and \( I_p \) are slightly larger
than 20\$\mu A\$ in the mid-supply region. For this reason the
net transconductance in this region is slightly higher than
that in the near-rail regions. As is the case with many
other rail-to-rail input stages, the one presented in this
paper relies on matching the transconductance parameter (β) of the used n-channel transistors to that of the used p-channel transistors. If the ratio between the mobility of the n-channel transistors and the mobility of the p-channel transistors $\mu_n/\mu_p$ is exactly known then $\beta_n$ can be made very close to $\beta_p$ by simply sizing the transistors whose β's are to be matched in accordance with: $W_n = W_p \mu_n$ for $L_n = L_p$. Unfortunately, for a given process from one run to another the ratio of the mobilities could vary as much as 30% from its nominal value [1] used to determine "the best" n-channel and p-channel aspect ratios. To illustrate the effect this variation would have on the net transconductance of the proposed input stage two additional simulations were performed. The width of the n-channel devices was changed to 48μ and 36μ — that is, a change of +15% and -15% from its nominal 42μ width. Since β-equality is achieved for $W_n = W_p = 42$, transistor having $W_n = 48\mu$ (36μ) would be equivalent to transistor having $W = 42$(the nominal value) and μ increased (decreased) by 15%. Fig. 3 shows the results from the simulations.

III. THE GAIN STAGE

Fig. 4 shows single-stage unbuffered op-amp which uses the input stage described in the previous section. The gain stage consists of two MOS-R current mirrors and a floating current source. Here, as in many other reported in the literature rail-to-rail topologies, in addition to providing voltage gain the gain stage is used to sum the small signal (differential) currents generated by the two input-stage differential pairs. However, there are some unique properties possessed by this gain stage. First, its output resistance — and thus the op-amp's gain — is independent of the level of the injected by the input stage common-mode currents ($I_n$, $I_p$). As a result the distortion caused by common-mode dependent gain is kept at its minimum. To show that the output resistance is constant it is sufficient to show that the output resistance of each current mirror is constant.
over the common-mode input range. Achieving equality of the above current gain expressions can be accomplished by making \( g_{m_{10}} = g_{m_{11,12}} = g_m \). This is done as in the input stage by sizing \( M_9, M_{10} \) and \( M_{11,12} \) so their \( \beta \)'s are identical.

The advantage of this gain stage over others becomes obvious only when the variations in \( g_mR \) and \( g_m' \) due to differences between the actual ratio of the mobilities and the one used to carry out the design are compared. The smaller the product \( g_mR \) the lower the \( g_m' \)-variation. However, this product should not be made lower than unity in order to retain a sufficiently large overall op-amp gain. As can be seen from the plots shown in Fig. 7, the change of \( \mu_n \) effects the transconductance of both the near-\( V_{ss} \) and near-\( V_{dd} \) range in same direction which results in lower relative variation within each curve. This can be explained with the fact that now each individual \( g_m' \) and \( g_m'' \) is determined by the transconductances of both n-channel and p-channel transistors.

If higher output resistance is desired the simple \( M_9,M_{10} \) and \( M_{11,12} \) current mirrors can be replaced by high-swing cascoded current mirrors without altering the properties of the gain stage.

IV. Conclusions
A simple rail-to-rail input stage operating in strong inversion was presented. Its net transconductance variation is approximately 15% over the entire common-mode range. A new gain stage was introduced. It was shown that the transconductance variation in this gain stage caused by imperfect \( \beta \)-matching is reduced as compared to previous techniques.

Figure 7: Effective net transconductance v.s. \( V_{inCM} \) for three different values of \( \mu_n' \): (1) "actual" \( \mu_n' \) is 15% higher than the one used in the design; (2) "actual" \( \mu_n' = \mu_n \) is used; (3) "actual" \( \mu_n' \) is 15% less than the used one;

REFERENCES