Optical to Electrical Converter

By

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Senior Project

ELECTRICAL ENGINEERING DEPARTMENT

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Acknowledgements

I would like to thank Professor Derickson for his help in advising me throughout the life of this project. I would also like to thank Chris Chicone for helping me use the photonics lab system to test my project. In turn thanks to all who helped whether it be bouncing ideas around or actual help building.
Abstract:

In this project I will be receiving two optical inputs from a tunable laser. As well as a Data valid signal that will indicate if my circuit should read inputs when valid or if the signal is not valid my circuit should hold until a valid signal is reapplied to avoid false zero crossings. The output of my circuit should be a digital signal that has a rising or falling edge when the two optical inputs have a zero crossing. This output will be a clock trigger that will input into the optical receiver of the overall optical coherence tomography system. Overall the system will be an optical to electrical converter that outputs a clock trigger to the receiver.
Introduction

In modern times there are many uses for optical coherence tomography (OCT) such as art conservation and diagnostic medicine. In particular OCT is used for imaging of biological tissues in varying medical fields. OCT uses optical beam that is shot into a sample and the reflected light is collected and used to form an image at very low depths. The OCT imaging process is especially useful since it provides higher resolution, three-dimensional imaging, and no damage is accessed by using OCT.

This senior project entails the use of an optical to electrical converter that will be used to signal when to receive optical signals in an OCT. These optical signals will be two varying sinusoids that are offset by two different phase angles from lasers. These signals will be received by respective photo detectors that will convert the optical signal into electrical current. This electrical current is then transformed into electrical voltages using transimpedance amplifiers. These voltages are then subtracted from each other and any time there is a zero value this sends a trigger to the receiver of the OCT.

In addition to triggering the OCT receiver when there is a zero crossing the optical to electrical receiver must have time gating features. This is due to the fact that the tunable lasers used in the OCT have transition switching times of 50 ns when the lasers are in an unknown mode. The times when the lasers are in the unknown mode there is a data valid signal with TTL logic levels. When the data valid signal
states the lasers are in the unknown mode the optical to electrical receiver must hold its state. Once the data valid signal states the laser is back in the known mode the optical to electrical receiver must start reading again from the hold state.
**Background and Conventions**

The first component of the optical coherence tomography (OCT) is the lasers that are typically use near-infrared light. This long wavelength allows the light to penetrate into any scattering medium. In this project the lasers that are being used are wavelength tunable sampled grating distributed Bragg reflector (SG-DBR) lasers. The SG-DBR lasers are usually tunable to 50 nm range. One of the unique attributes of the lasers used in this project is that they have concatenated “C Band” and “L-Band” SG-DBR lasers. This allows for the wavelength coverage to be increased from 50 nm to 100nm and the wavelengths that are encompassed by these lasers are 1525 nm to 1620nm. This concatenation is possible but with a transition time of 50 ns. Overall this added tuning length allows for enhanced distance resolution in OCT.

The second component in the OCT is the optical to electrical converter which tells the receiver when to receive. This part is important in attempting to figure out when the optical lasers are in the desired mode for reflectivity. These times are when the optical signal from the laser and the reflected signal have traveled the “same” optical length or a difference in length that is less than a coherence length. Secondary part of this application is that the transition time also must be accounted for. This transition time there might be false times when the receiver is signaled to receive. Therefore the optical to electrical converter must account and hold while the lasers are in transition mode. All these components added together with an optical receiver will create a functional OCT.
In this project one of the data types used in this project is Transistor Transistor Logic (TTL). This has a voltage range of 0V to some positive voltage usually around 5V. 0V is logic level low (Vol, zero) and the positive voltage acts as logic level high (Voh, one). This signal will be used in the data not valid signal to communicate to the optical to electrical converter when the lasers are in the transition mode. The output of the whole circuit will be using TTL logic.

There will a Transimpedance amplifier used in this circuit to transform the photodiode current to voltage that can be analyzed. Transimpedance amplifiers are given their name because they translate the output from a very high impedance current source to a low impedance op amp output or voltage. The bandwidth of the Transimpedance amplifier is inversely proportional to the gain. In this projects case that will be an issue as a big gain is needed as well as high bandwidth.

Another circuit element will be a difference amplifier that will be used to take two voltages and turn into a single voltage output. The difference amplifier has two inputs into the two input terminals. The signal input into the positive input will be subtracted by the input into the negative input. If you make all the resistors the same there will be no gain just a simple subtraction. This leaves the output with a low impedance single voltage.

The final circuit element used in this project will be a comparator. This device simply put changes an analog signal to a digital signal. This means one varying input signal is compared to either another varying input or a dc value input. In this project the one varying input will be compared to ground(zero volts). The
comparator will output high or Voh if the varying signal is above ground and will output low or Vol if the varying signal is below ground. The output will be in TTL logic.
Requirements
1. Receive input signal from tunable lasers and meet required bandwidth to properly convert signal to voltages.
2. Detect when zero crossings occur from two input signals.
3. Send clock signal to optical receiver of OCT that correlates to zero crossings.
4. Hold the present state when data not valid signal is low and once data not valid signal goes high continue from the same state.
Design

Optical to Electrical Converter Block Diagram

Figure 1: Block Diagram. Photodiodes will be used to translate the optical laser signal into a current signal. This current signal will be converted to a voltage signal. After that the two voltage signals will be converted to single signal. This signal will then be compared with ground to determine when zero crossings of the input signals has occurred. After that the signal will be a clock output with TTL logic and will need time gating feature to hold the signal when laser is an unknown mode.
Circuit Schematic

Figure 2: Schematic. The current source in the schematic is used to simulate the functionality of the photodiode. Then we have the transimpedance amplifier which will convert the current into voltage with a gain of about 33000. Then the two signals will be put into a difference amplifier that will subtract the signals and convert to a single voltage signal. Then the comparator will be used to create a rising or falling edge when the voltage signal has a zero crossing.
Simulation

Figure 3: Simulation Results for DC Circuit. With two anti-phase sine wave inputs and this is the comparator output for five periods.
Test Plans

Bandwidth Test

The first step in testing this circuit is to test the op amp that is being used as a Transimpedance amplifier for its bandwidth capability. To determine the bandwidth you must test the Transimpedance amplifier with varying frequencies to clearly see if all frequencies are being transmitted without any attenuation. In order to properly test the bandwidth a function generator must be used that runs a frequency sweep. First set the start and stop frequencies and in our case we used the full range of frequencies. The start was 0.1µHz and the stop frequency was at 20MHz.

![Bandwidth Test Schematic](image)

**Figure 4:** Bandwidth Test. Schematic of Bandwidth Test for each Transimpedance amplifier stage.

![Frequency Sweep Input](image)

**Figure 5:** Frequency Sweep Input. Input from Function Generator to test Bandwidth. This frequency sweep goes from DC to 20MHz range using a log scale.
DC Test

The secondary test is to make sure that once built the circuit has an accurate ground plane due to the high frequency range of use. Simply solder the circuit properly and excite the circuit while measuring all the individual ground connections. This process may be repeated numerous times throughout testing to ensure electrical connections are intact.

After ensuring that ground is connected properly a simple DC test is usually ran. This test is done to verify that the output of the circuit with varying inputs matches the simulations that were run for this circuit. The DC test has three different types to ensure complete working condition: Test 1 excite Transimpedance amplifier 1 and ground Transimpedance amplifier 2. Test 2 ground Transimpedance amplifier 1 and excite Transimpedance amplifier 2. Test 3 excite both Transimpedance amplifier.

![DC Test Circuit](image)

Figure 6: DC Test Circuit. This is the circuit used for DC test to simulate approximately 100μA as the input into the two Transimpedance amplifiers. T1 is transimpedance amplifier 1 and T2 is transimpedance amplifier 2.
**Final Test**

In the final test the total functionality of the circuit will be tested. This will include using two sine waves that are anti-phase as inputs to the respective Transimpedance amplifiers and also a data not valid signal as an input into the latch of the comparator. These inputs will be varied from DC to the highest frequency possible using an arbitrary waveform generator as shown in Figure 6.

In order to input two exactly anti-phase sine waves you must have an external trigger that is used by the two function generators. This was done by using another function generator as a square wave generator and attaching the output to the external trigger input of the function generator used as the input into the circuit. Once that is accomplished you take data with data not valid signal high and low to ensure the latch is working properly.

![Figure 7: Final Test Circuit. Final test layout with all inputs attached and output hooked to an oscilloscope.](image)
Development and Construction

In the development of this project there are very few components needed. This allowed for a simple construction. The circuit was built using a using point to point construction method where IC’s were place upside down and soldered in the air above the ground plane. This soldering was straight forward but due to the high frequency capabilities required for this circuit the IC’s were very small. This did cause complications as fine tip soldering tools are difficult to find. After many attempts and minor issues the circuit was constructed as shown in Figure 2 circuit schematic.

Figure 8: Soldering. This is the Physical board that was built. Here the final solder is being applied to bypass capacitors.
Test Results

Bandwidth Test
In running the Bandwidth Test there are many factors that are taken into consideration. The largest restriction on the Bandwidth of the Transimpedance amplifier is the bandwidth of the op amp itself. In this case our op amp the AD8047 has a small signal bandwidth of 250MHz and a large signal bandwidth of 130MHz. These are huge bandwidths and with the optical data that we are expecting this should work properly.

The final Bandwidth variable that must be taken into consideration is the resistance of the Transimpedance amplifier and the capacitance of the photodiode. In the case of this project the photodiode had a capacitance of about 0.8pF and the resistance used for the Transimpedance amplifier was 33k ohms.

$$\text{Bandwidth} = \frac{1}{R+C} = \frac{1}{33 \times 10^3 \times 0.8 \times 10^{-12}} = 37878787878 Hz.$$ This is approximately 37MHz which once again proves that the Transimpedance amplifier should be able to meet the full bandwidth of the function generator at 20MHz.
Figure 9: Bandwidth Test for T1. The oscilloscope capture of the frequency sweep from DC to 20 MHz and as is clearly visible all the frequencies are transmitted without attenuation.

Figure 10: Bandwidth Test for T2. The oscilloscope capture of the frequency sweep from DC to 20 MHz and as is clearly visible all the frequencies are transmitted without attenuation.
**DC Test**

In the DC Test the circuit was configured as seen in Figure 10. There was a constant voltage of 2.2V applied at Vin and data was taken at V1, V2, V3, and Vo as shown for the varying test in Table 1. Test 1 is when the circuit is connected as shown in Figure 10. Test 2 is when the circuit is configured with Vin connected to T2 side and T1 input is grounded. Test 3 is when the circuit is configured with Vin connected to T1 side and T2 input is grounded.

![Circuit Diagram for DC Test with labeled Nodes. Variation for the different test just determine how Vin is connected.](image-url)
The outputs of V1 and V2 proved that the Transimpedance amplifiers were achieving the gain that was expected. The output of V3 shows how the difference amp was applying no gain and V1-V2=V3 with minimal error. The final output Vo was the comparator output which should vary from Vol = .25V and Voh = 3.8V. The values of Vo also proved that the comparator was functioning as expected in DC frequency range.

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Table 1: DC Test Results. This is the results for the DC Test for the varying Vin input connections. As can be seen from the data the circuit is working as expected.
**Final Test**

In the final test the two anti-phase sine waves were used as the inputs into the circuit and a TTL logic signal was used to vary the latch from applied or unapplied. The two anti-phase sine waves were tested using the frequencies from 1Hz to 1 MHz in decade intervals. The latch was not applied for the first set of data. The second set there was 3 periods of the anti-phase sine waves that the latch was not applied and there were 2 periods were the latch was applied. The external trigger was used to create a pulse from the two arbitrary wave form generators that would result in the 5 period anti-phase sine wave inputs as shown in data. The screen capture data that was found had arbitrary axis used so I used the oscilloscope markers to gather pertinent information.

![Image of two anti-phase sine waves](image)

**Figure 12**: Two anti-phase sine waves. These signals were repeated for 5 periods total in the test. These were varied from 1Hz to 1MHz in decade intervals of frequency.
Figure 13: 1Hz anti-phase sine waves input latch not applied. In this circuit you see five pulses which indicate that the circuit is working properly. The first and last zero crossing is repressed but all the rest pass through. The Vol = .25V and the Voh = 3.81V. The horizontal axis is 2s per division which is about the same frequency as the trigger in this figure.

Figure 14: 10Hz anti-phase sine waves input latch not applied. Once again five pulses indicate the circuit is working properly with the latch not applied. The Vol=.25V and the Voh= 3.875V. The horizontal axis is 400ms per division.
Figure 15: 100Hz anti-phase sine waves input latch not applied. Five pulses indicate the circuit is properly finding zero crossings. The Vol=.25V and the Voh=3.875V. The horizontal axis of the capture is 10ms per division.

Figure 16: 1kHz anti-phase sine waves input latch not applied. Five pulses indicate the circuit is properly finding zero crossings. The Vol=.32V and the Voh=4.31V. The horizontal axis of the capture is 1ms per division.
Figure 17: 10kHz anti-phase sine waves input latch not applied. Five pulses indicate the circuit is properly finding zero crossings. The Vol=.25V and the Voh=4.875V. The horizontal axis of the capture is 40μs per division.

Figure 18: 100kHz anti-phase sine waves input latch not applied. Five pulses indicate the circuit is properly finding zero crossings. The Vol=.25V and the Voh=5V. The horizontal axis of the capture is 10μs per division.
Figure 19: 1MHz anti-phase sine waves input latch not applied. Five pulses indicate the circuit is properly finding zero crossings. The Vol=.25V and the Voh=5.5V. The horizontal axis of the capture is 1µs per division. The fact that Voh=5.5V is above the rail this means that this is some capacitive loading that is affecting the circuit at high frequency, but it still is working properly otherwise.

Figure 20: 1Hz anti-phase sine wave input latch applied 2 periods. Three pulses indicate the zero crossings are working properly and the latch is working properly to eliminate the last two pulses. The Vol=.25V and Voh=3.81V. The horizontal axis is 1s per division.
Figure 21: 10Hz anti-phase sine wave input latch applied 2 periods. Three pulses indicate the zero crossings are working properly and the latch is working properly to eliminate the last two pulses. The \( V_{OL} = 0.25 \text{V} \) and \( V_{OH} = 3.81 \text{V} \). The horizontal axis is 100ms per division.

Figure 22: 100Hz anti-phase sine wave input latch applied 2 periods. Three pulses indicate the zero crossings are working properly and the latch is working properly to eliminate the last two pulses. The \( V_{OL} = 0.25 \text{V} \) and \( V_{OH} = 3.81 \text{V} \). The horizontal axis is 4ms per division.
Figure 23: Trigger Pulse Output. This capture just shows how the trigger is working to excite the circuit for the pulse outputs.

Figure 24: 1kHz anti-phase sine wave input latch applied 2 periods. Three pulses indicate the zero crossings are working properly and the latch is working properly to eliminate the last two pulses. The Vol=.25V and Voh=3.81V. The horizontal axis is 400µs per division.
Figure 25: 10kHz anti-phase sine wave input latch applied 2 periods. Three pulses indicate the zero crossings are working properly and the latch is working properly to eliminate the last two pulses. The Vol=.25V and Voh=4.37V. The horizontal axis is 40μs per division.

Figure 26: 100kHz anti-phase sine wave input latch applied 2 periods. Three pulses indicate the zero crossings are working properly and the latch is working properly to eliminate the last two pulses. The Vol=.25V and Voh=5V. The horizontal axis is 10μs per division.
Figure 27: 1MHz anti-phase sine wave input latch applied 2 periods. Three pulses indicate the zero crossings are working properly and the latch is working properly to eliminate the last two pulses. The Vol=.25V and Voh=5.31V. The horizontal axis is 200ns per division.
Manufacturability and Sustainability

This project has a very good chance to be manufactured and it actually would work better if it was manufactured. This would allow for smaller IC size which is how the devices needed to build this product tend to come. The layout would be improved compared to the point-to-point construction. All this would lead to less capacitive coupling and in turn a cleaner output at even the highest frequencies.

The price of these products are very reasonable and I think in total I spent $28.37. This was with one extra part that I didn’t use so it would be reasonable to say that you could build this circuit from $30 and $60 at maximum. This would be very cost effective if someone was looking for a low cost optical to electrical converter. The parts used in my circuit were very replaceable and if one was discontinued it would be a simple to find another. I would not be surprised to see this manufactured in some way or another already though.

Environmentally this project has the problems of lead in components. Also the lead found in most solder. If these two parts are properly disposed it would be considered environmentally friendly. It is small and compact and therefore doesn’t require large amounts of energy to build which might harm the environment.
Conclusion

In the end the project turned out to be a complete success as we were able to build a circuit that could detect zero-crossings and create a clock output at all different types of frequencies. The results were only limited by the fact that we did not test with the photodiodes hooked up but simulated the functionality by creating a current source. This made testing much easier and also troubleshooting was much easier. The only drawback was the actual bandwidth of the optical signal was not able to be tested.

Some of the challenges I faced along the way were when I was attempting to find high frequency components this made finding big enough parts to solder very difficult. I bought a part and realized after many hours of failing that soldering a component that small is too difficult. So it took a lot longer to find parts that could meet the specifications but still be large enough to solder point-to-point. Using a PCB board would probably eliminate this problem as minimal soldering would be required.

Overall functionality the circuit worked perfectly and the final steps before this can be inserted into the OCT would be to add the photodiode. Test using this configuration and possibly creating a PCB board for better connections. Aside from that this circuit is ready to give the A/D converter its clock signal to allow for a proper OCT scan.
Bibliography

Brandon George and Dennis Derickson. “High-Speed Concatenation of Frequency Ramps Using Sampled Grating Distributed Bragg Reflector Laser Diode Sources for OCT Resolution Enhancement”. EE Department Cal Poly. 2010


Appendices

Specifications

- Average optical input power: 1-100 $\mu$W
- Optical input wavelength: 1550nm
- Data valid TTL level: 3.8-5V
- Data not valid TTL level: 0.25V
### Parts lists and cost

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**Various Capacitors, and resistors**

**Total** $28.37
## Schedule - time estimates

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