Hardware Verification Testing the Third Generation CiNIC

A Senior Project

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Abstract

The third generation NetPRL CiNIC co-processor cards were fabricated and partially assembled during Summer 2005. Unfortunately the prototype network processing hardware was incomplete, untested, and could not yet be used by NetPRL project teams as a firmware and software development platform. This project endeavored to prepare the latest CiNIC for use in advancing iNIC related research at Cal Poly.

The project began with the assembly and modifications necessary to complete the co-processor card. During assembly several manufacturability design issues were corrected or workarounds developed. Preliminary hardware verification testing was also conducted from continuity checks, power and smoke test, and hardware programming demonstration. The latest CiNIC prototype design is partially functional but many features are not yet proven and require additional testing.
Acknowledgments and Special Thanks

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Cain McDonald provided essential assistance in learning about the CiNIC architecture during the first quarter of this project and went out of his way to help with assembly. Thanks to my partner Henry Hu for the many hours spent assembling, testing, and researching to see this project through to the finish. And finally thanks to Matt Bates, Michael and Brian Bessette, and the other current NetPRL project students for listening to the issues we faced and offering your ideas. Finally, Solectron Technical Center for donated time and experience on X-ray imaging and ball grid array package replacement.
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1 Introduction

The focus of this project is the final assembly and hardware verification testing of the third generation CiNIC (Cal Poly Intelligent Network Interface Card) co-processor boards. The project goal was to demonstrate the readiness of the manufactured CiNIC board as a firmware and software development platform for Cal Poly Network Performance Lab (NetPRL) projects.

The purpose of hardware verification is to determine whether manufactured hardware meets or exceeds the specifications of the design and to discover any errors made in the manufacturing process. Electronic and computer hardware manufactured in volume is typically tested with several special machines that are setup to quickly test the hardware with continuity probes, burn-in operation periods, powered operation tests, X-ray images, and human or computer visual inspection. Prototype hardware is often inspected and tested by hand since these high volume test methods require significant cost to configure for several uses. The third generation CiNIC was tested and inspected with a variety of these methods both by outside vendors and in the lab at Cal Poly.

There were two of the CiNIC boards partially assembled following the final printed circuit board design and assembly preparations made in Spring 2005. The boards were not complete when received from the manufacturer due to several failures to follow manufacturability requirements in the design. Since the incomplete boards could not be powered and tested, it was necessary for the hardware verification team to complete the board assembly first and then conduct testing procedures.
Design validation is the process of demonstrating that correctly manufactured hardware meets the operating requirements for the purpose it was designed – to determine if the design is a valid solution for the application. Although this project intended to conduct validation testing of this CiNIC design, complications arose in the hardware verification phase which prevented more thorough testing of the hardware functionality. This has been left to future projects; at the completion of this project one CiNIC co-processor board is fully assembled and partially functional, but the second board remains incomplete.

2 NetPRL CiNIC Project Goal

The Cal Poly Intelligent Network Interface Card is a proposed solution to the steady increase in the processing loads of high speed network communications. The CiNIC provides a hardware based network protocol stack processing solution to assist a host system by performing many of the necessary data manipulation tasks prior to the host system receiving the data. The purpose of the CiNIC is to reduce software latency on the host system by freeing resources for other processing tasks under high loads, and if possible to reduce network latency in the process [5].

The CiNIC co-processor architecture supports the development of a general interface which is required before acceptance of similar devices in the mainstream market is realized.

3 History of the NetPRL CiNIC Architecture

3.1 First and Second Generation CiNIC

The first generation CiNIC was based on an EBSA based device chain connected to a PCI-to-
PCI bridge serving separate devices on a secondary PCI bus to appear as one device to the host system [1]. This architecture used Linux kernel device drivers to hijack the network stack and redirect CiNIC connections to this pseudo PCI device.

For the second generation CiNIC, a PLDA FPGA based development board was used to handle processing duties and a standard Ethernet NIC was connected to the board via the PCI Mezzanine interface. This architecture used software based protocol processing on the development board and followed a similar host kernel driver design from generation one.

3.2 Third Generation CiNIC

Design of the third generation CiNIC was done in large part by Kurtis Kredo II in 2004 [2][4], as the focus of his Master's thesis in Electrical Engineering. The latest architecture is a prototype FPGA based development board designed entirely at Cal Poly. The CiNIC was designed to provide better performance by implementing the network stack processing directly in hardware, with a supporting Xilinx MicroBlaze softcore processor for very flexible programming options [2]. The host system interface was also redesigned for the third generation to define the co-processor interface and implement the supporting network protocol on the host system rather than hijack the host network stack by redirecting CiNIC traffic [3].

The CiNIC design includes 341 components including two FPGAs and 14 other ICs attached to one side of a ten layer board. The primary processing FPGA is a Xilinx Virtex XCV1000. There are two common ground planes (layers), two different power planes (one at a voltage level of 3.3V and one at 2.5V), and six signal layers including the top and bottom exterior layers
arranged as shown in figure 1. The board is rectangular with overall dimensions of 5.5” wide by 11” long, and is designed to support a PCI version 3 interface with standard PCI fingers protruding on one side.

Figure 1. CiNIC PWB Stackup (layer arrangement, board cross section)

This card is part of a two card system that makes up the CiNIC hardware architecture. The design requirements of the architecture changed following Kredo's work and the design was modified to use two identical cards, programmed differently, rather than one card with both FPGAs and another processor island board [4]. The two cards are designed to work together to process inbound and outbound network traffic for one link. Both cards would have operational PCI buses for communication with the host computer system, and have several communication channels to the other card through ribbon cabling. Each card is able to access some memory and processor I/O signals of the other to enable them to transfer data during operation and avoid any unnecessary host system interaction.
Figure 2. CiNIC board one (fully assembled)

The major subsystems present on the board are identified in figure 3 by their respective numbers shown: primary FPGA (1), SystemACE configuration module (2), power supply (3), SODIMM memory (4), Ethernet (5), serial communication (6), SRAM memory (7), and PCI interface (8).

Figure 3. CiNIC subsystem locations
4 Final Hardware Assembly Process

4.1 Assembly Preparation – Understanding the CiNIC Architecture

Before undertaking the final assembly of the boards it was necessary to gain an understanding of the overall design including the type of components used, their general purpose, and placement locations. Cain McDonald provided a short introduction into using the Orcad Layout PLUS software to view the final board layout and gave a guided tour of the schematic in the Orcad Capture CIS design software. He also helped to identify components on the board, their locations in the schematic and layout, and their purpose in the design. Additional study of the schematic was necessary in order to quickly recognize components, their reference designators, and to identify the subsystem to which they belong. We also studied the conceptual design documentation in Kurtis Kredo's thesis [2], and read through Kelly Woo's senior project [4] on the printed wiring board (PWB) layout design and fabrication preparations. More information about the design of the hardware can be found in their respective reports.

Cain completed an updated copy of Kredo's original design schematic as part of his work with NetPRL which became the design schematic used for the layout. This schematic is all on one large page and is divided into isolated groups of components which make up the major subsystems of the design (see CD). A component list was created for the entire board from the schematic. The full component list was then broken into subsystems so that is was possible to identify what components would be necessary in each subsystem to assemble operational units on the board if the complete design could not be built. The incomplete state of the boards at the beginning of the project is shown in figure 4.
The component list was updated after examination of the current board state to indicate whether each component was present or missing, correctly oriented, or otherwise visually flawed. From the full component list we obtained a subset of the components which would require assembly in the lab at Cal Poly which included 89 capacitors, 4 resistors, 1 resistor network, 4 switches, and 23 headers per board, among others. Some visible flaws with the assembled board were noted at this stage including one incomplete header hole pattern and several solder-filled mounting holes (see section 6.1). The required parts list is shown in appendix E. All necessary components to complete one board were found in the available stock purchased for the initial assembly, as well as most of the components needed for the second board.

Accompanying the boards returned to Cal Poly was the vendor's *design for manufacturability* (DFM) report which noted each component they were unable to place and associated reasons or design flaws (see appendix B). The hardware team was not aware of this report's existence when this project was begun, so some of the information it contained we discovered for ourselves
when we attempted to finish the board assembly in the lab at Cal Poly. We later obtained this report from Dr. Jianbiao Pan, who was unaware we had not seen it. The DFM confirmed some of our findings regarding the reasons for the incomplete assembly.

4.2 Assembly Process

The assembly process was the next major hurdle in completing the project. At the suggestion of the faculty and other students involved in the project it was decided to build one board first and begin testing the hardware prior to completing the assembly process for the second board. Since the board design is modular in nature it would be possible to build the board with some subsystems deliberately isolated or incomplete in case a critical flaw in the design was found. Another reason to proceed with assembly at separate times was to allow for assembly process mistakes which could damage sensitive components already on the board.

The CiNIC design requires an assortment of surface mount technology (SMT) components and pin through hole (PTH) components all on one side of the printed wiring board. The Cal Poly SMT lab does not have the necessary equipment to assemble both types of components in one process, so these would be handled separately. First, most of the SMT components would be placed and soldered to the board, then all PTH components would be inserted and hand soldered. Finally any special case solder rework would be done to fix bridges or issues with the SMT placement.

The CiNIC design incorporates two ball-grid array (BGA) IC packages which house field-programmable gate-array devices (FPGAs) and several fine-pitch ICs. These packages were already placed on the board and soldered. BGA packages require precise placement and careful
handling when soldered to prevent bridging of the close solder ball connections underneath while the solder is molten. Since reflow soldering would be used in our process, and this would risk creating bridged connections which should not yet exist, the faculty advised that the assembly process should only reflow each board once during assembly. All missing SMT components would be placed at once and then the board would be sent through a reflow soldering oven only one time. For all other soldering necessary heat would be minimized near these components.

4.3 SMT Component Assembly

Most of the components to be placed were SMT components. The components are difficult, if not impossible, to hand solder due to their small size and close proximity. These would be placed prior to PTH components in a typical SMT process involving three main steps: solder paste application, component pick and placement, and reflow soldering. Since there were some components already placed on these boards a modified process would be required which suited our project.

Solder paste is typically applied to a PWB using a screen printing process where solder is pressed through holes in a stencil to apply solder paste only to the pad locations on the board where components will later be placed. The solder paste used in this process is a mixture of small solder alloy particles in a high viscosity flux paste. The flux contained in the solder paste acts as a surface cleaning agent when heated to remove organic and oxidation contaminants from the surface of metals to be soldered. The high viscous fluid paste also acts as a temporary adhesive for SMT components during the assembly process.
Since this board was partially assembled it would be impossible to use a stencil to apply the required solder. After consulting Dr. Pan on the original assembly process used it was determined that the board had a light volume of solder present on the pads for all missing components since the board had previously been stencil printed. Although some solder was already present on the board it was already solidified in the previous reflow soldering process and could not provide the tacky adhesion necessary to temporarily keep components in place. At Dr. Pan and Cain's suggestion a manual solder dispensing process would apply a very slight volume of solder to each pad as a temporary adhesive, but the volume applied must be low to avoid solder bridges due to excessive solder buildup on those component terminations.

We had two possible methods to apply the solder and tested each to determine which would provide better solder joints: hand-guided blunt instrument application, and air-pressurized syringe application. Application of the solder by hand using a blunt instrument proved too difficult to control consistent solder volume on the pads of the smallest components which are 0603 (60 mil x 30 mil) chip resistors. Instead, the Gold Place manual pick and place machine would be used. This machine has an air-pressure assisted syringe solder dispenser, but no solder syringes were available for this application. One syringe of rosin-free no-clean solder was donated to the university for use on this project through an IME department industry supplier. Solder paste must be maintained near room temperature during component placement, so the process of solder dispensing was quickly followed by component pick and placement.

In an automated pick and place process a machine would be programmed to pick up each component from tape and reel, tray, or tube dispensers using a vacuum nozzle and then
accurately place it on the board in the correct location. These fully automated pick and place
machines can operate at high speed, often finishing very complex boards in a matter of minutes.
However, these automated systems require a significant amount of programming and setup time
which is wasted on a single board run. The machine must also calculate a placement path which
allows the vacuum nozzle to move without collision with the board, and this is a complex
problem on a board that is not blank. For a single or low volume prototype assembly process
either a manual or semi-automatic pick and place machine is typically used instead. The SMT
lab at Cal Poly houses one manual machine, and one semi-automatic machine.

For the CiNIC assembly the Gold Place manual pick and place machine would be suitable, but
would require several hours of patient work. Each SMT component required would be picked up
on the vacuum nozzle, its intended placement location checked against the component list and its
reference designator verified to ensure the correct part is used, its orientation matched to the
board, and then placed as accurately as possible on the pads before the component list was
updated. During the pick and place process a design issue was discovered with an incorrect land
pattern for the SODIMM memory sockets which precluded placing these sockets.

After all SMT components were placed on the board it was ready for reflow soldering. A reflow
soldering oven uses a conveyor belt to slowly carry a PWB through several heated zones where
varied temperatures provide three or four phases of soldering: slow heating (and sometimes a
separate heat soak), solder reflow, and cool down. The board is slowly heated until the solder is
near melting temperature and all components are evenly heated, then the solder reflow phase
spikes the temperature to melt the solder and allow viscous flow before the cool down phase
solidifies the solder making electrical and physical connections.

The Cal Poly SMT lab contains a Heller EXP1500 reflow soldering oven which is adequate to handle the width and length dimensions of the CiNIC board, however vertical clearance in the oven for the components already placed on the board was not checked prior to the pick and place process. The RJ45 MAG jack for Ethernet connectivity had been soldered to the board but was too tall to fit in the oven and had to be removed before the reflow process. Fortunately most of the lighter weight unsoldered components remained on the board due to the tacky solder paste when it was inverted to remove the jack and only a few of the larger capacitors needed to be placed again. The reflow soldering process took roughly five minutes and produced very satisfactory solder connections. None of the placed components required additional soldering.

4.4 PTH Component Assembly

Some of the components not placed by the manufacturer were PTH headers, power and serial jacks, power supply, and SMT switches. These were not placed for several reasons: DC power and serial jacks were reversed on the board layout and would face inward on the board rather than outward, PTH headers were not shipped to the manufacturer to be installed, the PWB design lacked mounting holes for the power supply heat sink, and the SMT switches were too small for their PWB land pattern.

In a typical fabrication assembly line PTH components are inserted into the board using a robotic arm with special tooling for each type of component. These machines are used only where PTH components must be assembled quickly on high volume production runs and otherwise are
generally replaced by human labor for manual insertion. Once the components are inserted in
the PWB they are soldered to the board either by hand soldering or wave soldering. There is no
wave soldering machine available for our use in Cal Poly’s labs, so these components were
soldered in place by hand. Although this process is time consuming it is not difficult or
dangerous to the board or other installed components unless excessive heat is applied to any one
area of the board.

Special consideration was required for the DC power jack and serial communication jack since
the through holes for these parts were oriented 180 degrees from the intended design. In order
for these jacks to be useful they must be mounted with the external jack facing away from the
board edges for clearance to connect a cable to them. One solution would be for these parts to be
mounted on the reverse side of the board so that there would be ample clearance from other
components. However, this solution would cause additional problems for inserting the board
into a standard computer case as intended since the serial jack was meant to fit in the PCI slot
gap of one half inch alongside the Ethernet RJ45 jack and be accessible from the computer case
exterior. If the serial jack were placed on the bottom side it would be offset from the PCI slot
and would still only be accessible from inside the computer case.

The solution to the improperly oriented jacks was to fabricate interposer cards which would
rotation the jack 180 degrees and allow the jacks to face the board edges. Cain McDonald
quickly created a layout design for these small cards using Layout Plus since neither Andrew or
Henry knew the software well enough to do this. With Cain's guidance these cards were then
created using a single-sided copper-clad laminate sheet and chemical etch process.
Unfortunately an oversight was made on the interposer card for the serial port and we had insufficient clearance to the Ethernet RJ45 jack. We could not install the interposer card, so one side was cut down and a separate wire soldered in place where we lost a trace on the card. This situation was a good reminder that even with several people checking over a proposed solution it is easy to overlook what should have been obvious, and could have been more costly to remedy.

The final PTH component to install was the TI dual power supply which could not be placed due to the lack of heat sink mounting holes. The power supply has four large mounting studs at its corners which are intended to be soldered to the board for additional mechanical strength and heat transfer. It would be impossible to drill mounting holes in the PWB for this component since those holes would pass through all of the power and ground planes in the board without any etched clearance in the copper plane for the hole and might create direct power to ground shorts, as well as possibly breaking internal signal traces. This problem was avoided by bending the mounting studs outward at 90 degrees to create feet which would sit atop the PWB and still allow the component pins to protrude through the board and be soldered correctly. To provide adequate stability and mechanical strength some low-temp glue was applied to the feet against the board, and a bent sheet metal bracket was glued in place to help stabilize the top of the component. The only deficiency in this solution was a reduction in heat transfer from the power supply heat sink conducted to the board through the soldered mount studs which we deemed unlikely to cause any serious issue.

4.5 Final Rework and Routing

There were four SMT no momentary switches to be placed. The land patterns for the switches
had incorrect pitch such that the terminations on the switch body could not contact all four pads simultaneously. These were soldered by hand after the PTH assembly process. An excessive solder buildup around the terminations on the switch body bridged the gap from the body to the PWB pads.

The PWB shape had been routed by the manufacturer to the dimensions specified in the design, however the PCI slot finger was incorrectly sized to fit in a standard PCI slot. On both sides of the finger there was over one quarter inch of additional material left on the board which was removed using a hand-held Dremel motor and routing bit.

A second key was also routed into the PCI finger on the board. The PCI subsystem on the board was designed to work on a 3.3V PCI bus which follows the standard for PCI version 3. However, the design was also properly wired to work in a universal PCI slot which will allow either 5V or 3.3V operation depending on the voltage level present on the selection pin when power is applied to the card. All computers present in the NetPRL lab at Cal Poly have universal PCI slots rather than the newer version 3 slots which require a different key on the PCI finger.

To allow the PCI version 3 finger designed on the CiNIC to be used in a universal PCI slot it was necessary to route an additional key into the PCI finger which removed two unnecessary ground pins at the location of the version 3 slot key. The PCI standard definition was consulted to determine that removal of those two ground pins was safe.

The card was cleaned to remove debris from routing and flux residue from soldering. Flux
present in the solder used for hand soldering may cause corrosion on the solder joints, which
over time may bridge connections. The flux residue was removed using isopropyl alcohol and paper towels.

At this point CiNIC board one was fully assembled and ready for testing. The second partially
assembled CiNIC board was not yet modified up to this point since the team consensus was that
conducting initial power up tests on board one prior to buildup on board two would be more
prudent than moving ahead with board two. The plan was to finish the fabrication of board two
at a later time so that it would be possible to omit placement of components, or whole
subsystems, if necessary to prevent power up damage found when board one was tested.

5 Hardware Verification Testing

5.1 Continuity Tests

The first and most important test type to be performed on electrical equipment is to check for
continuity between test points which are expected to be electrically connected. In order to begin
these tests it is necessary to prepare a list of all expected connections, and to sort this list to
produce a database of individual point to point continuity tests to be performed for each type of
electrical connection on the board.

5.1.1 Preparing a Connection List

Preparing a list of all connections present on this board would be a daunting task if done
manually; fortunately, the Layout Plus software can prepare and output a complete list of all
component point to point connections in the design. The list created by Layout Plus has separate sections; one for component pins directly connected to each of the power or ground planes, and another section for all other signal connections. However the format of the list is very inconvenient for human reading and using it directly would make testing of one subsystem alone impossible since all the signal connections were in one large section.

To separate and resort the signal connections list into subsystems, Microsoft Excel was used to import the list from the comma separated text file into a spreadsheet. The result was a very messy spreadsheet since the format of the list had many newlines and tabs to limit the column width of the text file. A command line executed php script was used to quickly remove erroneous whitespace characters in the text file so that would be interpreted nicely in the Excel spreadsheet. After the spreadsheet connection list was created, we began separating the signal connections into their respective subsystems. Filtering the spreadsheet allowed entries that contained any reference designators associated with each subsystem to be copied to a new sheet. The resulting connection database has spreadsheets for each subsystem and shows the status of the connection on both of the CiNIC boards. The connection list format cannot be shown in this document, however it is stored for later projects use on the NetPRL server.

5.1.2 Continuity Test – Power Subsystem

The power subsystem on the CiNIC board incorporates four operating voltage levels: 5V DC supply from external jack or PCI, 3.3V power plane, 2.5V power plane, and 1.8V from a voltage regulator. To verify that the power subsystem was manufactured correctly it is necessary to test that each component requiring power supply is connected to the correct voltage level on the
correct pin.

Several test points were chosen for each of the appropriate voltage levels present on the board as shown in table 1. From these test points each IC power pin was tested to have continuity to the test point appropriate for that IC. We also tested that each of the voltage levels present on the board did not have any short to another voltage level or to the common ground planes. At this time the two BGA packages on the board were not fully tested for connection to the proper voltage levels as not all the power supply pins could be accessed. No continuity issues were found with the power supply subsystem on the board.

<table>
<thead>
<tr>
<th>Expected Voltage</th>
<th>Pin Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.8 V</td>
<td>U65.4</td>
</tr>
<tr>
<td></td>
<td>J29.1</td>
</tr>
<tr>
<td></td>
<td>U66.23</td>
</tr>
<tr>
<td>2.5 V</td>
<td>U66.6</td>
</tr>
<tr>
<td></td>
<td>U65.2</td>
</tr>
<tr>
<td></td>
<td>J11.B59</td>
</tr>
<tr>
<td></td>
<td>J29.3</td>
</tr>
<tr>
<td>3.3 V</td>
<td>U65.3</td>
</tr>
<tr>
<td></td>
<td>U66.7</td>
</tr>
<tr>
<td></td>
<td>J11.B22</td>
</tr>
<tr>
<td></td>
<td>J29.2</td>
</tr>
<tr>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>Power Jack 5V</td>
<td>J7.1</td>
</tr>
<tr>
<td></td>
<td>U66.13</td>
</tr>
<tr>
<td>PCI 5V</td>
<td>J11.B61</td>
</tr>
<tr>
<td></td>
<td>J11.B62</td>
</tr>
</tbody>
</table>

5.1.3 Continuity Test – Programming Subsystem

The CiNIC programming subsystem follows a Xilinx SystemACE reference design which uses a
re-programmable PROM to initialize and program a small FPGA to act as the SystemACE controller when the board is powered. The SystemACE controller then loads the selected main FPGA image from a non-volatile flash memory and programs the FPGA. The PROM and SystemACE controller are connected in a series chain with JTAG programming signal lines.

The intended programming method for the CiNIC was unclear when we began continuity testing for this subsystem. Although we determined that each of the JTAG signal paths had continuity from the CONNACE1 header (a connection point between the two cards when used in combination as designed) through to the PROM and SystemACE there was some confusion regarding where the JTAG cable would be connecting to the board. There is no location on the board where all six of the JTAG signals are available in the correct order on a PTH header. The header J15 had five of the signals available but they were not in the correct order, and the final signal was present on header J25. This appeared to be a design error that we noted for later programming tests. The programming subsystem did have viable continuity to all components involved in the chain.

5.1.4 Continuity Tests Not Conducted

The CiNIC board complexity required us to omit some test procedures that would typically be done to ensure that all hardware connections were correct. All signal connections should be checked for continuity from point to point between components, including checks to and from components which would not allow continuity unless the board was powered. This would require many hours to test each connection using a digital multimeter and individual leads.
Dr. Pan was consulted regarding the time expense in conducting all these separate signal tests. He assured us that the PWB manufacturer conducted internal wiring tests of the PWB after fabrication, and that we should assume the internal wiring of the board is a valid representation of the PWB design. In the interest of conducting power and programming tests sooner these tests were skipped until it becomes evident that the hardware contains signal path flaws.

Both of the BGA packages present on the board are Xilinx FPGAs. These components were not fully continuity tested due to the difficulty in accessing some test points on the signal paths to the BGA pads underneath the component. The power and ground connections to the FPGAs were later checked (after issues were found in power tests) using a blank copy of the PWB and were all connected correctly. The manufacturer provided X-ray images of the SystemACE FPGA on both boards which showed no shorts were present under those devices. We did not have any X-ray images of the primary FPGA BGA placements at this time.

5.2 Power On Tests

5.2.1 Smoke Test

When electrical hardware is powered any continuity issues such as direct power to ground short-circuits or incorrect voltage levels may cause damage to some components both visibly and internally. The first power test done is often called a 'smoke test' since short-circuits have a tendency to burn or overheat some of the organic materials used in the hardware.

The first power test was done using the DC 5V external power supply jack and a 1A rated power converter. When the power was turned on no smoke was observed and no components became
hot to the touch. We monitored the two power supply output voltages as power was turned on and noted that neither rose above 0.3V, but rather fluctuated rapidly from nearly 0V to around 0.3V. After reviewing the TI Dual Power Supply datasheet it was determined that the supply was behaving in short-circuit protection mode where it rapidly resets both output voltages and begins raising them again as soon as a short-circuit is detected. According to the datasheet however the short-circuit detection should occur at 13A draw on the outputs, and we were clearly not supplying that much current. We believed the external power supply we were using may not be providing adequate current for the transient draw that would be necessary in the FPGAs and nearby bypass capacitors, and this may in turn be triggering the short-circuit detection since the supply was incapable of raising the output voltage levels.

To test the behavior of the power supply with a slightly higher available input current a bench power supply was used to connect a 5V output directly to the input pins of the on-board dual power supply module, but bypassing the DC input jack on the board. The bench power supply was rated capable of outputting a 2A current at 5V which should be more than adequate for the requirements of the CiNIC board. When this power supply was turned on the input voltage to the board was steady at 5V and there was almost no current being supplied, yet the on-board supply outputs still did not rise above 0.3V and continued to fluctuate.

Since there had been no short-circuit issues found between the voltage planes on the board during continuity testing, and the on-board power supply was not known to work we suspected that there may be an issue with the supply design on our board. When we verified the reference design from Texas Instruments however, the schematic, layout, and datasheet all were consistent on how the power supply should be installed.
5.2.2 Isolated Power Supply Operation

Nothing more could be determined by testing the board with the installed power supply immediately triggering itself into short-circuit protection. Not knowing where to proceed at this point we returned to datasheets on the larger ICs and FPGAs on the board, as well as the power supply datasheet, to determine what could cause this behavior. There seemed to be no explanation unless a short-circuit actually existed on the board or inside an IC. The next objective was to determine if the power supply itself was damaged, but without removing it (which proved difficult later) we could not test it. Before attempting to remove the power supply a second unplaced part was tested where it could be isolated from board components.

The unplaced power supply was wire-wrapped to directly connect the groups of its 27 pins for input, two outputs, and ground. After some testing failures on this isolated power supply we discussed the situation with other members of the NetPRL team and realized that the power supply may be very susceptible to voltage transients on the input or output signals which could also trigger the short-circuit reset. We tested the isolated power supply without connecting bypass capacitors, however both the reference design for the power supply and the CiNIC design included bypass capacitors on input and outputs. Once the proper capacitors were included in the isolated system we observed steady output voltage levels on the power supply.

It was then necessary to remove the power supply placed on board one in order to test whether there was a failure in the power supply or in the board wiring. Removal was difficult due to the modified installation of the power supply which shortened the leads protruding through the PWB
and made wicking the solder out of the holes difficult. The leads were cut to remove the part, and most of the lead stubs left in the board were then easy to remove. The power supply operated as designed when tested off the board and showed no signs of short circuit behavior.

5.2.3 Current Limited Power On Test

Since the short-circuit issue was not caused by a damaged power supply there must be a problem with the board wiring, or a component installed on the board. Additional testing was done using an external bench power supply to determine if we could reach steady operating voltage levels on the board.

The bench power supply connected a 3.3V and 2.5V input directly to the board voltage reference points. This would allow us to test the two power planes separately to locate the short-circuit. The bench power supply was rated capable of outputting a 2A current at 5V. When this power supply was turned on the current meter on the 3.3V supply immediately registered above the 2A limit and the voltage meter registered an input voltage of under 1V, however no ICs became hot to the touch in the first few seconds. The test was repeated for up to a minute and still no signs of damage or excessive heat were seen. It was evident that the system was either consuming much more current than was anticipated, or there was a short-circuit present on the 3.3V power plane.

Although a 2A input current alarmed us at first we noted that the dual power supply installed on the board was rated to output a continuous 6A independently on its outputs, but the original design requirement set by Kredo was for a 3A rated power supply and the 6A supply was
substituted due to component availability. The board was never reaching its operational voltage levels, but there could be transient currents up to 3A drawn by the main FPGA at startup according to the component datasheets. The current draw observed was continuing much longer than it should in order to charge all the capacitors on the board and smooth out the transients in the FPGAs.

5.2.4 Chasing Down A Short-Circuit

The 3.3V power plane is connected to most of the ICs on the CiNIC board including the flash memories, FET switches on the PCI bus, and the primary FPGA I/O among others. The primary FPGA also uses the 2.5V power plane for its core voltage. A short circuit on this power plane could exist in any of these ICs, or in the wiring of the board itself.

The IC power related pin-outs were checked again, as well as the continuity on all the 3.3V power subsystem, but no shorts were found. The issue suspected of causing the short-circuit was an internally damaged IC. It was noted that the FPGA and several other components were shipped to the manufacturer without proper ESD shielded bags, and that this could have damaged any of these components prior to installation.

Another bench power supply was used for additional testing which would allow up to a maximum of 3A current supplied at 3.3V. This supply was connected and although the supplied current was limited at 3A the input voltage supplied to the 3.3V power plane fluctuated below 2V. After the board had been powered a short period (around one minute) we observed that the 3.3V power plane voltage began to rise very slowly while the consumed current remained at the
3A maximum until the voltage was almost steady at 3.3V.

We attempted to detect the primary FPGA with a boundary scan on the JTAG cable but no devices were detected. During this test the voltage on the 3.3V plane slowly crept above the designed operating voltage of the primary FPGA, reaching over 4V unnoticed. When the voltage was turned off, adjusted to 3.3V, and again connected to the board there was no longer a high current draw on this power plane. Instead the power supply registered less than 0.4A draw on both supply voltages as the board remained on for an extended period. The only possible explanation we have for the change in current behavior is internal damage to one or more ICs on the board, possibly including the primary FPGA which has a maximum operating voltage of 4V that was exceeded.

CiNIC board one was now powered with steady input and reference voltages and a low current draw, however it was possibly damaged in an unknown way. Since the mysterious short-circuit had disappeared, and the associated current draw was no longer present, the source of the problem could not be further investigated at this time.

5.3 Programming Tests
As previously mentioned, the programming signal paths on the CiNIC board are confusing. The PROM and SystemACE are connected in a series JTAG boundary scan chain, however the primary FPGA is not always part of this boundary scan chain. The primary FPGA can be included in the chain or omitted by using jumpers placed on three pin headers to determine where the chain ends. The primary FPGA can also be programmed directly by the SystemACE.
through a parallel programming path which does not use the boundary scan method, however some of the signal lines are common between these programming methods and cross in the J15 header and CONNACE1 header. To complicate things further the board design did not locate the six JTAG signal lines together in one header in the appropriate order for the standard cable.

To provide a usable JTAG cable connection it was necessary to wire-wrap the six signals for the PROM and SystemACE chain into a new header which could later be glued to the board surface. The primary FPGA chain signals were also wire-wrapped into a separate header for direct access to the FPGA. Initially the FPGA was not included in the new boundary scan chain for the PROM and SystemACE so that both of the FPGAs could be program tested separately.

These programming tests were done using Xilinx Impact 7.1. Although Impact detected the devices, and would program them, it displayed errors regarding the device IDs read from the devices. These errors can often be ignored when the proper device is configured in the development environment, and are the result of old device definition files. We attempted to modify the files to make the device IDs correspond but finally updated some of the definition files from Xilinx.

5.3.1 PROM
The PROM serves as a non-volatile storage for the SystemACE programming image. This is necessary for the board to program itself at power up since the SystemACE is a volatile FPGA which loses its program as soon as it is loses power. The PROM image contains a bitstream image for loading into the SystemACE FPGA which programs it to operate as a configuration
manager for primary FPGA. The default PROM image was obtained directly from Xilinx's support website.

The PROM was erased and then programmed with the new image. Once the board was reset and its power up complete, the SystemACE DONE LED turned on which indicates the SystemACE programming had completed. The PROM appeared to function correctly, but it was erased and re-programmed again to verify the result. Impact failed to read the current image from the device so it was not possible to compare the original image to the current device image.

5.3.2 SystemACE and FPGA image storage

The SystemACE FPGA was tested in two ways: programming a simple I/O image directly, and programming the Xilinx supplied SystemACE design image through the PROM. The SystemACE manages images for use in the primary FPGA by storing them into a non-volatile off-chip flash memory. An image is stored into the flash memory by selecting the appropriate image slot (out of four available) to replace and then programming into the SystemACE using Impact.

A simple I/O image was created for the Primary FPGA which would toggle an LED on when the system reset switch was depressed. This image was then programmed into the SystemACE as image 0, which stored it into the flash memory. The image again could not be read back from the device, perhaps due to the incorrect device ID errors displayed when the devices were scanned. When the board power was reset the PROM again programmed the SystemACE but
once the first DONE LED lit we observed no more activity to indicate the SystemACE had programmed the primary FPGA.

The SystemACE was also programmed with a simple I/O by erasing the PROM and then directly programming the SystemACE FPGA. A similar image was used for this smaller FPGA as for the primary FPGA which would toggle an LED based on the status of one no moment switch. The pin assignments for the VHDL signals were changed for this FPGA and to use a different LED and switch. The SystemACE FPGA programmed correctly and the LED toggle demonstration was successful.

5.3.3 Primary FPGA

The FPGA was never detected by the boundary chain scan and therefore could not be programmed directly. Unfortunately there was no indication that the FPGA was alive on the chain since no device was detected and the only errors displayed were failure to detect any device. When the FPGA was included in the full boundary scan chain with the PROM and SystemACE none of the three devices would be detected. The primary FPGA was not propagating the programming signals to complete the chain.

An attempt was made to program the FPGA through the SystemACE at power up as the architecture was designed, however this also failed to show any signs of success. The second DONE LED on the board never turned on after the SystemACE was configured by the PROM to indicate that the SystemACE had finished configuring the primary FPGA. This FPGA was not functional at all.
5.4 Post-Testing Rework

Consensus of opinion on why the FPGA failed to be detected and programmed was that either a short existed underneath the BGA package which was interfering with programming signal, or the FPGA itself was damaged. There were three suspected causes for damage: failure to protect the package from static discharge prior to installation, high voltage supplied to the FPGA I/O reference voltage pins during power testing, or signal voltage applied to no connect pins.

With Dr. Pan's assistance both the fully assembled and partial CiNIC boards were shipped to Solectron Technical Center for X-ray imaging of the BGA placement (to identify shorts present) and replacement of the component. We asked that the FPGA on board one be replaced since we believe it was damaged already, and the FPGA on board two only be replaced if shorts were found underneath it. The X-ray images taken of the board one BGA placement, both before and after rework was done, are shown in appendix C. Solectron identified no shorts in the images and the board one FPGA was replaced. We are grateful for the assistance provided by Solectron and the time donated by Sundar Sethuraman and any other employees who helped him.

5.5 Testing the Replaced FPGA

When the CiNIC boards were returned to Cal Poly from their X-ray and rework at Solectron, Henry Hu continued the testing phase. The remaining old power supply pin studs, from the cut-out power supply, were removed from the board and a new power supply was soldered in place. Henry then began working with the programming signal path to detect the primary FPGA on board one.
Now the JTAG boundary scan chain included the PROM, SystemACE, and FPGA. At first the FPGA could not be detected on the chain, however when the PROM was erased (and left blank) the FPGA could be detected. If the PROM was again programmed with the SystemACE image, which it would write into the SystemACE on board power up, then the FPGA would no longer be detected on the chain.

When Henry programmed the PROM, and then loaded the FPGA image into the SystemACE flash memory, the FPGA would not be programmed by the SystemACE on board power up. There are suspected problems with the programming signals from the SystemACE to the FPGA which have not yet been solved.

The FPGA was programmed directly after erasing the PROM and SystemACE. Operation of the FPGA was demonstrated by lighting one LED when one of the switches was depressed, in the same fashion the SystemACE was tested. This is a simple demonstration that only indicates that the programming was successful, but it provides hope that the hardware will be useful.
6 Design and Hardware Manufacture Review

6.1 Flaws in Layout and Design

The following flaws were found with the manufactured design which precluded the components involved from being assembled by the manufacturer and were all issues documented in the DFM review done by the manufacturer. Where applicable the workaround solution developed during assembly or testing is described.

- SODIMM socket footprint (components U6 and U24)

  The lead pitch of the PWB fab land pattern does not match the actual components which would cause bridging between leads if they were placed. There is also an incorrect pitch offset for the lower bank of leads in relation to the upper bank which should be only one-half pitch shifted rather than one and one-half pitch as seen in figures 5 and 6.

  Additionally the footprint has the mechanical mounting pads location reversed from the standard reference footprint; note the location of mechanical mounting pads in relation to the socket lead pads as shown in both figures. If the socket is rotated to match the mounting locations then the short and long lead banks are on the wrong sides. This issue has not been corrected by any workaround.
• CONNACE1 PTH header footprint

The PTH header for SystemACE connections between CiNIC cards has only vias present connecting to the signal traces rather than the correct size through holes. As seen in figure 7 there are only vias near the CONNACE1 reference designator (figure right side) where there should have been through holes similar to those seen for the other headers (figure top left). This header was an access point to programming signals for both the SystemACE and primary FPGA, however the JTAG signals are also accessible in the J15 header. No workaround has been made; if access to these signals is required fine wires could be soldered into the vias, but no connector can be used.

![Figure 7. CONNACE1 header footprint](image)

• DC power jack (component J18) is oriented incorrectly

The power jack should face outward from the board edge rather than inward. The PWB footprint should have been rotated 180 degrees from its current orientation. An
interposer card was fabricated to rotate the jack orientation to allow installation.

• Serial communication connector (component P1) is oriented incorrectly
  The serial connector should face outward from the board edge rather than inward. The PWB footprint should have been rotated 180 degrees from its current orientation. An interposer card was fabricated to rotate the jack orientation to allow installation.

• Component spacing for manufacturability
  Several components near the primary FPGA (U5) were not placed due to inadequate spacing to nearby components. The manufacturer requirements were not met to allow the automated pick and place process to locate these components. The components were placed by manually during our assembly process. Spacing requirements should be carefully observed when selecting component locations in a PWB design. Grouping similar components (tantalum capacitors, chip capacitors, chip resistors) in separate areas or aligned clusters would minimize spacing requirement issues.

• TI dual power supply (component U66) mount holes missing
  PWB footprint for this component did not include the standoff mount holes to secure the module to the PWB when assembled. To install the module these were bent to allow the PTH leads to protrude through the board enough for acceptable solder joints.

• FPGA No Connect and Special Use pins
  The required and general use pin assignments on configurable ICs should be strictly
adhered to in the schematic design. No connect pins must not be connected to any signal. The schematic design connected two of the Ethernet PHY chip configuration signals, MDIO and MDC, to no connect pins on the FPGA. These signals must be routed to other unused FPGA pins before the Ethernet subsystem will be operational, and the programming pin assignments must reflect the change when these signals are used. Special use pins such as temperature sense signal pins should be avoided whenever there are available general I/O pins.

• Incorrect reference designators for components C88 and C61

The silk screen reference designators for these two components were switched in the PWB layout. Component C61 is a 47μF tantalum capacitor whereas component C88 is a 0.1μF capacitor.

6.2 Suggestions for Improved Design

The following issues should be avoided in future CiNIC designs to ensure hardware quality and promote general ease of use for the finished product.

• Custom PWB footprints

When footprints must be created for components rather than using library supplied footprints careful review by more than one party is required. Component footprints should be compared directly to datasheet example footprint diagrams at full scale to identify mistakes in pin pitch or other dimensions. Test fitting the footprint general shape and size against the physical component could have identified issues in this design.
• JTAG programming path configuration headers
  The programming system should permit isolation of components suspected of failure. A
  set of header and jumper combinations should be used to allow testers to program each
  configurable IC in a chain, or isolated by itself. If isolation of the signals is not possible
  in between chained components then the programming system should not utilize a chain.

• Standard JTAG cable connection
  There should be a programming access header which has correctly ordered signals for the
  standard JTAG cable connection. If JTAG cable is not the programming method of
  choice then another standard cable configuration should be used so that available cables
  can be directly used with the hardware.
7 Conclusion

The first completed third generation CiNIC co-processor board has functioning power and programming subsystems. The primary FPGA can be programmed directly using the boundary scan method, however it cannot be programmed at board startup using the SystemACE configuration module to store a non-volatile image in flash memory. The parallel programming signals from the SystemACE to FPGA must be tested to identify the cause of this failure.

Further testing is necessary to determine if the other key subsystems of the CiNIC co-processor are working as intended, namely the Ethernet module and PCI interface. Without the functionality of these two subsystems the CiNIC architecture will not be realized using this design, however this board should be a useful development platform even if it is not complete.

Assembly of CiNIC board two should proceed whenever possible since there were no critical design flaws found through the verification testing up to this milestone.
Appendix A

Design for Manufacturability Review (page 1)

DESIGN FOR MANUFACTURABILITY (DFM) REVIEW AND FEEDBACK

<table>
<thead>
<tr>
<th>CUSTOMER</th>
<th>California Polytechnic State University</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASSEMBLY # &amp; REV.</td>
<td>N/A</td>
</tr>
<tr>
<td>FIRST RUN</td>
<td>Yes</td>
</tr>
<tr>
<td>KIT QUANTITY</td>
<td>2</td>
</tr>
<tr>
<td>PREPARED BY</td>
<td>Manuel Castro, Praveen Kumar Manjeshwar, Jorge Craik</td>
</tr>
<tr>
<td>PLANT</td>
<td>337, San Jose, California</td>
</tr>
<tr>
<td>DATE</td>
<td>09/12/2005</td>
</tr>
</tbody>
</table>

1. DOCUMENTATION
   a. Part references provided in the BOM was not available on the PCB fab. E.g. location U59 specified in the BOM is not available in the PCB fab.
      i. Recommendation: Review of the BOM must be conducted by the customer.
   b. Components provided by the customer is not mentioned in the BOM.
      i. Recommendation: Review of the BOM and components must be conducted by the customer.
   c. Assembly drawings were not provided by the customer
      i. Recommendation: Customer must provide assembly drawings prior to build.
   d. CAD file was provided by the customer. However, it was not useful.

2. PCB FAB & COMPONENTS
   a. Global and local fiducials are not provided on the PCB fab.
   b. Fab does not have any breakaways along its length.
   c. Components were received in bags, which were not ESD safe. Moreover, MSDs were not received in dry packs.
      i. Recommendation: Components must be stored in ESD safe bags. MSDs must be stored per J-STD-033 guidelines.
   d. Land pattern on location U60 has via openings, whereas the corresponding locations on the component had solder bumps [Figure 1]. During reflow, the solder paste and solder from the bumps will be transferred through this via opening creating an insufficient solder joint.

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i. Recommendation:

1. Short Term:
   a. Openings were plugged with solder and subsequently assemble BGA at rework station.
   b. Plug the openings with solder before assembling the PCB.

2. Long Term: Review fabs with vendor to replace vias with pads.
   e. Location P1 – Orientation of pin 1 on the fab must be rotated by 180° for the Serial port to face outside.

3. PCB ASSEMBLY PROCESS
   a. Location U6 (A&B) and U24 (A&B) – The pitch of the surface mount connectors does not correspond with that on the PCB fab.
      i. Recommendation: Review of the fab/component and drawings by the customer.
   b. U66 – Fab missing component standoff openings
      i. Recommendation: Review of the fab/component and drawings by the customer.
   c. C61 – Per BOM is 47µF Tantalum capacitor. But, land pattern does not conform to component size.
      i. Recommendation: Review of the BOM and fab by the customer.
Design for Manufacturability Review (page 3)

d. Components (Chips) in the vicinity of BGA at location U5, U60 must be spaced (preferred) 3.75 mm (150 mils) per Sanmina-SCI DFX guidelines for PCB assembly and test.
   i. Recommendation: Review of the fab design by the customer.

e. Components (Chips) in the vicinity of TSOP at locations U42, U43, U68 & SOIC U74 must be spaced (preferred) 1.25 mm (50 mils) per Sanmina-SCI DFX guidelines for PCB assembly and test.
   i. Recommendation: Review of the fab design by the customer.

f. Components (Chips) in the vicinity of QFP at location U1 and FQSOIC at locations U61, U62, & U63 must be spaced (preferred) 1.875 mm (75 mils) per Sanmina-SCI DFX guidelines for PCB assembly and test.
   i. Recommendation: Review of the fab design by the customer.

g. Clearance between components at J6 and PLUG must be spaced (preferred) 3.75 mm (150 mils) per Sanmina-SCI DFX guidelines for PCB assembly and test.
   i. Recommendation: Review of the fab design by the customer.

h. Components at locations C196 and C197 interfere with the placement of component at location J18.
   i. Recommendation: Review of the fab design by the customer

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Appendix B

X-ray Images of Xilinx XCV1000 FPGA Ball Grid Placement
(reference designator U5)

No shorts were identified by Solectron Technical Center in either placement.

Board One Before FPGA Replacement:

Figure 8: (top left)  
Figure 9: (top right)  
Figure 10: (bottom left)  
Figure 11: (bottom right)
Board One After FPGA Replacement:

Figure 12: (top left)

Figure 13: (top right)

Figure 14: (bottom left)

Figure 15: (bottom right)
Appendix C

Analysis of Senior Project Design

Project Title: *Hardware Verification Testing the Third Generation CiNIC*

Student's Name: Andrew J Farris  
Student's Signature: ______________________

Advisor's Name: Dr. Hugh Smith  
Advisor's Initials: _____

Summary of Functional Requirements:

The CiNIC is a programmable FPGA based network interface card. The purpose of this iNIC is to send and receive Ethernet based network traffic, handle network stack protocol processing in hardware, and communicate with a host system through a PCI interface to deliver data transferred. The current state of the device enables it to be powered and both the primary and configuration FPGAs to be programmed.

Primary Constraints:

This project began with a partially complete assembly with components not installed for unknown reasons. The first challenge was to determine why the device manufacturer had omitted these components, and then determine how to solve the associated design problems. The second significant challenge was conducting a thorough test of the complex prototype hardware to prevent unnecessary damage to components during the initial power cycle due to design flaws. The system had an electrical short which was difficult to isolate and resolve due to there being several untested ICs in the design that could not be removed.
Economic:

Original estimated cost of the CiNIC is unknown. The actual final cost of the CiNIC is unknown. Components damaged or replaced during testing are estimated at $250. The Bill of Materials used is shown in Appendix E. Additional equipment and shipping costs were $25.

Original development time for the CiNIC assembly was six weeks with an additional five weeks for testing. Actual development time was nine weeks for assembly with an additional eight weeks for testing, and a loss of two weeks in transit to outside vendors.

Environment:

The chemical etch process used in manufacturing PWBs is environmentally dangerous if chemicals are not disposed of properly. The manufacture of the various components used in this assembly pose many additional environment risks. The solder used on the assembly contains lead and should not be discarded in general purpose landfills or near drinking water supplies. The organic materials in the PWB and attached components should not be burned without ventilation and harmful gas containment.

Manufacturability:

The CiNIC uses a typical PWB manufacturing process, well developed assembly and soldering processes, and commonly available components. Manufacturing the CiNIC for widespread deployment would pose no technical difficulties once the design flaws were corrected. A lead-free solder fabrication process would be advisable to allow deployment of the product in countries requiring lead-free electronic assemblies for consumer products. The lead-free solution would also reduce the environmental impacts of product disposal.
**Sustainability:**

Maintenance of a commercially deployed CiNIC would include firmware update distribution which could improve features and performance. The CiNIC contains recyclable resources but they are not easily reclaimed. An upgrade to the software or firmware design would be trivial but the hardware cannot be changed or modified significantly. The materials used in the assembly are common and plentiful and in some cases can be recycled.

**Ethical:**

Some uses of network hardware are illegitimate or illegal, and distribution of this system may be forbidden if encryption technology is incorporated. This system could provide increased network capabilities to hostile entities for information warfare. If the system is flawed or insecure when deployed it could be the source of valuable information security leaks.

**Health and Safety:**

The assembly is a low voltage electrical component and poses no serious electrocution risk by itself, however improper installation could be potentially fatal. Materials used in the manufacture of the CiNIC assembly could pose a health risk if improperly discarded.

**Social and Political:**

Concerns regarding network dependence or addiction may be considerable for such a product but these issues are not caused by the technology. There are potential government and/or military markets for a product based on this technology worldwide.
Development:

New software was used for the project including Orcad Layout Plus, Orcad Capture CIS, and Xilinx Impact. The processes for SMT and PTH component automated assembly and soldering were new material studied for the project as well as single-sided chemical etch PWB fabrication. Current testing procedures and verification steps for assembled electronic hardware were a significant portion of the project development.
Appendix D

Bill of Materials – Components Not Placed by Manufacturer

Table 2: Component Necessary to Complete Assembly of Board One

<table>
<thead>
<tr>
<th>TOTALS:</th>
<th>Quantity in Stock</th>
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<tbody>
<tr>
<td>0.1u cap</td>
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<td>47u cap</td>
<td>45</td>
</tr>
<tr>
<td>470u cap</td>
<td>10</td>
</tr>
<tr>
<td>1.5k resistor</td>
<td>9</td>
</tr>
<tr>
<td>header 2x1</td>
<td>8</td>
</tr>
<tr>
<td>header 3</td>
<td>11</td>
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</tr>
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</tr>
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<td>u46 , Single header</td>
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<td>Sodimm socket</td>
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<td>Quad Nand</td>
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</table>

Additional materials used: ESD safe workbench mat, soldering iron, solder, one square foot copper-clad laminate, replaced FPGA, replaced power supply.

The complete CiNIC bill of materials was provided as an appendix to Kelly Woo's project report [4] and is stored on the NetPRL file server for reference.
References


