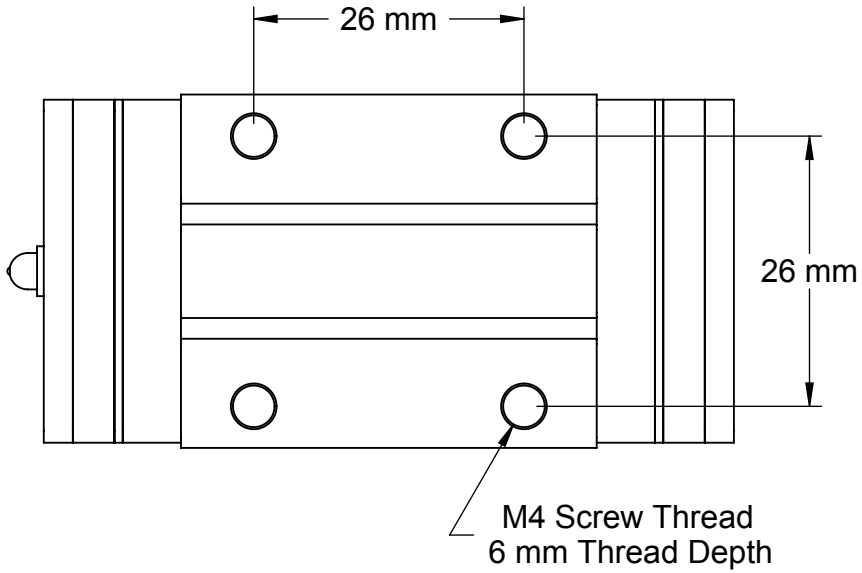
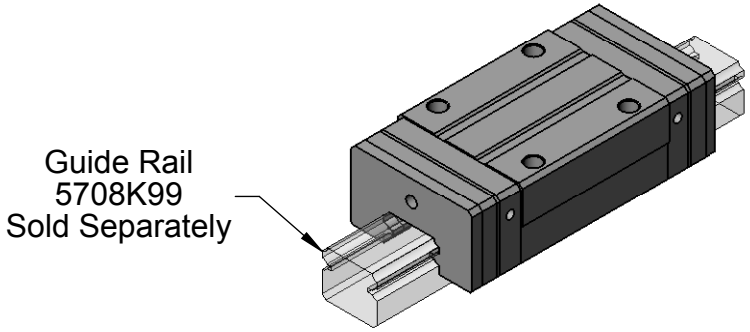
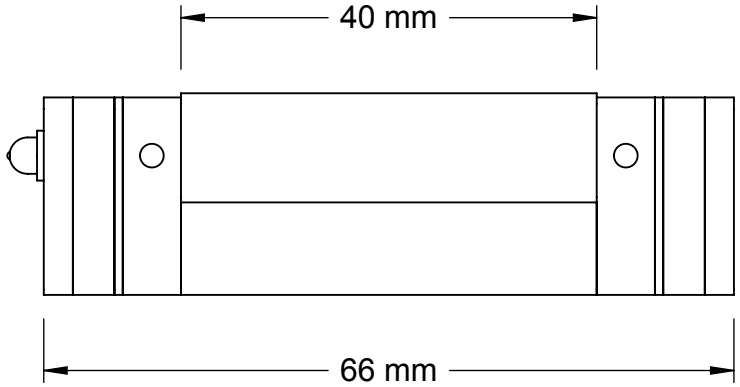
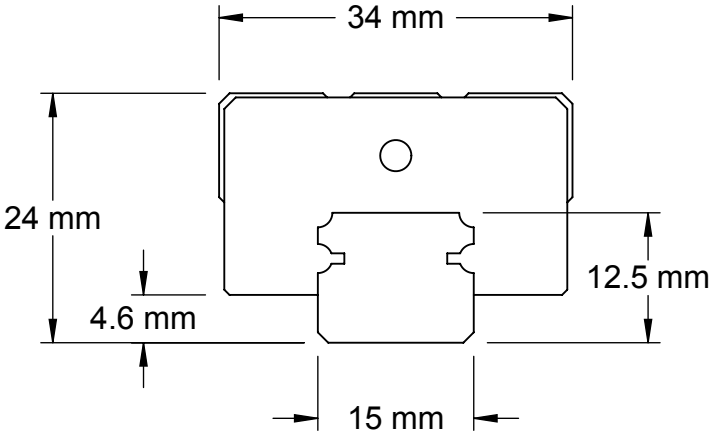
Appendix D: Vendor Supplied Specifications



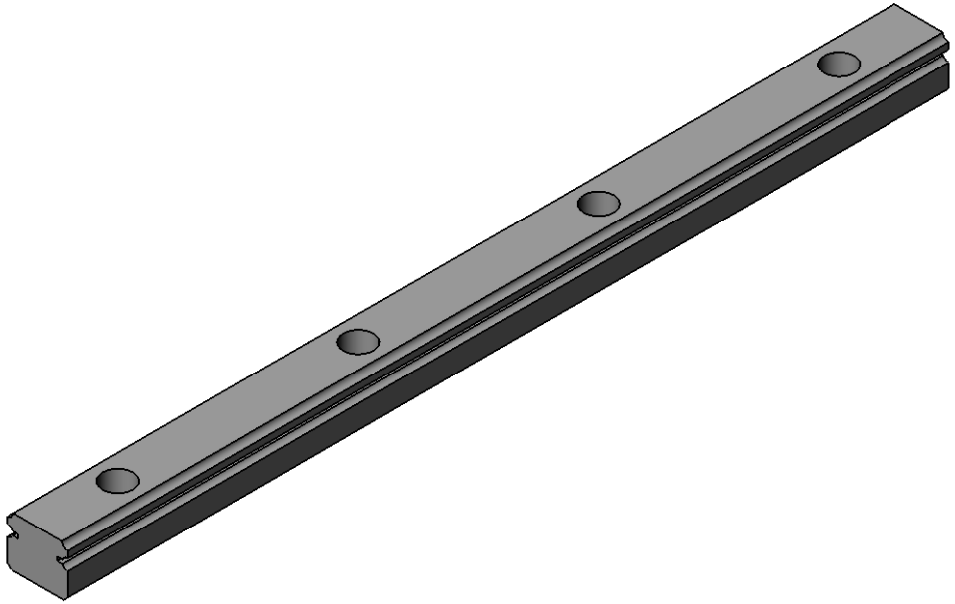


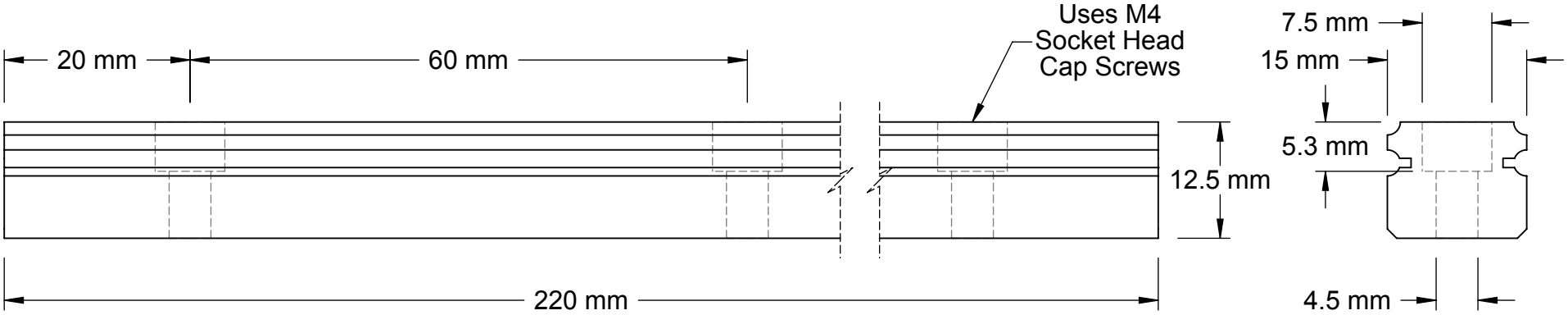




McMASTER-CARR® CAD	PART NUMBER	5708K25
http://www.mcmaster.com © 2012 McMaster-Carr Supply Company Information in this drawing is provided for reference only.	Type 440C Stainless Steel Threaded-Hole Carriage	

D2





McMASTER-CARR® CAD	PART NUMBER **5708K992**
http://www.mcmaster.com © 2013 McMaster-Carr Supply Company Information in this drawing is provided for reference only.	400 Series Stainless Steel Corrosion-Resistant Guide Rail

23AV Series Linear Actuators

ANAHEIM AUTOMATION

FEATURES

- NEMA 23 (57.15mm Square)
- Anti-Backlash and Self-Compensating Nut Option
- Nuts and Bushings can be Mounted on Either Front or Back of Motor
- Zero Backlash Operation
- Long life, Predictable Operation
- No Axial or Radial Play

DESCRIPTION

Anaheim Automation 23AV leadscrew step motors are the most versatile linear positioning motors on the market. They are available in thru-screw and fixed screw versions with a variety of drive nut and support bushing options. The 23AV motors are robust and can be easily configured to solve the most difficult application problems. Integration of a leadscrew with a motor saves space by eliminating components and reduces cost. While many standard configurations are available, custom modifications for OEM customers are available.

BUILD A PART NUMBER

23AV 1 02 AX 06 – AB

Motor Winding	
02	1.0A
04	2.0A
06	3.0A

Lead Screw Pitch (in)	
A	0.050”
B	0.100”
D	0.250”
E	0.500”

Lead Screw Length “L” (in)	
06	6”
12	12”

Front Attachment	
A	Anti-Backlash Nut
S	Standard Nut

Rear Attachment	
B	Bushing
C	Cover Only
E	Encoder Ready
N	No Extension

EXAMPLE:
23AV104AX12-SB = NEMA 17 Frame, 1 Stack, 2.0A Motor, 0.050” screw pitch resolution, 12” screw length, Standard Nut on the front of the motor along with a Bushing on the rear.

Note: See *Accessories* on our website for information on optional encoder and/or connector adders

MOTOR TYPES

23 AV
Anti-Backlash

23 AV
Standard Nut

23 AV
Centering Bushing

910 East Orangefair Ln. Anaheim, CA 92801 **Tel. (714) 992-6990** Fax. (714) 992-0471 **www.anaheimautomation.com**

SPECIFICATIONS

Model Number	Series Voltage (V)	Series RMS Current (A)	Series Resistance (ohms)	Power (W)	Series Inductance (mH)	Rotor Inertia (oz/sec)	Number of Leads	Motor Weight (oz)	Length (in)
23AV102	5.0	1.0	5.00	5.0	15.7	$1.7x10^{-3}$	4	18.3	1.81
23AV104	2.8	2.0	1.40	5.6	4.1	$1.7x10^{-3}$	4	18.3	1.81
23AV106	1.8	3.0	0.60	5.4	1.5	$1.7x10^{-3}$	4	18.3	1.81

Screw Pitch Options						
Screw Pitch	Screw Pitch (in)	Static Force (lb)	Dynamic Force (lb)	Travel per Full Step (in)	Travel per Microstep (in)	Positioning Accuracy (in/in)
A	0.050	165	150	0.00025	$.98x10^{-6}$	0.0004
B	0.100	165	128	0.00050	$1.95x10^{-6}$	0.0004
D	0.250	165	76	0.00125	$4.88x10^{-6}$	0.0004
E	0.500	165	45	0.00250	$9.77x10^{-6}$	0.0004

MODIFICATIONS

Anaheim Automation welcomes the opportunity to customize 23AV motors for our OEM customers to better meet application requirements or supply a drop-in solution. Here are just a few options we have had experience with:

- Custom Motor Windings
- Alternate Lead Configurations - 6 lead, 8 lead
- Longer Motor Stack Lengths
- Custom Cabling and/or Connectors
- Encoder Feedback
- Alternate Screw Leads
- Machined Screw Journals to Print
- Teflon Coating on Screw
- Custom Drive Nut Materials or Design

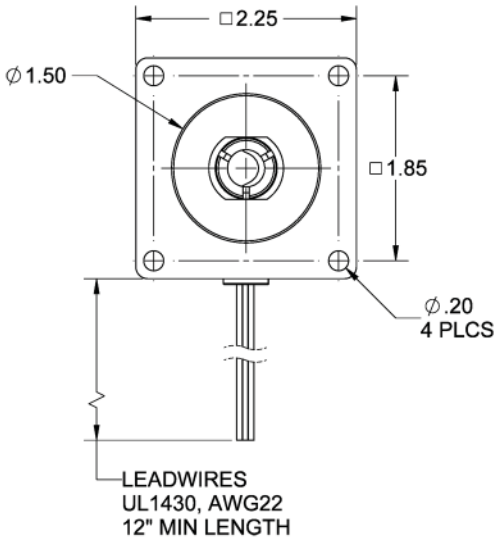
OPTIONS

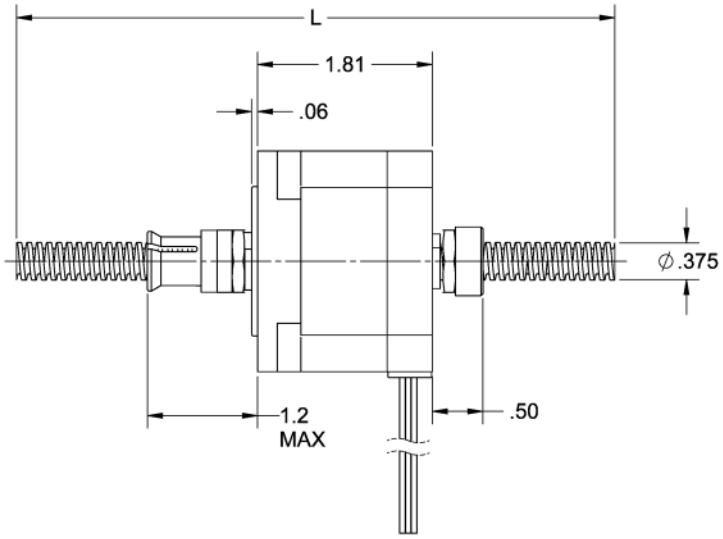
23AV Encoder Option:

Note: See *Accessories* on our website for information on optional encoder and/or connector adders

DIMENSIONS

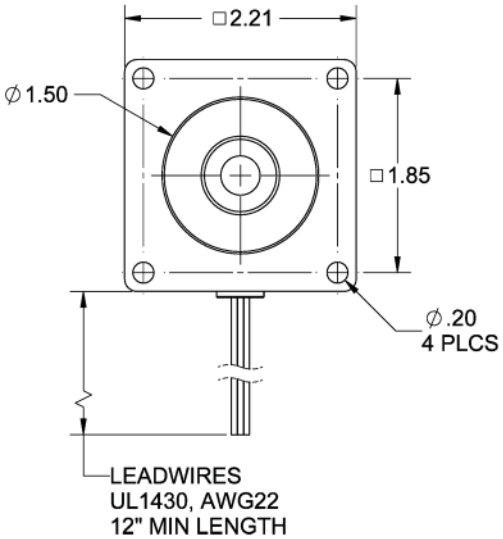
With Anti-Backlash

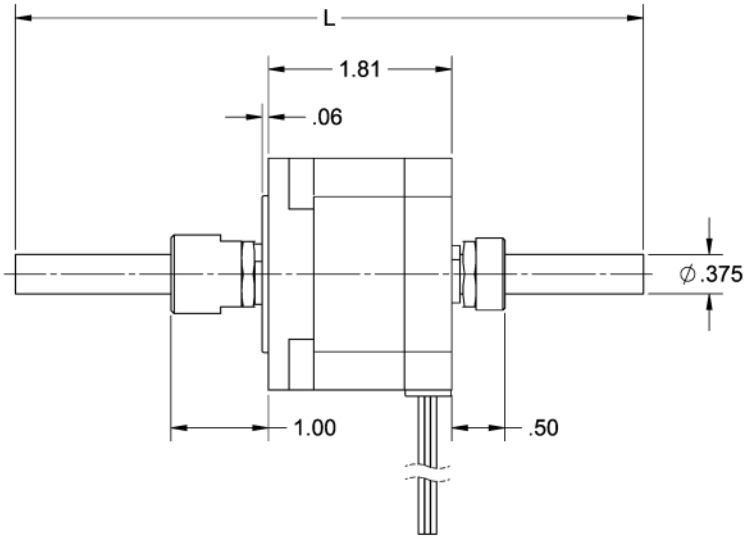




All units are in inches

With Standard-Nut



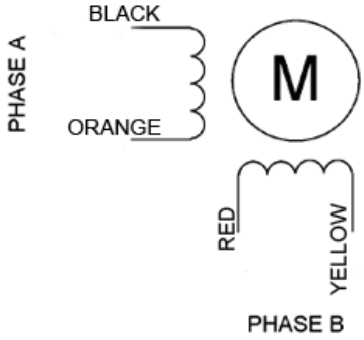


All units are in inches

WIRING

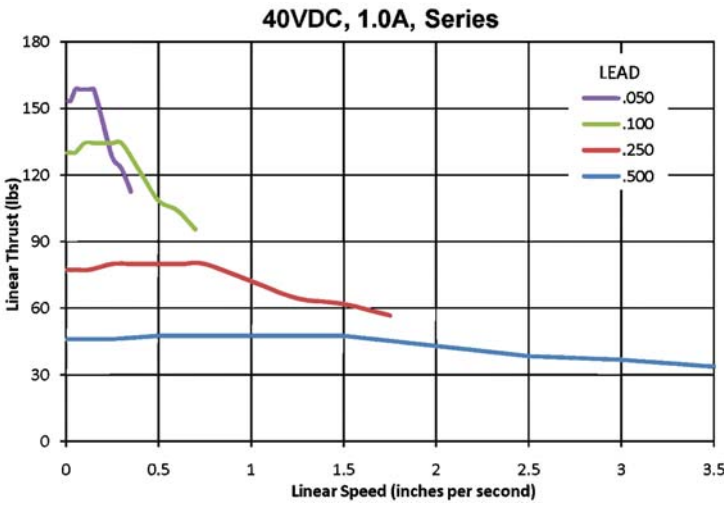
Switching Sequence

Step	Black	Orange	Red	Yellow
1	+	-	+	-
2	-	+	+	-
3	-	+	-	+
4	+	-	-	+

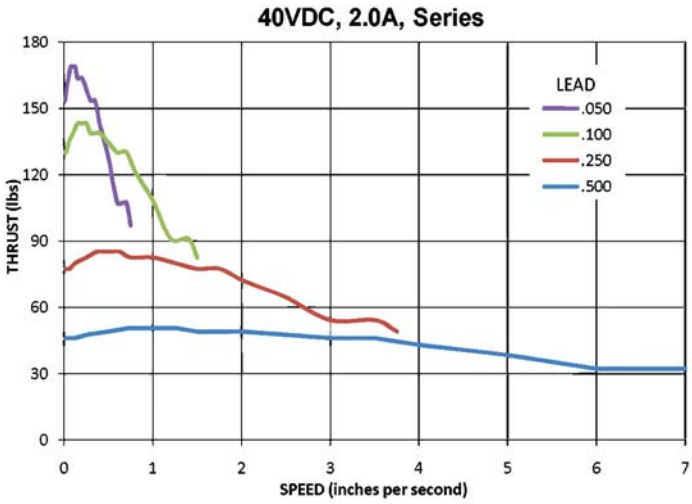


TORQUE CURVES

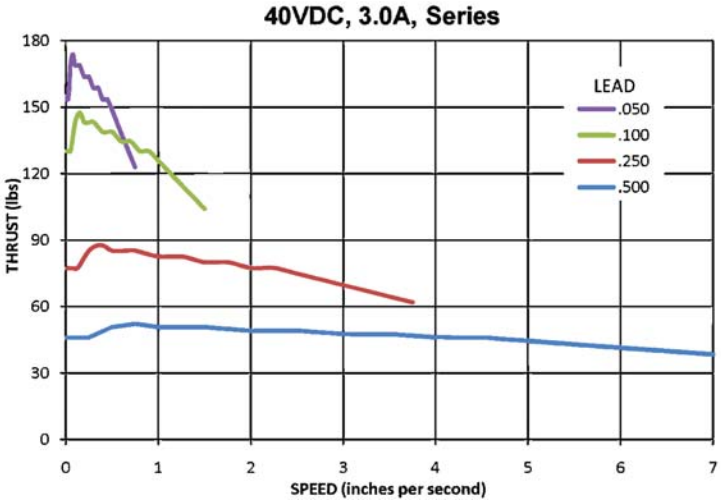
23AV102



23AV104



23AV106



Data sheet acquired from Harris Semiconductor
SCHS209C

February 1998 - Revised July 2003

CD74HC4067, CD74HCT4067

High-Speed CMOS Logic 16-Channel Analog Multiplexer/Demultiplexer

Features

- **Wide Analog Input Voltage Range**
- **Low "ON" Resistance**
  - **V_{CC} = 4.5V . . . . . 70Ω (Typ)**
  - **V_{CC} = 6V . . . . . 60Ω (Typ)**
- **Fast Switching and Propagation Speeds**
- **"Break-Before-Make" Switching. . . . . 6ns (Typ) at 4.5V**
- **Available in Both Narrow and Wide-Body Plastic Packages**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The CD74HC4067 and CD74HCT4067 devices are digitally controlled analog switches that utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL, with the low power consumption of standard CMOS integrated circuits.

These analog multiplexers/demultiplexers control analog voltages that may vary across the voltage supply range. They are bidirectional switches thus allowing any analog input to be used as an output and vice-versa. The switches have low "on" resistance and low "off" leakages. In addition, these devices have an enable control which when high will disable all switches to their "off" state.

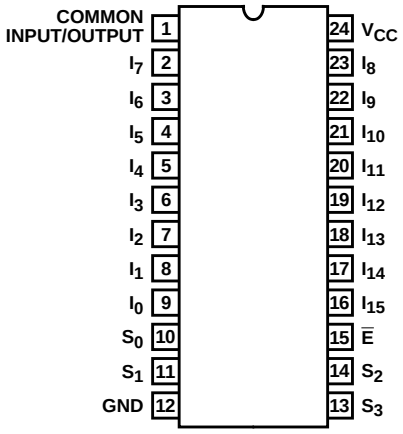
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD74HC4067E	-55 to 125	24 Ld PDIP
CD74HC4067M	-55 to 125	24 Ld SOIC
CD74HC4067M96	-55 to 125	24 Ld SOIC
CD74HC4067SM96	-55 to 125	24 Ld SSOP
CD74HCT4067M	-55 to 125	24 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel.

Pinout

CD74HC4067 (PDIP, SOIC, SSOP)
CD74HCT4067 (SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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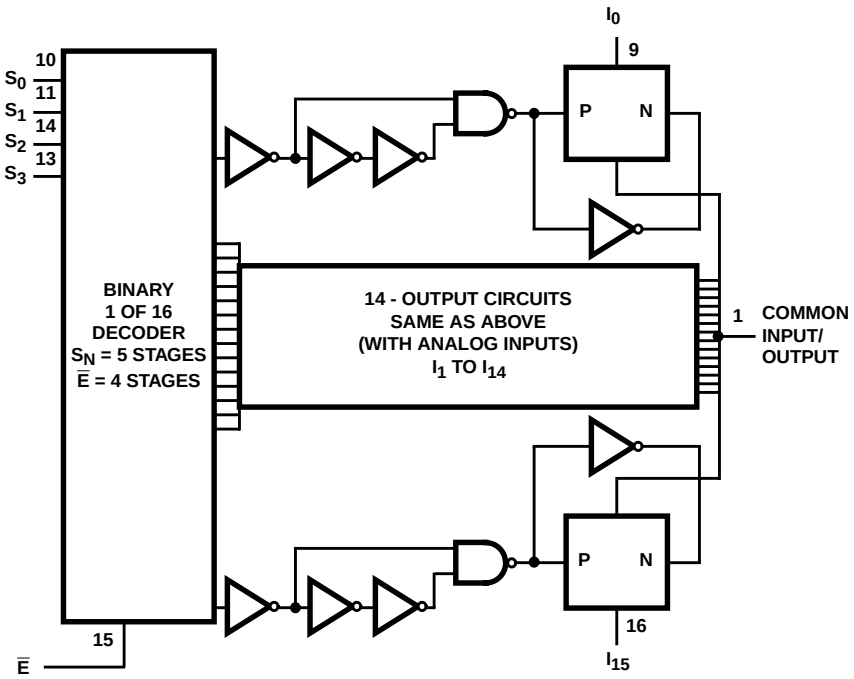
Functional Diagram



TRUTH TABLE

S0	S1	S2	S3	$\overline{E}$	SELECTED CHANNEL
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

H= High Level
L= Low Level
X= Don’t Care

Absolute Maximum Ratings

DC Supply Voltage, V_{CC}
(Voltages Referenced to Ground) . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Drain Current, I_O
For -0.5V < V_O < V_{CC} + 0.5V . . . . . ±25mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . . ±50mA

Operating Conditions

Temperature Range, T_A . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical) θ_{JA} (°C/W)
E (PDIP) Package, Note 1 67
M (SOIC) Package, Note 2 46
SM (SSOP) Package, Note 2. 63
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The package thermal impedance is calculated in accordance with JESD 51-3.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS V_{IS} (V)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
Maximum "ON" Resistance I_O = 1mA	R_{ON}	V_{CC} or GND	V_{CC} or GND	4.5	-	70	160	-	200	-	240	Ω
				6	-	60	140	-	175	-	210	Ω
		V_{CC} to GND	V_{CC} to GND	4.5	-	90	180	-	225	-	270	Ω
				6	-	80	160	-	200	-	240	Ω
Maximum "ON" Resistance Between Any Two Switches	ΔR_{ON}	-	-	4.5	-	10	-	-	-	-	-	Ω
				6	-	8.5	-	-	-	-	-	Ω
Switch "Off" Leakage Current 16 Channels	I_{IZ}	$\overline{E}$ = V_{CC}	V_{CC} or GND	6	-	-	±0.8	-	±8	-	±8	µA
Logic Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS V_{IS} (V)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
Quiescent Device Current I_O = 0mA	I_{CC}	V_{CC} or GND	-	6	-	-	8	-	80	-	160	µA
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5	-	-	0.8	-	0.8	-	0.8	V
Maximum "ON" Resistance I_O = 1mA	R_{ON}	V_{CC} or GND	V_{CC} or GND	4.5	-	70	160	-	200	-	240	Ω
		V_{CC} to GND	V_{CC} to GND	4.5	-	90	180	-	225	-	270	Ω
Maximum "ON" Resistance Between Any Two Switches	ΔR_{ON}	-	-	4.5	-	10	-	-	-	-	-	Ω
Switch "Off" Leakage Current 16 Channels	I_{IZ}	$\overline{E} = V_{CC}$	V_{CC} or GND	6	-	-	±0.8	-	±8	-	±8	µA
Logic Input Leakage Current	I_I	V_{CC} or GND (Note 3)	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	-	6	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 4)	V_{CC} -2.1	-	-	-	100	360	-	450	-	490	µA

NOTES:

3. Any voltage between V_{CC} and GND.
4. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOAD
S_0 - S_3	0.5
$\overline{E}$	0.3

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360µA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES											
Propagation Delay Time Switch In to Out	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
		C_L = 15pF	5	-	6	-	-	-	-	-	ns

Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Switch Turn On $\overline{E}$ to Out	t_{PZH}, t_{PZL}	C_L = 50pF	2	-	-	275	-	345	-	415	ns
			4.5	-	-	55	-	69	-	83	ns
			6	-	-	47	-	59	-	71	ns
		C_L = 15pF	5	-	23	-	-	-	-	-	ns
Switch Turn On Sn to Out	t_{PZH}, t_{PZL}	C_L = 50pF	2	-	-	300	-	375	-	450	ns
			4.5	-	-	60	-	75	-	90	ns
			6	-	-	51	-	64	-	76	ns
		C_L = 15pF	5	-	25	-	-	-	-	-	ns
Switch Turn Off $\overline{E}$ to Out	t_{PHZ}, t_{PLZ}	C_L = 50pF	2	-	-	275	-	345	-	415	ns
			4.5	-	-	55	-	69	-	83	ns
			6	-	-	47	-	59	-	71	ns
		C_L = 15pF	5	-	23	-	-	-	-	-	ns
Switch Turn Off Sn to Out	t_{PHZ}, t_{PLZ}	C_L = 50pF	2	-	-	290	-	365	-	435	ns
			4.5	-	-	58	-	73	-	87	ns
			6	-	-	49	-	62	-	74	ns
		C_L = 50pF	5	-	21	-	-	-	-	-	ns
Input (Control) Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 5, 6)	C_{PD}	-	5	-	93	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay Time Switch In to Out	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
		C_L = 15pF	5	-	6	-	-	-	-	-	ns
Switch Turn On $\overline{E}$ to Out	t_{PZH}, t_{PZL}	C_L = 50pF	4.5	-	-	60	-	75	-	90	ns
		C_L = 15pF	5	-	25	-	-	-	-	-	ns
Switch Turn On Sn to Out	t_{PZH}, t_{PZL}	C_L = 50pF	4.5	-	-	60	-	75	-	90	ns
		C_L = 15pF	5	-	25	-	-	-	-	-	ns
Switch Turn Off $\overline{E}$ to Out	t_{PHZ}, t_{PLZ}	C_L = 50pF	4.5	-	-	55	-	69	-	83	ns
		C_L = 15pF	5	-	23	-	-	-	-	-	ns
Switch Turn Off Sn to Out	t_{PHZ}, t_{PLZ}	C_L = 50pF	4.5	-	-	58	-	73	-	87	ns
		C_L = 15pF	5	-	21	-	-	-	-	-	ns
Input (Control) Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 5, 6)	C_{PD}	-	5	-	96	-	-	-	-	-	pF

NOTES:

5. C_{PD} is used to determine the dynamic power consumption, per package.
6. $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L + C_S) V_{CC}^2 f_o$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, C_S = switch capacitance, V_{CC} = supply voltage.

Analog Channel Specifications $T_A = 25^oC$

PARAMETER	TEST CONDITIONS	V_{CC} (V)	HC/HCT	UNITS
Switch Frequency Response Bandwidth at -3dB (Figure 2)	Figure 4, Notes 7, 8	4.5	89	MHz
Sine Wave Distortion	Figure 5	4.5	0.051	%
Feedthrough Noise $\overline{E}$ to Switch	Figure 6, Notes 8, 9	4.5	TBE	mV
Feedthrough Noise S to Switch			TBE	mV
Switch “OFF” Signal Feedthrough (Figure 3)	Figure 7	4.5	-75	dB
Switch Input Capacitance, C_S		-	5	pF
Common Capacitance, C_{COM}		-	50	pF

NOTES:

7. Adjust input level for 0dBm at output, f = 1MHz.
8. V_{IS} is centered at $V_{CC}/2$.
9. Adjust input for 0dBm at V_{IS}.

Typical Performance Curves

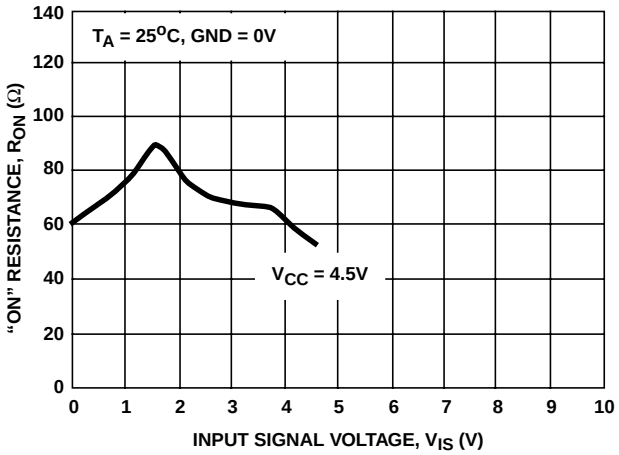


FIGURE 1. TYPICAL “ON” RESISTANCE vs INPUT SIGNAL VOLTAGE

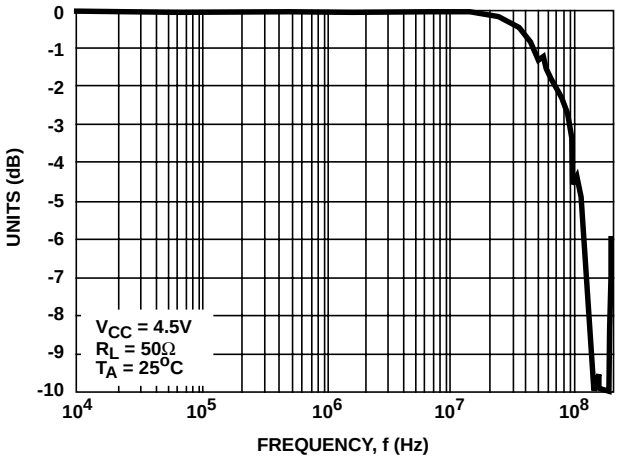


FIGURE 2. TYPICAL SWITCH FREQUENCY RESPONSE

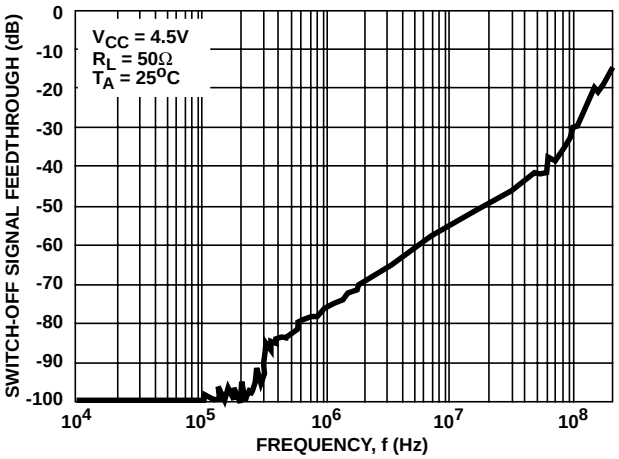


FIGURE 3. TYPICAL SWITCH-OFF SIGNAL FEEDTHROUGH vs FREQUENCY

Analog Test Circuits

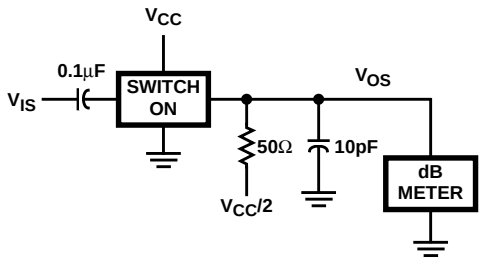


FIGURE 4. FREQUENCY RESPONSE TEST CIRCUIT

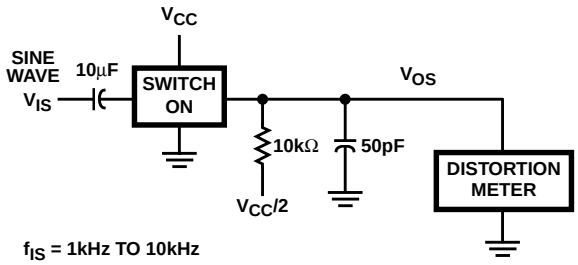


FIGURE 5. SINE WAVE DISTORTION TEST CIRCUIT

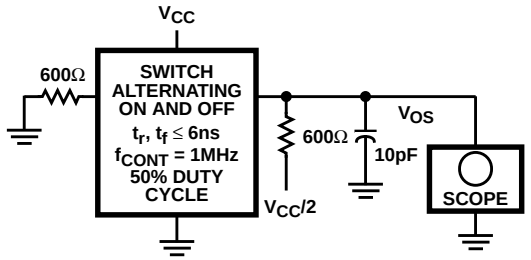


FIGURE 6. CONTROL-TO-SWITCH FEEDTHROUGH NOISE TEST CIRCUIT

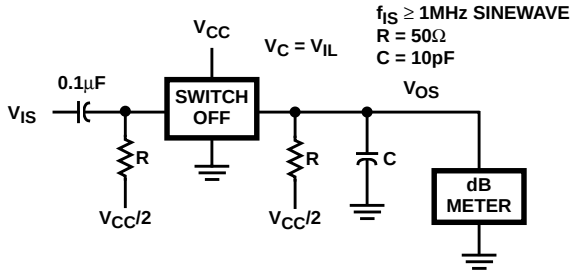


FIGURE 7. SWITCH OFF SIGNAL FEEDTHROUGH TEST CIRCUIT

Test Circuits and Waveforms

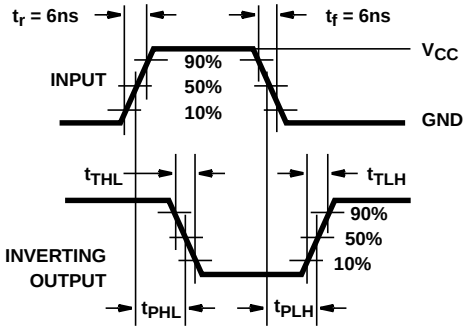


FIGURE 8. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

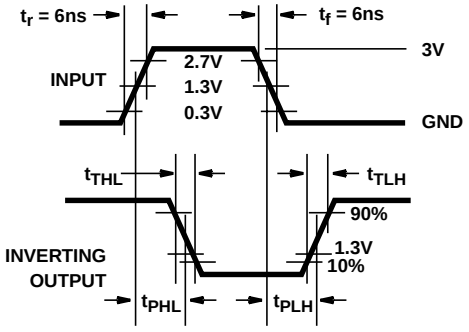


FIGURE 9. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

TEXAS INSTRUMENTS
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PACKAGE OPTION ADDENDUM

18-Sep-2008

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CD74HC4067DB	PREVIEW	SSOP	DB	24	60	TBD	Call TI	Call TI
CD74HC4067E	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC4067EE4	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC4067M	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4067M96	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4067M96E4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4067M96G4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4067ME4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4067MG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4067SM	PREVIEW	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
CD74HC4067SM96	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
CD74HC4067SM96E4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
CD74HC4067SM96G4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
CD74HCT4067M	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4067ME4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4067MG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder

temperature.

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OTHER QUALIFIED VERSIONS OF CD74HCT4067 :

- Automotive: CD74HCT4067-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

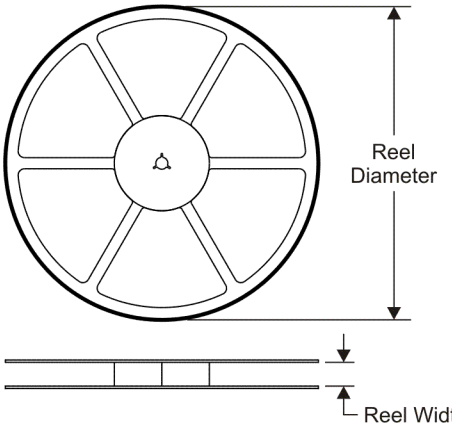
PACKAGE MATERIALS INFORMATION

www.ti.com

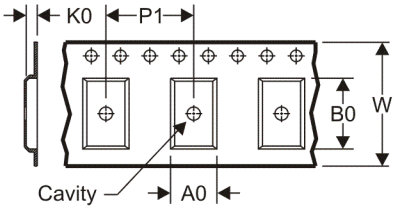
11-Mar-2008

TAPE AND REEL INFORMATION

REEL DIMENSIONS

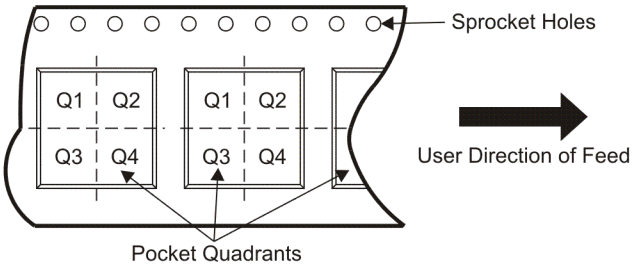


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

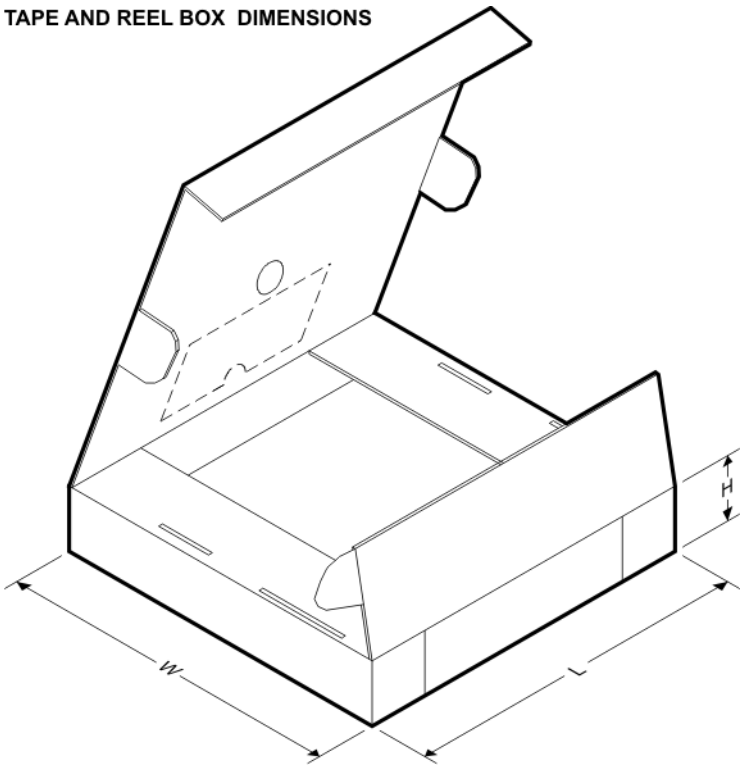


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4067M96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD74HC4067SM96	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

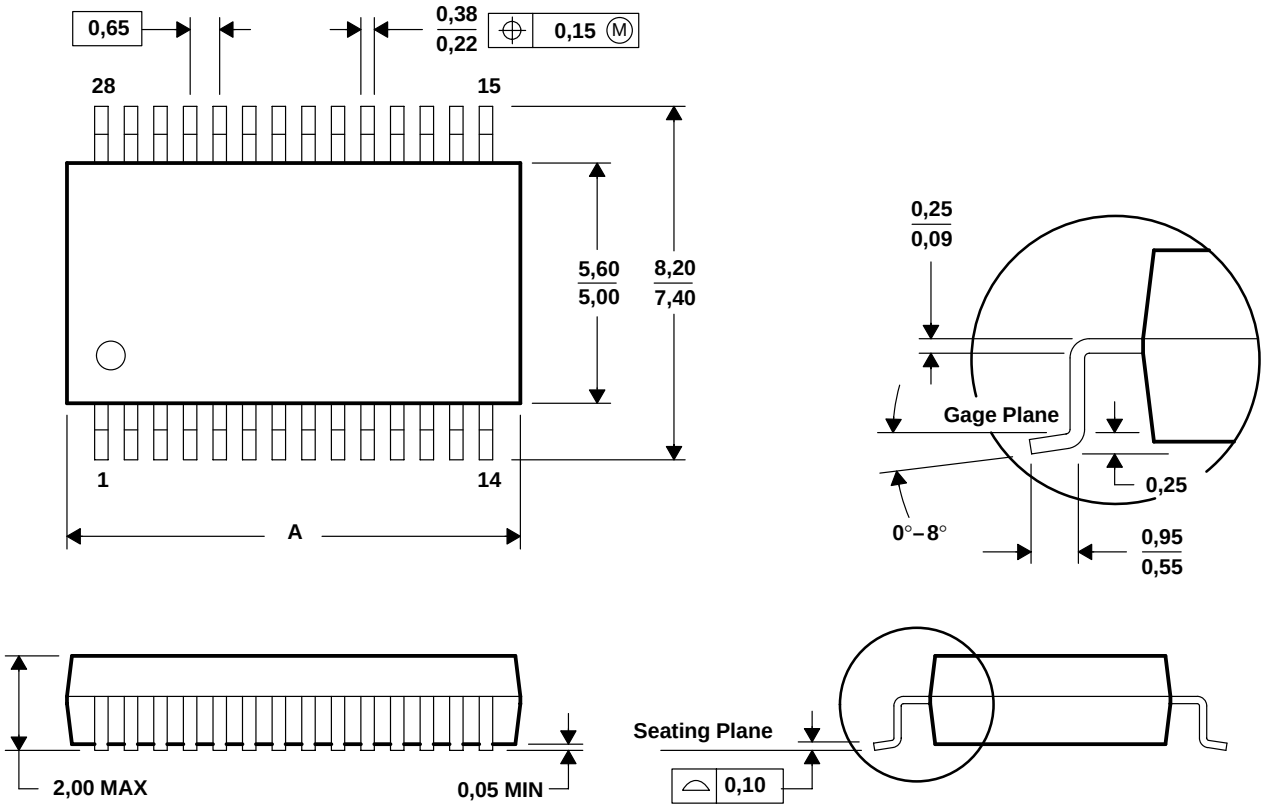


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4067M96	SOIC	DW	24	2000	346.0	346.0	41.0
CD74HC4067SM96	SSOP	DB	24	2000	346.0	346.0	33.0

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

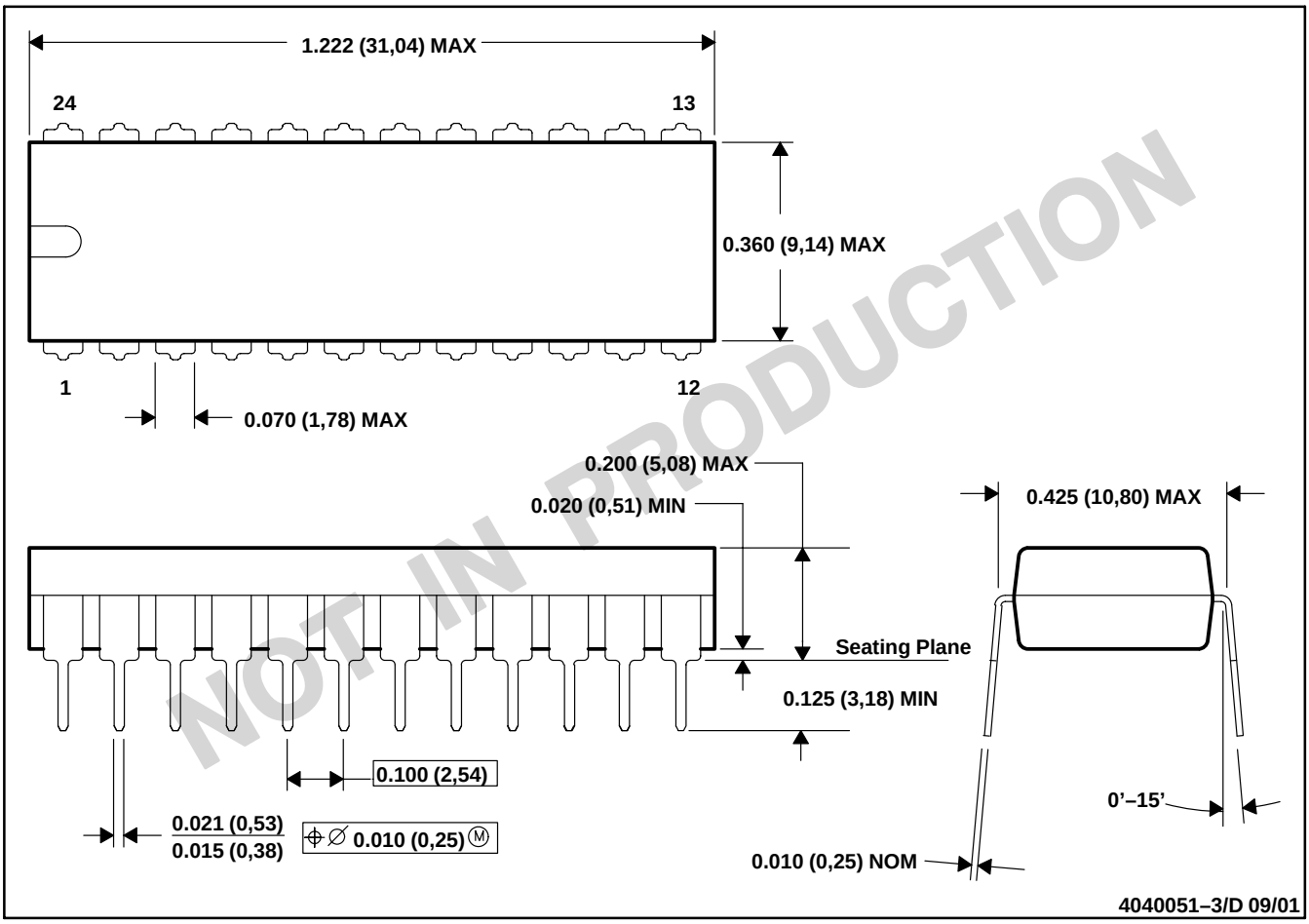


DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

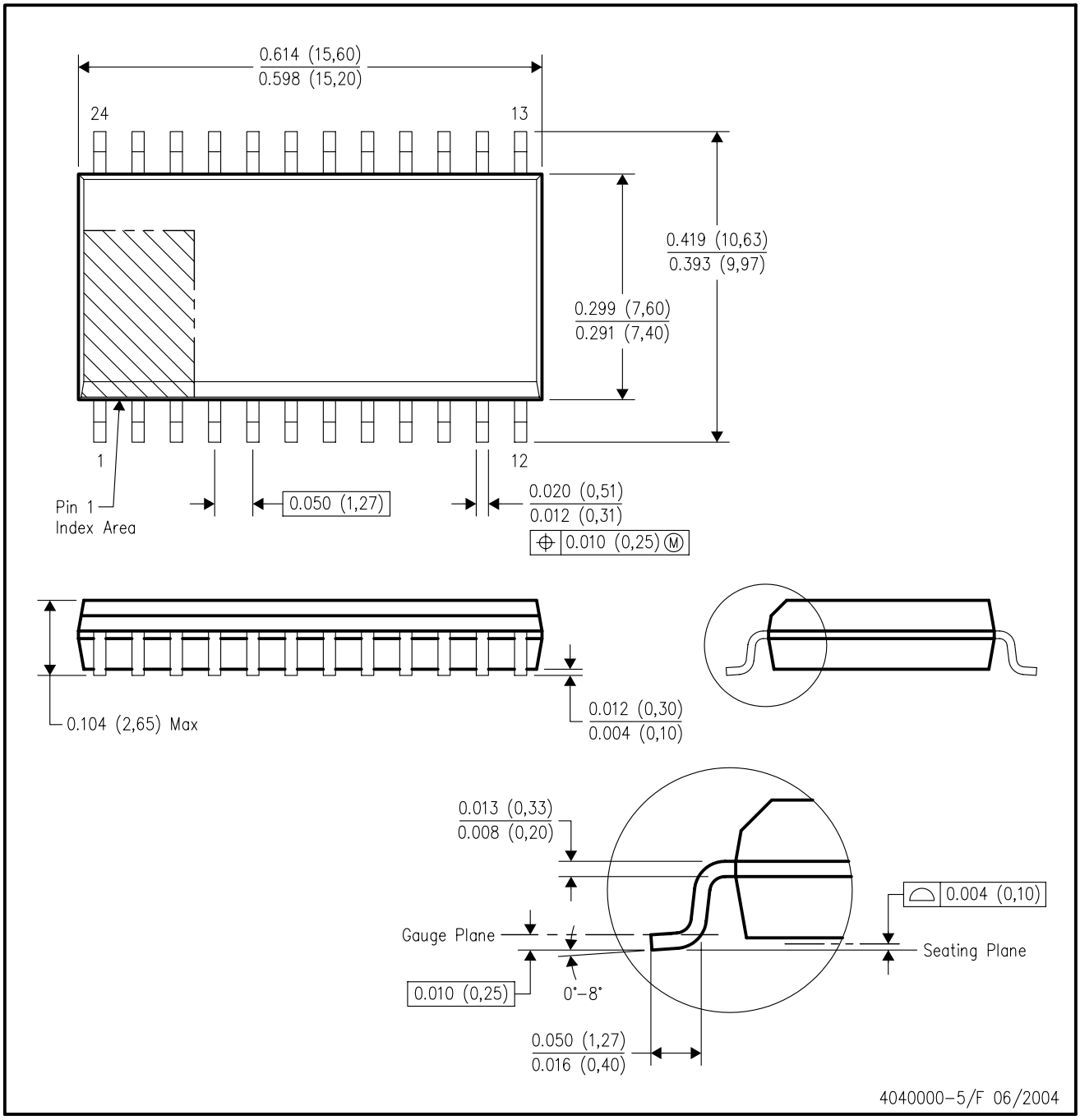
N (R–PDIP–T24) **PLASTIC DUAL–IN–LINE**



NOT IN PRODUCTION

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–010

DW (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE

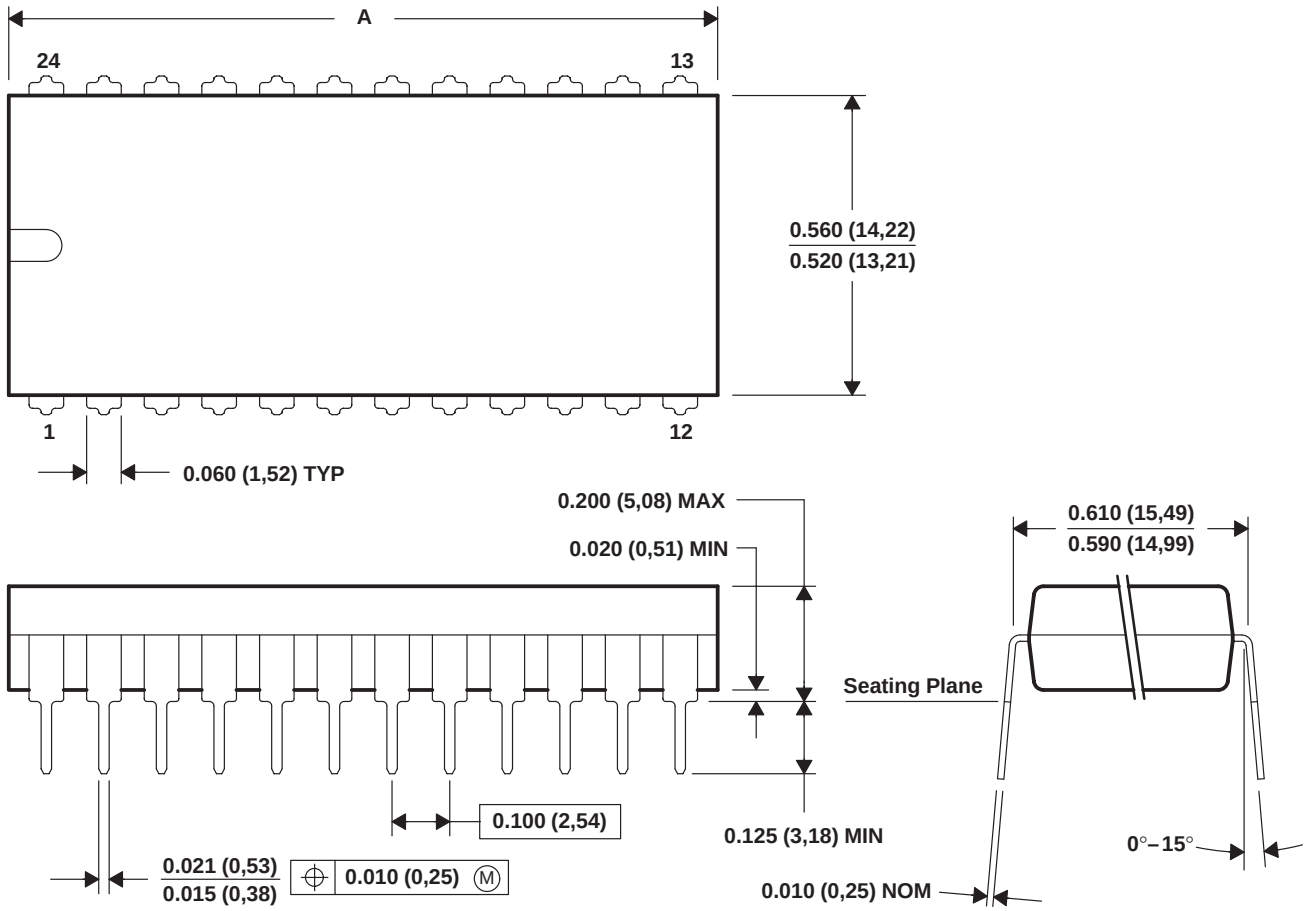


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN



DIM \ PINS **	24	28	32	40	48	52
A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)	2.650 (67,31)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)

4040053 / B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-011
D. Falls within JEDEC MS-015 (32 pin only)

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ANALOG DEVICES

LC²MOS Single Supply, 12-Bit 600 kSPS ADC

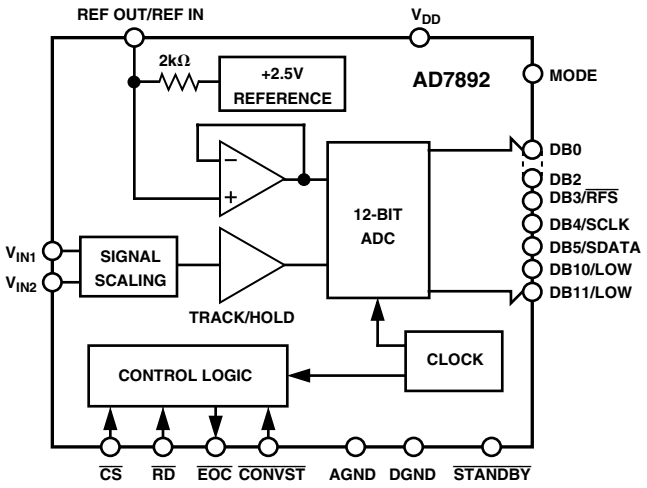
AD7892

FEATURES

Fast 12-Bit ADC with 1.47 µs Conversion Time
600 kSPS Throughput Rate (AD7892-3)
500 kSPS Throughput Rate (AD7892-1, AD7892-2)
Single Supply Operation
On-Chip Track/Hold Amplifier
Selection of Input Ranges:
- **±10 V or ±5 V for AD7892-1**
- **0 V to +2.5 V for AD7892-2**
- **±2.5 V for AD7892-3**

High Speed Serial and Parallel Interface
Low Power, 60 mW typ
Overvoltage Protection on Analog Inputs (AD7892-1 and AD7892-3)

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7892 is a high speed, low power, 12-bit A/D converter that operates from a single +5 V supply. The part contains a 1.47 µs successive approximation ADC, an on-chip track/hold amplifier, an internal +2.5 V reference and on-chip versatile interface structures that allow both serial and parallel connection to a microprocessor. The part accepts an analog input range of ±10 V or ±5 V (AD7892-1), 0 V to +2.5 V (AD7892-2) and ±2.5 V (AD7892-3). Overvoltage protection on the analog inputs for the AD7892-1 and AD7892-3 allows the input voltage to go to ±17 V or ±7 V respectively without damaging the ports.

The AD7892 offers a choice of two data output formats: a single, parallel, 12-bit word or serial data. Fast bus access times and standard control inputs ensure easy parallel interface to microprocessors and digital signal processors. A high speed serial interface allows direct connection to the serial ports of microcontrollers and digital signal processors.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the part is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The AD7892 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. It is available in a 24-lead, 0.3" wide, plastic or hermetic DIP or in a 24-lead SOIC.

PRODUCT HIGHLIGHTS

1. The AD7892-3 features a conversion time of 1.47 µs and a track/hold acquisition time of 200 ns. This allows a throughput rate for the part up to 600 kSPS. The AD7892-1 and AD7892-2 operate with throughput rates of 500 kSPS.
2. The AD7892 operates from a single +5 V supply and consumes 60 mW typ making it ideal for low power and portable applications.
3. The part offers a high speed, flexible interface arrangement with parallel and serial interfaces for easy connection to microprocessors, microcontrollers and digital signal processors.

REV. C

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Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703
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AD7892–SPECIFICATIONS (V_{DD} = +5 V ± 5%, AGND = DGND = 0 V, REF IN = +2.5 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Versions[1]	B Versions	S Version[2]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
AD7892-1, AD7892-2					f_{IN} = 100 kHz. f_{SAMPLE} = 500 kSPS
Signal to (Noise + Distortion) Ratio[3]	70	70	70	dB min	
Total Harmonic Distortion[3]	–78	–78	–78	dB max	typ –84 dB
Peak Harmonic or Spurious Noise[3]	–79	–79	–79	dB max	
Intermodulation Distortion[3]					fa = 49 kHz, fb = 50 kHz
2nd Order Terms	–78	–78	–78	dB max	typ –84 dB
3rd Order Terms	–78	–78	–78	dB max	typ –84 dB
AD7892-3					f_{IN} = 100 kHz. f_{SAMPLE} = 600 kSPS
Signal to (Noise + Distortion) Ratio[3]	70	70		dB min	
Total Harmonic Distortion[3]	–78	–78		dB max	
Peak Harmonic or Spurious Noise[3]	–79	–79		dB max	
Intermodulation Distortion[3]					fa = 49 kHz, fb = 50 kHz
2nd Order Terms	–78	–78		dB max	
3rd Order Terms	–78	–78		dB max	
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for Which No Missing Codes Are Guaranteed	12	12	12	Bits	
Relative Accuracy[3]	±1.5	±1	±1	LSB max	
Differential Nonlinearity[3]	±1	±1	±1	LSB max	
AD7892-1					
Positive Full-Scale Error[3]	±4	±4	±5	LSB max	
Negative Full-Scale Error[3]	±4	±4	±5	LSB max	
Bipolar Zero Error[3]	±3	±2	±3	LSB max	
AD7892-3					
Positive Full-Scale Error[3]	±4	±4		LSB max	
Negative Full-Scale Error[3]	±4	±4		LSB max	
Bipolar Zero Error[3]	±4	±3		LSB max	
AD7892-2					
Positive Full-Scale Error[3]	±5	±5	±5	LSB max	
Unipolar Offset Error[3]	±4	±3	±4	LSB max	
ANALOG INPUT					
AD7892-1					
Input Voltage Range	±10	±10	±10	Volts	Input Applied to V_{IN1} with V_{IN2} Grounded
Input Voltage Range	±5	±5	±5	Volts	Input Applied to V_{IN1} and V_{IN2}
Input Resistance	8	8	8	kΩ min	Input Applied to V_{IN1} with V_{IN2} Grounded
AD7892-2					
Input Voltage Range on V_{IN1}	0 to +2.5	0 to +2.5	0 to +2.5	Volts	Input Applied to V_{IN1}
Input Current	10	10	50	nA max	
Input Voltage Range on V_{IN2}	±50	±50	±50	mV max	
AD7892-3					
Input Voltage Range on V_{IN1}	±2.5	±2.5		Volts	Input Applied to V_{IN1}
Input Resistance	2	2		kΩ min	
REFERENCE OUTPUT/INPUT					
REF IN Input Voltage Range	2.375/2.625	2.375/2.625	2.375/2.625	V min/V max	2.5 V ± 5%
Input Impedance	1.6	1.6	1.6	kΩ min	Resistor Connected to Internal Reference Node
Input Capacitance[4]	10	10	10	pF max	
REF OUT Output Voltage	2.5	2.5	2.5	V nom	
REF OUT Error @ +25°C	±10	±10	±10	mV max	
T_{MIN} to T_{MAX}	±20	±20	±25	mV max	
REF OUT Temperature Coefficient	25	25	25	ppm/°C typ	
REF OUT Output Impedance	5.5	5.5	5.5	kΩ nom	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	10	pF max	

Parameter	A Versions[1]	B Versions	S Version[2]	Unit	Test Conditions/Comments
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0					
Floating-State Leakage Current	±10	±10	±10	µA max	
Floating-State Capacitance[4]	15	15	15	pF max	
Output Coding					
AD7892-1 and AD7892-3	Two's Complement				
AD7892-2	Straight (Natural) Binary				
CONVERSION RATE					
Conversion Time	1.47	1.47		µs max	AD7892-3
Track/Hold Acquisition Time[3]	0.2	0.2		µs max	AD7892-3
Conversion Time	1.6	1.6	1.68	µs max	AD7892-1 and AD7892-2
Track/Hold Acquisition Time[3]	0.4	0.4	0.32	µs max	AD7892-1 and AD7892-2
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
I_{DD}[5]					
Normal Operation	18	18	19	mA max	
Standby Mode[6]					
AD7892-2	250	250		µA typ	
AD7892-3, AD7892-1	80	80	100	µA max	typ 15 µA
Power Dissipation[5]					
Normal Operation	90	90	95	mW max	V_{DD} = +5 V. Typically 60 mW
Standby Mode[6]					
AD7892-2	1.25	1.25		mW typ	
AD7892-3, AD7892-1	400	400	500	µW max	V_{DD} = +5 V. Typically 75 µW

NOTES
[1]Temperature ranges are as follows: A, B Versions: –40°C to +85°C; S Version: –55°C to +125°C.
[2]S Version available on AD7892-1 and AD7892-2 only.
[3]See Terminology.
[4]Sample tested @ +25°C to ensure compliance.
[5]These normal mode and standby mode currents are achieved with resistors (in the range 10 kΩ to 100 kΩ) to either DGND or V_{DD} on Pins 8, 9, 16 and 17.
[6]A conversion should not be initiated on the part within 30 µs of exiting standby mode.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND . . . . . –0.3 V to +7 V
V_{DD} to DGND . . . . . –0.3 V to +7 V
Analog Input Voltage to AGND
AD7892-1 . . . . . ±17 V
AD7892-2 . . . . . –0.3 V, V_{DD}
AD7892-3 . . . . . ±7 V
Reference Input Voltage to AGND . . . –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Commercial (A, B Versions) . . . . . –40°C to +85°C
Extended (S Version) . . . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . +150°C
Plastic DIP Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 105°C/W
Lead Temperature (Soldering, 10 sec) . . . . . +260°C
Cerdip Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 70°C/W
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
SOIC Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 75°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AD7892

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, AGND = DGND = 0 V, REF IN = +2.5 V)

Parameter	A, B Versions	S Version	Unit	Test Conditions/Comments
t_{CONV}	1.47		µs max	Conversion Time for AD7892-3
	1.6	1.68	µs max	Conversion Time for AD7892-1, AD7892-2
t_{ACQ}	200		ns min	Acquisition Time for AD7892-3
	400	320	ns min	Acquisition Time for AD7892-1, AD7892-2
Parallel Interface				
t_1	35	45	ns min	$\overline{CONVST}$ Pulsewidth
t_2	60	60	ns min	$\overline{EOC}$ Pulsewidth
t_3	0	0	ns min	$\overline{EOC}$ Falling Edge to $\overline{CS}$ Falling Edge Setup Time
t_4	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_5	35	45	ns min	Read Pulsewidth
t_6[3]	35	40	ns max	Data Access Time After Falling Edge of $\overline{RD}$
t_7[4]	5	5	ns min	Bus Relinquish Time After Rising Edge of $\overline{RD}$
	30	40	ns max	
t_8	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_9	200	200	ns min	$\overline{RD}$ to $\overline{CONVST}$ Setup Time
Serial Interface				
t_{10}	30	35	ns min	$\overline{RFS}$ Low to SCLK Falling Edge Setup Time
t_{11}[3]	25	30	ns max	$\overline{RFS}$ Low to Data Valid Delay
t_{12}	25	25	ns min	SCLK High Pulsewidth
t_{13}	25	25	ns min	SCLK Low Pulsewidth
t_{14}[3]	5	5	ns min	SCLK Rising Edge to Data Valid Hold Time
t_{15}[3]	25	30	ns max	SCLK Rising Edge to Data Valid Delay
t_{16}	20	30	ns min	$\overline{RFS}$ to SCLK Falling Edge Hold Time
t_{17}[4]	0	0	ns min	Bus Relinquish Time after Rising Edge of $\overline{RFS}$
	30	30	ns max	
t_{17A}[4]	0	0	ns min	Bus Relinquish Time after Rising Edge of SCLK
	30	30	ns max	

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are measured with tr = tf = 1 ns (10% to 90% of +5 V) and timed from a voltage level of +1.6 V.
[2]See Figures 2 and 3.
[3]Measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[4]These times are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.
[5]Assumes CMOS loads on the data bits. With TTL loads, more current is drawn from the data lines and the $\overline{RD}$ to $\overline{CONVST}$ time needs to be extended to 400 ns min.
Specifications subject to change without notice.

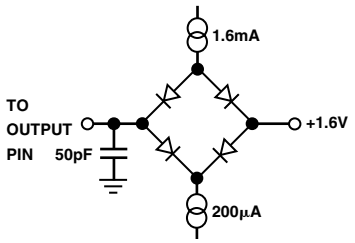


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7892 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Input Range	Sample Rate	Relative Accuracy	Temperature Range	Package Option[1]
AD7892AN-1	±5 V or ±10 V	500 kSPS		–40°C to +85°C	N-24
AD7892BN-1	±5 V or ±10 V	500 kSPS	±1 LSB	–40°C to +85°C	N-24
AD7892AR-1	±5 V or ±10 V	500 kSPS		–40°C to +85°C	R-24
AD7892BR-1	±5 V or ±10 V	500 kSPS	±1 LSB	–40°C to +85°C	R-24
AD7892SQ-1	±5 V or ±10 V	500 kSPS	±1 LSB	–55°C to +125°C	Q-24
AD7892AN-2	0 V to +2.5 V	500 kSPS		–40°C to +85°C	N-24
AD7892BN-2	0 V to +2.5 V	500 kSPS	±1 LSB	–40°C to +85°C	N-24
AD7892AR-2	0 V to +2.5 V	500 kSPS		–40°C to +85°C	R-24
AD7892BR-2	0 V to +2.5 V	500 kSPS	±1 LSB	–40°C to +85°C	R-24
AD7892AN-3	±2.5 V	600 kSPS		–40°C to +85°C	N-24
AD7892BN-3	±2.5 V	600 kSPS	±1 LSB	–40°C to +85°C	N-24
AD7892AR-3	±2.5 V	600 kSPS		–40°C to +85°C	R-24
AD7892BR-3	±2.5 V	600 kSPS	±1 LSB	–40°C to +85°C	R-24
EVAL-AD7892-2CB[2]	Evaluation Board				
EVAL-AD7892-3CB[2]	Evaluation Board				
EVAL-CONTROL BOARD[3]	Controller Board				

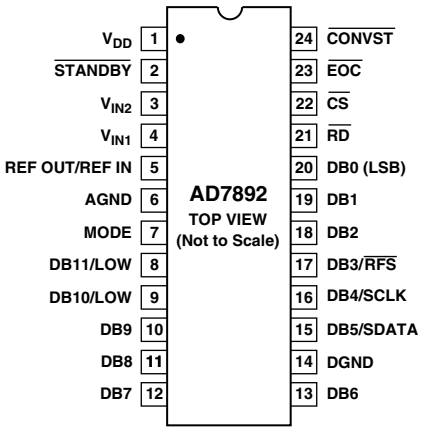
NOTES
[1]N = Plastic DIP; Q = Cerdip; R = SOIC.
[2]These boards can be used as stand-alone evaluation boards or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.
[3]This board is a complete unit allowing a PC to control and communicate with all Analog Devices' evaluation boards ending in the CB designators.

PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Description
1	V_{DD}	Positive Supply Voltage, +5 V ± 5%.
2	$\overline{\text{STANDBY}}$	Standby Input. Logic Input. With this input at a logic high, the part is in its normal operating mode; with this input at a logic low, the part is placed in its standby or power-down mode, which reduces power consumption to 5 mW typical.
3	V_{IN2}	Analog Input 2. For the AD7892-1, this input either connects to AGND or to V_{IN1} to determine the analog input voltage range. With V_{IN2} connected to AGND on the AD7892-1, the analog input range at the V_{IN1} input is ±10 V. With V_{IN2} connected to V_{IN1} on the AD7892-1, the analog input range to the part is ±5 V. For the AD7892-2 and AD7892-3, this input can be left unconnected but must not be connected to a potential other than AGND.
4	V_{IN1}	Analog Input 1. The analog input voltage to be converted by the AD7892 is applied to this input. For the AD7892-1, the input voltage range is either ±5 V or ±10 V depending on where the V_{IN2} input is connected. For the AD7892-2, the voltage range on the V_{IN1} input is 0 V to +2.5 V with respect to the voltage appearing at the V_{IN2} input. For the AD7892-3, the voltage range on the V_{IN1} input is ±2.5 V.
5	REF OUT/REF IN	Voltage Reference Output/Input. The part can be used with either its own internal reference or with an external reference source. The on-chip +2.5 V reference is provided at this pin. When using this internal reference as the reference source for the part, REF OUT should be decoupled to AGND with a 0.1 μF disc ceramic capacitor. The output impedance of this reference source is typically 5.5 kΩ. When using an external reference source as the reference voltage for the part, the reference source should be connected to this pin. This overdrives the internal reference and provides the reference source for the part. The REF IN input is buffered on-chip but must be able to sink or source current through the resistor to the output of the on-chip reference. The nominal reference voltage for correct operation of the AD7892 is +2.5 V.
6	AGND	Analog Ground. Ground reference for track/hold, comparator and DAC.
7	MODE	Mode. Control input which determines the interface mode for the AD7892. With this pin at a logic low, the device is in its serial interface mode; with this pin at a logic high, the device is in its parallel interface mode.
8	DB11/LOW	Data Bit 11/Test Pin. When the device is in its parallel mode, this pin is Data Bit 11 (MSB), a three-state TTL-compatible output. When the device is in its serial mode, this is used as a test pin which must be tied to a logic low for correct operation of the AD7892.
9	DB10/LOW	Data Bit 10/Test Pin. When the device is in its parallel mode, this pin is Data Bit 10, a three-state TTL-compatible output. When the device is in its serial mode, this is used as a test pin which must be tied to a logic low for correct operation of the AD7892.
10	DB9	Data Bit 9. Three-state TTL-compatible output. This output should be left unconnected when the device is in its serial mode.
11	DB8	Data Bit 8. Three-state TTL-compatible output. This output should be left unconnected when the device is in its serial mode.
12	DB7	Data Bit 7. Three-state TTL-compatible output. This output should be left unconnected when the device is in its serial mode.
13	DB6	Data Bit 6. Three-state TTL-compatible output. This output should be left unconnected when the device is in its serial mode.
14	DGND	Digital Ground. Ground reference for digital circuitry.
15	DB5/SDATA	Data Bit 5/Serial Data. When the device is in its parallel mode, this pin is Data Bit 5, a three-state TTL-compatible output. When the device is in its serial mode, this becomes the serial data output line. Sixteen bits of serial data are provided with four leading zeros preceding the 12 bits of valid data. Serial data is valid on the falling edge of SCLK for sixteen edges after $\overline{\text{RFS}}$ goes low. Output coding is two's complement for AD7892-1 and AD7892-3 and straight (natural) binary for AD7892-2.

Pin No.	Mnemonic	Description
16	DB4/SCLK	Data Bit 4/Serial Clock. When the device is in its parallel mode, this pin is Data Bit 4, a three-state TTL-compatible output. When the device is in its serial mode, this becomes the serial clock pin, SCLK. SCLK is an input and an external serial clock must be provided at this pin to obtain serial data from the AD7892. Serial data is clocked out from the output shift register on the rising edges of SCLK after $\overline{\text{RFS}}$ goes low.
17	DB3/$\overline{\text{RFS}}$	Data Bit 3/Receive Frame Synchronization. When the device is in its parallel mode, this pin is Data Bit 3, a three-state TTL-compatible output. When the device is in its serial mode, this becomes the receive frame synchronization input with $\overline{\text{RFS}}$ provided externally to obtain serial data from the AD7892.
18	DB2	Data Bit 2. Three-state TTL-compatible output. This output should be left unconnected when the device is in its serial mode.
19	DB1	Data Bit 1. Three-state TTL-compatible output. This output should be left unconnected when the device is in its serial mode.
20	DB0	Data Bit 0 (LSB). Three-state TTL-compatible output. Output coding is two's complement for AD7892-1 and AD7892-3 and straight (natural) binary for AD7892-2. This output should be left unconnected when the device is in its serial mode.
21	$\overline{\text{RD}}$	Read. Active low logic input which is used in conjunction with $\overline{\text{CS}}$ low to enable the data outputs.
22	$\overline{\text{CS}}$	Chip Select. Active low logic input which is used in conjunction with $\overline{\text{RD}}$ to enable the data outputs.
23	$\overline{\text{EOC}}$	End-of-Conversion. Active low logic output indicating converter status. The end of conversion is signified by a low going pulse on this line. The duration of this $\overline{\text{EOC}}$ pulse is nominally 100 ns.
24	$\overline{\text{CONVST}}$	Convert Start. Logic Input. A low-to-high transition on this input puts the track/hold into its hold mode and starts conversion.

PIN CONFIGURATION
DIP and SOIC



TERMINOLOGY

Signal to (Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\textit{Signal to (Noise + Distortion)} = (6.02\,N + 1.76)\ dB$$

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7892, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7892 is tested using two input frequencies away from the bottom end of the input bandwidth. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Relative Accuracy

Relative accuracy or endpoint nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Positive Full-Scale Error (AD7892-1)

This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal 4 × REF IN – 3/2 LSB (±10 V range) or 2 × REF IN – 3/2 LSB (±5 V range) after the bipolar zero error has been adjusted out.

Positive Full-Scale Error (AD7892-2)

This is the deviation of the last code transition (11 . . . 110 to 11 . . . 111) from the ideal (REF IN – 3/2 LSB) after the unipolar offset error has been adjusted out.

Positive Full-Scale Error (AD7892-3)

This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal (REF IN – 3/2 LSB) after the bipolar zero error has been adjusted out.

Bipolar Zero Error (AD7892-1, AD7892-3)

This is the deviation of the midscale transition (all 1s to all 0s) from the ideal (AGND – 1/2 LSB).

Unipolar Offset Error (AD7892-2)

This is the deviation of the first code transition (00 . . . 000 to 00 . . . 001) from the ideal (AGND + 1/2 LSB).

Negative Full-Scale Error (AD7892-1)

This is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal –4 × REF IN + 1/2 LSB (±10 V range) or –2 × REF IN + 1/2 LSB (±5 V range) after bipolar zero error has been adjusted out.

Negative Full-Scale Error (AD7892-3)

This is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal – REF IN + 1/2 LSB after bipolar zero error has been adjusted out.

Track/Hold Acquisition Time

Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (the point at which the track/hold returns to track mode). It also applies to situations where there is a step input change on the input voltage applied to the V_{IN} input of the AD7892. It means that the user must wait for the duration of the track/hold acquisition time after the end of conversion or after a step input change to V_{IN} before starting another conversion, to ensure that the part operates to specification.

CIRCUIT DESCRIPTION

The AD7892 is a fast, 12-bit single supply A/D converter. It provides the user with signal scaling, track/hold, reference, A/D converter and versatile interface logic functions on a single chip. The signal scaling on the AD7892-1 allows the part to handle either ±5 V or ±10 V input signals while operating from a single +5 V supply. The AD7892-2 handles a 0 V to +2.5 V analog input range, while signal scaling on the AD7892-3 allows it to handle ±2.5 V input signals when operating from a single supply. The part requires a +2.5 V reference which can be provided from the part's own internal reference or from an external reference source.

Conversion is initiated on the AD7892 by pulsing the $\overline{\text{CONVST}}$ input. On the rising edge of $\overline{\text{CONVST}}$, the track/hold goes from track mode to hold mode and the conversion sequence is started. At the end of conversion (falling edge of $\overline{\text{EOC}}$), the track/hold returns to tracking mode and the acquisition time begins. Conversion time for the part is 1.47 µs (AD7892-3) and the track/hold acquisition time is 200 ns (AD7892-3). This allows the AD7892-3 to operate at throughput rates up to 600 kSPS. The AD7892-1 and AD7892-2 are specified with a 1.6 µs conversion and 400 ns acquisition time allowing a throughput rate of 500 kSPS.

Track/Hold Section

The track/hold amplifier on the AD7892 allows the ADC to accurately convert an input sine wave of full-scale amplitude to 12-bit accuracy. The input bandwidth of the track/hold is greater than the Nyquist rate of the ADC even when the ADC is operated at its maximum throughput rate of 600 kHz (i.e., the track/hold can handle input frequencies in excess of 300 kHz).

The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 200 ns. The operation of the track/hold is essentially transparent to the user. The track/hold amplifier goes from its tracking mode to its hold mode on the rising edge of $\overline{\text{CONVST}}$. The aperture time for the track/hold (i.e., the delay time between the external $\overline{\text{CONVST}}$ signal and the track/hold actually going into hold) is typically 15 ns. At the end of conversion, the part returns to its tracking mode. The acquisition time of the track/hold amplifier begins at this point.

Reference Section

The AD7892 contains a single reference pin, labelled REF OUT/REF IN, which either provides access to the part's own +2.5 V reference or to which an external +2.5 V reference can be connected to provide the reference source for the part. The part is specified with a +2.5 V reference voltage. Errors in the reference source will result in gain errors in the AD7892's transfer function and will add to the specified full-scale errors on the part. On the AD7892-1 and AD7892-3, it will also result in an offset error injected in the attenuator stage.

The AD7892 contains an on-chip +2.5 V reference. To use this reference as the reference source for the AD7892, simply connect a 0.1 µF disc ceramic capacitor from the REF OUT/REF IN pin to AGND. The voltage that appears at this pin is internally buffered before being applied to the ADC. If this reference is required for use external to the AD7892, it should be buffered as the part has a FET switch in series with the reference output resulting in a source impedance for this output of 5.5 kΩ nominal. The tolerance on the internal reference is ±10 mV at 25°C with a typical temperature coefficient of 25 ppm/°C and a maximum error over temperature of ±25 mV.

If the application requires a reference with a tighter tolerance or the AD7892 needs to be used with a system reference, then the user has the option of connecting an external reference to this REF OUT/REF IN pin. The external reference will effectively overdrive the internal reference and thus provide the reference source for the ADC. The reference input is buffered before being applied to the ADC with the maximum input current is ±100 µA. Suitable reference sources for the AD7892 include the AD680, AD780 and REF43 precision +2.5 V references.

INTERFACING

The part provides two interface options, a 12-bit parallel interface and a three-wire serial interface. The required interface mode is selected via the MODE pin. The two interface modes are discussed in the following sections.

Parallel Interface Mode

The parallel interface mode is selected by tying the MODE input to a logic high. Figure 2 shows a timing diagram illustrating the operational sequence of the AD7892. The on-chip track/hold goes into hold mode, and conversion is initiated on the rising edge of the $\overline{\text{CONVST}}$ signal. When conversion is complete, the end of conversion line ($\overline{\text{EOC}}$) pulses low to indicate that new data is available in the AD7892's output register. This $\overline{\text{EOC}}$ line can be used to drive an edge-triggered interrupt of a microprocessor. The falling edge of the $\overline{\text{RD}}$ signal should occur 200 ns prior to the next rising edge of $\overline{\text{CONVST}}$. $\overline{\text{CS}}$ and $\overline{\text{RD}}$ going low accesses the 12-bit conversion result. In systems where the part is interfaced to a gate array or ASIC, this $\overline{\text{EOC}}$

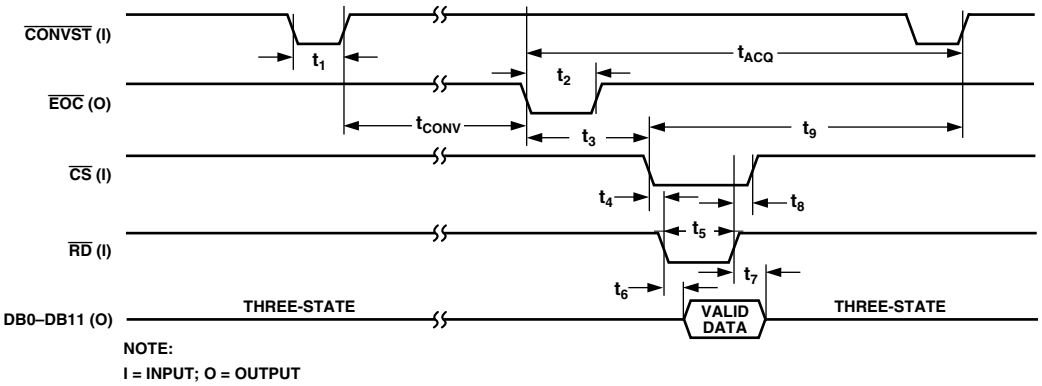


Figure 2. Parallel Mode Timing Diagram

pulse can be applied to the $\overline{CS}$ and $\overline{RD}$ inputs to latch data out of the AD7892 and into the gate array or ASIC. This eliminates the logic required in the gate array or ASIC to recognize the end of conversion and generate the read signal for the AD7892. To obtain optimum performance from the AD7892, it is not recommended to tie $\overline{CS}$ and $\overline{RD}$ permanently low as this keeps the three-state active during conversion.

Serial Interface Mode

The AD7892 is configured for serial mode interfacing by tying the MODE input low. It provides for a three-wire, serial link between the AD7892 and industry-standard microprocessors, microcontrollers and digital signal processors. SCLK and $\overline{RFS}$ of the AD7892 are inputs, and the AD7892's serial interface is designed for direct interface to systems that provide a serial clock input that is synchronized to the serial data output including microcontrollers such as the 80C51, 87C51, 68HC11 and 68HC05 and most digital signal processors.

Figure 3 shows the timing diagram for reading from the AD7892 in the serial interface mode. $\overline{RFS}$ goes low to access data from the AD7892. The serial clock input does not have to be continuous. The serial data can be accessed in a number of bytes. However, $\overline{RFS}$ must remain low for the duration of the data transfer operation. Sixteen bits of data are transmitted with four leading zeros followed by the 12-bit conversion result starting with the MSB. Serial data is clocked out of the device on the rising edge of SCLK. Old data is guaranteed to be valid for 5 ns after this edge. This is useful for high speed serial clocks where the access time of the part would not allow sufficient set-up time for the data to be accepted on the falling edge of the clock. In this case, care must be taken that $\overline{RFS}$ does not go just prior to a rising edge of SCLK. For slower serial clocks data is valid on the falling edge of SCLK. At the end of the read operation, the SDATA line is three-stated by a rising edge on either the SCLK or $\overline{RFS}$ inputs, whichever occurs first. Serial data cannot be read during conversion to avoid feedthrough problems from the serial clock to the conversion process. For optimum performance of the AD7892-3, a serial read should also be avoided within 200 ns of the rising edge of $\overline{CONVST}$ to avoid feedthrough into the track/hold during its acquisition time. The serial read should, therefore, occur between the end of conversion ($\overline{EOC}$ falling edge) and 200 ns prior to the next rising edge of $\overline{CONVST}$. For the AD7892-1 and AD7892-2, a serial read should also be avoided within 400 ns of the rising edge of $\overline{CONVST}$. This limits the maximum achievable throughput rate in serial mode (assuming 20 MHz serial clock) to 400 kSPS for the AD7892-3 and 357 kSPS for the AD7892-1 and AD7892-2.

Analog Input Section

The AD7892 is offered as three part types allowing for four different analog input voltage ranges. The AD7892-1 handles either ±5 V or ±10 V input voltage ranges. The AD7892-2 handles a 0 V to +2.5 V input voltage range while the AD7892-3 handles an input range of ±2.5 V.

AD7892-1

Figure 4 shows the analog input section for the AD7892-1. The analog input range is pin-strappable (using V_{IN2}) for either ±5 V or ±10 V on the V_{IN1} input. With V_{IN2} connected to AGND, the input range on V_{IN1} is ±10 V, and the input resistance on V_{IN1} is 15 kΩ nominal. With V_{IN2} connected to V_{IN1}, the input range on V_{IN1} is ±5 V, and the input resistance on V_{IN1} is 8 kΩ nominal. As a result, the V_{IN1} and V_{IN2} inputs should be driven from a low impedance source. The resistor attenuator stage is followed by the high input impedance stage of the track/hold amplifier. This resistor attenuator stage allows the input voltage to go to ±17 V without damaging the AD7892-1.

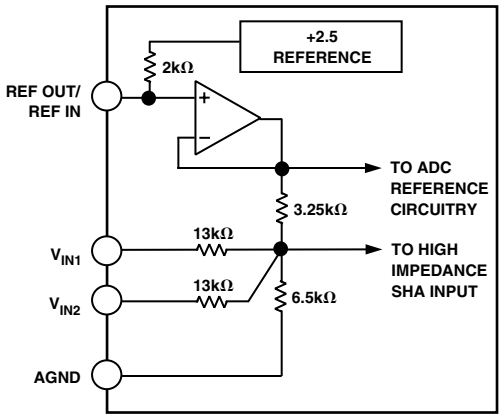


Figure 4. AD7892-1 Analog Input Structure

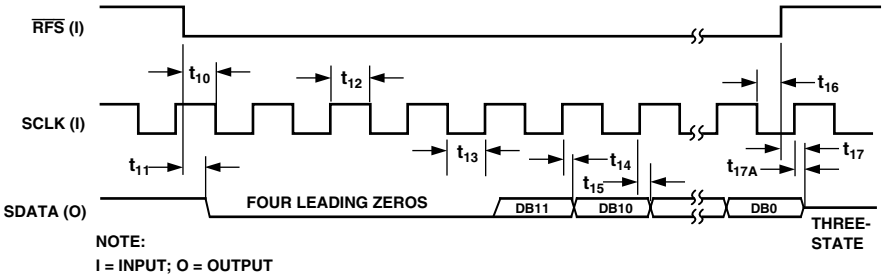


Figure 3. Serial Mode Timing Diagram

The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs). Output coding is two's complement binary with 1 LSB = FSR/4096 = 20 V/4096 = 4.88 mV for the ±10 V range and 1 LSB = FSR/4096 = 10 V/4096 = 2.44 mV for the ±5 V range. The ideal input/output transfer function for the AD7892-1 is shown in Table I.

AD7892-2

The analog input section for the AD7892-2 contains no biasing resistors. The analog input looks directly into the track/hold input stage. The analog input range on the V_{IN1} input is 0 V to +2.5 V. The V_{IN2} input can be left unconnected but if it is connected to a potential then that potential must be AGND. The V_{IN1} input connects directly to the input sampling capacitor of the AD7892-2's track/hold. The value of this input sampling capacitor is nominally 10 pF.

Once again, the designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs). Output coding is straight (natural) binary with 1 LSB = FSR/4096 = 2.5 V/4096 = 0.61 mV. The ideal input/output transfer function for the AD7892-2 is shown in Table II.

Table I. Ideal Input/Output Code Table for the AD7892-1

Analog Input	Digital Output Code Transition
+FSR/2 – 3/2 LSB[1, 2] (9.99268 or 4.99634)[3]	011 . . . 110 to 011 . . . 111
+FSR/2 – 5/2 LSBs (9.98779 or 4.99390)	011 . . . 101 to 011 . . . 110
+FSR/2 – 7/2 LSBs (9.98291 or 4.99146)	011 . . . 100 to 011 . . . 101
AGND + 3/2 LSB (0.00732 or 0.00366)	000 . . . 001 to 000 . . . 010
AGND + 1/2 LSB (0.00244 or 0.00122)	000 . . . 000 to 000 . . . 001
AGND – 1/2 LSB (–0.00244 or –0.00122)	111 . . . 111 to 000 . . . 000
AGND – 3/2 LSB (–0.00732 or –0.00366)	111 . . . 110 to 111 . . . 111
–FSR/2 + 5/2 LSB (–9.98779 or –4.99390)	100 . . . 010 to 100 . . . 011
–FSR/2 + 3/2 LSB (–9.99268 or –4.99634)	100 . . . 001 to 100 . . . 010
–FSR/2 + 1/2 LSB (–9.99756 or –4.99878)	100 . . . 000 to 100 . . . 001

NOTES
[1]FSR is full-scale range and REF IN = +2.5 V, is 20 V for the ±10 V range and 10 V for the ±5 V range.
[2]1 LSB = FSR/4096 = 4.88 mV (±10 V range) and 2.44 mV (±5 V range) with REF IN = +2.5 V.
[3]±10 V range or ±5 V range.

Table II. Ideal Input/Output Code Table for the AD7892-2

Analog Input	Digital Output Code Transition
+FSR – 3/2 LSB[1, 2] (2.499084 V)	111 . . . 110 to 111 . . . 111
+FSR – 5/2 LSBs (2.498474 V)	111 . . . 110 to 111 . . . 110
+FSR – 7/2 LSBs (2.497864 V)	111 . . . 100 to 111 . . . 101
AGND + 5/2 LSB (0.001526 V)	000 . . . 010 to 010 . . . 011
AGND + 3/2 LSB (0.00916 V)	000 . . . 001 to 001 . . . 010
AGND + 1/2 LSB (0.000305 V)	000 . . . 000 to 000 . . . 001

NOTES
[1]FSR is full-scale range and is 2.5 V with REF IN = +2.5 V.
[2]1 LSB = FSR/4096 = 0.61 mV with REF IN = +2.5 V.

AD7892-3

Figure 5 shows the analog input section for the AD7892-3. The analog input range is ±2.5 V on the V_{IN1} input. The V_{IN2} input can be left unconnected but if it is connected to a potential then that potential must be AGND. The input resistance on the V_{IN1} is 1.8 kΩ nominal. As a result, the V_{IN1} input should be driven from a low impedance source. The resistor attenuator stage is followed by the high input impedance stage of the track/hold amplifier. This resistor attenuator stage allows the input voltage to go to ±7 V without damaging the AD7892-3.

The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs). Output coding is two's complement binary with 1 LSB = FSR/4096 = 5 V/4096 = 1.22 mV with REF IN = +2.5 V. The ideal input/output transfer function for the AD7892-3 is shown in Table III.

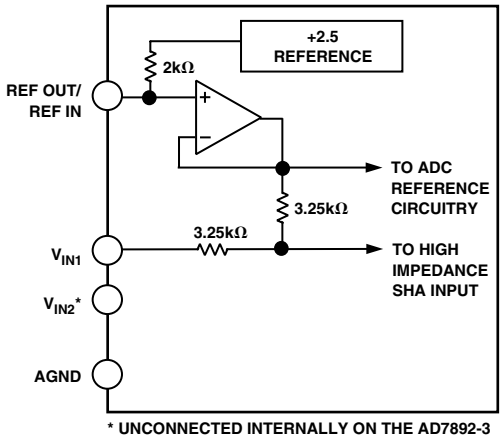


Figure 5. AD7892-3 Analog Input Structure

Table III. Ideal Input/Output Code Table for the AD7892-3

Analog Input	Digital Output Code Transition
+FSR/2 – 3/2 LSB[1, 2] (2.49817)	011 . . . 110 to 011 . . . 111
+FSR/2 – 5/2 LSBs (2.49695)	011 . . . 110 to 011 . . . 110
+FSR/2 – 7/2 LSBs (2.49573)	011 . . . 110 to 011 . . . 101
AGND + 3/2 LSB (0.00183)	000 . . . 001 to 000 . . . 010
AGND + 1/2 LSB (0.00061)	000 . . . 000 to 000 . . . 001
AGND – 1/2 LSB (–0.00061)	111 . . . 111 to 000 . . . 000
AGND – 3/2 LSB (–0.00183)	111 . . . 110 to 111 . . . 111
–FSR/2 + 5/2 LSB (–2.49695)	100 . . . 010 to 100 . . . 011
–FSR/2 + 3/2 LSB (–2.49817)	100 . . . 001 to 100 . . . 010
–FSR/2 + 1/2 LSB (–2.49939)	100 . . . 000 to 100 . . . 001

NOTES
[1]FSR is full-scale range and is 5 V with REF IN = +2.5 V.
[2]1 LSB = FSR/4096 = 1.22 mV with REF IN = +2.5 V.

MICROPROCESSOR INTERFACING

The AD7892 features both high speed parallel and serial interfaces, allowing considerable flexibility in interfacing to microprocessor systems. To obtain optimum performance from the part, data should not be read during conversion and this limits the achievable throughput rate in serial mode to 400 kSPS for the AD7892-3.

Figures 6, 7 and 9 show some typical interface circuits between the AD7892 and popular DSP processors. Figure 8 shows an interface between the part and a gate array or ASIC where data is clocked into the ASIC by the AD7892 itself at the end of conversion. In all cases, the $\overline{\text{CONVST}}$ signal is generated from an external timer to ensure equidistant sampling.

AD7892 to ADSP-2101 Interface

Figure 6 shows a parallel interface between the AD7892 and the ADSP-2101 DSP processor. $\overline{\text{CONVST}}$ starts conversion and at the end of conversion the falling edge of the $\overline{\text{EOC}}$ output provides an interrupt request to the ADSP-2101.

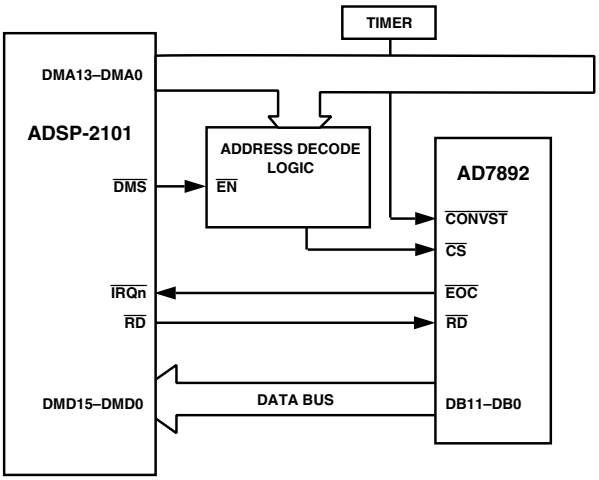


Figure 6. AD7892 to ADSP-2101

AD7892 to TMS320C25 Interface

Figure 7 shows a parallel interface between the AD7892 and the TMS320C25 DSP processor. $\overline{\text{CONVST}}$ starts conversion and at the end of conversion the falling edge of the $\overline{\text{EOC}}$ output provides an interrupt request to the TMS320C25.

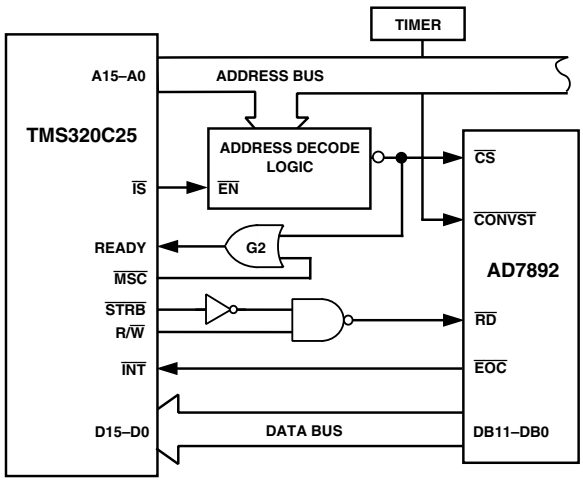


Figure 7. AD7892 to TMS320C25 Interface

EOC Pulse Provides $\overline{\text{CS}}$ and $\overline{\text{RD}}$

Figure 8 shows a parallel interface between the AD7892 and a gate array or ASIC. $\overline{\text{CONVST}}$ starts conversion and at the end of conversion the falling edge of the $\overline{\text{EOC}}$ output provides the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ pulse to latch data out of the AD7892 and into the gate array/ASIC. This scheme allows for the fastest possible throughput rate with the part as no time is lost in interrupt service routines and as soon as data is available from the part it is transferred out of it.

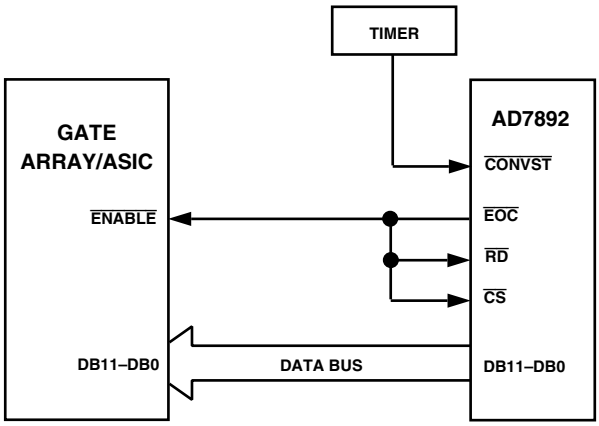


Figure 8. AD7892 to Gate Array/ASIC Interface

AD7892 to DSP56000 Interface

Figure 9 shows a serial interface between the AD7892 and the DSP56000 DSP processor. $\overline{\text{CONVST}}$ starts conversion and at the end of conversion the falling edge of the $\overline{\text{EOC}}$ output provides an interrupt request to the DSP56000.

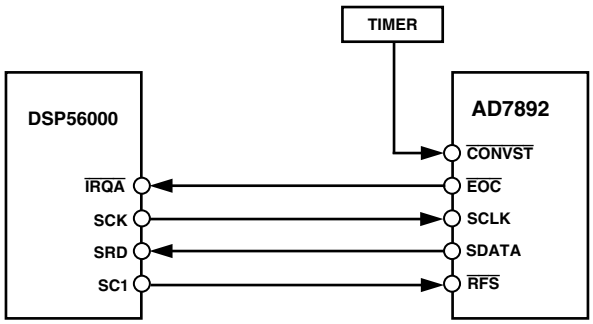


Figure 9. AD7892 to DSP56000 Interface

Grounding and Layout

The AD7892 has a single supply voltage pin, V_{DD}, which supplies both the analog and digital circuitry on the part. For optimum performance from the part, it is recommended that this +5 V is taken from the +5 V analog supply in the system. The analog and digital grounds to the AD7892 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The part exhibits good immunity to noise on the supplies but care must still be taken with regard to grounding and layout especially when using switching mode supplies.

The printed circuit board which houses the AD7892 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes which can be separated easily. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should only be joined in one place. If the AD7892 is the only device requiring an AGND to DGND connection, then the ground planes should be connected at the AGND and DGND pins of the AD7892. If the AD7892 is in a system where multiple devices require AGND to DGND connections, the connection should still be made at one point only, a star ground point which should be established as close as possible to the AD7892.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7892 to avoid noise coupling. The power supply lines to the AD7892 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. All analog supplies should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to AGND. To achieve the best from these decoupling components, they have to be placed as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1 µF disc ceramic capacitors to DGND. It is recommended that the system's AV_{DD} supply is used to supply the V_{DD} for the AD7892. This supply should have the recommended analog supply decoupling capacitors between the V_{DD} pin of the AD7892 and AGND and the recommended digital supply decoupling capacitor between the V_{DD} pin of the AD7892 and DGND.

Evaluating the AD7892 Performance

The recommended layout for the AD7892 is outlined in the evaluation board for the AD7892. The evaluation board package includes a fully assembled and tested evaluation board, documentation and software for controlling the board from a PC using the EVAL-CONTROL BOARD. The EVAL-CONTROL BOARD can be used in conjunction with the AD7892 evaluation board, as well as many other Analog Devices evaluation boards ending in the CB designator. Using the EVAL-CONTROL BOARD with the AD7892 evaluation board allows the user to evaluate the ac and dc performance of the AD7892 on a PC.

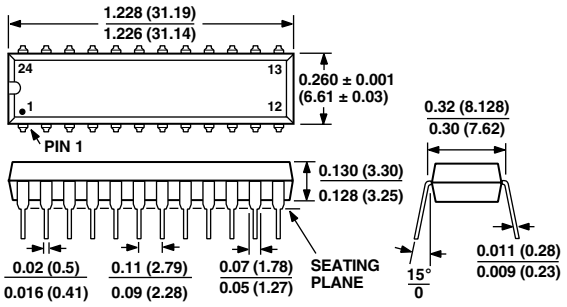
The software provided with the evaluation board allows the user to perform ac (Fast Fourier Transform) and dc (histogram of codes) tests on the AD7892. The evaluation board can also be used in a stand-alone fashion without the EVAL-CONTROL BOARD but in this case, the user has to write their own software to evaluate the part. There are two versions of the evaluation board available, one for the AD7892-2 and one for the AD7892-3. To order the AD7892-2 evaluation board, the order number is EVAL-AD7892-2CB and to order the AD7892-3 evaluation board, the order number is EVAL-AD7892-3CB.

AD7892

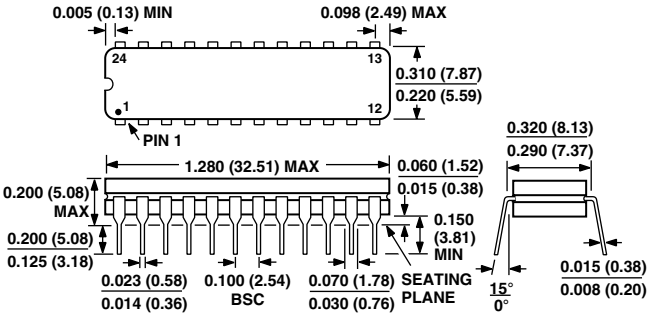
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

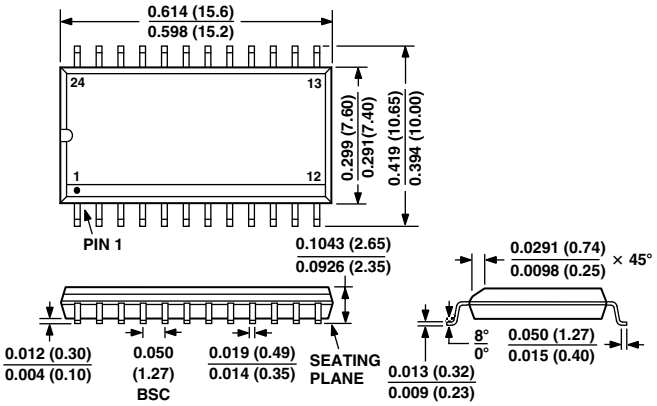
Plastic DIP (N-24)



Cerdip (Q-24)



SOIC (R-24)



C1933c–2.5–6/00 (rev. C) 01359

PRINTED IN U.S.A.

LM193, LM293, LM393

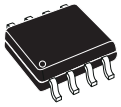
Low power dual voltage comparators

Datasheet –production data

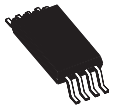
Features

- Wide single-supply voltage range or dual supplies: +2 V to +36 V or ±1 V to ±18 V
- Very low supply current (0.45 mA) independent of supply voltage (1 mW/comparator at +5 V)
- Low input bias current: 20 nA typ.
- Low input offset current: ±3 nA typ.
- Low input offset voltage: ±1 mV typ.
- Input common-mode voltage range includes ground
- Low output saturation voltage: 80 mV typ. (I_{sink} = 4 mA)
- Differential input voltage range equal to the supply voltage
- TTL, DTL, ECL, MOS, CMOS compatible outputs
- Available in DIP8, SO-8, TSSOP8, MiniSO-8, and DFN8 2 x 2 mm packages

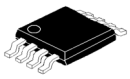
DIP8
(plastic package)



SO-8
(plastic micropackage)



TSSOP8
(thin shrink small outline package)



MiniSO-8
(plastic micropackage)

DFN8 2 x 2 mm
(plastic micropackage)

Description

The LM193, LM293, and LM393 devices consist of two independent low voltage comparators designed specifically to operate from a single supply over a wide range of voltages. Operation from split power supplies is also possible.

These comparators also have a unique characteristic in that the input common-mode voltage range includes ground even though operated from a single power supply voltage.

This is information on a product in full production. www.st.com

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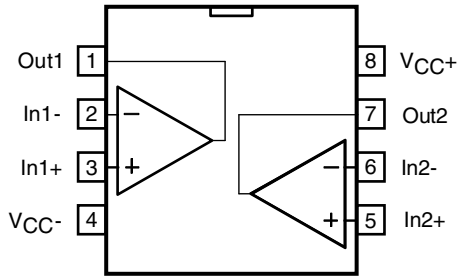
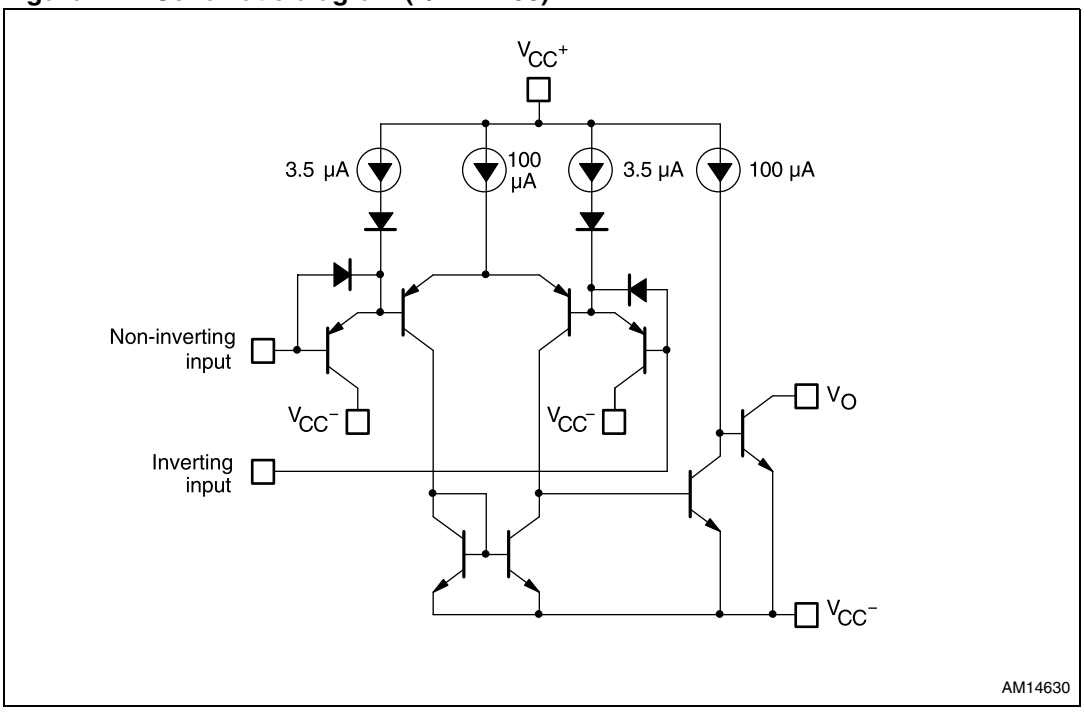
1 Pin connections

Figure 1. Pin connections (top view)



2 Schematic diagram

Figure 2. Schematic diagram (1/2 LM193)



3 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	±18 or 36	V
V_{id}	Differential input voltage	±36	V
V_{in}	Input voltage	-0.3 to +36	V
	Output short-circuit to ground(1)	Infinite	
R_{thja}	Thermal resistance junction to ambient(2) SO-8 TSSOP8 DIP8 MiniSO-8 DFN8 2 x 2 mm	 125 120 85 190 57	°C/W
R_{thjc}	Thermal resistance junction to case(2) SO-8 TSSOP8 DIP8 MiniSO-8 DFN8 2 x 2 mm	 40 37 41 39	°C/W
T_j	Maximum junction temperature	150	°C
T_{stg}	Storage temperature range	-65 to +150	°C
ESD Class(3)	HBM: human body model	H1B	
	MM: machine model	M2	
	CDM: charged device model	C5	

1. Short-circuits from the output to V_{CC}+ can cause excessive heating and potential destruction. The maximum output current is approximately 20 mA independent of the magnitude of V_{CC}+.
2. Short-circuits can cause excessive heating and destructive dissipation. Values are typical.
3. ESD class definition from AEC-Q100:
HBM class H1B: ESD voltage level from 500 V to 1000 V
MM class M2: ESD voltage level from 100 V to 200 V
CDM class C5: ESD voltage level greater than 1500 V.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (V_{CC}^+ - V_{CC}^-)	2 to 36	V
V_{icm}	Common mode input voltage range (V_{CC}^+= 30 V)(1) T_{amb} = +25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 0 to V_{CC}^+ -1.5 0 to V_{CC}^+ -2	V
T_{oper}	Operating free-air temperature range LM193, LM193A LM293, LM293A LM393, LM393A	 -55 to +125 -40 to +105 0 to +70	°C

1. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The high end of the common-mode voltage range is V_{CC}^+ -1.5 V, but either or both inputs can go to +30 V without damage.

4 Electrical characteristics

Table 3. V_{CC}^+ = +5V, V_{CC}^-= 0V, T_{amb} = +25 °C (unless otherwise specified)

Symbol	Parameter	LM193A - LM293A LM393A			LM193- LM293 LM393			Unit
		Min.	Typ.	Max.	Min	Typ.	Max.	
V_{io}	Input offset voltage(1) $T_{min} \leq T_{amb} \leq T_{max}$		1	2 4		1	5 9	mV
I_{io}	Input offset current $T_{min} \leq T_{amb} \leq T_{max}$		3	25 100		3	50 150	nA
I_{ib}	Input bias current (I^+ or I^-)(2) $T_{min} \leq T_{amb} \leq T_{max}$		20	100 300		20	250 400	nA
A_{vd}	Large signal voltage gain V_{CC} = 15 V, R_L = 15 kΩ, V_o = 1 V to 11 V	50	200		50	200		V/mV
I_{CC}	Supply current (all comparators) V_{CC} = +5 V, no load V_{CC} = +30 V, no load		0.45 0.6	1 2.5		0.45 0.6	1 2.5	mA
V_{id}	Differential input voltage(3)			V_{CC}^+			V_{CC}^+	
V_{OL}	Low level output voltage V_{id} = -1 V, I_{sink} = 4 mA $T_{min} \leq T_{amb} \leq T_{max}$		80	400 700		80	400 700	mV
I_{OH}	High level output current V_{CC} = V_o = 30 V, V_{id} = 1 V $T_{min} \leq T_{amb} \leq T_{max}$		0.1	 1		0.1	 1	nA µA
I_{sink}	Output sink current V_{id}= 1 V, V_o = 1.5 V	6	18		6	18		mA
t_{re}	Response time (4) R_L= 5.1 kΩ connected to V_{CC}^+		1.3			1.3		µs
t_{rel}	Large signal response time R_L= 5.1 kΩ connected to V_{CC}^+ e_I = TTL,$V_{(ref)}$ = +1.4 V		300			300		ns

1. At output switch point, $V_o \approx$ 1.4 V, R_s = 0 with V_{CC}^+ from 5 V to 30 V, and over the full common-mode range (0 V to V_{CC}^+ -1.5 V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading charge exists on the reference of input lines.
3. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3 V (or 0.3 V below the negative power supply, if used).
4. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained.

Figure 3. Supply current vs. supply voltage

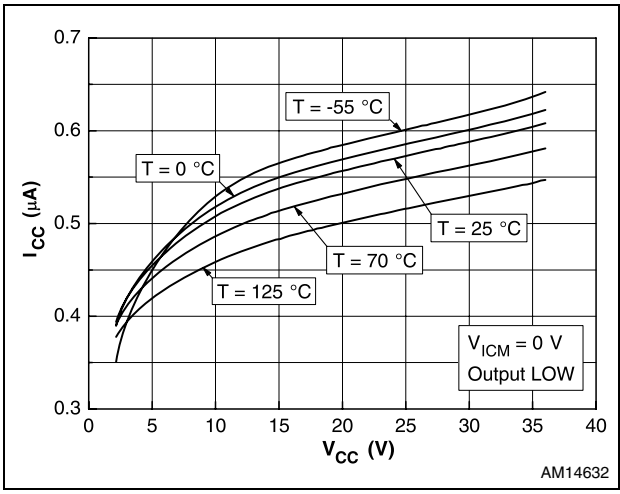


Figure 4. Input current vs. supply voltage

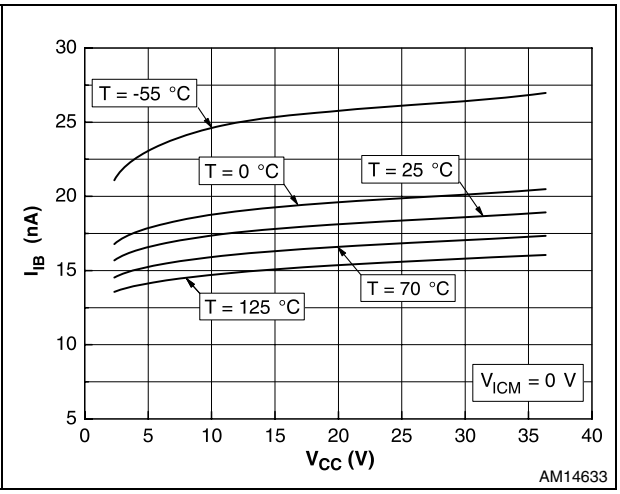


Figure 5. Output saturation voltage vs. output current

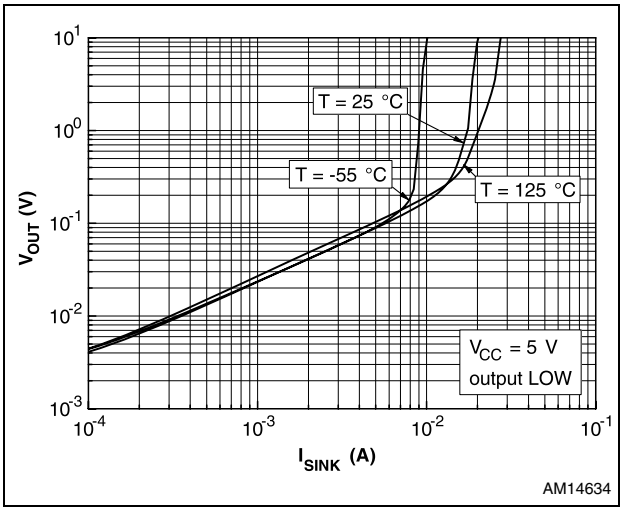


Figure 6. Response time for various input overdrives - negative transition

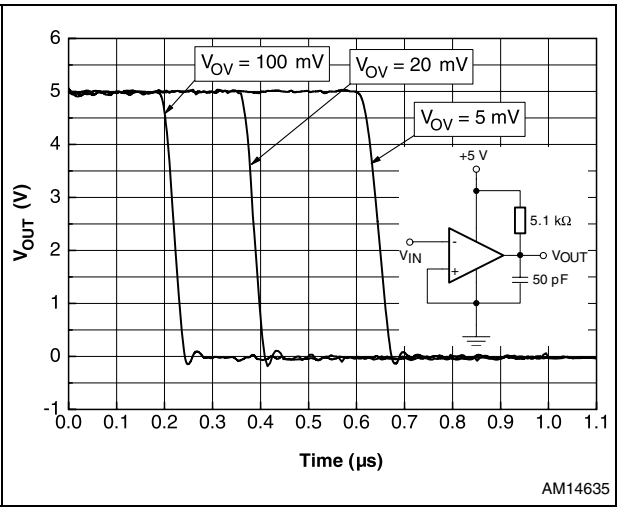
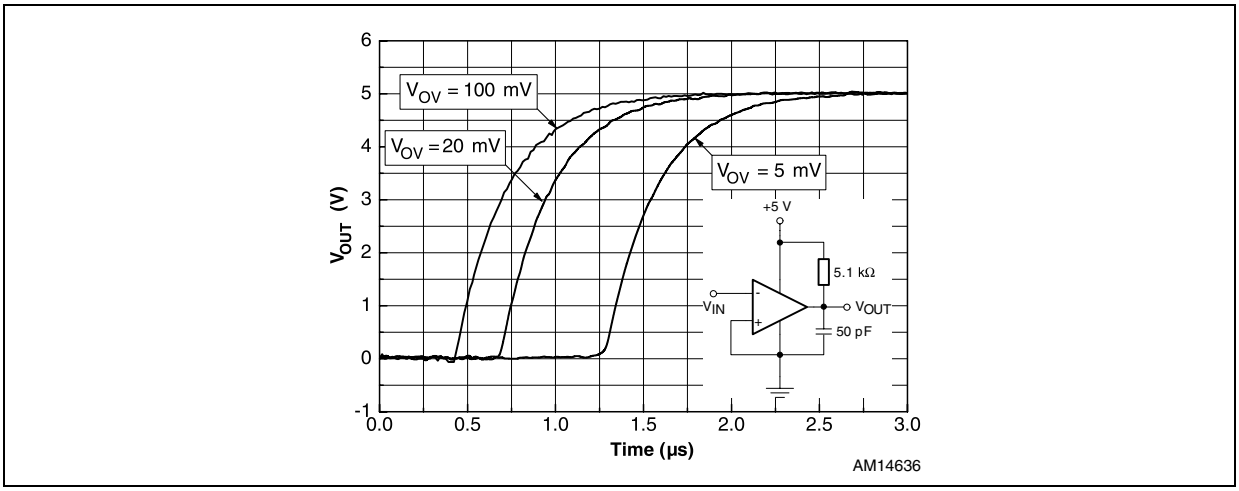


Figure 7. Response time for various input overdrives - positive transition



5 Typical applications

Figure 8. Basic comparator

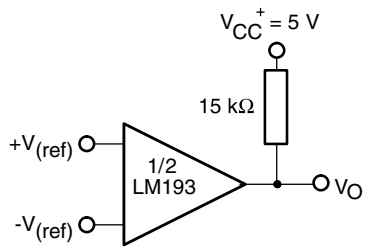


Figure 9. Driving TTL

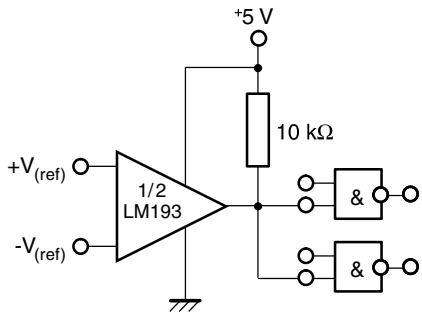


Figure 10. Low frequency op amp

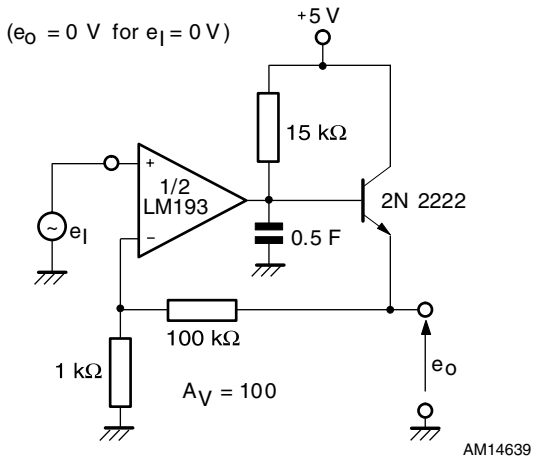


Figure 11. Driving CMOS

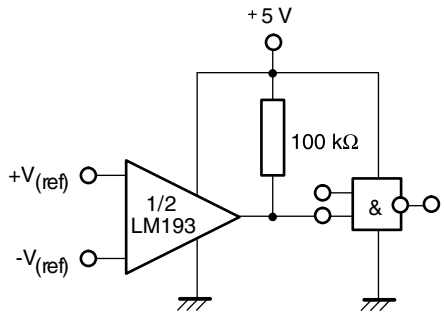


Figure 12. Low frequency op amp

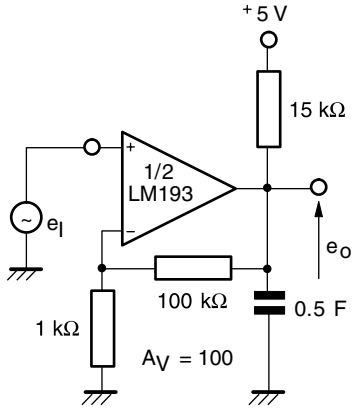


Figure 13. Transducer amplifier

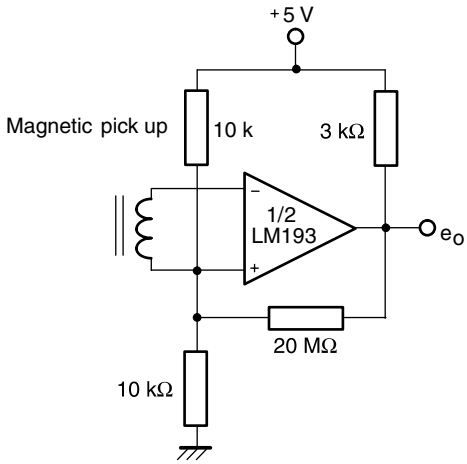


Figure 14. Low frequency op amp with offset adjust

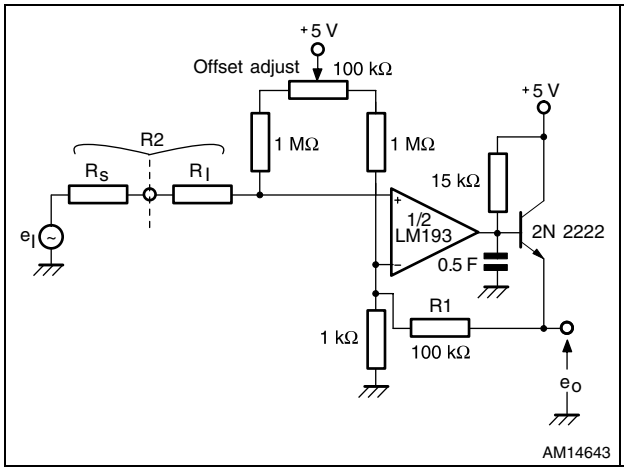


Figure 15. Zero crossing detector (single power supply)

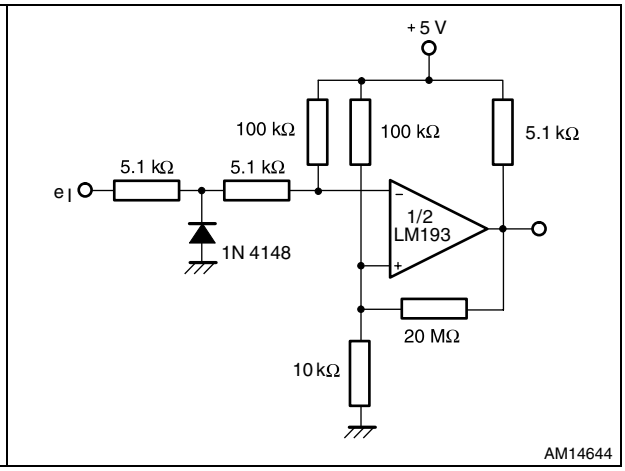


Figure 16. Limit comparator

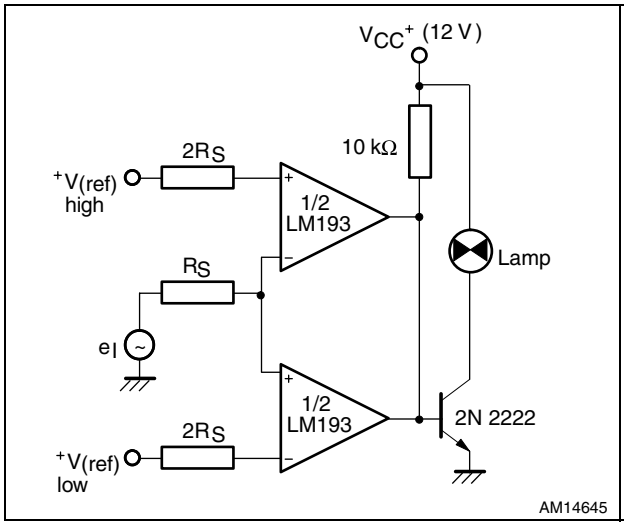


Figure 17. Crystal controlled oscillator

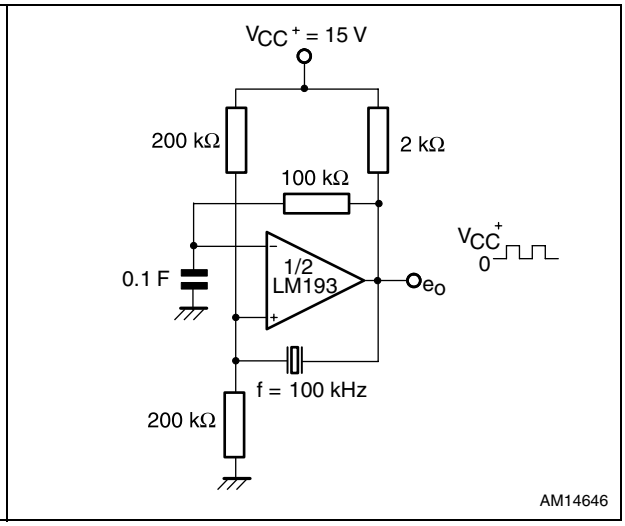


Figure 18. Split-supply applications - zero crossing detector

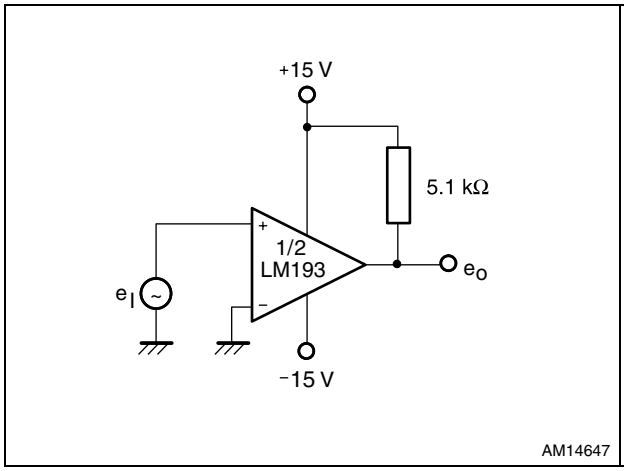


Figure 19. Comparator with a negative reference

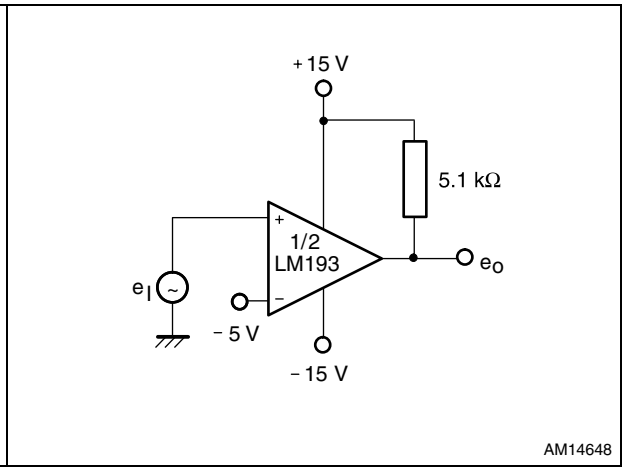
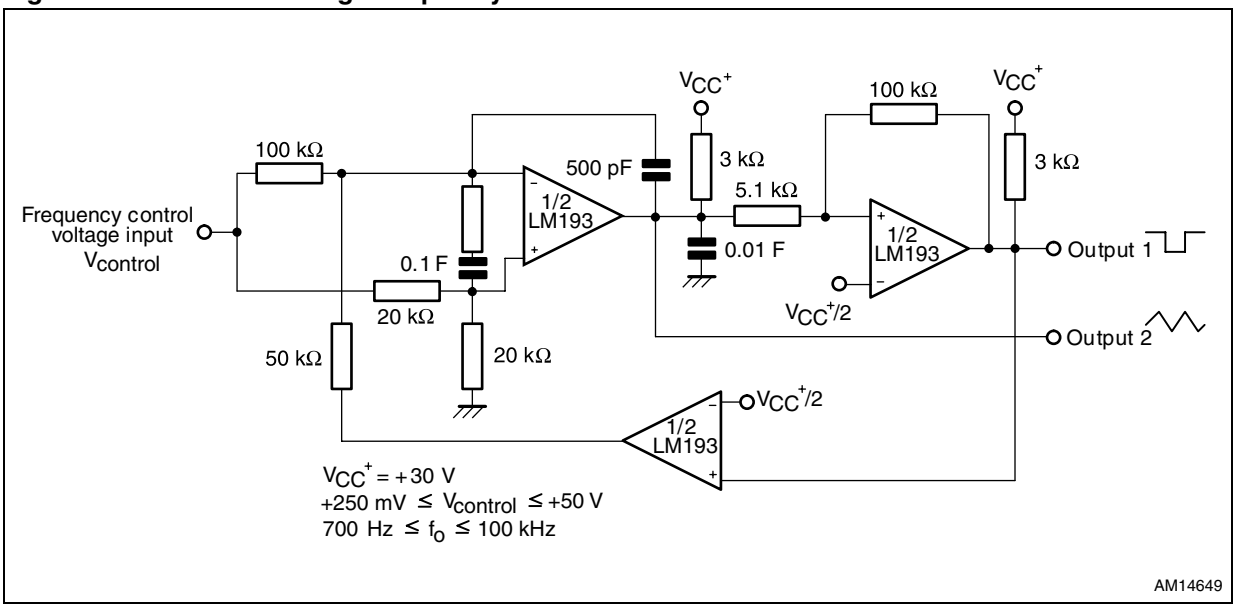


Figure 20. Two-decade high frequency VCO



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

6.1 DIP8 package information

Figure 21. DIP8 package outline

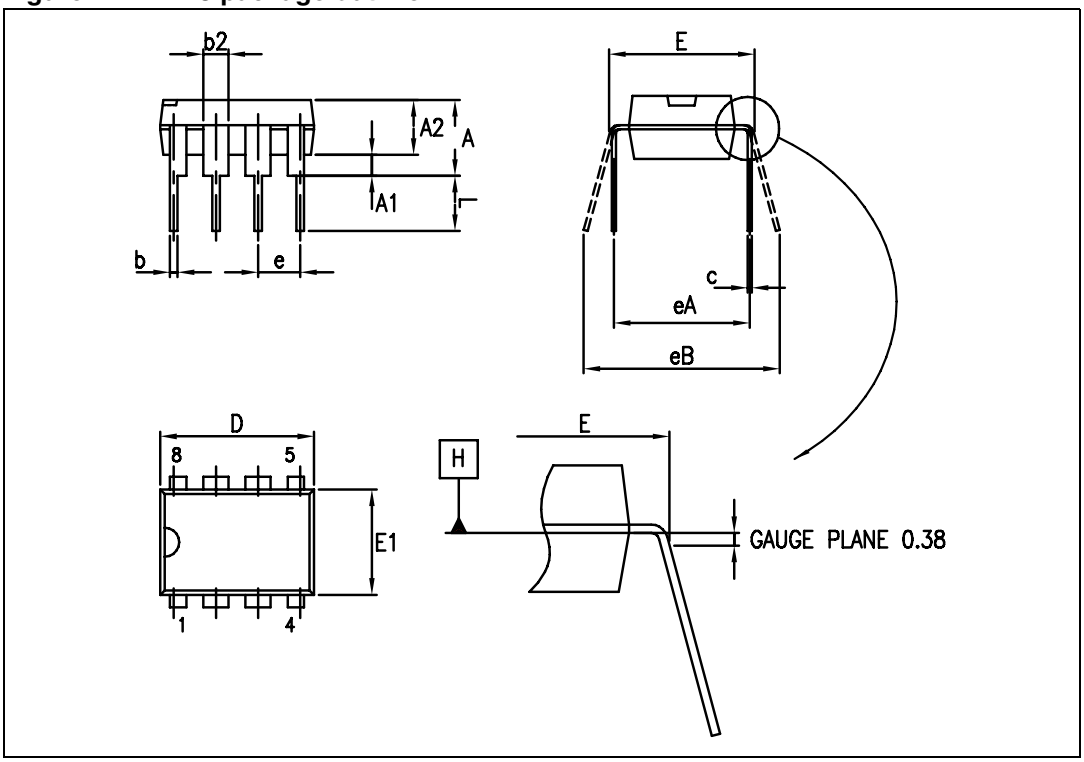


Table 4. DIP8 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
e		2.54			0.100	
eA		7.62			0.300	
eB			10.92			0.430
L	2.92	3.30	3.81	0.115	0.130	0.150

6.2 SO-8 package information

Figure 22. SO-8 package outline

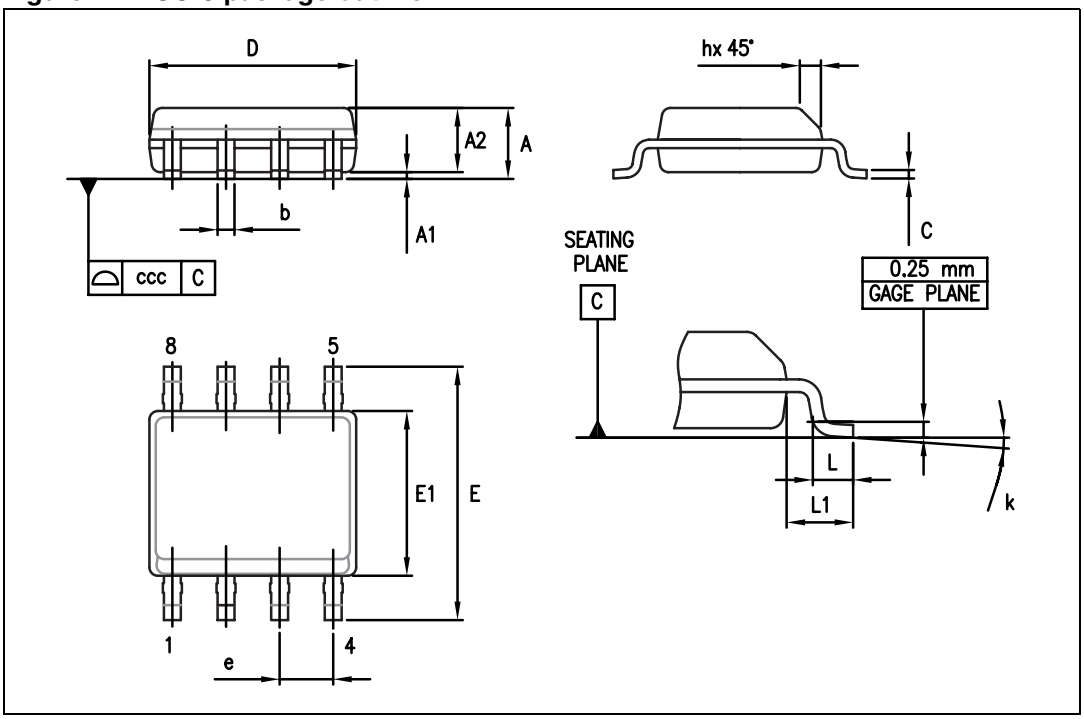


Table 5. SO-8 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0		8°	1°		8°
ccc			0.10			0.004

6.3 TSSOP8 package information

Figure 23. TSSOP8 package outline

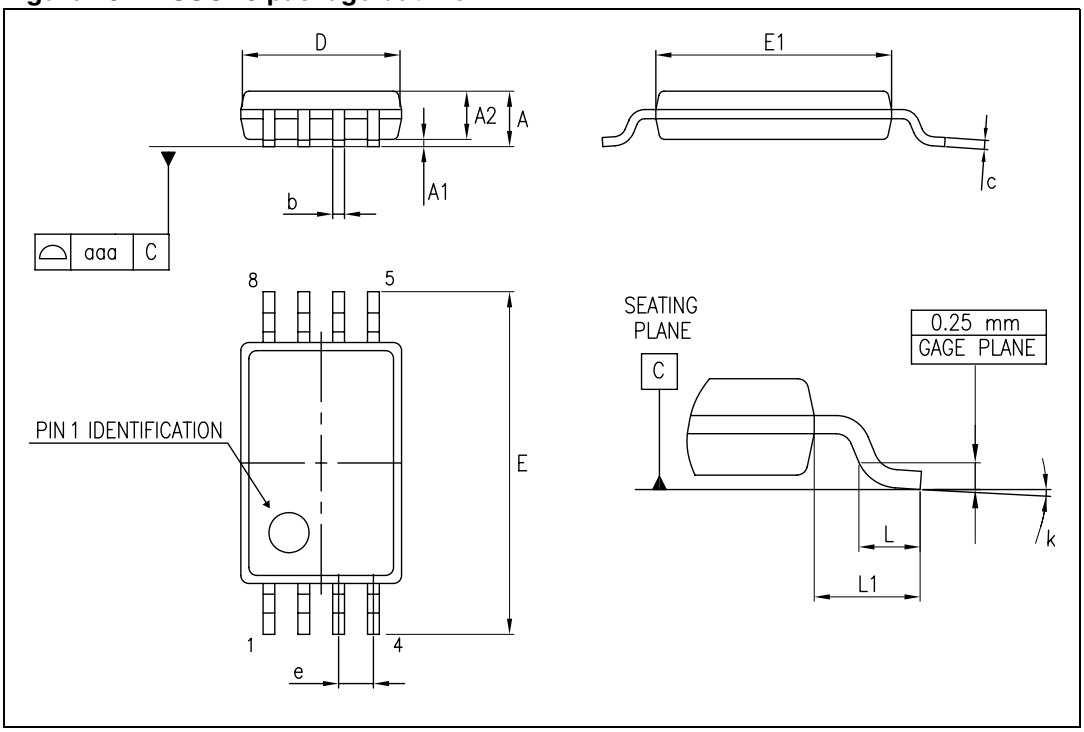


Table 6. TSSOP8 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa			0.10			0.004

6.4 MiniSO-8 package information

Figure 24. MiniSO-8 package outline

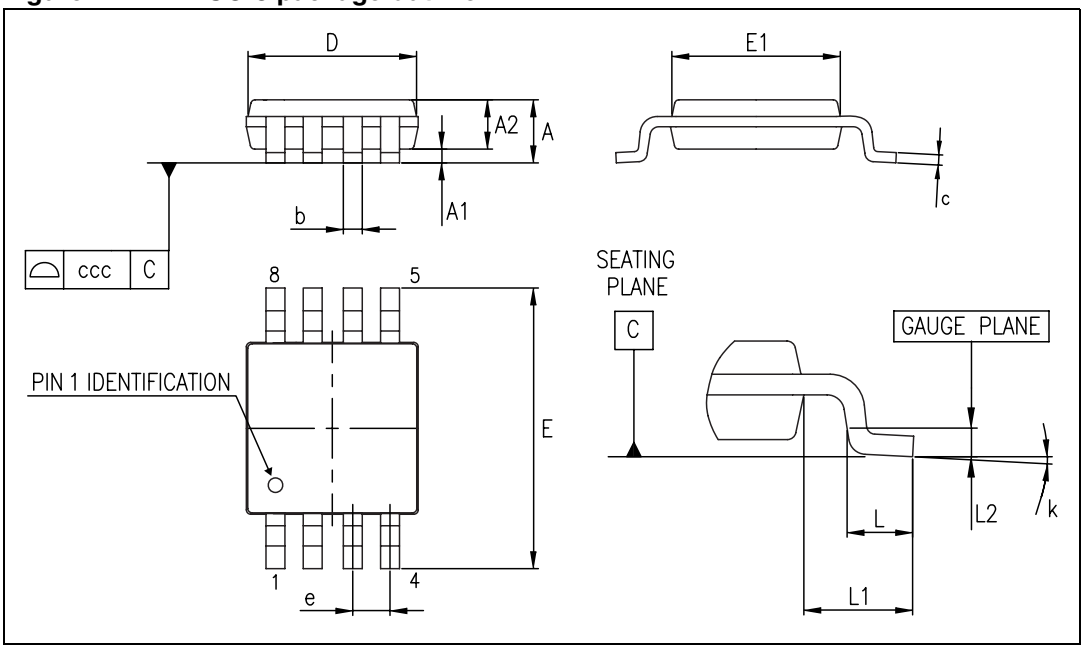


Table 7. MiniSO-8 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

6.5 DFN8 package information

Figure 25. DFN8 2 x 2 x 0.6 mm package outline (pitch 0.5 mm)

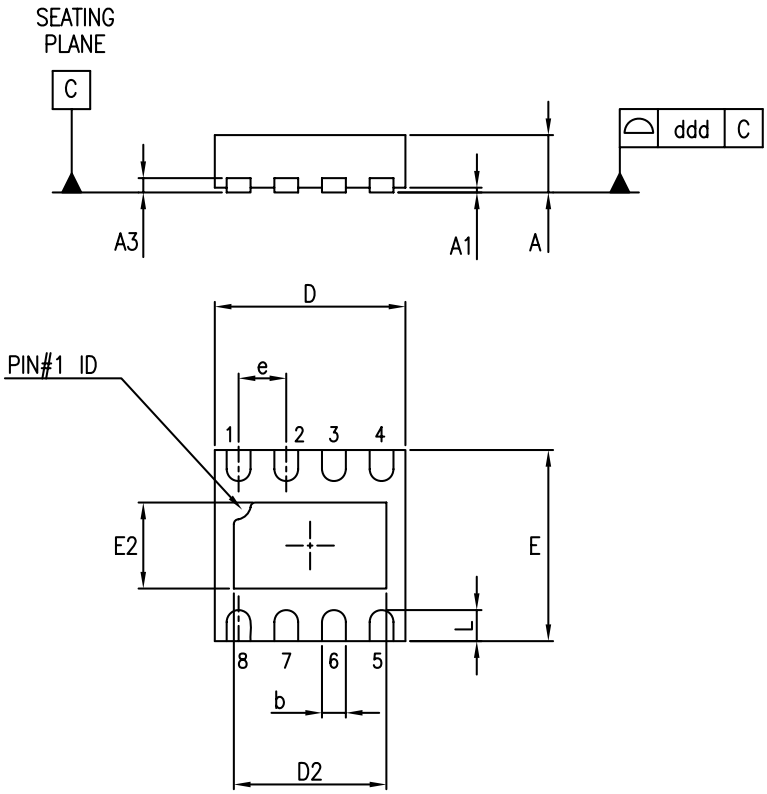
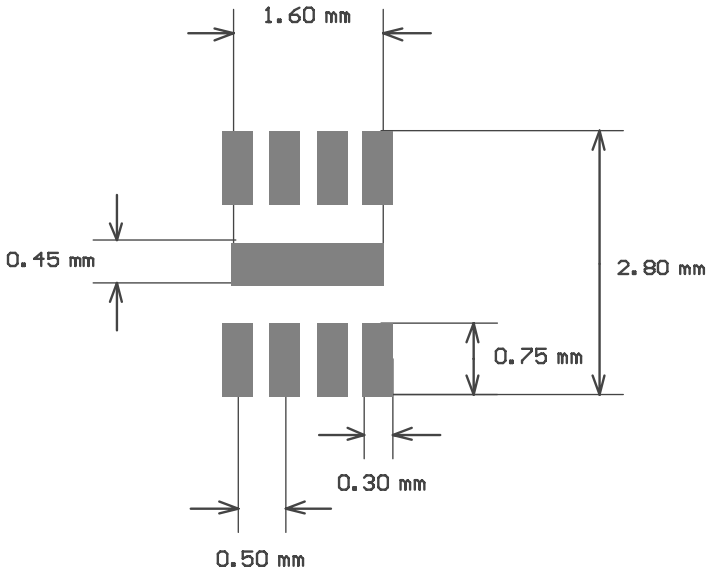


Table 8. DFN8 2 x 2 x 0.6 mm package mechanical data (pitch 0.5 mm)

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
e		0.50			0.020	
L			0.50			0.020
ddd			0.08			0.003

Figure 26. DFN8 2 x 2 footprint recommendation



7 Ordering information

Table 9. Order codes

Order code	Temperature range	Package	Packing	Marking
LM193AD LM193ADT	-55 °C, +125 °C	SO-8	Tube or tape and reel	193A
LM193D LM193DT				193
LM193AN		DIP8	Tube	LM193AN
LM193N				LM193N
LM293AD LM293ADT	-40 °C, +105 °C	SO-8	Tube or tape and reel	293A
LM293D LM293DT				293
LM293AN		DIP8	Tube	LM293AN
LM293N				LM293N
LM293PT		TSSOP8	Tape and reel	293
LM293ST		MiniSO-8	Tape and reel	K512
LM293QT		DFN8 2 x 2	Tape and reel	K59
LM393AD LM393ADT	0 °C, +70 °C	SO-8	Tube or tape and reel	393A
LM393D LM393DT				393
LM393AN		DIP8	Tube	LM393AN
LM393N				LM393N
LM393PT		TSSOP8	Tape and reel	393
LM393ST		MiniSO-8	Tape and reel	M393
LM393QT		DFN8 2 x 2	Tape and reel	K5C

8 Revision history

Table 10. Document revision history

Date	Revision	Changes
02-Jul-2002	1	First release.
02-Jan-2005	2	Class A of the product included in the datasheet.
02-May-2005	3	PPAP references inserted in the datasheet, see *Table 7: Ordering information on page 18*.
02-Jul-2005	4	Modification on PPAP references - Errors on part numbers, see *Table 7: Ordering information on page 18*.
22-Nov-2005	5	Modification on *Table 3 on page 6*. LM293,A must be -40/+105°C instead of -40/+125°C.
16-Feb-2006	6	Unit error for V_{ol} parameter see *Table 3 on page 6*.
23-Aug-2007	7	Corrected error in DIP8 package information related to lead thickness, see *Figure 21 on page 12*. Added values for R_{thja} and R_{thjc}, and ESD parameters in *Table 1: Absolute maximum ratings*.
08-Nov-2007	8	Updated MiniSO-8 package information. Reformatted package information. Added automotive grade order codes.
19-Feb-2008	9	Corrected error in SO-8 package mechanical data: E dimension in drawing was marked with an F in table.
15-Dec-2008	10	Corrected heading in *Figure 5*.
22-Feb-2010	11	Deleted automotive grade order codes for LM293 and LM393.
22-Jun-2011	12	Updated typical performance curves. Updated typical values on *Table 3 on page 6*. Updated ESD parameters with ESD classes in *Table 1: Absolute maximum ratings*. Added DFN8 2x2mm package mechanical drawing. Added DFN8 2x2mm recommended footprint. Added DFN8 2x2mm order codes in *Table 9*.
27-Jun-2012	13	Updated *Features* (added package information), *Description* (added RPNs), *Figure 1: Pin connections (top view)* moved to page 3, added *Contents*, updated marking of the LM293QT device in *Table 9*, minor text corrections throughout document.
18-Jan-2013	14	Updated *Table 8* (added dimensions in inches).

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LOC	DIST
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REVISIONS

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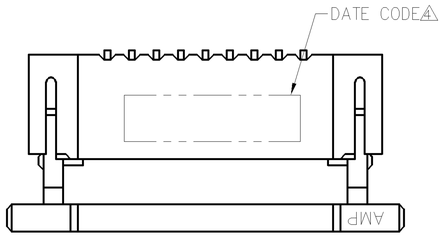
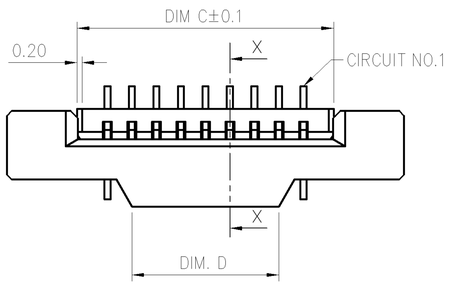
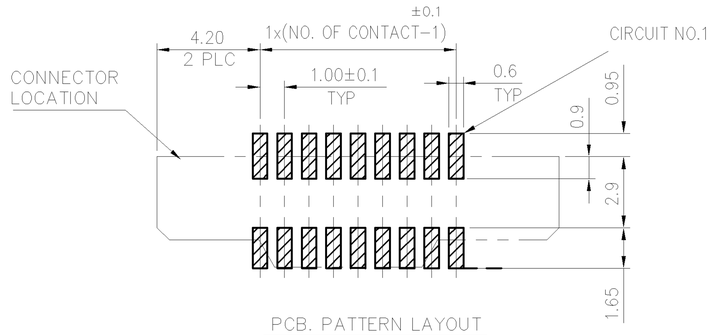
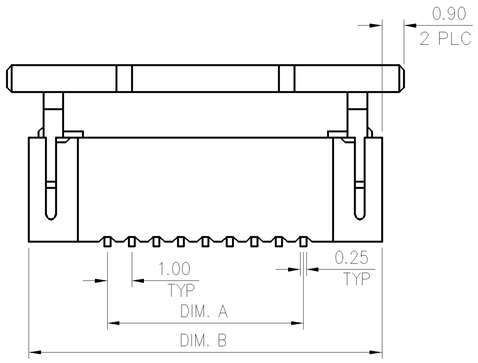


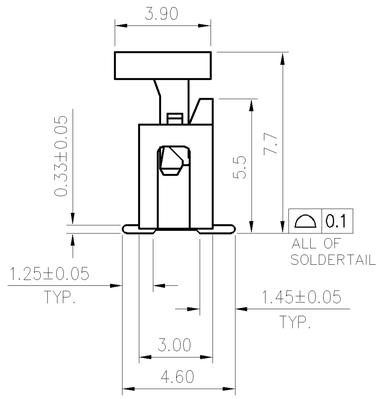


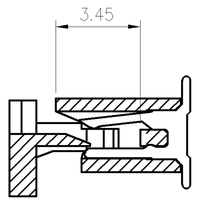


PCB. PATTERN LAYOUT

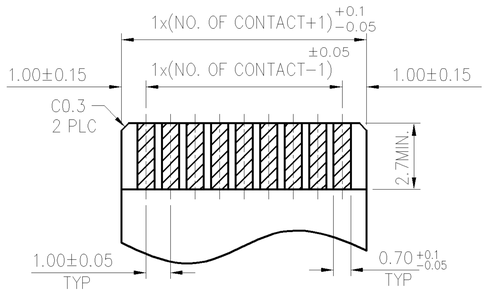
NOTES:
1. MATERIAL:
 1.1 HOUSING: THERMOPLASTIC (PA9T)
 UL94 V-0, COLOR: BLACK.
 1.2 ACTUATOR: THERMOPLASTIC (PA9T)
 UL94 V-0, COLOR: BLACK.
 1.3 CONTACTS: PHOSPHOR BRONZE
2. FINISH:
 2.1 CONTACT:
 GOLD FLASH PLATING OVERALL.
 1.27μm (50μ") MIN. NICKEL UNDERPLATING OVERALL.
3. REFLOW SOLDER CAPABLE TO 260°C PER TEC-109-201, CONDITION B.
⚠ WITHOUT DATE CODE FOR 8 POSITION UNDER.







SECTION X-X



APPLICABLE FPC RECOMMENDED DIMENSION
(THICKNESS: 0.3±0.05)

	DIM D	DIM C	DIM B	DIM A	POS.	PART NUMBER
	37	41.40	45.6	39.0	40	4-1734248-0
OBSOLETE	~~36~~	~~40.40~~	~~44.6~~	~~38.0~~	~~39~~	~~3-1734248-9~~
	~~35~~	~~39.40~~	~~43.6~~	~~37.0~~	~~38~~	~~3-1734248-8~~
	~~34~~	~~38.40~~	~~42.6~~	~~36.0~~	~~37~~	~~3-1734248-7~~
	~~33~~	~~37.40~~	~~41.6~~	~~35.0~~	~~36~~	~~3-1734248-6~~
	~~32~~	~~36.40~~	~~40.6~~	~~34.0~~	~~35~~	~~3-1734248-5~~
	~~31~~	~~35.40~~	~~39.6~~	~~33.0~~	~~34~~	~~3-1734248-4~~
	~~30~~	~~34.40~~	~~38.6~~	~~32.0~~	~~33~~	~~3-1734248-3~~
	~~29~~	~~33.40~~	~~37.6~~	~~31.0~~	~~32~~	~~3-1734248-2~~
	~~28~~	~~32.40~~	~~36.6~~	~~30.0~~	~~31~~	~~3-1734248-1~~
	27	31.40	35.6	29.0	30	3-1734248-0
	26	30.40	34.6	28.0	29	2-1734248-9
	25	29.40	33.6	27.0	28	2-1734248-8
	24	28.40	32.6	26.0	27	2-1734248-7
	23	27.40	31.6	25.0	26	2-1734248-6
	22	26.40	30.6	24.0	25	2-1734248-5
	21	25.40	29.6	23.0	24	2-1734248-4
OBSOLETE	~~20~~	~~24.40~~	~~28.6~~	~~22.0~~	~~23~~	~~2-1734248-3~~
	19	23.40	27.6	21.0	22	2-1734248-2
	18	22.40	26.6	20.0	21	2-1734248-1
	17	21.40	25.6	19.0	20	2-1734248-0
	16	20.40	24.6	18.0	19	1-1734248-9
	15	19.40	23.6	17.0	18	1-1734248-8
	14	18.40	22.6	16.0	17	1-1734248-7
	13	17.40	21.6	15.0	16	1-1734248-6
	12	16.40	20.6	14.0	15	1-1734248-5
	11	15.40	19.6	13.0	14	1-1734248-4
	10	14.40	18.6	12.0	13	1-1734248-3
	9	13.40	17.6	11.0	12	1-1734248-2
	8	12.40	16.6	10.0	11	1-1734248-1
	7	11.40	15.6	9.0	10	1-1734248-0
	6	10.40	14.6	8.0	9	1734248-9
	5	9.40	13.6	7.0	8	1734248-8
	4	8.40	12.6	6.0	7	1734248-7
	3	7.40	11.6	5.0	6	1734248-6
	2	6.40	10.6	4.0	5	1734248-5
	2	5.40	9.6	3.0	4	1734248-4
	2	4.40	8.6	2.0	3	1734248-3

THIS DRAWING IS A CONTROLLED DOCUMENT.

DIMENSIONS: mm

TOLERANCES UNLESS OTHERWISE SPECIFIED:

0 PLC	± -
1 PLC	± 0.3
2 PLC	± 0.2
3 PLC	± -
4 PLC	± -
ANGLES	± 3°

MATERIAL: SEE NOTE

FINISH: SEE NOTE

DWN	H. HUANG	30MAR2007
CHK	S. HOU	30MAR2007
APVD	W.J. KE	30MAR2007
PRODUCT SPEC	108-57080	
APPLICATION SPEC	—	
WEIGHT	—	

CUSTOMER DRAWING

TE Connectivity

NAME: 1.0 MM FPC, ZIF VERTICAL, SMT TYPE

SIZE	CAGE CODE	DRAWING NO	RESTRICTED TO
A3	00779	C-1734248	—

SCALE: — SHEET: 1 OF 2 REV: C2

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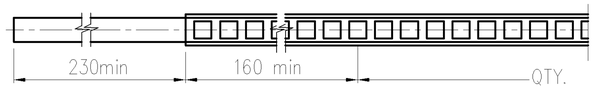
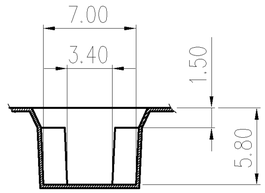
LOC	DIST
DW	–

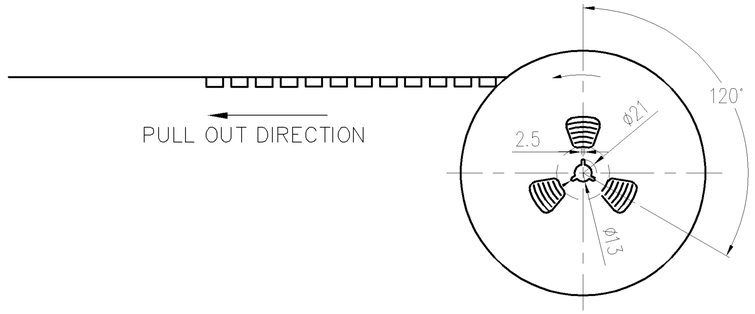
REVISIONS

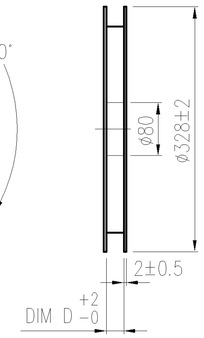
P	LTR	DESCRIPTION	DATE	DWN	APVD
		SEE SHEET 1.			



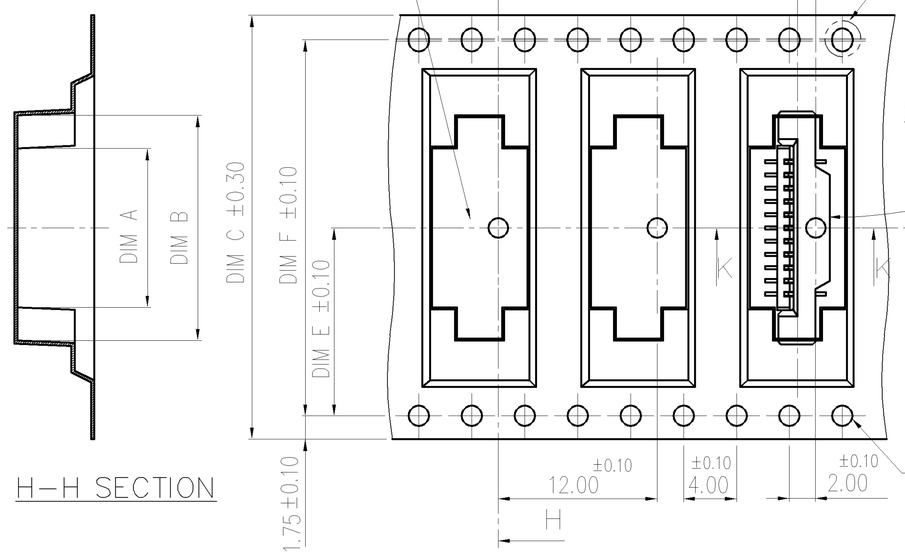


K–K SECTION

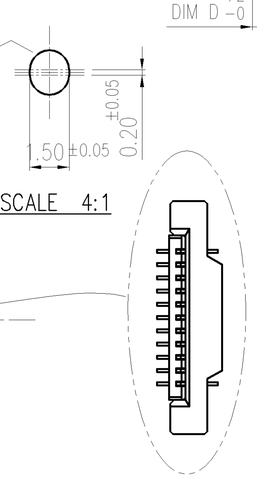




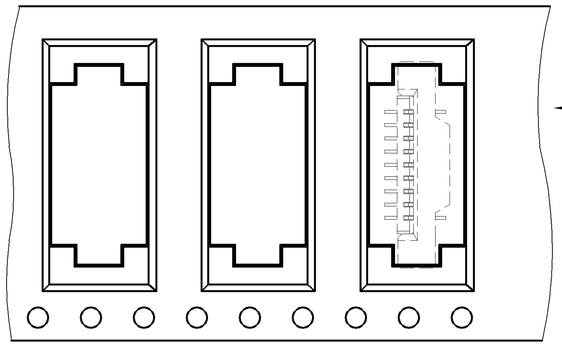
USER DIRECTION OF UNREELING



H–H SECTION



SCALE 4:1



USER DIRECTION OF UNREELING

FOR 3 TO 10 POS.

NOTES:
1. MATERIAL :
 1.1 EMBOSSED CARRIER: PS
 1.2 COVER TAPE: PS
 1.3 SHIPPING CARTON: CORRUGATED FIBER
2. DIMENSION :
 2.1 REEL: W=DIM C
 2.2 SHIPPING BOX: L=350, W=350, H=350
3. QUANTITY: PRIMARY PACKING: 1000 PCS/REEL
4. PEELING RESISTANCE: 10.2gf~71.4gf.
5. PEELING SPEED: 300mm/minutes.

REELS/ BOX	DIM F	DIM E	DIM D	DIM C	DIM B	DIM A	G/W (kg)	N/W (kg)	POS.	PART NUMBER
4	68.4	34.2	72.4	72	46	41	8.70	5.50	40	4–1734248–0
					~~45~~	~~40~~	~~8.57~~	~~5.37~~	~~39~~	~~3–1734248–9~~
					~~44~~	~~39~~	~~8.45~~	~~5.25~~	~~38~~	~~3–1734248–8~~
5	52.4	26.2	56.4	56	~~43~~	~~38~~	~~11.60~~	~~7.68~~	~~37~~	~~3–1734248–7~~
					~~42~~	~~37~~	~~11.40~~	~~7.48~~	~~36~~	~~3–1734248–6~~
					~~41~~	~~36~~	~~11.21~~	~~7.29~~	~~35~~	~~3–1734248–5~~
					~~40~~	~~35~~	~~11.02~~	~~7.10~~	~~34~~	~~3–1734248–4~~
					~~39~~	~~34~~	~~10.83~~	~~6.91~~	~~33~~	~~3–1734248–3~~
					~~38~~	~~33~~	~~10.63~~	~~6.71~~	~~32~~	~~3–1734248–2~~
					~~37~~	~~32~~	~~10.44~~	~~6.52~~	~~31~~	~~3–1734248–1~~
					36	31	10.25	6.33	30	3–1734248–0
					35	30	10.06	6.14	29	2–1734248–9
					34	29	9.86	5.94	28	2–1734248–8
					33	28	9.67	5.75	27	2–1734248–7
					32	27	9.00	5.56	26	2–1734248–6
6	40.4	20.2	44.4	44	31	26	8.80	5.36	25	2–1734248–5
					30	25	8.61	5.17	24	2–1734248–4
					~~29~~	~~24~~	~~8.42~~	~~4.98~~	~~23~~	~~2–1734248–3~~
					28	23	8.23	4.79	22	2–1734248–2
					27	22	8.03	4.59	21	2–1734248–1
					26	21	7.84	4.40	20	2–1734248–0
					25	20	7.65	4.21	19	1–1734248–9
					24	19	7.46	4.02	18	1–1734248–8
					23	18	7.26	3.82	17	1–1734248–7
					22	17	7.07	3.63	16	1–1734248–6
8	28.4	14.2	32.4	32	21	16	9.20	5.16	15	1–1734248–5
					20	15	8.91	4.87	14	1–1734248–4
					19	14	8.62	4.58	13	1–1734248–3
					18	13	8.33	4.29	12	1–1734248–2
					17	12	8.04	4.00	11	1–1734248–1
10	–	11.5	24.4	24	16	11	7.73	4.13	10	1–1734248–0
					15	10	7.41	3.81	9	1734248–9
					14	9	7.08	3.48	8	1734248–8
					13	8	6.76	3.16	7	1734248–7
					12	7	6.44	2.84	6	1734248–6
					11	6	6.12	2.52	5	1734248–5
					10	5	5.80	2.20	4	1734248–4
					9	4	5.48	1.88	3	1734248–3

THIS DRAWING IS A CONTROLLED DOCUMENT.

DIMENSIONS: mm

TOLERANCES UNLESS OTHERWISE SPECIFIED:

0 PLC	± –
1 PLC	± 0.3
2 PLC	± 0.2
3 PLC	± 0.15
4 PLC	± –
ANGLES	± 3°

MATERIAL –

FINISH –

DWN –
CHK –
APVD –
PRODUCT SPEC –
APPLICATION SPEC –
WEIGHT –

TE Connectivity

NAME 1.0 MM FPC, ZIF VERTICAL, SMT TYPE

SIZE	CAGE CODE	DRAWING NO	RESTRICTED TO
A3	00779	C–1734248	–

CUSTOMER DRAWING | SCALE – | SHEET 2 OF 2 | REV C2

MEAN WELL

350W Single Output Switching Power Supply

SE-350 series

■ Features :

- AC input range selectable by switch
- Protections: Short circuit / Overload / Over voltage/ Over temperature
- Forced air cooling by built-in DC fan
- Withstand 300vac surge input for 5 second
- Built-in cooling Fan ON-OFF control
- Built-in constant current limiting circuit
- 100% full load burn-in test
- LED indicator for power on
- Fixed switching frequency at 90KHz
- Low cost,high reliability
- 2 years warranty

SPECIFICATION

MODEL		SE-350-3.3	SE-350-5	SE-350-7.5	SE-350-12	SE-350-15	SE-350-24	SE-350-27	SE-350-36	SE-350-48
OUTPUT	DC VOLTAGE	3.3V	5V	7.5V	12V	15V	24V	27V	36V	48V
	RATED CURRENT	60A	60A	46A	29A	23.2A	14.6A	13A	9.7A	7.3A
	CURRENT RANGE	0 ~ 60A	0 ~ 60A	0 ~ 46A	0 ~ 29A	0 ~ 23.2A	0 ~ 14.6A	0 ~ 13A	0 ~ 9.7A	0 ~ 7.3A
	RATED POWER	198W	300W	345W	348W	348W	350.4W	351W	349.2W	350.4W
	RIPPLE & NOISE (max.) Note.2	150mVp-p	150mVp-p	150mVp-p	150mVp-p	150mVp-p	150mVp-p	200mVp-p	240mVp-p	240mVp-p
	VOLTAGE ADJ. RANGE	2.97 ~ 3.7V	4.5 ~ 5.6V	6 ~ 9V	10 ~ 13.5V	13.5 ~ 18V	20 ~ 26.4V	26 ~ 32V	32~40V	41 ~ 56V
	VOLTAGE TOLERANCE Note.3	+3%,-4.5%	±3.0%	±2.0%	±1.5%	±1.0%	±1.0%	±1.0%	±1.0%	±1.0%
	LINE REGULATION	±0.5%	±0.5%	±0.5%	±0.5%	±0.5%	±0.5%	±0.5%	±0.5%	±0.5%
	LOAD REGULATION	±2.5%	±2.0%	±2.0%	±1.0%	±0.5%	±0.5%	±0.5%	±0.5%	±0.5%
	SETUP, RISE TIME	1000ms, 50ms/230VAC 1000ms,50ms/115VAC at full load								
	HOLD UP TIME (Typ.)	20ms/230VAC 16ms/115VAC at full load								
INPUT	VOLTAGE RANGE Note.4	90 ~ 132VAC / 180 ~ 264VAC by switch 254 ~ 370VDC								
	FREQUENCY RANGE	47 ~ 63Hz								
	EFFICIENCY (Typ.)	74%	78%	80%	83%	84%	87%	88%	87.5%	87.5%
	AC CURRENT (Typ.)	7A/115VAC 4A/230VAC								
	INRUSH CURRENT (Typ.)	40A/115VAC 60A/230VAC								
	LEAKAGE CURRENT	<3.5mA / 240VAC								
PROTECTION	OVER LOAD	105 ~ 135% rated output power								
		Protection type : Constant current limiting, recovers automatically after fault condition is removed								
	OVER VOLTAGE	3.8 ~ 4.6V	5.75 ~ 7.5V	9.4 ~ 11.25V	13.8 ~ 16.2V	18 ~ 21V	27.6 ~ 32.4V	33.7 ~ 39.2V	41.4~46.8V	57.6 ~ 67.2V
		Protection type :Shut down O/P voltage, re-power on to recover								
	OVER TEMPERATURE	90℃±5℃(3.3~7.5V); 85℃±5℃(12~15V); 80℃±5℃(24V);75℃±5℃(27~48V) (TSW1) Detect on case								
		Protection type : Shut down O/P voltage, recovers automatically after temperature goes down								
FUNCTION	FAN ON/OFF CONTROL(Typ.)	RTH2≧50℃ FAN ON, ≦45℃ FAN OFF (3.3 ~ 7.5V)								
		RTH2≧55℃ FAN ON, ≦50℃ FAN OFF (12 ~ 48V)								
ENVIRONMENT	WORKING TEMP.	-20 ~ +60℃ (Refer to output load derating curve)								
	WORKING HUMIDITY	20 ~ 90% RH non-condensing								
	STORAGE TEMP., HUMIDITY	-20 ~ +85℃, 10 ~ 95% RH								
	TEMP. COEFFICIENT	±0.03%/℃ (0 ~ 50℃)								
	VIBRATION	10 ~ 500Hz, 5G 10min./1cycle, 60min. each along X, Y, Z axes								
SAFETY	SAFETY STANDARDS	UL60950-1 approved								
	WITHSTAND VOLTAGE	I/P-O/P:3KVAC I/P-FG:2KVAC O/P-FG:0.5KVAC								
	ISOLATION RESISTANCE	I/P-O/P, I/P-FG, O/P-FG:100M Ohms/500VDC / 25℃/ 70% RH								
OTHERS	MTBF	234.3K hrs min. MIL-HDBK-217F (25℃)								
	DIMENSION	215*115*50mm (L*W*H)								
	PACKING	1.07Kg; 12pcs/13.5Kg/0.92CUFT								
NOTE	1. All parameters NOT specially mentioned are measured at 230VAC input, rated load and 25℃ of ambient temperature. 2. Ripple & noise are measured at 20MHz of bandwidth by using a 12" twisted pair-wire terminated with a 0.1uf & 47uf parallel capacitor. 3. Tolerance : includes set up tolerance, line regulation and load regulation. 4. Please connect positive pole of input voltage with mark "N" of terminal block, connect negative pole of input voltage with mark "L" of terminal block, using DC voltage for input voltage.									

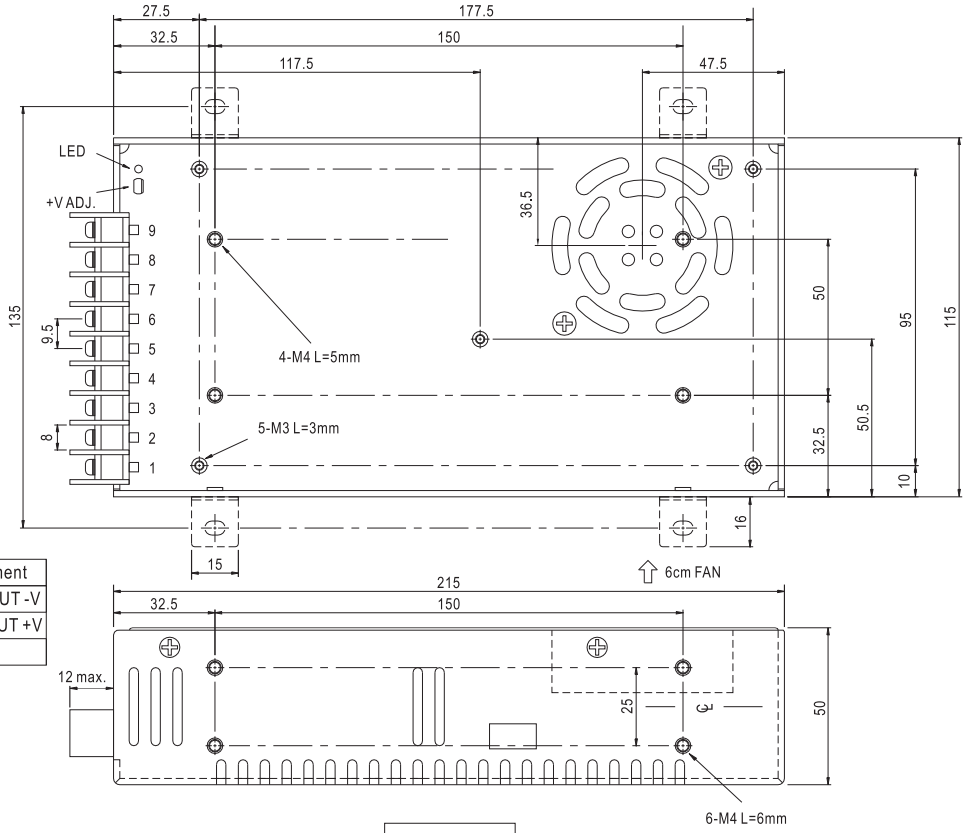
MEAN WELL

350W Single Output Switching Power Supply

SE-350 series

■ Mechanical Specification

Case No. 912C Unit:mm

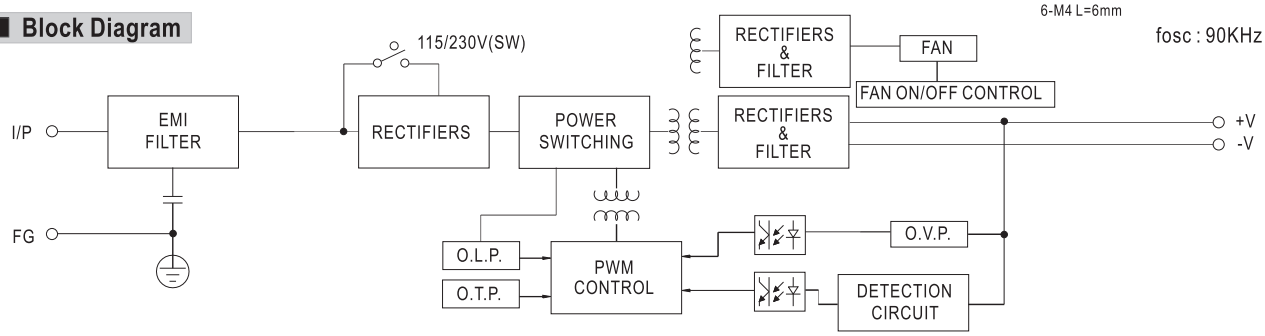


Terminal Pin No. assignment :

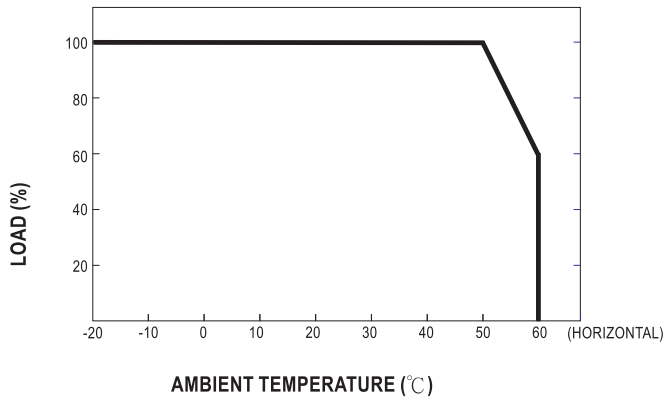
Pin No.	Assignment	Pin No.	Assignment
1	AC/L	4~6	DC OUTPUT -V
2	AC/N	7~9	DC OUTPUT +V
3	FG ⏚		

■ Block Diagram

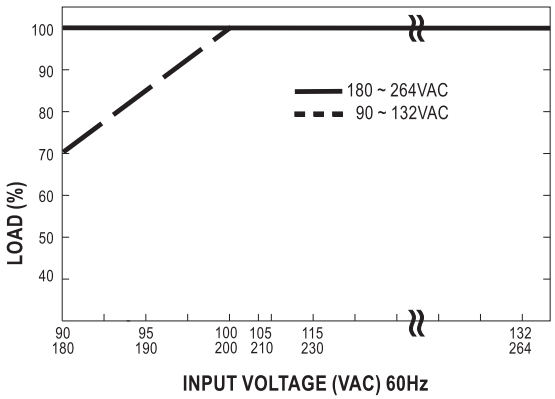
fosc : 90KHz



■ Derating Curve



■ Static Characteristics



G213V STEP MOTOR DRIVE

REV 7: March 25, 2011

GECKODRIVE, INC.
14662 FRANKLIN AVE
SUITE E
TUSTIN, CA 92780
(714) 832-8874

Thank you for purchasing the G213V drive. The G213V is part of Geckodrive's new generation of CPLD-based microstep drives. It has short-circuit protection for the motor outputs, over-voltage and under-voltage protection, over-temperature protection, reversed power supply polarity protection and will survive accidental motor disconnects while powered-up.

The G213V uses a synchronous PWM design that is absolutely silent when the motor is stopped or turning slowly. It virtually eliminates stopped-motor heating regardless of power supply voltage.

The STEP, DIRECTION and DISABLE inputs are opto-isolated. All three inputs work with 2.5V, 3.3V or 5V logic drive signals. The input drive current is now 2.5mA at 2.5V so almost all logic family (74LS, 74HC, etc.) can be used to drive these inputs. The COMMON return for the signals is controller ground referenced instead of +5VDC. This greatly eases the drive to controller interface.

There are no unusual STEP to DIRECTION timing restrictions. Stepping occurs on the positive edge of the STEP pulse. The DIRECTION input must be true 200nS before and after this STEP pulse edge.

The G213V microstep drive is warranted to be free of manufacturing defects for 1 year from the date of purchase. Anyone who is dissatisfied with it or is unable to make it work to their satisfaction for any reason will be cheerfully refunded the purchase price if the G213V is returned within 15 days of the purchase date in a cosmetically and electrically undamaged condition.

PLEASE READ FIRST BEFORE USING THE G213V

Before you start you must have a 2-phase hybrid PM step motor (ordinary 1.8 or 0.9 degree per step motor), a DC power supply suitable for the motor and a current set resistor. The motor's rated phase current must not be more than 7 Amps. The power supply voltage must be between 15VDC and 80VDC unregulated. The current set resistor may be a 1/4-Watt, 5% part. Finally have a STEP, DIRECTION and DISABLE (if needed) source available.

G213V TERMINAL WIRING

The G213V uses a 2-piece modular main connector. The connector is split in two pieces; terminals 1 through 6 (power supply and motor leads) and terminals 7 through 12 (control interface). Each can be removed separately by pulling the connector body upwards and off of the mating header pins on the G213V. The connectors must initially be removed to mount the G213V to a heatsink or chassis.

TERMINAL 1 Power Ground
Connect the negative (black) lead of your power supply to this terminal.

TERMINAL 2 Power (+)
Connect the positive (red) lead of your power supply to this terminal. It must be between +18VDC to +80VDC.

TERMINAL 3 Motor Phase A
Connect one end of your "Phase A" motor winding here.

TERMINAL 4 Motor Phase /A
Connect the other end of your "Phase A" motor winding here.

TERMINAL 5 Motor Phase B
Connect one end of your "Phase B" motor winding here.

TERMINAL 6 Motor Phase /B
Connect the other end of your "Phase B" motor winding here.

TERMINAL 7 Disable
This terminal will force the winding currents to zero when tied to the step and direction controller +5V.

TERMINAL 8 Direction
Connect the DIRECTION signal to this terminal.

TERMINAL 9 Step
Connect the STEP signal to this terminal.

TERMINAL 10 Common

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Connect the controller's GROUND to this terminal.

TERMINAL 11 Current Set
Connect one end of your current set resistor to this terminal.

TERMINAL 12 Current Set
Connect the other end of your current set resistor to this terminal.

POWER SUPPLY WIRING

TERMINAL 1 Power Ground
Connect the power supply ground to term.1

TERMINAL 2 Power (+)
Connect the power supply "+" to this terminal

The power supply voltage must be between 15 VDC and 80 VDC. The maximum power supply current required is equal to the motor's rated phase current. An unregulated power supply may be used so long as the voltage stays between the specified limits; keep the power supply ripple voltage to 10% or less for best results.

CAUTION! Power supply voltage in excess of 80 VDC **will** blow the G213V internal fuse.

CAUTION! Reversed power supply polarity will blow the G213V internal fuse.

CAUTION! Never put a switch on the DC side of the power supply! This will damage, if not destroy, your drive!

The choice of power supply voltage depends on the required high-speed performance from the motor; doubling the voltage doubles the motor's high-speed power. In all cases the power supply voltage should be no less than 4 times or no more than 20 times the motor's rated voltage. The motor may not run as smoothly as possible if the power supply voltage is less than 4 times or more than 20 times the motor's rated voltage. A power supply voltage greater than 20 times the motor's rated voltage may overheat and damage the motor. Motor winding inductance should be 500uH or greater.

A more accurate calculation of power supply voltage is to find your motor's inductance, and put it into the following equation.

$$32 * (\sqrt{\text{mH inductance}}) = \text{Power Supply Voltage}$$

If your motor has 2mH of inductance, the equation would look as follows.

$$32 * (\sqrt{2}) = 45.12\text{V}$$

MOTOR CONNECTION

TERMINAL 3 Phase A
Connect one motor winding to this terminal

TERMINAL 4 Phase /A
Connect the other end of the winding to this terminal

TERMINAL 5 Phase B
Connect the other motor winding to this terminal

TERMINAL 6 Phase /B
Connect the other end of the winding to this terminal

One motor winding connects to terminals 3 and 4 and the other winding connects to terminals 5 and 6. Turn the power supply off when connecting or disconnecting the motor. If the motor turns in the wrong direction, reverse the motor winding connections to terminals 3 and 4.

CAUTION! Avoid shorting the motor leads to each other or to ground or the G213V will enter protective shut-down.

4-wire, 6-wire and 8-wire motor may be used. If 6-wire motors are used, they may be connected in half winding or full winding. This is equivalent to an 8-wire motor connected in parallel or series. If a motor is connected in series or full winding, the motor's

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phase current rating is half of its parallel or unipolar rating. The choice depends on the high-speed performance required; a parallel-connected motor will provide twice the power of a series-connected motor at the same power supply voltage.

DISABLE PIN

TERMINAL 7 Disable
This terminal will force the winding currents to zero when tied to the step and direction controller +5V.

The DISABLE input on the G213V is optically isolated and requires logic "1" to DISABLE and logic "0" to ENABLE the drive. Once it is disabled, the motor windings are unergenized and the motor freewheels.

STEP AND DIRECTION INPUTS

TERMINAL 8 Direction
Connect the DIRECTION line to this terminal.

TERMINAL 9 Step
Connect the STEP line to this terminal.

TERMINAL 10 Common
Connect this terminal to the controller GROUND

These 3 inputs are optically isolated from the rest of the drive. They will operate with 2.5V, 3.3V or 5V logic outputs with 2.5mA minimum source drive current. The STEP input's maximum rated frequency is 350kHz with a 50% duty-cycle waveform. The G213V steps the motor on the 0 to 1 logic (positive) edge of the STEP signal.

TERMINAL 11 Current Set
Connect the current set resistor to this terminal

TERMINAL 12 Current Set
Connect the other end of the current set resistor to this terminal

This input matches the G213V's current output to the motor windings. The G213V will accommodate motor winding currents from 0 to 7A. Use the following equation to calculate the value, (in kilo-Ohms) of the current set resistor:
R (in kilo-ohms) = 47 * I / (7 – I) Use the nearest standard value 5% tolerance, 1/4W resistor for this setting.

Here are the current set resistor values for motor current in .5A increments. Round the appropriate answer to the nearest 5% resistor value.

a. 1A – 7.8K
b. 1.5A – 12.8K
c. 2A – 18.8K
d. 2.5A – 26.1K
e. 3A – 35.25K
f. 3.5A – 47K
g. 4A – 62.67K
h. 4.5A – 84.6K
i. 5A – 117.5K
j. 5.5A – 172.33K
k. 6A – 282K
l. 6.5A – 611K
m. 7A – OPEN

OTHER CONSIDERATIONS:

HEATSINKING: The G213V needs heatsinking for current settings greater than 3 amps. The case temperature (measured on the bottom plate) should not exceed 70 degrees C, and for best life should be kept at 50C degrees or less. Use heatsink compound between the G213V and your heatsink.

CAUTION! Current settings above 3A without a heatsink may result in the G213V entering thermal shutdown.

AUTO CURRENT REDUCTION: The G213V reduces motor phase current to 71% of the set current value 1 second after the last step pulse is sent. The G213V also changes to a special recirculating current mode to nearly eliminate motor heating.

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ADJUST: This trimpot adjusts the motor for the smoothest possible low-speed operation. Set the motor speed to about 1/2 revolution per second and then turn the trimpot until a distinct null is noted in the motor's vibration. This will result in the most even microstep placement for a given motor and power supply voltage. The default setting for this trimpot is at ½ -turn and the setting for your motor will be within +/- ¼-turn of the default setting.

G213V INDICATORS:

POWER LED: The **GREEN** POWER indicator is lit whenever the G213V has power supply voltage applied.

FULL POWER LED: The **YELLOW** FULL POWER indicator is lit when the motor is turning fast enough to generate maximum possible mechanical power. Power is torque times RPM and power output reaches its maximum value when this indicator is lit. Use this indicator to verify your motor is optimally geared to the load.

ERROR LED: The **RED** ERROR indicator is lit when:

1) During power-on reset for 1 second when power is first applied to the G213V.
2) While the DISABLE input is active.
3) When there is a short-circuit on any motor output. Momentarily activate the DISABLE input to reset.
4) During over-temperature shutdown. The LED automatically resets when the drive temperature drops.

INTERNAL FUSE: The G213V uses a socketed, user-replaceable internally mounted fuse (Littlefuse Inc. part # 0251005.MXL). Reversing the power supply polarity or a power supply voltage over 114VDC will cause the internal fuse to blow.

CAUTION! Do not use any other type of fuse, do not bridge a blown fuse with wire and do not solder the fuse in place. Doing so will void the drive's warranty.

REMOVING AND REPLACING THE COVER:

REMOVING THE COVER:

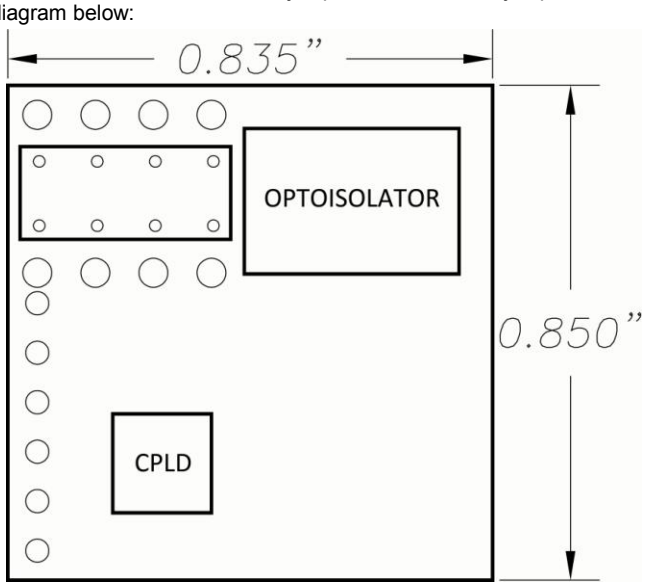
1) Remove the two 2-56 phillips-head screws on the bottom of the drive.
2) Slide the cover backwards until it clears the drive.

REPLACING THE COVER:

1) Slide the cover forward over the drive while lifting the back of the cover.
2) Replace the screws on the bottom of the drive.

ADJUSTING MICROSTEP RESOLUTION

The G213V has an onboard step pulse multiplier called the G901X that allows the drive to operate in full step, half step, 5 microstep and 10 microstep modes. The G901X uses a 2mm jumper block and two jumpers to set the resolution. The jumper block can be found by using the diagram below:



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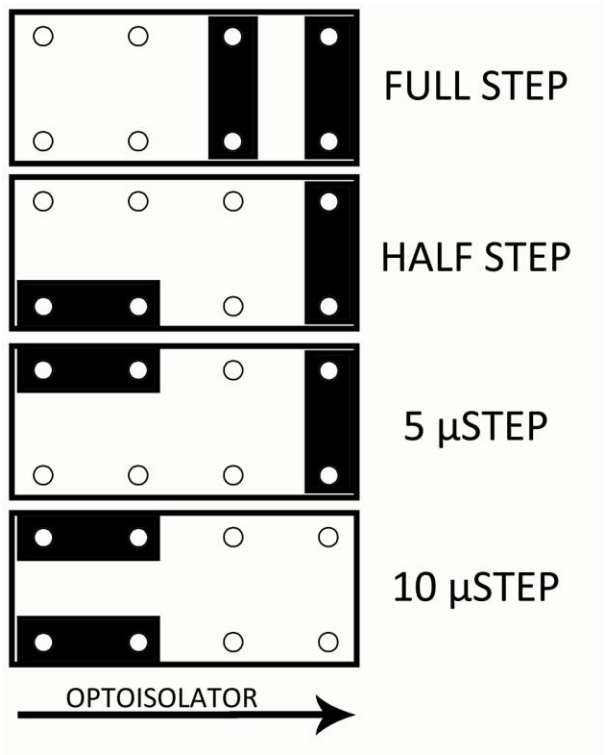
Once the jumpers have been located they may be set according to the diagram below. Please note that the four pins closest to the optoisolator are unconnected and can be used as jumper storage. It is recommended that needle nose pliers or tweezers be used to adjust the jumper settings. The power to the G213V must be turned off before any adjustment is to be made on the step pulse multiplier.



METHOD OF OPERATION FOR STEP PULSE MULTIPLIER:

The G901X step pulse multiplier still allows all of the benefits of microstepping at low speeds and full stepping at high speeds that the G203V has. The step pulse multiplier works by outputting a set number of pulses to the main motor control board it is attached to, which is the G203V in the case of the G213V.

If the step pulse multiplier is set to full stepping mode it will output ten microsteps for every pulse it receives on its input; as far as the base drive is concerned, it is always microstepping at its normal rate. This means that the drive will continue to morph to full step at higher speeds to allow the highest possible torque from the motor.

TROUBLESHOOTING:

EVERYTHING IS CONNECTED, NOTHING HAPPENS: Is the **GREEN** LED lit? If not, either the G213V has no power supply voltage connected or something very bad caused its internal fuse to blow. Check the power supply voltage using a multimeter set to 'DC VOLTS' on terminal screw heads 1,2 of the drive.

The internal fuse is the G213V's final line of protection. It blows only under the most extreme circumstances. Those are reversed power supply polarity; AC voltage instead of DC voltage on terminals 1 and 2 and power supply voltages in excess of 114VDC. Correct the problem and replace the fuse with the only approved type. It is the only kind that blows fast enough to protect the G213V. Anything else voids the warranty.

EVERYTHING IS CONNECTED, RED INDICATOR STAYS LIT: If the **RED** and **GREEN** indicator LEDs are lit then the motor is miswired, the motor has a wire shorted to ground, is shorted to another motor wire or the motor is bad. Secondarily: Everything ran OK but the **RED** LED lit a while later. Check the drive temperature; it may have overheated because of inadequate heatsinking. Also see that the DISABLE input isn't being activated (+5VDC on DISABLE).

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MOTOR HAS NO HOLDING TORQUE: If the **RED** LED is off and the **GREEN** LED is on, check the CURRENT SET resistor with a multimeter. Re-calculate the resistor value. Check to see if the motor is connected to the G213V.

MOTOR HAS HOLDING TORQUE BUT WON'T MOVE: Check your STEP, DIRECTION, DISABLE (if used) and COMMON interface. Verify COMMON goes to your controller GND.

MY MOTOR RUNS ROUGH AT LOW SPEEDs: Try adjusting the ADJUST trimpot setting. Verify you are using the correct CURRENT SET resistor. A round stepper motor will not operate as well as a square stepper motor as they were not designed for microstepping.

MY YELLOW LED NEVER LIGHTS: You are not going fast enough to get full power from your motor. If you don't need to go any faster, use a lower power supply voltage. This indicator is a good application diagnostic for motor gearing and power supply voltage choice. Using it correctly will help you to optimize your system.

DISCLAIMER

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G213V STEP MOTOR DRIVE

REV 7: March 25, 2011

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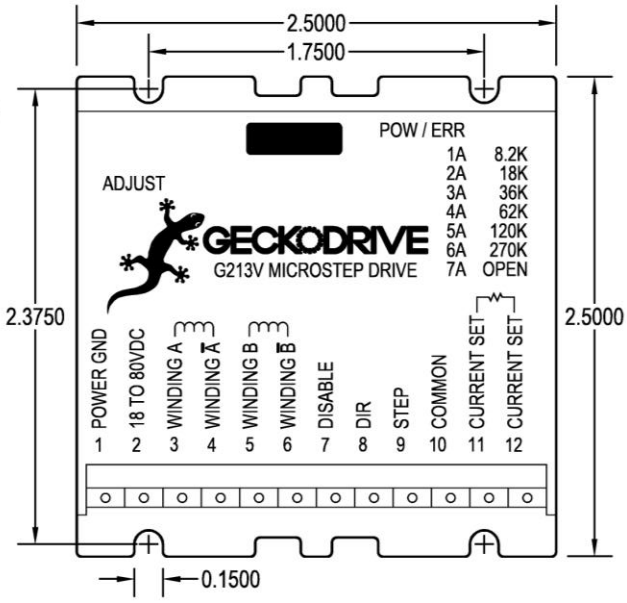
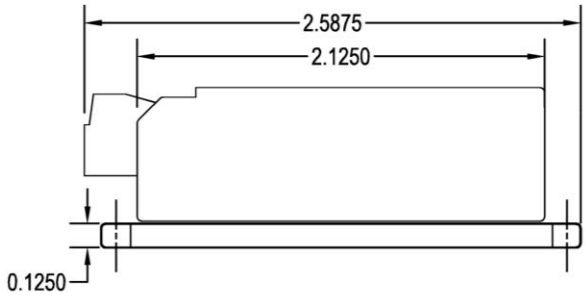
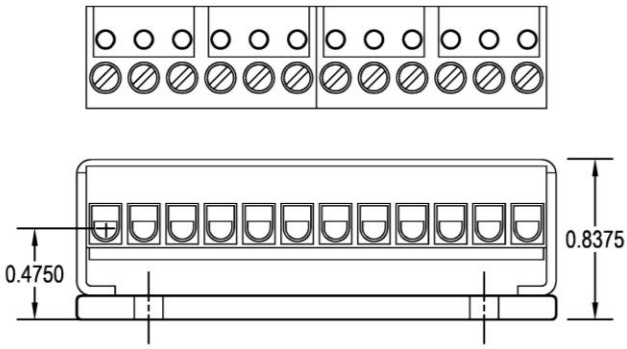
G213V Microstep Drive

Cover:	Aluminum, Anodised
Connector:	Modular, 5 mm pitch
Plate:	Aluminum, Hard Anodised
Color:	Red Anodised, White Text
Weight:	3.7 oz, (104 gm)
Size:	2.5" by 2.5" by 0.8375"
	63.5 mm, 63.5 mm, 21.3 mm



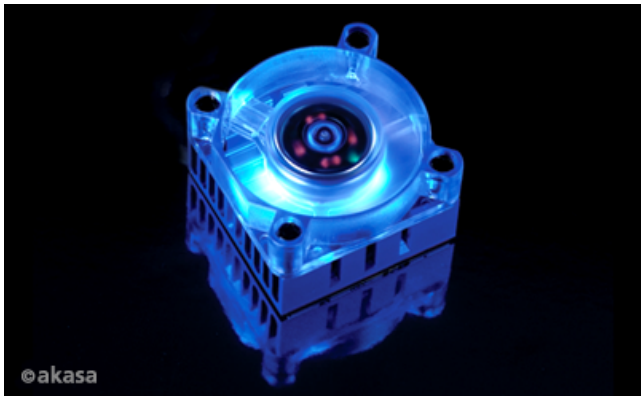




SPECIFICATIONS:

Supply Voltage:	15 to 80 VDC
Phase Current:	0 to 7 Amps
Auto Current Reduction:	71% of set current, 1 second after last Step Pulse
Size:	2.5"W, 2.5"D, .85"H (63.5mm, 63.5mm, 21.5mm)
Mounting Pattern:	4 6-32 screws, 1.75" by 2.375" (44.5 mm, 60 mm)
Weight:	3.6 oz. (100 gm)
Quiescent Current:	20 Ma or less (drive disabled)
Short-circuit trip current:	10A, 3uS response time
Step Frequency:	0 to 333 kHz
Step Pulse "0" Time:	2uS min (Step on rising edge)
Temp:	0 to 70 C
Step Pulse "1" Time:	1 uS min
Humidity:	0 to 95 % (non-condensing)
Direction Setup:	200nS before step pulse rising edge
	200nS hold after step pulse rising edge
Power Dissipation:	1 to 13 W (0 to 7 Amps)

akasa
SUPERB DESIGN ENGINEERING



Chipset Cooler

Keep your chipset cool in style

Product Code: AK-210

Application	Chipset cooler
Cooler dimension	40 x 40 x 24 (H) mm
Heatsink material	Blue anodized aluminium
Weight	38g
Installation	Thermally conductive adhesive tape (pre-applied)
Fan diamension	40 x 40 x 10mm
Fan Speed	5000 RPM
Fan airflow	5.20 CFM (8.18 m^3/h)
Fan air pressure	2.23 mm H20
Noise level	20.0 dB(A)
Current rating	0.10 A
Voltage rating	12V DC
Bearing type	Sleeve bearing
Fan life expectancy	30,000 hours
Fan connector	3pin
Product code	AK-210

NOTE: Before installing the cooler, ensure the surface of the chipset is perfectly clean. If any residue of old thermal compound is present, clean it with Isopropyl or Akasa TIM clean.

get in touch!
contact a specialist
Contact Us
Talk to us for your thermal solution and modding advice

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ARCTIC MX-2

Award-Winning High Performance Thermal Compound

Main Features

- High thermal conductivity
- Low thermal resistance
- Electrically non-conductive
- Non-capacitive
- Non-curing
- Non-corrosive
- Non-bleeding

8 Year durability

www.arctic.ac

ARCTIC MX-2 [270]

Award-Winning High Performance Thermal Compound

Non-Metallic Thermal Paste

The **ARCTIC MX-2** outperforms other metallic thermal pastes in the market. Its metal-free, non-electrical conductive design eliminates any risks of causing short circuit, adding more protection to the CPU and VGA cards.

High Performance

Due to its high thermal conductivity and low thermal resistance, the **ARCTIC MX-2** guarantees efficient thermal dissipation from the components. With excellent temperature reduction performance, the **ARCTIC MX-2** is ideal for CPU and GPU cooling, and other applications between power semiconductor components and heatsinks. It is also one of the easy ways to improve the overclockability

4g

8g

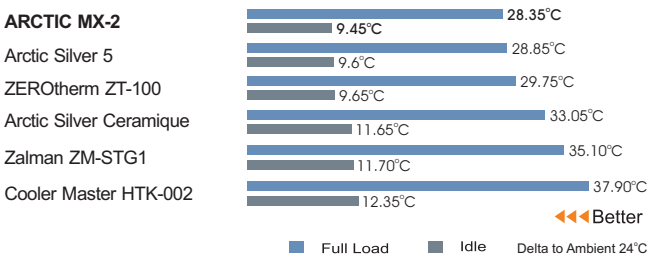
30g

65g

Application

CPU, GPU, power semiconductor components

Specifications:	
Viscosity:	850 poise
Density:	3.96 g/cm^3
Net weight:	4 g / 8 g / 30 g / 65 g



Tested Intel Qx6850 Core 2 Extreme at 3.00GHz
Data source: HardwareLogic.com
CPU Cooler: Zalman Reserator XT

DARKHARDWARE

"It is exciting to see a non-metallic paste showing better performance than metal based ones."
– DarkHardware.com

hardwaretech
www.hwtech.ru

"This paste can produce excellent results in the case for the video, and the processor. ARCTIC MX-2 is an excellent choice for enthusiasts."
– HardwareTech

ARCTIC

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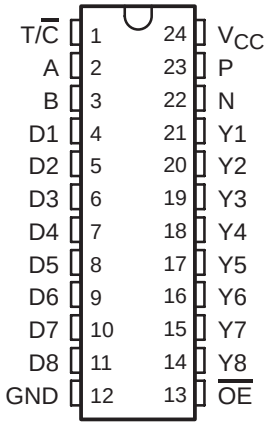
SN74LV8151
10-BIT UNIVERSAL SCHMITT-TRIGGER BUFFER WITH 3-STATE OUTPUTS

SCES610 − OCTOBER 2004

- **2-V to 5.5-V V_{CC} Operation**
- **Max t_{pd} of 15 ns at 5 V**
- **Schmitt-Trigger Inputs Allow for Slow Input Rise/Fall Time**
- **Polarity Control for Y Outputs Selects True or Complementary Logic**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Supports Mixed-Mode Voltage Operation on All Ports**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

NT OR PW PACKAGE (TOP VIEW)



description/ordering information

The SN74LV8151 is a 10-bit universal Schmitt-trigger buffer with 3-state outputs, designed for 2-V to 5.5-V V_{CC} operation. The logic control (T/$\overline{C}$) pin allows the user to configure Y1 to Y8 as noninverting or inverting outputs. When T/$\overline{C}$ is high, the Y outputs are noninverted (true logic), and when T/$\overline{C}$ is low, the Y outputs are inverted (complementary logic).

When output-enable ($\overline{OE}$) input is low, the device passes data from Dn to Yn. When $\overline{OE}$ is high, the Y outputs are in the high-impedance state. The path A to P is a simple Schmitt-trigger buffer, and the path B to N is a simple Schmitt-trigger inverter.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP − NT	Tube	SN74LV8151NT	SN74LV8151NT
	TSSOP − PW	Tube	SN74LV8151PW	LV8151
		Tape and reel	SN74LV8151PWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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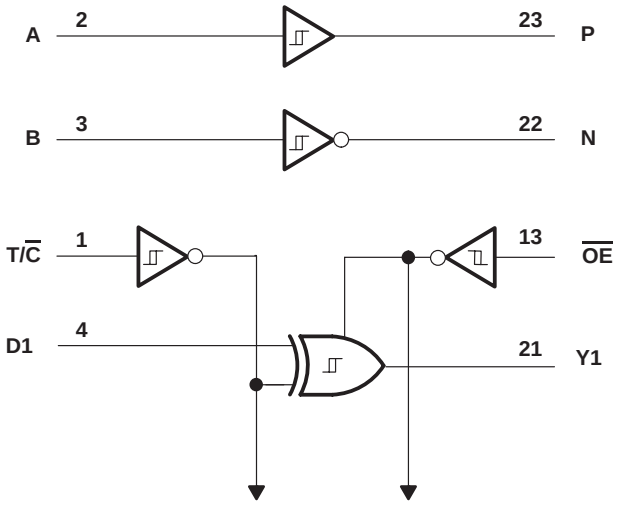
FUNCTION TABLES

INPUT A	OUTPUT P
L	L
H	H

INPUT B	OUTPUT N
L	H
H	L

INPUTS			OUTPUT Y
$\overline{OE}$	$T/\overline{C}$	D	
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	H
H	X	X	Z

logic diagram



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	−0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0)	−20 mA
Output clamp current, I_{OK} (V_O < 0)	−50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3): NT package	67°C/W
(see Note 4): PW package	88°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-3.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 5)

			V_{CC}	MIN	MAX	UNIT
V_{CC}	Supply voltage			2	5.5	V
V_{IH}	High-level input voltage		2 V	1.5		V
			2.3 V to 2.7 V	$V_{CC} \times 0.7$		
			3 V to 3.6 V	$V_{CC} \times 0.7$		
			4.5 V to 5.5 V	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage		2 V		0.5	V
			2.3 V to 2.7 V		$V_{CC} \times 0.3$	
			3 V to 3.6 V		$V_{CC} \times 0.3$	
			4.5 V to 5.5 V		$V_{CC} \times 0.3$	
V_I	Input voltage			0	5.5	V
V_O	Output voltage	High or low state		0	V_{CC}	V
		3-state		0	5.5	
I_{OH}	High-level output current		2 V		−50	µA
			2.3 V to 2.7 V		−2	mA
			3 V to 3.6 V		−6	
			4.5 V to 5.5 V		−12	
I_{OL}	Low-level output current		2 V		50	µA
			2.3 V to 2.7 V		2	mA
			3 V to 3.6 V		6	
			4.5 V to 5.5 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	T/$\overline{C}$, $\overline{OE}$ inputs	2.3 V to 2.7 V		200	ns/V
			3 V to 3.6 V		100	
			4.5 V to 5.5 V		20	
		A, B, D inputs	2.3 V to 2.7 V		4	ms/V
			3 V to 3.6 V		3	
			4.5 V to 5.5 V		2	
T_A	Operating free-air temperature			−40	85	°C

NOTES: 5. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{T+} Positive-going input threshold voltage	A, B, and D inputs	2.5 V			1.75	V
		3.3 V			2.31	
		5 V			3.5	
V_{T-} Negative-going input threshold voltage	A, B, and D inputs	2.5 V	0.75			V
		3.3 V	0.99			
		5 V	1.5			
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	A, B, and D inputs	2.5 V	0.25		1	V
		3.3 V	0.33		1.32	
		5 V	0.5		2	
V_{OH}	I_{OH} = −50 µA	2 V to 5.5 V	V_{CC} − 0.1			V
	I_{OH} = −2 mA	2.3 V	2			
	I_{OH} = −6 mA	3 V	2.48			
	I_{OH} = −12 mA	4.5 V	3.8			
V_{OL}	I_{OL} = 50 µA	2 V to 5.5 V			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4	
	I_{OL} = 6 mA	3 V			0.44	
	I_{OL} = 12 mA	4.5 V			0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1	µA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±5	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			20	µA
I_{off}	V_I or V_O = 0 to 5.5 V	0			5	µA
C_i	$V_I = V_{CC}$ or GND	3.3 V		3		pF
		5 V		3		
C_o	$V_O = V_{CC}$ or GND	3.3 V		5		pF
		5 V		5		

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C TYP	MIN	MAX	UNIT
t_{pd}	A or B	P or N	C_L = 15 pF	22	1	45	ns
	D	Y		23	1	49	
	T/$\overline{C}$			24	1	50	
t_{en}	$\overline{OE}$	Y		12	1	25	ns
t_{dis}	$\overline{OE}$	Y		11	1	20	ns
t_{pd}	A or B	P or N	C_L = 50 pF	26	1	52	ns
	D	Y		28	1	57	
	T/$\overline{C}$			29	1	58	
t_{en}	$\overline{OE}$	Y		15	1	30	ns
t_{dis}	$\overline{OE}$	Y		15	1	26	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C TYP	MIN	MAX	UNIT
t_{pd}	A or B	P or N	C_L = 15 pF	14	1	26	ns
	D	Y		15	1	29	
	T/$\overline{C}$			16	1	30	
t_{en}	$\overline{OE}$	Y		9	1	16	ns
t_{dis}	$\overline{OE}$	Y		8	1	14	ns
t_{pd}	A or B	P or N	C_L = 50 pF	17	1	32	ns
	D	Y		18	1	34	
	T/$\overline{C}$			20	1	36	
t_{en}	$\overline{OE}$	Y		11	1	20	ns
t_{dis}	$\overline{OE}$	Y		11	1	18	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C TYP	MIN	MAX	UNIT
t_{pd}	A or B	P or N	C_L = 15 pF	9	1	15	ns
	D	Y		10	1	16	
	T/$\overline{C}$			11	1	17	
t_{en}	$\overline{OE}$	Y		6	1	10.5	ns
t_{dis}	$\overline{OE}$	Y		6	1	10	ns
t_{pd}	A or B	P or N	C_L = 50 pF	11	1	18	ns
	D	Y		12	1	20	
	T/$\overline{C}$			13	1	21	
t_{en}	$\overline{OE}$	Y		8	1	12.5	ns
t_{dis}	$\overline{OE}$	Y		8	1	11.5	ns

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF (see Note 6)

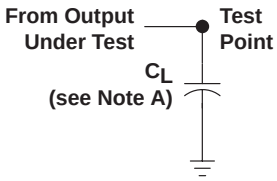
PARAMETER		T_A = 25°C MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.6		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 6: Characteristics are for surface-mount packages only.

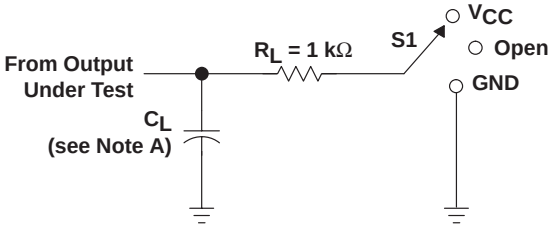
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = No load, f = 1 MHz	3.3 V	15	pF
			5 V	16	

PARAMETER MEASUREMENT INFORMATION

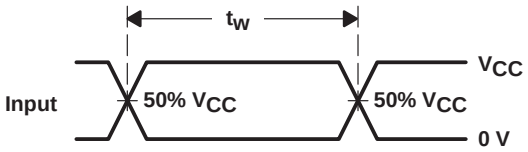


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

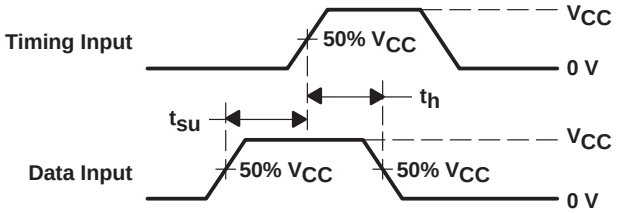


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

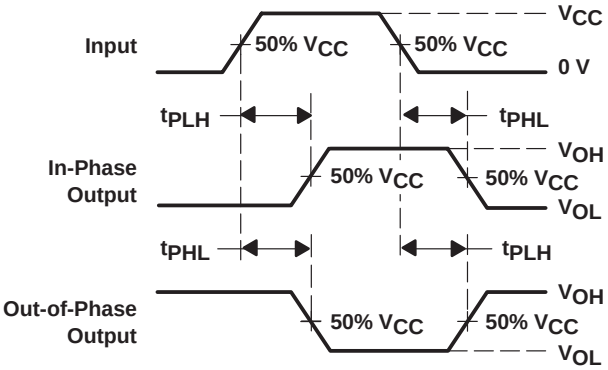
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



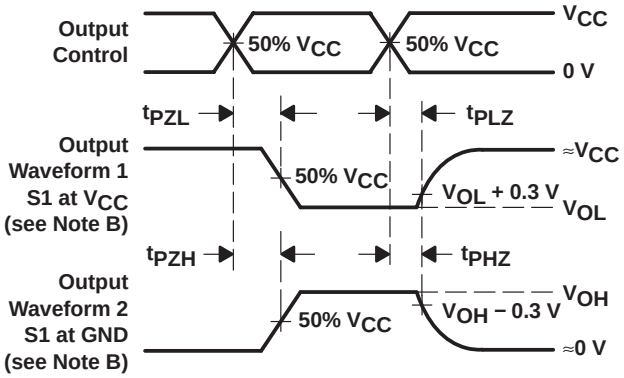
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74LV8151DGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8151	Samples
SN74LV8151DGVRE4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8151	Samples
SN74LV8151DGVRG4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8151	Samples
SN74LV8151DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8151	Samples
SN74LV8151DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8151	Samples
SN74LV8151DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8151	Samples
SN74LV8151DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8151	Samples
SN74LV8151DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8151	Samples
SN74LV8151DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8151	Samples
SN74LV8151NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV8151NT	Samples
SN74LV8151NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV8151NT	Samples
SN74LV8151PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8151	Samples
SN74LV8151PWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8151	Samples
SN74LV8151PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8151	Samples
SN74LV8151PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8151	Samples
SN74LV8151PWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8151	Samples
SN74LV8151PWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8151	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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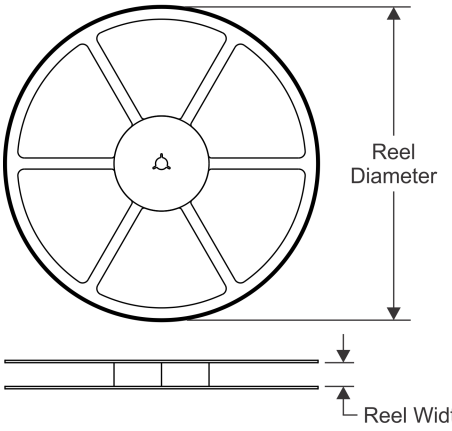
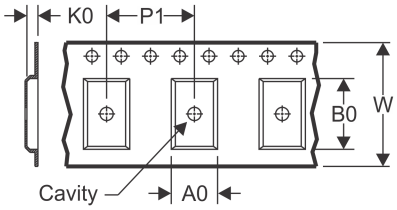
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

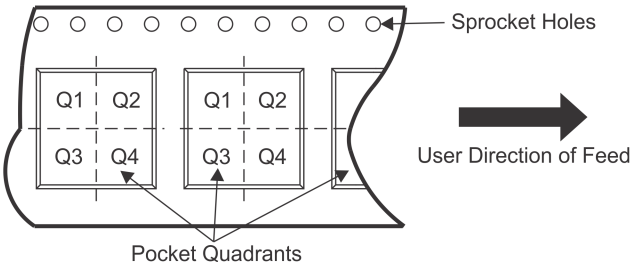


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

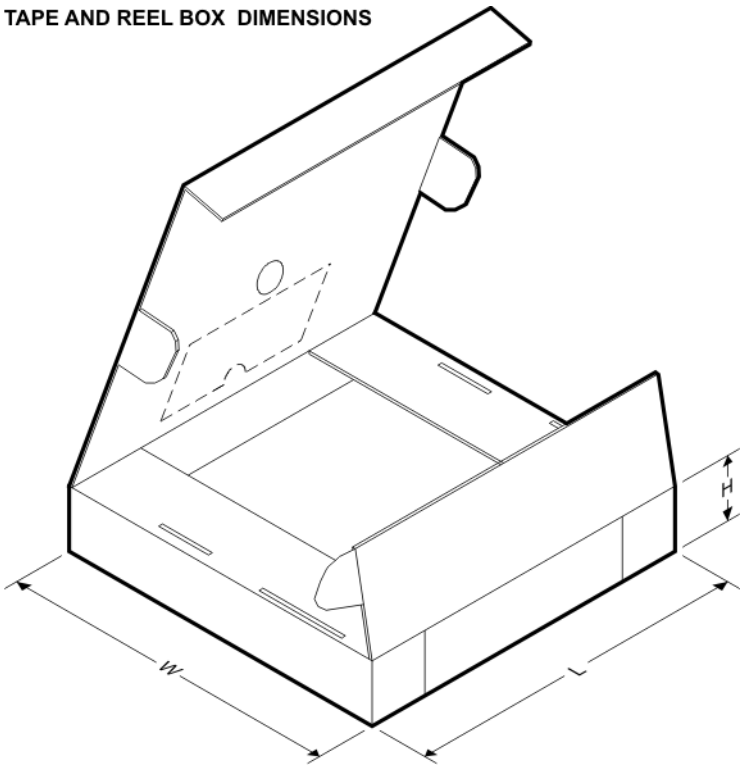
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV8151DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV8151DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

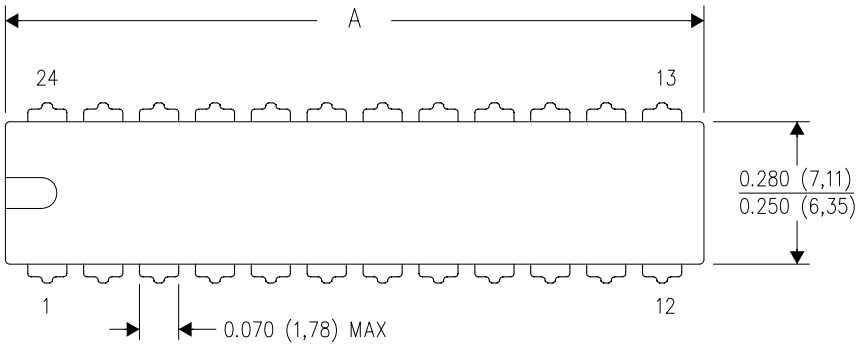


*All dimensions are nominal

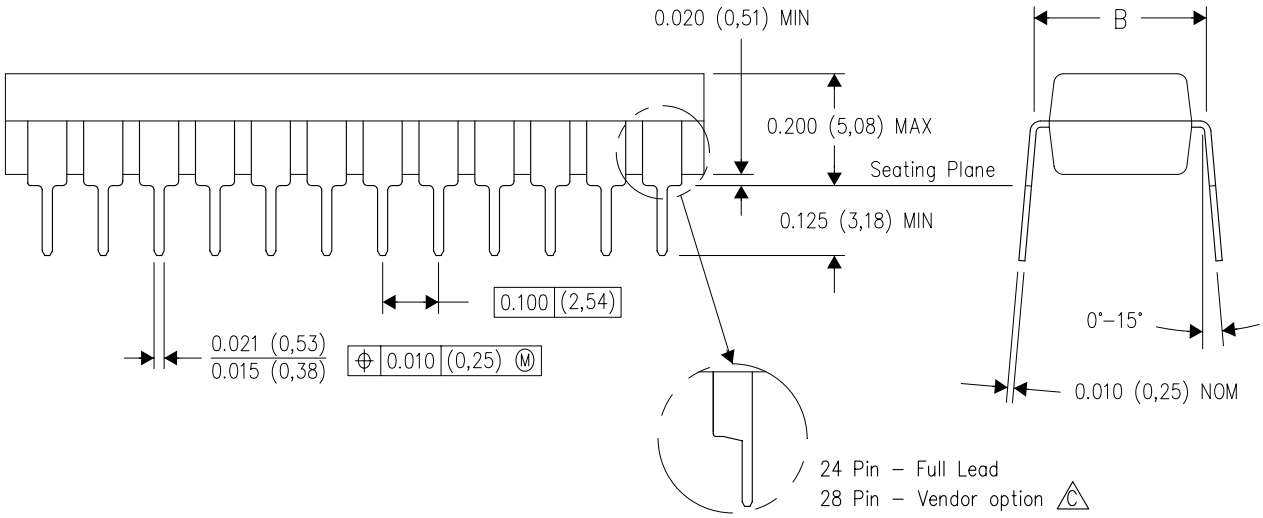
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV8151DGVR	TVSOP	DGV	24	2000	367.0	367.0	35.0
SN74LV8151DWR	SOIC	DW	24	2000	367.0	367.0	45.0

NT (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

24 PINS SHOWN



DIM \ PINS **	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)



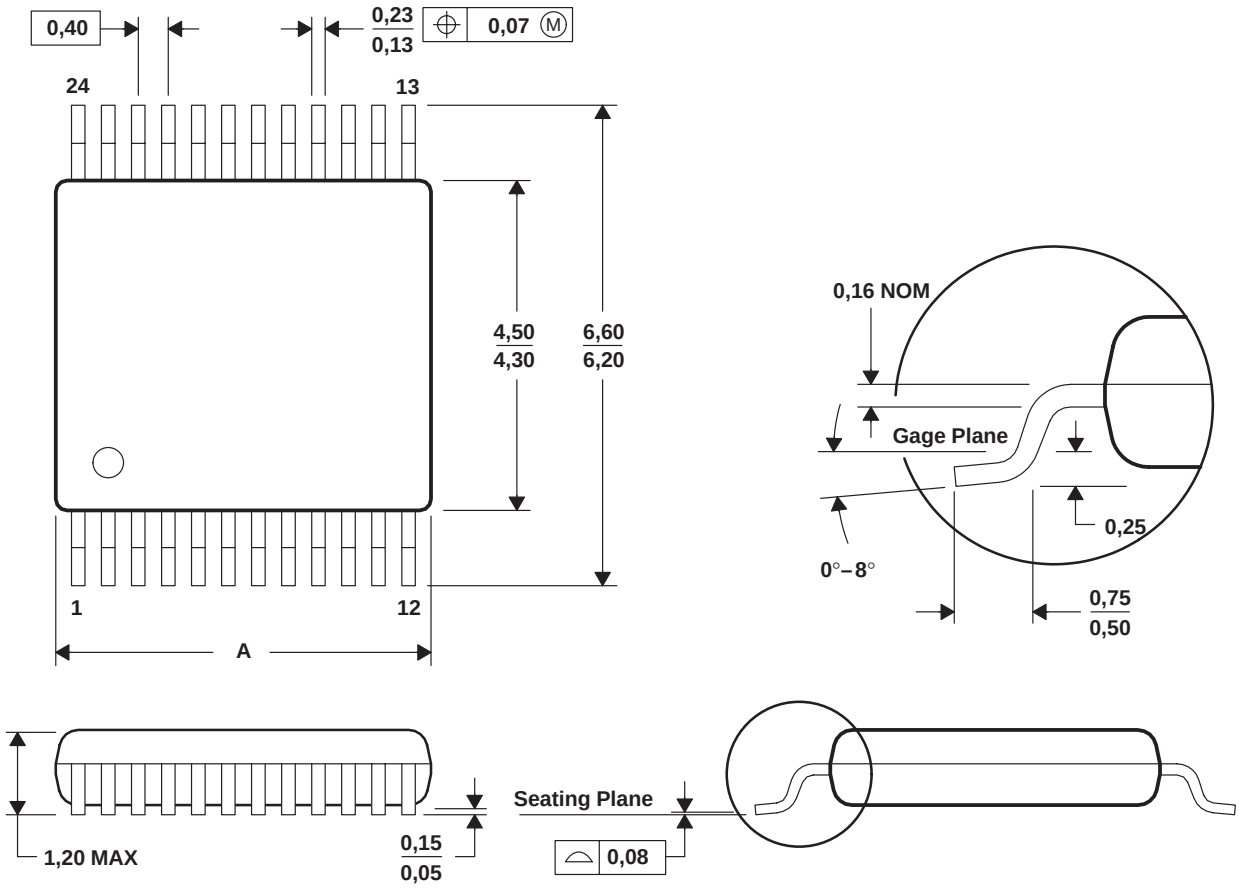
4040050/C 04/09

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The 28 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

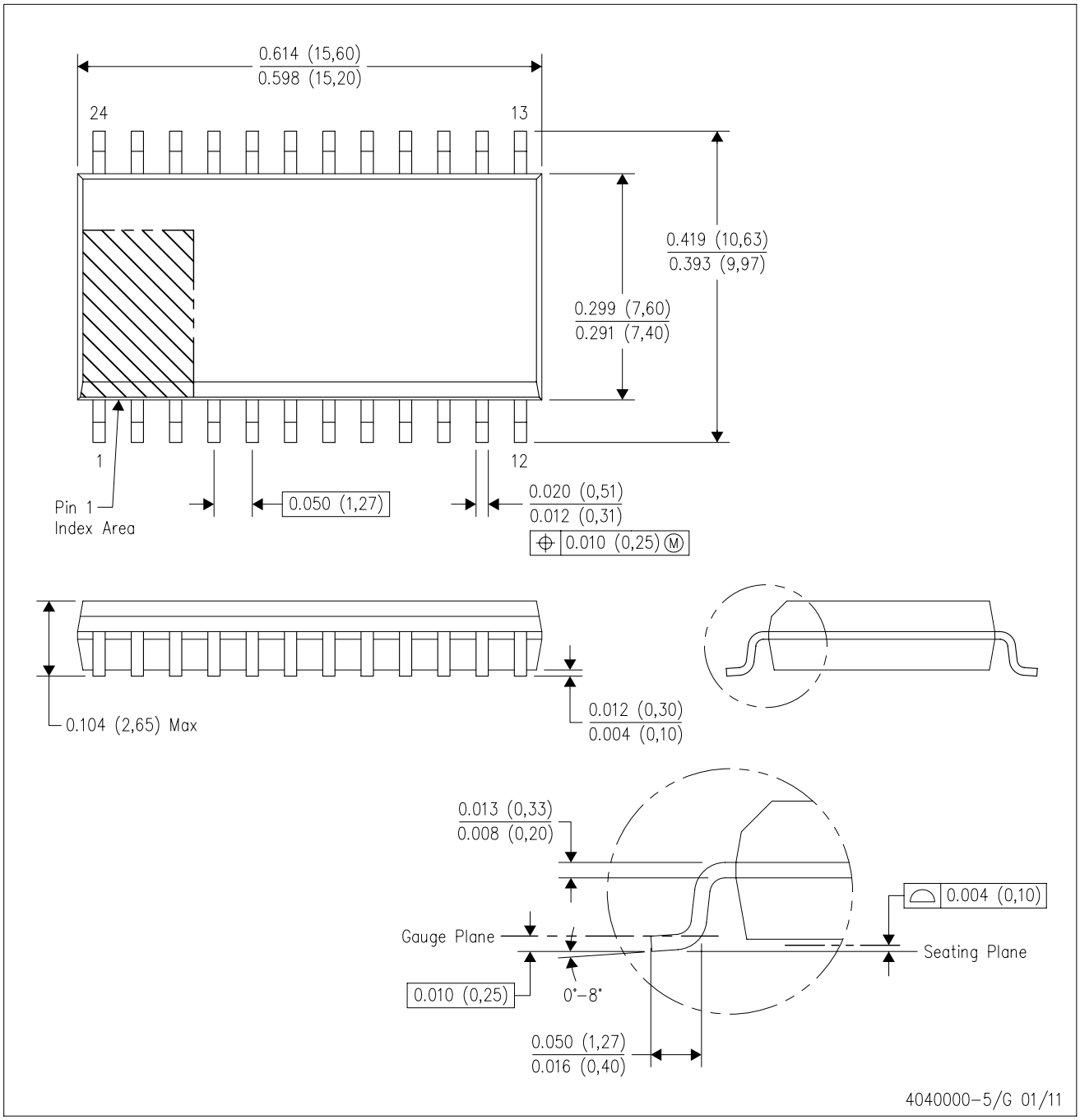


DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

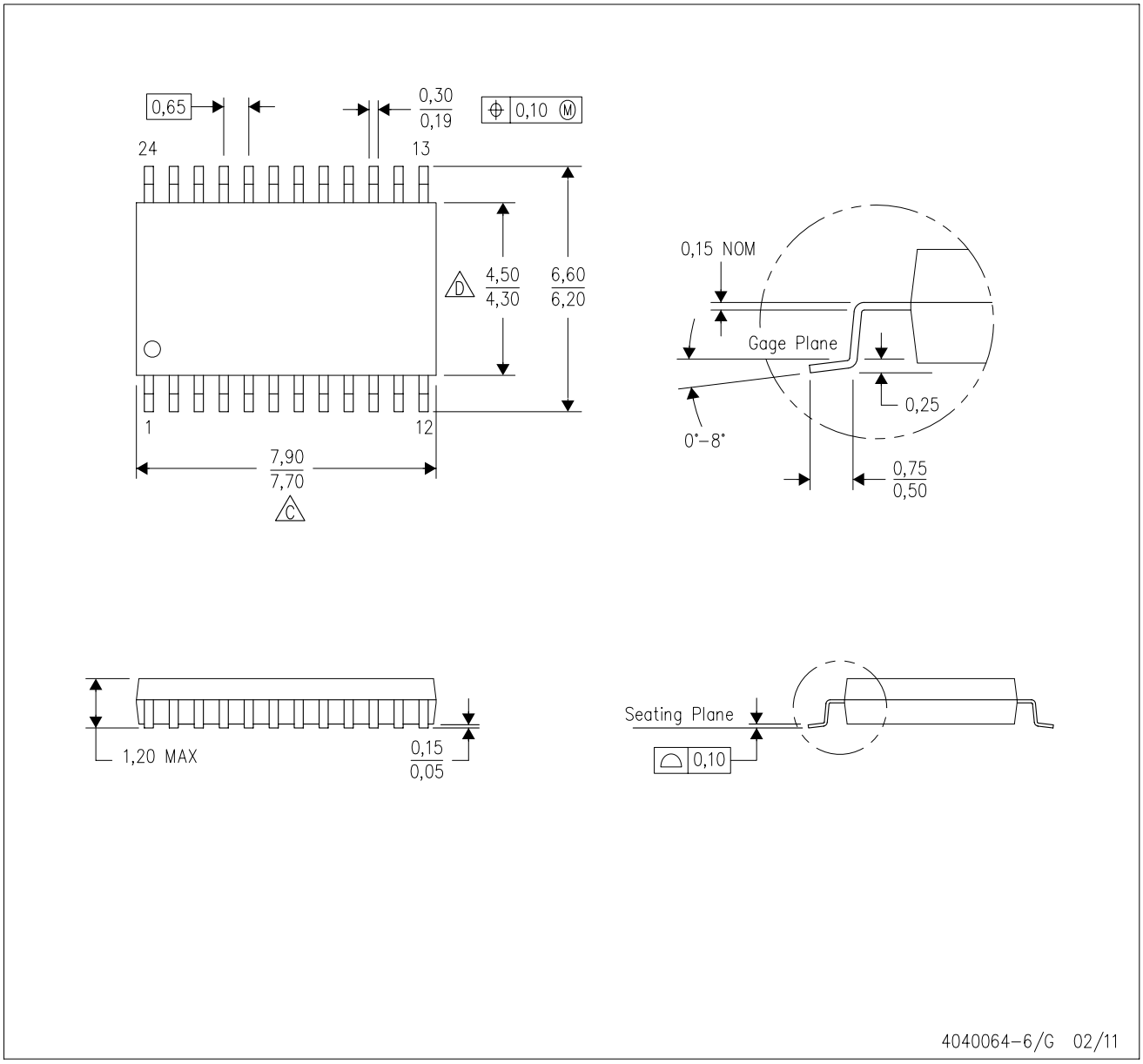
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



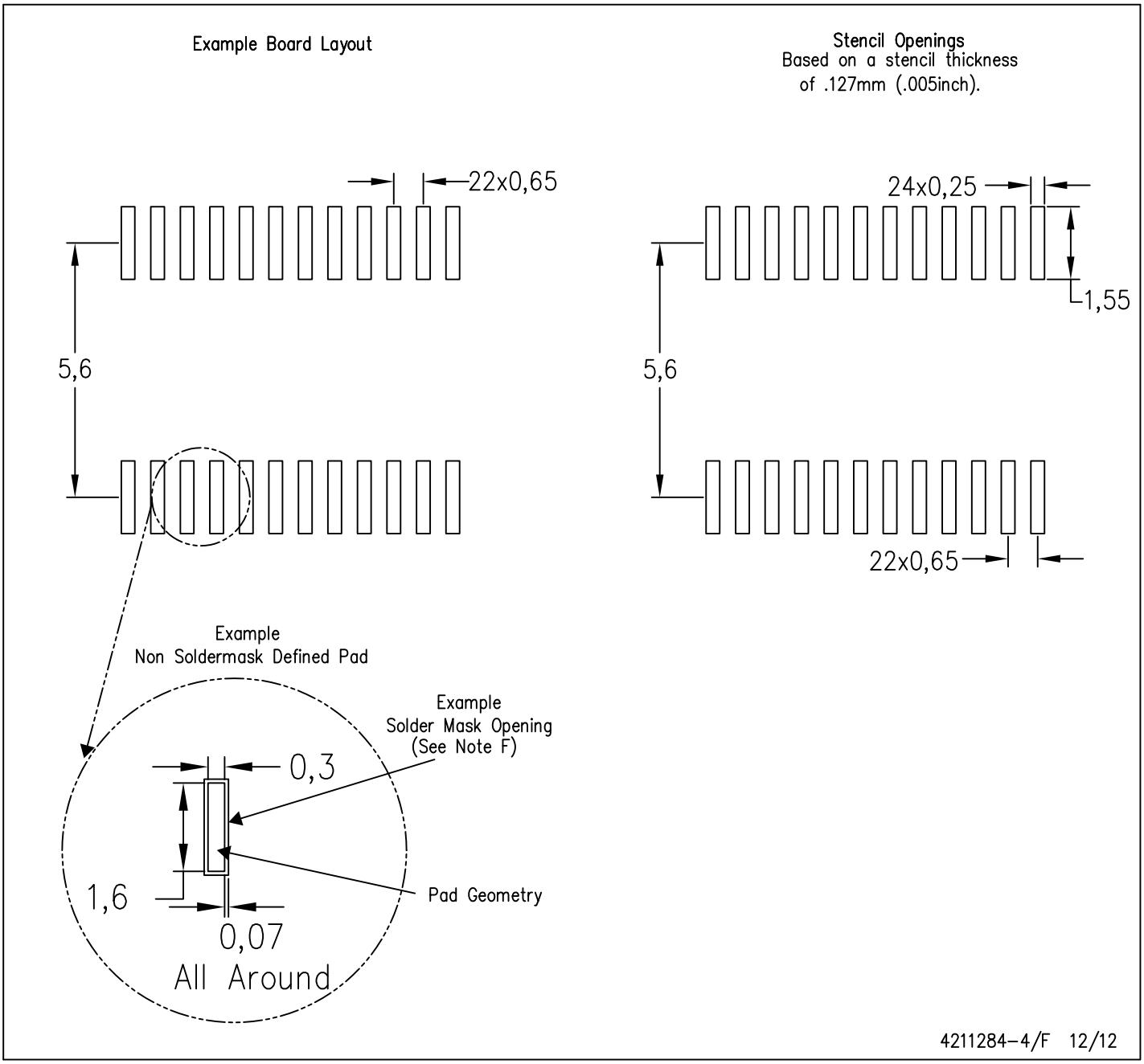
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

PW (R-PDSO-G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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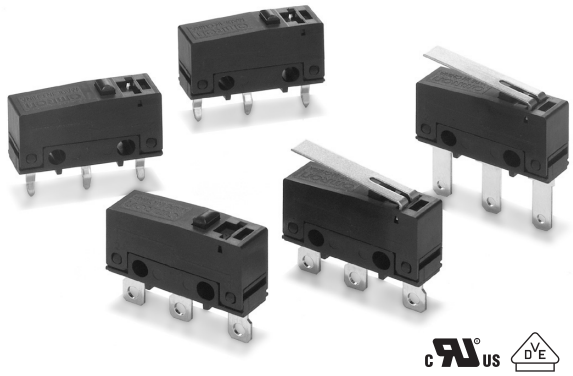
Subminiature Basic Switch
SS-P

SS Series Compatible Mounting with a Simple Construction and Easy-to-Use Design Concept

- Insert molded base and improved case-to-base seal provides enhanced resistance to flux.
- Switch rating of 3 A at 125 VAC possible with a single-leaf movable spring. Models for micro loads with gold crossbar contact are also available.
- Solder, quick-connect terminals (#110), and PCB terminals are available, including even-pitched PCB terminals.
- RoHS Compliant.



Ordering Information

Rating	Actuator	Terminals	Solder terminals	Quick-connect terminals (#110)	PCB terminals	
					Uneven pitch	Even pitch
3 A	Pin plunger		**SS-3GP**	**SS-3GPT**	**SS-3GPD**	**SS-3GPB**
	Hinge lever		**SS-3GLP**	**SS-3GLPT**	**SS-3GLPD**	**SS-3GLPB**
	Simulated roller lever		**SS-3GL13P**	**SS-3GL13PT**	**SS-3GL13PD**	**SS-3GL13PB**
0.1 A	Pin plunger		**SS-01GP**	**SS-01GPT**	**SS-01GPD**	**SS-01GPB**
	Hinge lever		**SS-01GLP**	**SS-01GLPT**	**SS-01GLPD**	**SS-01GLPB**
	Simulated roller lever		**SS-01GL13P**	**SS-01GL13PT**	**SS-01GL13PD**	**SS-01GL13PB**

Model Number Legend

SS-□ □□P□
1 2 3 4

1. **Ratings**
   3: 3 A at 125 VAC
   01: 0.1 A at 30 VDC

2. **Contact Gap**
   G: 0.5 mm

3. **Actuator**
   None: Pin plunger
   L: Hinge lever
   L13: Simulated roller lever

4. **Terminals**
   None: Solder terminals
   T: Quick-connect terminals (#110)
   D: PCB terminals (Uneven pitch)
   B: PCB terminals (Even pitch)

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Specifications

■ Characteristics

Operating speed	0.1 mm to 1 m/s (for pin plunger models)
Operating frequency	Mechanical: 300 operations/min Electrical: 30 operations/min
Insulation resistance	100 MΩ min. (at 500 VDC)
Contact resistance	SS-3P: 50 mΩ max. SS-01P: 100 mΩ max.
Dielectric strength (See note 2)	1,000 VAC, 50/60 Hz for 1 min between terminals of the same polarities 1,500 VAC, 50/60 Hz for 1 min between current-carrying metal parts and ground, and between each terminal and non-current-carrying metal parts
Vibration resistance (See note 3)	Malfunction: 10 to 55 Hz, 1.5-mm double amplitude
Shock resistance (See note 3)	Destruction: 1,000 m/s^2 (approx. 100 G) max. Malfunction: 300 m/s^2 (approx. 30 G) max.
Degree of protection	IEC IP40
Degree of protection against electrical shock	Class I
Proof tracking index (PTI)	175
Ambient operating temperature	–25°C to 85°C (at 60% RH max.) with no icing
Ambient operating humidity	85% max. (for 5°C to 35°C)
Life expectancy	Mechanical: 1,000,000 operations min. (60 operations/min) Electrical: SS-3P: 70,000 operations min. (20 operations/min, 125 VAC) 100,000 operations min. (20 operations/min, 30 VDC) SS-01P: 200,000 operations min. (20 operations/min)
Weight	Approx. 1.6 g (for pin plunger models)

Note: 1. The data given above are initial values.
2. The dielectric strength shown in the table indicates a value for models with a Separator.
3. For the pin plunger models, the above values apply for both the free position and total travel position. For the lever models, the values apply at the total travel position. Contact opening or closing time is within 1 ms.

■ Ratings

Rated voltage / Model / Item	SS-3P	SS-01P
	Resistive load	
125 VAC	3 A	0.1 A
30 VDC	3 A	0.1 A

Note: The electrical rating applies under the following test conditions:
Ambient Temperature = 20±2°C, Ambient Humidity = 65±5%, Operating frequency = 30 operations/minute

■ Approved Standards

UL Recognized (File No. E41515)
CSA Certified (UL approval)

Rated Voltage	SS-3P	SS-01P
125 VAC	3 A	0.1 A
30 VDC	3 A	0.1 A

EN61058-1 - - VDE approval
(File No. 40008425)

Rated Voltage	SS-3P	SS-01P
125 VAC	3 A	0.1 A
30 VDC	3 A	0.1 A

Testing conditions: 5E4 (50,000 operations), T55 (0°C to 55°C)

Note: The rated values approved by each of the safety standards (e.g. UL, CSA) may be different from the performance characteristics individually defined in this catalog.

■ Contact Specifications

Item	SS-3P	SS-01P
Specification	Rivet	Crossbar
Material	Silver alloy	Gold alloy
Gap (standard value)	0.5 mm	
Minimum applicable load (see note)	160 mA at 5 VDC	1 mA at 5 VDC

Note: Minimum applicable loads are indicated by N standard reference values. This value represents the failure rate at a 60% (λ_{60}) reliability level (JIS C5003).
The equation $\lambda_{60}=0.5 \times 10^{-6}$ / operations indicates that a failure rate of 1/2,000,000 operations can be expected at a reliability level of 60%

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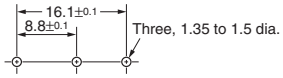
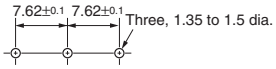
Engineering Data

■ Mounting Holes

PCB Mounting Dimensions (Reference - uneven spacing)

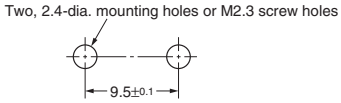


PCB Mounting Dimensions (Reference - even spacing)



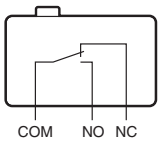
Panel Mounting

All switches may be panel mounted using M2.3 mounting screws with plane washers or spring washers to securely mount the switch. Tighten the screws to a torque of 0.23 to 0.26 N·m



■ Contact Form

SPDT



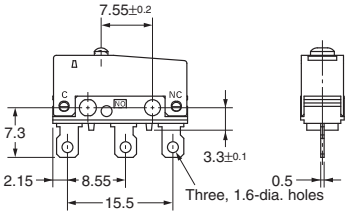
Dimensions

■ Terminals

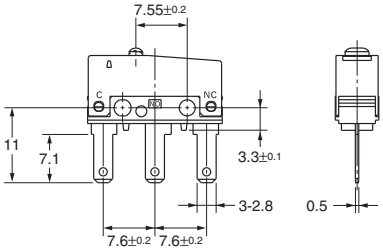
Note: 1. Unless otherwise specified, all units are in millimeters and a tolerance of ±0.4 mm applies to all dimensions

2. Terminal plate thickness is 0.5 mm for all models.

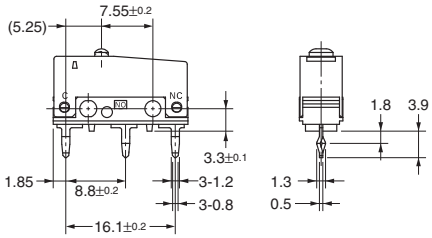
Solder Terminals



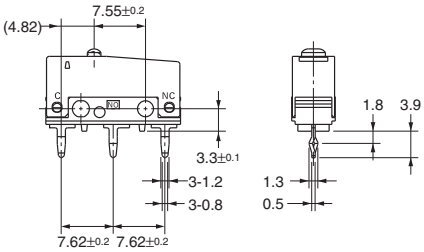
Quick-connect Terminals (#110)



PCB Terminals (Uneven pitch)



PCB Terminals (Even pitch)



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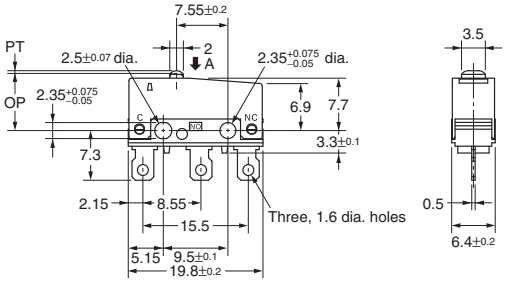
■ Dimensions and Operating Characteristics

Note: 1. Unless otherwise specified, all units are in millimeters and a tolerance of ±0.4 mm applies to all dimensions
2. The following illustrations are for solder terminal models. Refer to "Terminals" for models with quick-connect terminals (#110) and PCB terminals.
3. The operating characteristics are for operation in the A direction(⬇)

Pin Plunger Models

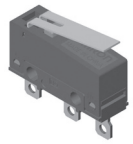
SS-3GP
SS-01GP

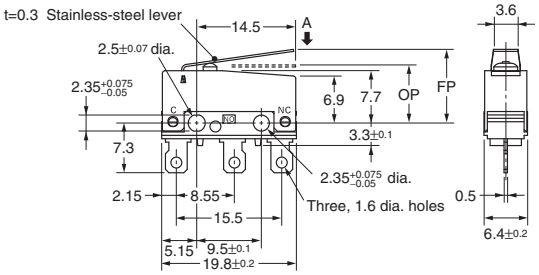


Characteristics	SS-3GP	SS-01GP
OF max.	153 gf	
RF min.	20 gf	
PT max.	0.6 mm	
OT min.	0.4 mm	
MD max.	0.15 mm	
OP	8.4 ± 0.3 mm	

Hinge Lever Models

SS-3GLP
SS-01GLP

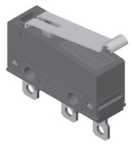


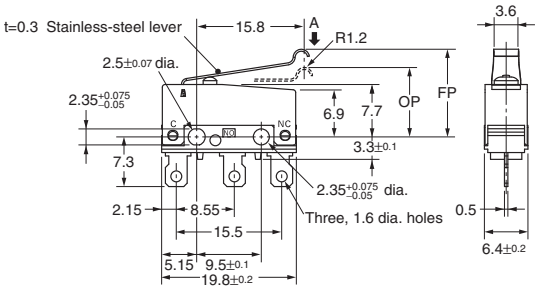


Characteristics	SS-3GLP	SS-01GLP
OF max.	51 gf	
RF min.	5 gf	
OT min.	1.0 mm	
MD max.	0.8 mm	
FP max.	13.6 mm	
OP	8.8 ± 0.8 mm	

Simulated Roller Lever Models

SS-3GL13P
SS-01GL13P





Characteristics	SS-3GL13P	SS-01GL13P
OF max.	51 gf	
RF min.	5 gf	
OT min.	1.0 mm	
MD max.	0.8 mm	
FP max.	15.5 mm	
OP	10.7 ± 0.8 mm	

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Precautions

■ Correct Use

Mounting

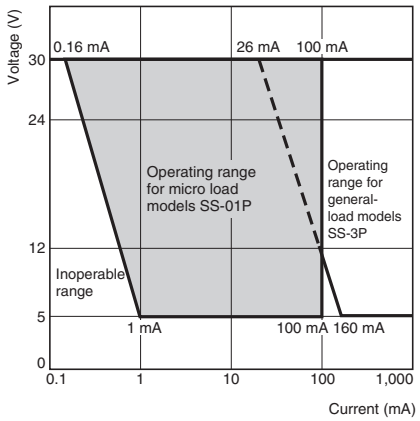
Mount the Switch onto a flat surface. Mounting on an uneven surface may cause deformation of the Switch, resulting in faulty operation or breakage in the housing.

Operating Stroke Setting

Take particular care in setting the operating stroke for the pin plunger models. Make sure that the operating stroke is 60% to 90% of the rated OT distance. Do not operate the actuator exceeding the OT distance, otherwise the life expectancy of the Switch may be shortened.

Using Microloads

Using a model for ordinary loads to switch microloads may result in faulty operation. Instead, use the models that are designed for microloads and that operate in the following range;



However, even when using microload models within the operating range shown above, if inrush current or inductive voltage spikes occur when the contact is opened or closed, it may increase contact wear and so decrease the service life. Therefore, insert a contact protection circuit where necessary.

■ Cautions

Handling

Turn OFF the power supply before mounting or removing the Switch, wiring, or performing maintenance or inspection. Failure to do so may result in electric shock or burning.

Solder Terminal Connection

When soldering lead wires to solder terminals, first insert the lead wire conductor through the terminal hole and then solder.

Make sure that the temperature at the tip of the soldering iron is 350 to 400°C. Do not take more than 3 seconds to solder the switch terminal, and do not impose external force on the terminal for 1 min after soldering. Improper soldering involving an excessively high temperature or excessive soldering time may deteriorate the characteristics of the Switch.

Quick-Connect Terminals

Wire quick-connect terminals (#110) with receptacles. Insert the terminals straight into the receptacles. Do not impose excessive force on the terminal in the horizontal direction, otherwise the terminal may be deformed or the housing may be damaged.

Use appropriate #110 QC connectors, made by Nippon Tanshi or Tyco Electronics, to mate with the quick-connect versions of the switch. These connectors are not sold by OMRON. Contact Nippon Tanshi or Tyco Electronics to purchase these connectors.

PCB Terminal Connection

When using automatic soldering baths, we recommend soldering at 260±5°C within 5 seconds. Make sure that the liquid surface of the solder does not flow over the edge of the board.

When soldering by hand, as a guideline, solder with a soldering iron with a tip temperature of 350 to 400°C within 3 seconds, and do not apply any external force for at least 1 minutes after soldering. When applying solder, keep the solder away from the case of the Switch and do not allow solder or flux to enter the case.

Insulation Distance

Use a separator between the switch and metal mounting panels, to ensure proper dielectric characteristics are achieved.

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ALL DIMENSIONS SHOWN ARE IN MILLIMETERS.
To convert millimeters into inches, multiply by 0.03937. To convert grams into ounces, multiply by 0.03527.

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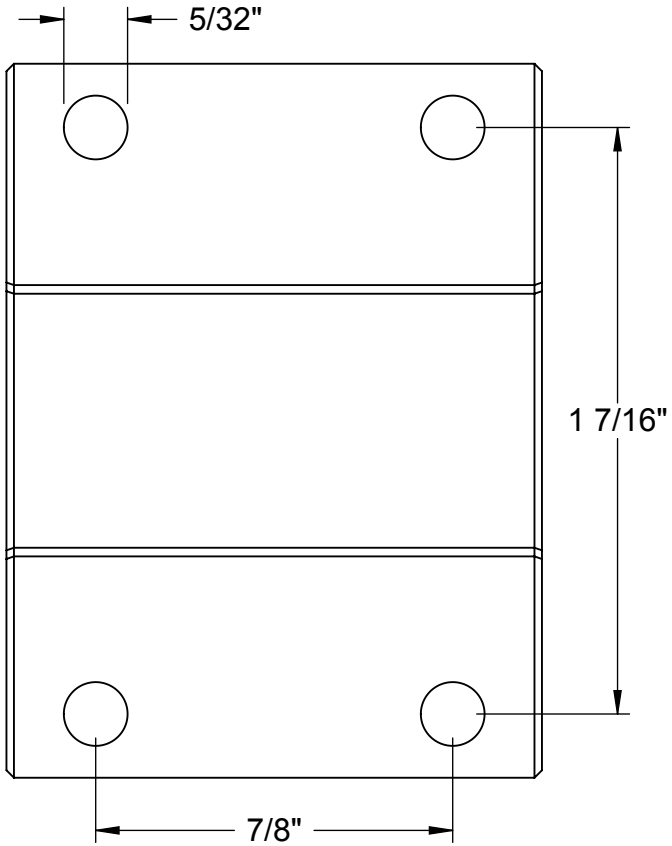
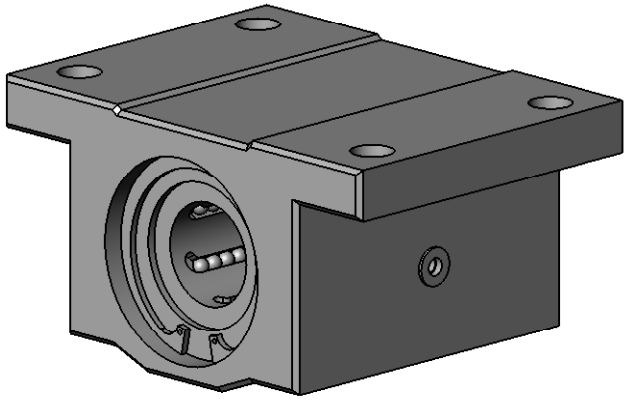
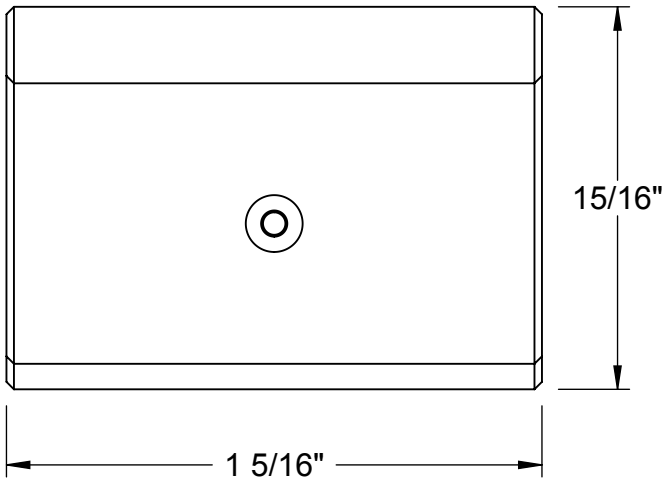
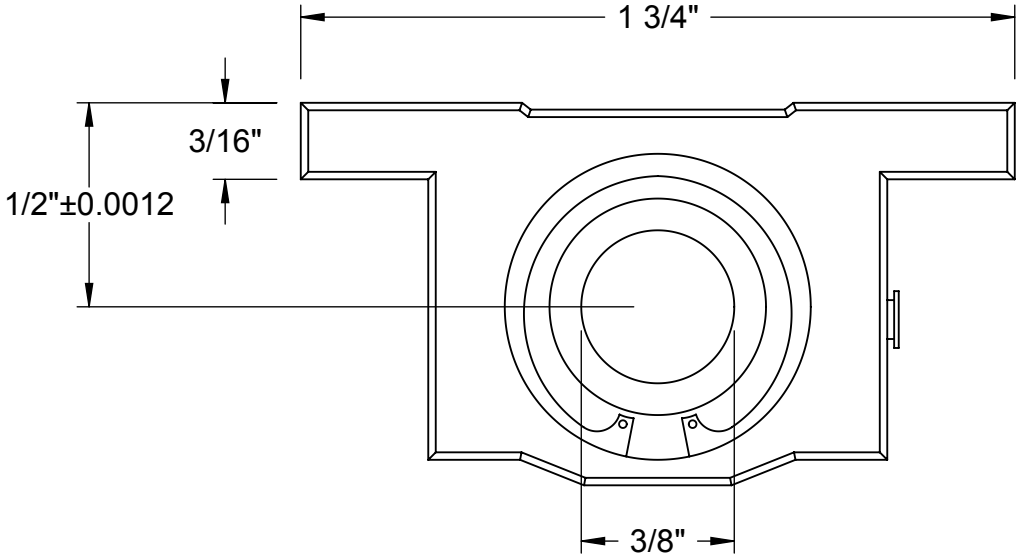








McMASTER-CARR® CAD	PART NUMBER	6255K32
http://www.mcmaster.com © 2011 McMaster-Carr Supply Company Information in this drawing is provided for reference only.	Pillow-Block Linear Ball Bearing	

11AV Series Linear Actuators

ANAHEIM AUTOMATION

FEATURES

- NEMA 11 (28.2mm Square)
- Single Size and Winding Available
- Single Lead Screw Available
- Unique Centering Bushing Option
- 1.8 Degree Stepping Motor
- Optional Adders Available

DESCRIPTION

Anaheim Automation's 11AV leadscrew Stepper Motors were designed to be the most versatile linear position motors in today's market. Based on the NEMA 11 hybrid step motor, they are available in thru-screw verisons with a variety of drive-nut and support bushing options. AV Linear Actuator motors are robust and can be easily configured to solve some of the most difficult application problems. Integration of a leadscrew with a motor saves space, elimates components, and reduces cost. While many standard configurations are available, custom modifications for OEM customers are welcome.

BUILD A PART NUMBER

11AV102 - AX - 06 - SB

Lead Screw Pitch (in)	
A	0.050"
C	0.125"

Lead Screw Length (in)	
06	6"
12	12"

Rear Attachment	
B	Bushing
C	Cover Only
E	Encoder
N	No Extension

EXAMPLE:
11AV102CX12-SC = NEMA 11 Frame, 1 Stack, 1.0A Motor, 0.125" screw pitch resolution, 12" screw length, Standard Nut on the front of the motor and a cover on the rear.

Note: See *Accessories* on our website for optional encoder and/or connector adders.

L010786

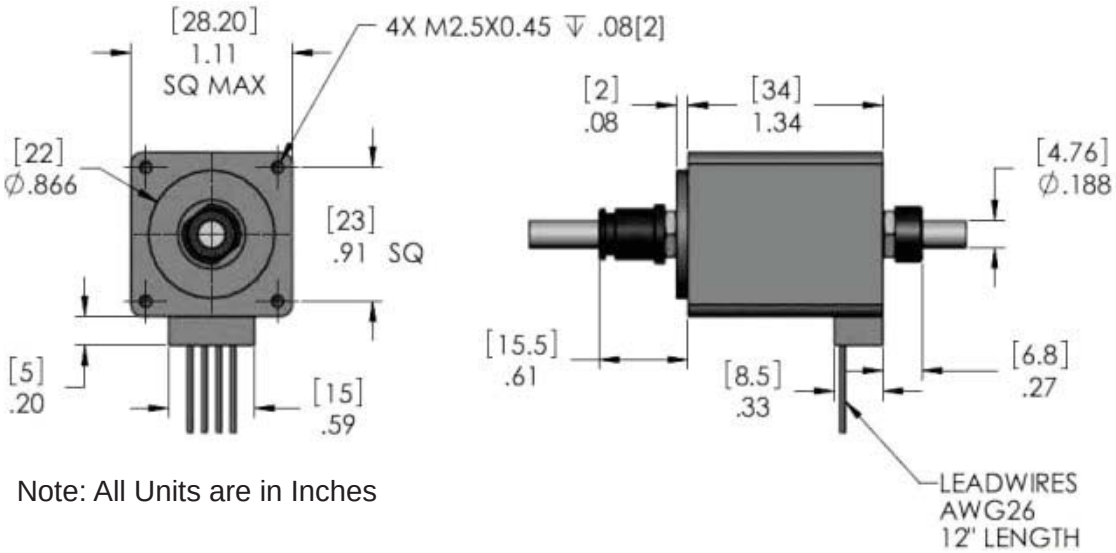
910 East Orangefair Ln. Anaheim, CA 92801 **Tel. (714) 992-6990** Fax. (714) 992-0471 **www.anaheimautomation.com**

SPECIFICATIONS

Motor Specifications									
Model Number	Series Voltage (V)	Series RMS Current (A)	Series Resistance (ohms)	Power (W)	Series Inductance (mH)	Rotor Interia (oz/sec^2)	Number of Leads	Motor Weight (oz)	Motor Length (in)
11AV102	3.2	1.0	2.1	3.2	1.5	1.28×10^{-4}	4	3.9	1.34

Screw Pitch Options						
Screw Pitch	Screw Pitch (in)	Static Force (lb)	Dynamic Force (lb)	Travel per Full Step (in)	Travel per Microstep (in)	Positioning Accuracy (in)
A	0.050	32	27	0.00025	$.98 \times 10^{-6}$	0.0004
C	0.125	20	16	0.00063	2.44×10^{-6}	0.0004

DIMENSIONS

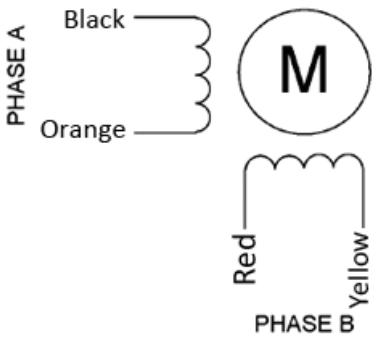


Note: All Units are in Inches

WIRING INFORMATION

Switching Sequence

Step	Black	Orange	Red	Yellow
1	+	-	+	-
2	-	+	+	-
3	-	+	-	+
4	+	-	-	+



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Angled Acrylic Box Display Cases with Hardwood Base

Angled Acrylic Box Display Cases with Clear Base

Angled Acrylic Box Display Cases with Black Base

Clear Acrylic Box Display Cases with Hinged Lid

Clear Acrylic Box Display Cases with Angled Top and Hinged Lid

Clear Acrylic Bases for Acrylic Box Cases

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Acrylic Display Risers, Stairs & More

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Glass Domes

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Item Number: AD0704

These Display Cases with no Base are 10" x 10" x 10" (Interior Dimensions). The Acrylic Display Case walls are 1/4" thick. Our Clear Box Acrylic Display Cases from Collecting Warehouse will show case your items and protect them at the same time.

Quantity	Price
1 – 2	$36.72
3 +	$33.05

Quantity in Cart: 1 ($36.72 each)

1 Add to Cart

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This Size Acrylic Box Case is also available with the options shown below:

Acrylic Display Case with Hardwood Base 10" x 10" x 10"

Case walls are 1/4" thick.

Quantity	Price
1 – 2	$64.34
3 +	$57.91

1 Add to Cart

Acrylic Display Case with Clear Base 10" x 10" x 10"

Case walls are 1/4" thick.

Quantity	Price

Doll Display Cases & Doll Domes
Plastic Clamshell Storage Display Cases
Action Figure Cases
Glass Cases, Clear Display Show cases
Plastic Zip Lock Bags
Action Figure Stands - Bases
Ornament Stands and Hanger Displays
Mirrors - Table Centerpiece - Display Mirrors
Acrylic & Wood Display Bases
Car Display Cases
Clear Acrylic Easels and Plastic Displays
Sports Ball Case Displays
Adhesive Backed Rubber Feet
About Us

1 – 2	$59.15
3 +	$53.23

1 Add to Cart

Acrylic Display Case with Black Base 10" x 10" x 10"

Case walls are 1/4" thick.

Quantity	Price
1 – 2	$63.41
3 +	$57.06

1 Add to Cart