DEVELOPMENT OF A SENSOR READOUT INTEGRATED CIRCUIT TOWARDS A CONTACT LENS FOR WIRELESS INTRAOCULAR PRESSURE MONITORING

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TITLE: Development of a Sensor Readout Integrated Circuit Towards a Contact Lens for Wireless Intraocular Pressure Monitoring

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ABSTRACT

Development of a Sensor Readout Integrated Circuit Towards a Contact Lens for Wireless Intraocular Pressure Monitoring

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This design covers the design of an integrated circuit (IC) in support of the active contact lens project at Cal Poly. The project aims to monitor intraocular eye pressure (IOP) to help diagnose and treat glaucoma, which is expected affect 6.3 million Americans by 2050. The IC is designed using IBM's 130 nm 8RF process, is powered by an on-lens thin film 3.8 V rechargeable battery, and will be fabricated at no cost through MOSIS. The IC features a low-power linear regulator that powers a current-starved voltage-controlled oscillator (CSVCO) used for establishing a backscatter communication link. Additional circuitry is included to regulate power to and from the battery. An undervoltage lockout circuit protects the battery from deep discharge damage. When recharging, a rectifier and a voltage regulator provides overvoltage protection. These circuit blocks are biased primarily using a 696 mV subthreshold voltage reference that consumes 110.5 nA.

Keywords: RF-DC converter, backscatter, LDO, linear regulator, subthreshold voltage reference, ring oscillator, intraocular pressure, UVLO, undervoltage lockout

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I would like to thank Professor Tina Smilkstein for providing me with the opportunity to contribute to this project. I would also like to thank my mother, for having the patience to put up with me for all these years.

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CHAPTER 1: INTRODUCTION

This thesis encompasses the design of an integrated circuit (IC) in support of the active contact lens project at Cal Poly. The contact lens project has the goal of integrating a biosensor system within a contact lens. Thus, it is necessary to design a circuit to interface with the sensor, and transmit sensor data off the contact lens. There are many biological parameters that could be measured on the eye. This thesis concentrates on the circuitry for managing power and data transmission from a capacitive sensor, and the targeted sensor is an intraocular pressure sensor to help diagnose and treat glaucoma.

Glaucoma is a disease that damages the eye's optic nerve with the potential for vision loss and blindness. According to the National Eye Institute (NIH), glaucoma affects 2.7 million Americans as of 2010, and this number is projected to more than double to 6.3 million by 2050 [1]. Glaucoma is closely linked to high intraocular pressure (IOP) exceeding 21 mmHg and is typically measured by an ophthalmologist at a single point in time during the day. However, this is not an adequate benchmark for a proper diagnosis as a person's IOP will fluctuate throughout the day, and the range of fluctuations varies from person to person [2]. Glaucoma has been diagnosed in patients with IOP levels as low as 14 mmHg and, conversely, IOP levels above the 21 mmHg threshold have been measured in people with no symptoms of glaucoma [3]. It is suggested in [2], [4], and [5] that characterizing IOP peaks and fluctuations over a 24 hour period provides a better metric for assessing a patient's risk factor for glaucoma. In [6], a retroactive study on glaucoma patients treated between 1965 and 1980 also suggests that therapy based on irregular IOP measurements is insufficient for preventing loss of vision. Methods are available for continuously monitoring IOP over a 24 hour period in a clinical setting, but they can be costly and inconvenient for patients. Nonetheless, these techniques have merit in the valuable data they provide as

demonstrated in [5] where 36% of patients received a change in therapy due to the additional IOP data from extended monitoring.

An integrated biosensor system within a contact lens offers ophthalmologists and their patients a convenient means for noninvasive and continuous monitoring of IOP. The idea of a contact lens instrumented with a biosensor goes as far back as 1974 in [7], which explored the idea of embedding a strain gauge within a contact lens. The shortcoming of their design is that it required mechanical calibration of the strain gauges to properly fit to the shape of the eye on a case by case basis, which is not a cost effective process. More recently in 2004, [8] presents another contact lens integrated with a strain gauge and a thin, flexible cable for connecting to external electronics for calibration and measurements. Although it is unrelated to measuring IOP, [9] features a contact lens with an electrochemical sensor for monitoring glucose levels in ocular fluids. Their design is of interest as it integrates a loop antenna and an integrated circuit for wireless telemetry of measurements. In a departure from strain gauge sensors, [10] and [11] utilize capacitive pressure sensors that exhibit higher sensitivity to changes in pressure, and also feature components for wireless communication. Another design in [12] from the University of Michigan integrates a rechargeable battery alongside a miniature solar cell. Their design, however, requires surgery to implant the device into the anterior chamber of the eye.

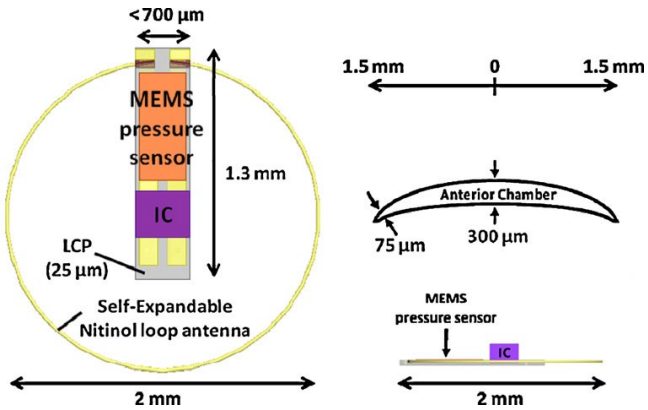

Figure 1.1 - Packaging of contact lens with a capacitive IOP sensor from [10]

The active contact lens project at Cal Poly is an ongoing interdisciplinary research project led by Dr. Tina Smilkstein with the goal of creating its own version of a contact lens platform for monitoring intraocular eye pressure. Previous work on the project was carried out by former Cal Poly electrical engineering students Errol Leon, Benny Ng and Alex Do [13][14][15]. They were supported by biomedical engineering students Paul Heckler and Philip Azar [15]. Benny, Errol, and Alex collaborated on an antenna design that acts as a receiving antenna at 2.4 GHz for communication, and as an inductive coil at 13.56 MHz for power scavenging [13][14]. Because of issues with the antenna's coupling efficiency, it was decided that an on-lens power source would be needed. After evaluating several potential power sources, the team settled on using a rechargeable Cymbet thin film battery. They worked together with the biomedical engineering students to evaluate the biocompatibility and mechanical properties of different materials as a potential contact lens substrate. In addition to selecting a substrate material, the team performed preliminary work on encapsulation of project components within the chosen material. The effects of heat transfer on the human eye were also modeled using COMSOL, which indicated that a continuous power dissipation of 10 mW

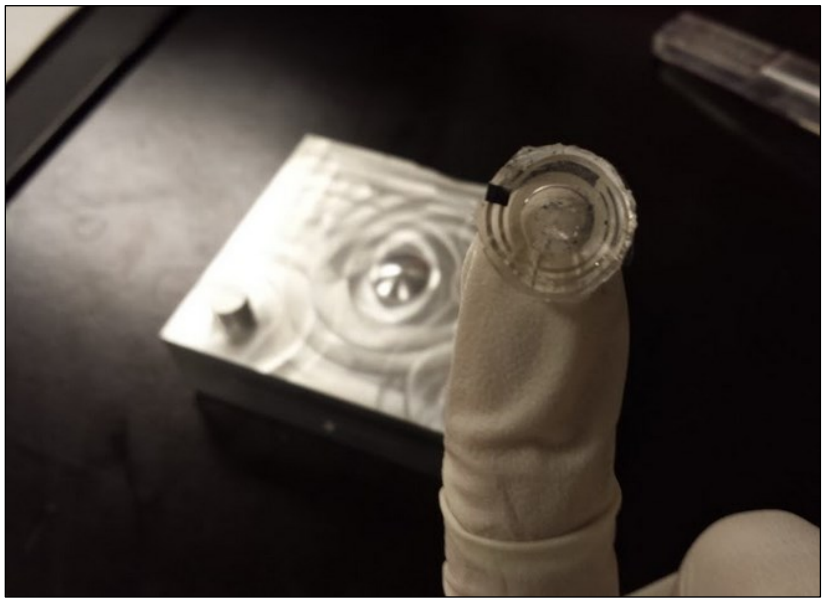

Figure 1.2 - Encapsulated contact lens [13]

induces no more than 0.7 °C in the cornea of the eye [15]. Former undergraduate student Matthew Lin carried out work to create a piezoelectric pressure sensor, but was not successful [16].

One of the key components of the active contact lens project is the integrated circuit through which all other project components will interface with each other. Benny Ng designed the first IC using ON Semiconductor's C5N 0.5 μm process, and had it fabricated by MOSIS (Metal Oxide Semiconductor Implementation Service). However, test results on the fabricated chips revealed design flaws [14]. An internal voltage reference was designed to generate 2.5 V, but was not functional. Consequently, all other circuits relying on the voltage reference were nonfunctional as well. It is interesting to note that some parts of the design use the reference as though it were a regulated supply capable of sourcing current. This is likely the root cause of the problem as voltage references are normally not capable of sourcing any significant current. As a workaround, an external 2.5 V generated from a bench power supply was applied at one of the probe pads included in the chip layout for testing. Additional testing showed that the low voltage cutoff for preventing deep discharge of the battery did not trigger at the desired cutoff value. Furthermore, the rectifying circuitry for recharging the battery did not generate the minimum voltage needed to do so. The major shortcoming of the rectifier is that it treats the battery as a constant resistive load based only on its nominal internal cell resistance when discharging. The internal resistance when charging is different from its nominal rating when discharging. In spite of these issues, it should be noted that some components of the Cadence software suite used to design and lay out the chip were not fully functional at the time. It is a credit Benny that he was still able to successfully complete a design that met fabrication requirements set by MOSIS.

A new integrated circuit is designed in this thesis. With regard to power regulation, the design features an improved rectifier circuit for recharging the battery, a

new subthreshold voltage reference, and a separate internally regulated supply capable of sourcing current to other subcircuits. The circuit is designed using the smaller IBM 130 nm 8RF process, and is expected to be fabricated in the future by MOSIS through their educational program at no cost. Chapter 2 begins with a discussion on the design constraints and specifications. Chapter 3 begins the design on the voltage reference, and voltage regulator. The proposed wireless communications method for transmitting measurement data is detailed in Chapter 4. Chapter 5 goes over all the circuitry used for power management. Chapter 6 discusses the interfacing of all the subcircuits. The report concludes in Chapter 7, and a brief discussion of future work is presented in Chapter 8.

CHAPTER 2: DESIGN OVERVIEW

2.1. Design Constraints

Before discussing the goals of the design for the integrated circuit, it is first necessary to define the project constraints. The primary constraints on the design are set by the specifications of the thin film battery, the performance of the antenna previously designed in [13]-[15], and the type of IOP sensor. There are also additional design considerations relating to the available chip area, and limits on RF power due to safety in terms of temperature changes of the lens.

2.1.1. Cymbet CBC005 Thin Film 5 µAh Rechargeable Battery

From previous work completed on the project in [13], [14], and [15], the power source is the rechargeable Cymbet CBC005 thin film battery. It measures 1.7 mm X 2.25 mm, and is 200 µm thick [17], making it well suited for encapsulation within the dimensions of a contact lens. It is also designed to be attached by wirebonding, a common method for establishing interconnections with integrated circuits.

The battery complies with both the directive on the Restriction of Hazardous Substance (RoHS), and the regulations on Registration, Evaluation, Authorization, and Restriction of Chemicals (REACH) [18]. RoHS places restrictions on a ten chemicals identified as hazardous to humans, and only pertains to them as used in electronics [19]. REACH is significantly broader in scope with restrictions placed on over 40,000 chemicals, and is not limited to the electronics industry [20]. Compliance with both standards is desirable given that the battery will be used within the human body. More critically given the goals of the lens project, the battery has been proven to be non-cytotoxic for *in vitro* and *in vivo* applications [18][21]. Its biological safety was assessed in [21] by crushing the battery to replicate a catastrophic failure, exposing the internal

solid state battery materials, and injecting the material into an *in vivo* environment where the materials exhibited no toxic effects on exposed tissue.

The battery has a nominal output voltage of 3.8 V and a 3 V cutoff voltage, which is defined as the "empty" state of the battery [17]. The CBC005 is rated for a discharge capacity of 5 µAh, meaning that it can continuously supply 5 µA at 3.8 V for one hour before falling to its cutoff voltage [22]. At higher load currents, its capacity decreases by a proportionate amount. For example, pulling four times the rated current at 20 µA will cut the discharge time by one-fourth to 15 minutes. Similarly, the battery will last twice as long at a lighter load of 2.5 µA. However, battery chemistry places limits on the maximum current it can supply. The CBC005 discharge characteristics in Figure 2.1 show it can supply a maximum of a little over 10 µA continuously [17].

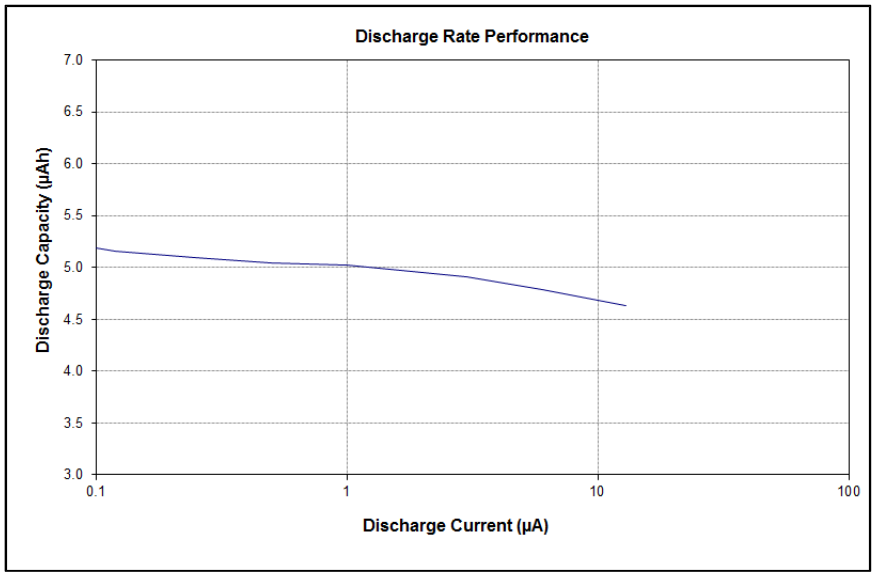

Figure 2.1 - CBC005 discharge characteristics

To recharge the battery, the guidelines in [23] specify that a constant voltage ranging from 4 V to 4.3 V be applied to the terminals of the battery. The recommended charging voltage is 4.1 V. Values above the nominal recharge voltage reduces the number of life time recharge cycles, whereas values below it reduces its discharge capacity. Considerations also need to be made to ensure that the charging supply can deliver the

necessary current. Figure 2.2 shows the CBC005 charging profile. The battery should not be discharged below its rated cutoff voltage of 3 V. Deep discharge of the battery below 3 V will damage the battery and reduce its overall lifetime [17][23].

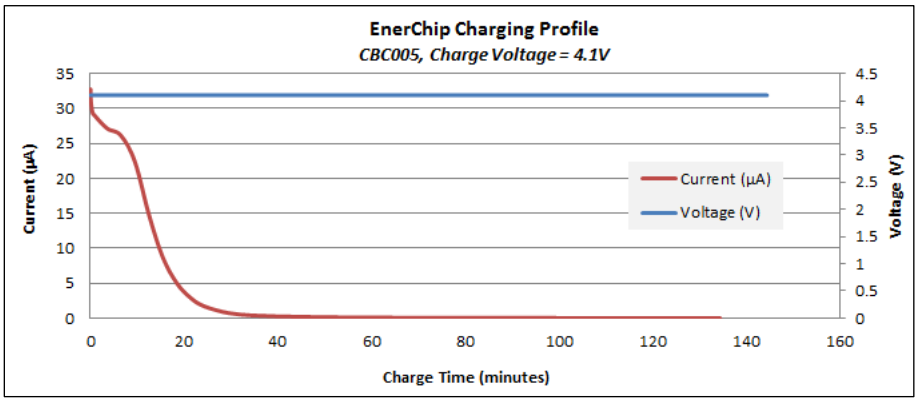

Figure 2.2 - CBC005 charging profile for a 4.1 V charge voltage

2.1.2. Antenna Performance

The finalized antenna design in [13] and [14] is an inverted-F antenna (IFA) that acts as a receiving antenna at 2.4 GHz, and as an inductive charging coil at 13.56 MHz., which is the standard frequency for near field communication (NFC) [24]. NFC has been demonstrated in [25] to be suitable for wireless power delivery of up to 1 W at the receiver side, corresponding to a received power level of 30 dBm. Measurements in [13] and [14] show the IFA can output 22 dBm of power when inductively coupled with a 30 dBm source. At 2.4 GHz, it has an efficiency of 33.5% at a distance of 42 cm.

2.1.3. Type of Intraocular Pressure Sensor

An intraocular pressure sensor has not been successfully designed and characterized at Cal Poly. Errol Leon fabricated strain gauge sensors using resources available in the microfabrication lab provided by the biomedical engineering department. He was able to encapsulate the sensors within a contact lens substrate, but could not characterize their sensitivity to pressure changes due to a lack of test equipment [13].

Matthew Lin pursued a piezoelectric design, but was unable to create a functional sensor because of limitations on the equipment available [16]. Thus, assumptions will have to be made regarding the performance of the IOP sensor based on other reported designs.

Strain gauge designs are featured in [7] and [8]. The designs in [7] were measured to have resistances ranging from 300 to 960 Ω with a sensitivity of 0.08 Ω/mmHg on rabbit eyes. The sensor in [8] was characterized with a sensitivity of 8.37 μV/mmHg using juvenile porcine eyes. Each report did not include sufficient information to relate the different units of measurement to one another.

Capacitive IOP sensors are presented in [10] and [11]. There are two sensors in [10]. One has a base capacitance of 1.167 pF with a sensitivity of 0.75 fF/mmHg. The second has a smaller base capacitance of 784.92 fF with a sensitivity of 0.3 fF/mmHg. The work in [11] resulted in a sensor with a much larger 12.06 pF base capacitance and a sensitivity of 20 fF/4.5 mmHg.

The capacitive sensors are more appealing given that they do not consume any real power and can be driven with the microamp current levels available from the battery. In contrast, the base resistance of a strain gauge must be large to function with the small currents. Assuming the battery voltage is regulated down to 1 V by the integrated circuit and 5 μA is used to drive the strain gauge, the base resistance needs to measure 200 kΩ, which is over two orders of magnitude larger than the strain gauge reported in [7]. Thus, the design will proceed with the assumption that the IC will interface with a capacitive sensor with a capacitance ranging from 700 fF up to 12 pF.

2.1.4. Additional Design Constraints

MOSIS imposes size limits on chips fabricated through their educational program. The total dimensions of the chip cannot exceed 1.5 mm X 1.5 mm, including the space taken up by IO pads. The pads take up 350 μm on all sides of the chip, leaving

a working area of 800 µm X 800 µm for all circuits and wiring. Additional area will also be consumed by the placement of probe pads for testing.

With regard to the RF power levels used for communication, the transmitted power should follow guidelines specified by the IEEE C95 standard [26]. The maximum allowable power density *S* for signals in the 30 to 3000 MHz range is

$$S = \frac{f_{MHz}}{30}$$

At 2.4 GHz, this evaluates to a maximum power density of 80 W/m^2, or 8 mW/cm^2. There is no concern for human safety with regard to power density when recharging at 13.56 MHz as this occurs when the lens is removed from the eye.

2.2. Design Specifications

The integrated circuit cannot draw more than 10 µA at any point because of limitations on the battery. Since the project is interested in monitoring IOP over 24 hours, the IC must feature a sleep state where current consumption is minimized. Dividing the nominal 5 µAh discharge capacity over 24 hours yields a maximum continuous discharge current of 208 nA in the standby state. Furthermore, the sleep circuit needs to be able to wake the core measurement circuits within the performance parameters of the antenna and RF power limits discussed in sections 2.1.2 and 2.1.4, respectively. The recharging circuit needs to function using no more than 22 dBm of power as specified in section 2.1.2. It must also clamp the applied voltage within 4 to 4.3 V. Additional cutoff circuitry needs to be included to stop the battery from discharging below 3 V.

These specifications for the IC are summarized in Table 2.1. The design will proceed according to the preliminary block diagram in Figure 2.3. Additionally, the design uses IBM's 130 nm 8RF process and will be fabricated through MOSIS in the future. Several types of transistors are available, with maximum voltage ratings ranging

from 1.6 V up to 3.6 V. Their characteristics vary in many ways, but at this point the discussion will focus on differences in the threshold voltages V_{TN} and V_{TP}, and the transconductance parameters K_N and K_P. Each of these parameters vary with sizing and biasing point. To obtain an initial ballpark value for these parameters, each transistor is characterized using the circuit in Figure 2.4 and measuring the current with a 1 V gate voltage when V_{DD} is at 1 V. For PMOS transistors, the current is measured with V_{SS} at 1 V. All transistors are sized with 2 μm widths and lengths. The threshold voltages and transconductances are summarized in Table 2.2.

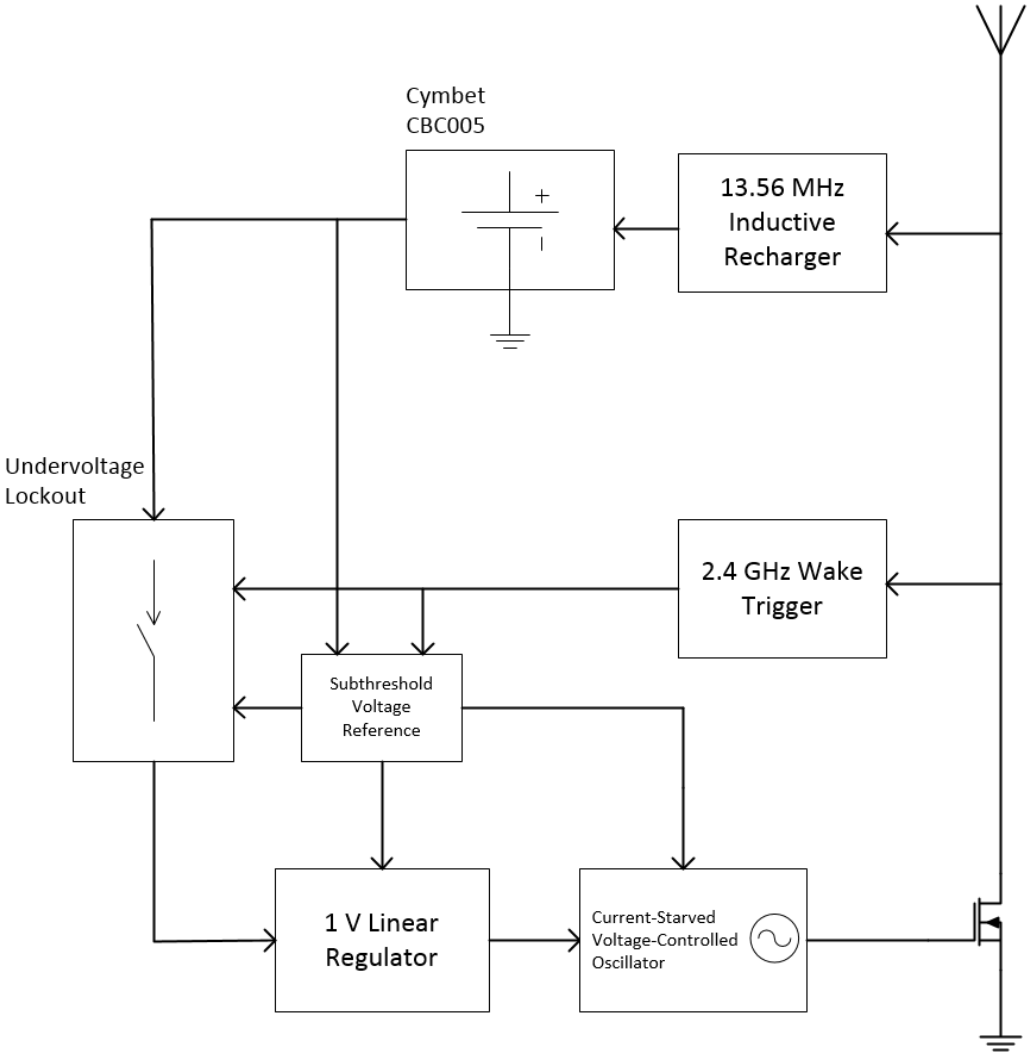

Figure 2.3 - Initial block diagram for the integrated circuit

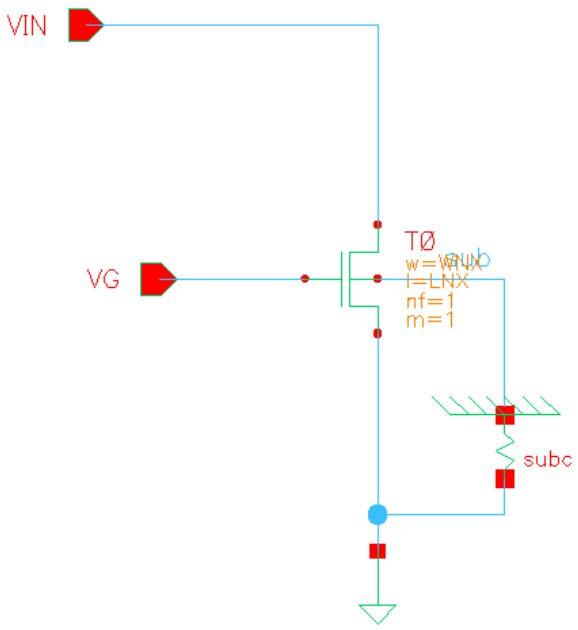

Figure 2.4 - Test circuit for characterizing transistors

Table 2.1 - Summary of design specifications

Parameter	Specification
Nominal Battery Voltage	3.8 V
Cutoff Voltage	3.0 V
Nominal Charge Voltage	4.1 V
Maximum Current	10 µA
Discharge Capacity	5 µAh
Maximum Standby Current	208 nA
Power Available for Recharge	22 dBm

Table 2.2 - Basic transistor characteristics

NMOS Transistor	Drain Current I_D (µA)	Threshold V_{TN} (mV)	Transconductance K_N (µA/V^2)
NFET	REDACTED		
LPNFET			
LVTNFET			
DGNFET			
NFET33			
PMOS Transistor	**Source Current I_S (µA)**	**Threshold V_{TP} (mV)**	**Transconductance K_P (µA/V^2)**
PFET	REDACTED		
LPPFET			
LVTPFET			
DGPFET			
PFET33			

CHAPTER 3: CORE CIRCUITRY

3.1. Voltage References

The majority of analog circuits is dependent on some bias circuit that produces a reliable reference voltage or current. The reference is necessary for ensuring the transistors operate in the desired mode [27]. In general, an analog circuit is only as accurate as the reference used to derive its bias point [28]. Consequently, analog designs begin with creating the necessary voltage or current reference. For this project, the design begins with establishing a reliable voltage reference with high immunity to variations in supply voltage and temperature. To achieve temperature independence, voltage references are derived from the sum of two voltages with opposite temperature coefficients. In other words, a voltage that is proportional to absolute temperature (PTAT), which rises with temperature, is combined with another voltage that decreases with temperature such that it is complementary to absolute temperature (CTAT). By combining the PTAT and CTAT voltage, the result is an ideal voltage reference with zero temperature coefficient [27]-[29]. Realistically, the reference will still exhibit some small temperature coefficient, and it is up to the designer to minimize the temperature coefficient across the expected operating range of temperatures.

3.1.1. Traditional Voltage References

Early voltage references were derived from temperature-compensated Zener diodes [30]. Zener voltage references are easily implemented by applying a sufficient voltage to drive the diode into reverse bias, along with a current limiting resistor tied to the supply. Because it requires a voltage in excess of 6 V to drive it into breakdown, Zener references quickly fell out of use in integrated circuits as shrinking transistor processes required smaller supply voltages [30].

In 1971, Widlar popularized the classical bandgap voltage reference (BGR) [30]. The BGR presented by Widlar derives a CTAT voltage from an emitter-base junction, and a PTAT voltage from the differential voltage of two additional emitter-base junctions operating at different currents. The result is a reference of approximately 1.2 V, close to the bandgap of silicon. This was later improved by Paul Brokaw in 1974 to allow for scalable reference values above 1.2 V [31]. CMOS implementations of the BGR are possible by exploiting the parasitic PNP BJT that appears in the substrate [27][29].

As with the Zener-based references, references above 1.2 V are not compatible with shrinking processes. However, BGRs below 1.2 V can be implemented by summing two currents that are PTAT and CTAT, then applying the current across a resistor to obtain a temperature independent voltage [27]. There are also beta multiplier references (BMR) that use only MOSFETs and resistors [29]. The biasing for these methods presented in [27]-[29], however, are not suitable for this project as the necessary currents exceed what is available from the thin film battery.

3.1.2. Subthreshold Voltage References

Traditionally, MOSFETS are operated in the linear or saturation region, and it is assumed that the transistor turns off when $V_{GS} < V_{TN}$, resulting in zero drain-source current. In reality, current flows through the channel even when V_{GS} is below the threshold voltage V_{TN}. This mode of operation is called subthreshold conduction, and is also commonly referred to as the weak-inversion mode [27][29]. Qualitatively, subthreshold conduction can be attributed to nonideal diffusion of electrons through the transistor channel in the presence of any finite gate voltage [32]. The subthreshold current is orders of magnitude less than the current normally observed in the linear and saturation modes, and ranges from picoamps up to nanoamps. This effect is greatly exacerbated in

deep submicron technologies, and is especially problematic in digital circuits as it increases static power consumption [32].

However, subthreshold conduction is especially appealing in small, low power applications for minimizing power consumption. MOSFETs operating in subthreshold can be exploited to generate a subthreshold voltage reference. The process of combining PTAT and CTAT voltages as discussed previously still applies. Subthreshold voltage references are not a new idea, and date back to 1979 in [33], which presents a traditional BGR that uses subthreshold MOSFETs to generate its PTAT component.

3.2. Subthreshold Voltage Reference Design

Modern implementations of a subthreshold voltage reference using submicron technologies are presented in [34]-[37]. The designs in [34], [35], and [37] utilize the same PTAT structure presented in [33], while the CTAT voltage is derived using a bandgap. The references in [34] and [37] use the parasitic PNP found in CMOS substrates to obtain a bandgap, while [35] uses a Schottky diode for its bandgap. The reference in [37] consumes 25 μA from the supply, making it unsuitable for this application. The output voltage in [35] and [36] are below 0.3 V, which is not high enough to turn on the transistors they will be biasing. The remaining design in [34] consumes a 20.5 nA, and does not occupy much area. Thus, the subthreshold voltage reference will be based on [34].

3.2.1. Preliminary Transistor Characterization

The design begins with characterizing the BJTs and MOSFETs under the bias conditions in which they will be operated. The simulated transfer characteristic of a CMRF8SF PNP BJT sized W/L = DATA REDACTED is plotted in Figure 3.1. Because V_E and I_E are exponentially related, plotting the curve on a semilog scale results

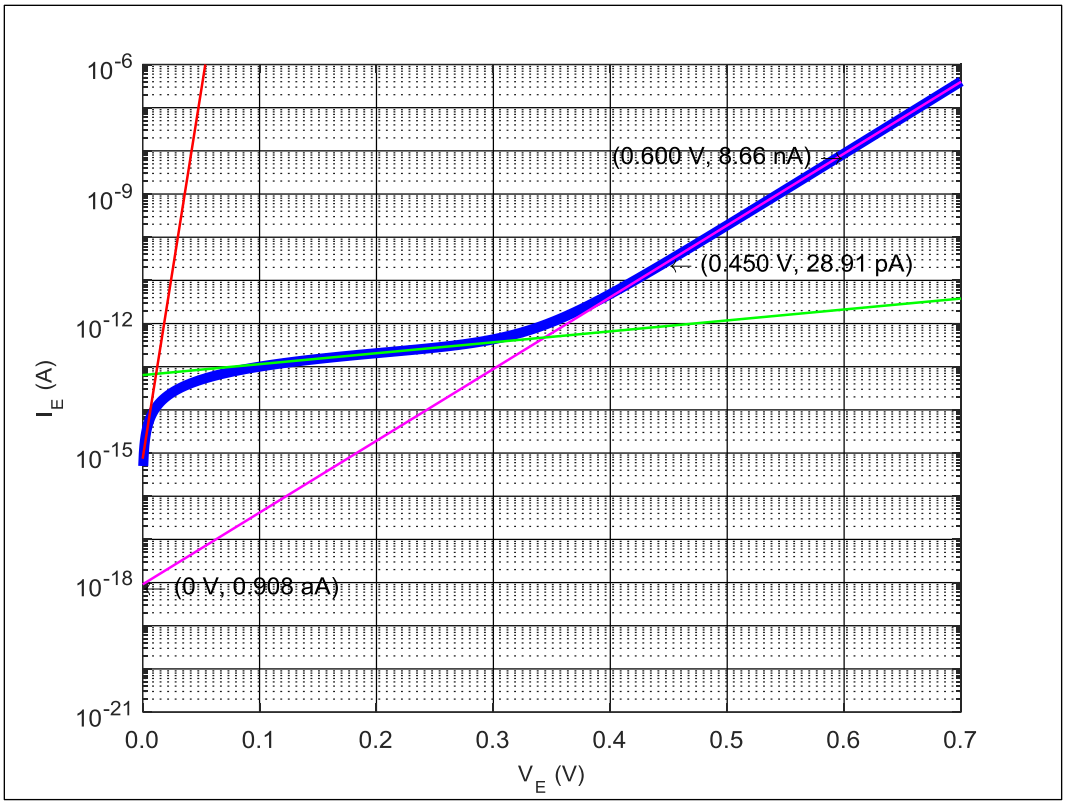

Figure 3.1 - Simulated I_E vs. V_E (blue) for a BJT sized W/L =DATA REDACTED

in a straight line with a constant slope. Notice from the additional red, green, and pink lines that the slope varies for different regions of V_E, corresponding to changes in the exponential behavior of the emitter-base PN junction as the bias voltage increases. The forward biased region where VE ≥ 0.4 V contains the slope of interest as this is the mode where the diode formed by the PN junction generates a voltage V_D that is inherently CTAT. The diode does not exhibit CTAT behavior when it is not forward biased [28].

The emitter current I_E in the forward biased region is given in [34] as:

$$I_E = I_{SE} \exp\left(\frac{V_E}{mV_T}\right) \qquad \textit{(Eq. 3.1)}$$

where V_T is the thermal voltage, m is the slope factor, and I_{SE} is the reverse saturation current for the base-emitter PN junction, which is a dependent on process and sizing. The slope factor is also referred to as the emission coefficient. The thermal voltage V_T is approximately 25.865 mV at room temperature, while V_E and I_E are known input and

output values from the simulation results in Figure 3.1. The remaining unknowns are the slope factor *m* and reverse saturation current I_{SE}, both of which can be found analytically.

To find the slope factor, begin by determining the slope using two points from the region of interest in Figure 3.1 where $V_E \geq 400$ mV:

$$\text{Slope} = \ REDACTED \qquad \textit{(Eq. 3.2)}$$

The BJT slope factor *m* is then found using the following equation from [32]:

$$\frac{1}{\text{Slope}} = 2.3\text{mV}_\text{T} \qquad \textit{(Eq. 3.3)}$$

Solving for slope factor *m* yields a value of REDACTED for $V_E \geq 400$ mV. Next, the reverse saturation current I_{SE} is described in [38] as:

$$\text{I}_\text{SE} = \text{n}_\text{i}{}^2\text{qA}[\frac{\text{D}_\text{p}}{\text{L}_\text{p}\text{N}_\text{D}} + \frac{\text{D}_\text{n}}{\text{L}_\text{n}\text{N}_\text{A}}] \qquad \textit{(Eq. 3.4)}$$

where *q* is the charge in an electron, *A* is the emission coefficient of the junction, D_p and D_n are the diffusion coefficients, L_p and L_n are the carrier lifetimes, N_D and N_A are the donor and acceptor concentrations, respectively, and n_i is the intrinsic semiconductor carrier concentration. Subscripts *p* and *n* refers to holes and electrons, respectively. These parameters are process dependent, and are not provided for the 8RF process to facilitate calculating a numeric value for I_{SE}. From (3.1), it is evident that I_{SE} is equivalent to I_E when V_E is zero. Since (3.1) describes I_E in the forward biased region, it is best to use the point where V_E is zero on the pink line in Figure 3.1 rather than where V_E is zero in the simulation behavior plotted in blue. This corresponds to a value of 0.908 aA for I_{SE}, which completes the characterization of the BJT.

Next, the MOSFET subthreshold characteristics are determined. Since the voltage reference is generated directly from the 3.8 V battery, the design will use thick oxide 3.3 V FETs rated for a maximum voltage 3.6 V across any two terminals of the

FET. The 8RF documentation specifies a nominal 0.380 V turn-on voltage for the 3.3 V FETs. Figure 3.2 shows the drain current I_D is linear for subthreshold voltages ranging from 200 mV to about 400 mV. Notice that V_{DD} induces a small vertical shift on I_D, but has no visible effect on the slope for V_G ranging from 0.2 V to 0.4 V where the MOSFET begins to leave the subthreshold region as it approaches its threshold voltage V_{TN0}.

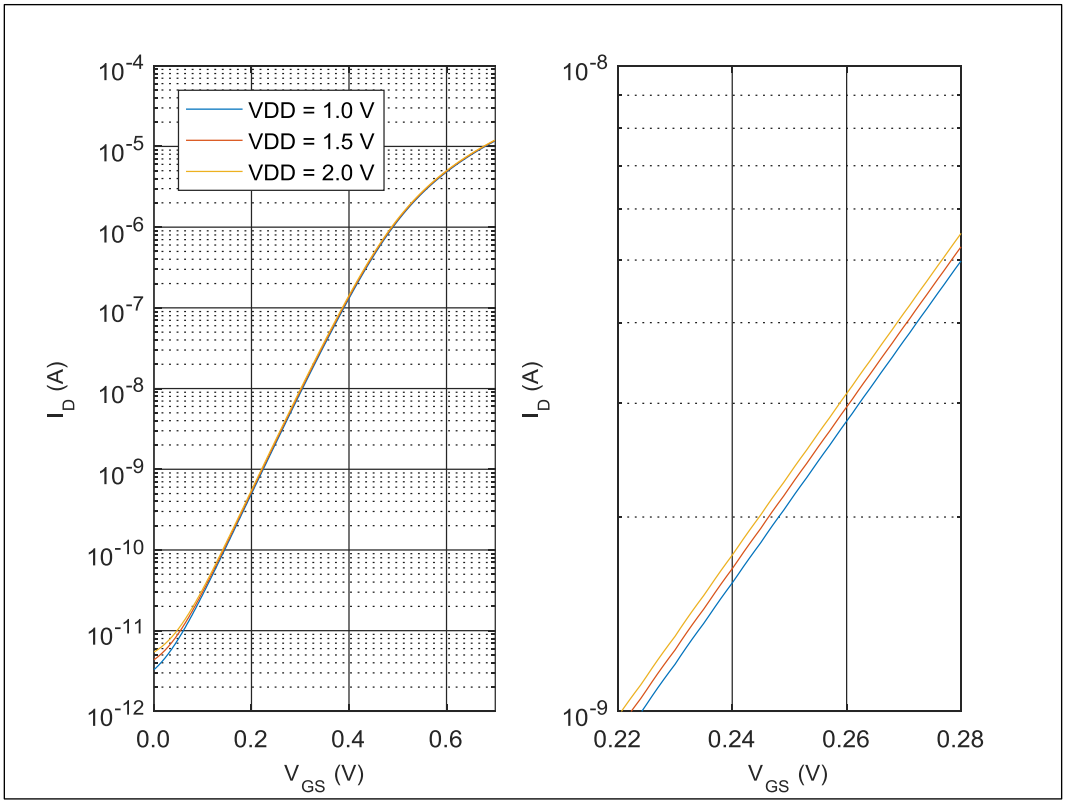

Figure 3.2 - I_D vs. V_{GS} for an NFET sized W/L = REDACTED µm at various V_{DD}.

For a MOSFET operating in the subthreshold region, the advanced compact MOSFET (ACM) model [39] defines drain current I_D according to:

$$I_D = 2eSI_{SQ}\exp\left(\frac{V_G - V_{TN}}{nV_T} - \frac{V_S}{V_T}\right) \qquad \textit{(Eq. 3.5)}$$

where V_{TN} is the threshold voltage, V_T is the thermal voltage, n is the MOSFET slope factor, e is Euler's number 2.71828, I_{SQ} is the sheet normalization current, V_G and V_S are the gate and source voltages measured with respect to the substrate body terminal, and S

is the aspect ratio *W/L* of the transistor. The unknown parameters to be determined are *n* and I_{SQ}.

The subthreshold slope factor *n* can be found using (3.3) which was used to previously determine the BJT slope factor *m*. Using two points from Figure 3.2, the subthreshold slope *S* is:

$$S = REDACTED \qquad (Eq.\ 3.6)$$

Evaluating (3.3) using the calculated slope *S* yields a subthreshold slope factor *n* of REDACTED.

The sheet normalization current I_{SQ} is defined in the ACM model [39] as:

$$I_{SQ} = \frac{\mu C_{ox}'}{2} n V_T^2 \qquad (Eq.\ 3.7)$$

where *n* is the subthreshold slope factor previously found, μ is the effective carrier mobility, V_T is the thermal voltage, and C_{ox}' is the oxide capacitance. Note that the terms $\mu C_{ox}'/2$ simplifies to the transconductance parameter K_N. Characterization of the 3.3 V NFETs in simulation yields a value of REDACTED for K_N. Thus, I_{SQ} evaluates to REDACTED nA.

Table 3.1 - Summary of transistor parameters.

Parameter	Value
BJT Slope Factor *m*	REDACTED
BJT Reverse Saturation Current I_{SE}	REDACTED
MOSFET Slope Factor *n*	REDACTED
MOSFET Sheet Normalization Current I_{SQ}	REDACTED

3.2.2. Voltage Reference Design Process

The subthreshold voltage reference in Figure 3.3 is based on work presented in [34]. As stated previously, the bandgap voltage reference is comprised of three fundamental blocks: a CTAT voltage source, a PTAT voltage source, and some biasing stage. Thus, the output of the voltage reference is:

$$V_{REF} = V_{CTAT} + V_{PTAT} \qquad \textit{(Eq. 3.8)}$$

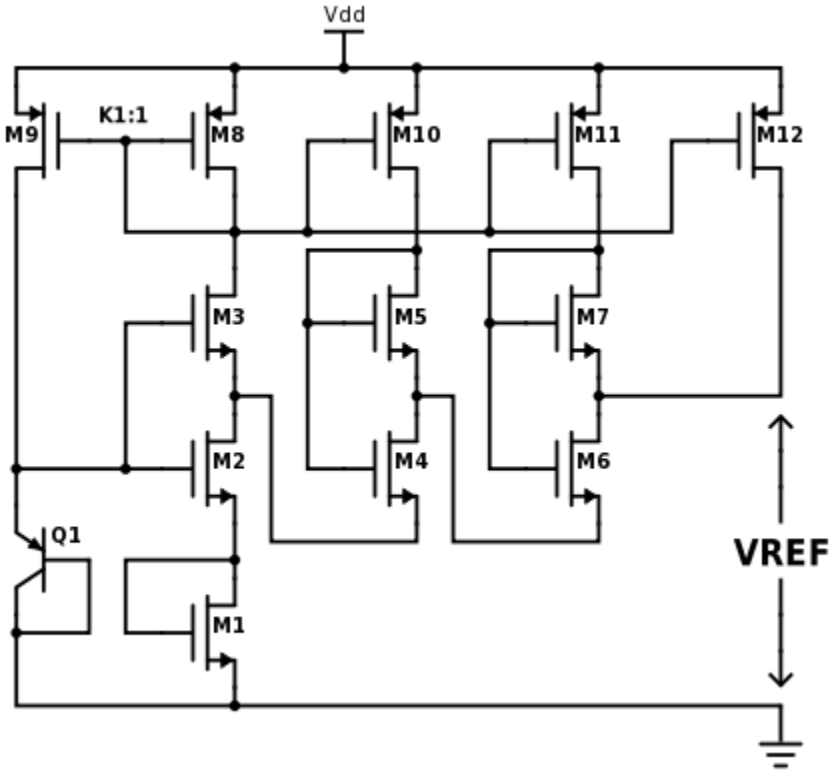

Figure 3.3 - Schematic of the subthreshold voltage reference [34].

In [34], the PTAT voltage is generated from multiple self-cascode MOSFET structures placed in series. The self-cascode MOSFET (SCM) structure originates from the bandgap reference designed in [33]. In Figure 3.4, the first SCM cell is formed from transistors M1 and M2, which are both biased in the subthreshold region by current I_{REF}. Additionally, both are operating in saturation because of the diode-connected upper transistor M2. The lower transistor M1 will have current $2I_{REF}$ entering its drain. Additional SCM cells are formed using transistor pairs M3-M4, and M5-M6. Each subsequent cell placed in series will have an additional I_{REF} entering the drain of the lower transistor. The lower transistor in the final stage will have a drain current of $(N+1)I_{REF}$, where N is the number of SCM cells. The resulting PTAT voltage is the sum of the drain-source voltages across the lower transistor of each SCM cell [33].

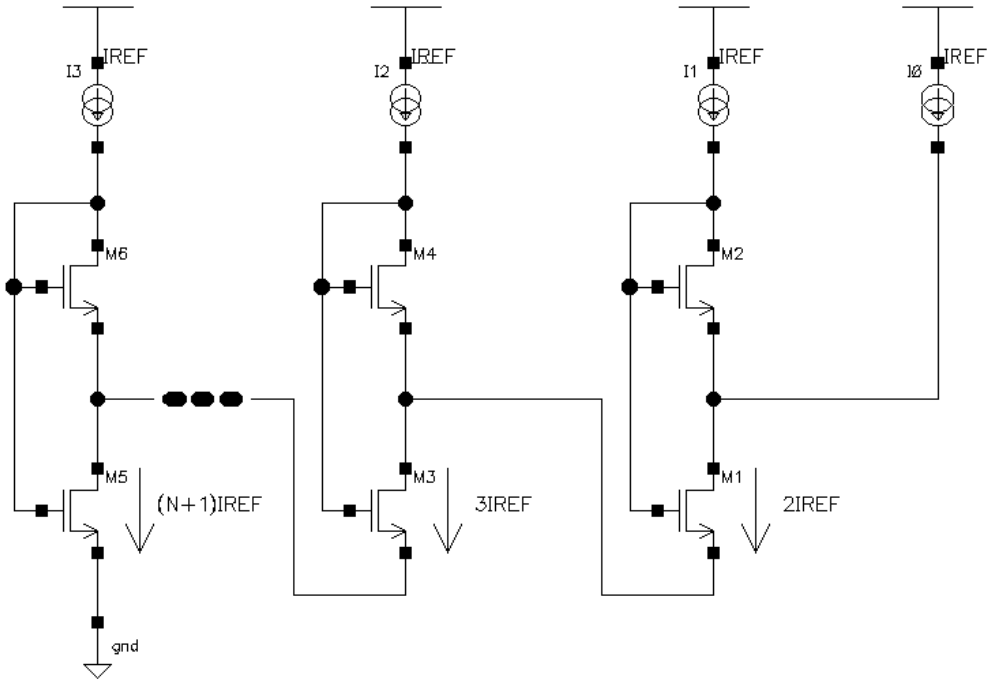

Figure 3.4 - Self-cascode MOSFET structure from [33].

The topology in Figure 3.3 uses three SCM stages formed by transistor pairs M6-M7, M4-M5, and M2-M3. Note that transistor pairs M2-M3 are not diode-connected via the upper transistor. Instead, they will be put into saturation by the current mirror as a part of the biasing for the CTAT voltage. For the three SCM cells, the PTAT voltage is:

$$V_{PTAT} = V_{DS2} + V_{DS4} + V_{DS6} \qquad \textit{(Eq. 3.9)}$$

From [34], the drain-source voltage across the lower transistor in each SCM cell is:

$$V_{DS(LOW)} = nV_T \ln\left(\frac{I_{LOW}}{I_{HIGH}}\frac{S_{HIGH}}{S_{LOW}}\right) = nV_T \ln\left(\frac{I_{LOW}}{I_{HIGH}}\frac{(W/L)_{HIGH}}{(W/L)_{LOW}}\right) \qquad \textit{(Eq. 3.10)}$$

where *n* is the subthreshold slope factor, *VT* is the thermal voltage, and *S* is the aspect ratio of the transistor width and length *W/L*. To simplify the design, all transistors are sized such that the length of the upper and lower transistors of each cell is equal at *L* = REDACTED. The drain-source voltage in (3.10) then simplifies to:

$$V_{DS(LOW)} = nV_T \ln\left(\frac{I_{LOW}}{I_{HIGH}}\frac{W_{HIGH}}{W_{LOW}}\right) \qquad \textit{(Eq. 3.11)}$$

Substituting (3.11) into (3.9) for each lower transistor yields:

$$V_{PTAT} = nV_T \ln\left(\frac{I_{D(M2)}}{I_{D(M3)}}\frac{I_{D(M4)}}{I_{D(M5)}}\frac{I_{D(M6)}}{I_{D(M7)}}\frac{W_{M3}}{W_{M2}}\frac{W_{M5}}{W_{M4}}\frac{W_{M7}}{W_{M6}}\right) \qquad \textit{(Eq. 3.12)}$$

From Figure 3.3, it can be seen that $I_{D(M6)} = 2I_{REF}$, $I_{D(M4)} = 3I_{REF}$, and $I_{D(M2)} = 4_{IREF}$; the current in the upper transistors M3, M5, and M7 is I_{REF}. Therefore, the PTAT voltage simplifies to the final form of:

$$V_{PTAT} = nV_T \ln\left(24\frac{W_{T3}}{W_{T2}}\frac{W_{T5}}{W_{T4}}\frac{W_{T7}}{W_{T6}}\right) \qquad \textit{(Eq. 3.13)}$$

Continuing onto the CTAT voltage and the biasing for the PTAT cells, implementation of the current mirror biasing and the CTAT voltage is centered on bipolar transistor Q1 as the primary element [34]. The junction voltage V_{EB} is used to generate a CTAT voltage that is extracted using the stacked transistors M1 and M2 in Figure 3.3. If the two are sized with the same aspect ratio, and the source-bulk voltage V_{SB} of both transistors is zero, then both transistors will have equal gate-source voltages V_{GS}. The resulting CTAT voltage from [34] is:

$$V_{CTAT} = V_{GS1} = \frac{V_{EB}}{2} \qquad \textit{(Eq. 3.14)}$$

However, this requires a triple-well process where each NFET transistor can be isolated within its own individual n-well to achieve a V_{SB} of zero such that both NFETs have the same the threshold voltage V_{TN}. IBM's 8SF 180 nm process is a dual-well process where all NFET transistors share a common well. Thus, only NFET transistors with the source terminal tied to ground will have zero V_{SB}. All other NFETs will have a source voltage $V_{SB} > 0$ V, and be subject to the body effect which increases the threshold voltage V_{TN}. As a result, the junction voltage V_{EB} will not be divided evenly across M1 and M2. The CTAT voltage will instead be:

$$V_{CTAT} = V_{GS1} \approx \frac{V_E}{n+1} \qquad \textit{(Eq. 3.15)}$$

The emitter current I_E of Q1 was defined in (3.1), and the drain current I_D of M1 was defined in (3.5). Since M1 has its source and body terminals tied together such that $V_{SB} = 0$ V, (3.5) simplifies to:

$$I_D = 2eSI_{SQ}\exp\left(\frac{V_G - V_{TN}}{nV_T}\right) \qquad \textit{(Eq. 3.16)}$$

The current used to bias the PTAT cells is generated using a current mirror formed by Q1, M8, M9, and M1-M3. The current in M9 is equal to the emitter current, and is related to the reference current I_{REF} in M8 by gain K_1, which is set according to the aspect ratios of PFETs M8 and M9.

$$I_E = I_{D(M9)} = K_1 I_{D(M8)} \qquad \textit{(Eq. 3.17)}$$

Knowing that $4I_{D(M8)} = I_{D(T1)}$, the emitter current can be related to the drain current of NFET M1 so (3.17) can be rewritten:

$$I_E = K_1 \frac{I_{D(M1)}}{4} \qquad \textit{(Eq. 3.18)}$$

Substituting (3.1), (3.15), and (3.16) into (3.18) and solving for V_E will eventually yield:

$$V_E = \frac{V_T}{\frac{1}{m} - \frac{1}{2n}}\left[\ln\left(2eS\frac{K_1}{4}\frac{I_{SQ}}{I_{SE}}\right) - \frac{V_{TN}}{nV_T}\right] \qquad \textit{(Eq. 3.19)}$$

The output of the voltage reference in (3.8) can finally be rewritten as:

$$V_{REF} = \frac{V_E}{n+1} + nV_T\ln\left(24\frac{W_{M3}}{W_{M2}}\frac{W_{M5}}{W_{M4}}\frac{W_{M7}}{W_{M6}}\right) \qquad \textit{(Eq. 3.20)}$$

where V_E is the emitter voltage defined in (3.19), n is the subthreshold slope factor, and V_T is the thermal voltage.

To begin the design, an emitter voltage V_E is chosen such that V_{GS1} as defined in (3.15) falls into the subthreshold region plotted in Figure 3.2. Additionally, the emitter current will be divided down by K_1 to generate I_{REF} to bias the SCM cells. According to [33], this bias current should also be at subthreshold levels, but should still be sufficiently

high enough to minimize the error from leakage currents. The design proceeds by setting V_E equal to 0.75 V. The authors in [34] set K_1 equal to 6, but advises that K_1 should be greater for processes without access to triple-well FETs. The effect of a nonzero V_{SB} on the stacked transistors M1 and M2 has already been discussed in developing (3.15), but it also effects the SCM cells. Because V_{TN} increases for NFETs with greater V_{SB}, the effective drain current decreases in SCM cells higher up in the stack. Increasing the current mirror gain K_1 compensates for this effect. Thus, K_1 is set to 15.

Solving for the aspect ratio S_1 using (3.19) with V_E and K_1 set to 0.75 V and 15, respectively, yields a ratio of 0.603 for S_1. For convenient sizing, this is rounded up to an integer value of 1. Since the PTAT cells already have their lengths chosen as REDACTED in deriving (3.13), this same length is used for M1. Thus, M1 and M2 are sized with REDACTED width and length. Re-evaluating (3.19) with the chosen aspect ratio yields 0.771 V for V_E.

In sizing transistors M2-M7 in the PTAT SCM cells, the aspect ratio of the upper transistor must be greater than the aspect ratio of the lower transistor to guarantee that the lower transistor operates in saturation [33]-[37]. As stated previously in deriving (3.13), all transistors in the PTAT cells are sized with REDACTED lengths. Transistor M2 has already been sized with a length and width of REDACTED to attain the desired V_E. The ratio S_3/S_2 is chosen to be 5, resulting in a width of REDACTED for M3. The remaining SCM pairs M4-M5 and M6-M7 are sized with a larger ratio of REDACTED because of the nonzero V_{SB} that increases V_{TN}. Thus, M5 and M7 have a width of REDACTED.

Table 3.2 - Voltage reference transistor sizing in µm

	Q1	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12
W	REDACTED												
L													

The sizing of all transistors is summarized in Table 3.2. The expected output of the voltage reference is determined by evaluating (3.20) with the chosen parameters:

$$V_{REF} = \text{REDACTED} = 684\ \text{mV} \qquad \textit{(Eq. 3.21)}$$

3.2.3. Voltage Reference Simulation Results

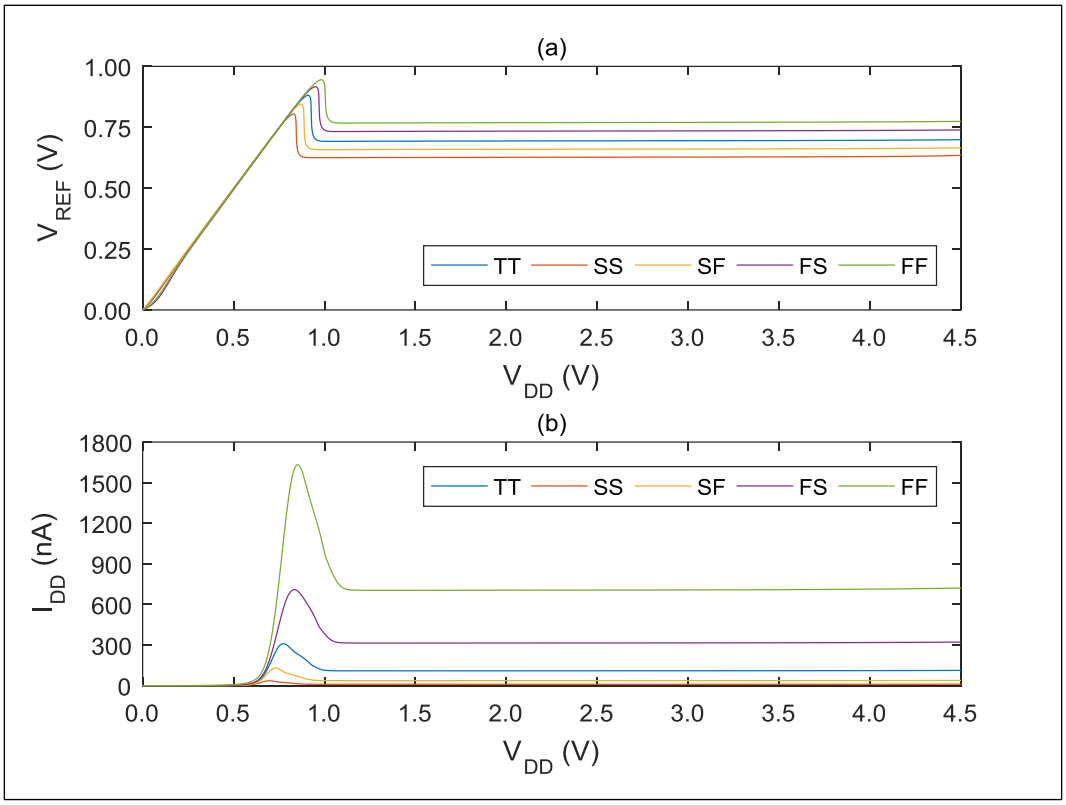

Figure 3.5 - V_{REF} (a) and I_{DD} (b) vs. V_{DD} from 0-4.5 V

Figure 3.5 shows the simulated output voltage and current consumption across all performance corners for supply voltages up to 4.5 V. At the worst performance corner, the reference is operational down to a supply of 1.1 V. Below this point, there is insufficient headroom to drive the full stack of SCM cells. Because of this, the feedback loop formed by the current mirror increases the current in M1-M3, resulting in a higher steady state current [34]. The minimum operating point is not a concern since the lowest supply voltage is 3 V. Figure 3.6 plots the performance across the expected operating

range of the battery. For the nominal TT corner, the voltage reference consumes 110.58 nA, and outputs 696 mV at the nominal 3.8 V battery voltage, 1.8% higher than the value calculated in (3.21). Table 3.3 summarizes the DC operating points for all corners at 3.8 V.

Table 3.3 - Voltage reference DC operating point at V_{DD} = 3.8 V across corners

Corner	Voltage (mV)	Current (nA)
TT	REDACTED	
FF		
FS		
SS		
SF		

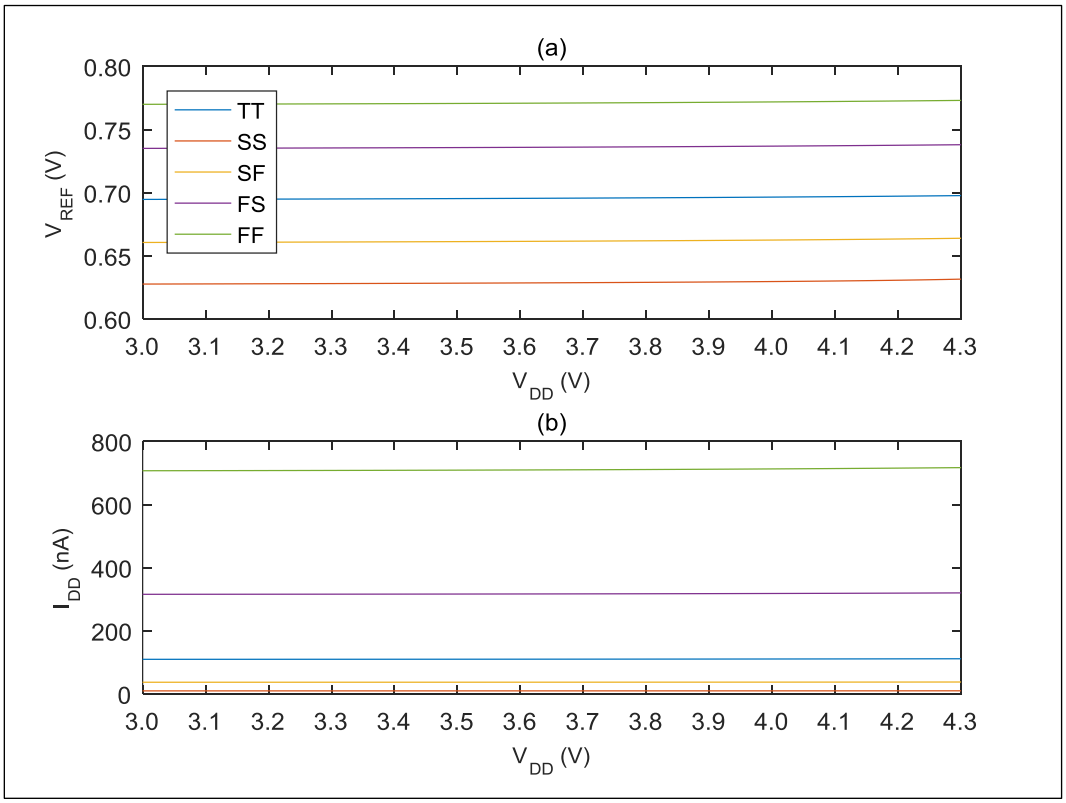

Figure 3.6 - V_{REF} (a) and I_{DD} (b) vs. V_{DD} from 3-4.3 V

Using Figure 3.6, the line regulation is determined using the following equation:

$$\text{Line Regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \qquad \textit{(Eq. 3.22)}$$

At the nominal TT corner, the voltage reference has a good line regulation of REDACTED across the operating range of the battery from 3 V to 4.3 V. Similarly, the current sensitivity is determined in the same manner and evaluates to REDACTED. The voltage line regulation is fairly constant across all performance corners. At the FF corner, the regulation evaluates to REDACTED and REDACTED, while the SS corner evaluates to REDACTED and REDACTED.

The temperature sensitivity of the voltage reference is plotted in Figure 3.7. It is evident that the voltage reference does not exhibit high sensitivity to temperature variations. This confirms that the PTAT and CTAT voltages behave as expected. For the nominal TT corner, the temperature sensitivity is REDACTED. The temperature sensitivity is more commonly presented in datasheets as an effective temperature coefficient which is expressed in units of ppm/°C. From [34], the effective temperature coefficient is given by:

$$\mathrm{TC_{eff}} = \frac{\mathrm{V_{REFmax}} - \mathrm{V_{REFmin}}}{(\mathrm{T_{max}} - \mathrm{T_{min}})\mathrm{V_{REF(27°C)}}} \qquad \textit{(Eq. 3.23)}$$

At the nominal TT corner, the effective temperature coefficient from 0 °C to 60 °C is an acceptable REDACTED. For the extreme FF and SS corners, this degrades to REDACTED and REDACTED, respectively. Equivalently, this is a temperature sensitivity of REDACTED and REDACTED, respectively.

Figure 3.8 shows the PSRR of the reference with a 211 fF output capacitor for all corners at 27 °C and 40 °C. The temperature has a minuscule effect on PSRR, with a difference of less than 0.5 dB. The figure is presented as a scalable vector graphic (SVG) generated via MATLAB, making it possible to zoom in on extremely fine details in the image without losing any quality. Nonetheless, Figure 3.9 has been included to show the PSRR from 10 kHz to 1 MHz on a smaller scale. At the nominal TT corner, the voltage reference exhibits a good rejection of supply noise with a PSRR of -59 dB of at DC,

peaks at -20.6 dB at 150 kHz, and settles at -48 dB at high frequencies beyond 10 MHz. If desired, the PSRR can be improved by placing bypass capacitors at the output of the reference, or using a cascode current mirror in place of the simple current mirror.

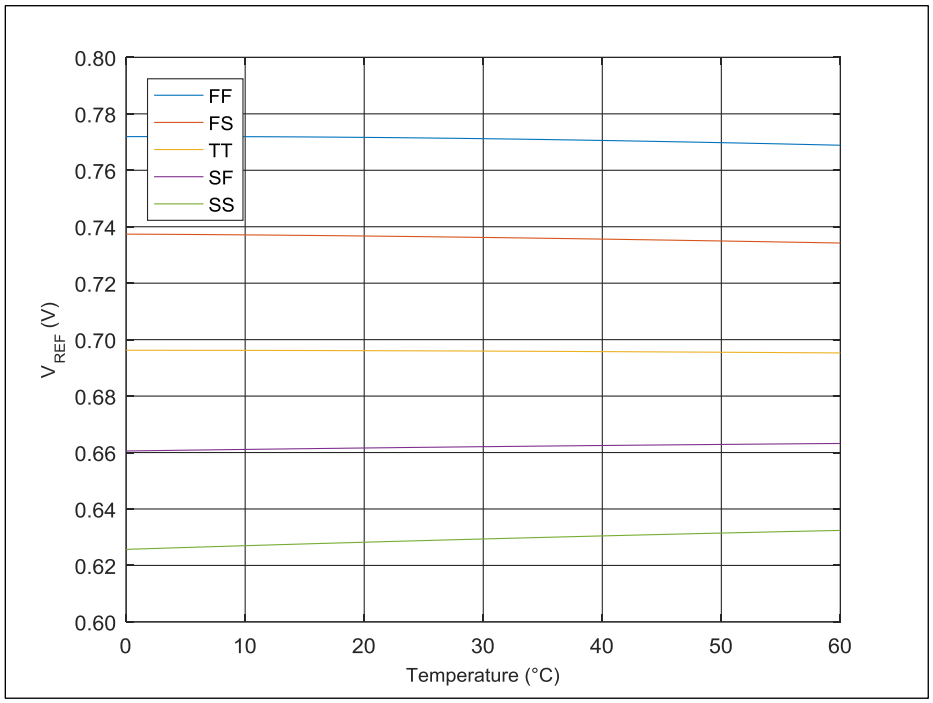

Figure 3.7 - V_{REF} vs. temperature for all process corners at V_{DD} = 3.8 V

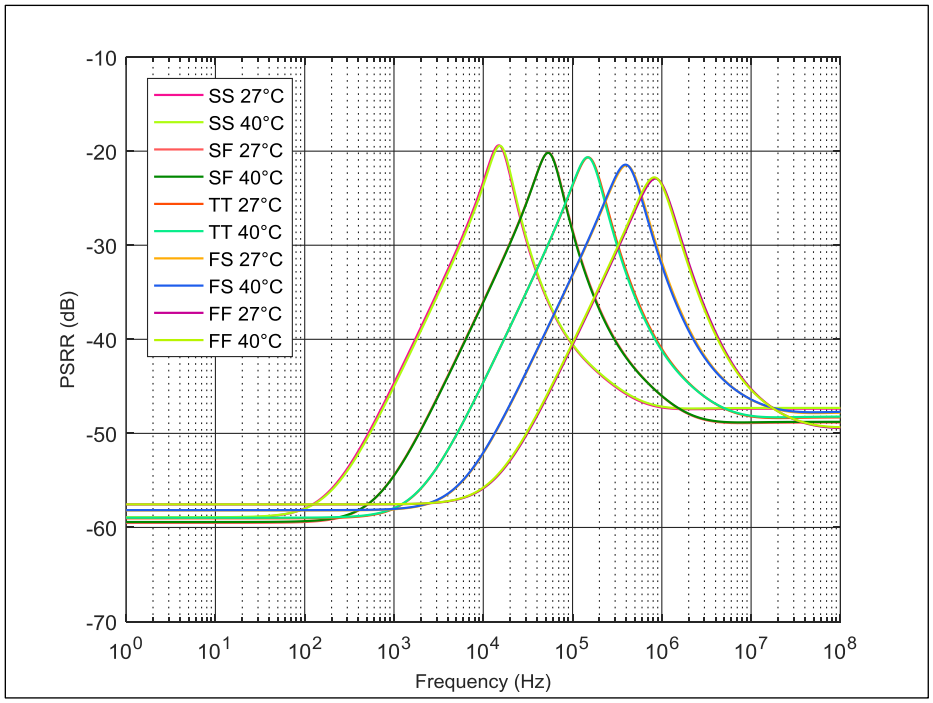

Figure 3.8 - Voltage reference PSRR vs. frequency

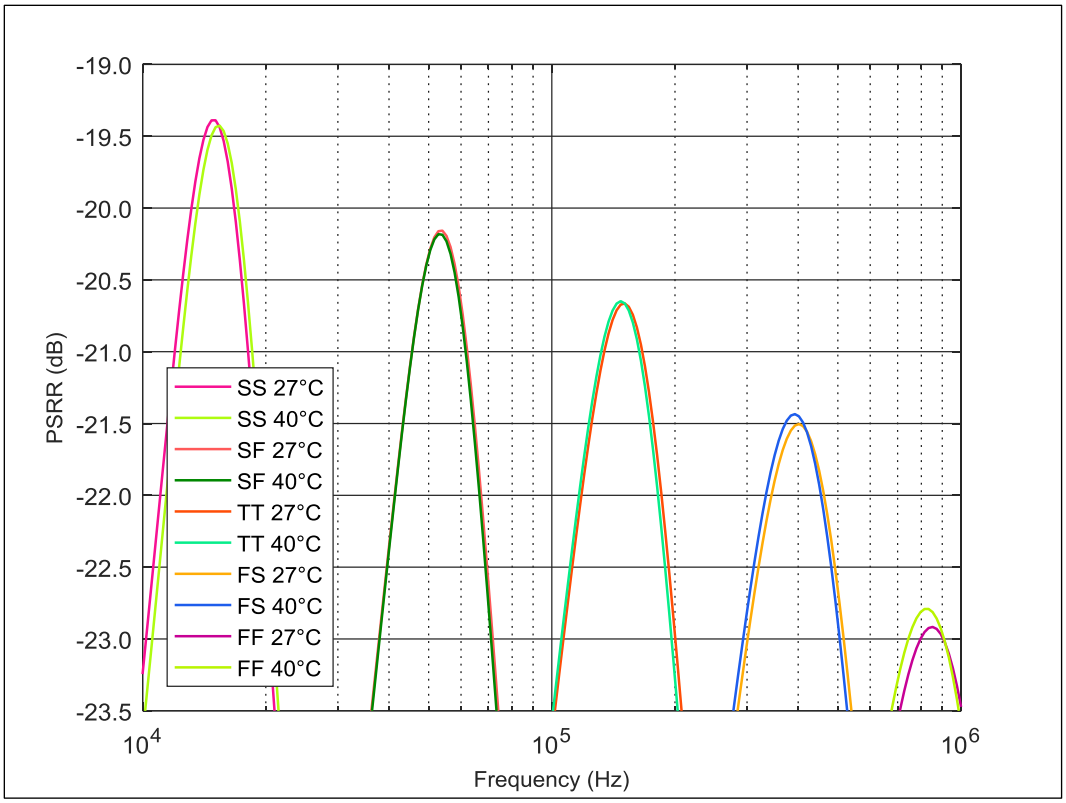

Figure 3.9 - Voltage reference PSRR vs. frequency from 10 kHz to 1 MHz

Startup behavior of the circuit is plotted in Figure 3.10. Leakage currents are sufficient for starting the circuit [34]. The reference settles to its steady state operating point within 25 µs without the inclusion of any startup circuitry. A faster startup can be achieved with the addition of a startup circuit, but is not necessary for this particular application.

Turning the discussion back to process variations, the corner performance results in Figure 3.5 and Table 3.3 make the assumption that all transistors are equally varied in the same manner. For example, the FS corner assumes that all PFETs are faster than normal, and all NFETs are slower than normal. The models at the corners do not account for mismatches where the parameters of each individual transistor is varied randomly. This analysis can only be done through Monte Carlo simulations. Figure 3.11 shows the distribution for 2000 runs of Monte Carlo simulation. The results have a mean μ of

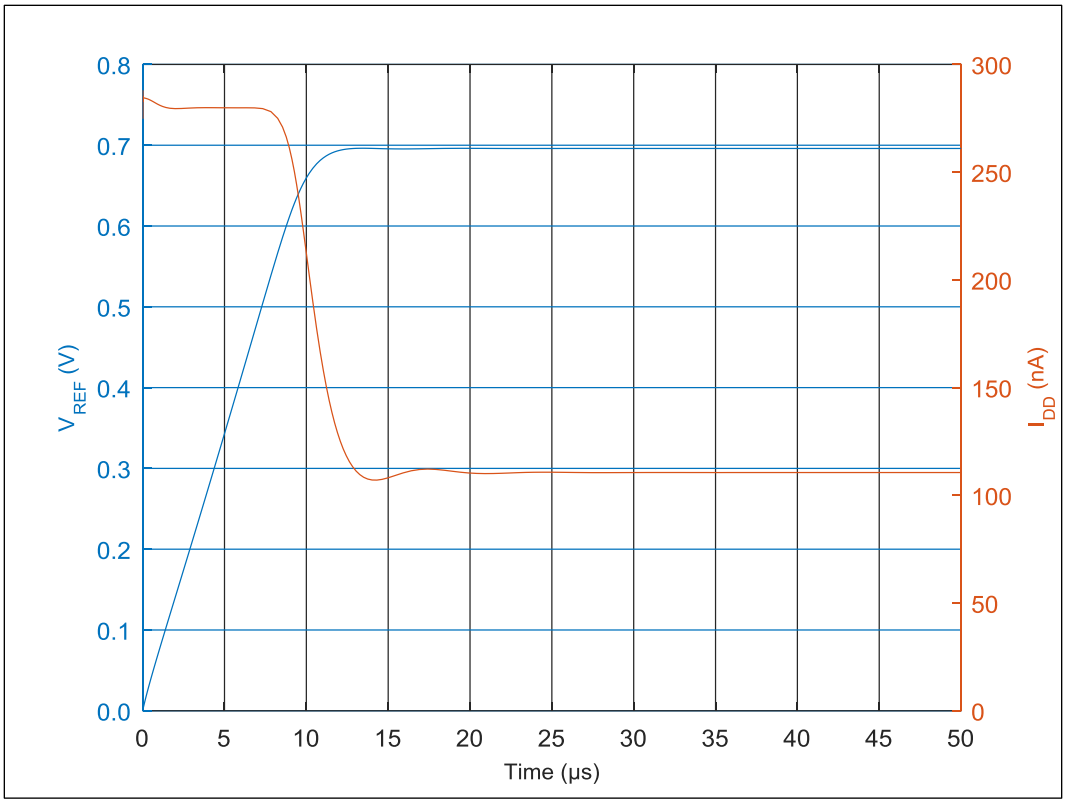

Figure 3.10 - Voltage reference startup waveforms

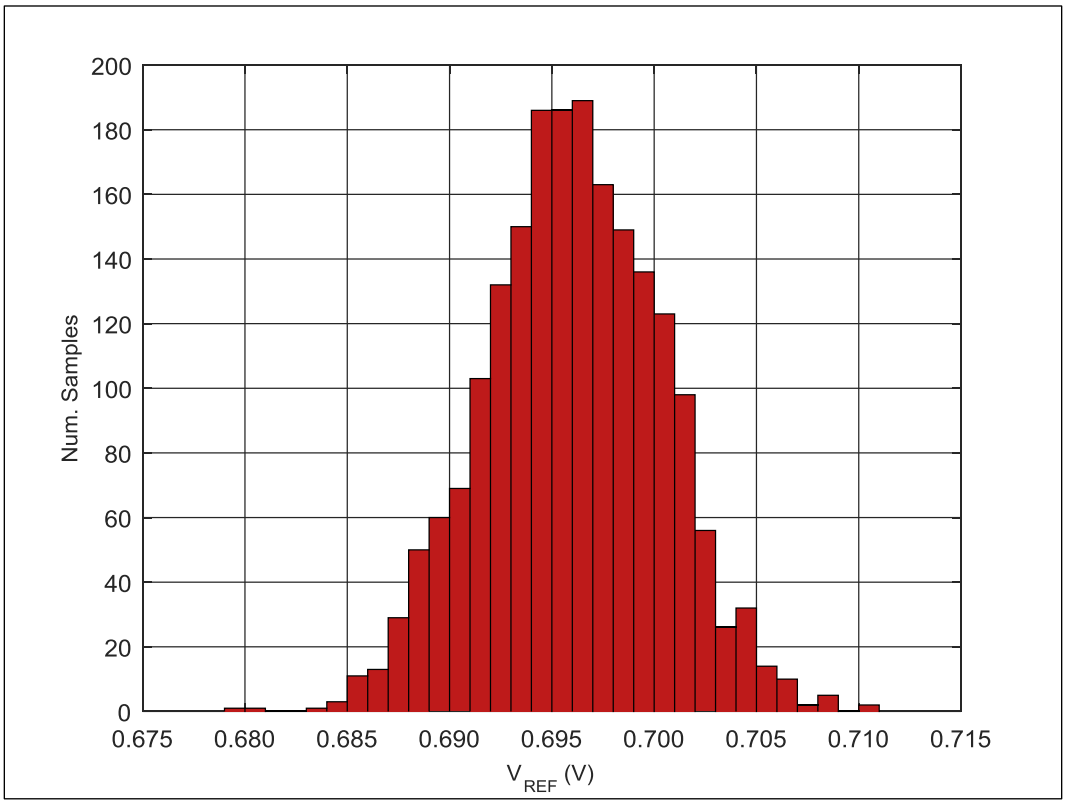

Figure 3.11 - Histogram of 2000 Monte Carlo iterations of transistor mismatches

696 mV, and a standard deviation σ of 4.27 mV. The coefficient of variation σ/μ is 0.61%. It can be concluded that random transistor mismatches do not affect functionality of the voltage reference.

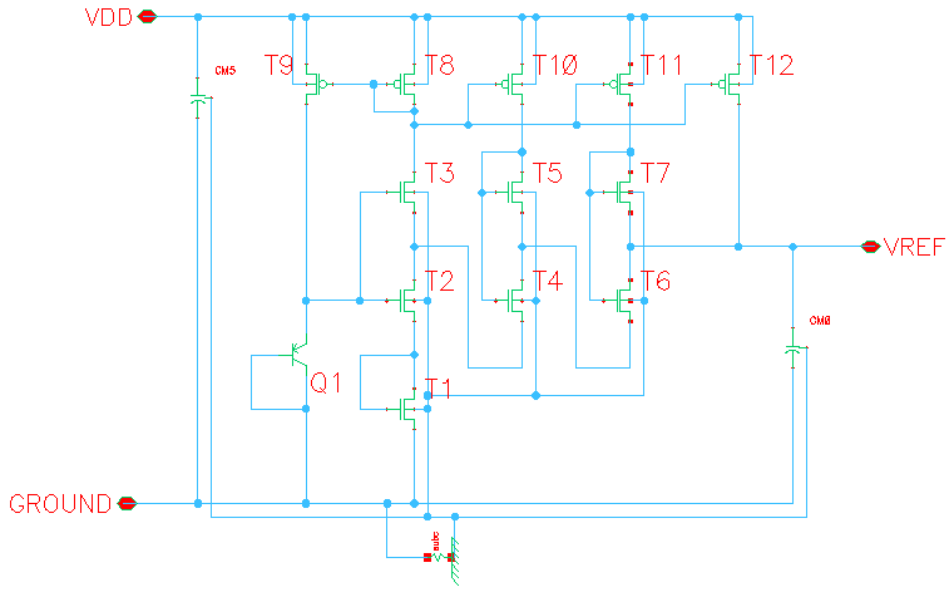

Figure 3.12 - Full schematic of the subthreshold voltage reference

3.3. Voltage Regulator

Because the battery voltage decreases over time, it is necessary to regulate it to a stable power supply voltage. Unlike references, a regulator is capable of supplying steady state currents to the load. For this project, a linear regulator provides a convenient means to do so. DC-DC switching converters are an alternative method for creating a source voltage, but requires the use of an inductor as an energy storage element. Integrating this within a chip consumes significant area to generate a usable inductance, and is not appropriate for this application.

3.3.1. Background on Linear Regulators

A linear regulator consists of a feedback network that drives a pass element connecting the unregulated supply V_{DD} to the regulated output supply V_{OUT} [28]. The

pass element, also called a power transistor, is either an NFET or PFET transistor whose conductance is regulated by the feedback loop. The feedback network is composed of an error amplifier, a voltage reference, and a divider network for comparing the output to the

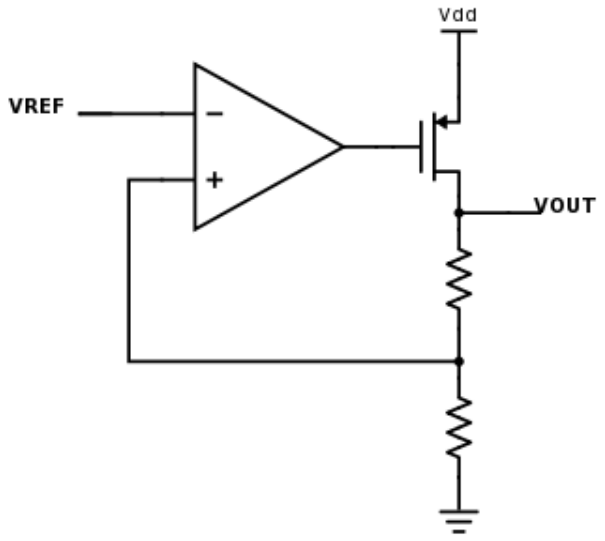

Figure 3.13 - Linear regulator with PFET pass element.

reference [28]. The output of the regulator is set by the feedback according to:

$$V_{OUT} = V_{REF}(1 + \frac{R_2}{R_1}) \qquad \textit{(Eq. 3.24)}$$

The maximum theoretically efficiency of the linear regulator is:

$$Efficiency = \frac{V_{out}}{V_{in}} \times 100\% \qquad \textit{(Eq. 3.25)}$$

The primary drawback of a linear regulator is that efficiency is low if V_{out} is not close to V_{in}. In larger systems, it is possible to overcome this shortcoming using a switching regulator to step the supply voltage down to a level closer to the desired Vout prior to passing it through the linear regulator. For example, if one is working with an unregulated 12 V power source that needs to power devices rated for 3 V, a high efficiency buck converter can be used to step the 12 V source down to 5 V, which is then linearly regulated down to 3 V. This is a common method for removing the switching noise inherent to a DC-DC converter.

3.3.2. Linear Regulator Design Process

Normally, it is necessary to implement complex amplifier topologies to attain the DC gain needed to regulate the output. Because this application uses small load currents, it is feasible to create a linear regulator using a single stage amplifier. The design begins with a basic single output, differential pair amplifier shown in Figure 3.14.

The linear regulator is designed to output 1V as this is the supply voltage from which the oscillator in chapter 4 is designed to operate. All transistors are the same 3.3 V FETs previously used in designing the voltage reference. All widths are sized at REDACTED. Transistors M1-M4 are sized with a length of REDACTED. The tail transistor M5 operates in saturation and is biased using the 0.696 mV voltage reference. To reduce current consumed, M5 is sized with a long length of REDACTED. Using the standard equation for a MOSFET in saturation and neglecting the effects of channel length modulation, the

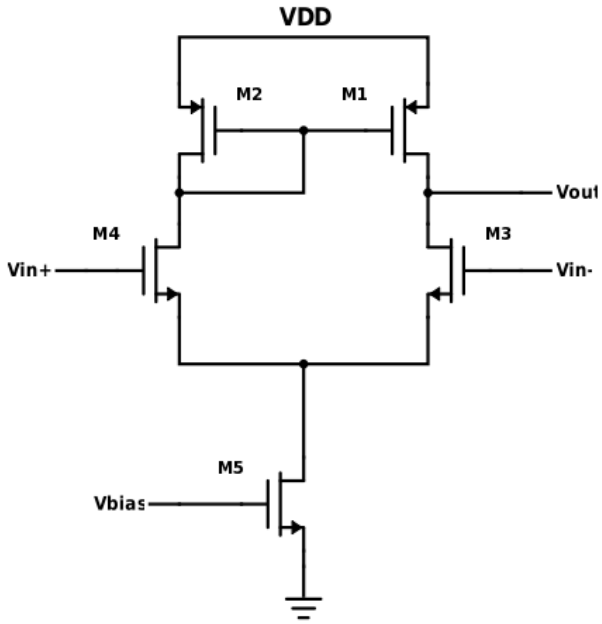

Figure 3.14 - Basic differential pair amplifier.

expected current is 314 nA. The output pass element is a PFET sized *W/L* = REDACTED. Because large resistors consume significant area, the feedback loop is

formed using diode-connected PFETs instead. Lastly, a large 5 pF capacitor is placed at the output to handle high frequency load transients for the oscillator designed in chapter 4.

Consideration is also given to the possibility of in-rush current from the source during startup. The oscillator circuit that loads the regulator is designed using 1.2 V transistors rated for a maximum of 1.6 V. During startup, in-rush current may cause the output of the regulator to momentarily overshoot to unsafe levels. When powered by the thin film battery, voltage overshoot is unlikely given that the maximum output current of the battery is limited by its chemistry as discussed in section 2.1.1. The load also will shunt some of the current as the regulator starts up, further mitigating the effects of any in-rush current from the battery. However, during testing, the IC will be powered by a bench power supply capable of sourcing much more current. Most power supplies cannot set a current limit below 1 mA, which far exceeds the microamp levels that the regulator expects. A current limiter circuit can be implemented externally, but this leaves the potential for human error whenever the test environment needs to be modified. To protect the transistors downstream from the regulator's output, a diode stack is placed at the output of the regulator to clamp any potential overshoot. Additionally, an 18 kΩ resistor is included at the input to further dampen the effects of in-rush current.

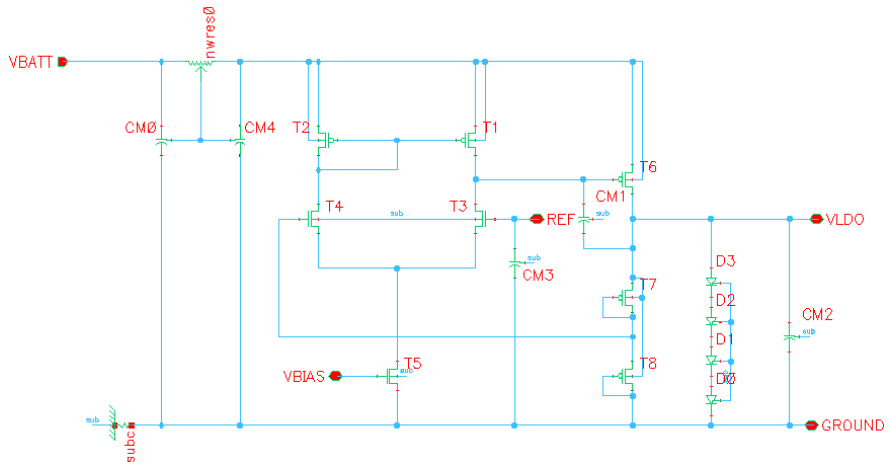

Figure 3.15 - Full schematic of the 1 V linear regulator

Figure 3.15 shows the completed schematic of the 1 V linear regulator, including all input and output capacitors. The sizing for all devices is tabulated in Table 3.4.

Table 3.4 - Component sizing for the linear regulator

Component	Width (µm)	Length (µm)	Multiplicity	Bars	Value
T1	REDACTED				
T2					
T3					
T4					
T5					
T6					
T7					
T8					
D0					
D1					
D2					
D3					
CM0					
CM1					
CM2					
CM3					
CM4					
NWRES0					

3.3.3. Linear Regulator Simulation Results

Figure 3.16 shows the startup waveform for an instantaneous 3.8 V input. As discussed previously, the output overshoots the desired 1 V, but is clamped to 1.48 V by the diode stack. The regulator stabilizes to a steady state value within 9 µs. At the nominal TT corner, regulation is maintained for supply voltages down to 1.05 V at which point the regulator begins to drop out. At the nominal 3.8 V battery voltage, the linear regulator outputs 1.006 V and consumes 0.914 µA. The regulation for all corners is

Table 3.5 - Linear regulator DC operating point at V_{DD} = 3.8 V across corners

Corner	Voltage (V)	Current (µA)
TT	REDACTED	
FF		
FS		
SF		
SS		

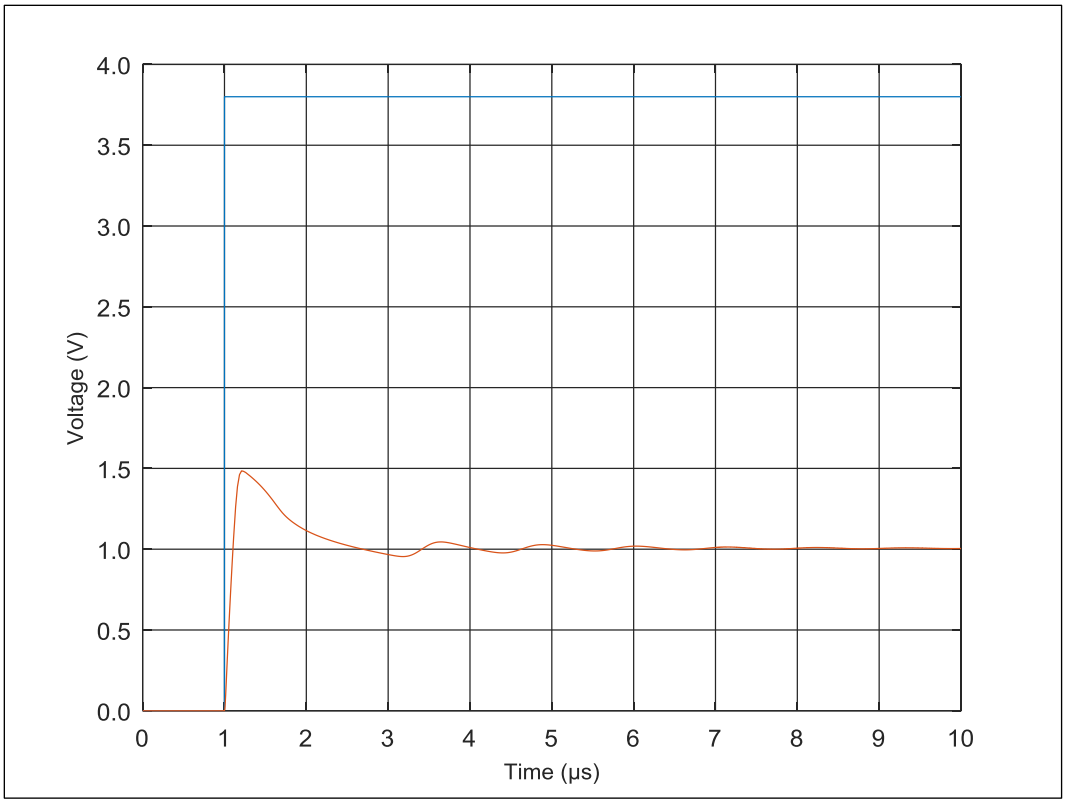

Figure 3.16 - Linear regulator startup waveform

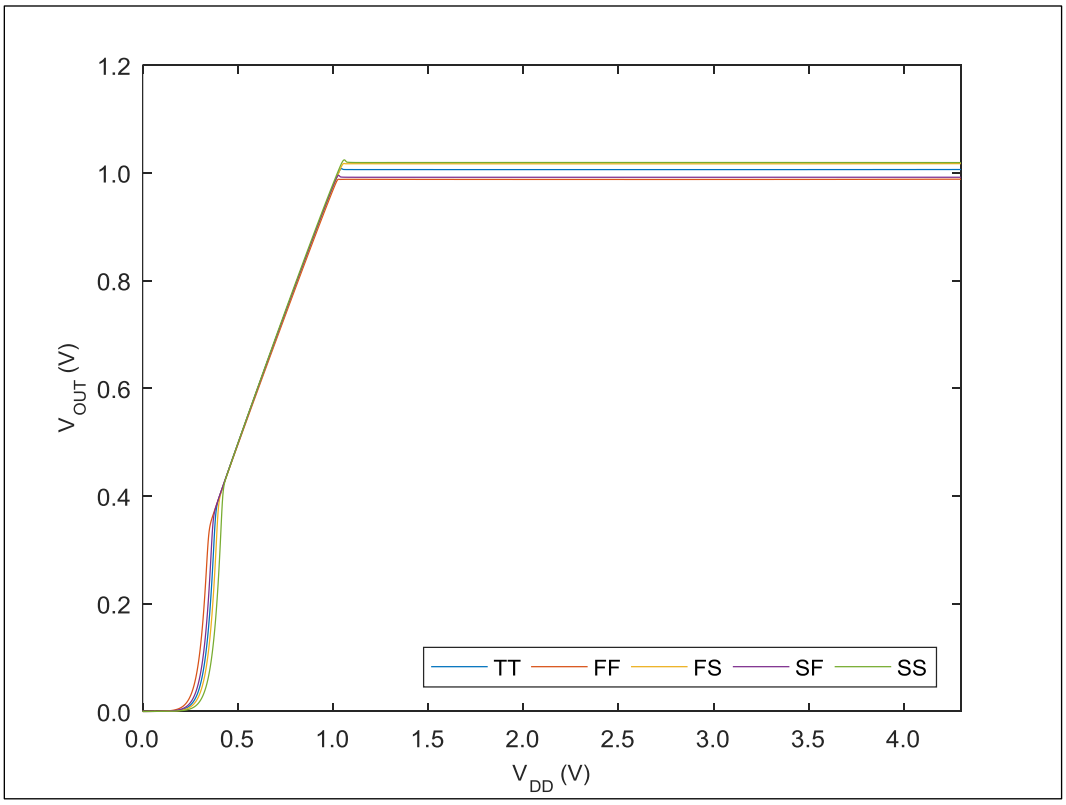

Figure 3.17 - DC operating point of the linear regulator

plotted in Figure 3.17, and the DC operating points for all corners is tabulated in Table 3.5.

The simulation results in Figure 3.17 and Table 3.5 assumes the bias on the tail transistor M5 is a constant 696 mV across all corners. This will not be the case since the bias is derived from the voltage reference, which varies from 629 to 771 mV across corners. Nonetheless, it turns out this variation has no effect on the steady state output of the regulator. Simulation using the subthreshold voltage reference as a bias source results in the same data in Table 3.5. It does, however, affect the drop out point of the regulator at some corners. Comparing Figure 3.5 to Figure 3.17, the drop out point of the reference is higher than the drop out point of the regulator at some corners and, subsequently, causes the regulator to drop out sooner as shown in Figure 3.18. Because the regulator only works when a valid bias is on the tail transistor, its drop out point is now limited by the reference. Since the lowest battery voltage is 3 V, this does not pose any real issue.

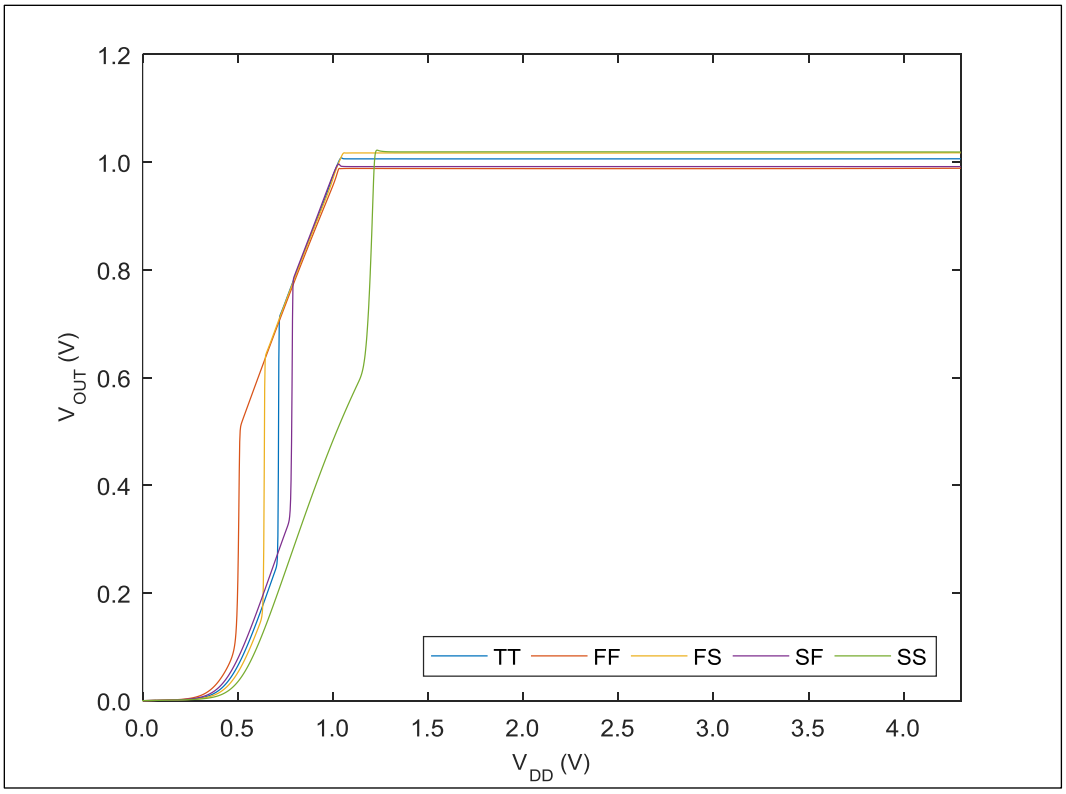

Figure 3.18 - DC operating point of the linear regulator with sub-V_T reference bias

CHAPTER 4: WIRELESS COMMUNICATION

4.1. RF Communication Link

It is expected that the active contact lens will transmit sensor information to an external monitoring device, such as the user's cell phone or some custom PCB with a microcontroller. Wireless communication usually requires a dedicated RF front-end consisting of filters, mixers, oscillators, and amplifiers, all of which require significant power. Given that the battery current is limited to a maximum of 10 μA, this precludes the usage of any high power RF front-end components. To meet the low power requirements, it is proposed that the contact lens communicate using RF backscatter.

4.1.1. Background on RF Backscattering

Figure 4.1 shows the implementation of a backscatter radio link. An external device transmits a 2.4 GHz carrier signal directed towards the antenna on the contact lens. By connecting the lens' antenna to a transistor switch, the reflection coefficient of the antenna can be modulated with a signal at a subcarrier frequency. Because of the change in the antenna's impedance, power from the carrier is reflected back upon itself, creating a backscattered, amplitude modulated signal [40]. This reflected waveform has an AM envelope at the subcarrier frequency of the modulator which can then be extracted using an envelope detector. Thus, a backscatter radio link transmits data by scavenging RF power from the incident carrier without any active RF components [40][41].

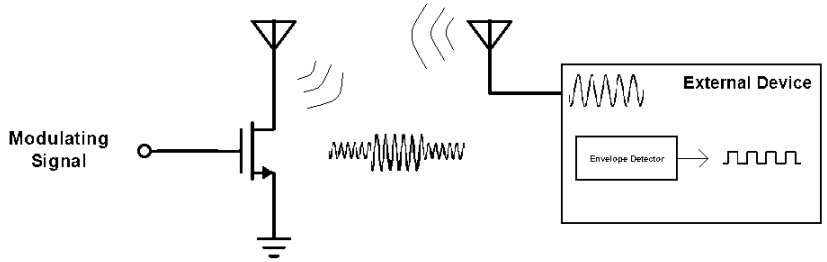

Figure 4.1 - System level block diagram of backscatter communication

4.1.2. Backscatter Prototype and Characterization

Before beginning a modulator design at the transistor level, the performance of a backscatter radio link is first characterized with a prototype utilizing discrete components. The prototype uses an Avago AT-32032 NPN bipolar transistor as the modulating switch. The modulating signal is synthesized using a Silicon Labs Si5351 CMOS clock generator which is programmed via I2C using a microcontroller and is capable of generating frequencies up to 200 MHz [42]. The Si5351 is powered from a 3.3 V rail generated from a LP2950 linear regulator. Additional circuit components to operate the Si5351 are shown in Figure 4.2. Note that an AD8032 amplifier is also included as an output buffer due to the limited current drive of the Si5351.

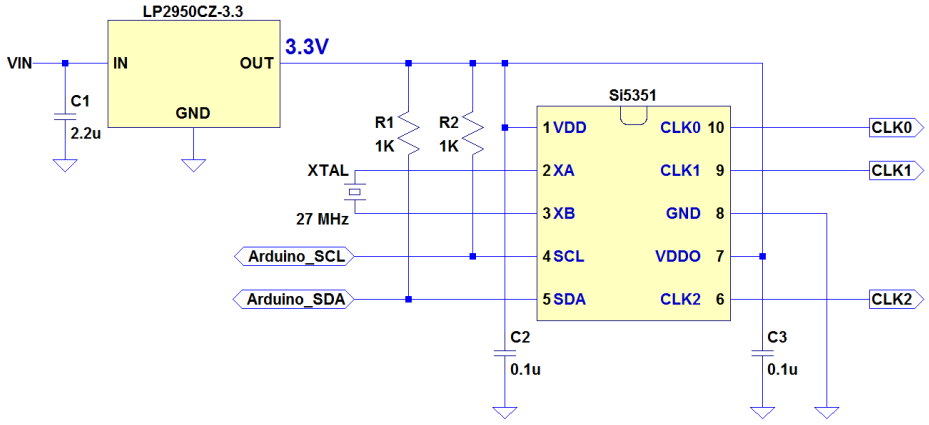

Figure 4.2 - Si5351 frequency synthesizer circuit

Three Taoglas ceramic patch antennas were used for the transmitting (TX), receiving (RX), and backscattering (BX) antennas. The antenna datasheet states a center frequency of 2482 MHz within the ISM band, a bandwidth of 85 MHz, and requires a minimum ground plane of 50 mm^2 [43]. Figure 4.3 shows the antennas mounted onto 100 mm^2 sheets of FR4. In Figure 4.4, the center frequency of the mounted antennas is measured at 2.5 GHz. Thus, the prototype uses a carrier at 2.5 GHz to maximize power. The TX antenna is connected directly to a bench top frequency synthesizer that generates the 2.5 GHz carrier with a transmit power of -10 dBm. The BX antenna is connected to

the collector of the Avago NPN transistor with the base driven by the Si5351 frequency synthesizer. The RX antenna is connected to an Agilent N9000A signal analyzer to detect the backscattered signal.

Figure 4.3 - Taoglas patch antennas mounted on an FR4 ground plane

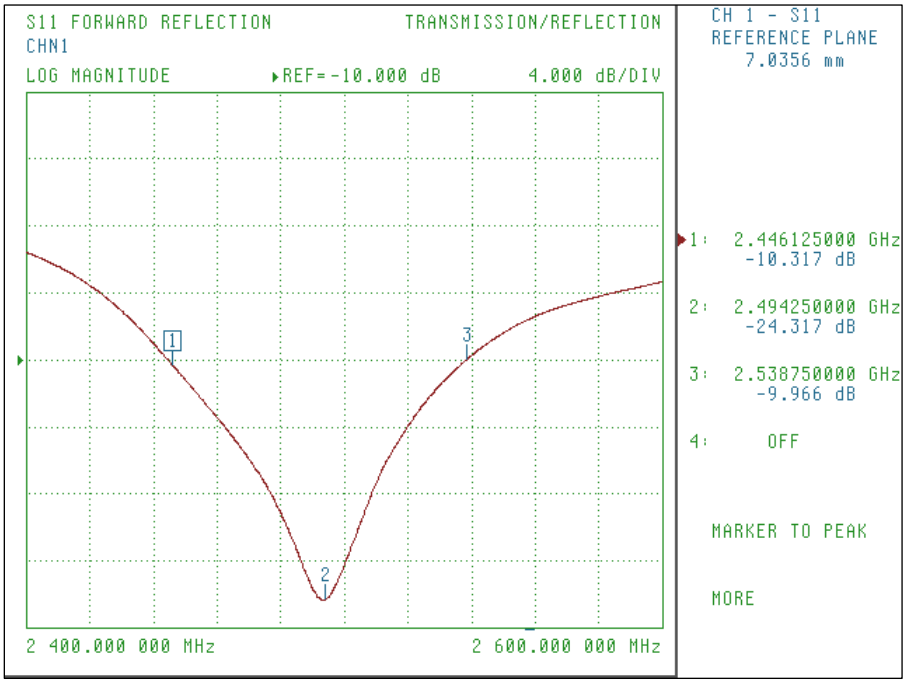

Figure 4.4 - Patch antenna center frequency measured at 2.5 GHz

The measured data in Table 4.1 show that the received power level is initially in the range of hundreds of nanowatts at low modulation frequencies, and decreases as the modulation frequency is increased. Thus, it is best to design a modulator on the integrated circuit that operates at lower frequencies for easier detection of the backscattered signal.

Additionally, a higher TX power can be used to attain a higher RX power since the prototype was only tested with -10 dBm, or 100 µW, of TX power.

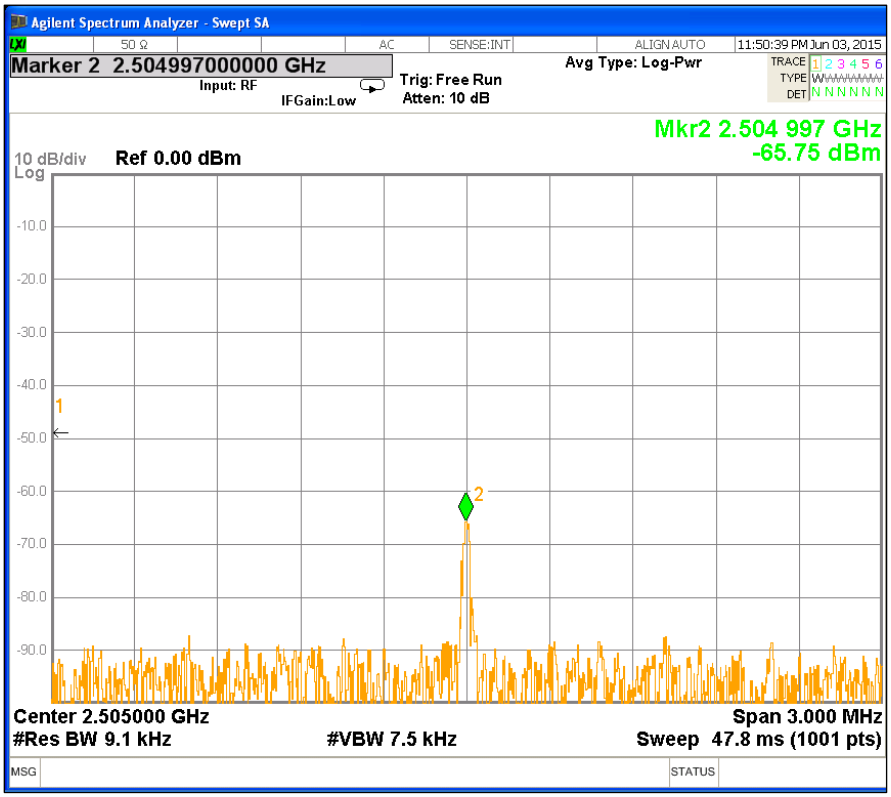

Figure 4.5 - RX power of -65.75 dBm for a 5 MHz subcarrier

Table 4.1 - Measured backscatter RX strength

Modulation Frequency (MHz)	RX Signal Strength (dBm)	RX Signal Strength (nW)
5.0	-65.75	266.07
10.0	-69.95	101.16
15.0	-66.21	239.33
20.0	-67.44	180.30
25.0	-70.55	88.10
30.0	-78.78	13.24

4.2. Current-Starved Ring Oscillator

Because the oscillator needs to be integrated on-chip, this precludes the use of any crystal oscillators. LC oscillators require the use of on-chip inductors which consumes significant area [27]. It is also desirable to have an oscillator that can easily interface with the capacitive IOP sensor.

Ring oscillators composed of CMOS inverters are appealing because their oscillation frequency is primarily dependent on the number of inverter stages, and the capacitance at the output of each inverter stage. The capacitance can easily be controlled by varying the transistor sizing of the following stage, which changes the total gate capacitance, or by placing an actual capacitor between the adjacent stages. The oscillation frequency is given by:

$$f_{osc} = \frac{1}{n \cdot (t_{PHL} + t_{PLH})} \quad \textit{(Eq. 4.1)}$$

where n is the number of inverter stages, t_{PHL} is the intrinsic high-low propagation delay, and t_{PLH} is the intrinsic low-high propagation delay [29]. Assuming the capacitance comes only from the gate capacitance of the next inverter stage, the total propagation delay is:

$$(t_{PHL} + t_{PLH}) = 0.7(R_n + R_p)C_{tot} = 0.7(R_n + R_p)\left[\frac{5}{2}(C_p + C_n)\right] \quad \textit{(Eq. 4.2)}$$

where C_p and C_n are the gate capacitances of the PFET and NFET, respectively, and R_n and R_p are the channel resistances of the PFET and NFET, respectively. From these two equations, it is evident it requires a combination of many stages or significant capacitance to obtain oscillation frequencies below 100 MHz.

To limit the oscillation frequency, the current going into the inverter stages can be restricted. The result is the current-starved voltage-controlled oscillator (CSVCO) in Figure 4.6, which is commonly used in digital phase-locked loops [29]. The oscillation frequency is set by the control voltage V_{inVCO} on transistor M5. Transistors M4 and M1 serve as a current source and current sink, respectively. Both are biased using transistors M5 and M6 to restrict the charging current to I_{D4}, and the discharging current to I_{D1}, respectively. Since the current is limited, the oscillation frequency is no longer dependent on the intrinsic propagation delays t_{PHL} and t_{PLH}. Assuming the current starving transistors

M1 and M4 are sized to achieve $I_{D1} = I_{D4} = I_D$, the center frequency of the current-starved ring oscillator where V_{inVCO} is at $V_{DD}/2$ is defined in [29] as:

$$f_{osc} = \frac{I_D}{nC_{tot}V_{DD}} \qquad \textit{(Eq. 4.3)}$$

where n is the total number of inverter stages, C_{tot} is the total capacitance at the inverter's input and output, and V_{DD} is the supply voltage.

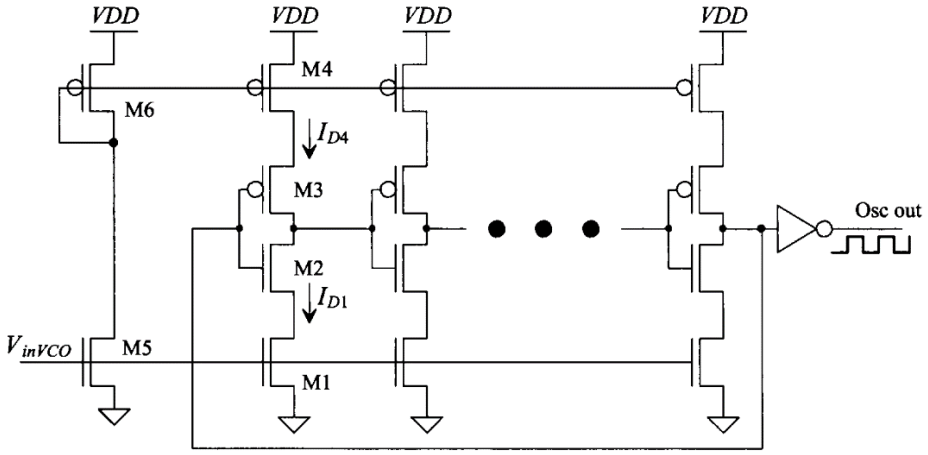

Figure 4.6 - Current-starved voltage-controlled oscillator [29]

4.2.1. Current-Starved Voltage-Controlled Oscillator Design Process

The project proceeds using the CSVCO topology to generate the modulating signal for the backscatter radio link. The current starving transistors allow for straightforward control of the current through each inverter stage, and does not require any complex biasing circuitry. Because the CSVCO's oscillation frequency is dependent on capacitance as shown in (4.3), it can easily be interfaced with the capacitive IOP sensor. This is discussed in further detail in the following section in 4.2.2.

For this design, the control voltage V_{INVCO} will be fixed to a constant 696 mV from the subthreshold voltage reference designed previously. The supply voltage V_{DD} is chosen to be 1 V, which is supplied from the linear regulator designed in chapter 3. Subsequently, the oscillator uses 1.2 V transistors rated for a maximum of 1.6 V.

There are three types of 1.2 V FETs available in the IBM 8RF process: the standard 1.2 V FETs, low V_T FETs (LVTNFET, LVTPFET), and low power FETs (LPNFET, LPPFET). The low V_T FETs have a threshold voltage that is about 100 mV lower than the standard FETs at the cost of ten times more leakage [(cite confidential IBM documents?)]. In contrast, the low power FETs have approximately 300 times less leakage, at the cost of a threshold voltage that is about 200 mV higher. The threshold voltages and transconductances of each are summarized in Table 2.2. From the standard equation for a MOSFET in saturation, it is clear that a higher transconductance requires a longer length to reduce the current ID, provided that the transistor has sufficient gate drive. However, the amount of gate overdrive, which is the amount of drive voltage in excess of the threshold voltage, also plays a role. With a 696 mV gate voltage, the standard NFETs with a 138 mV threshold will be more overdriven than the low power FETs which have a 622 mV threshold voltage. Simulation shows that using low power FETs for the current sinks to ground results in a much smaller design, despite having more transconductance than the standard FETs.

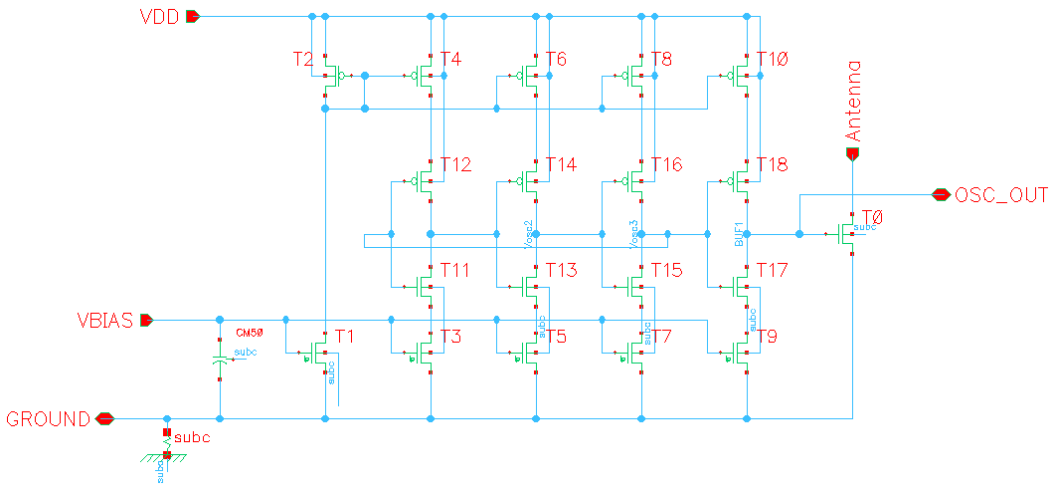

Figure 4.7 - CSVCO schematic

The full schematic is shown in Figure 4.7 and the transistor sizings are in Table 4.2. The CSVCO features three inverter stages formed by T11-T16. The current sources

and sinks formed by T3-T8. Each stage is biased by the current mirror formed by T1 and T2, which has a 1.6 µA DC bias current. Transistors T17 and T18 form a fourth inverter at the output to function as a buffer for driving the FET that modulates the antenna, and for driving additional test circuitry discussed later in the report. The buffer has its own current sink and source using T9, and T10, respectively. Transistor T0 is the FET that directly modulates the antenna.

Table 4.2 - CSVCO transistor sizing

Transistor	Type	Width (µm)	Length (µm)
T0	REDACTED		
T1			
T2			
T3			
T4			
T5			
T6			
T7			
T8			
T9			
T10			
T11			
T12			
T13			
T14			
T15			
T16			
T17			
T18			

4.2.2. Interfacing with the Intraocular Pressure Sensor

As discussed previously in section 2.1.3, the IOP sensor is assumed to be a capacitance ranging from 700 fF to 12 pF. Since the CSVCO's oscillation frequency is dependent on the total capacitance, it is convenient to directly connect the sensor to one of the inverter stages in the CSVCO. As the capacitance changes with pressure, the frequency will change accordingly. This removes the need for additional circuitry needed to sense information from the sensor.

4.2.3. Current-Starved Ring Oscillator Simulation Results

Figure 4.8 shows the output frequency of the CSVCO with the capacitive sensor placed between the first and second stage of the oscillator. The sensor is emulated using an ideal capacitance that is swept from 500 fF up to 13 pF. The frequency ranges from 71.7 MHz at low capacitances, down to 14.3 MHz at high capacitances. It is evident that the frequency sensitivity, defined as $\Delta f/\Delta C$, is high for capacitances below 6 pF. Larger capacitances above 6 pF exhibit a linear behavior of about 819 Hz/fF. The sensor presented in [11] has a resolution of 20 fF/4.5 mmHg with a base capacitance of 12 pF, which translates to a relative sensitivity of 16.4 kHz/4.5 mmHg. The two sensors in [10] have resolutions of 7.5 fF/10 mmHg, and 3 fF/10 mmHg with base capacitances of 1.167 pF and 784.92 fF, respectively. For the region ranging from 700 fF to 1.2 pF, the oscillator has a sensitivity of approximately 26.5 kHz/fF. Thus, the two sensors in [10]

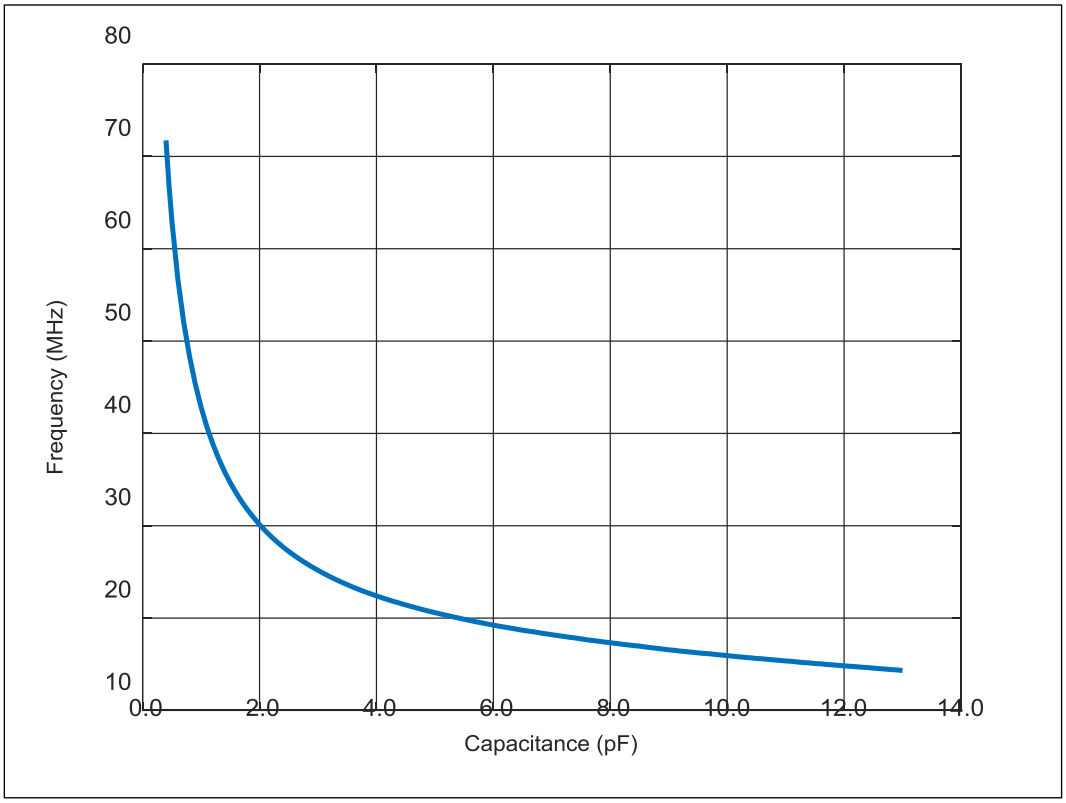

Figure 4.8 - Output frequency vs. sensor capacitance

would give a relative sensitivity of 198.8 kHz/10 mmHg and 79.5 kHz/10 mmHg. This is summarized in Table 4.3.

Table 4.3 - CSVCO sensitivity relative to sensor data

Sensor Source	Base Value	Sensor Resolution	CSVCO Sensitivity at Base Value	Total Relative Sensitivity
[10]	1.167 pF	7.5 fF/10 mmHg	26.5 kHz/fF	198.8 kHz/10 mmHg
[10]	784.92 fF	3 fF/10 mmHg	26.5 kHz/fF	79.5 kHz/10 mmHg
[11]	12 pF	20 fF/4.5 mmHg	819 Hz/fF	16.4 kHz/4.5 mmHg

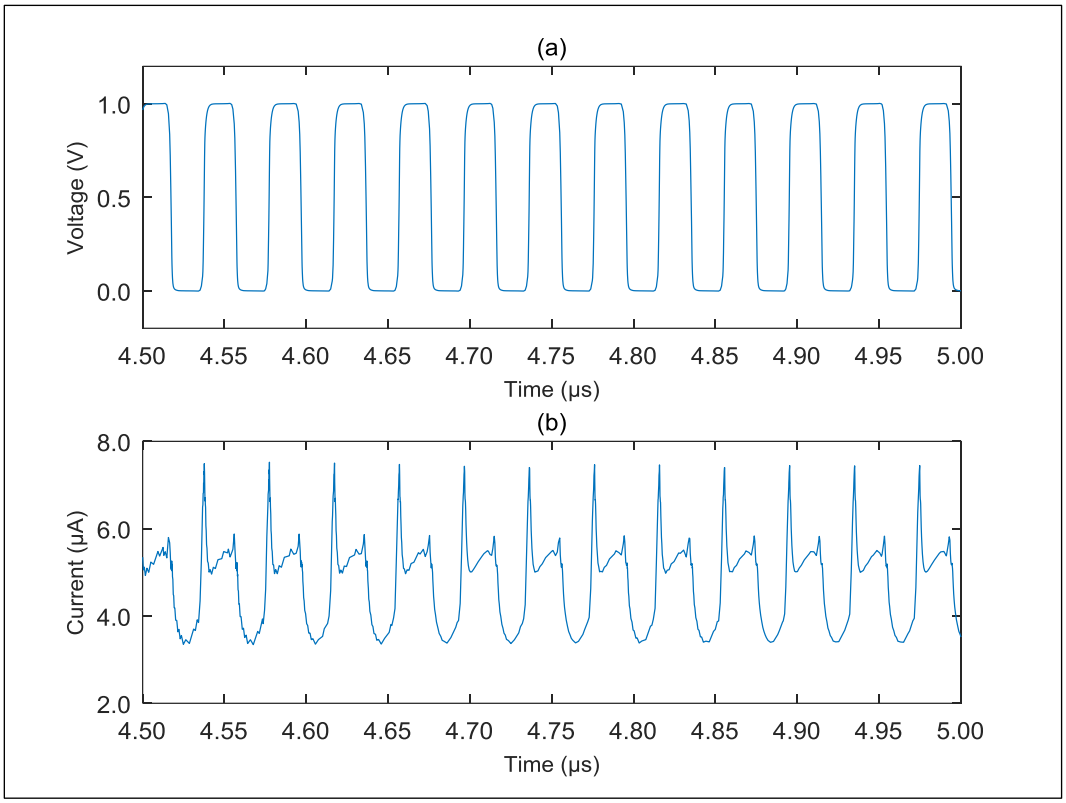

Figure 4.9 - Oscillator waveform (a) and input current (b)

Figure 4.9 shows the oscillator waveform with a sensor capacitance of 3 pF, along with the total input current consumption. The current peaks at 7.4 µA and is constant at across capacitances from 400 fF to 13 pF.

CHAPTER 5: BATTERY POWER MANAGEMENT

5.1. Recharging the Battery

As discussed previously in section 2.1.1, the Cymbet thin film battery is recharged by applying a 4.1 V to the battery terminals, but it is acceptable to apply any voltage ranging from 4.0 V to 4.3 V [17]. There are tradeoffs in charge capacity at the low end, and reduced lifetime at the high end. No external current limiting circuitry is necessary as long as the applied voltage does not exceed 4.3 V.

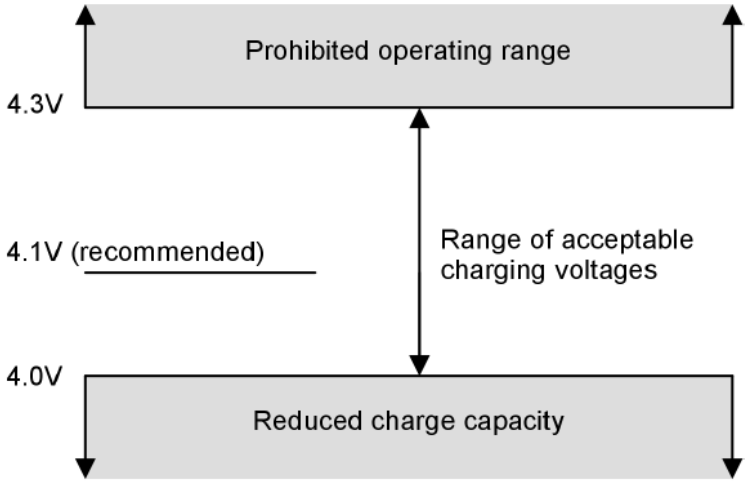

Figure 5.1 - Allowable voltage range for recharging [23]

5.1.1. Inductive RF-DC Rectifier

Since the antenna designed in [13] and [14] acts as an inductive coil at 13.56 MHz, it follows that the charging circuitry will be an RF-DC rectifier at this frequency. From section 2.1.2, there is a maximum of 22 dBm available when coupled with a 30 dBm source.

Figure 5.2 shows a basic one-stage voltage multiplier that will be used as the rectifier [44][45]. During negative cycles from the input V_{RF}, diode D1 is forward biased and capacitor C1 is charged to the signal's peak amplitude minus the diode drop from D1. During positive cycles, diode D1 is reverse biased, and diode D2 is forward biased. The

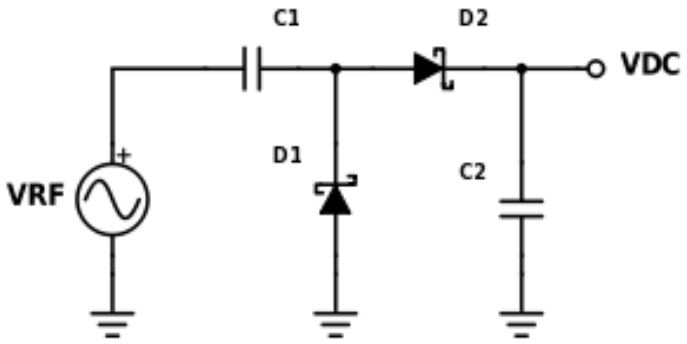

Figure 5.2 - One-Stage Voltage Multiplier [44][45]

voltage on C1 is added on top of the signal's positive peak amplitude, and goes to the output V_{DC} through diode D2, which incurs another diode drop. The resulting output voltage V_{DC} on the output capacitor C2 is twice the peak voltage minus two diode drops. Additional multiplier stages can be cascaded to attain a higher voltage. From [45], an N-stage voltage multiplier has an output given by:

$$V_{DC} = (N + 1)(V_p - 2V_D) \qquad \textit{(Eq. 5.1)}$$

where V_p is the peak amplitude of the input, V_D is the forward drop of the diodes, and N is the number of stages. Since the available inductive power is relatively high, it is not necessary to use more than one multiplier stage in the rectifier. A 22 dBm input corresponds to a 3.981 V peak. Ignoring the diode drops, the output of a single stage multiplier will be just under 8 V. In the 8RF process, the maximum voltage rating of the highest rated transistor type is 3.6 V. It is clear that the rectified output greatly exceeds the maximum rating of the available transistors. This precludes the design of any op-amp circuits, which restricts the design of the charging circuitry to an open loop design using only passive devices for regulating the output.

Figure 5.3 shows the full schematic of the RF-DC rectifier. The device sizings are tabulated in Table 5.1. The rectifier itself is composed of Schottky diodes D1 and D2, and capacitors CM1 and CM2. Diode D3 represents a series stack of 12 diodes, forming a voltage clamp. Diode D4 is placed to prevent the battery from discharging back through

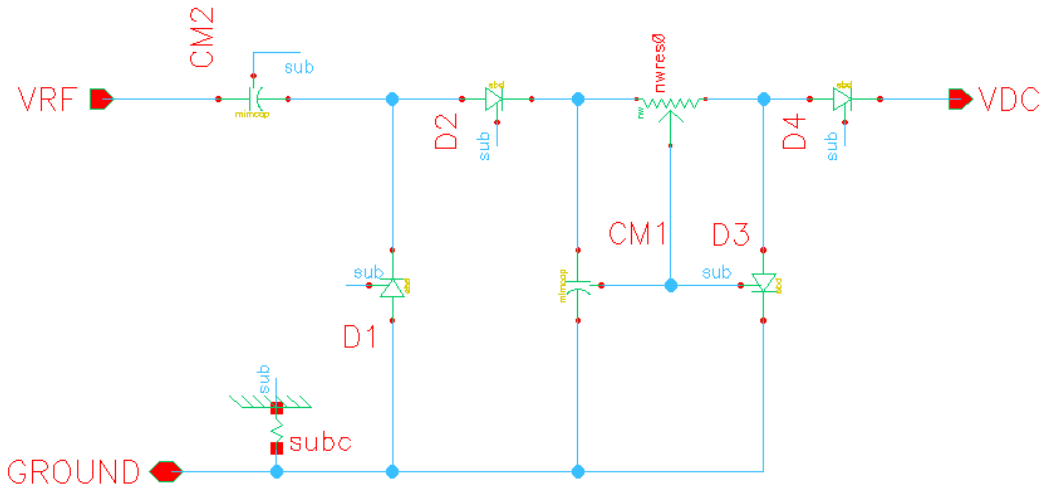

Figure 5.3 - RF-DC rectifier schemetic

Table 5.1 - Device sizing for the RF-DC rectifier

Component	Width (µm)	Length (µm)	Multiplicity	Bars	Value
D1	REDACTED				
D2					
D3 (x12)					
D4					
NWRES0					
CM1					
CM2					

the rectifier. The circuit is simulated using a 35 µA load that represents the battery charging profile from Figure 2.2. The input is a 13.56 MHz signal at a 20 dBm power level, corresponding to a peak amplitude of 3.16 V. The simulated output waveform is plotted in Figure 5.4. There is a small AC ripple on the output, which is expected from any type of AC-DC conversion. With a 10 pF output capacitor, the output waveform ripples between 3.60 V and 3.80 V, which gives a 3.70 V DC average. If desired, a larger output capacitance can be used to further reduce the ripple. Figure 5.5 shows the load behavior of the rectifier from a full 35 µA load, down to no load. The output ripples between 4.20 V and 4.26 V at no load.

Although a constant voltage is recommended by Cymbet for the fastest recharge time, it is not an absolute requirement [23]. In general, lithium ion batteries are recharged

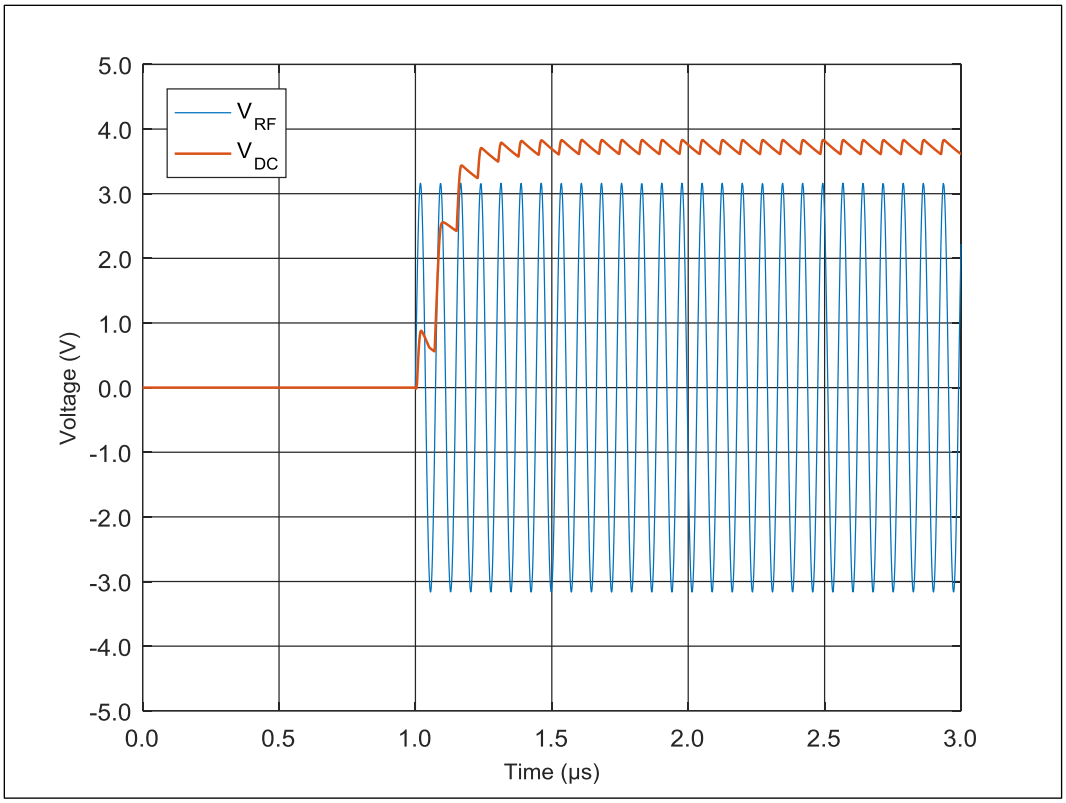

Figure 5.4 - Rectifier startup for a 20 dBm input and a 35 µA load

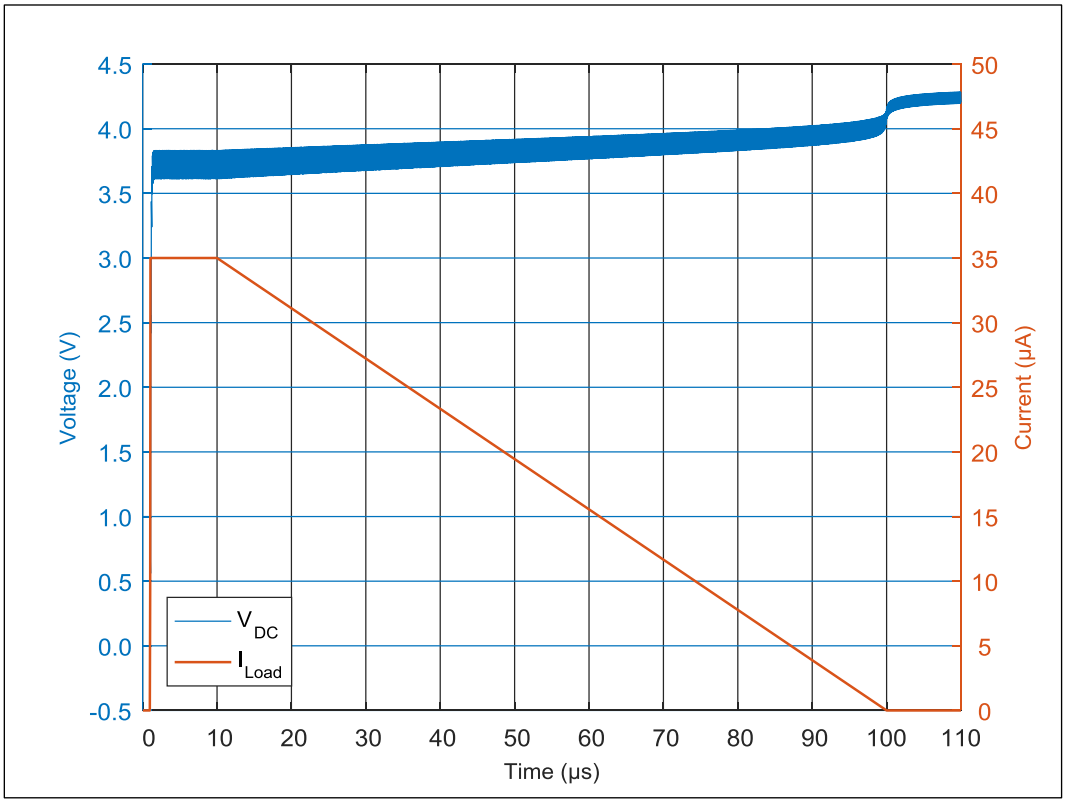

Figure 5.5 - Load behavior of the RF-DC rectifier

using four states as shown in Figure 5.6 [46]. The trickle charge region is reserved for batteries that have been discharged beyond their cutoff state. The constant current region is a mode that uses higher charging currents as the battery voltage recovers. The current is not necessarily held constant in this region. As the battery approaches its full capacity, it enters the constant voltage state where the charge current begins to drop off rapidly.

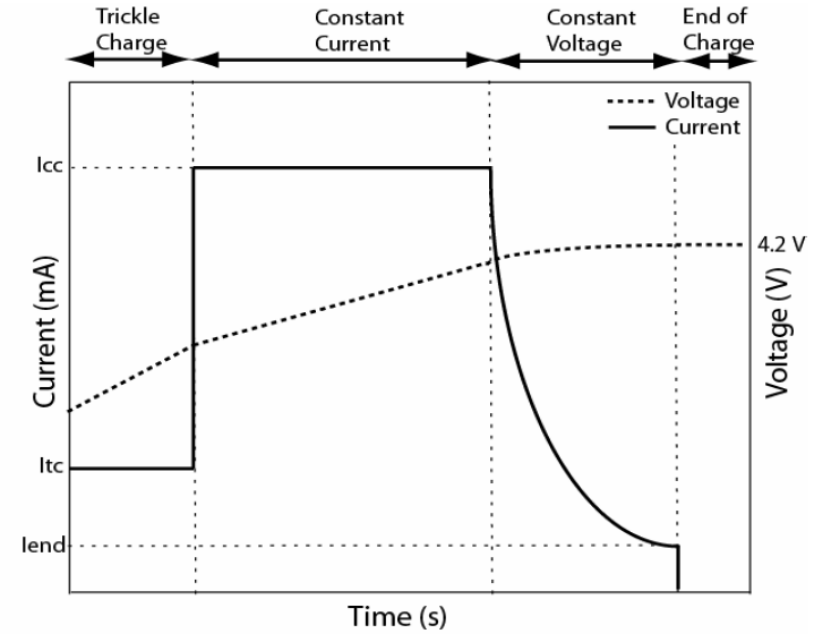

Figure 5.6 - Recommended general li-ion charging profile [46]

With this in mind, it is speculated that the performance of the RF-DC rectifier shown in Figure 5.5 will be sufficient to recharge the Cymbet battery. When the recharge begins with the battery in its empty state, it will pull the highest current and the output of the rectifier will be at an average of 3.72 V. Although the minimum of 4.0 V is recommended for charging, any voltage greater than the 3.0 V cutoff voltage will charge the battery [17][23]. The tradeoff is that it will not reach its full capacity. However, this is not expected to be a problem. As the battery is recharged, the current draw will decrease as shown by its charging profile in Figure 2.2, and this decreased load will cause the rectifier's output voltage to rise accordingly. Towards the end of the charge, the rectifier's output will eventually reach the recommended 4.0-4.3 V charging range, as

shown in Figure 5.5. Thus, this mitigates the issue with not reaching the battery's full capacity.

Because this is an open loop system, a major drawback is that the circuit has no method for detecting when large input power is applied to the rectifier. There is no workaround since no transistors with a sufficiently high voltage rating are available. The diode clamp at the output of the rectifier provides minimal protection from overvoltage conditions. Care must be taken during the testing process to monitor the input and output of the rectifier to ensure that damaging voltages are not applied.

5.2. Low Voltage Cutoff

To prevent the battery from falling into a deep discharge state, an undervoltage lockout (UVLO) circuit is employed. Figure 5.7 shows a generic hysteretic UVLO circuit from [48] that has been implemented in LTSpice using an op-amp configured as a comparator. The supply voltage V_{DD} is compared to some reference V_{REF} through the resistive divider network R1-R3. When V_{DD} is low, the output of the comparator is high, and both PFETs are off. The threshold voltage at the op-amp's inverting input is set by

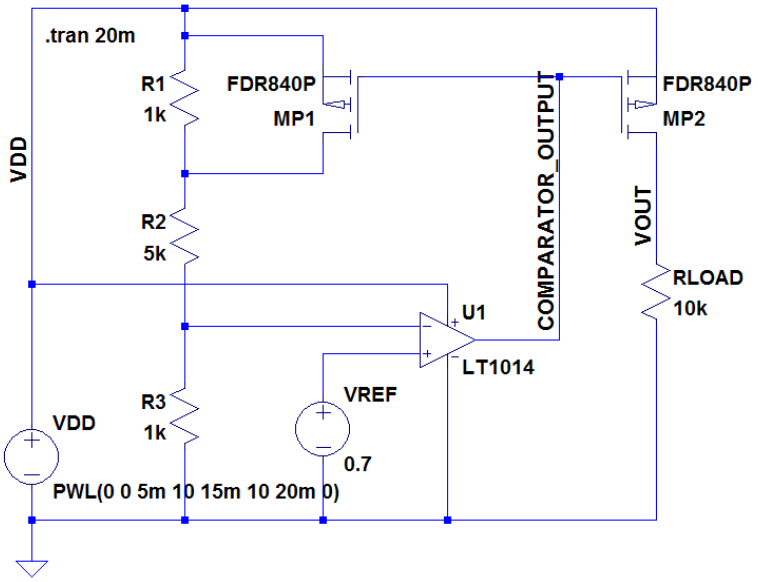

Figure 5.7 - Generic hysteretic UVLO circuit [48]

the three resistors. When V_{DD} rises high enough for the voltage across R3 to exceed V_{REF}, the comparator's output goes low, turning on both PFETs. Transistor MP2 passes the supply voltage to the load, and MP1 bypasses resistor R1, which has the effect of generating hysteresis by lowering the threshold voltage below the value initially set by the three resistors.

The simulated output of the circuit is plotted in Figure 5.8. The output V_{OUT} is cut off by MP2 until the supply V_{DD} reaches the turn-on threshold at 5 V. The hysteresis provided by MP1 lowers the threshold to 4 V. This hysteresis is important in battery powered systems since the presence of a load often causes the battery voltage to droop. Without hysteresis, the droop may be enough trip the comparator into turning off MP2 to cut off the load, where the battery voltage will then rise back up and flip the comparator again, resulting in oscillation.

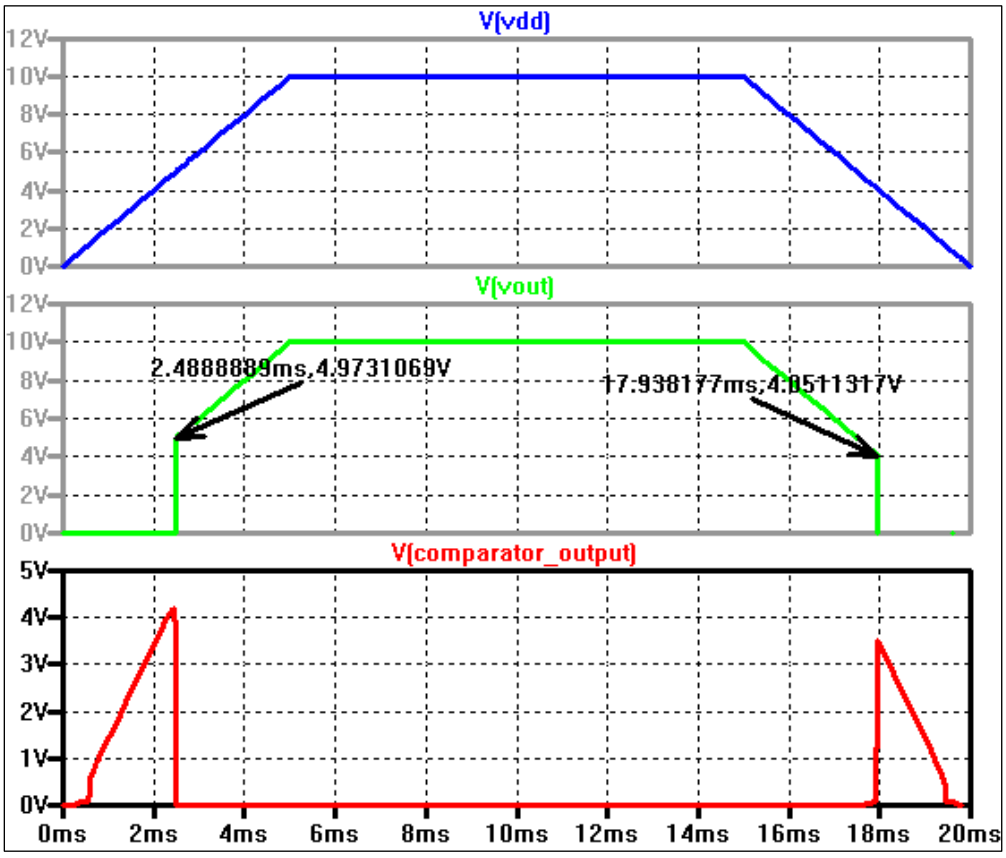

Figure 5.8 - Output of the hysteretic UVLO circuit

5.2.1. UVLO Circuit Design and Simulation Results

The transistor level design of the UVLO circuit is shown in Figure 5.9. It follows the same topology presented in Figure 5.7 above, and Table 5.2 contains the device sizings. The comparator is derived from the same error amplifier used for the 1 V linear regulator from section 3.3.2. The length of tail transistor T5 has been elongated significantly to minimize the quiescent current. The voltage reference is now tied to the noninverting input at the gate of T4, instead of the inverting input on T3 as was done for the linear regulator. The reference and bias use the 696 mV subthreshold voltage reference.

Instead of using resistors that consume significant area, transistors are used to sense the battery voltage. Transistor T7 is configured as a constant current source so that the current consumption in the sensing network remains constant across the entire range

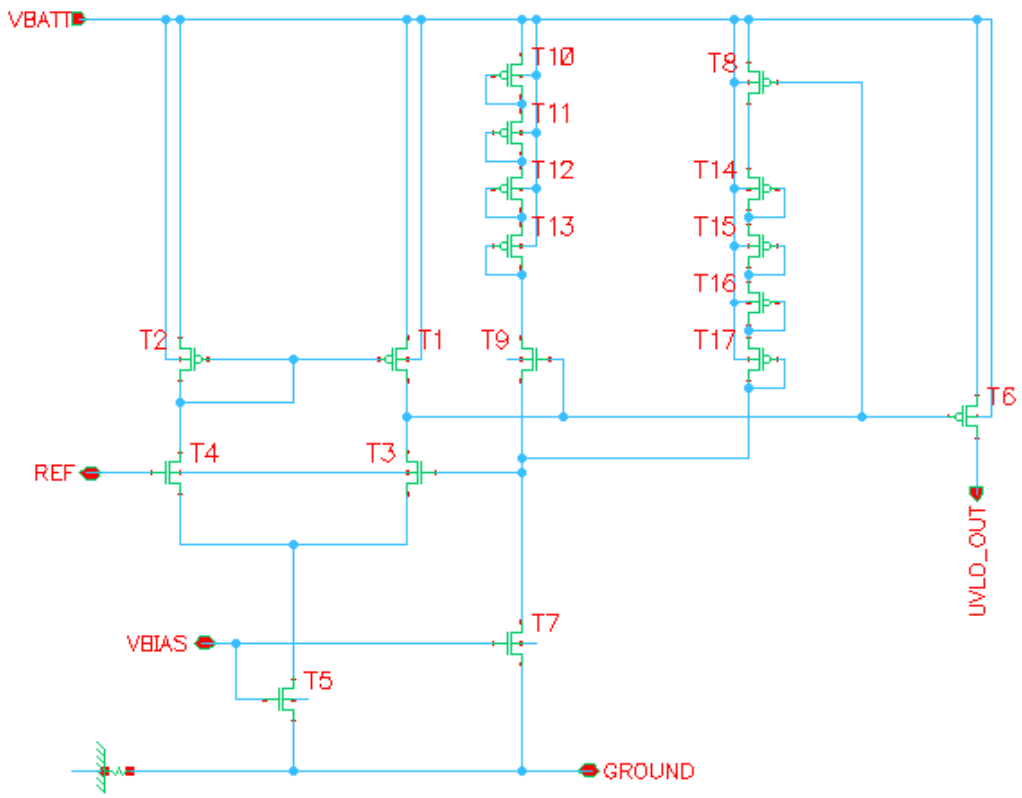

Figure 5.9 - Full hysteretic UVLO schematic

Table 5.2 - Transistor sizings for the UVLO circuit

Transistor	Width (µm)	Length (µm)
T1	REDACTED	
T2		
T3		
T4		
T5		
T6		
T7		
T8		
T9		
T10		
T11		
T12		
T13		
T14		
T15		
T16		
T17		

of V_{DD}. The rest of the sensing network is composed from transistors T10-T13, or T14-T17, depending on which state the UVLO circuit is in. When the battery voltage is low, the output of the comparator will be high, T9 will be on, T8 will be off, and the sense network will use transistors T10-T13. If there is sufficient battery voltage to drive the comparator's output low, then T9 will turn off, and T8 will turn on, switching the sense network to transistors T14-T17. Hysteresis is attained by varying the total length of the two sets of transistors.

The simulation result in Figure 5.10 shows that the UVLO circuit passes the supply voltage when it exceeds 3.2 V. On the falling edge, it cuts off the supply when it dips below 3.1 V, resulting in 100 mV of hysteresis. The hysteresis is more visible when the output is plotted against the supply in Figure 5.11. The cut off threshold is set above the 3.0 V to allow for some headroom to ensure that the battery does not fall into a deep discharge state. The UVLO circuit consumes 84.5 nA of quiescent current. This small current draw is due to the use of long lengths in transistors T5 and T7.

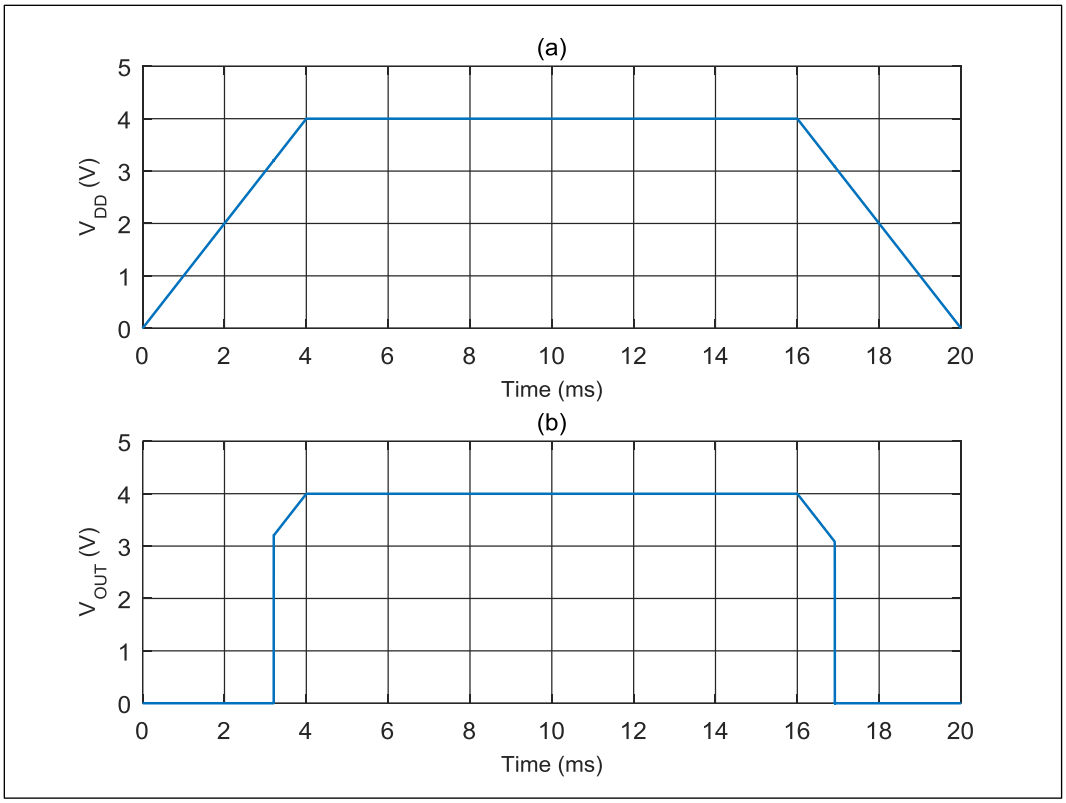

Figure 5.10 - UVLO input (a) and output (b)

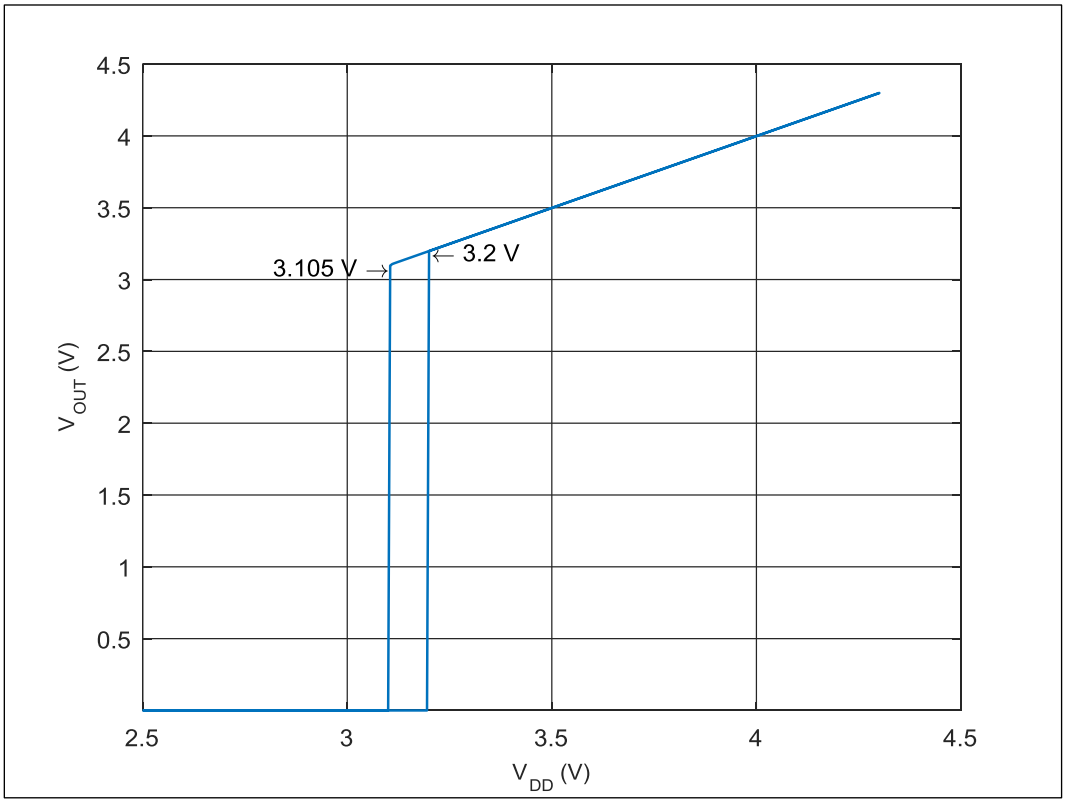

Figure 5.11 - UVLO V_{OUT} vs. V_{DD}

5.3. Standby State

To maximize operating time, the system needs to fall into a standby or sleeping state where power consumption is minimized. When an external trigger is presented, the circuit needs to resume normal operation and transmit sensor data. Since the only available external stimulus is the 2.4 GHz signal used for the backscatter communication link, the circuit needs to be triggered using the limited power that can be scavenged at this frequency. With a nominal capacity of 5 μAh available from the Cymbet battery, the quiescent current needs to be limited to 208 nA for 24 hours of standby power. For 12 hours of standby power, the requirement is relaxed to 416 nA.

5.3.1. Standby State Implementation

Each of the circuit blocks designed thus far serve as a potential point for creating a low power sleep state. The CSVCO is the first point of interest since it is the primary source of current consumption. However, putting only the CSVCO into standby would still leave the 1 V linear regulator in operation. From Table 3.5, the regulator draws 914 nA, which will greatly reduce standby operating time. It follows that turning off the regulator would also have the greatest effect on reducing quiescent current. Shutting down the regulator would also remove the CSVCO's power source.

The linear regulator is dependent on the subthreshold voltage reference, and the UVLO circuit. The two consume 110 nA and 84.5 nA of quiescent current, respectively, for a total of 194.5 nA. Combined with the regulator, this value rises to over 1 μA. Turning off the voltage reference is the most straightforward way of deactivating the regulator since its biasing comes from the reference. However, the UVLO circuit is also dependent on the reference for biasing. If the subthreshold voltage reference is to be

disabled, modifications on either the UVLO, linear regulator or the reference itself are needed.

The voltage reference is modified as shown in Figure 5.12. Transistor T13 has been added and is controlled by the wake signal *EN*, which is discussed later in section 5.4. When T13 is off, the output V_{REF} follows the battery voltage V_{DD}. The current mirror biasing formed by MOSFETs T1-T3, T8-T9, and BJT Q1 remains on. The UVLO is also modified to use the *EN* signal in Figure 5.13. Since the voltage reference follows V_{DD} when EN is low, transistors T18 and T19 are added to cut off the current through T5 and T7.

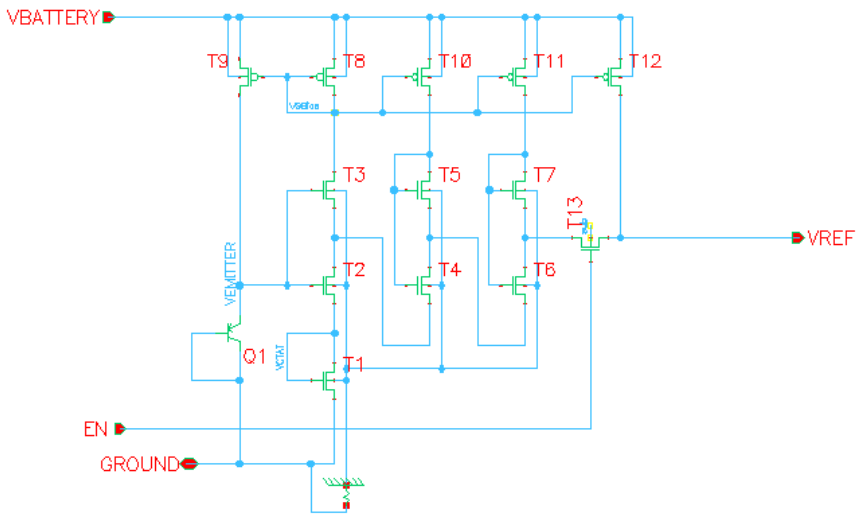

Figure 5.12 - Modified voltage reference with EN function

Figure 5.14b shows the outputs of the modified UVLO and voltage reference circuits for two sweeps of V_{DD}. In the first sweep, *EN* is low. As V_{DD} rises, both the reference and UVLO is disabled and its output V_{REF} follows V_{DD}. The UVLO output V_{UVLO} remains low as desired. During this state, the quiescent current of both circuits is 161 nA, which is drawn entirely by the subthreshold voltage reference. The addition of T13 in Figure 5.12 slightly disturbs the bias point of current mirror, which results in a quiescent current that is higher than the 110 nA in Table 3.3. However, this increase is acceptable since this setup disables the UVLO and the 1 V regulator, removing their

quiescent current from the overall drain. In the second sweep beginning at 75 ms, *EN* is asserted. The voltage reference functions as normal, and the UVLO circuit passes V_{DD} when it reaches the appropriate thresholds.

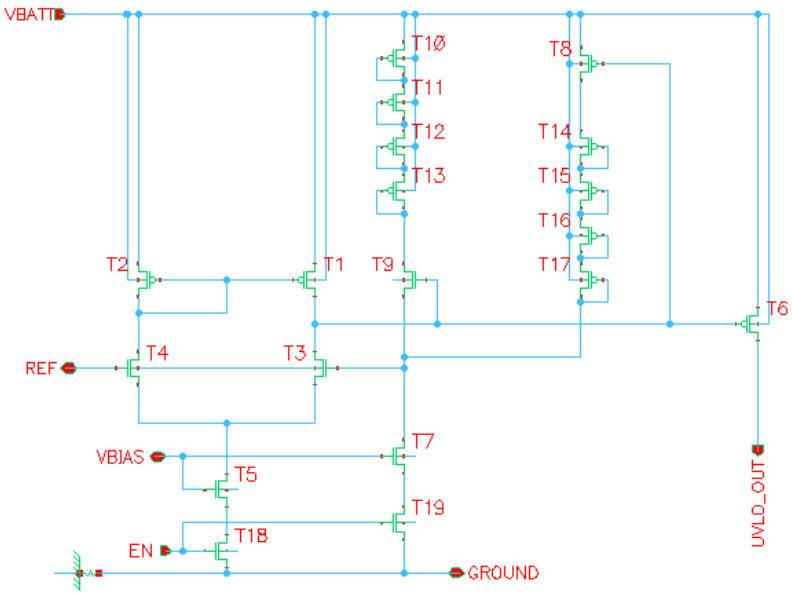

Figure 5.13 - Modified UVLO with EN function

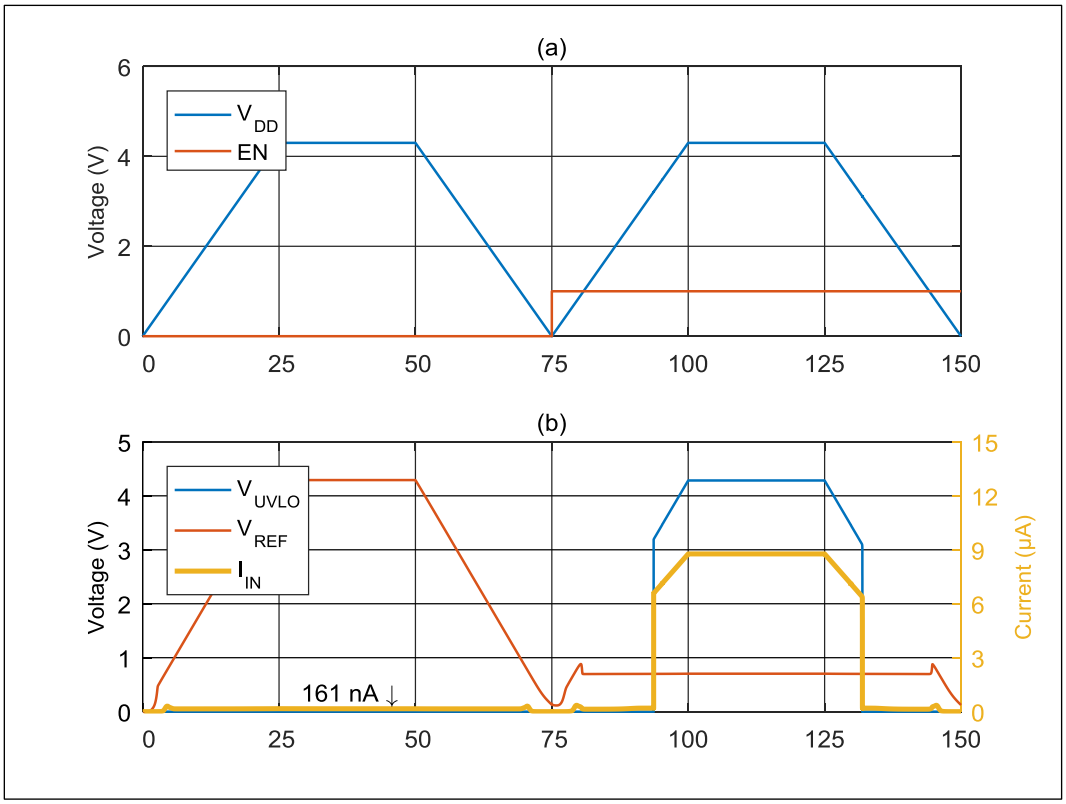

Figure 5.14 - Inputs (a) to modified UVLO and V_{REF} circuit, and the outputs (b)

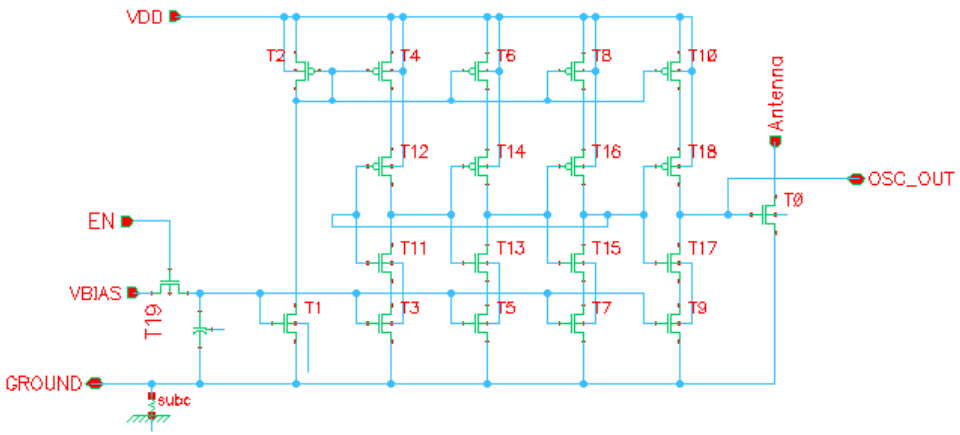

Figure 5.15 - Modified CSVCO with EN input

Figure 5.15 shows the CSVCO modified to have its bias VBIAS controlled by transistor T19. Since the simulation in Figure 5.14 above shows VREF rising to the supply rail during the standby state, there is a potential for the bias to overdrive the current sinks formed by transistors T1, and T3-T9. Although the UVLO output is low, the overdrive may cause measurable leakage current through the CSVCO. Transistor T19 cuts off this possible overdrive state.

5.4. EN Wake Signal

As discussed in section 5.3, the only external stimulus available comes from the 2.4 GHz signal used for the backscatter communication link. Thus, the wake trigger will be generated using another RF-DC rectifier placed in parallel with the previously designed rectifier from section 5.1.1. Since the signal's power level is expected to be much lower, additional multiplier stages are needed. Additionally, there is a minimum power level required to overcome the threshold voltages of the devices being used.

5.4.1. 2.4 GHz RF-DC Rectifier

From the simulation results in Figure 5.14, the rectifier needs to generate close to 1 V for the *EN* signal. The *EN* signal needs to be asserted long enough for a measurement

to be performed. The previous 13.56 MHz rectifier design in section 5.1.1 uses Schottky diodes with a threshold voltage of about 0.380 V. The input signal peak needs to exceed this threshold for the rectifier to function. This requirement can be relaxed by taking advantage of the body diode in PFET transistors. Using the low threshold voltage PFET transistors (LVTPFET) from Table 2.2 and connecting their body terminal to their source, a low voltage diode is obtained [9]. There is also another restriction on power level in that the rectifier should not be triggered by ambient RF signals at the antenna's operating frequency. Thus, the required power level to wake the system should be low enough to not require excessive transmit power from the external measurement device, yet still high enough to avoid having the circuit be pulled out of its sleep state by ambient energy. [49] and [50] features research on harvesting energy from ambient RF energy, which the authors define as power levels up to -20 dBm. Thus, a minimum power level of -10 dBm is chosen, which corresponds to the power level used in the backscatter prototype in section 4.1.2.

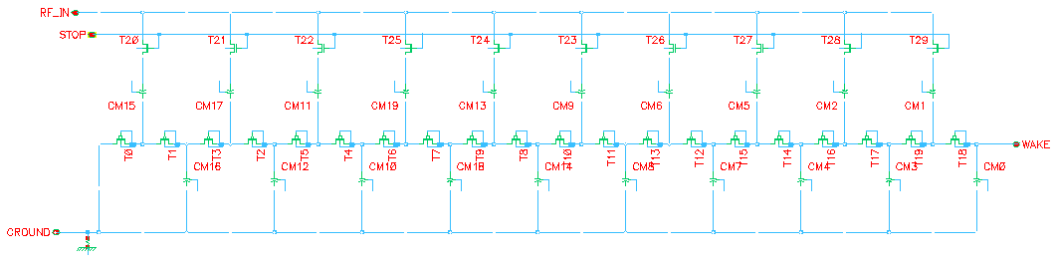

Figure 5.16 - Wake rectifier circuit

The RF-DC rectifier in Figure 5.16 features a 10-stage RF-DC rectifier. Using equation 5.1, this is the minimum number of stages required to attain close to a 1 V output for a -10 dBm input, which has a peak voltage of 100 mV. Transistors T0-T19 are the LVTPFETs in the middle forming the rectifying diodes. All are sized with REDACTED widths, and REDACTED lengths. All capacitors are sized REDACTED for a capacitance of 1.3 pF with the exception of the output capacitor CM0, which is sized

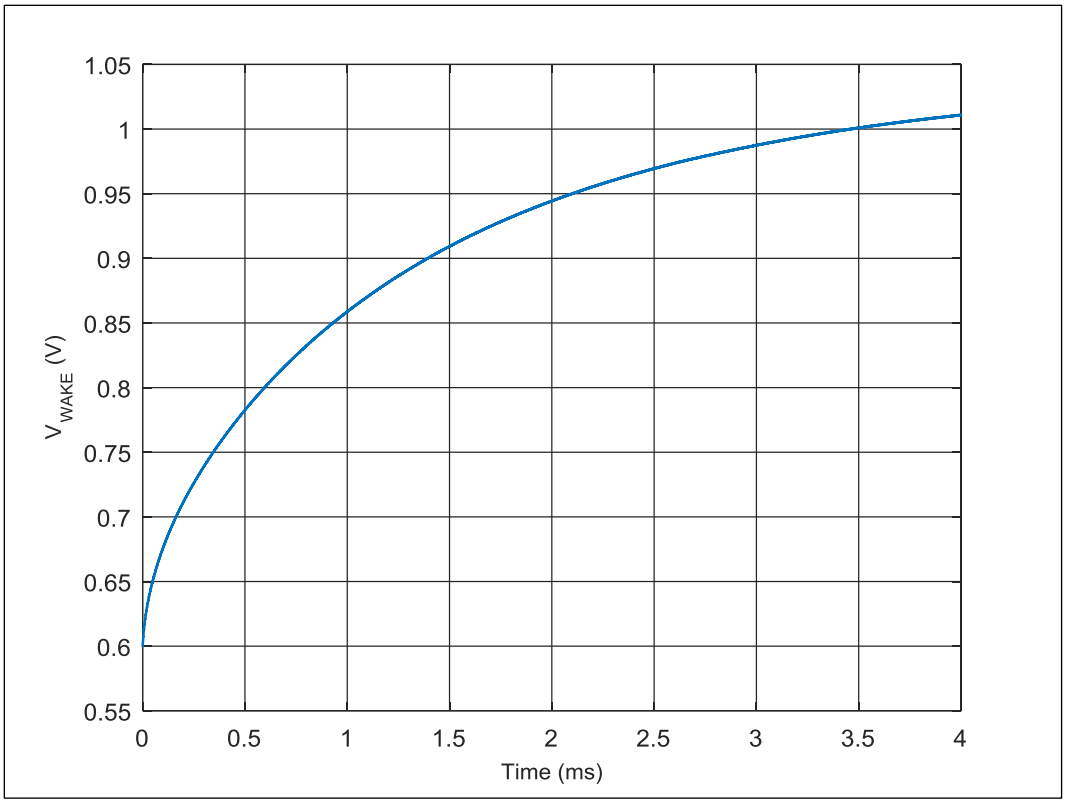

Figure 5.17 - Output V_{WAKE} for a -10 dBm input

REDACTED for a capacitance of 10 pF. Transistors T20-T29 are used as switches to cut off the rectifier stages when the *WAKE* output activates on the UVLO and voltage reference circuits. These signals are controlled by the *STOP* pin, and is connected to the comparator in the UVLO. Not shown in Figure 5.16 is a diode stack used as a voltage limiter as done with the charge rectifier in Figure 5.3. Since the wake rectifier is connected to the same antenna used for inductive charging, it is possible to generate excessively large voltages at its output. This will be clamped by the diode stack.

Figure 5.17 shows the rectifier output for a -10 dBm input signal. The STOP signal is fixed high to verify the rectifier is capable of generating sufficient output voltage. Functionally, the STOP pin will be pulled low by the UVLO's comparator which will clamp the *WAKE* output to the *EN* threshold needed to turn on the UVLO and voltage reference. This is discussed further in the next chapter.

CHAPTER 6: COMPLETE SYSTEM PERFORMANCE

6.1. Subcircuit Interfacing

This chapter covers the interfacing of all subcircuits designed. The complete system is shown with all the circuit blocks abstracted to block diagram symbols to simplify the figures presented. The interfacing will be done in multiple steps to minimize circuit complexity to reduce simulation time.

6.1.1. Inductive Rectifier and Battery

The output V_{CHG} of the 13.56 MHz rectifier is directly connected to the battery. The UVLO and voltage reference are also connected directly to the battery, which opens the possibility of large voltages being applied to these two circuits. To prevent this, a transistor switch is placed between the battery and the two subcircuits as shown in Figure 6.1. When inductively coupled, both the charge rectifier and wake rectifier will start to ramp up their outputs since both are connected to the antenna. When charging, V_{DC} is high and will turn off transistor T0, cutting the battery off from the rest of the system for the duration of the charge. Figure 6.2 confirms this behavior. At 5 ms, a 20 dBm signal is applied to turn on both rectifiers. Signal V_{DC} turns off transistor T0, while V_{WAKE} is clamped by its output limiter.

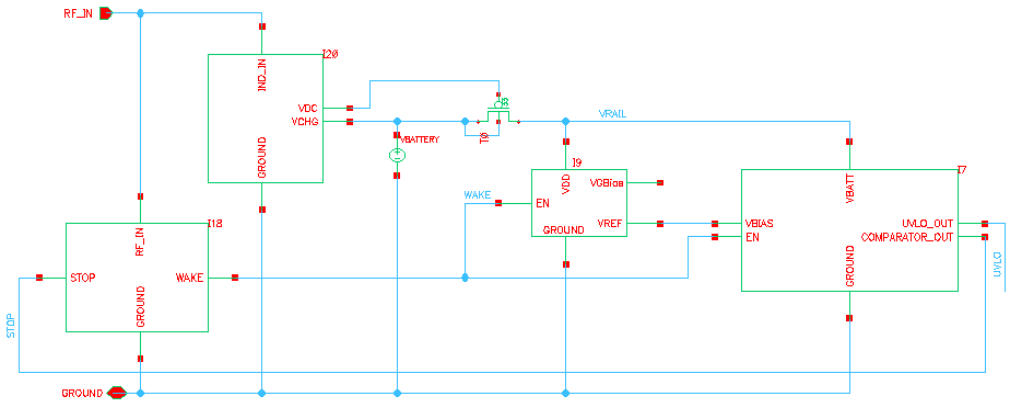

Figure 6.1 - Inductive rectifier connected to the UVLO and sub-V_T voltage reference

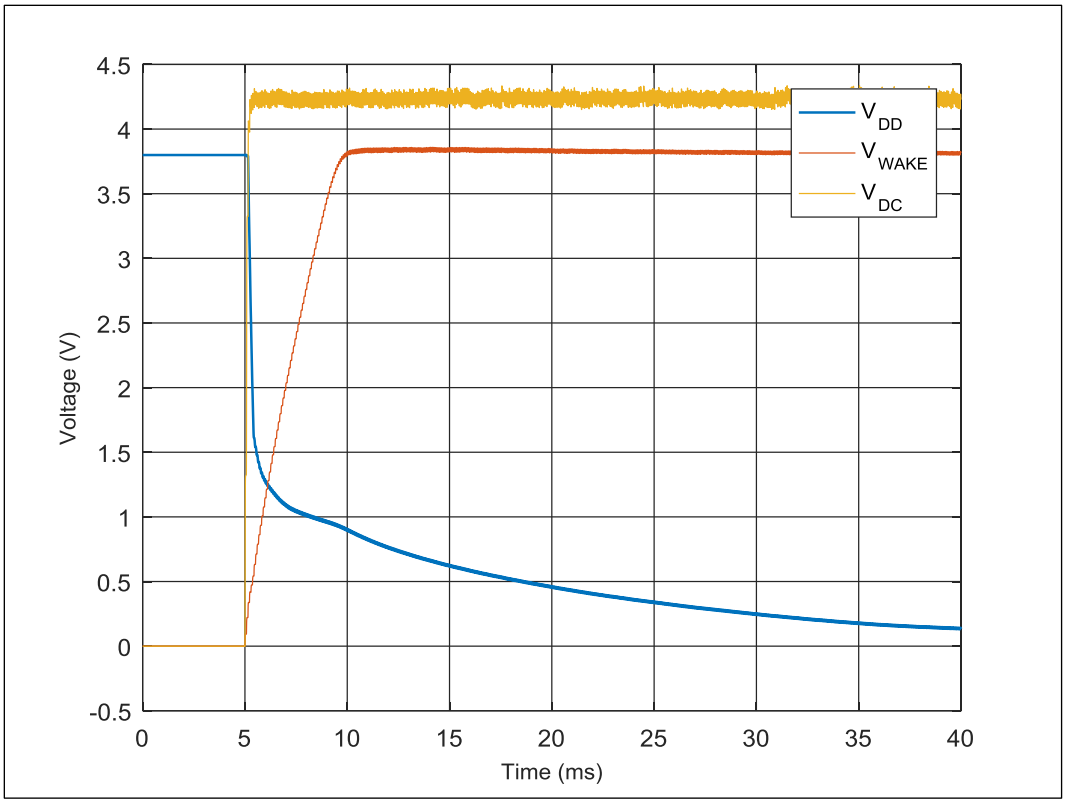

Figure 6.2 - Behavior of the interface when charging

6.1.2. Interfacing the Wake Trigger with the UVLO and Sub-V_T Reference

Figure 6.3 shows the wake circuit connected to the UVLO and subthreshold voltage reference. The 1 V regulator and CSVCO are not included here. The two are

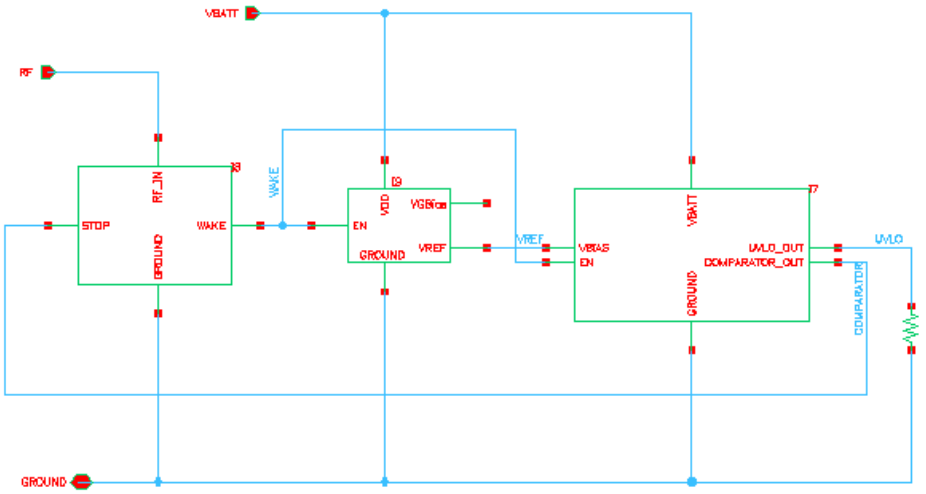

Figure 6.3 - Interfacing the wake circuitry with the UVLO and voltage reference

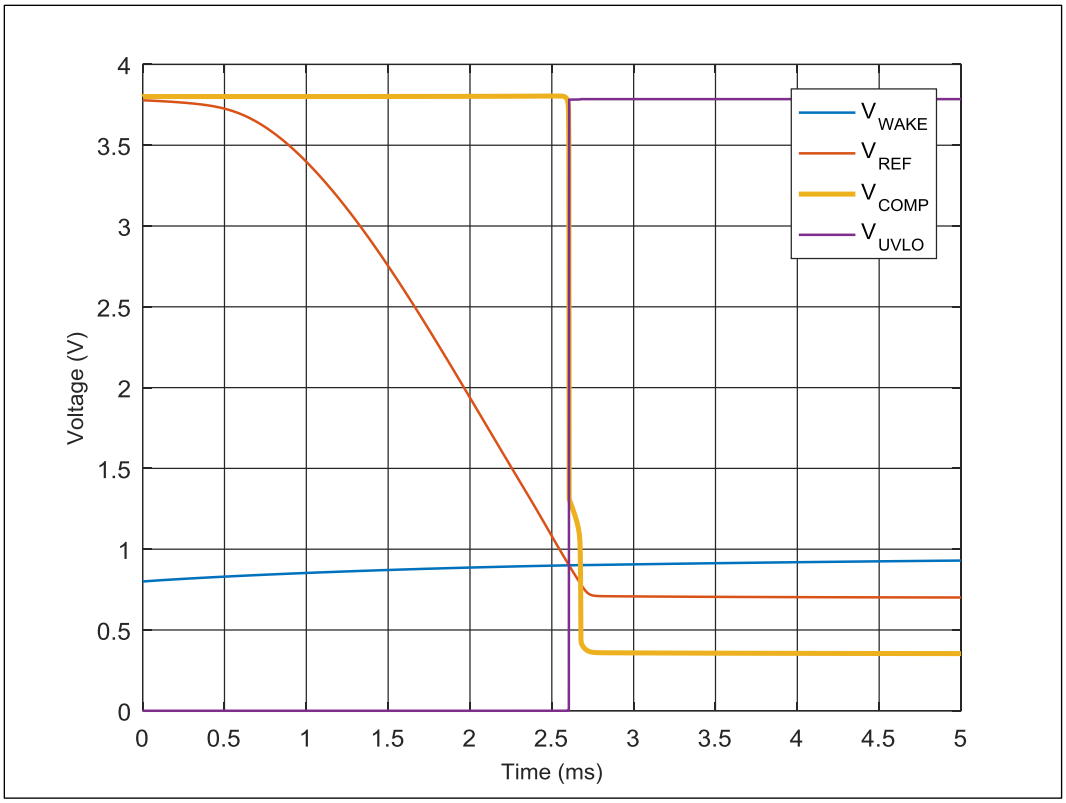

Figure 6.4 - Startup output signals for the wake interface

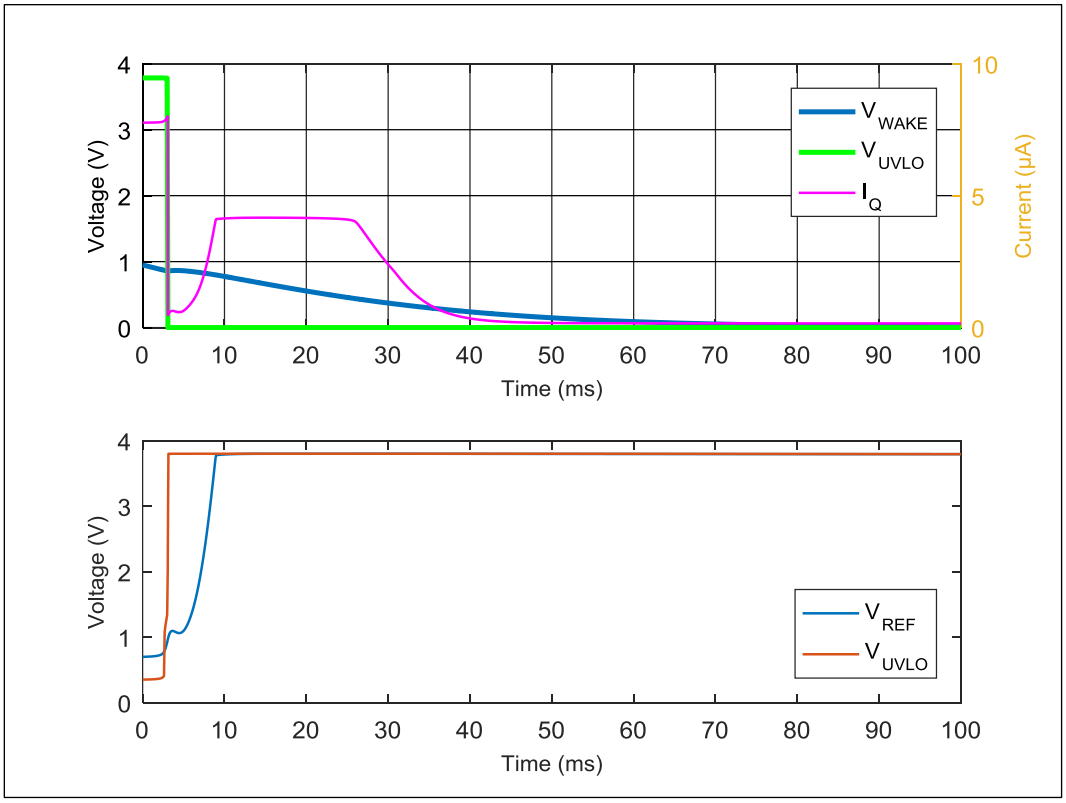

Figure 6.5 - Shutdown sequence for the wake interface

instead represented as a resistive load attached to the UVLO output to simplify the simulation. The charge rectifier is also excluded since the low power levels used to trigger the wake rectifier will not generate any output on it. Figure 6.4 above shows the simulated outputs. As V_{WAKE} rises beyond 800 mV, V_{REF} is the first to come out of standby. Transistor T13 in Figure 5.12 begins conducting current, and V_{REF} starts to fall towards its reference value. When V_{WAKE} exceeds 900 mV, the UVLO comparator output V_{COMP} falls low, and V_{UVLO} rises to the battery voltage.

The simulated shutdown sequence is plotted in Figure 6.5 on the previous page. When the RF input is removed, V_{WAKE} begins to decay. Within 5 ms, the UVLO comparator goes high and cuts off V_{UVLO}. The reference circuit turns off, and V_{REF} rises to the battery voltage. The total current falls to the 161 nA quiescent value as V_{WAKE} continues to decay to zero, and the circuit eventually settles into its standby state.

6.1.3. Interfacing the UVLO, Sub-V_T Reference, 1 V Regulator, and CSVCO

Figure 6.6 shows the circuits being interfaced in this section. For this portion, the wake rectifier has been removed since its functionality has already been verified in the previous section. The wake signal will be generated using an input pin. The oscillator stage is loaded with a 12 pF capacitor to force it to run at a lower frequency that will allow for a quicker simulation.

The simulated startup is presented in Figure 6.7. The simulation is cropped to the region of interest from 9.5 ms to 10 ms. Prior to this, the wake signal is still ramping up and the circuit is in its sleep state. As shown before in Figure 6.4, the UVLO circuit passes the supply voltage once it comes out of standby. At this

point, the 1 V linear regulator output quickly ramps up to its 1 V DC steady state value. Simultaneously, the CSVCO begins oscillating. Figure 6.8 shows the DC steady state

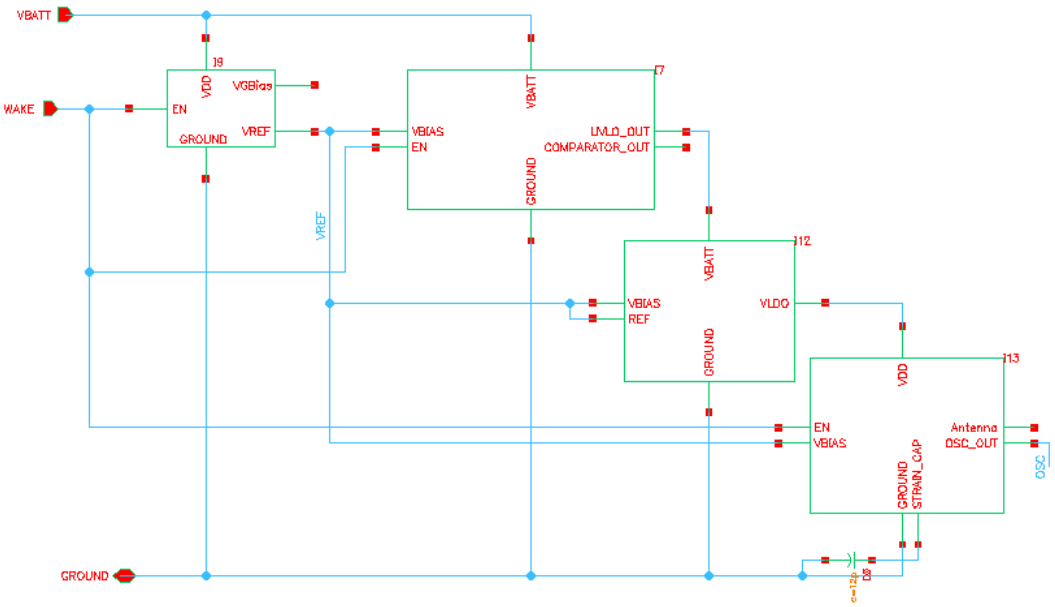

Figure 6.6 - Interfacing the UVLO, Sub-VT reference, 1 V regulator, and CSVCO

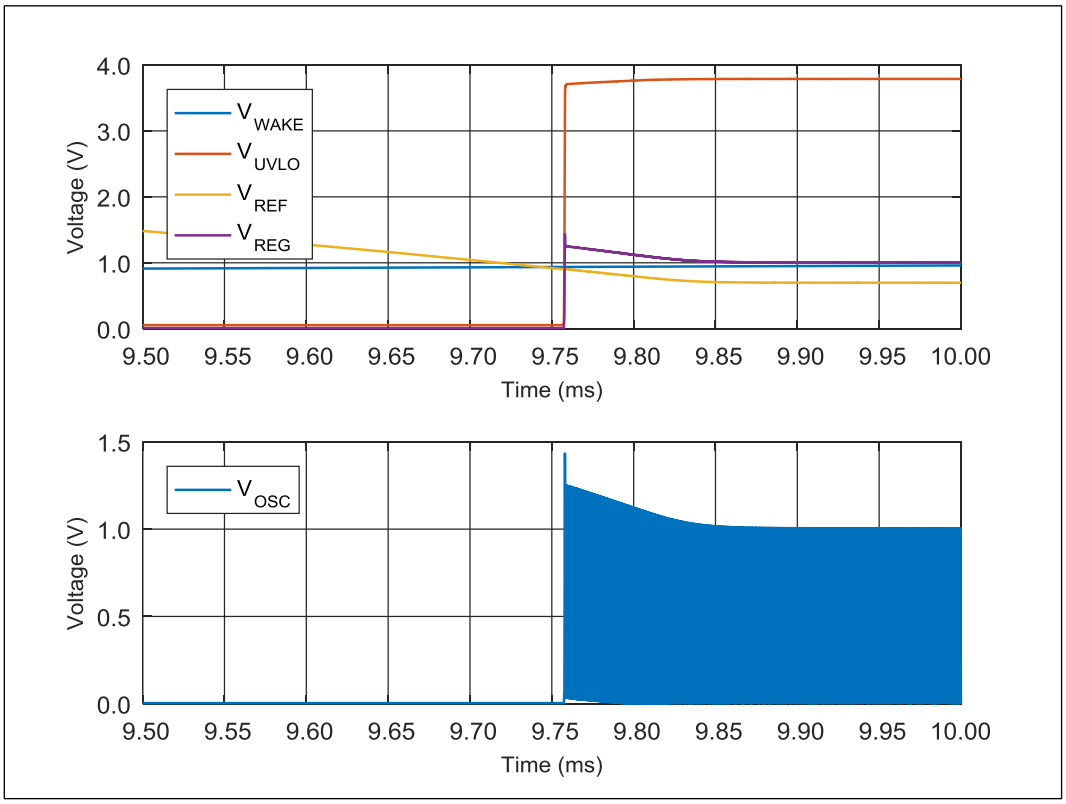

Figure 6.7 - Start up waveforms for the interface in Figure 6.6

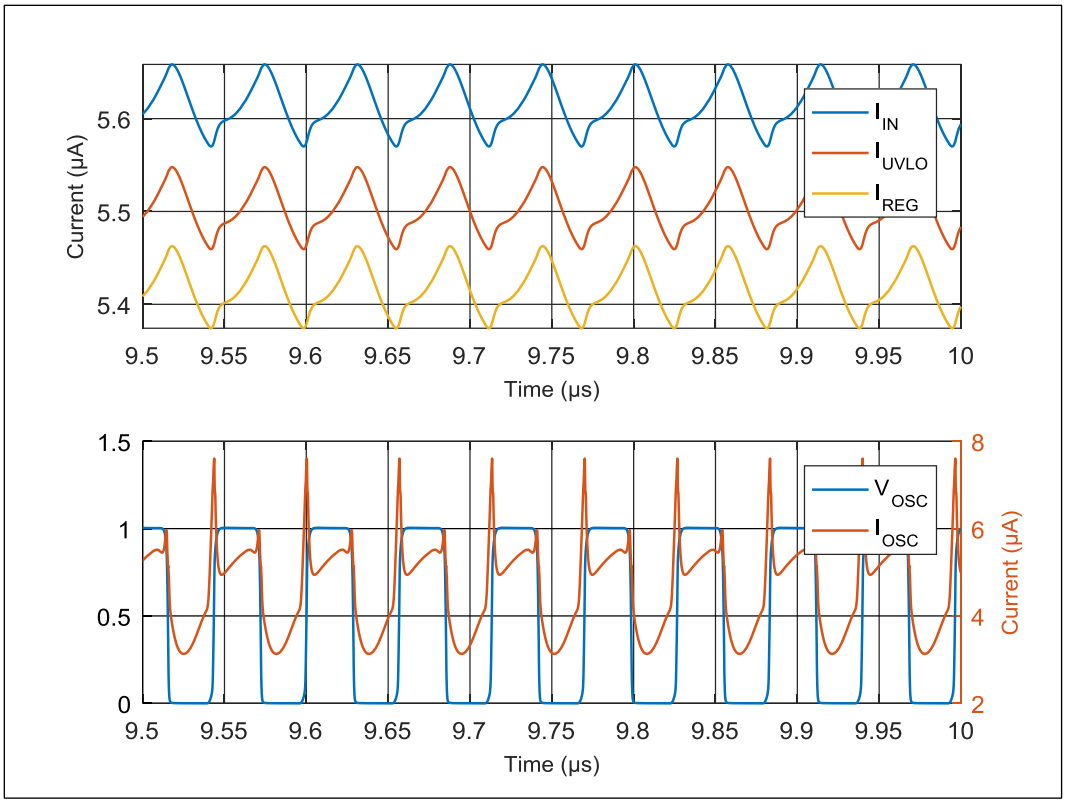

Figure 6.8 - DC steady state currents

currents when the system is running. Current I_{IN} is the total current drawn from the supply. I_{UVLO} is the current going through the UVLO block. Most of the current going into the UVLO circuit is passed directly to the regulator, whose input current is plotted as I_{REG}. The difference between I_{UVLO} and I_{REG} is the quiescent current of the UVLO. This was measured as 84.5 nA in section 5.2.1. Notice that the oscillator's switching current exceeds what is drawn by the regulator used to supply the oscillator. This is because the large 5 pF capacitor at the regulator output in Figure 3.15 supplies the switching current for the oscillator. The oscillation waveform V_{OSC} is included as a timing reference for the current ripples.

Summarily, the system draws an average of 5.61 µA during normal operation, which is less than the maximum 10 µA specified in the design parameters from section 2.2.

6.2. Layout Considerations

Using only device sizings, the approximate area consumption of the circuit can be determined. From Table 2.2, the voltage reference consumes 206 μm^2. From Table 3.4, the linear regulator uses 3436 μm^2. The CSVCO's transistors in Table 4.2 use an area of 13.1 μm^2. The RF-DC rectifier devices in Table 5.1 consume another 10,595 μm^2. The UVLO circuit in Table 5.2 uses 343 μm^2. Lastly, the wake rectifier in section 5.4 uses 16,776 μm^2. This sums to a total area of 31,369 μm^2. As discussed in section 2.1.4, the total area available is 800x800 µm, or 640,000 μm^2. Thus, there is plenty of area available for probe pads, additional bypass capacitors, and wiring needed to interconnect all devices.

The minimum dimensions for a probe pad is REDACTED. Probe points will be placed at the nodes listed in Table 6.1. There are a total of 14 points. Using the minimum probe pad size, this consumes REDACTED. If the dimensions are increased to REDACTED to make probing easier, this increases to REDACTED, which still leaves sufficient space for wire routing and extra bypass capacitors.

Table 6.1 - Probe pad locations

Subcircuit	Node Name	Description
Subthreshold Voltage Reference	V_{GBIAS}	Bandgap current mirror bias
	V_{REF}	Voltage reference output
Undervoltage Lockout	V_{UVLO}	UVLO output
	V_{COMP}	Comparator output
	$V_{UVLO-FB}$	Comparator feedback pin
	$V_{UVLO-TAIL}$	Differential pair tail voltage
1 V Linear Regulator	V_{LDO}	Regulator output
	V_{ERR}	Error amplifier output
	V_{REG-FB}	Error amplifier feedback pin
	$V_{REG-TAIL}$	Differential pair tail voltage
Current-Starved Voltage-Controlled Oscillator	V_{OSC}	Oscillator output
	V_{MIRROR}	Current mirror bias point
Wake Rectifier	V_{WAKE}	Wake signal
Inductive Rectifier	V_{DC}	Rectifier output

CHAPTER 7: CONCLUSION

An integrated circuit was designed using IBM's 130 nm process in support of Cal Poly's active lens contact lens project. The circuitry necessary for performing biosensor measurements include a current-starved voltage-controlled oscillator, 1 V regulator, undervoltage lockout circuit, and a subthreshold voltage reference for biasing. Additional RF-DC rectifiers are also included for recharging the thin-film battery that powers the IC, and for waking the system from a low-power sleep state. Because no sensor design has been completed, the chip is designed assuming that a capacitance pressure sensor will be used based on previous works in [10] and [11].

The subthreshold voltage reference outputs a 696 mV at the nominal 3.8 V battery voltage. It is operational across the entire voltage range of the battery with a line sensitivity of 2.32 mV/V. The original design draws 110 nA of quiescent current, but this rises to 161 nA after modifications for putting the other circuit blocks into a sleep state. For a 5 μAh battery, this gives 31 hours of standby power.

The 1 V linear regulator provides a steady, regulated supply voltage for the CSVCO downstream from it. The error amplifier and feedback circuitry draws 914 nA once it is pulled out of standby by the wake signal generated by the 2.4 GHz RF-DC rectifier. A large output capacitor ensures that there is not any significant ripple from the high frequency swings generated by the CSVCO, which oscillates from 14.3 to 71.7 MHz, depending on the sensor capacitance.

The UVLO circuit and the 13.56 MHz RF-DC rectifier regulate power to and from the Cymbet battery. The UVLO cuts off power when the voltage drops below 3.1 V, and features 100 mV of hysteresis such that it does not pass power until the voltage rises above 3.2 V. The battery can be recharged using 20 dBm of inductive power based on data presented in [13] and [14].

CHAPTER 8: FUTURE WORK

8.1. Verification of Integrated Circuit Design

Once fabricated, the IC performance needs to be verified before it can be encapsulated within a contact lens substrate. MOSIS provides unpackaged, bare dies, as well as dies packaged within a DIP package. Preliminary testing should be done using the pre-packaged dies. Evaluation of chip's DC performance can be done on a breadboard. This includes the output of the voltage reference, 1 V regulator, and functionality of the UVLO circuit. It may be possible to test the CSVCO on a breadboard, but it is likely that the parasitic capacitances will filter out or attenuate the higher output frequencies. It may be necessary to create a PCB, or even a simple "dead bug" style board on a copper substrate. It should be noted that previous contributors had issues with testing and verification due to a lack of proper equipment. With that said, it may be difficult to accurately measure the microamps and nanoamps of current drawn by the circuits for verifying the chip's power performance.

After verifying functionality with benchtop power supplies, the chip should also be tested when powered by the thin-film battery. Generally, the batteries come as bare dies that require wirebonding to form a connection. However, Cymbet has an evaluation kit available for the CBC005. The product number is CBC-EVAL-05B. It may be possible to evaluate the IC's power performance using the evaluation kit. Nonetheless, the bare batteries should be wirebonded directly to the IC at some point to confidently claim that the two components are functional with each other.

Ultimately, the fabricated chip should be tested using the bare, unpackaged dies provided by MOSIS for best results. Probe pads will be included at several points in the layout for testing with a probing machine; these probe pads can also be used to inject signals or voltages to debug nonfunctional circuit blocks. One such probing machine is

available in the microfabrication lab in Building 41A. The lab is managed by Dr. Richard Savage and lecturer Hans Mayer, and can be accessed with their permission after passing a safety test. Future students who decide to continue this project should be encouraged to acquire access as they will likely require access to the fabrication equipment available in the lab. This is true even for students who are interested in other aspects of the project, such as encapsulation, sensor design, and antenna design.

8.2. Integrated Circuit Design Improvements

The most evident shortcoming in the design is the charge regulator in presented in 5.1.1. Because there are no transistors available with a sufficiently high voltage rating, the regulator is an open loop design using only passive devices. It may be necessary to switch to another process that features transistors with higher voltage ratings. Benny Ng's IC was designed using ON Semiconductor's C5N 0.5 μm process, which features transistors rated up to 5 V. MOSIS still offers the C5N process for educational purposes, so the project can still revert to the older process if desired.

If the design is verified to be functional, then the probe pads can be removed which would free up significant chip area. This opens the potential for a battery-less design as done in [9]. Their work uses a large 500 pF on-chip capacitance as a temporary power source that is charged using power scavenged from a 1.8 GHz signal used for backscatter communication. Figure 8.1 shows the capacitor dimensions needed to obtain

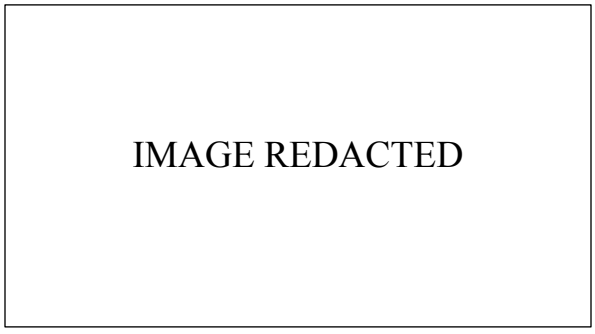

Figure 8.1 - Capacitor dimensions needed for 500 pF

a 500 pF capacitor in the 8RF process. The dimensions for a regular metal-in-metal MIMCAP and a dual layer MIMCAP would consume REDACTED, and REDACTED, respectively. If this is pursued, antenna efficiency may have to be improved to maximize the power scavenged.

8.3. External Measurement Recorder

Benchtop spectrum analyzers and RF synthesizers can be used during testing, but eventually a fully packaged external recorder needs to be designed. The recorder needs to transmit at the backscatter frequency with sufficient RF power, and feature an envelope detector to capture the reflected envelope as shown in Figure 4.1. The designer should reference the backscatter performance discussed in section 4.1.2 as a starting point. The actual backscatter performance using the IC should also be evaluated prior to any design work.

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