VERIFICATION OF RECEIVER EQUALIZATION

BY INTEGRATING DATAFLOW SIMULATION

AND PHYSICAL CHANNELS

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COMMITTEE MEMBERSHIP

TITLE: Verification of Receiver Equalization by

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                                Channels

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ABSTRACT

Verification of Receiver Equalization by Integrating
Dataflow Simulation and Physical Channels
David Ritter

This thesis combines Keysight's SystemVue software with a Vector Signal Analyzer (VSA) and Vector Signal Generator (VSG) to test receiver equalization schemes over physical channels. The testing setup, "Equalization Verification," is intended to be able to evaluate any equalization scheme over any physical channel, and a decision-directed feed-forward LMS equalizer is used as an example. The decision-directed feed-forward LMS equalizer is shown to decrease the BER from 10^{-2} to 10^{-3} (average of all trials) over a CAT7 and CAT6A cable, both simulated and physical, for 1GHz and 2GHz carrier, and 80MHz data rate. A wireless channel, 2.4GHz Dipole Antenna, is also tested to show that the addition of the equalization scheme decreases BER from 10^{-5} to less than 10^{-5}. Then the simulation and equalization parameters (LMS step size, PRBS, etc.) are changed to further verify the equalization scheme. The simulated channel BER results do not always match the physical channel BER results, but the equalization scheme does decrease BER for both wired and wireless channels.

Then transistor-based equalization model is created using both HDL SystemVue components and blocks easily implemented by transistors. The model is then verified using HDL, Spice, and SystemVue simulation. Overall this thesis accomplishes its goal of creating a testing setup, Equalization Verification, to show that adding a given simulated equalization scheme in SystemVue can improve the quality of the link, by decreasing BER by at least an order of magnitude, over a specific physical channel.

Keywords: Equalization, Decision-directed, SystemVue, Vector Signal Analyzer, Vector Signal Generator, CAT7, CAT6A

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GLOSSARY OF TERMS

Term	Definition
VSA	Vector Signal Analyzer; In this thesis, VSA is typically referring to the M9391A Keysight 10MHz to 6GHz VSA
VSG	Vector Signal Generator; In this thesis, VSG is typically referring to the M9381A Keysight 10MHz to 6GHz VSG
Equalization Verification	The main testing setup for this thesis; a combination of a SystemVue Simulation, VSG output, physical channel, and VSA input to verify an Equalization Scheme
Equalization Scheme	A combination of hardware components (circuits) to implement equalization on a signal
LMS	Least Mean Squared; An algorithm used in equalization to calculate a channel's taps (see background chapter for more info)
Chipset	A combination of a transmitter and receiver to be used in combination; can be entirely in simulation, a physical chip is not required (but may be intended)
Link/Quality of Link	The flow of data from a transmitter to a receiver; the quality of the link is determined by the amount of correctly received data
Dataflow Programming/Modeling	A type of simulation that treats a signal as a set of data; can be used to model both time and frequency signals. This thesis uses Keysight's SytemVue software for all dataflow programming. See background chapter for more information
SystemVue	A dataflow programming software used to model communication systems
Channel Tap Values /Weights	The coefficients of the sampled time domain representation of the channel impulse response; often the number of taps are specified and are according to the system sample rate
Baseband Signal	A signal that has not been upmixed into a higher RF band
RF Signal	A signal that has been upmixed into a higher RF (Radio Frequency) band;
Complex Datatype	A dataflow programming signal that is used to represent an Baseband signal; represented in the time domain
Envelope Datatype	A dataflow programming signal that is used to represent an RF signal; represented in the frequency domain
HDL	Hardware Description Language; A programming language used to represent physical transistor logic gates and implement hardware; typically referring to VHDL or Verilog
IC	Integrated Circuit

1. Introduction

Verification of transmitter and receiver chipsets is often performed entirely in simulation prior to fabrication. Design tools, such as the Cadence Suite along with a transistor process model file, are able to simulate a chipset's behavior across a simulated channel [1]. For different applications, the simulated channel will be modeling the corresponding channel type, such as wired or wireless. The s-parameter file for the channel will be imported into the simulation and the chipset's functionality will be confirmed in an analog simulation using that s-parameter file [1]. However the channel requirements can change during production for wired systems [2] or the typical location can be unknown in the case of a wireless system [3]. Because of the variability of the channel, it can be difficult to simulate a channel correctly and completely. This thesis presents a solution to currently unknown or constantly changing channel requirements for a given transmitter/receiver chipset by integrating Keysight's SystemVue software with Keysight's Vector Signal Generator (VSA) and Vector Signal Analyzer (VSA).

1.1 Current TX/RX Verification Procedures

Present day transmitter and receiver verification procedures include importing the s-parameter model of the channel and running channel simulations completely in simulation [1]. Figure 1-1 shows the S21 and S11 characteristics of the channel being examined for equalization requirements.
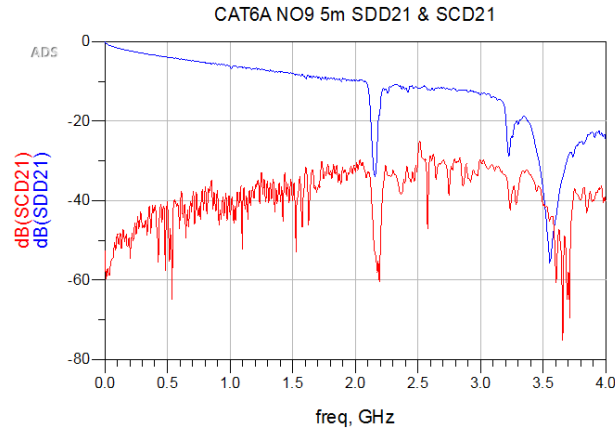
Figure 1-1: Example of SDD21 and SDD11 Cable Measurements (differential S21 and S11)

Because the channel requirements can change from the beginning of the product development cycle with wired systems [4], or the channel location is currently unknown for the end user [3] a static channel definition does not provide a complete, real world result and may mislead designers into designing to an exception and create less than stable products. A verification scheme that can be used to test physical channels using behavioral models could be of use when testing applications where complete verification of a link chipset is required.

1.2 Current Channel Modeling and Verification

S-parameter modeling captures the frequency response of the channel which includes the entire channel model. However there are imperfections due to a finite number of measurement points when creating the s-parameter file. Being able to output a signal with known characteristics of the final transmitter across the actual channel, and received with the same characteristics as the receiver, the equalization scheme can then be more accurately verified. An s-parameter file is less accurate than using a physical channel because of the finite precision of an s-parameters measurement. Another reason an s-

parameter file is less accurate is that the channel or channel requirements can change so the s-parameter file is no longer representative of the channel.

Some of the current software that runs s-parameter simulations with integrated circuits includes Cadence Virtuoso AMS, CST STUDIO SUITE, and Keysight's Advanced Design Systems. These software will perform a signal integrity analysis using integrated circuit models (transistor or functional) and s-parameter blocks. Keysight's SystemVue software, used in this thesis, can also perform integrated circuit simulations with s-parameter files, which will be compared to the results using physical cables.

1.3 Previous Keysight Designs and Work

Keysight's SystemVue Software includes many example designs, including interfacing between the Vector Signal Generator (VSG) and Vector Signal Analyzer (VSA) in the same chassis. The added benefit this thesis brings is to integrate both interfacing with a VSG and VSA in one design for the purpose of verifying a receiver's equalization scheme. To verify the equalization scheme, the transmitter and receiver are examined as part of the same system (point-to-point network) allowing the designer to use SystemVue to verify any communication system within the equipment's specified range.

This thesis's design relies on the interface's impedance between the equipment and physical channel in order to model the transmitter and receiver properly. Keysight's Vector Signal Generator (VSG) at the system's transmitter can fix its output impedance at 50 ohms (Rout) and the capacitance low enough to be negligible (Cout) [5]. This

models an ideal transmitter which is often able to be realized in a design [6]. The receiver, or Vector Signal Analyzer (VSA), can also control its input impedance to 50 ohms (Rin), and negligible input capacitance over the equipment's specified bandwidth and frequency range [5]. The VSA can thus model a realistic receiver [6].

1.4 Motivation for Integrating Dataflow Simulation and Physical channels

In high speed links, verification is often performed in simulation and then separately in hardware once the chipset has been fabricated. Because high speed links are application dependent, i.e. the chipset is designed for a specific set of channels, it would be more desirable if the current channel requirements could be tested before taping out. Currently design simulation practices include measuring the channel's s-parameters and then importing into simulation. Because during the time it takes to design and fabricate a chipset, the channel requirements could change and there is no guarantee that the chipset will match the final environment unless the s-parameters are constantly being updated. Another benefit to importing s-parameters is that the simulation can be used by customers of the chipset before the chip has been manufactured to test with given cables, which will provide a more extensive scope of a model than the existing timing IBIS models for transmitter and receiver combinations. The system designed in this thesis bridges the gap between channel simulation and hardware testing by allowing simulations using actual cables in order to allow for designs to be successful in fewer iterations saving time to market, cost, progress and frustration. In this thesis, the results from this proposed verification solution will be compared against the simulated s-parameter solution.

1.5 Types of Channels and Conditions for Testing

This thesis will evaluate a decision directed feed forward (FFE) least mean squared (LMS) equalizer on the channels and frequencies identified in (Table 1-1). Both wireless and wired channels will be used to evaluate the equalizer's bit error rate (BER) under the conditions identified in Table 1-1 and presented in Chapters 4 and 5.

Table 1-1: Parameters to sweep for Systems Lab BER testing

Cable/Channel	Carrier Freq	Input Data/BW	PRBS Input	Number of Samples	Number of Taps	Step Size
CAT7 3ft	1,2 GHz	80Mz	7	12801	10	0.0001
CAT7 15ft*	1,2 GHz	(80MHz), 50Mz	4,(7),12	1601,(12801), 25602	4,(10)	.001, (.0001)
CAT7 25ft	1,2 GHz	80MHz	7	12801		0.0001
CAT6A 3ft	1,2 GHz	80M	7	12801	10	0.0001
CAT6A 15ft	1,2 GHz	80M	7	12801	10	0.0001
CAT6A 25ft	1,2 GHz	80M	7	12801	10	0.0001
Dipole Antenna (2.8 GHz)	2.8 GHz	(80M), 50MHz	7	12801	10	0.0001

*control value in parenthesis

1.6 Overview of Thesis

This thesis integrates transmitter and receiver simulation with physical channel testing in an effort to allow for validation of a pre-silicon equalization scheme (Figure 1-2).
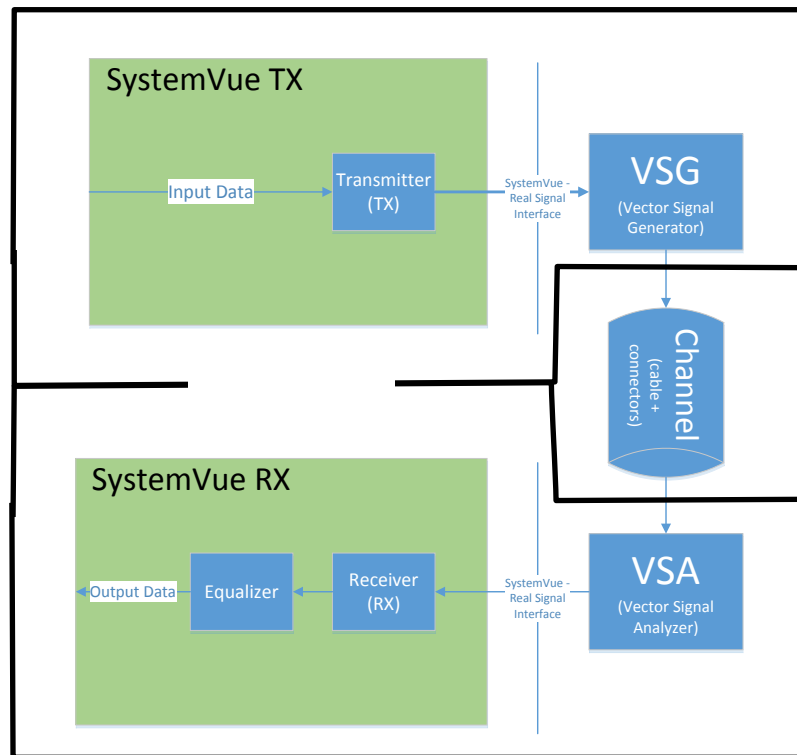
Figure 1-2: Proposed Equalization Verification – TX/RX in Simulation - Physical channel; Keysight chassis includes all inside black outline

The proposed and implemented design includes the transmitter and receiver entirely in simulation, while the channel is a physical / physical channel. The equalizer, with a given equalization scheme, is under test to be verified for the given channel.

This thesis document's main goal is to show how an equalization scheme can be evaluated using SystemVue and physical cables, and then evaluate an equalization scheme using the methods described. This thesis document will first provide the necessary background information. Then the Equalization Verification design will be

presented and outlined. The setup and design sections includes how to setup the VSG and VSA equipment, how to setup the SystemVue simulation, how to integrate the simulation with the equipment, how to evaluate the entire system setup, and finally how to evaluate the equalization scheme under test.

After the methods to verify an equalization scheme are presented in Chapter 3, an equalization scheme will be tested in Chapters 4 and 5 with both wired and wireless channels respectively. The equalization scheme under test is decision directed feed forward LMS, but other equalization schemes could be evaluated due to the flexible nature of the Equalization Verification setup. Once an equalization scheme has been verified, with BER testing in Chapters 4 and 5, the accuracy of SystemVue's dataflow modeling for an equalization scheme are compared to a spice model of an equalization scheme. This comparison is to increase the reader's confidence in SystemVue's dataflow modeling and the validity of the Equalization Verification setup presented in this thesis.

Then in Chapter 6, SystemVue is used to produce a more transistor-based equalization scheme using both LTSpice and HDL modeling to show the possibilities of the software and future uses for integrating dataflow programming, such as SystemVue, into the integrated circuit design process. Finally the conclusion of the thesis and future work is presented in the last chapter.

2. Background

This chapter will give background on equalization techniques, dataflow modeling, and Keysight's equipment, SystemVue, and other relevant background information for this thesis. This chapter will present topics required to understand this thesis beyond an undergraduate electrical engineering level.

2.1 Equalization Overview

Equalization is the technique of compensating for a signals attenuation or distortion across a channel [7]. A variable filter is used to compensate for the channel, and the variable filter is set based on the channel's output and the desired received signal (Figure 2-1).
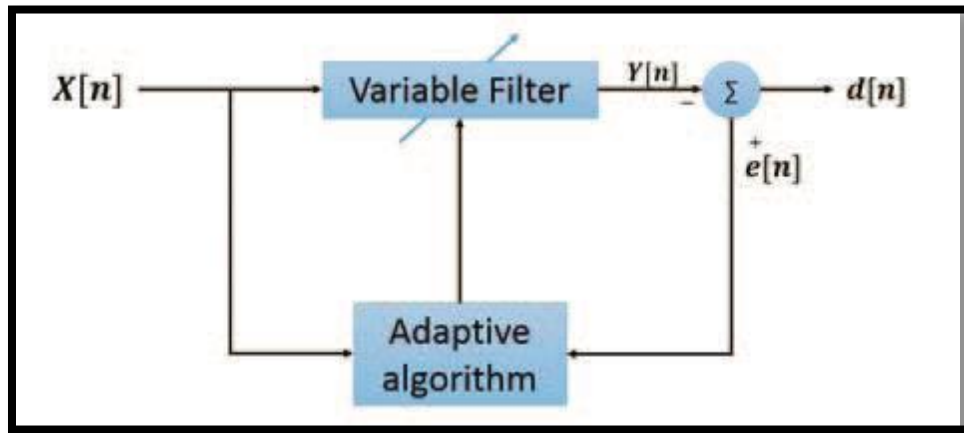
Figure 2-1: Variable filter based on an adaptive algorithm; building block of equalization [8]

The variable filter, or adaptive filter, is the building block of equalization because it performs a summation of delayed and scaled inputs or outputs to produce the output based on the filter coefficients (taps) calculated by the adaptive algorithm. In this thesis the adaptive algorithm is the Least Mean Squared algorithm (LMS), the variable filter is a feed-forward equalizer (FFE), and the d[n] desired signal is decision directed. Each of

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these components including feed-forward, decision-directed, and LMS will be outlined in this section.

2.1.1 Feed-forward Equalizer

Equalization techniques can be either linear, FIR with delayed inputs, or non-linear, IIR with delayed outputs, and are often performed in combination on both the transmitter and receiver side of the link [9]. This thesis only examines a linear FIR feed-forward equalizer (FFE) that uses delayed and scaled versions of the input as seen in Figure 2-2.
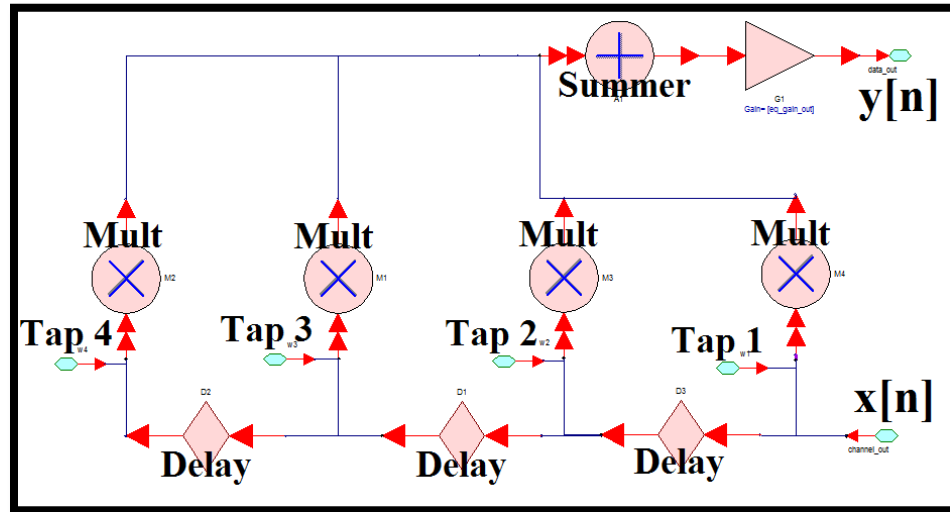
Figure 2-2: 4-Tap Feed Forward Equalizer (FFE) implemented in SystemVue software

2.1.2 Receiver Side Equalization

Transmitter equalization "predistorts" the signal according to a-priori knowledge about the signals distortion, and existing information about the channel. Receiver equalization recovers the original signal properties by comparing the current output signal (y[n]) to a known reference value, often called the desired signal (d[n]), to create an error signal (e[n]) [7]. That error signal along with the channel output is used to calculate the channel

tap coefficients. For both TX and RX equalization and both linear and nonlinear equalization, a channel's impulse response is calculated and compensates for the channel by using a series of coefficients to delayed versions of the signal [9]. This thesis only evaluates a receiver side feed-forward equalizer.

2.1.3 Decision-Directed Equalization

A receiver-side decision directed equalizer is a linear equalizer that uses a decision signal as the "desired" signal (d[n]). A decision directed equalizer takes the received signal (y[n]), makes a comparison, or "decision," to a correct output value (1 or 0) and uses the error between the decision and the output to update the adaptive filter's coefficients (Figure 2-3).
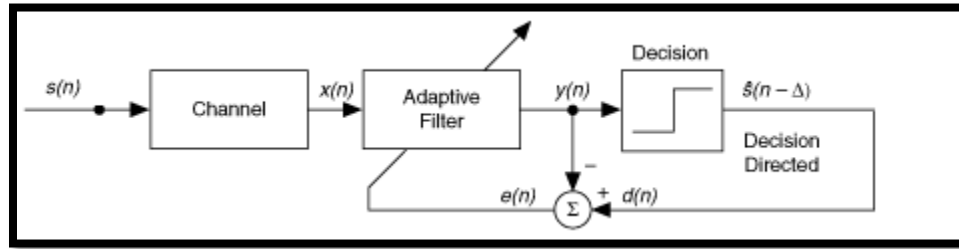
Figure 2-3: Decision Directed Equalization; adaptive filter based on output comparator (decision) [8]
This is opposed to an equalizer that uses a training sequence or blind mode to calculate the desired signal (Figure 2-4).
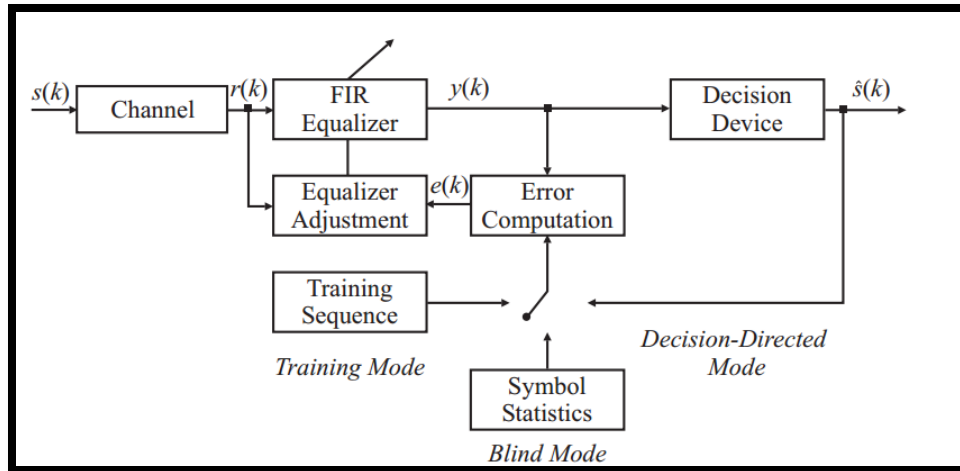
Figure 2-4: All Components of an Adaptive Equalizer; Note the different ways to calculate the desired signal, such as "decision-directed mode" [10]

A decision directed equalizer is often used on the receiver side of the link since it does not require the transmitter's input to operate, and this characteristic lends itself well to this thesis's design. This thesis only examines a decision directed feed-forward equalizer (FFE) which uses delayed versions of the input signal to perform equalization on the received signal (x[n]). The LMS algorithm is used to calculate the filter tap coefficients for this thesis's equalization scheme and is explained in the following section.

2.1.4 LMS Algorithm

The Least Mean Squared (LMS) algorithm is used in this thesis to calculate the channel coefficients for the adaptive filter to be used to compensate for the channel [8]. LMS uses the input and error signal (from a determined desired signal) to calculate the channel coefficients. Variable definitions are found in Equation 2-1.

Equation 2-1: Variable Definitions for LMS Algorithm

$$y(n) = \sum_{k=0}^{M} w_k(n)x(n-k)$$

$$X(n) \triangleq [x(n), x(n-1), ..., x(n-M)]^T$$

$$W(n) \triangleq [w_0(n), w_1(n), ..., w_M(n)]^T$$

$$y(n) = W^T(n)X(n), \quad n \geq 0$$

$$e(n) = d(n) - y(n)$$

$$= d(n) - W^T(n)X(n)$$

In the LMS algorithm, the filter coefficients W[n] are updated based on Equation 2-2. The LMS algorithm converges to the filter tap coefficients that track the desired signal which creates an all-pass filter when combined with the channel.

Equation 2-2: LMS Filter Coefficient Algorithm from input x[n] and error e[n] [7]

$$W(n+1) = W(n) + \Delta W(n)$$

$$\Delta W(n) = 2\mu e(n)X(n)$$

$$W(n+1) = W(n) + 2\mu e(n)X(n)$$

As seen in Equation 2-2 the filter tap coefficients, W(n), are updated only according multiplication and adding of the input x[n] and the error signal e[n] which allows for reduced hardware. The step size, μ, is constant, so the only signal multiplication is from e[n] and x[n]. The LMS algorithm is used extensively for hardware implementations for filter tap coefficient calculations. The recursive least squared (RLS) algorithm is an alternative to the LMS algorithm. The main differences lie in that the RLS algorithm

converges faster but requires more computational effort. Therefore the LMS algorithm is used in this thesis.

2.1.5 Chapter 2.1 Conclusion

As mentioned before, this section explained what a decision directed feed-forward LMS equalizer is and that it is used in this thesis because it can be implemented on the receiver side of the link (decision directed), is a linear operation (feed-forward), and requires limited hardware (LMS).

2.2 Dataflow Modeling

Dataflow modeling is used throughout this thesis with the SystemVue software, and is a type of behavioral modeling that is at a higher abstraction level than circuit level modeling. Dataflow modeling makes use of efficient and fast simulation times for large designs. The voltage and current calculations of spice models are left behind in order to expedite simulation times, so each value at a node in between blocks (at a given time) represents a voltage. Dataflow modeling lends well to high frequency design where voltage and current are directly related, and when combining digital and analog domain computations. Dataflow modeling also can perform functions in the frequency domain, around a given carrier frequency, for fast high frequency simulations.

An example of a dataflow design can be seen in Figure 2-5, which shows an input voltage, a modulation scheme, a filter, and a sink to display the spectrum.
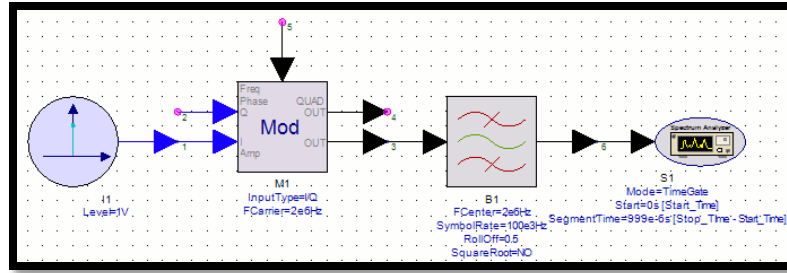
Figure 2-5: Dataflow modeling in SystemVue example

The dataflow modeling software only requires one connection and the data only flows in the direction of the arrow. SystemVue is simulation software to create and simulate dataflow programming. SystemVue has a similar programming and modeling style of Simulink and LabView software where a block's input must receive data before it performs an operation of the data, and outputs to its output node. As an example in Figure 2-5, the data port of the "Mod" block will only perform a modulation on its data input once the previous block has provided the data to its input. Once the data has been received on the "Mod's" input, the block performs its intended function on the data (modulation in this case) and outputs to its output node where the data will travel to whatever blocks are connected to the same node (in this case the filter block).

2.3 Keysight Tools: SystemVue, VSG, VSA, and Integration

Keysight's SystemVue is a dataflow modeling software designed for baseband and high frequency simulations [11]. SystemVue includes an "envelope" datatype that requires a center/carrier frequency and the frequency components around the center frequency [12]. The bandwidth of the signal is equal to the sampling rate of the system. As an example, Figure 2-6 shows the spectrum of a signal with a 1 MHz sample rate. The envelope datatype has a bandwidth equal to the sample rate, which is 2MHz in Figure 2-6.

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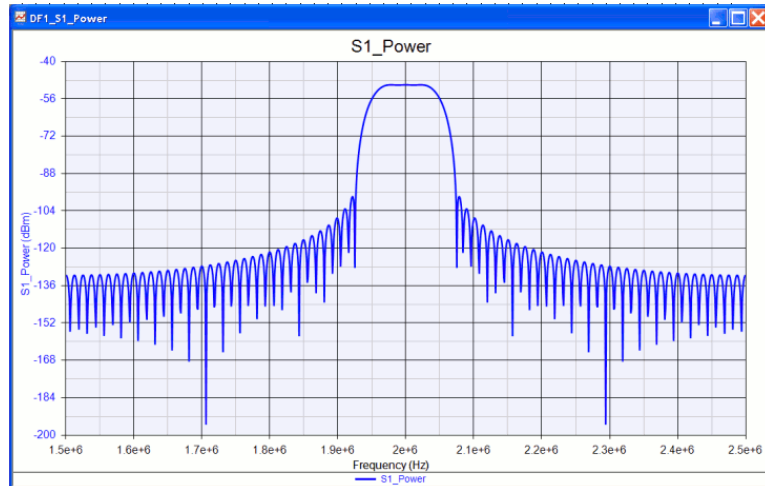
Figure 2-6: Envelope datatype power spectrum example

The envelope datatype lends well to high frequency simulations that operate in the upper bands, so high sampling rates are not required when operating in only a small portion of the upper bands [12]. This is a result of the simulation treating the envelope datatype as a baseband signal about a center frequency, which emulates an RF signal about the center frequency. SystemVue also treats complex data types like IQ data signals. The real portion of the variable corresponds to the "I" portion of the signal, and the complex portion of the variable corresponds to the "Q" portion of the signal [12]. The complex datatype allows for efficient computation of frequency domain calculations.

SystemVue can be used to create dataflow schematics, run simulations of the schematics, graph outputs, set variables, and even program [12]. A typical workspace view of a SystemVue design can be seen in Figure 2-7.
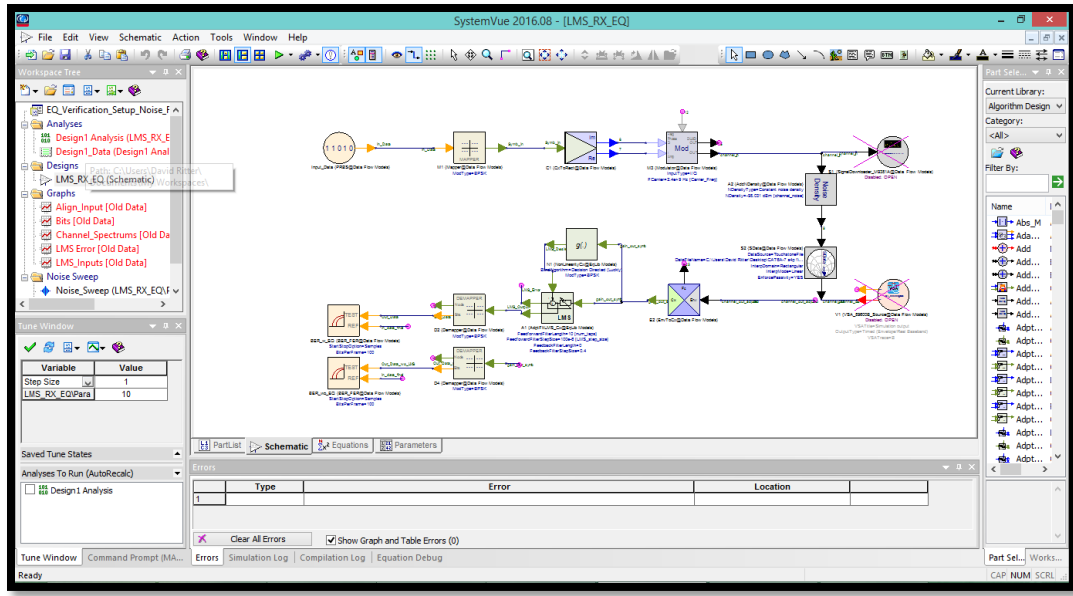
Figure 2-7: A Typical Workspace Design; the main schematic can be seen in the main window

Keysight's Vector Signal Generator (VSG) can take a recorded waveform and output it continuously. A SystemVue block exists to interface with the VSG in order to take a SystemVue simulation, record a sequence of voltages and then output the voltages through the VSG. The M9381A VSG is used in this thesis for the verification of equalization setup. It can output from 1MHz - 6GHz with a 160MHz bandwidth. The M9381A VSG is appropriate for this thesis because of its large frequency range and relatively high data bandwidth. Specifically for the wireless application, this VSG is highly flexible and can cover most frequency ranges including most ISM bands (below 6GHz).

Keysight's Vector Signal Analyzer (VSA) reads an input signal over a given frequency range. A SystemVue block exists to interface with the VSA 89600 software in order to import a recorded waveform into SystemVue for processing. The VSA 89600 displays the VSA's input waveform and provides an interface between the VSA and SystemVue.

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The M9391A VSA is used in this thesis for the verification of equalization setup, which can read from 1MHz - 6GHz with a 160MHz bandwidth.

Both the VSG and VSA are located in the same Keysight Chassis as seen in Figure 2-8. The VSG and VSA are composed of three different modules, and share a frequency reference of 10MHz.
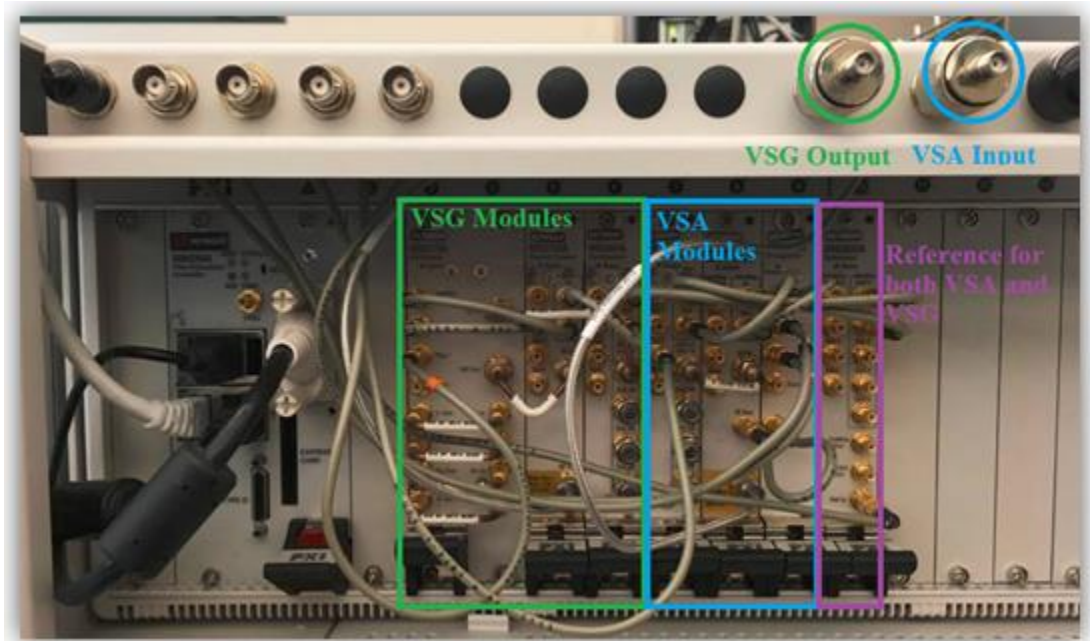
Figure 2-8: Keysight Chassis Containing M9381A VSG (green) and M9391A VSA (blue); modules shown for each VSA and VSG, and reference shared by both VSA and VSG

SystemVue is gaining widespread use in the Wireless application field for testing transmitters and receivers separately. Keysight has provided example designs with the integration of SystemVue and the VSG, and SystemVue and the VSA, but not all three together. This thesis integrates SystemVue, the VSG, and the VSA to perform verification on a given equalization scheme, which is the novelty of this paper.

2.4 Communication Channel Modeling

A communication channel is the medium that a signal passes through from the transmitter to the receiver [13]. A simple communication channel can be modeled as an addition of random white Gaussian noise to a linear time invariant (LTI) filter [13]. This thesis uses the simple communication channel model as seen in as seen in Figure 2-9.
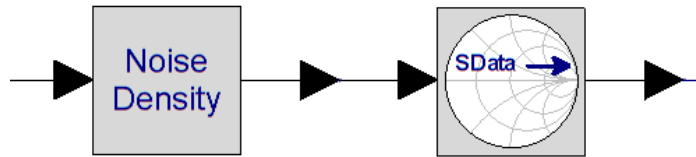
Figure 2-9: Simulated Channel SystemVue blocks;

includes both an added noise density block and s-parameter block (LTI filter)

The additive white Gaussian noise (AWGN) causes a random addition of noise to the transmitter signal, and the LTI filter attenuates different frequencies causing inter-symbol interference (ISI) on the transmitted signal [14]. Channel attenuation of different frequencies can result in ISI in the time-domain [15]. As an example, a low-pass filter (which is often representative of a communication channel) can cause the time domain version of a pulse to have less sharp transitions, causing the bit to "bleed" into the next bit (Figure 2-10).
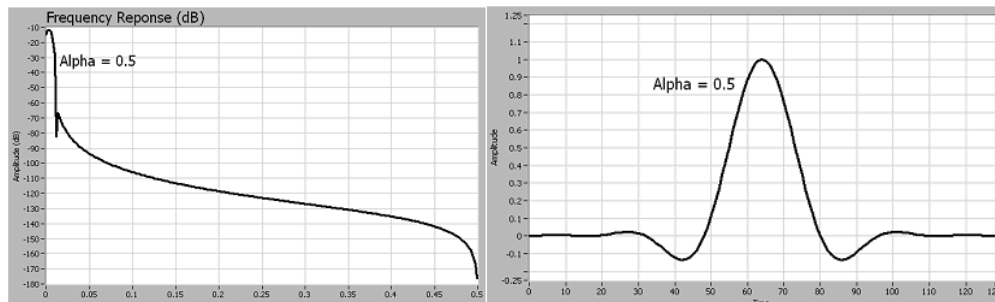
Figure 2-10: Inter-symbol Interference; pulse goes through frequency response above, to obtain time

domain above [15]

Both the channel AWGN and LTI filter can cause bit errors. A system's equalization scheme should prevent bit errors (decrease BER) by effectively undoing the LTI filter of the channel, and thus creating an all-pass filter overall [16]. However, the equalization does not prevent the AWGN, which also causes bit errors. Equalization should improve the BER of the link, by reducing inter-symbol interference, even when the noise power of the AWGN is increased [14], as shown in the BER vs. Eb/N0 graphs presented throughout this thesis.

2.5 Channel Modeling using S-parameters

S-parameter files provide a convenient and packaged way to represent the reflection and transmission properties of an RF system component. The "scattering" parameters include the attenuation (for passive components) reflected back (S11 and S22), transmitted through (S21 and S12), on all the ports specified.

The LTI filter portion of a communication channel can be modeled using s-parameters over a given frequency range [13]. Common wired channels have a low pass characteristic for the transmission (S21 and S11) and a high pass characteristic for reflected (S11 and S22). This is a result of conduction losses dominating loss at low to mid-range frequencies (100MHz – 2GHz) proportional to $1/f$ and dielectric losses dominating loss at mid-range to high frequencies (>2GHz) proportional to $1/f^2$ [17]. The exact frequency where the type of loss dominates is determined by the material, length, and make of the cable. The switch from conduction ($1/f$) to dielectric loss ($1/f^2$) can be seen in Figure 2-11.
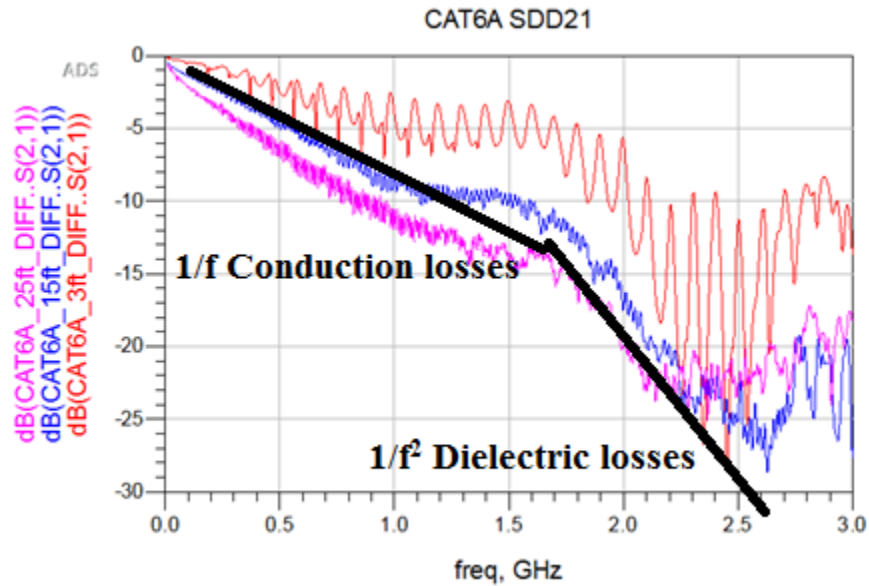
Figure 2-11: Conduction and Dielectric losses in SDD21 (differential S21) for lengths of CAT6A cables;

Dielectric losses dominate loss at ~1.5GHz

2.6 Antenna Path Loss Calculation

An Antenna Path Loss can be calculated from Friis's Free Space Equation as seen in Figure 2-12 [18].

$$P_r = P_t G_t G_r \frac{\lambda^2}{(4\pi d)^2}$$

- G_t and G_r are the transmit and receive antenna gains
- λ is the wavelength
- d is the T-R separation
- P_t is the transmitted power
- P_r is the received power
- P_t and P_r are in same units
- G_t and G_r are dimensionless quantities.

Figure 2-12: Friis's Free Space Equation for Antennas [19]

An alternative way to write Friis's formula, solving for path loss in dB:

Path Loss (dB) = 20*log$_{10}$(distance) + 20*log$_{10}$(frequency) + 20*log$_{10}$(4π/c) − G$_{TX}$ - G$_{RX}$

If the distance, frequency, medium of propagation, and gain of both the transmitting and receiving antenna are known, then the path loss under those conditions can be calculated. For this thesis, the distance is fixed, the frequency is known, the propagation is through free space, and the gains of both TX and RX antennas are known. Therefore the results of Friis's formula can be compared to the measured path loss of the S21 s-parameter measurements made on the Vector Network Analyzer (VNA).

An example calculation from this thesis is:

For a 2.4GHz carrier frequency, 0.4m distance, propagating through free space, with TX and RX antennas with 2dBi gain:

Path Loss = 20log(0.4m) + 20log(2.4E9) + 20log(4*pi / 3E8) − 2dBi − 2dBi

= -7.959dB + 187.6dB − 147.558dB − 2dBi − 2dBi

= 28.087 dB = *25.37 V/V*

2.7 Bit Error Rate Testing and Link Performance

Bit error rate (BER) testing is often used to assess if any bit errors have occurred during transmission of data across a link [17]. The BER is displayed as a ratio of bit flips to correctly transmitted bits as seen in Equation 2-3.

Equation 2-3: Bit Error Rate (BER) Formula

$$BER = \frac{Bit\ Errors}{Total\ Transmitted\ Bits}$$

If a BER of an equalization scheme is smaller than transmission without the equalization scheme, then the equalization scheme has improved the quality of the link. Many other factors such as signal to noise ratio (SNR or Eb/N0) effect the bit error rate and are often displayed against each other as seen in Figure 2-13 [20]. BER vs. Eb/N0 curves will be calculated from simulated channels by sweeping noise power throughout this thesis.
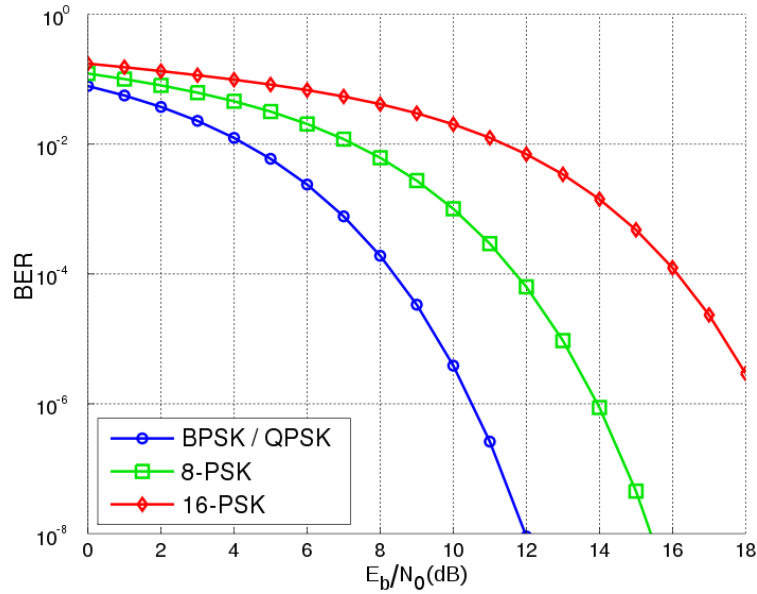
Figure 2-13: BER vs. Eb/N0 (SNR) for different modulation schemes; this thesis uses BER as a comparison of a link with and without an equalization scheme [17]

This thesis primarily uses BER as a reference to compare a link with and without a given equalization scheme in order to determine if the equalization scheme improved the quality of the link. BER is the primary benchmark used in this thesis, since this thesis only uses BPSK signaling. The BER is calculated by comparing the received bit stream to the transmitted bit stream in SystemVue. The bits must be aligned in SystemVue (within the delay bound) in order to accurately calculate the BER of the link.

3. Design of Equalization Verification using Dataflow Simulation

This thesis examines how to perform verification of a transmitter/receiver (TX/RX) chipset while in the design stages using an actual physical channel. More specifically, the chipset's equalization, modeled in SystemVue, is evaluated in a system using simulated and physical, wired and wireless channels.

The Equalization Verification system for physical channels includes (as outlined in Figure 3-1*):*

- A SystemVue simulation of the transmitter dataflow (behavioral) model to match the same transistor level design made on such platforms as Cadence and other IC design software

- A module in SystemVue to interface to the Vector Signal Generator (VSG model M9381A), to transmit a recorded waveform generated from simulation

- A VSG that outputs to an existing physical channel on the TX side

- A channel, wired or wireless, that the signal/data is transmitted over

- The Vector Signal Analyzer (VSA model M9391A) that receives the data on the RX side of the channel

- A module in SystemVue to interface with the VSA, to import the signal via a recorded waveform into SystemVue
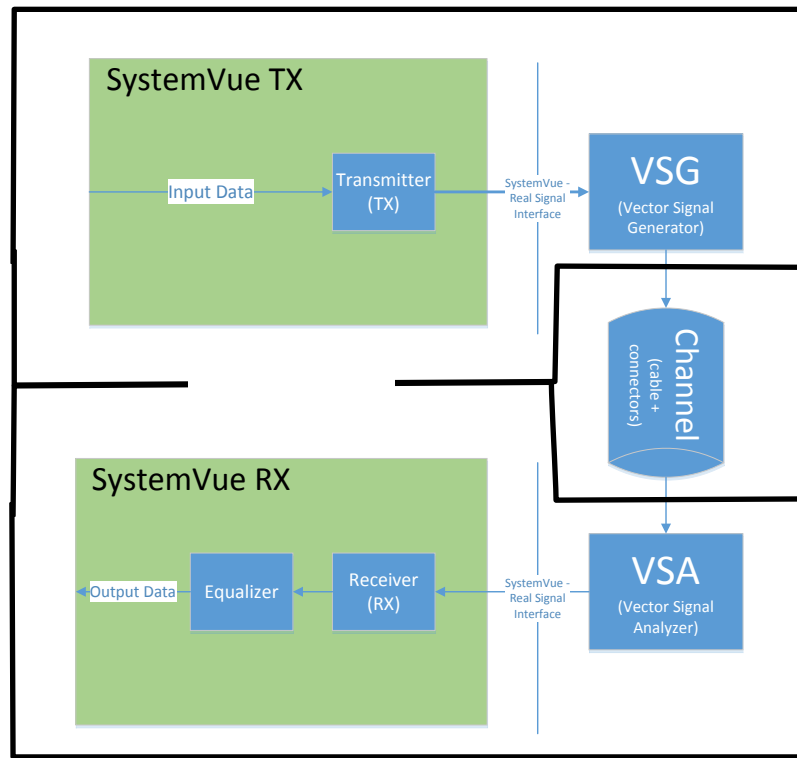
Figure 3-1: Block Diagram of Dataflow modeling with Physical channel for Equalization

The equalization is the primary target of this system's verification since it is easily isolated when simulation and a physical channel are separate. The equalization scheme is easily isolated in SystemVue since it is not dependent on the receiver interface, and can be compared against received data that is not equalized. The equalization scheme can be evaluated based on this setup with a transmitter and receiver during the design stages, before they have been fabricated. This thesis examines speeds up to 2GHz with both wired and wireless channels. However this verification method could be further used with any channel, and across different carriers and data rates, as long as it's within the specifications of the VSA/VSG set in accordance with SystemVue.

Before the detailed explanation, as an overview, here are the steps of the Equalization Verification testing procedure of an equalization scheme across a physical channel:

1. Create the SystemVue dataflow model of equalization scheme to be tested.

2. Insert the equalization scheme into the SystemVue Simulation (blue receiver box of Figure 3-5).

3. Determine and set the frequency and data rates for the Equalization Verification SystemVue simulation.

4. (Optional) Take S21 s-parameter measurements of the channel (Chapter 3.4).

5. (Optional) Run the Equalization Verification SystemVue simulation across the simulated channel with the SData block, disconnect VSA/VSG; record the BER results with and without equalization.

6. Test the equalization scheme with a physical channel, with the determined testing parameters (see Chapter 3.5); make sure to disconnect the SData simulated channel in SystemVue; record the BER results with and without equalization

7. Compare the results of the simulated vs. physical channel to verify the testing setup (Chapter 3.4); then compare the BER results with and without equalization to verify that the equalization scheme improved the link quality (Chapter 3.5).

This chapter intends to walk the user through the Equalization Verification setup and the procedures for how to evaluate an equalization scheme. This chapter will cover the VSA/VSG equipment, the SystemVue simulation, the interface between the VSA/VSG and SystemVue, the channel testing setup, procedures on how to evaluate the testing setup, and procedures on how to evaluate an equalization scheme.

3.1 VSA and VSG Equipment Setup

The Keysight MS9381A Vector Signal Generator (VSG) takes a recorded waveform from the SystemVue Simulation and repeatedly outputs it at the simulation period, based on the number of samples and sample rate [21]. An output trigger connected to the VSA from the VSG allows the Keysight MS9391A to synchronize with the VSA receiver. The VSG can create waveforms by setting individual frequency powers over a specified bandwidth, around a given center frequency. A baseband waveform is first created by the VSG and then upmixed to produce the final RF output waveform, with the parameters set by the user.

A recorded waveform can be uploaded to the VSG that contains frequency components about a center frequency. The frequency range of the VSG MS9381A is 1MHz to 6GHz with a 160MHz maximum bandwidth about the center frequency specified. The period of the waveform, frequency resolution, and bandwidth are set in the SystemVue simulation that produces the recorded waveform to be output to the VSG (.wfm filetype). The VSG then takes that recorded waveform and plays it continuously, with the VSG output trigger signifying the beginning of the waveform. The VSG is composed of all of its module components including a Frequency Reference (10MHz), Frequency Synthesizer, Digital Vector Modulator, and Source Output (see Figure 2-8) [21]. All the VSG components interface with the computer that runs SystemVue via PXIe. The VSG output power can also be selected in the SystemVue module (see Chapter 3.3 for VSG setup). See [22] for more information on the M9381A VSG.
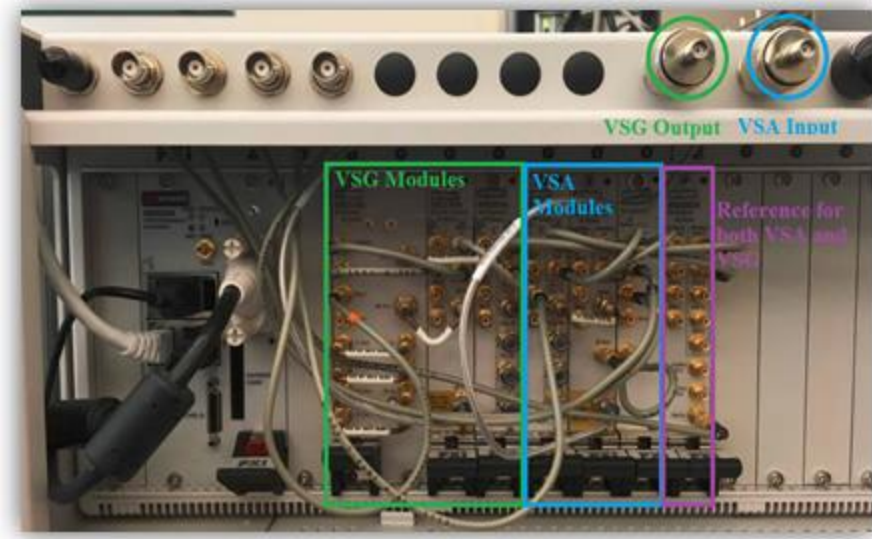
Figure 3-2: Keysight Chassis Containing M9381A VSG (green) and M9391A VSA (blue); modules shown for each VSA and VSG, and reference shared by both VSA and VSG

The VSG output is connected to the desired channel under test. As seen in Figure 3-3 the VSG is connected to a connector board which interfaces with a CAT7 cable via a RJ45 connector, for wired channel testing. The signal runs through the channel under test and is read in through the Keysight MS9391A Vector Signal Analyzer (VSA). The signal is continuously displayed using the VSA 89600 Software and triggered off of the VSG's trigger.

Figure 3-3: System Integration of Physical channel, VSG, and VSA

The MS9391A VSA is monitored completely with the VSA 89600 software [23]. The waveform is recorded and imported into SystemVue via the 89600 SystemVue block, and the SystemVue simulation is set paused automatically in order to allow the user to adjust the VSA input waveform before SystemVue imports the recorded waveform [24]. The VSA includes four modules including a downconverter, digitizer, frequency synthesizer, and frequency reference (see Figure 2-8) [5]. The VSA determines a center frequency for the input signal and measures the frequency amplitudes and phases around the center, with the same range and frequency specifications as the VSG of 1MHz to 6GHz with a max bandwidth of 160MHz. See the [25] for more details on the M9391A VSA.

3.2 Simulation Setup

The SystemVue simulation is used to verify the receiver's equalization scheme. From a high abstraction level, SystemVue has a transmitter to produce a waveform, a channel that the waveform travels through, and a receiver to receive and perform equalization on the waveform.
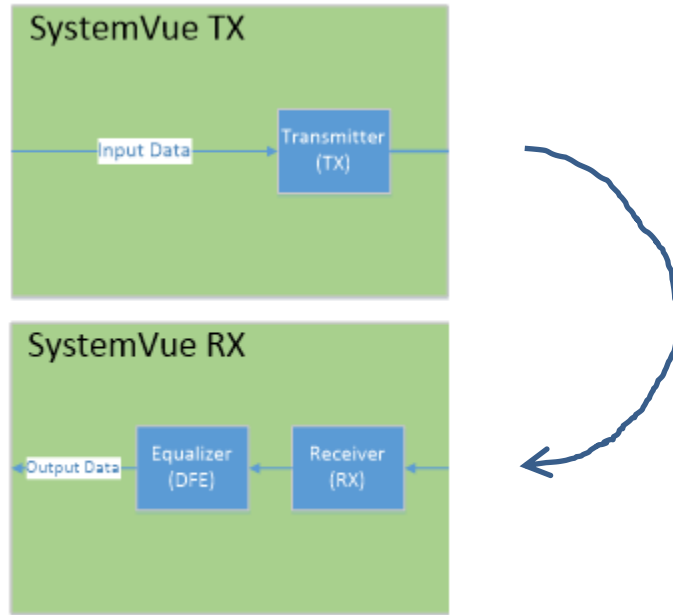
Figure 3-4: Representation of SystemVue Transmitter and Receiver

In the transmitter, SystemVue provides the data stream, modulation (NRZ), and upmixing. In the receiver, SystemVue down converts, equalizes, demodulates, and compares the output data to the input data (BER).

Keysight's SystemVue software is used for its dataflow simulation and interfacing with the VSG and VSA. As shown in Figure 3-5, this thesis's Equalization Verification SystemVue setup includes creating a desired waveform (Transmitter block, green box), downloading the waveform to the VSG via the VSG SystemVue block (VSG block, orange box), importing the received waveform from the VSA via the VSA 89600

SystemVue Block (VSA block, orange box), performing equalization on the received signal (Receiver block, blue box), and calculating BER results for the equalized signal and for the non-equalized received signal (BER blocks after Receiver).
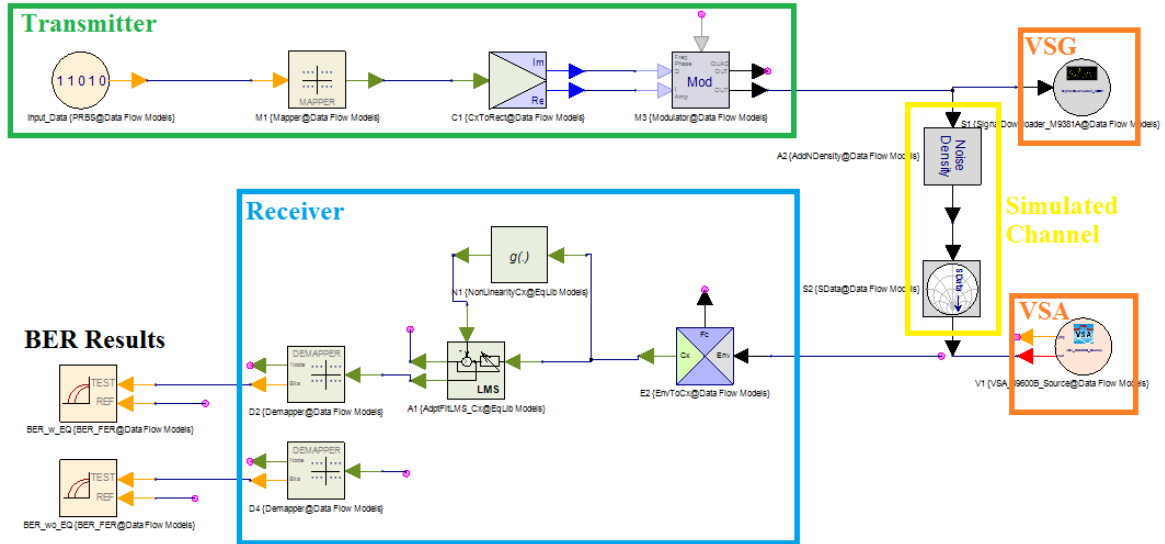
Figure 3-5: SystemVue Simulation: with S-parameter channel and VSA/VSG

(S-parameter channel and VSA/VSG not to be used at the same time)

Figure 3-5 presents the main component of the Equalization Verification SystemVue Simulation that includes the transmitter, VSG interface module, simulated channel, VSA interface module, and Receiver. The Receiver block includes the equalization scheme to be verified, which in this case is the "LMS" block and "g(.)" block. The simulated channel (yellow box in Figure 3-5) is not intended to be used simultaneously with the VSA and VSG blocks. The simulated channel is mainly used for comparison of the physical channel under test (see Chapter 3.4 for simulated channel measurements). The physical channel to be tested is not shown in Figure 3-5, since SystemVue interfaces to the physical channel via the VSG and VSA.

The Equalization Verification SystemVue Simulation includes helper blocks to graph and measure data correctly (Figure 3-6). The delay and mapping blocks in Figure 3-6 are used for aligning the input and output data to correctly measure the bit error rate. For explanations of all of the blocks used in Figure 3-5, see Appendix A.
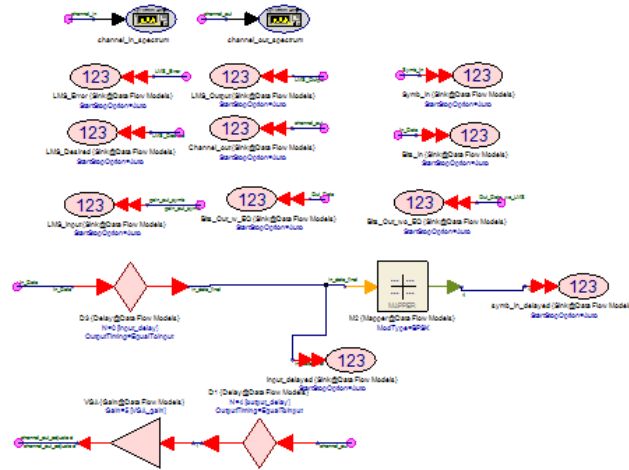
Figure 3-6: Helper blocks to graph data, and to set up delay for input and output data to match for BER measurements

SystemVue designs can also include equations to set variables/parameters [12]. This Equalization Verification SystemVue design includes the parameters in Figure 3-7 which are to be set depending on the testing conditions. The exact testing conditions will be outlined in Chapter 4 and 5 but can be adjusted to the user's application.

```
1    %%%%%%%%%%TX Setup%%%%%%%%%%
2    Bit_Rate = 80E6;
3    PRBS_Len = 7;
4    Carrier_Freq = 2.4E9;
5
6    %%%%%%%%%%RX Setup%%%%%%%%%%
7    VGA_gain = 35;
8
9    %LMS Param
10   num_taps = 10;
11   LMS_step_size = .0001;
12
13   %BER settings
14   input_delay = 139;
15   output_delay = 0;
16   BER_delay_w_EQ = 10;
17   BER_start_w_EQ = 10000;
18   BER_delay_wo_EQ = BER_delay_w_EQ;
19   BER_start_wo_EQ = BER_start_w_EQ;
20
21
22   %Power/Noise Equations
23   EbN0 = 29;
24   Mod_Power_dbm = 10;
25   Mod_Power_W = 10^( (Mod_Power_dbm-30)/10 );
26   Mod_Gain = sqrt(2*50*Mod_Power_W);
27   Eb_dbm = Mod_Power_dbm - 10*log10(Bit_Rate);
28   channel_noise = Eb_dbm - EbN0;
```
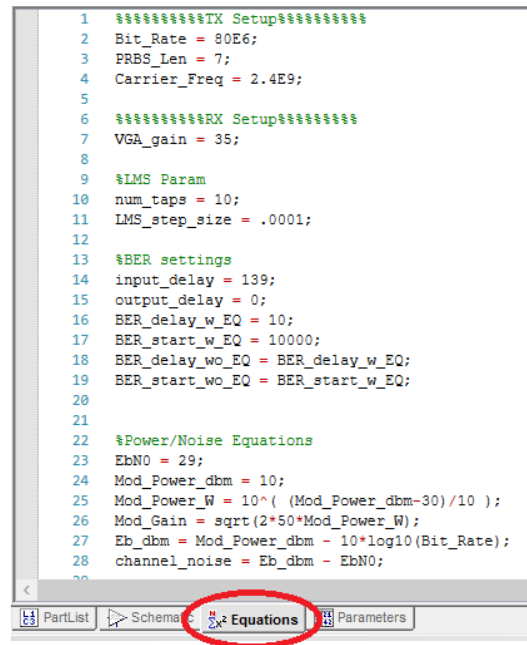
Figure 3-7: Equations tab in the Equalization Verification SystemVue design (navigate in main design by clicking equations)

The parameters set in the equations tab in Figure 3-7 correspond to the model parameters in the schematic portion of the design (Figure 3-5) [12]. The parameters that can be set are organized according to their placement in the design. The bit rate, PRBS length, and carrier frequency can be set for the transmitter. The VGA gain can be set for the receiver. The number of taps and step size can be set for the equalizer parameters (LMS). To align the input data to the output data, the input delay, output delay, BER delay bound, and BER start time can be set for BER measurements.

A behavioral model for the equalization scheme is created and tested in SystemVue in Chapters 4 and 5, and a transistor-based model for the equalization scheme is created and tested in SystemVue in Chapter 6. The transistor-based model in Chapter 6 is compared to transistor models in LTSpice and VHDL to verify the accuracy of the model. The equalization blocks, used in Chapter 4 and 5, are provided by SystemVue to implement a

32

simple LMS algorithm for calculating and applying the filter tap coefficients for the equalization of the channel.

3.3 Integration of VSG, VSA, and SystemVue

The Keysight M9381A Vector Signal Generator (VSG) takes the recorded waveform from the SystemVue simulation and repeatedly outputs it at the simulation period. The waveform from SystemVue is recorded with the following M9381A Downloader SystemVue block.

Figure 3-8: M93981A Downloader SystemVue Block

Once the waveform has been downloaded to the VSG, it will continue to output the waveform until another waveform is downloaded. The power levels of the VSG must be set properly as well (see Appendix B) [26].

The Keysight M9391A Vector Signal Analyzer (VSA) interfaces with SystemVue through the VSA 89600 software. The VSA 89600 software continuously displays the input signal to the VSA from the channel.
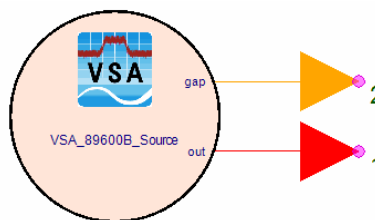
Figure 3-9: VSA 89600 SystemVue Source Block

The VSA 89600 SystemVue Source block allows the input signal to the VSA to be downloaded to the SystemVue simulation. The VSA 89600 Source block records and imports a waveform into SystemVue corresponding to the input waveform of the VSA. The VSA 89600 will then display the current incoming signal from the VSG across the physical channel. All other settings should match the simulation, refer to Appendix C for more VSA setup steps.

3.4 Channel Specific Setup

The channel is the main system component, other than the equalization scheme in SystemVue, to be changed from test to test. The channel is application dependent and either simulated or physical, wired or wireless. This section first present how to find the SystemVue simulation parameters and then will present the channel specific setup steps for a wired physical channel, wireless physical channel, and simulated channel (for both wired and wireless s-parameter data).

3.4.1 SystemVue Simulation Channel Dependent Parameters

One of the SystemVue simulation parameters to be set, which is channel dependent, is the receiver Variable Gain Amplifier (VGA) gain. The VGA gain is found iteratively in simulation and set to receive the best BER without equalization. The reason the VGA is included in this design is since most receivers have a VGA that is set depending on the channel in the link.

The input and output delay for the BER measurements are also set. The input delay is found for a simulated channel in SystemVue iteratively, and the output delay is set to non-zero so the BER delay bound can align to the proper input. See Chapter 4 and 5 for the input and output delay for BER measurements.

3.4.2 Wired Channel Setup

The wired channels for this thesis are either CAT7 or CAT6A and require two SMA to RJ-45 connector board to connect to the VSA and VSG as seen in Figure 3-10.
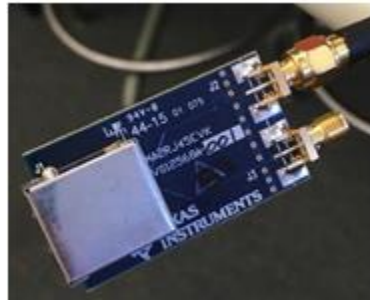
Figure 3-10: RJ-45 to SMA Connector Board made by Texas Instruments [27]

One connector board is connected to the VSG and one side of the cable under test. The other connector board is connected to the VSA and the other side of the cable under test (Figure 3-11).

Figure 3-11: Wired Channel Testing Connections [28]

The VGA gain for each physical cable and frequency conditions is confirmed with its S21 s-parameter graphs in Chapter 4.1.

3.4.3 Wireless Channel Setup

The wireless channel that is tested is with a TX and RX 2.4GHz WiFi Router Dipole Antennas with 2dBi of directional gain as seen in Figure 3-12 [29].
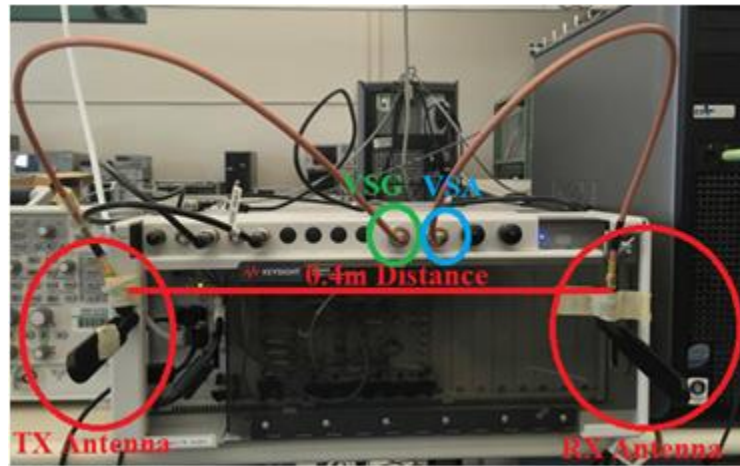
Figure 3-12: Wireless Channel Testing Setup

The VGA gain calculated using Friis's formula, for 2.4GHz carrier frequency and 0.4m distance for the 2dBi TX and RX antennas, is 25.37V/V. The VGA gain found iteratively is 35V/V for 80MBPS data and 30V/V for 50MBPS, which correlates to the Path loss calculated from Friis's formula [19].

3.4.4 Simulated Channel Setup

The simulated channel contains two blocks, the Noise Density block and the SData block (Figure 2-9). The noise density adds noise set by the noise power parameter. The SData, the s-parameter file is selected in the SystemVue SData block with the attenuation proportional to the S21 value at the given frequency (see Appendix A). The SData s-

parameter file is set depending on the simulated channel to test. The noise power in the Noise Density block is found based on the physical channel's BER measurements. The noise power is selected based on the closest BER with and without equalization for the physical channel BER measurements.
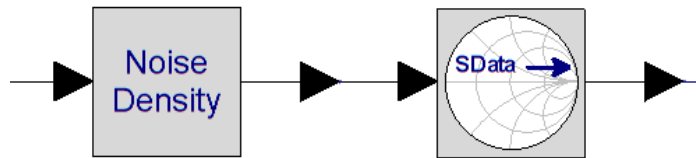
Figure 3-13: Simulated Channel SystemVue blocks; includes both an added noise density block and s-parameter block

The simulated channel's BER with and without the equalization scheme are used to identify if the Equalization Verification setup for testing physical channels is representative of the simulated channel. A simulated channel often only contains an additive white Gaussian noise component and the s-parameter channel file. The simulated channel BER measurements in SystemVue provide a comparison for the physical channel BER measurements. Also the noise power can be swept and a traditional BER vs. Eb/N0 graph can be found for further confirmation of the setup (see Appendix E for graphing steps).

3.5 Procedures to Evaluate Testing Setup

To evaluate an Equalization Verification Testing Setup with a physical channel, the BER results must be compared to the simulated channel BER results. The SystemVue simulated channel includes a noise density and s-parameter block to model the channel under test. If the SystemVue simulated channel using the s-parameter block, with a chosen noise power, matches the results from the SystemVue simulation outputting to the physical channel with the VSG/VSA, then the setup is valid.

The procedure to validate a setup using a physical channel includes the following steps in order:

1. Taking an s-parameter measurement of the channel to be tested (Figure 3-14)

2. Running a Simulated Channel Noise power sweep to graph BER vs. Eb/N0 using the SystemVue simulation with the s-parameter block, with the channel's s-parameter file (Figure 3-5)

3. Running the SystemVue simulation with the VSG/VSA, and outputting to the physical channel under test (Chapter 3.3 outlines in more detail); record the BER with and without equalization

4. Find the Simulated Channel Noise power that produces the same BER results with the simulated channel

5. Compare the BER of the Simulated channel (with added noise power) to the physical channel (compare with and without equalization)
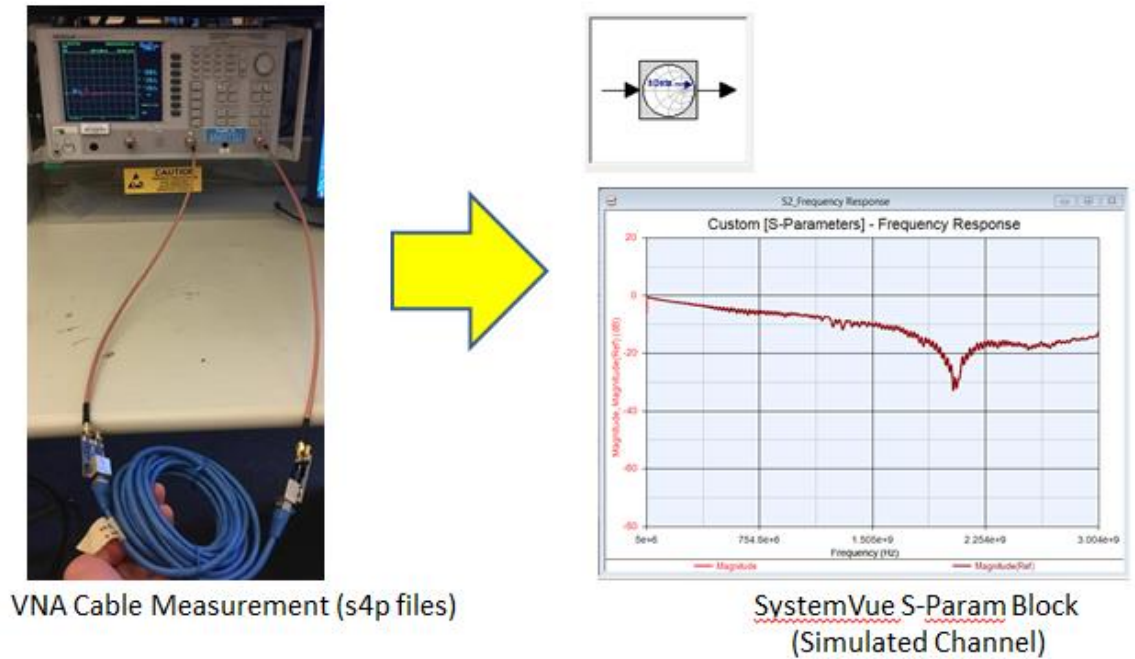
Figure 3-14: Physical Channel S-Parameters Capture and Simulation

The BER results are presented in the given channel chapters (Chapters 4 and 5) for setup evaluation. If the BER results for both with and without equalization match to the simulated s-parameter channel, then the testing setup is valid, and how closely the s-parameter file matches the physical channel's performance with the Equalization Verification setup. If both setups were completely accurate, there would be no differences between the s-parameter simulation and the Equalization Verification simulation using the physical channel. But the differences in BER between the two simulations may point to the inaccuracy of the s-parameter measurements or the Equalization Verification setup. This thesis will present both possibilities and make an educated conclusion for all channel measurements. In this thesis, testing setups are evaluated are for both wired and wireless channels. These testing setups will be evaluated in Chapters 4 and 5.

3.6 Procedures to Test an Equalization Scheme

An evaluation of the equalization scheme is the core of this research. An end user of the Equalization Verification setup would want to verify that their equalization scheme improves the quality of the link, reducing the BER, for a given channel. An end user would need to perform the following steps to perform an Equalization Verification for a given channel (same steps for wired or wireless channel) in order:

1. Connect the desired channel under test to the VSG and VSA

2. Run the SystemVue Simulation with the SystemVue VSG block on, VSA block off (Figure 3-15); see Chapter 3.3 for VSG setup
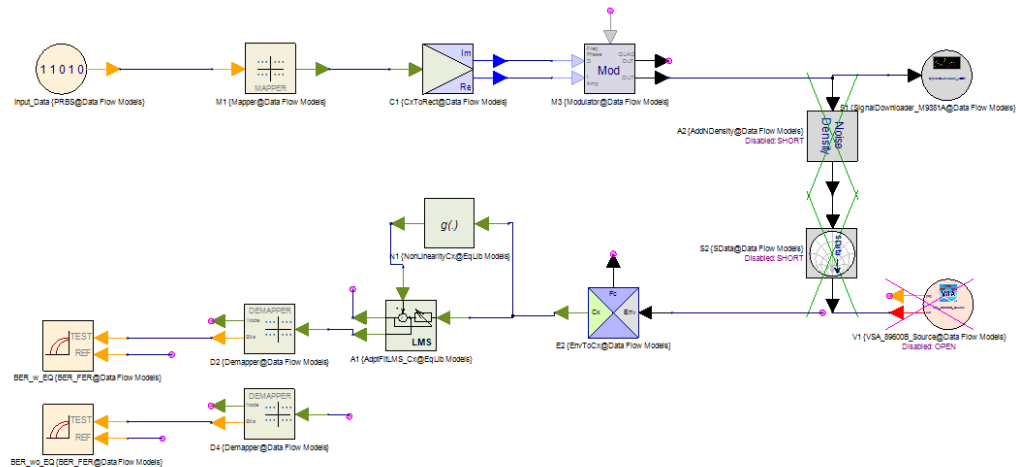
Figure 3-15: SystemVue Simulation with VSG on, VSA off, simulated channel short

3. Run the SystemVue Simulation with the SystemVue VSA block on, VSG block off (Figure 3-16); see Chapter 2.3 for VSA setup
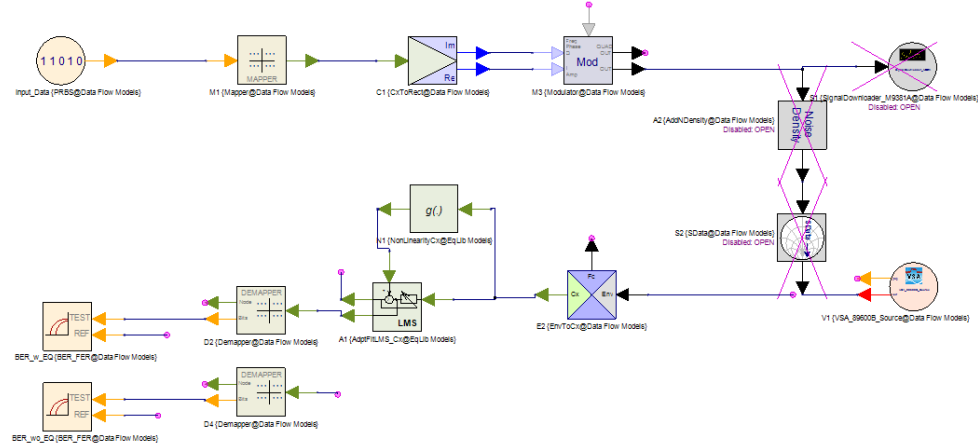
Figure 3-16: SytemVue Simulation with VSA on, VSG off, simulated channel off

4. Compare the BER of the simulation with and without the receiver's equalization scheme; BER recorded with BER SystemVue blocks recorded in the data section

These steps are necessary to setup the Equalization Verification SystemVue simulation that interfaces with the VSG and VSA to a physical channel. The equalization schemes that this thesis uses as an example include: 1) a decision directed feed-forward LMS equalizer using the SystemVue LMS block and 2) a decision directed feed-forward equalizer using SystemVue HDL blocks and more hardware portable blocks, designed as part of this research. The first is simply a behavioral model of a typical linear receiver equalizer. The second is a lower level (HDL) model that intends to more accurately represent the functionality of an integrated circuit's equalization scheme.

The SystemVue LMS blocks are used throughout this thesis as the control case for equalization verification. The SystemVue blocks are compared to a Spice model in Chapter 6.2 to demonstrate that the filter tap coefficients can be accurately calculated and equalize a channel, and in Chapter 6.3 to show the HDL model accurately represents a Spice circuit design.

The equalization scheme that this thesis will test (to verify this procedure is valid) is a decision directed feed forward LMS equalizer across wired channels in Chapter 4, wireless channels in Chapter 5, and implemented with SystemVue HDL blocks across a simulated channel in Chapter 6.

4. *Analysis and Results of Equalization Verification over Wired Channels*

This chapter will cover the analysis and results of testing this thesis's equalization scheme, decision directed feed forward LMS equalizer, over wired channels using the Equalization Verification Setup as described in Chapter 3. The wired channels to be tested are CAT7 cable 3ft, 15ft, 25ft [28] and CAT6A cable 3ft, 15ft, 25ft [30] for both 1GHz and 2GHz carrier frequency with 80MBPS baseband data. The CAT7 cable is rated up to 600MHz error free for wideband operation and the CAT6A cable is rated up to 500MHz error free for wideband operation. Therefore frequencies above 600MHz for CAT7 and 500MHz for CAT6A should require equalization for reduced bit errors. These two cables types are chosen as both an example case of the system performing as intended and because of the widespread use of CAT cables used with the Ethernet standard.

In this chapter, first the s-parameter measurements for each of the six cables will be presented. S-parameter results will be displayed graphically to show visually the different attenuation for different frequencies. The s-parameter files are used in SystemVue as the simulated channel. The Equalization Verification setup will be run with the simulated and physical channel to evaluate the accuracy of both setups. Then the equalization scheme will be evaluated based on its performance over the simulated and physical channels, and data will be presented on whether the link's performance improved with the addition of the equalization scheme.

4.1 S-parameter Measurements of Wired Channels

All measurements of the CAT7 and CAT6A cables are made using the RJ-45 to SMA board as shown in Figure 4-1 [27]. The connectors and board are included in all channel measurements and setups including the s-parameter measurements with the VNA and Equalization Verification setup. The connector board is made to emulate a typical connection on a PCB [27].

Figure 4-1: RJ-45 to SMA Connector Board made by Texas Instruments

The s-parameter measurements are made using the Anritsu MS4624B 10MHz – 9GHz Vector Network Analyzer (VNA) as seen in Figure 4-2.

Figure 4-2: Cable S-parameter Measurement setup using the Anritsu VNA

The procedure to measure the CAT7 and CAT6A cables and store the S2P (touchstone) file is as follows:

- Calibrate the VNA to desired range

- Connect the connector board and cable to the VNA

- Import the S2P file to the connected computer (via GPIB)

- Import the S2P to Keysight's Advanced Design System (ADS) Software

- Graph the S2P file

The CAT7 and CAT6A S21 s-parameter measurements are presented in Figure 4-3, Figure 4-4, Figure 4-5, and Figure 4-6 according the same frequency ranges used in the rest of Chapter 4.
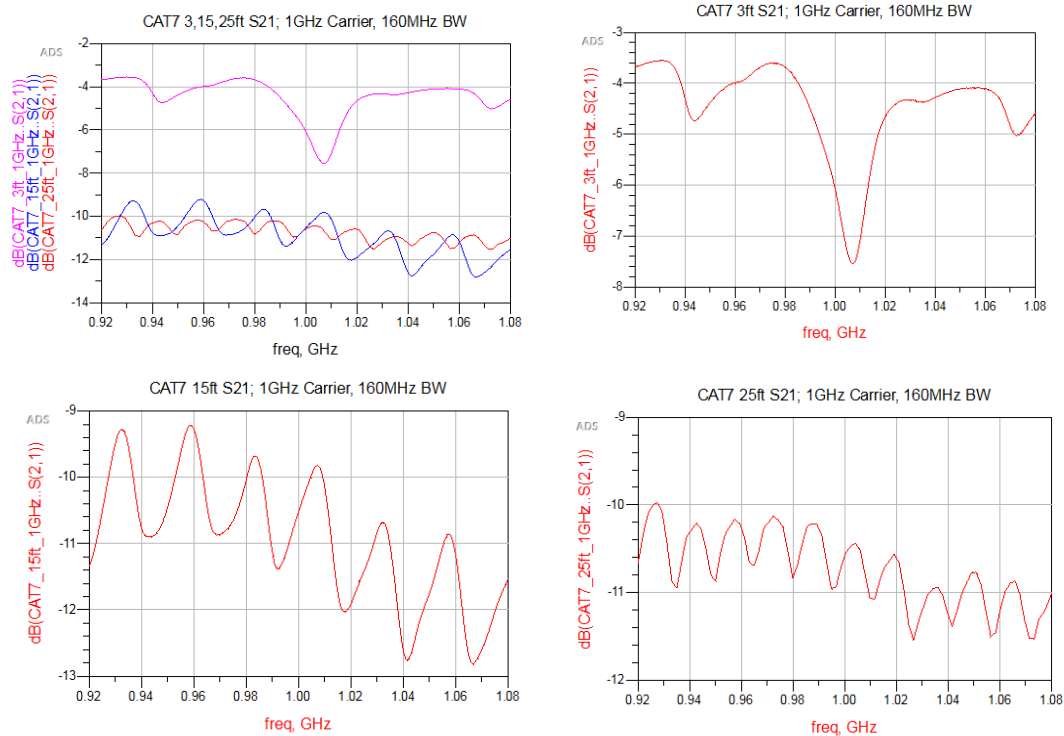
Figure 4-3: CAT7 S21 measurements for 1GHz center frequency and 160MHz bandwidth
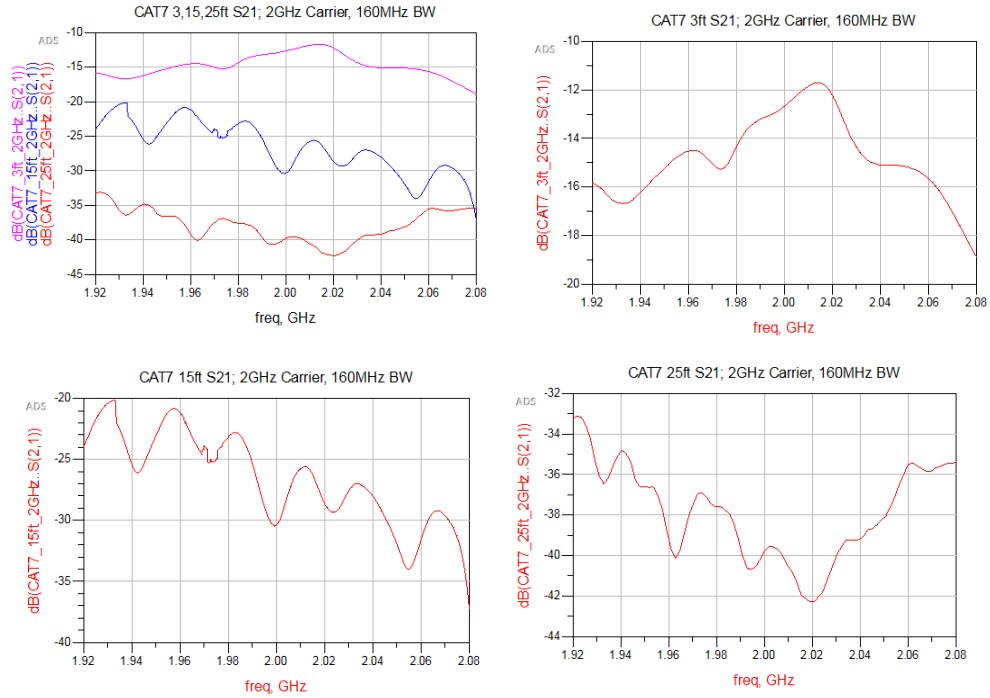
Figure 4-4: CAT7 S21 measurements for 2GHz center frequency and 160MHz bandwidth
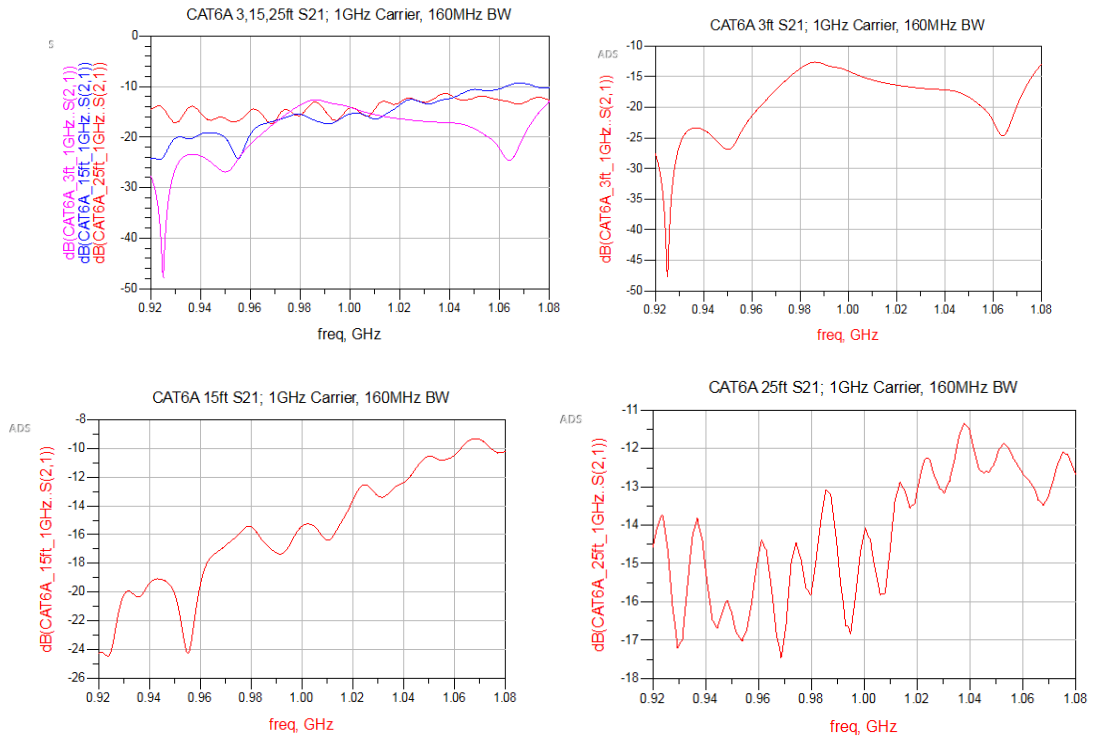
Figure 4-5: CAT6A S21 measurements for 1GHz center frequency and 160MHz bandwidth
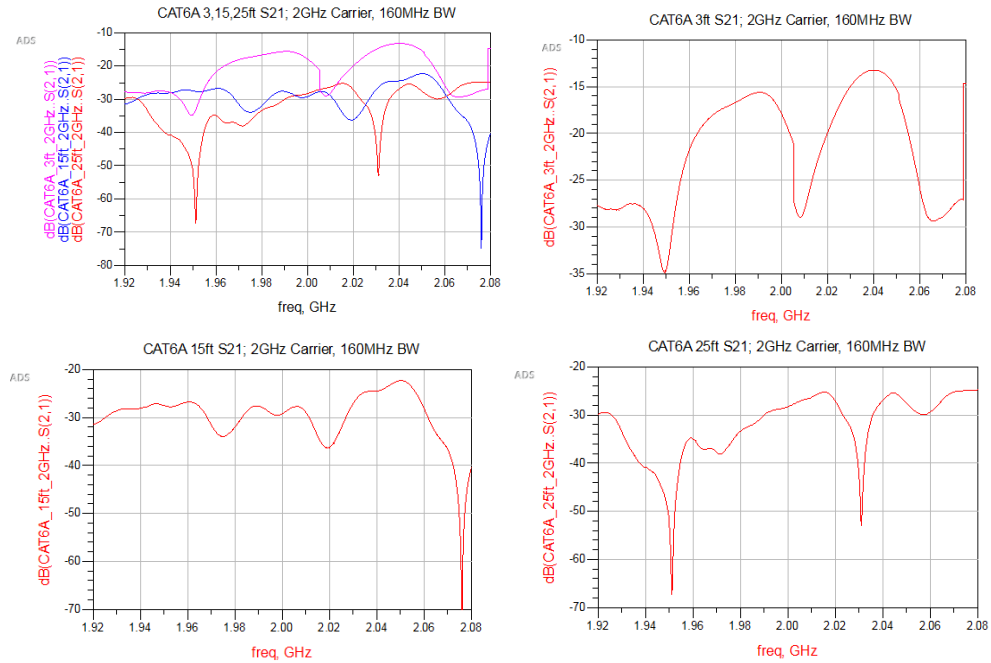
Figure 4-6: CAT6A S21 measurements for 2GHz center frequency and 160MHz bandwidth

The full range of the CAT7 and CAT6A from 10MHz to 3GHz is also presented in Figure 4-7 and Figure 4-8 for reference. The primary frequencies of interest are 1GHz and 2GHz center frequency with 160MHz bandwidth. This thesis intends to evaluate an equalization scheme over a different physical channel over different frequencies to cause different bit errors that must be corrected.
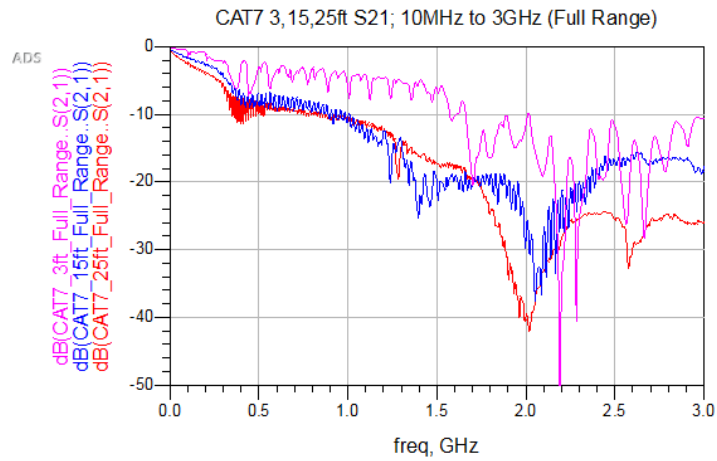
Figure 4-7: CAT7 S21 s-parameter measurement from 10MHz to 3GHz
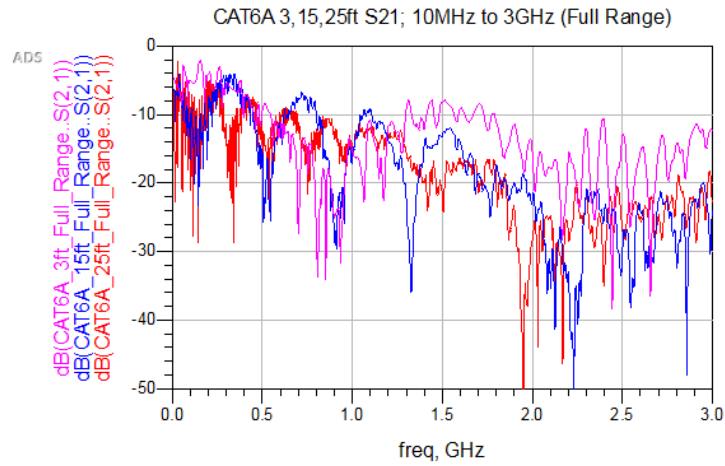
Figure 4-8: CAT6A S21 s-parameter measurement from 10MHz to 3GHz

The VGA gain as seen in Table 4-1 is determined roughly from the average value of the S21 loss for each cable set across the given spectrum. The S21 graphs also determine the contributed intersymbol interference that impacts the BER for each equalization verification test. A more detailed comparison of the S21 channel graphs will be examined in Chapter 4.5.

4.2 Equalization Verification Simulated Wired Channel Results

The simulated wired channel results are presented in this section which includes BER results for a specific noise power, and an Eb/N0 graph for a swept noise power. The S2P files for CAT7 3ft, 15ft, and 25ft and CAT6A 3ft, 15ft, and 25ft are used to simulate the BER results and Eb/N0 graphs.

4.2.1 BER Results for Measured Noise Level

The BER results in this section are found from the simulated cables (s-parameter files) with added noise. The noise power levels used in the simulated channel correspond to the noise level approximated when making the VSG/VSA measurements using the physical wired channels in Chapter 4.3.

Table 4-1: BER Results for Simulated Channels using Measured Noise Levels

Cable Type	Length	Carrier	Sample Rate	Input Delay	VGA Gain	Eb/N0 for Physical channel	BER w EQ	BER wo EQ
CAT7	3ft	1GHz	160MHz	1813	-5	no noise	0.00E+00	6.40E-02
CAT7	3ft	2GHz	160MHz	1867	-5	9	1.71E-03	2.70E-02
CAT7	15ft	1GHz	160MHz	779	-5	16	8.78E-05	2.38E-03
CAT7	15ft	2GHz	160MHz	1411	-30	no noise	0.00E+00	3.10E-02
CAT7	25ft	1GHz	160MHz	25	-5	17.5	0.00E+00	6.38E-03
CAT7	25ft	2GHz	160MHz	28	30	16	2.64E-04	5.71E-04
CAT6A	3ft	1GHz	160MHz	1540	-5	10	1.20E-02	3.90E-02
CAT6A	3ft	2GHz	160MHz	4097	5	25	0.00E+00	2.00E-02
CAT6A	15ft	1GHz	160MHz	1548	-5	3	9.10E-02	1.44E-01
CAT6A	15ft	2GHz	160MHz	620	30	no noise	0.00E+00	1.60E-02
CAT6A	25ft	1GHz	160MHz	128	-10	13.5	1.71E-03	1.40E-02
CAT6A	25ft	2GHz	160MHz	126	-20	17.5	1.27E-03	4.46E-03

The simulation results are presented in Table 4-1. The simulation parameters used for the results in Table 4-1 can be seen in Table 4-2.

Table 4-2: Simulated Cable BER Simulation Parameters

TX Setup				Simulation Setup					LMS Param		BER Settings	
Input Data	PR BS	Carr ier	BW	Sim Ti-me	Sam-ple Rate	Num Sam-ples	Time Spac-ing	Freq Res	# Ta ps	St-ep Si-ze	BER start	BER delay bou-nd
80 Mbps	7	1 GHz	160 MHz	80us	160 MHz	12801	6.25E-3 us	12.5 kHz	10	0.0 01	10E3	10

A few notes on the BER results for the simulated channel:

- The sample rate is chosen to be twice the Input data, which is twice the required Nyquist rate. This is to allow for a baseband pulse of BPSK without any special modulation.

- The BER settings the same for with and without EQ

- The BER recording start is at 10000, so the LMS has time to settle

- The BER delay bound is the amount of potential forward deviation in input vs. output bits for BER calculation.

The input delay corresponds to the s-parameter file's (S2P) simulated delay (group delay) and the VGA gain is found by iteratively changing the delay until the channel's input and output. This is an iterative process in includes changing the delay, looking at the graphs of the baseband input and output of channel, and adjusting the delay until they match. The VGA gain is used to emulate a Variable Gain Amplifier that auto adjusts to a correct fixed value in an increment of +/-5.

4.2.2 Eb/N0 Graphs

Eb vs. N0 graphs are simulated by sweeping noise power. See Chapter 2 for background on Eb/N0 graphs and how they relate to Signal to Noise ratio. Also see Chapter 3 for how to simulate the Eb/N0 graphs for each channel. The Eb/N0 graphs are used to identify the possible noise levels when measuring physical cables with the VSG and VSA, and to show that the equalization scheme works across different noise levels with the same channel.

All graphs use 160MHz sample, 80MBPS data rate, 32768 num samples, 10000 BER delay (unless specified otherwise). 1GHz and 2GHz carriers examined, VGA and delay specified in Table 4-1. The red curve is curve with equalization while the blue curve is without equalization for Figure 4-10 to Figure 4-15.
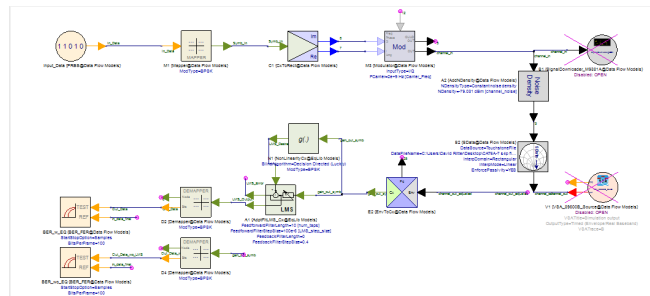
Figure 4-9: Eb/N0 simulation setup; with S2P channel and Noise density
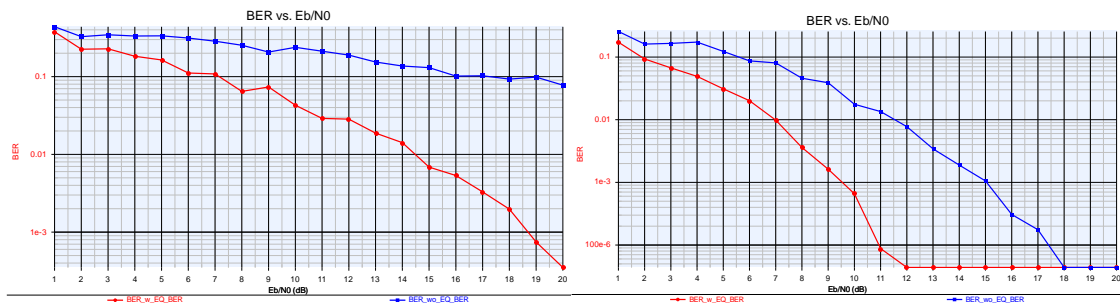
Figure 4-10: CAT7 3ft 1GHz and 2GHz (respectively) Eb/N0 graphs

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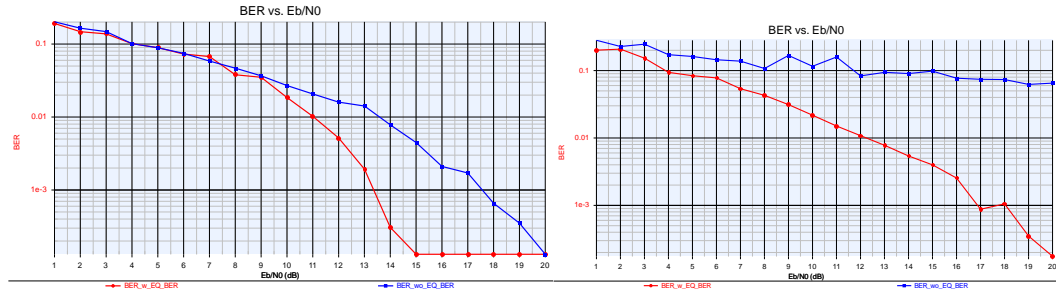
Figure 4-11: CAT7 15ft 1GHz and 2GHz (respectively) Eb/N0 graphs
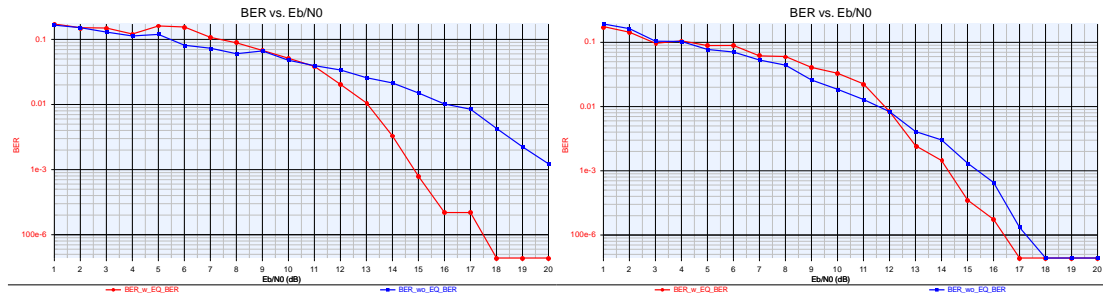
Figure 4-12: CAT7 25ft 1GHz and 2GHz (respectively) Eb/N0 graphs
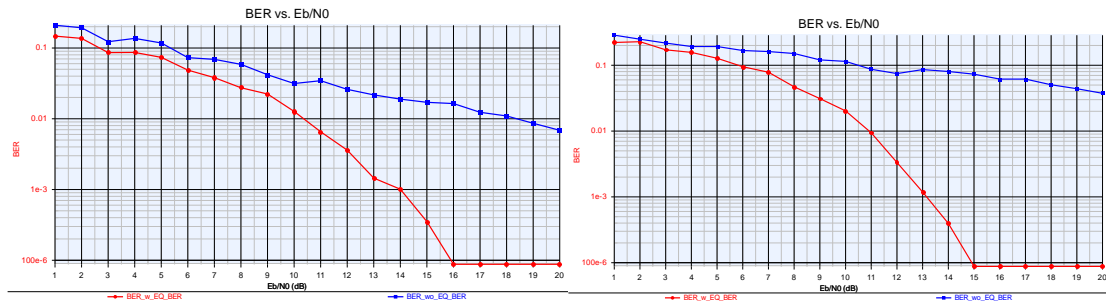
Figure 4-13: CAT6A 3ft 1GHz and 2GHz (respectively) Eb/N0 graphs
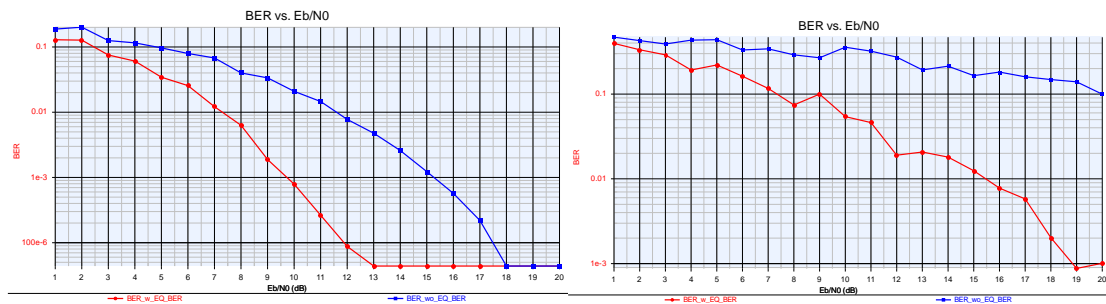
Figure 4-14: CAT6A 15ft 1GHz and 2GHz (respectively) Eb/N0 graphs
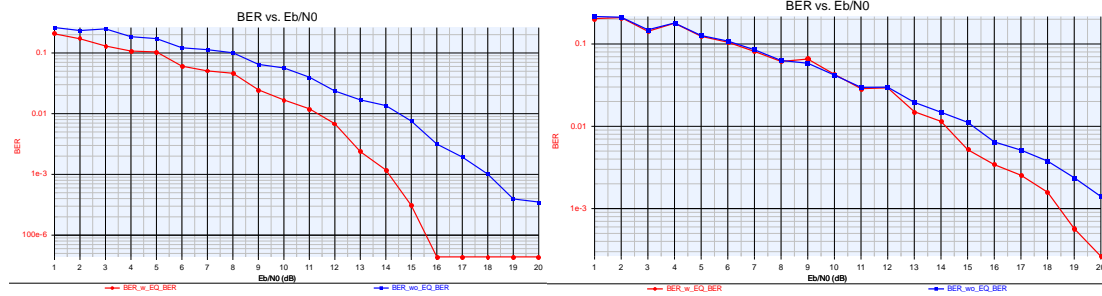
Figure 4-15: CAT6A 25ft 1GHz and 2GHz (respectively) Eb/N0 graphs

Analysis of the simulated Eb/N0 graphs for the wired cables can be found in Chapter 4.5.

The resulting Eb/N0 graphs are separated from analysis for ease of comparison.

4.3 Equalization Verification Physical Wired Channel Results

Physical wired cables are measured with the procedures outlined in Chapter 3 for taking the BER measurements using the SystemVue in combination with the VSG, VSA, and physical channel. The physical wired channels that are tested are CAT7 3ft, 15ft, 25ft and CAT6A 3ft, 15ft, 25ft.

4.3.1 BER Results

The BER results in Table 4-3 are found using the Equalization Verification Setup using physical wired channels. The BER simulations used the simulation parameters in Table 4-4 and Table 4-5.

Table 4-3: BER Results for Physical wired Channels

Cable Type	Length	Carrier	Sample Rate	Input Delay	VGA Gain	Average* BER w EQ	Average* BER wo EQ	Eb/N0 for Physical channel
CAT7	3ft	1GHz	160MHz	1813	-5	0.00E+00	0.00E+00	no noise
CAT7	3ft	2GHz	160MHz	1867	-5	5.83E-03	2.76E-02	9
CAT7	15ft	1GHz	160MHz	779	-5	2.27E-05	2.64E-03	16
CAT7	15ft	2GHz	160MHz	1411	-30	0.00E+00	5.82E-03	no noise
CAT7	25ft	1GHz	160MHz	25	-5	0.00E+00	6.40E-03	17.5
CAT7	25ft	2GHz	160MHz	28	30	2.05E-04	2.51E-02	16
CAT6A	3ft	1GHz	160MHz	1540	-5	1.14E-02	4.94E-02	10
CAT6A	3ft	2GHz	160MHz	4097	5	0.00E+00	2.00E-02	25
CAT6A	15ft	1GHz	160MHz	1548	-5	9.06E-02	2.07E-01	3
CAT6A	15ft	2GHz	160MHz	620	30	0.00E+00	4.86E-03	no noise
CAT6A	25ft	1GHz	160MHz	128	-10	1.45E-03	2.40E-02	13.5
CAT6A	25ft	2GHz	160MHz	126	-20	1.39E-03	1.55E-02	17.5

*Average is across 5 trials, because sampling rate caused large phase error (non-deterministic)

Table 4-4: Physical cable BER TX Setup and Sim Setup

TX Setup				Simulation Setup				
Input Data	PRBS	Carr-ier	BW	Sim Time	Sample Rate	Num Samples	Time Spacing	Freq Res
80 Mbps	7	1GHz	160 MHz	80us	160MHz	12801	6.25E-3 us	12.49 kHz

Table 4-5: Physical cable BER LMS Param and BER Settings

LMS Param		BER Settings			
Num Taps	Step Size	Output Delay	Input Delay	BER start (delay)	BER delay bound
10	0.0001	3	0	4000	10

A few notes on the BER results for the simulated channel:

- The sample rate is chosen to be twice the Input data, which is twice the required Nyquist rate. This is to allow for a baseband pulse of BPSK without any special modulation.

- The BER settings the same for with and without EQ

- The BER recording start is at 4000, so the LMS has time to settle

- The BER delay bound is the amount of potential forward deviation in input vs. output bits for BER calculation.

- The Input and Output Delay are used for BER calculations only. The Output delay is non-zero in order to allow the input to precede the output (casual).

- Sometimes the BER would be greater than .10 for both with and without EQ (unexpected for certain setup), these results would be a result of excessive and outside disturbance and would be thrown out (not included in average).

The input delay corresponds to the s-parameter file's (S2P) simulated delay (group delay) and the VGA gain is found by iteratively changing the delay until the channel's input and output. The VGA gain is used to emulate a Variable Gain Amplifier that auto adjusts to a correct fixed value in an increment of +/-5.

4.3.2 Graphs Produced by SystemVue Simulation

An example of the SystemVue graphs produced from a simulated wired channel measurement is outlined in this section. The same type of graphs are also produced when running the Equalization Verification setup with the physical wired channel, and are used to verify the setup is running properly and the BER results are valid. All graphs in this section are from a simulated CAT7 15ft at 1GHz carrier, 160MHz bandwidth with 80MBPS data.

The "Align Input" graph in Figure 4-16 is used to compare the baseband data of the input of the channel vs. the output of the channel. This graph is used to iteratively find the simulated channel delays found in Table 4-1 by adjusting the channel input delay for the channel's input and output baseband signals to align.
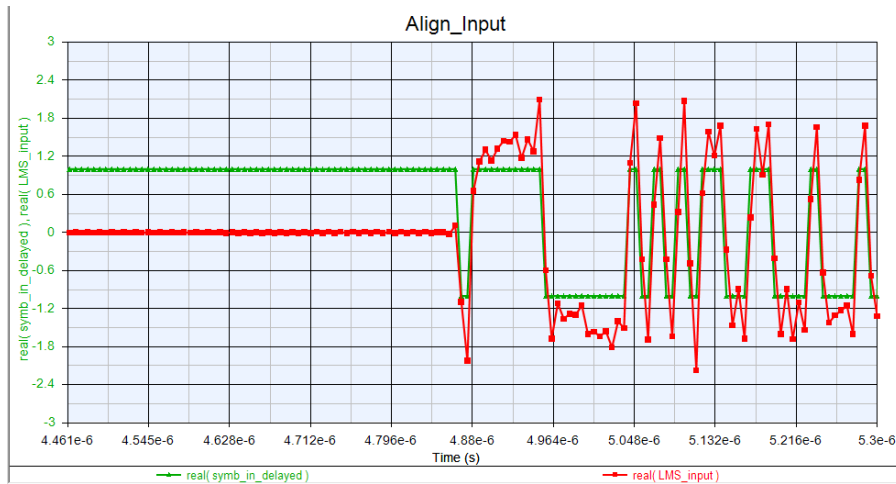
Figure 4-16: Align Input graph to iteratively find the input delay for simulated cable

An example of the spectrums for both the input and output of the channel (both simulated and real) can be seen in Figure 4-17. The channel output spectrum is an attenuated version of the input spectrum by the S21 loss of the channel. The S21 loss of the simulated channel, in this example graph, can be seen below in order to show the attenuation of the signal by the channel.
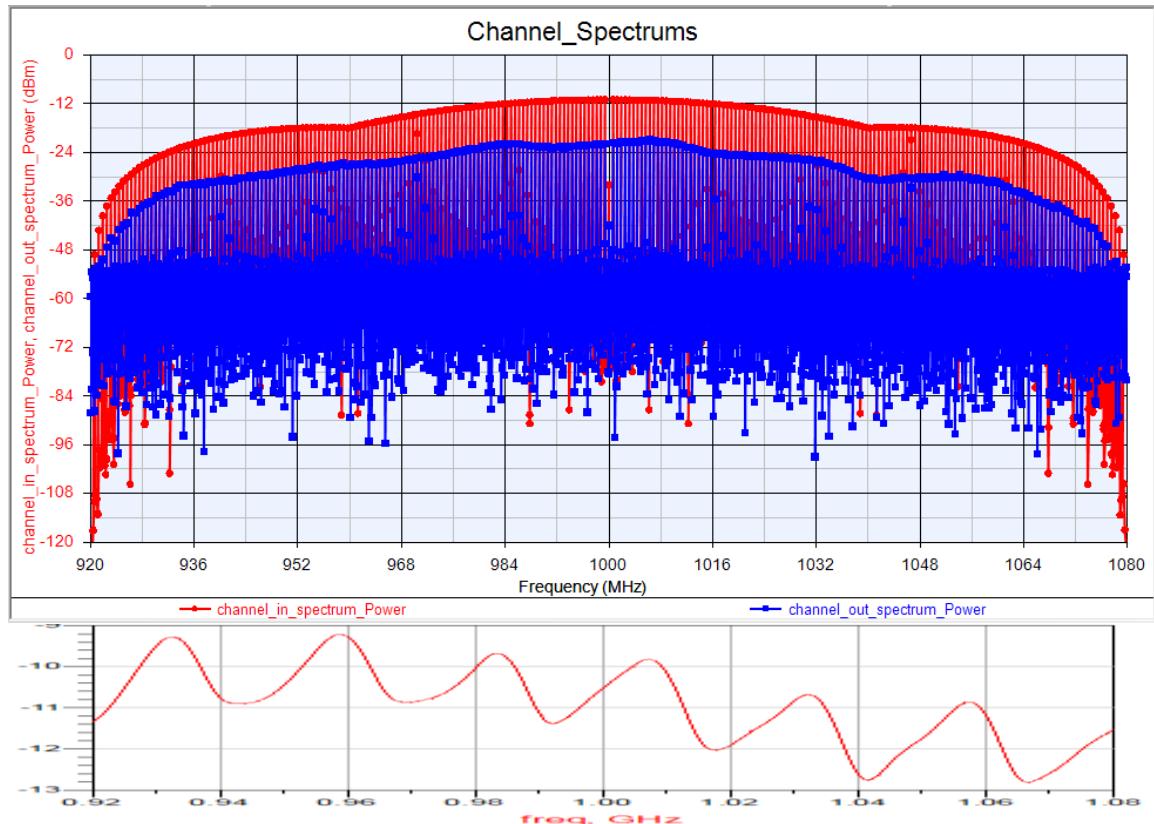
Figure 4-17: Simulated Input and Output Channel Spectrums using CAT7 15ft 1GHz; CAT7 15ft 1GHz S21 graph is plotted below to show the expected attenuation

The LMS error for the equalization scheme is plotted in Figure 4-18. The LMS error is the difference between the output of the equalization and the input of the equalization. The LMS error must converge for the most accurate reading of BER, and is the main reason the BER calculations are delayed. The BER start time must be greater than when the LMS error converges for the smallest and most accurate BER measurement when

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using equalization. This applies for both a simulated and physical channel. The BER results for Chapter 6 are presented with the LMS error converging. An example LMS error converging can be seen in Figure 4-18.
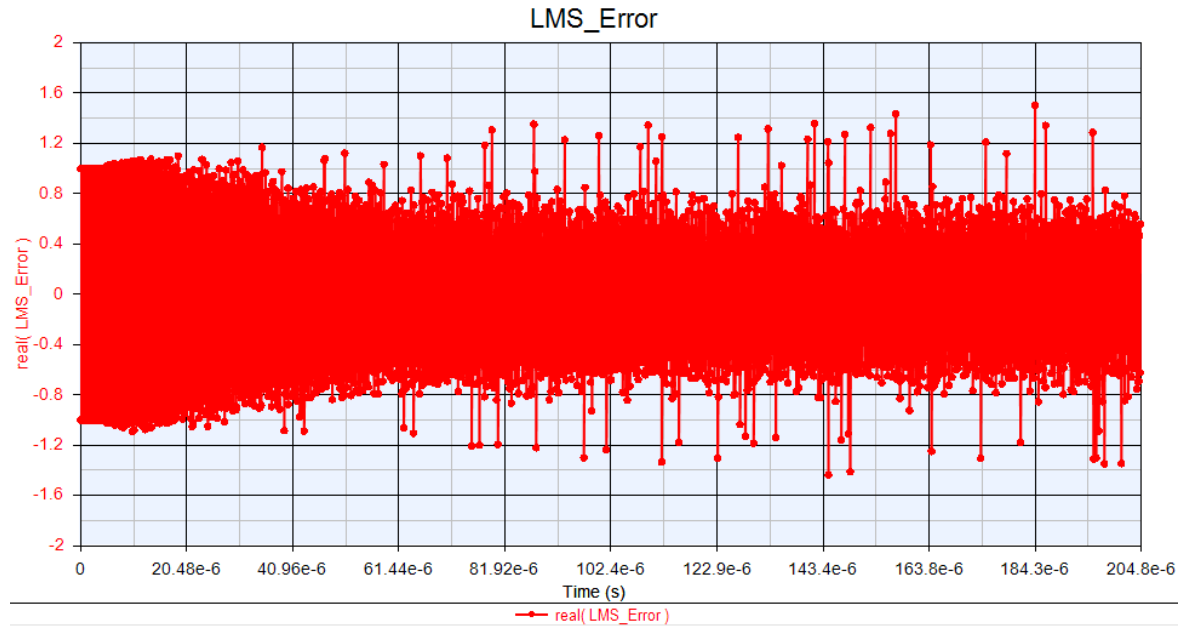
Figure 4-18: LMS error is the difference between the Equalization output and desired output; the LMS error converges once the LMS tap values settle

The LMS output in Figure 4-19, when zoomed out, can be seen to correlate with the LMS error in Figure 4-20. The "LMS inputs" graphs of Figure 4-19 and Figure 4-20 plot the LMS input, LMS output, and desired signal. The LMS input is the demodulated channel output in the time domain, which is equivalent to a non-equalized received signal. The desired output of the LMS block is the LMS input that is set to a 1 or 0 value (decision directed). The LMS output is the LMS input multiplied by a delayed version of the input determined by the LMS taps. This is representative of the decision directed feed forward LMS equalizer that is used on all measurements in Chapters Sections 4 and 5.

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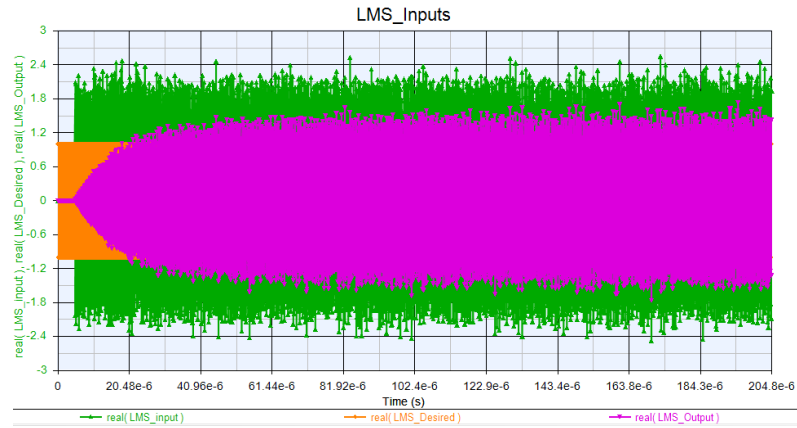
Figure 4-19: LMS Input and Outputs (zoomed out) to show that the LMS (EQ) output follows the LMS error, once the LMS taps settle

A zoomed in version of the same graph of Figure 4-19 can be seen in Figure 4-20. The zoomed in graph of the LMS inputs and outputs shows that the LMS output tracks the desired signal better than the LMS input. This signifies that the equalizer is performing its function correctly and should decrease the BER compared to a non-equalized signal.
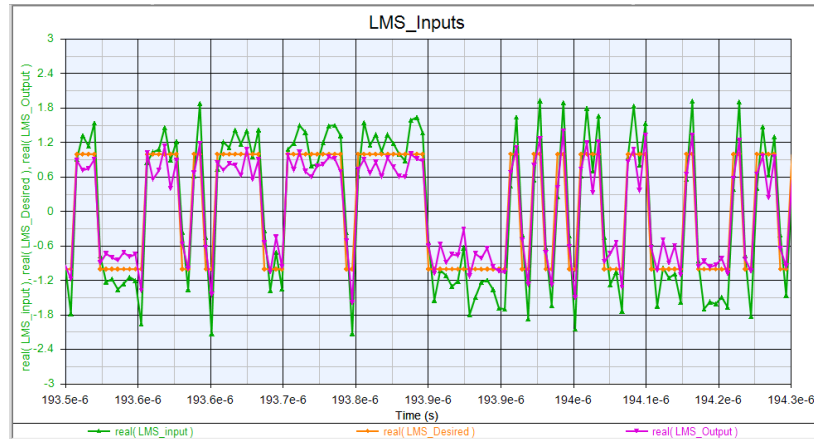
Figure 4-20: LMS Input and Outputs once the taps have settled; the LMS output (with EQ) follows the desired signal better than the LMS input (without EQ)

4.4 Evaluation of Wired Testing Setup

This section compares the simulated to physical channel BER results in order to determine if the wired testing setup is valid. The simulated noise power is determined by finding the simulated noise power that produced the same BER as the physical channel. The noise value varies from trial to trial due to the variable phase noise of the VSA in combination with the VSG and is discussed in more detail in Section 3.4.4.

The BER of the Equalization Verification setup using the physical channel is compared to the BER of the simulated channel. Table 4-3 presents a side-by-side comparison of the BER measurements with the real and simulated channel.

Table 4-6: BER comparison for Wired Simulated and Physical channel

				Physical cable			Simulated Cable	
Cable Type	Length	Carrier	Sample Rate	Average* BER w EQ	Average* BER wo EQ	Eb/N0 for Physical cable	BER w EQ**	BER wo EQ**
CAT7	3ft	1GHz	160MHz	0.00E+00	0.00E+00	no noise	0.00E+00	6.40E-02
CAT7	3ft	2GHz	160MHz	5.83E-03	2.76E-02	9	1.71E-03	2.70E-02
CAT7	15ft	1GHz	160MHz	2.27E-05	2.64E-03	16	8.78E-05	2.38E-03
CAT7	15ft	2GHz	160MHz	0.00E+00	5.82E-03	no noise	0.00E+00	3.10E-02
CAT7	25ft	1GHz	160MHz	0.00E+00	6.40E-03	17.5	0.00E+00	6.38E-03
CAT7	25ft	2GHz	160MHz	2.05E-04	2.51E-02	16	2.64E-04	5.71E-04
CAT6A	3ft	1GHz	160MHz	1.14E-02	4.94E-02	10	1.20E-02	3.90E-02
CAT6A	3ft	2GHz	160MHz	0.00E+00	2.00E-02	25	0.00E+00	2.00E-02
CAT6A	15ft	1GHz	160MHz	9.06E-02	2.07E-01	3	9.10E-02	1.44E-01
CAT6A	15ft	2GHz	160MHz	0.00E+00	4.86E-03	no noise	0.00E+00	1.60E-02
CAT6A	25ft	1GHz	160MHz	1.45E-03	2.40E-02	13.5	1.71E-03	1.40E-02
CAT6A	25ft	2GHz	160MHz	1.39E-03	1.55E-02	17.5	1.27E-03	4.46E-03

(yellow)	=	EQ has better BER
(orange)	=	(approx) same BER
(red)	=	without EQ has better BER
(purple)	=	Sim BER does not match Actual Data for Eb/N0 level

*Average is across 5 trials, because sampling rate caused large phase error (non-deterministic)

**input delay and VGA gain according to Table 4-1

Wired simulated and physical channel testing setup is the same as those described in Chapters 4.2 and 4.3 (Table 4-1, Table 4-2, Table 4-4 and Table 4-5).

A detailed analysis of each cable type and length follows for comparing the simulated vs. physical channel:

CAT7 3ft 1GHz: Even when no noise is present (Eb/N0 > 100), the simulated cable BER measurements do not match the same magnitude for both with and without equalization. The BER magnitude for the simulated cable is 0 with EQ and 6.4E-2 without EQ, and the BER magnitude for the physical cable is 0 with EQ and 0 without EQ. This is because even if Eb/N0 is decreased, the BER of the simulated cable without equalization will only increase, which does not match the physical cable BER measurements. This may be due to the large dip in attenuation at 1GHz as seen in Figure 4-3.

CAT7 3ft 2GHz: The BER magnitudes for the simulated cable match the physical cable when the Eb/N0 is set to 9dB, i.e. the BER magnitude with EQ is 10^{-3} and the BER magnitude without EQ is 10^{-2}. Both the BER with and without equalization matches the same magnitude of the simulated vs. physical cable. Therefore the simulated cable, when the Eb/N0 is set to 9dB, is representative of the physical cable BER measurements since both magnitudes are the same (less than 10x different). An Eb/N0 of 9dB is slightly low compared to the typical range of between 10dB and 20dB for BER in the order of 10^{-2} to 10^{-9} [20].

CAT7 15ft 1GHz: The BER magnitudes for the simulated cable match the physical cable when the Eb/N0 is set to 16dB, i.e. the BER magnitude with EQ is 10^{-5} and the BER magnitude without EQ is 10^{-3}. Both the BER with and without equalization matches the same magnitude of the simulated vs. physical cable. Therefore the simulated cable, when the Eb/N0 is set to 16dB, is representative of the physical cable BER measurements since both magnitudes are the same (less than 10x different). An Eb/N0 of 16dB is a valid value for typical operation of a link since it is between 10dB and 20dB for BER in the order of 10^{-2} to 10^{-9} [20].

CAT7 15ft 2GHz: Even when no noise is present (Eb/N0 > 100), the simulated cable BER measurements do not match the same magnitude for both with and without equalization. The BER magnitude for the simulated cable is 0 with EQ and 3.1E-2 without EQ, and the BER magnitude for the physical cable is 0 with EQ and 5.82E-3 without EQ. This is because even if Eb/N0 is decreased, the BER of the simulated cable without equalization will only increase, which does not match the physical cable BER measurements.

CAT7 25ft 1GHz: The BER magnitudes for the simulated cable match the physical cable when the Eb/N0 is set to 17.5dB, i.e. the BER magnitude with EQ is 0 and the BER magnitude without EQ is 10^{-3}. Both the BER with and without equalization matches the same magnitude of the simulated vs. physical cable. Therefore the simulated cable, when the Eb/N0 is set to 17.5dB, is representative of the physical cable BER measurements since both magnitudes are the same (less than 10x different). An Eb/N0 of 17.5dB is a valid value for typical operation of a link since it is between 10dB and 20dB for BER in the order of 10^{-2} to 10^{-9} [20].

CAT7 25ft 2GHz: Even when Eb/N0 is set to 16dB, the simulated cable BER measurements do not match the same magnitude for both with and without equalization. The BER magnitude for the simulated cable is 2.64E-4 with EQ and 5.71E-4 without EQ, and the BER magnitude for the physical cable is 2.05E-4 with EQ and 2.51E-2 without EQ. Eb/N0 cannot be decreased from 16dB to match the BERs without EQ, because then the BER of the simulated cable with equalization will no longer match the physical cable BER with equalization.

CAT6A 3ft 1GHz: The BER magnitudes for the simulated cable match the physical cable when the Eb/N0 is set to 10dB, i.e. the BER magnitude with EQ is 10^{-2} and the BER magnitude without EQ is 10^{-2} (with EQ has lower value). Both the BER with and without equalization matches the same magnitude of the simulated vs. physical cable. Therefore the simulated cable, when the Eb/N0 is set to 10dB, is representative of the physical cable BER measurements since both magnitudes are the same (less than 10x different). An Eb/N0 of 10dB is a valid value, although on the low side, for typical operation of a link since it is between 10dB and 20dB [20].

CAT6A 3ft 2GHz: The BER magnitudes for the simulated cable match the physical cable when the Eb/N0 is set to 25dB, i.e. the BER magnitude with EQ is 0 and the BER magnitude without EQ is 10^{-2}. Both the BER with and without equalization matches the same magnitude of the simulated vs. physical cable. Therefore the simulated cable, when the Eb/N0 is set to 25dB, is representative of the physical cable BER measurements since both magnitudes are the same (less than 10x different). An Eb/N0 of 25dB is a high value for typical operation of a link since it above 20dB [20].

CAT6A 15ft 1GHz: The BER magnitudes for the simulated cable match the physical cable when the Eb/N0 is set to 3dB, i.e. the BER magnitude with EQ is 10^{-2} and the BER magnitude without EQ is 10^{-1}. Both the BER with and without equalization matches the same magnitude of the simulated vs. physical cable. Therefore the simulated cable, when the Eb/N0 is set to 3dB, is representative of the physical cable BER measurements since both magnitudes are the same (less than 10x different). An Eb/N0 of 3dB is a low value for typical operation of a link since it is below 10dB [20]. The Eb/N0 value is low (3) which means the noise power of the VSA/VSG is higher than the other measurements in this section. This is unlike any of the other physical channel measurements and may be due to the S21 value increasing (attenuation decreasing) with frequency as seen in Figure 4-14.

CAT6A 15ft 2GHz: Even when no noise is present (Eb/N0 > 100), the simulated cable BER measurements do not match the same magnitude for both with and without equalization. The BER magnitude for the simulated cable is 0 with EQ and 4.86E-3 without EQ, and the BER magnitude for the physical cable is 0 with EQ and 1.60E-2 without EQ. This is because even if Eb/N0 is decreased, the BER of the simulated cable without equalization will only increase, which does not match the physical cable BER measurements.

CAT6A 25ft 1GHz: The BER magnitudes for the simulated cable match the physical cable when the Eb/N0 is set to 13.5dB, i.e. the BER magnitude with EQ is 10^{-3} and the BER magnitude without EQ is 10^{-2}. Both the BER with and without equalization matches the same magnitude of the simulated vs. physical cable. Therefore the simulated cable, when the Eb/N0 is set to 13.5dB, is representative of the physical cable BER

measurements since both magnitudes are the same (less than 10x different). An Eb/N0 of

13.5dB is a valid value for typical operation of a link since it between 10dB and 20dB

[20].

CAT6A 25ft 2GHz: Even when Eb/N0 is set to 17.5dB, the simulated cable BER

measurements do not match the same magnitude for both with and without equalization.

The BER magnitude for the simulated cable is 1.27E-3 with EQ and 4.46E-3 without EQ,

and the BER magnitude for the physical cable is 1.39E-3 with EQ and 1.55E-2 without

EQ. Eb/N0 cannot be decreased from 17.5dB to match the BERs without EQ, because

then the BER of the simulated cable with equalization will no longer match the physical

cable BER with equalization. This may be due to the average of 5 trials not being fully

representative of the channel BER with and without equalization, or because of the large

dips in the S21 plot as seen in Figure 4-15.

The overall conclusion of this section is that the simulated channel, even with added

simulated noise, is not always representative of the physical channel when using the VSA

and VSG. The channels that differed from physical to simulated BER results with and

without equalization are CAT7 3ft 1GHz carrier, CAT7 15ft 2GHz carrier, CAT7 25ft

2GHz carrier, CAT6A 15ft 2GHz carrier, and CAT6A 25ft 2GHz carrier. The higher

carrier frequency of 2GHz produced the higher number of differences from simulated to

physical channel compared to 1GHz carrier. The difference between the simulated and

physical channel BER results is likely due to a finite number of trials (5) when measuring

across the physical channels, and the added phase noise of the VSA/VSG due to timing

imperfections. The added phase noise of the VSA/VSG changes from trial to trial. The

phase noise likely changes because it is on the same order of magnitude as the simulation time. This large noise addition is hard to model without using an iterative approach and multiple trials with the current setup.

However for most of the wired channels, with added simulated noise, the real vs. simulated channels had the same order of magnitude for the BER with and without equalization. Therefore, a conclusion will be made that if the VSA and VSG phase noise could be more accurately controlled, the physical channel BER measurements would follow current s-parameter simulated channel BER measurements. The testing setup is valid, but the phase noise would need to be more closely controlled if this system was to go to be more extensively used. This is not related to evaluating the equalization scheme across these wired channels, which is analyzed in Chapter 4.5.

4.5 Evaluation of Equalization Scheme over Simulated and Physical Wired Channels

This section compares the BER results with and without the equalization scheme for the wired channels identified in Chapter 4. The equalization scheme under test is the decision directed feed forward LMS equalizer as seen in Figure 4-21.
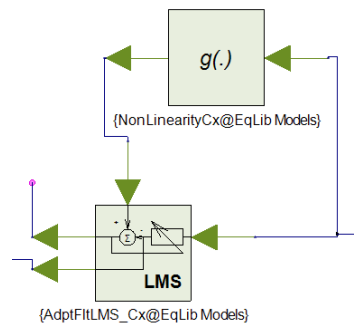
Figure 4-21: Decision Directed Feed Forward LMS Equalizer as implemented by SystemVue dataflow modeling blocks

The BER with and without this equalization scheme will be compared for both the simulated and physical wired channels across the given simulation parameters. Three components will be evaluated to determine if the equalization scheme improved the link for each wired channel: 1) the physical cable BER, 2) the simulated cable BER, 3) if the BER vs. Eb/N0 graph improved for all noise levels. For comparing the equalization scheme, Chapter 4.5.1 evaluates different cables for the same simulation setup while Chapter 4.5.2 evaluates different setups for the same cable.

4.5.1 Evaluation of Typical Case Equalization Scheme

Different cables and carrier frequencies are used to determine if the decision directed feed forward LMS equalizer (as modeled in SystemVue) improves the quality of the link according to the three criteria:

1) The physical cable BER

2) The simulated cable BER

3) If the BER vs. Eb/N0 graph improved for all noise levels

Each cable setup will be analyzed independently and then a final section conclusion will be made.

Table 4-7: Evaluation of Equalization Scheme over different Wired Channels (Real and Simulated); (Reprinted with last column for Eb/N0 analysis)

				Physical cable		Eb/N0 for Physical cable	Simulated Cable		
Cable Type	Length	Carrier	Sample Rate	Average* BER w EQ	Average* BER wo EQ		BER w EQ**	BER wo EQ**	EbN0 Sim Better for EQ?
CAT7	3ft	1GHz	160MHz	0.0E+00	0.0E+00	no noise	0E+00	6E-02	Yes
CAT7	3ft	2GHz	160MHz	5.8E-03	2.8E-02	9	2E-03	3E-02	Yes
CAT7	15ft	1GHz	160MHz	2.3E-05	2.6E-03	16	9E-05	2E-03	EQ Better at 10dB
CAT7	15ft	2GHz	160MHz	0.0E+00	5.8E-03	no noise	0E+00	3E-02	Yes
CAT7	25ft	1GHz	160MHz	0.0E+00	6.4E-03	17.5	0E+00	6E-03	EQ Better at 10dB
CAT7	25ft	2GHz	160MHz	2.0E-04	2.5E-02	16	3E-04	6E-04	EQ Better at 12dB
CAT6A	3ft	1GHz	160MHz	1.1E-02	4.9E-02	10	1E-02	4E-02	Yes
CAT6A	3ft	2GHz	160MHz	0.0E+00	2.0E-02	25	0E+00	2E-02	Yes
CAT6A	15ft	1GHz	160MHz	9.1E-02	2.1E-01	3	9E-02	1E-01	Yes
CAT6A	15ft	2GHz	160MHz	0.0E+00	4.9E-03	no noise	0E+00	2E-02	Yes
CAT6A	25ft	1GHz	160MHz	1.5E-03	2.4E-02	13.5	2E-03	1E-02	Yes
CAT6A	25ft	2GHz	160MHz	1.4E-03	1.5E-02	17.5	1E-03	4E-03	EQ Better at 12dB

(yellow)	=	EQ has better BER
(orange)	=	(approx) same BER
(red)	=	without EQ has better BER
(purple)	=	can't get BER Sim to match Actual Data

*Average is across 5 trials, because sampling rate caused large phase error (non-deterministic)

**input delay and VGA gain according to Table 4-1

Wired simulated and physical channel testing setup is the same as Chapters 4.2 and 4.3 (Table 4-1, Table 4-2, Table 4-4, and Table 4-5
Table 4-5).

A detailed analysis of each cable type and length follows for the physical channel BER, simulated channel BER, and BER vs. Eb/N0 simulated graph:

CAT7 3ft 1GHz: The BER is the same for with and without equalization for the physical channel of 0. The BER decreases (improves) with equalization for the simulated channel with no noise (Eb/N0 > 100) from 10^{-2} to 0 BER. The BER also decreases with equalization for the simulated channel for all Eb/N0 values (see BER vs. Eb/N0 graph in Figure 4-10).

CAT7 3ft 2GHz: The BER decreases (improves) with equalization for both the simulated channel, when Eb/N0 is 9dB, and the physical channel from 10^{-2} to 10^{-3} BER. The BER also decreases with equalization for the simulated channel for all Eb/N0 values (see BER vs. Eb/N0 graph in Figure 4-10).

CAT7 15ft 1GHz: The BER decreases (improves) with equalization for both the simulated channel, when Eb/N0 is 16dB, and the physical channel from 10^{-3} to 10^{-5} BER. The BER also decreases with equalization for the simulated channel at all Eb/N0 values greater than 10dB (see BER vs. Eb/N0 graph in Figure 4-11).

CAT7 15ft 2GHz: The BER decreases (improves) from 10^{-2} to 0 BER when adding equalization with the simulated channel and no noise power (Eb/N0 > 100). The BER also decreases from 10^{-3} to 0 BER when adding equalization with the physical channel. The BER also decreases with equalization for the simulated channel for all Eb/N0 values (see BER vs. Eb/N0 graph in Figure 4-11).

CAT7 25ft 1GHz: The BER decreases (improves) with equalization for both the simulated channel, when Eb/N0 is 17.5dB, and the physical channel from 10^{-3} to 0 BER.

The BER also decreases with equalization for the simulated channel at all Eb/N0 values greater than 10dB (see BER vs. Eb/N0 graph in Figure 4-12).

***CAT7 25ft 2GHz*:** The BER decreases (improves) from $6*10^{-4}$ to $3*10^{-4}$ BER when adding equalization with the simulated channel and no noise power (Eb/N0 is 16dB). The BER also decreases from 10^{-2} to 10^{-4} BER when adding equalization with the physical channel. The BER also decreases with equalization for the simulated channel at all Eb/N0 values greater than 12dB (see BER vs. Eb/N0 graph in Figure 4-12).

***CAT6A 3ft 1GHz*:** The BER decreases (improves) with equalization for both the simulated channel, when Eb/N0 is 10dB, and the physical channel from 10^{-2} to 10^{-2} BER (values decrease). The BER also decreases with equalization for the simulated channel for all Eb/N0 values (see BER vs. Eb/N0 graph in Figure 4-13).

***CAT6A 3ft 2GHz*:** The BER decreases (improves) with equalization for both the simulated channel, when Eb/N0 is 25dB, and the physical channel from 10^{-2} to 0 BER. The BER also decreases with equalization for the simulated channel for all Eb/N0 values (see BER vs. Eb/N0 graph in Figure 4-13).

***CAT6A 15ft 1GHz*:** The BER decreases (improves) with equalization for both the simulated channel, when Eb/N0 is 3dB, and the physical channel from 10^{-2} to 0 BER. The BER also decreases with equalization for the simulated channel for all Eb/N0 values (see BER vs. Eb/N0 graph in Figure 4-14).

***CAT6A 15ft 2GHz*:** The BER decreases (improves) from 10^{-2} to 0 BER when adding equalization with the simulated channel and no noise power (Eb/N0 > 100). The BER also decreases from 10^{-3} to 0 BER when adding equalization with the physical channel.

The BER also decreases with equalization for the simulated channel for all Eb/N0 values (see BER vs. Eb/N0 graph in Figure 4-14).

CAT6A 25ft 1GHz: The BER decreases (improves) with equalization for both the simulated channel, when Eb/N0 is 13.5dB, and the physical channel from 10^{-2} to 10^{-3} BER. The BER also decreases with equalization for the simulated channel for all Eb/N0 values (see BER vs. Eb/N0 graph in Figure 4-15).

CAT6A 25ft 2GHz: The BER decreases (improves) from $5*10^{-3}$ to $1*10^{-3}$ BER when adding equalization with the simulated channel and no noise power (Eb/N0 is 17.5dB). The BER also decreases from 10^{-2} to 10^{-3} BER when adding equalization with the physical channel. The BER also decreases with equalization for the simulated channel at all Eb/N0 values greater than 12dB (see BER vs. Eb/N0 graph in Figure 4-15).

Overall the decision directed feed forward LMS equalization scheme improves the BER across different simulated and physical cables, 1GHz and 2GHz, and simulated noise power for 80MBPS data. The longer physical cables in general do not match their simulated versions as well for CAT6A and CAT7, but there is no correlation between 1GHz and 2GHz carrier. The Equalization Verification has successfully shown, for the cases examined, that this equalization scheme, modeled in SystemVue, improves the link quality by reducing BER under different conditions, for wired cables for 80MBPS baseband data.

4.6 Evaluation of Equalization Scheme with Parameter Variation

The Equalization Scheme will now be verified in simulation across a simulated and physical cable for variations of the equalization scheme. The physical and simulated cable will be not change, unlike the previous section, and will be a CAT7 15ft cable. The variations in both simulated and physical cable testing are LMS step size, number of LMS taps, PRBS input stream, number of data samples, and input data rate. The results of this testing can be seen in Table 4-8.

4.6.1 Eb/N0 Simulations

Eb vs. N0 graphs are simulated by sweeping noise power. See Chapter 2 for background on Eb/N0 graphs and how they relate to Signal to Noise ratio. Also see Chapter 3 for how to simulate the Eb/N0 graphs for each channel. The Eb/N0 graphs are used to identify the possible noise levels when measuring physical cables with the VSG and VSA, and to show that the equalization scheme works across different noise levels with the same channel (Figure 4-22 to 4-28). All BER vs. Eb/N0 graphs use 160MHz sample, 80MBPS data rate, 32768 number of simulation samples 10000 BER delay (unless specified otherwise). BER delay is when the simulation sample at which the BER starts recording data. For Eb/N0 graphs, 1GHz and 2GHz carriers are examined. VGA and input delay are specified in Table 4-8. For BER vs. Eb/N0 curves of Figure 4-22 to Figure 4-28, the red curves are with equalization and the blue curves are without equalization.
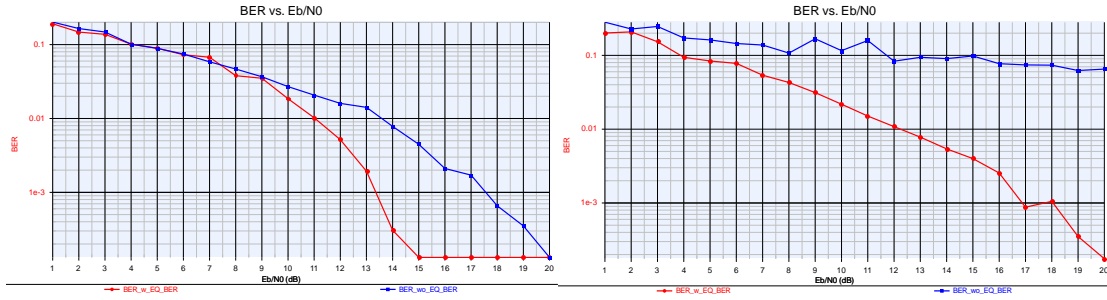
Figure 4-22: CAT7 15ft 1GHz and 2GHz (Control) BER vs. Eb/N0 (reprinted for convenience)
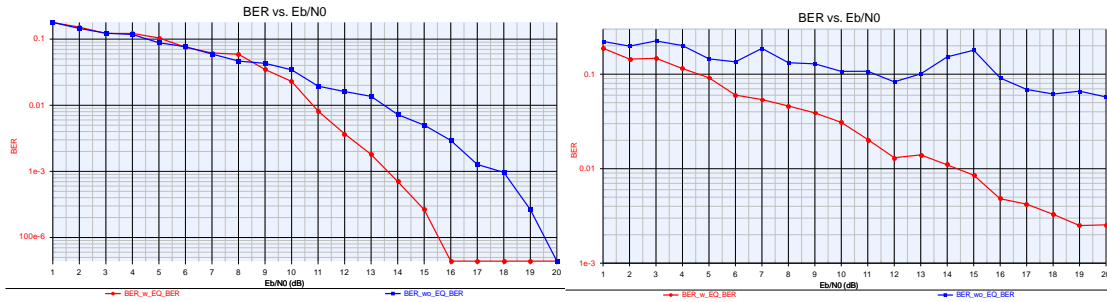
Figure 4-23: CAT7 15ft 1GHz and 2GHz, Step Size = .001 BER vs. Eb/N0
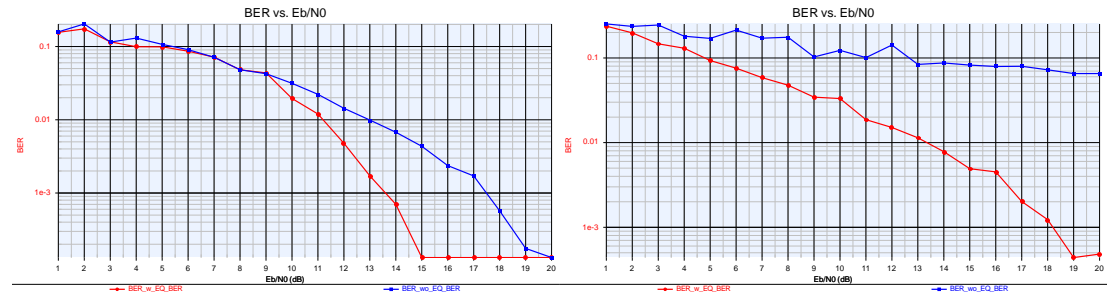
Figure 4-24: CAT7 15ft 1GHz, Taps = 4 BER vs. Eb/N0
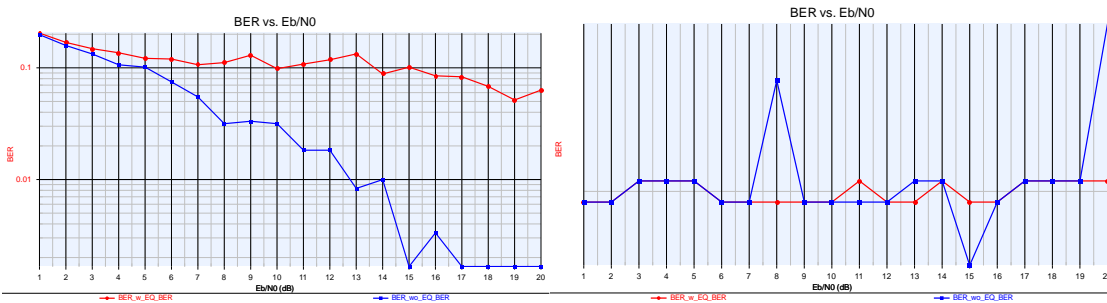
Figure 4-25: CAT7 15ft 1GHz, Samples = 1601 BER vs. Eb/N0
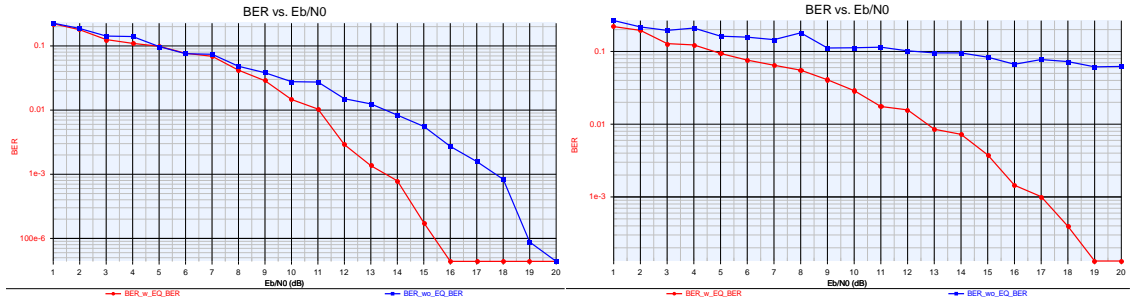
Figure 4-26: CAT7 15ft 1GHz and 2GHz, PRBS = 4 BER vs. Eb/N0
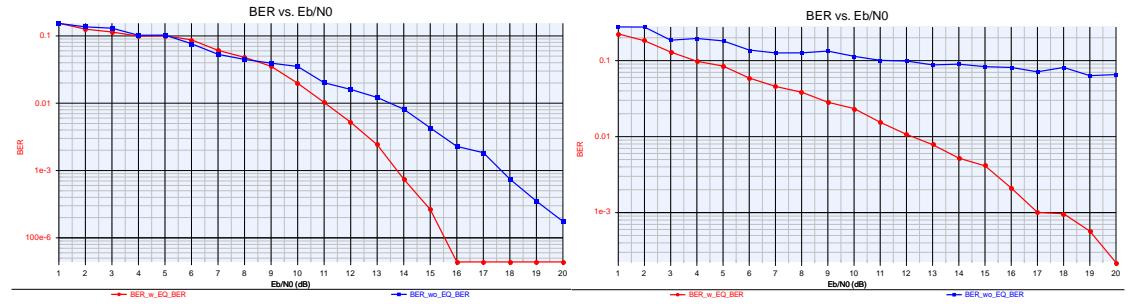
Figure 4-27: CAT7 15ft 1GHz and 2GHz, PRBS = 12 BER vs. Eb/N0
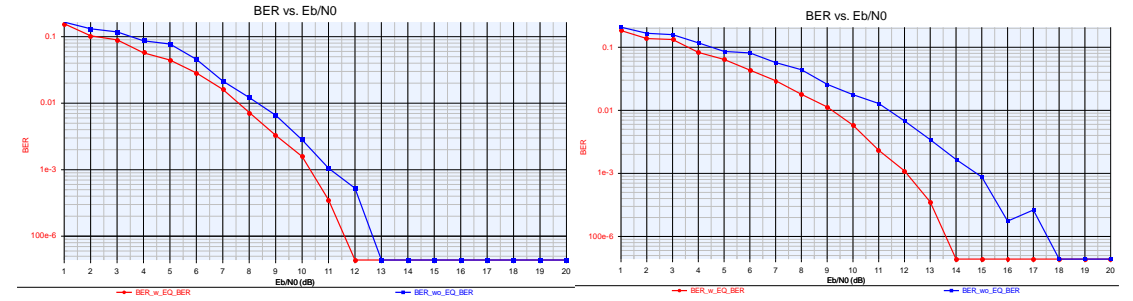
Figure 4-28: CAT7 15ft 1GHz and 2GHz, 100 MHz Sample, 50MBPS data BER vs. Eb/N0

4.6.2 BER Results

The BER results in this section are found from the simulated cable, CAT7 15ft only, with added noise when varying simulation and equalization parameters. The noise level corresponding to the noise level approximated in the VSG/VSA measurements using the physical wired channels in Table 4-9. The simulation or equalization parameter that is changed is specified in the "Variable Change" column in Table 4-8.

Table 4-8: Simulated Cable BER Results, Equalization Parameter Variation

Cable Type	Length	Carrier	Sample Rate	Input Delay	VGA Gain	Variable Change	Eb/N0 for Sim	BER w EQ	BER wo EQ
CAT 7	15ft	1GHz	160 MHz	779	-5	Control	16.0	8.78E-05	2.38E-03
CAT 7	15ft	1GHz	160 MHz	779	-5	Step Size = .001	16	0.00E+00	2.59E-03
CAT 7	15ft	1GHz	160 MHz	779	-5	Taps = 4	13	1.71E-03	1.20E-02
CAT 7	15ft	1GHz	160 MHz	779	-5	Samples = 1601**	no noise	3.00E-02	0.00E+00
CAT 7	15ft	1GHz	160 MHz	779	-5	Samples = 25602	17	0.00E+00	1.41E-03
CAT 7	15ft	1GHz	160 MHz	779	-5	PRBS = 4	20	0.00E+00	4.39E-05
CAT 7	15ft	1GHz	160 MHz	779	-5	PRBS = 12	15	8.78E-05	2.50E-02
CAT 7	15ft	1GHz	100 MHz	186	-5	Data = 50MBPS	14.5	0.00E+00	4.39E-05
CAT 7	15ft	2GHz	160 MHz	1411	-30	Control	no noise	0.00E+00	3.10E-02
CAT 7	15ft	2GHz	160 MHz	1411	-30	Step Size = .001	no noise	0.00E+00	3.20E-02
CAT 7	15ft	2GHz	160 MHz	1411	-30	Taps = 4	no noise	0.00E+00	3.20E-02
CAT 7	15ft	2GHz	160 MHz	1411	-30	Samples = 1601**	no noise	1.40E-02	3.30E-02
CAT 7	15ft	2GHz	160 MHz	1411	-30	Samples = 25602	no noise	0.00E+00	3.20E-02
CAT 7	15ft	2GHz	160 MHz	1411	-30	PRBS = 4	no noise	0.00E+00	3.30E-02
CAT 7	15ft	2GHz	160 MHz	1411	-30	PRBS = 12	no noise	0.00E+00	3.60E-02
CAT 7	15ft	2GHz	100 MHz	674	-30	Data = 50MBPS	14.5	0.00E+00	1.01E-03

*Average is across 5 trials, because sampling rate caused large phase error (non-deterministic)

**1601 simulation samples uses BER recording start of 1000 (instead of 10000)

Wired simulated channel testing setup is the same as Chapters 4.2.

The BER results in Table 4-9 are found using the Equalization Verification Setup using physical wired channels. The BER simulations use the same as Chapter 4.3.1.

Table 4-9: Physical cable BER Results, Equalization Parameter Variation

Cable Type	Length	Carrier	Sample Rate	VGA Gain	Variable Change	Average* BER w EQ	Average* BER wo EQ
CAT7	15ft	1GHz	160MHz	-5	Control	2.27E-05	2.64E-03
CAT7	15ft	1GHz	160MHz	-5	Step Size = .001	0.00E+00	1.28E-02
CAT7	15ft	1GHz	160MHz	-5	Taps = 4	1.05E-03	3.81E-02
CAT7	15ft	1GHz	160MHz	-5	Samples = 1601**	1.88E-02	9.20E-03
CAT7	15ft	1GHz	160MHz	-5	Samples = 25602	0.00E+00	2.48E-03
CAT7	15ft	1GHz	160MHz	-5	PRBS = 4	0.00E+00	0.00E+00
CAT7	15ft	1GHz	160MHz	-5	PRBS = 12	3.18E-04	1.64E-02
CAT7	15ft	1GHz	100MHz	-5	Data = 50MBPS	0.00E+00	0.00E+00
CAT7	15ft	2GHz	160MHz	-30	Control	0.00E+00	5.82E-03
CAT7	15ft	2GHz	160MHz	-30	Step Size = .001	2.27E-05	3.75E-03
CAT7	15ft	2GHz	160MHz	-30	Taps = 4	4.55E-04	6.39E-03
CAT7	15ft	2GHz	160MHz	-30	Samples = 1601***	9.25E-03	6.25E-04
CAT7	15ft	2GHz	160MHz	-30	Samples = 25602	2.80E-03	1.57E-02
CAT7	15ft	2GHz	160MHz	-30	PRBS = 4	4.77E-04	2.00E-03
CAT7	15ft	2GHz	160MHz	-30	PRBS = 12	1.23E-03	3.38E-03
CAT7	15ft	2GHz	100MHz	-30	Data = 50MBPS	0.00E+00	1.45E-03

*Average is across 5 trials, because sampling rate caused large phase error (non-deterministic)
**1601 simulation samples uses BER start of 1000 (instead of 10000)
Wired physical channel testing setup is the same as Chapters 4.3.

Table 4-10 compares the simulated to physical channel BER results in order to determine if the wired testing setup is valid and if the equalization scheme improves the quality of the link. The simulated noise is determined based on the physical channel BER in order to correctly set the noise value in simulation to compare the two results.

Table 4-10: BER Results for Equalization Parameter Variation; Comparing CAT7 15ft Simulated to Physical cable, and Evaluating EQ Scheme

Cable Type	Frequency	Variable Change	Physical cable		Eb/N0 for Sim	Simulation		EbN0 Sim Better for EQ?
			Average* BER w EQ	Average* BER wo EQ		BER w EQ**	BER wo EQ**	
CAT 7 15ft	1GHz, 160MHz BW	Control	2.27E-05	2.64E-03	16.0	8.78E-05	2.38E-03	EQ gets better at 10dB
CAT 7 15ft	1GHz, 160MHz BW	Step Size = .001	0.00E+00	1.28E-02	16	0.00E+00	2.59E-03	EQ gets better at 10dB
CAT 7 15ft	1GHz, 160MHz BW	Taps = 4	1.05E-03	3.81E-02	13	1.71E-03	1.20E-02	EQ gets better at 10dB
CAT 7 15ft	1GHz, 160MHz BW	Samples = 1601***	1.88E-02	9.20E-03	no noise	3.00E-02	0.00E+00	No
CAT 7 15ft	1GHz, 160MHz BW	Samples = 25602	0.00E+00	2.48E-03	17	0.00E+00	1.41E-03	Not Run
CAT 7 15ft	1GHz, 160MHz BW	PRBS = 4	0.00E+00	0.00E+00	20	0.00E+00	4.39E-05	EQ gets better at 8dB
CAT 7 15ft	1GHz, 160MHz BW	PRBS = 12	3.18E-04	1.64E-02	15	8.78E-05	2.50E-02	EQ gets better at 9dB
CAT 7 15ft	1GHz, 160MHz BW	Data = 50MBPS	0.00E+00	0.00E+00	14.5	0.00E+00	4.39E-05	Yes
CAT 7 15ft	2GHz, 160MHz BW	Control	0.00E+00	5.82E-03	no noise	0.00E+00	3.10E-02	Yes
CAT 7 15ft	2GHz, 160MHz BW	Step Size = .001	2.27E-05	3.75E-03	no noise	0.00E+00	3.20E-02	Yes
CAT 7 15ft	2GHz, 160MHz BW	Taps = 4	4.55E-04	6.39E-03	no noise	0.00E+00	3.20E-02	Yes
CAT 7 15ft	2GHz, 160MHz BW	Samples = 1601***	9.25E-03	6.25E-04	no noise	1.40E-02	3.30E-02	Not Run
CAT 7 15ft	2GHz, 160MHz BW	Samples = 25602	2.80E-03	1.57E-02	no noise	0.00E+00	3.20E-02	Not Run
CAT 7 15ft	2GHz, 160MHz BW	PRBS = 4	4.77E-04	2.00E-03	no noise	0.00E+00	3.30E-02	Yes
CAT 7 15ft	2GHz, 160MHz BW	PRBS = 12	1.23E-03	3.38E-03	no noise	0.00E+00	3.60E-02	Yes
CAT 7 15ft	2GHz, 160MHz BW	Data = 50MBPS	0.00E+00	1.45E-03	14.5	0.00E+00	1.01E-03	Yes

Legend:
- (yellow) EQ has better BER
- (orange) (approx) same BER
- (red) without EQ has better BER
- (purple) Can't match magnitude of Sim to Physical cable with Eb/N0

*Average is across 5 trials, because sampling rate caused large phase error (non-deterministic)
**input delay are 779 and 1411 for 1GHz and 2GHz respectively and VGA gain are -5 and -30 respectively
***1601 simulation samples uses BER start of 1000 (instead of 10000)
Wired simulated and physical channel testing setup is the same as Chapters 4.2 and 4.3.

For comparing simulated vs. physical channel BERs (all CAT7 15ft channel, and all variables set to control values unless specified):

1GHz, Control: The BER magnitudes for the simulated cable match the physical cable when the Eb/N0 is set to 16dB, i.e. the BER magnitude with EQ is 10^{-5} and the BER magnitude without EQ is 10^{-3}. Both the BER with and without equalization matches the same magnitude of the simulated vs. physical cable. Therefore the simulated cable, when the Eb/N0 is set to 16dB, is representative of the physical cable BER measurements since both magnitudes are the same (less than 10x different). An Eb/N0 of 16dB is a valid value for typical operation of a link since it is between 10dB and 20dB for BER in the order of 10^{-2} to 10^{-9} [20].

1GHz, Step Size = .001: Even when the Eb/N0 is set to 16dB, the simulated cable BER measurements do not match the same magnitude for both with and without equalization. The BER magnitude for the simulated cable is 0 with EQ and 1.28E-2 without EQ, and the BER magnitude for the physical cable is 0 with EQ and 2.59E-3 without EQ. This is because even if Eb/N0 is increased, the BER of the simulated cable without equalization will only decrease, which does not match the physical cable BER measurements.

1GHz, Taps = 4: The BER magnitudes for the simulated cable match the physical cable when the Eb/N0 is set to 13dB, i.e. the BER magnitude with EQ is 10^{-3} and the BER magnitude without EQ is 10^{-2}. Both the BER with and without equalization matches the same magnitude of the simulated vs. physical cable. Therefore the simulated cable, when the Eb/N0 is set to 13dB, is representative of the physical cable BER measurements (less than 10x different). An Eb/N0 of 13dB is a valid value for typical operation of a link (between 10dB and 20dB), although on the low end [20].

1GHz, Samples = 1601: The BER magnitude for the simulated cable does not match the physical cable with and without equalization. The BER magnitude for the simulated cable is 1.88E-2 with EQ and 9.2E-3 without EQ, and the BER magnitude for the physical cable is 3E-2 with EQ and 0 without EQ. The BER is larger (worse) with equalization for both the physical and simulated cable measurements. Even when no noise (Eb/N0 > 100) is added to the simulated channel, the BER did not match with the physical and simulated cable BER magnitudes.

1GHz, Samples = 25602: The BER magnitudes for the simulated cable match the physical cable when the Eb/N0 is set to 17dB, i.e. the BER magnitude with EQ is 0 and the BER magnitude without EQ is 10^{-3}. Both the BER with and without equalization matches the same magnitude of the simulated vs. physical cable. Therefore the simulated cable, when the Eb/N0 is set to 17dB, is representative of the physical cable BER measurements since both magnitudes are the same (less than 10x different). An Eb/N0 of 17dB is a valid value for typical operation of a link since it is between 10dB and 20dB for BER in the order of 10^{-2} to 10^{-9} [20].

1GHz, PRBS = 4: The BER of the physical cable is both 0 for both with and without equalization but matches the simulated cable BER measurements when Eb/N0 is set to >20. If Eb/N0 is set to greater than 20, then both with and without equalization have 0 BER which is identical for both simulated and physical cable. A Eb/N0 value of 20 is a valid value for a typical link operation since it is between 10dB and 20dB for BER in the order of 10^{-2} to 10^{-9} [20].

1GHz, PRBS = 12: Even when the Eb/N0 is set to 15dB, the simulated cable BER measurements do not match the same magnitude for both with and without equalization. The BER magnitude for the simulated cable is 3.18E-4 with EQ and 1.64E-2 without EQ, and the BER magnitude for the physical cable is 8.78E-5 with EQ and 2.50E-2 without EQ. Changing the Eb/N0 (noise power) of the simulated channel will not cause the magnitudes of the simulated cable BER measurements with and without equalization to converge to the physical channel BER measurements.

1GHz, Data = 50MBPS: The BER of the physical cable is both 0 for both with and without equalization but matches the simulated cable BER measurements when Eb/N0 is set to >14.5. If Eb/N0 is set to greater than 14.5, then both with and without equalization have 0 BER which is identical for both simulated and physical cable. A Eb/N0 value of 14.5 is a valid value for a typical link operation (between 10dB and 20dB), although on the low end [20].

2GHz, Control: The BER value of the simulated cable without equalization is higher than the BER value of the physical cable without equalization even when the noise power of the simulated channel is set to 0 (Eb/N0 > 100). The BER magnitude for the simulated cable is 0 with EQ and 5.82E-3 without EQ, and the BER magnitude for the physical cable is 0 with EQ and 3.1E-2 without EQ. Therefore the BER of the physical and simulated cable did not match magnitudes for any Eb/N0 value since the noise could not be decreased to a lower value. The BER of the simulated cable without equalization is unusually high, and is likely a product of high ISI for mis-alignment in simulation, i.e. the ISI aligns to cause BER on a frequent and periodic basis. Apply the same analysis for the rest of the 2GHz simulated vs. physical cable analysis.

2GHz, Step Size = .001: The BER value of the simulated cable without equalization is higher than the BER value of the physical cable without equalization even when the noise power of the simulated channel is set to 0 (Eb/N0 > 100). The BER magnitude for the simulated cable is 2.27E-5 with EQ and 3.752E-3 without EQ, and the BER magnitude for the physical cable is 0 with EQ and 3.2E-2 without EQ. Therefore the BER of the physical and simulated cable did not match magnitudes for any Eb/N0 value since the noise could not be decreased to a lower value.

2GHz, Taps = 4: The BER value of the simulated cable without equalization is higher than the BER value of the physical cable without equalization even when the noise power of the simulated channel is set to 0 (Eb/N0 > 100). The BER magnitude for the simulated cable is 4.55E-4 with EQ and 6.39E-3 without EQ, and the BER magnitude for the physical cable is 0 with EQ and 3.2E-2 without EQ. Therefore the BER of the physical and simulated cable did not match magnitudes for any Eb/N0 value since the noise could not be decreased to a lower value.

2GHz, Samples = 1601: The BER values of the simulated cable with and without equalization did not match the physical cable's BER magnitudes. The BER magnitude for the simulated cable is 9.25E-3 with EQ and 6.25E-4 without EQ, and the BER magnitude for the physical cable is 1.4E-2 with EQ and 3.2E-2 without EQ. For the physical cable, the BER is worse with equalization while with the simulated cable the BER is worse without equalization. The simulated cable's BER measurements, even with different noise powers, did not match the physical cable's BER magnitudes of 10^{-3} with EQ and 10^{-4} without EQ. This is likely due to the small number of simulation samples.

2GHz, Samples = 25602: The BER value of the simulated cable without equalization is higher than the BER value of the physical cable without equalization even when the noise power of the simulated channel is set to 0 ($Eb/N0 > 100$). The BER magnitude for the simulated cable is 2.80E-3 with EQ and 1.57E-2 without EQ, and the BER magnitude for the physical cable is 0 with EQ and 3.2E-2 without EQ. Therefore the BER of the physical and simulated cable did not match magnitudes for any Eb/N0 value since the noise could not be decreased to a lower value.

2GHz, PRBS = 4: The BER value of the simulated cable without equalization is higher than the BER value of the physical cable without equalization even when the noise power of the simulated channel is set to 0 ($Eb/N0 > 100$). The BER magnitude for the simulated cable is 4.77E-4 with EQ and 2.00E-3 without EQ, and the BER magnitude for the physical cable is 0 with EQ and 3.3E-2 without EQ. Therefore the BER of the physical and simulated cable did not match magnitudes for any Eb/N0 value since the noise could not be decreased to a lower value.

2GHz, PRBS = 12: The BER value of the simulated cable without equalization is higher than the BER value of the physical cable without equalization even when the noise power of the simulated channel is set to 0 ($Eb/N0 > 100$). The BER magnitude for the simulated cable is 1.23E-3 with EQ and 3.38E-3 without EQ, and the BER magnitude for the physical cable is 0 with EQ and 3.6E-2 without EQ. Therefore the BER of the physical and simulated cable did not match magnitudes for any Eb/N0 value since the noise could not be decreased to a lower value.

2GHz, Data = 50MBPS: The BER magnitudes for the simulated cable matches the physical cable when the Eb/N0 is set to 14.5dB. Both the BER with and without equalization matches the same magnitude of the simulated vs. physical cable of 0 with EQ and 10^{-3} without EQ. Therefore the simulated cable, when the Eb/N0 is set to 14.5dB, is representative of the physical cable BER measurements.   An Eb/N0 of 14.5dB is a valid value for typical operation of a link (between 10dB and 20dB), although slightly low [20].

For comparing equalization scheme improving link (all CAT7 15ft channel, and all variables set to control values unless specified):

1GHz, Control: The BER decreases (improves) with equalization for both the simulated channel, when Eb/N0 is 16dB, and the physical channel from 10^{-3} to 10^{-5} BER. The BER also decreases with equalization for the simulated channel at all Eb/N0 values greater than 10dB (see BER vs. Eb/N0 graph in Figure 4-22).

1GHz, Step Size = .001: The BER decreases (improves) from 10^{-3} to 0 BER when adding equalization with the simulated channel and 16dB Eb/N0. The BER also decreases from 10^{-2} to 0 BER when adding equalization with the physical CAT7 15ft channel. The BER also decreases with equalization for the simulated channel at all Eb/N0 values greater than 10dB (see BER vs. Eb/N0 graph in Figure 4-23Figure 4-22).

1GHz, Taps = 4: The BER decreases (improves) with equalization for both the simulated channel, when Eb/N0 is 13dB, and the physical channel from 10^{-2} to 10^{-3} BER. The BER also decreases with equalization for the simulated channel at all Eb/N0 values greater than 10dB (see BER vs. Eb/N0 graph in Figure 4-24).

1GHz, Samples = 1601: The BER increases from 10^{-2} to 10^{-3} BER when adding equalization with the simulated channel and 16dB Eb/N0. BER also increases from 0 to with the physical CAT7 15ft channel when adding equalization. The BER also increases when equalization is added for all Eb/N0 values for the simulated channel (see BER vs. Eb/N0 graph in Figure 4-25). The increase in BER for adding equalization is because the equalization does not have time for the tap values to settle, thus causing the addition of incorrect equalization, causing bit errors higher than without equalization.

1GHz, Samples = 25602: The BER decreases (improves) with equalization for both the simulated channel, when Eb/N0 is 17dB, and the physical channel from 10^{-3} to 0 BER. The Eb/N0 simulation for sweeping noise power with the simulated channel is not run, because the results are not needed for comparison.

1GHz, PRBS = 4: The BER is the same for with and without equalization for the physical channel. The BER decreases (improves) with equalization for the simulated channel when Eb/N0 is 20dB from 10^{-5} to 0 BER. The BER also decreases with equalization for the simulated channel at all Eb/N0 values greater than 8dB (see BER vs. Eb/N0 graph in Figure 4-26).

1GHz, PRBS = 12: The BER decreases (improves) from 10^{-2} to 10^{-5} BER when adding equalization with the simulated channel and 15dB Eb/N0. The BER also decreases from 10^{-2} to 10^{-4} BER when adding equalization with the physical CAT7 15ft channel. The BER also decreases with equalization for the simulated channel at all Eb/N0 values greater than 9dB (see BER vs. Eb/N0 graph in Figure 4-27).

1GHz, Data = 50MBPS: The BER is the same for with and without equalization for the physical channel of 0. The BER decreases (improves) with equalization for the simulated channel when Eb/N0 is 14.5dB from 4.39E-5 to 0 BER. The BER also decreases with equalization for the simulated channel for all Eb/N0 values (see BER vs. Eb/N0 graph in Figure 4-28).

2GHz, Control: The BER decreases (improves) from 10^{-2} to 0 BER when adding equalization with the simulated channel and no noise power (Eb/N0 > 100). The BER also decreases from 10^{-3} to 0 BER when adding equalization with the physical CAT7 15ft channel. The BER also decreases with equalization for the simulated channel for all Eb/N0 values (see BER vs. Eb/N0 graph in Figure 4-22).

2GHz, Step Size = .001: The BER decreases (improves) from 10^{-2} to 0 BER when adding equalization with the simulated channel and no noise power (Eb/N0 > 100). The BER also decreases from 10^{-3} to 10^{-5} BER when adding equalization with the physical CAT7 15ft channel. The BER also decreases with equalization for the simulated channel for all Eb/N0 values (see BER vs. Eb/N0 graph in Figure 4-23Figure 4-22).

2GHz, Taps = 4: The BER decreases (improves) from 10^{-2} to 0 BER when adding equalization with the simulated channel and no noise power (Eb/N0 > 100). The BER also decreases from 10^{-3} to 10^{-4} BER when adding equalization with the physical CAT7 15ft channel. The BER also decreases with equalization for the simulated channel for all Eb/N0 values (see BER vs. Eb/N0 graph in Figure 4-24).

2GHz, Samples = 1601: The BER of the physical channel increased from 10^{-4} to 10^{-3} with the addition of equalization, which is the result of not enough time for the equalization tap values to settle (LMS error to settle). The BER of the simulated channel decreased with the addition of equalization from 10^{-2} to 10^{-2} (same magnitude but lower value), but less than the control, which is also the result of not enough time for the equalization tap values to settle. The Eb/N0 simulation for sweeping noise power could not be run since the group delay of the simulated channel was greater than 1601 samples for a sample rate of 160MHz (see BER vs. Eb/N0 graph in Figure 4-25).

2GHz, Samples = 25602: The BER decreases (improves) from 10^{-2} to 0 BER when adding equalization with the simulated channel and no noise power (Eb/N0 > 100). The BER also decreases from 10^{-2} to 10^{-3} BER when adding equalization with the physical CAT7 15ft channel. The Eb/N0 simulation for sweeping noise power with the simulated channel is not run, because the results are not needed for comparison.

2GHz, PRBS = 4: The BER decreases (improves) from 10^{-2} to 0 BER when adding equalization with the simulated channel and no noise power (Eb/N0 > 100). The BER also decreases from 10^{-3} to 10^{-4} BER when adding equalization with the physical CAT7 15ft channel. The BER also decreases with equalization for the simulated channel for all Eb/N0 values (see BER vs. Eb/N0 graph in Figure 4-26).

2GHz, PRBS = 12: The BER decreases (improves) from 10^{-2} to 0 BER when adding equalization with the simulated channel and no noise power (Eb/N0 > 100). The BER also decreases from 10^{-3} to 10^{-3} BER (same magnitude but lower value) when adding equalization with the physical CAT7 15ft channel.   The BER also decreases with equalization for the simulated channel for all Eb/N0 values (see BER vs. Eb/N0 graph in Figure 4-27).

2GHz, Data = 50MBPS: The BER decreases (improves) from 10^{-3} to 0 BER when adding equalization with the simulated channel and no noise power (Eb/N0 > 100). The BER also decreases from 10^{-3} to 0 BER when adding equalization with the physical CAT7 15ft channel.   The BER also decreases with equalization for the simulated channel for all Eb/N0 values (see BER vs. Eb/N0 graph in Figure 4-28).

4.6.3 Conclusion of Chapter 4.6

The overall conclusion of this section is that the simulated channel, even with added simulated noise, does not always have the same magnitude BER of the physical channel when using the VSA and VSG, even across different simulation and data parameters for wired channels. The magnitude of the BER with and without equalization did not always match for the simulated and real channel tests.

The decision directed feed forward LMS equalization scheme improves (decreases) the BER across different simulation and data parameters for CAT7 15ft with 1GHz and 2GHz carrier. The decrease in BER from adding the equalization scheme is more than an order of magnitude for most of the tests. Also the 2GHz carrier frequency results show a more consistent improvement than 1GHz carrier when adding equalization because the quality of the CAT7 15ft channel is worse at 2GHz than 1GHz. Equalization Verification has successfully shown that this equalization scheme, modeled in SystemVue, improves the link quality by reducing BER under different conditions, under the conditions specified in Table 4-10.

5. *Analysis and Results of Equalization Verification over Wireless Channels*

This chapter will cover the analysis and results of testing this thesis's equalization scheme, decision directed feed forward LMS equalizer over a wireless channel using the Equalization Verification Setup as described in Chapter 3. The wireless channel to be tested is a "Super Power Supply 2dBi 2.4GHz Dual Band WiFi Antenna Style 1 for Routers" which is a 2.4GHz WiFi Router Dipole Antenna with 2dBi gain as shown in Figure 5-1 [29]. This antenna is a typically used antenna for WiFi routers carrying digital baseband data. The frequencies to be tested are 2.4GHz with 80MBPS and 50MBPS baseband data.

Figure 5-1: 2.4GHz WiFi Router Diploe Antenna made by Super Power Supply [29]

In this chapter, first the s-parameter measurements for the Antenna will be presented. Then the simulated and physical channel Equalization Verification results from will be presented. Then the simulated and physical channel results will be compared to evaluate the testing setup. Finally the equalization scheme will be evaluated based on its performance over the simulated and physical channel, and if the link's performance improved with the addition of the equalization scheme.

5.1 S-parameter Measurements of Wireless Channels

The procedure to measure the 2.4GHz Dipole Antenna and store the S2P (touchstone) file is as follows (Figure 5-2):

- Calibrate the VNA to desired range

- Connect the SMA to SMA cable from calibrated connections to Antennas (SMA cable included in s-parameter measurement)

- Set Antennas 0.4m away from each other, fixed location for measurement (0.4m for VSA/VSG setup as well)

- Import the S2P file to the connected computer (via GPIB)

- Import the S2P to Keysight's Advanced Design System (ADS) Software

- Graph the S2P file
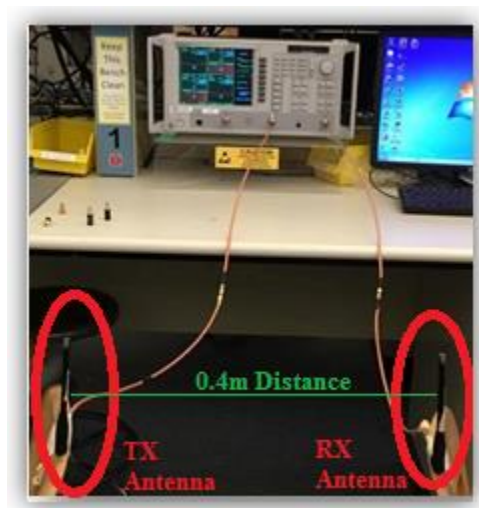
Figure 5-2: 2.4GHz Dipole Antenna VNA S-parameter Measurement Setup; 0.4m distance

The 2.4GHz Dipole Antenna is measured with a Vector Network Analyzer (VNA) and the graphs in Figure 5-3, Figure 5-4, and Figure 5-5 show different s-parameter measurements and ranges.

The S11 measurements for both the TX and RX antenna show that the antennas are designed for 2.4GHz in Figure 5-3 since the S11 is less than -20dB for both TX and RX antenna.
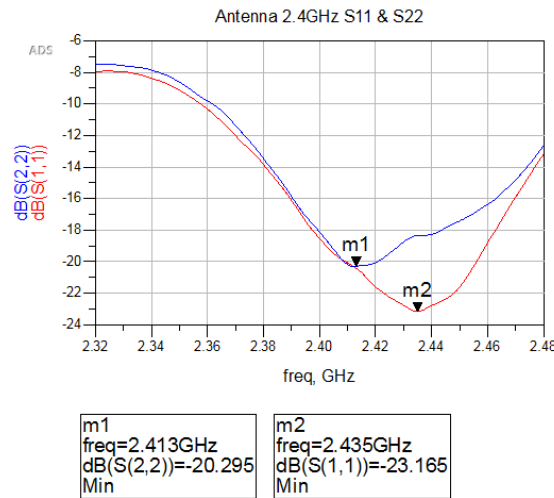
Figure 5-3: 2.4GHz Dipole Antenna S11 measurements for both TX and RX Antenna; blue is RX, red is TX

The S21 measurements of the 2.4GHz Dipole Antennas show the frequency range that will be tested for the Equalization Verification measurements throughout this chapter in Figure 5-4. The variations in S21 across the desired frequency range, 2.4GHz center with 160MHz span, show the required equalization to be performed to improve the quality of the link.
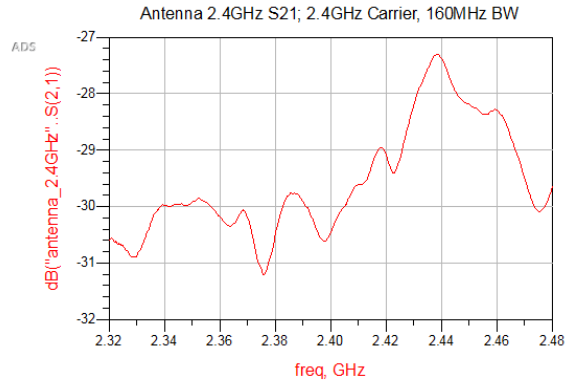
Figure 5-4: 2.4GHz Dipole Antenna S21 measurements; across frequency range for Equalization Verification testing

A larger S21 frequency range is showed in Figure 5-5 in order to give more context for the smaller 160MHz span that the equalization verification measurements will be performed.
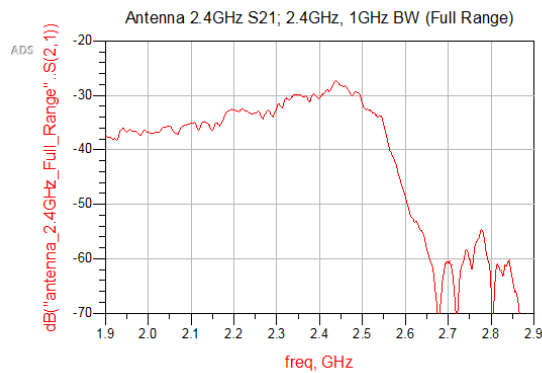
Figure 5-5: 2.4GHz Dipole Antenna S21 measurements across 1GHz range; gives context for 160MHz BW

5.2 Equalization Verification Simulated Wireless Channel Results

The simulated wireless channel results are presented in this section which includes BER results for a specific noise power, and a Eb/N0 graphs for a swept noise power. The S2P file for the 2.4GHz WiFi Router Antenna is used to simulate the BER results and Eb/N0 graphs. The Eb/N0 calculations for the wireless channel are the same as the wired channel since they are both under the assumption of additive white Gaussian noise.

5.2.1 BER Results for Measured Noise Level

The BER results in this section are found from the simulated wireless channels (S2P) with added noise. The noise power levels used in the simulated channel correspond to the noise level approximated when making the VSG/VSA measurements using the physical wireless channels in Chapter 5.3.

Table 5-1: BER Results for Simulated Channels using Measured Noise Levels

Channel Type	Distance	Carrier	Sample Rate	Input Delay	VGA Gain	Eb/N0 for Physical Channel	BER w EQ**	BER wo EQ**
Antenna	.4m	2.4GHz	160MHz	139	35	29	0.00E+00	8.79E-05
Antenna	.4m	2.4GHz	100MHz	83	30	10	5.27E-04	2.06E-03

**Simulated noise level set according to Eb/N0 noise level of physical channel

The simulation results are presented in Table 5-1. The simulation parameters used for the results in Table 5-1 can be seen in Table 5-2.

Table 5-2: Simulated 2.4GHz Antenna BER Simulation Parameters

TX Setup				Simulation Setup					LMS Param		BER Settings	
Input Data	PRBS	Carrier	BW	Sim Time	Sample Rate	Num Samples	Time Spacing	Freq Res	Num Taps	Step Size	BER start (delay)	BER delay bound
80 Mbps	7	2.4 GHz	100 & 160 MHz	80us	100 & 160 MHz	32768	6.25E-3 us	12.499 kHz	10	0.0001	10000	10

A few notes on the BER results for the simulated channel:

- The sample rate is chosen to be twice the Input data, which is twice the required Nyquist rate. This is to allow for a baseband pulse of BPSK without any special modulation.

- The BER settings the same for with and without EQ

- The BER recording start is at 10000, so the LMS has time to settle

- The BER delay bound is the amount of potential forward deviation in input vs. output bits for BER calculation.

The input delay corresponds to the s-parameter file's (S2P) simulated delay (group delay) and the VGA gain is found by iteratively changing the delay until the channel's input and output. This is an iterative process in includes changing the delay, looking at the graphs of the baseband input and output of channel, and adjusting the delay until they match. The VGA gain is used to emulate a Variable Gain Amplifier that auto adjusts to a correct fixed value in an increment of +/-5. The VGA gain is confirmed based on the calculated path loss, for a 2.4GHz carrier frequency, 0.4m distance, propagating through free space, with TX and RX antennas with 2dBi gain, for 25.37 V/V path loss.

5.2.2 Eb/N0 Graphs

Eb vs. N0 graphs are simulated by sweeping noise power. See Chapter 2 for background on Eb/N0 graphs and how they relate to Signal to Noise ratio. Also see Chapter 3 for how to simulate the Eb/N0 graphs for each channel. The Eb/N0 graphs are used to identify the possible noise levels when measuring the physical 2.4GHz Dipole Antenna using the VSG and VSA, and to show that the equalization scheme works across different noise levels.

The two Eb/N0 graphs for the 2.4GHz Dipole Antenna use 160MHz sample rate, 80MBPS and 50MBPS data rate, 32768 num samples, and 10000 BER delay. VGA and delay specified in Table 5-1.
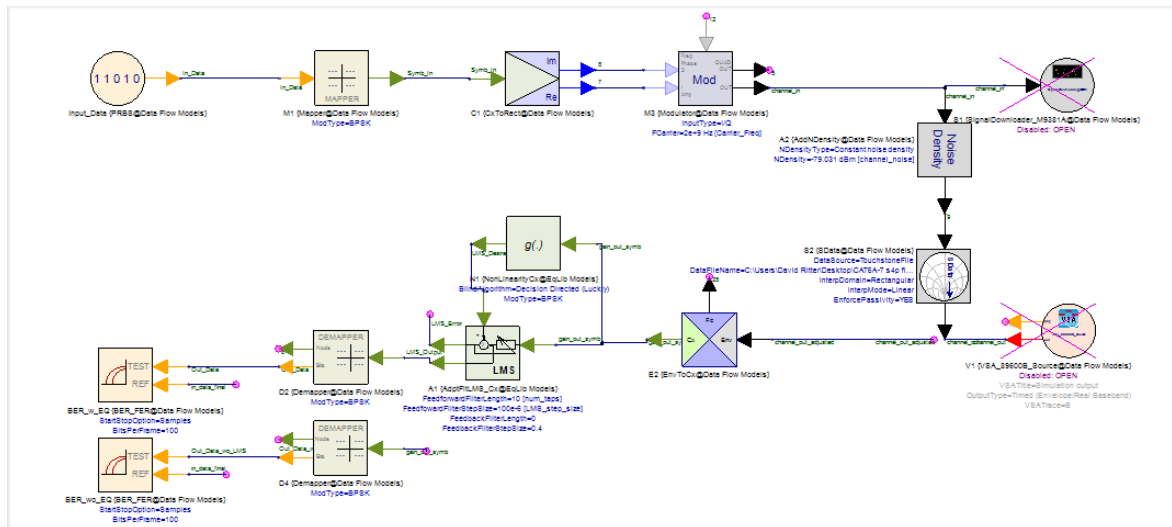
Figure 5-6: Eb/N0 simulation setup; with S2P channel and Noise density

Analysis of the simulated Eb/N0 graphs for the wireless channel is in Chapter 5.5.
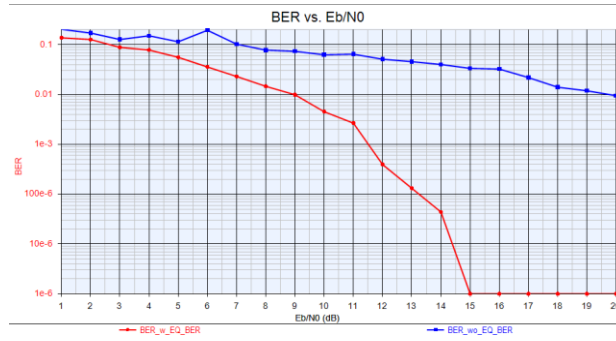
Figure 5-7: Eb/N0 Graph of 2.4GHz Dipole Antenna, 2.4GHz center, 160MHz span, 80MBPS data
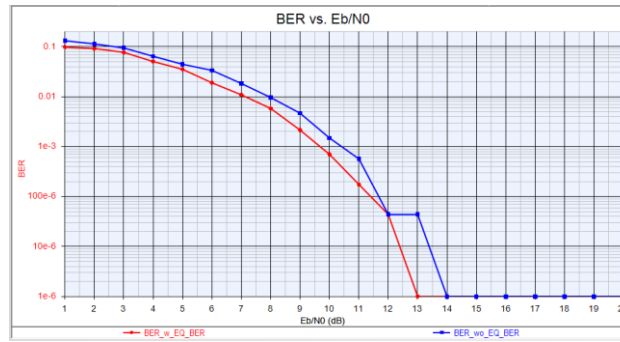
Figure 5-8: Eb/N0 Graph of 2.4GHz Dipole Antenna, 2.4GHz center, 100MHz span, 50MBPS data

5.3 Equalization Verification Physical Wireless Channel Results

Physical wireless channel is measured with the procedures outlined in Chapter 3 for taking the BER measurements using the SystemVue in combination with the VSG, VSA, and physical channel. The physical wireless channel that is tested is the 2.4GHz WiFi Router Antenna.

5.3.1 BER Results

The BER results in Table 5-3 are found using the Equalization Verification Setup using physical wireless channels. The BER simulations used the simulation parameters in Table 5-4 and Table 5-5.

Table 5-3: BER Results for Physical Wireless Channels

Channel Type	Distance	Carrier	Sample Rate	Input Delay	VGA Gain	Average* BER w EQ	Average* BER wo EQ	Eb/N0 for same BER (approx)
Antenna (WiFi)	.4m	2.4 GHz	160MHz	139	35	0.00E+00	9.09E-05	29
Antenna (WiFi)	.4m	2.4 GHz	100MHz	83	30	0.00E+00	4.02E-03	10

*Average is across 5 trial, because sampling rate caused large phase error

Table 5-4: Physical 2.4GHz Dipole Antenna BER TX Setup and Sim Setup

TX Setup				Simulation Setup				
Input Data	PRBS	Carrier	BW	Sim Time	Sample Rate	Num Samples	Time Spacing	Freq Res
80 Mbps	7	2.4GHz	100 & 160MHz	80us	100 & 160MHz	12801	6.25E-3 us	12.499 kHz

Table 5-5: Physical 2.4GHz Dipole Antenna BER LMS Param and BER Settings

LMS Param		BER Settings			
Num Taps	Step Size	Output Delay	Input Delay	BER start (delay)	BER delay bound
10	0.0001	3	0	4000	10

A few notes on the BER results for the simulated channel:

- The sample rate is chosen to be twice the Input data, which is twice the required Nyquist rate. This is to allow for a baseband pulse of BPSK without any special modulation.

- The BER settings the same for with and without EQ

- The BER recording start is at 4000, so the LMS has time to settle

- The BER delay bound is the amount of potential forward deviation in input vs. output bits for BER calculation.

- The Input and Output Delay are used for BER calculations only. The Output delay is non-zero in order to allow the input to precede the output (casual).

- Sometimes the BER would be greater than .10 for both with and without EQ (unexpected for certain setup), these results would be a result of excessive and outside disturbance and would be thrown out (not included in average).

The input delay corresponds to the s-parameter file's (S2P) simulated delay (group delay) and the VGA gain is found by iteratively changing the delay until the channel's input and output. This is an iterative process in includes changing the delay, looking at the graphs of the baseband input and output of channel, and adjusting the delay until they match. The VGA gain is used to emulate a Variable Gain Amplifier that auto adjusts to a correct fixed value in an increment of +/-5. The VGA gain is also verified against the path loss equation as calculated in Chapter 5.2.1, of 25.37 V/V path loss.

5.3.2 Graphs Produced by SystemVue Simulation

An example of the SystemVue graphs produced from a simulated wireless channel measurement is outlined in this section. The same type of graphs are also produced when running the Equalization Verification setup with the physical wireless channel, and are used to verify the setup is running properly and the BER results are valid. All graphs in this section are from a simulated 2.4GHz Dipole Antenna at 2.4GHz carrier, 160MHz bandwidth with 80MBPS data.

The "Align Input" graph in Figure 5-9 is used to compare the baseband data of the input of the channel vs. the baseband output of the channel. This graph is used to iteratively find the simulated channel delays found in Table 5-1 by adjusting the channel input delay for the channel's input and output baseband signals to align.
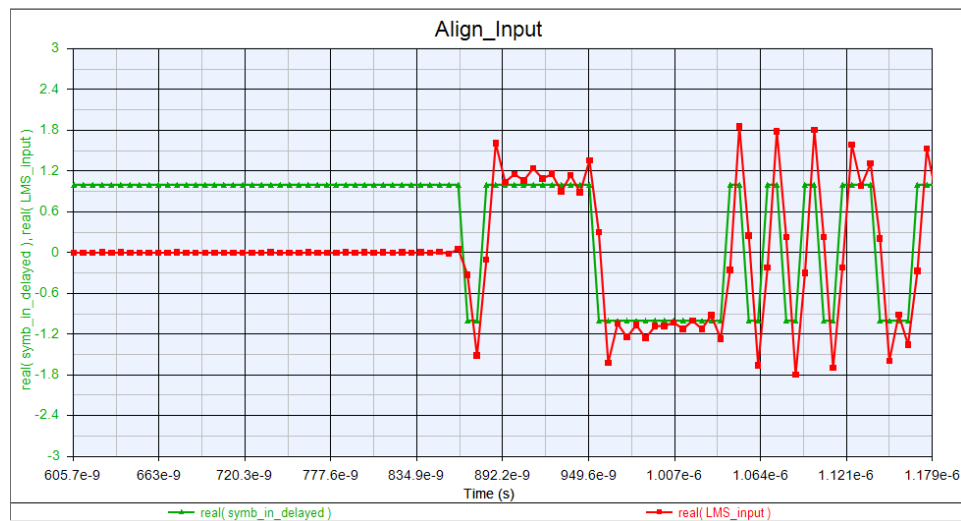
Figure 5-9: Align Input graph used to iteratively find the input delay for simulated 2.4GHz Antenna

An example of the spectrums for both the input and output of the simulated channel can be seen in Figure 5-10. The channel output spectrum is an attenuated version of the input spectrum by the S21 loss of the channel. The S21 loss of the simulated channel, in this

example graph, can be seen below in order to show the attenuation of the signal by the channel.
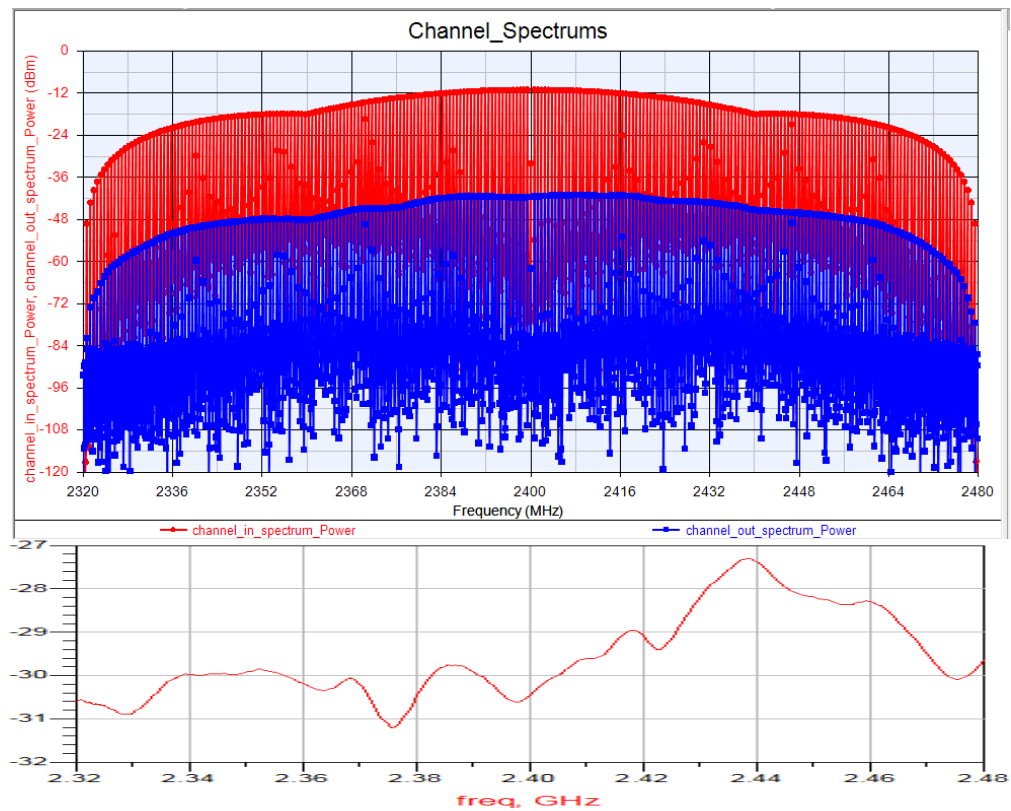
Figure 5-10: Simulated Input and Output Channel Spectrums using 2.4GHz Dipole Antenna 2.4GHz; 2.4GHz Antenna S21 graph is plotted below to show the expected attenuation

The LMS error for the equalization scheme is plotted in Figure 5-11. The LMS error is the difference between the output of the equalization and the input of the equalization. The LMS error must converge for the most accurate reading of BER, and is the main reason the BER calculations are delayed. The BER start time must be greater than when the LMS error converges for the smallest and most accurate BER measurement when using equalization. This applies for both a simulated and physical channel. The BER results for Chapter 6 are presented with the LMS error converging. These results can be

seen in Table 5-1, for the simulated wireless channel, and in Table 5-3, for the physical wireless channel.
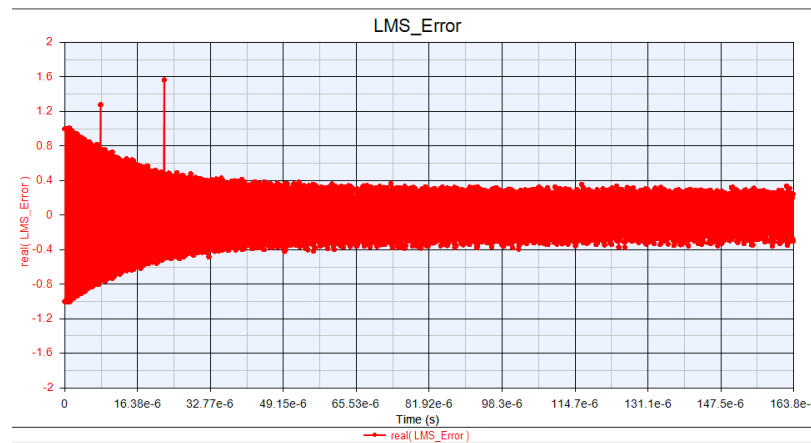
Figure 5-11: LMS error is the difference between the Equalization output and desired output; the LMS error converges once the LMS taps settle

The LMS output in Figure 5-12, when zoomed out, can be seen to correlate with the LMS error in Figure 5-11. The "LMS inputs" graphs of Figure 5-12 and Figure 5-13 plot the LMS input, LMS output, and desired signal. The LMS input is the demodulated channel output in the time domain, which is equivalent to a non-equalized received signal. The desired output of the LMS block is the LMS input that is set to a 1 or 0 value (decision directed). The LMS output is the LMS input multiplied by a delayed version of the input determined by the LMS taps. This is representative of the decision directed feed forward LMS equalizer that is used on all measurements in Chapters 4 and 5.
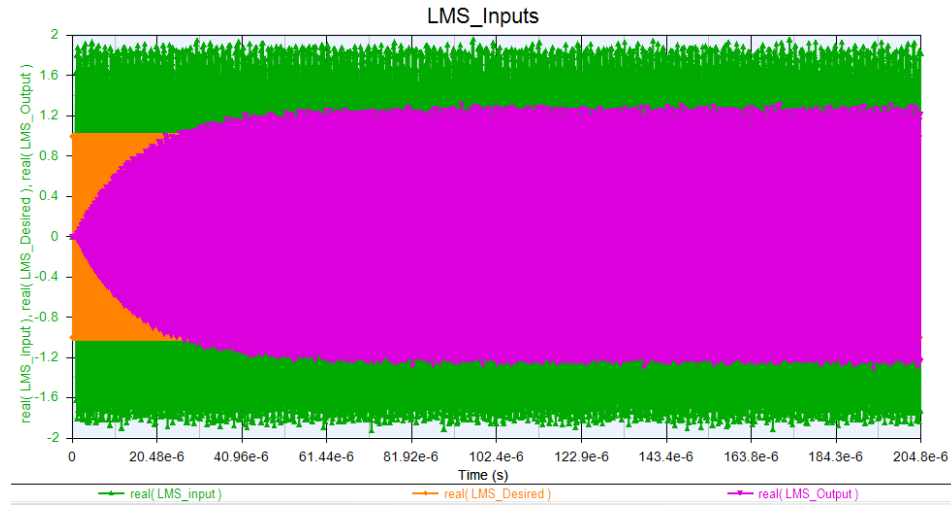
Figure 5-12: LMS Input and Outputs (zoomed out) to show that the LMS (EQ) output follows the LMS error, once the LMS tap values settle

A zoomed in version of the same graph of Figure 5-12 can be seen in Figure 5-13. The zoomed in graph of the LMS inputs and outputs shows that the LMS output tracks the desired signal better than the LMS input. This signifies that the equalizer is performing its function correctly and should decrease the BER compared to a non-equalized signal.
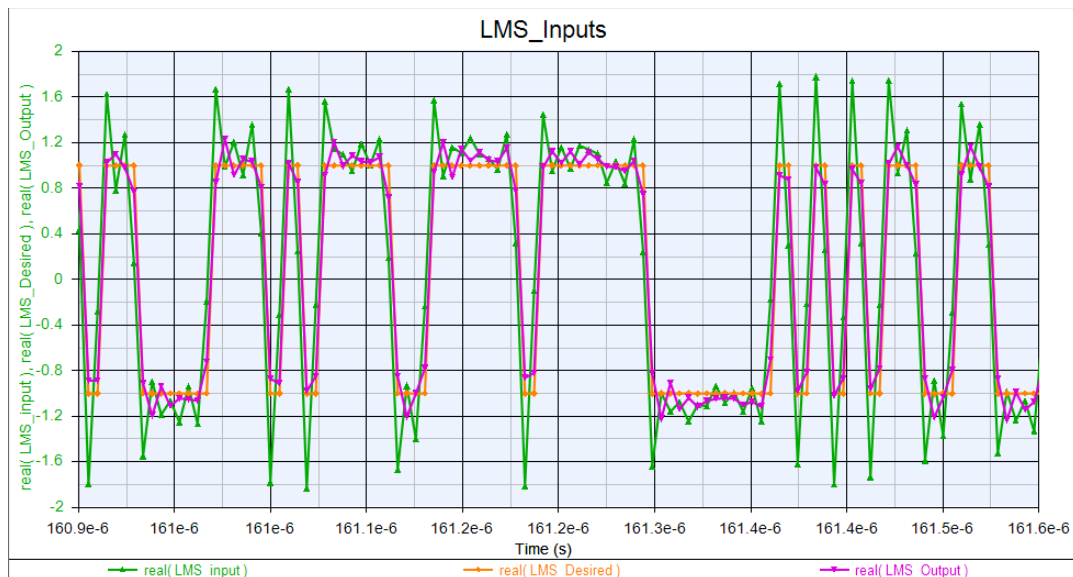
Figure 5-13: LMS Input and Outputs once the taps have settled; the LMS output (with EQ) follows the desired signal better than the LMS input (without EQ)

5.4 Evaluation of Wireless Testing Setup

This section compares the simulated to physical channel BER results in order to determine if the wireless testing setup is valid. The simulated noise power is determined by finding the simulated noise power that produced the same BER as the physical channel. The noise value varies from trial to trial due to the variable phase noise of the VSA in combination with the VSG and is discussed in more detail in Chapter 3.4.4.

The BER of the Equalization Verification setup using the physical channel is compared to the BER of the simulated channel. Table 4-3 presents a side-by-side comparison of the BER measurements with the physical and simulated channel.

Table 5-6: BER comparison for Wireless Simulated and Physical Channel

Channel Type	Dist-ance	Carrier	Data/Sample Rate	Physical Channel			Simulation	
				Average* BER w EQ	Average* BER wo EQ	Eb/N0 for Physical Channel	BER w EQ**	BER wo EQ**
Antenna	.4m	2.4 GHz	80MBPS / 160MHz	0.00E+00	9.09E-05	29	0.00E+00	8.79E-05
Antenna	.4m	2.4 GHz	50MBPS / 100MHz	0.00E+00	4.02E-03	10	5.27E-04	2.06E-03

	=	EQ has better BER
	=	(approx) same BER
	=	
	=	

*Average is across 5 trial, because sampling rate caused large phase error (non-deterministic)

**Simulated noise level set according to Eb/N0 noise level of physical channel

Note: input delay and VGA gain according to Table 5-1

Wireless simulated and physical channel testing setup is the same as Chapters 5.2 and 5.3 (Table 5-4 and Table 5-5).

A detailed analysis of both baseband data (signal bandwidth) for the 2.4GHz Dipole Antenna follows for comparing the simulated vs. physical channel:

2.4GHz Dipole Antenna, 80MBPS (160MHz sample rate): The BER magnitudes for the simulated cable match the physical cable when the Eb/N0 is set to 29dB, i.e. the BER magnitude with EQ is 0 and the BER magnitude without EQ is 10^{-5}. Both the BER with and without equalization matches the same magnitude of the simulated vs. physical cable. Therefore the simulated cable, when the Eb/N0 is set to 29dB, is representative of the physical cable BER measurements since both magnitudes are the same (less than 10x different). An Eb/N0 of 29dB is a valid value for typical operation of a wireless link [20].

2.4GHz Dipole Antenna, 50MBPS (100MHz sample rate): Even when Eb/N0 is set to 10dB, the simulated cable BER measurements do not match the same magnitude for both with and without equalization. The BER magnitude for the simulated cable is 5.27E-4 with EQ and 2.06E-3 without EQ, and the BER magnitude for the physical cable is 0 with EQ and 4.02E-3 without EQ. Eb/N0 cannot be decreased from 10dB to match the BERs without EQ, because then the BER of the simulated cable with equalization will no longer match the physical cable BER with equalization.

A similar conclusion will be given as in Chapter 4.4 that the simulated channel, even with added simulated noise, is not always representative of the physical channel when using the VSA and VSG. This is likely due to a finite number of trials (5) when measuring across the physical channels, and the added phase noise of the VSA/VSG due to timing imperfections. Therefore, a conclusion will be made that if the VSA and VSG phase noise could be more accurately controlled, the physical channel BER measurements would follow current s-parameter simulated channel BER measurements.

5.5 Evaluation of Equalization Scheme over Simulated and Physical Wireless Channels

This section compares the BER results with and without the equalization scheme for the 2.4GHZ Dipole Antenna for 80MBPS and 50MBPS. The equalization scheme under test is the decision directed feed forward LMS equalizer as seen in Figure 4-21.
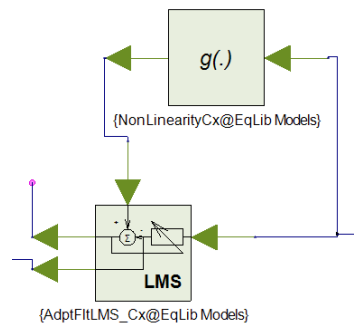
Figure 5-14: Decision Directed Feed Forward LMS Equalizer as implemented by SystemVue dataflow modeling blocks

The BER with and without this equalization scheme will be compared for both the simulated and physical wired channels across the given simulation parameters. Three components will be evaluated to determine if the equalization scheme improved the link for each wired channel: 1) the physical channel BER, 2) the simulated channel BER, 3) if the BER vs. Eb/N0 graph improved for all noise levels.

5.5.1 Evaluation of Typical Case Equalization Scheme

The two 2.4GHz antenna data rates are used to determine if the decision directed feed forward LMS equalizer (as modeled in SystemVue) improves the quality of the link according to the three criteria:

1. the physical channel BER

2. the simulated channel BER

3. if the BER vs. Eb/N0 graph improved for all noise levels

Each wireless setup from Table 5-7 will be analyzed independently and then a final section conclusion will be made.

Table 5-7: Evaluation of Equalization Scheme over Wireless Channel (Physical and Simulated)

				Physical Channel			Simulation		
Cha-nnel Type	Dist-ance	Carr-ier	Data/Sam ple Rate	Aver-age* BER w EQ	Aver-age* BER wo EQ	Eb/N0 for Physical Channel	BER w EQ**	BER wo EQ**	EbN0 Sim Better for EQ?
Antenna	.4m	2.4 GHz	80MBPS / 160MHz	0.00E+0	9.09E-05	29	0.00E+0	8.79E-5	Yes
Antenna	.4m	2.4 GHz	50MBPS / 100MHz	0.00E+0	4.02E-03	10	5.27E-4	2.06E-3	Yes (barely)

(yellow)	=	EQ has better BER
(orange)	=	(approx) same BER
(red)	=	
(purple)	=	

*Average is across 5 trial, because sampling rate caused large phase error (non-deterministic)

**Simulated noise level set according to Eb/N0 noise level of physical channel

Note: input delay and VGA gain according to Table 5-1.

Wireless simulated and physical channel testing setup is the same as Chapters 5.2 and 5.3 (Table 5-4and Table 5-5).

A detailed analysis of each channel type and length follows for the physical channel BER, simulated channel BER, and BER vs. Eb/N0 simulated graph:

2.4GHz Dipole Antenna, 80MBPS (160MHz sample rate): The BER decreases (improves) with equalization for both the simulated channel, when Eb/N0 is 29dB, and the physical channel from 10^{-5} to 0 BER. The BER also decreases with equalization for the simulated channel for all Eb/N0 values (see BER vs. Eb/N0 graph in Figure 5-7).

2.4GHz Dipole Antenna, 50MBPS (100MHz sample rate): The BER decreases (improves) from $4.02*10^{-3}$ to 0 BER when adding equalization with the simulated channel and Eb/N0 set to 10dB. The BER also decreases from $2.06*10^{-3}$ to $5.27*10^{-4}$ BER when adding equalization with the physical channel. The BER also decreases with equalization for the simulated channel at all Eb/N0 values (see BER vs. Eb/N0 graph in Figure 5-8).

5.5.2 Conclusion of Chapter 5

Overall the decision directed feed forward LMS equalization scheme improves the BER across both the simulated and physical 2.4GHz Dipole Antenna, and simulated noise power for 80MBPS. The Equalization Verification has successfully shown, for the cases examined, that this equalization scheme, modeled in SystemVue, improves the link quality by reducing BER under different conditions, for the 2.4GHz Dipole Antenna with 50MBPS and 80MBPS.

6. Transistor-Based SystemVue Model

This chapter presents an equalization scheme, modeled completely in SystemVue, which is more transistor based. Therefore this design is more portable to integrated circuit design tools. The dataflow blocks in SystemVue will be compared against their circuit equivalents step-by-step in order to ensure the reader that a behavioral equalizer designed in SystemVue is representative of its hardware implementation. First the main analog portion of the SystemVue design will be compared against an LTSpice circuit in Chapter 6.2. Then in Chapter 6.3, the digital portions of the design, for the equalization coefficient LMS algorithm, will be implemented in SystemVue and then exported to VHDL. The VHDL simulations will be compared to the SystemVue simulations. Chapter 6.4 will discuss all other blocks used in the design such as ADCs (Analog to digital converters) and DACs (Digital to analog converters). Then in Chapter 6.5 all the portions will be combined and tested using the Equalization Verification testing setup outlined in Chapter 3 and that was used in Chapters 4 and 5. Figure 6-1 shows the intended split of the analog and digital portions of the more realistic decision directed feed-forward LMS equalizer.
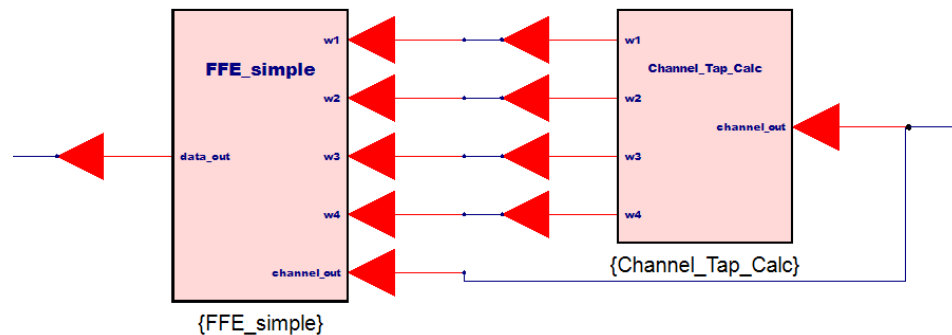
Figure 6-1: High Level Block Diagram of Transistor-Based Equalization Scheme Implemented in SystemVue; Analog (FFE simple) and digital (Channel_Tap_Calc) portions

The equalization scheme to be modeled is a 4-tap decision directed feed-forward LMS equalizer, a more simplified version of the equalizer used in Chapters 3, 4, and 5. The analog portion of the equalizer (FFE_simple) includes the "feed-forward" components (Chapter 6.2) while digital portion of the equalizer (Channel_Tap_Calc) includes the "decision directed" and "LMS" components (Chapter 6.3). The entire equalization design was integrated and tested to ensure the BER improves when equalization is added.

6.1 Motivation for a Transistor Based Model

Spice models are used by integrated circuit designers to model analog components at the transistor level. In order for this thesis to be of use to integrated circuit designers, the accuracy of the models must be examined. A designer must be confident that the SystemVue dataflow model of their equalization scheme accurately represents the chipset in which the equalization scheme is intended.

Two requirements must be met for this thesis to aid designers:

1. The equalization scheme successfully improves the quality of the link (lowers BER) when testing across an intended real channel

2. The equalization scheme SystemVue dataflow model accurately represents the transistor level design

The first requirement was covered in the results and analysis chapters (Chapters 4 and 5), and the second requirement is addressed in this chapter (Chapter 6).

6.2 Analog Comparison of SystemVue Model and LTSpice

In this section, SystemVue dataflow models of equalization components, Spice models are compared to the SystemVue dataflow behavioral models In order to ensure the accuracy. LTSpice will be used to create and run a simulation of the feed forward equalizer which includes the analog components of the equalization schemes. The tap values are set in the digital portion of the equalizer and will be inputs to the feed-forward equalizer portion of the design. The analog components include the input gain stage, the tap multipliers, and the input delays.

6.2.1 High Level Comparison

The high level comparison of the SystemVue dataflow model and the LTSpice spice model includes an input of the four tap level values (digital input), the channel output (analog input), and the data output (analog output) as seen in Figure 6-2.
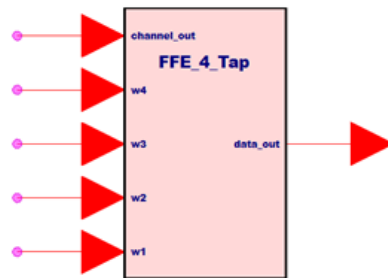
Figure 6-2: FFE_4_Tap Symbol; High Level Block Diagram for analog portion of transistor-based Equalization Model

The SystemVue dataflow model takes an input of four analog values to set the tap values. These channel tap values are not determined by this module, but are determined by the LMS Channel Tap Calculator module in Chapter 6.3. The tap inputs are used to set the

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differential tail current in each of the multiplication branches. The FFE_4_Tap taps, for both models, would be set by the digital output of the LMS block.

6.2.2 Block Level Comparison

The SystemVue dataflow model implementation can be seen in Figure 6-3 and shows the tap multiplication to delayed versions of the channel output (analog input). All the tap multiplications, w1, w2, w3, w4, are then summed together after being multiplied by delayed version of the channel output.
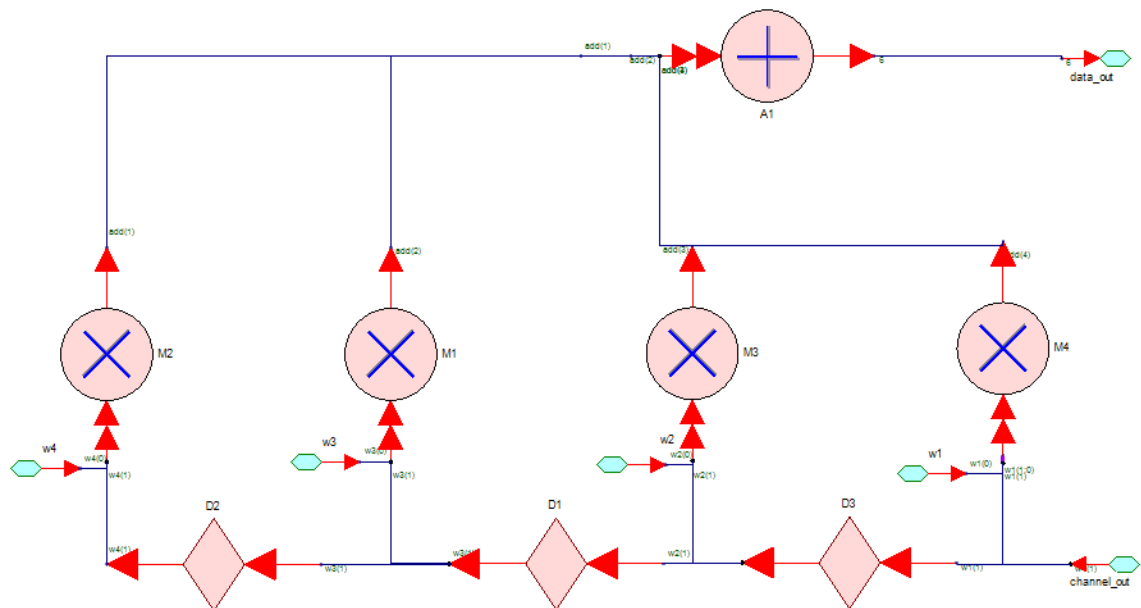
Figure 6-3: FFE_4_Tap SystemVue/Dataflow implementation, to be compared with LTSpice design

The SystemVue dataflow model in Figure 6-3 presents a much more straight forward and functional based approach to equalization. The feed forward equalizer is comprised of a summation of a multiplication of delayed versions of the input (channel output). The diamonds are delays, and the w1, w2, w3, w4 are the channel tap inputs to the module in Figure 6-3. The LTSpice model, corresponding to the SystemVue model, performs the same function but is implemented by transistors and ideal logic gates in Figure 6-4. The

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logic gates and ideal delays can be created by digital circuits, and thus by MOSFET transistors. The ideal components of the circuit can be implemented by transistors including the current sources (Tap1, Tap2, Tap3, Tap4), the flip-flops (A1,A2,A3), the XOR logic gates (A4-A9), and ideal voltage to voltage converters (E1-E6). The ideal components are used for each of design and can be implemented on a lower level.
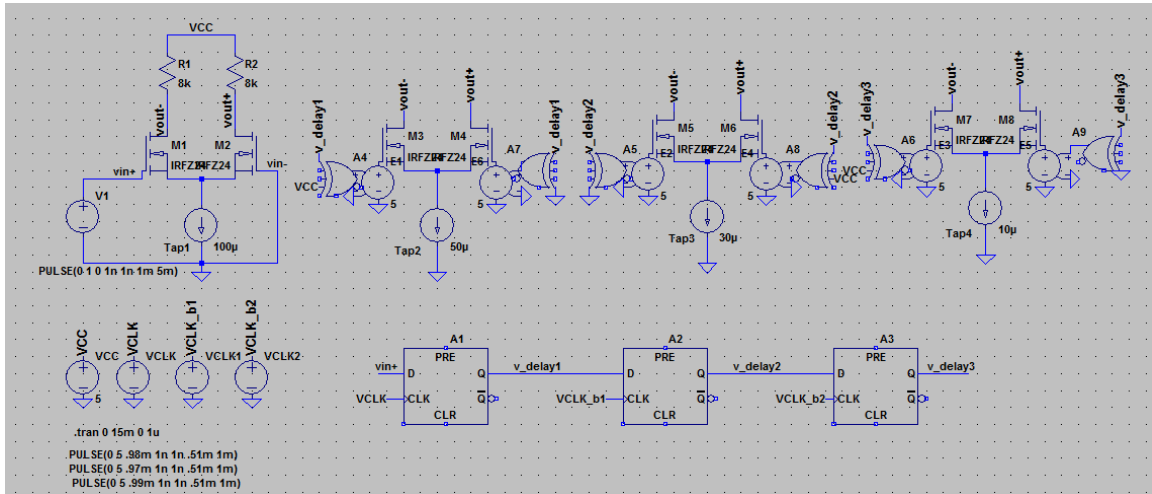
Figure 6-4: LTSpice Design of FFE_4_Tap; Circuit/Spice model of analog portion of equalization scheme

The delays of the LTSpice design of Figure 6-4 include A1, A2, A3 and correspond to the delays in the SystemVue model. The tap multiplications of Tap1, Tap2, Tap3, and Tap4 in the LTSpice model, implemented by the differential amplifiers with the set current gains, correspond to the multiplication of the taps in the SystemVue model. The tap values in the LTSpice model are determined by 100uA, 50uA, 30uA, 10uA, and the 8k ohm source resistors, and the sign of the taps correspond to the XOR inputs of each of the differential amplifiers. The tap values correspond to the values of [1,-.5,.6,.1], chosen for testing purposes only.

6.2.3 Functionality Comparison

The two models are implemented and tested with the tap values of [1,-.5,.6,.1] with a pulse input of 1ms width with a period of 6ms as seen in Figure 6-5. The testing conditions are to show functionality at a lower speed.
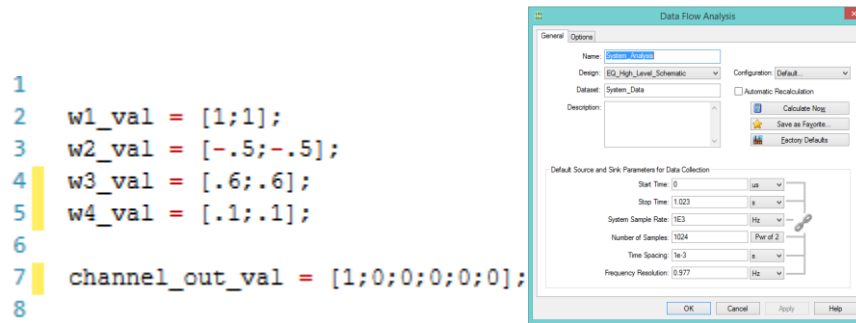
Figure 6-5: Feed-Forward Equalizer SystemVue dataflow model testing input

The SystemVue dataflow implementation of the feed-forward equalizer is tested using four input waveforms for the predetermined tap values, one analog input for the channel output, and a sink to monitor the data output which can be seen in Figure 6-6.
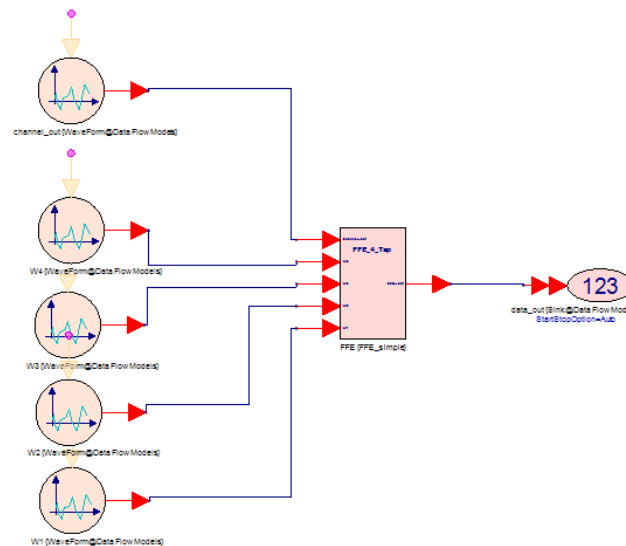
Figure 6-6: FFE_4_Tap SystemVue implementation, functional testing setup in SystemVue

The feed-forward equalizer SystemVue testing input and output can be seen in Figure 6-7. The channel output (blue in Figure 6-7) is simply the 1ms wide pulse with 6ms

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period. The data output (red in Figure 6-7) is the tap multplication of the input pulse with the tap multiplied by the delayed version of the pulse. The tap values of 1, -.5, .6 and .1 are multpiled to the delayed version of the channel output. The testing results of the SystemVue block perform exactly as expected since it is a behavrioal model.
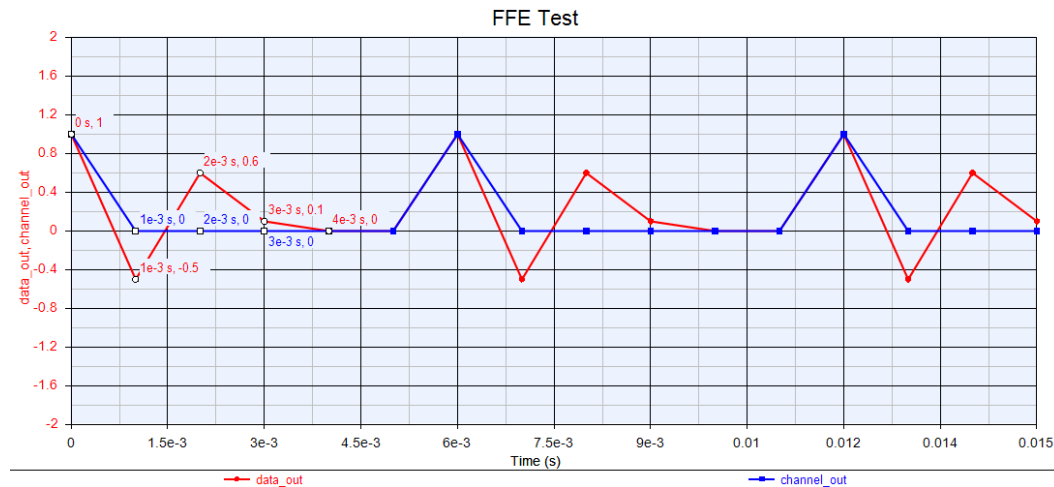
Figure 6-7: FFE_4_Tap SystemVue implementation testing output data waveform for taps =

[1,-.5,.6,.1]

Then the LTSpice model of the feed-forward equalizer is tested using the same testing parameters as used for the SystemVue model to show the similarity of the designs. The channel output (analog input to FFE) is a 1ms wide pulse with a 6ms period. The input and delayed versions of the input can be seen in Figure 6-8.
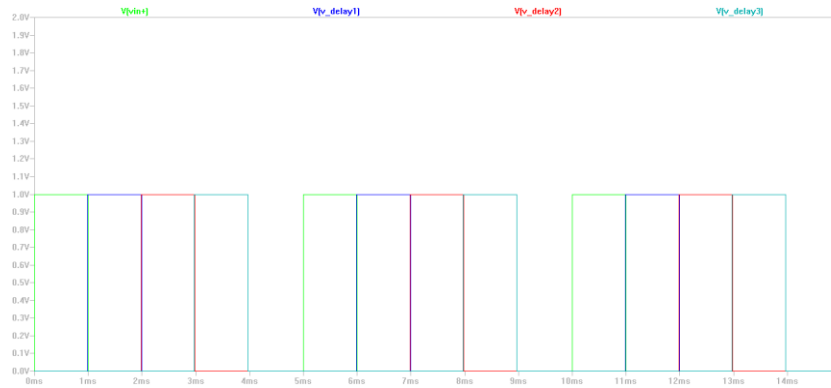
Figure 6-8: LTSpice FFE test input; green signal is input, and others are delayed versions of the input pulse

The LTSpice model's tap values are set with the differential tail current, current gain of the mosfet, and source resistor as seen in Figure 6-4. The output of the LTSpice model, with the set tap values, and input of 1ms wide pulse can be seen in Figure 6-9
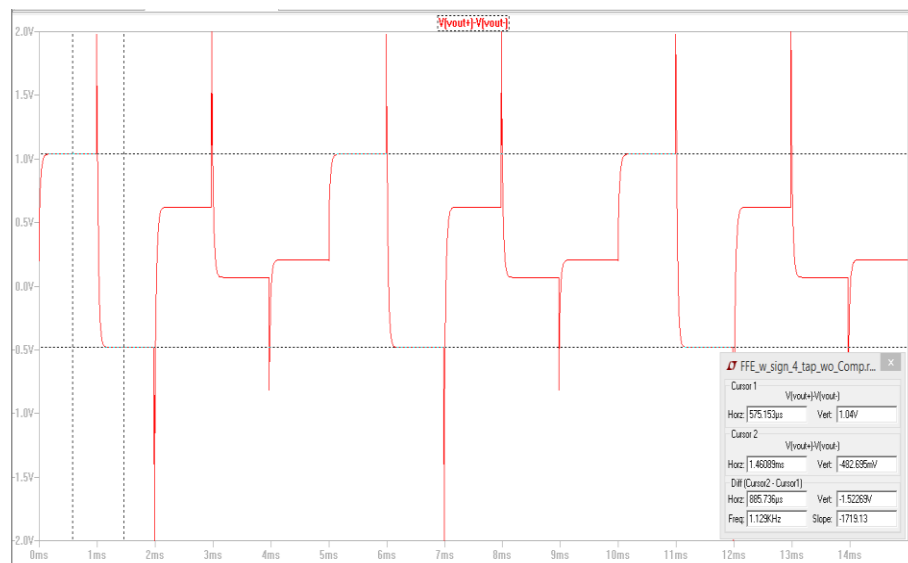
Figure 6-9: LTSpice testing output waveform; shows the input 1ms wide pulse multiplied by tap values of [1,-.5,.6,.1]

The actual levels of the output waveform are 1.04V, -.482V, .621V, and .069V compared to the expected values of 1V, -.5 V, .6V, and .1V. All are less than 10% error however, and match the same timing as the SystemVue model. Also each section of the LTSpice output waveform requires some charging time and a slight overshoot. This is to be

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expected from the non-ideal components of the MOSFETS including the gate and drain capacitance of each MOSFETS. The MOSFETS model used is the IRFZ24 with a gate capacitance of 25 nF so quite large compared to today's pF standard.

Overall the LTSpice implementation of the feed-forward equalizer, even with the non-ideal transistors, shows that the SystemVue behavioral model can be represented with transistors.

6.3 Digital Comparison of SystemVue Model and HDL

The digital, LMS Tap Calculator for generating the filter taps/coefficients, portion of the equalizer is covered in this section. The LMS Tap Calculator is used to generate the equalizer channel tap coefficients for adaptive equalization by using the channel output, error signal, and a fixed step size (See Background Chapter 2.4.1). The LMS block is first implemented in SystemVue using HDL blocks only, and then the HDL code is generated by SystemVue. The HDL code that is generated by SystemVue is tested in ModelSim to verify that the logic works as intended.

6.3.1 Overview of LMS Tap Calculator

The high level block diagram of the LMS Tap Calculator SystemVue model can be seen in Figure 6-10. The inputs to the LMS Tap Calculator include the x_input, or channel output, and the d_input, or the desired input. This LMS filter calculator calculates four tap values and outputs them as weight1, weight2, weight3, and weight4. The four weights or tap values are also multiplied to delayed versions of the x_input signal and output to the y_output. The error signal is a result of subtracting the y_output from the d_input and also used to calculate the filter tap values.
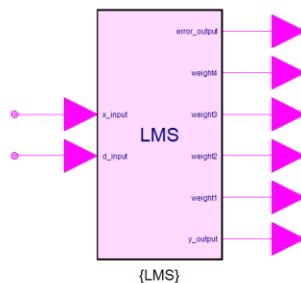
Figure 6-10: LMS Tap Calculator, high level block diagram, implemented in SystemVue HDL blocks

An implementation of the SystemVue LMS Tap Calculator can be seen in Figure 6-11. The blue ports specify where the inputs and outputs are attached and the block diagram shows the multiplication of the delayed versions of the inputs. A more in depth analysis of how an LMS filter tap calculator is included in the Background portion of this thesis in Chapter 2.
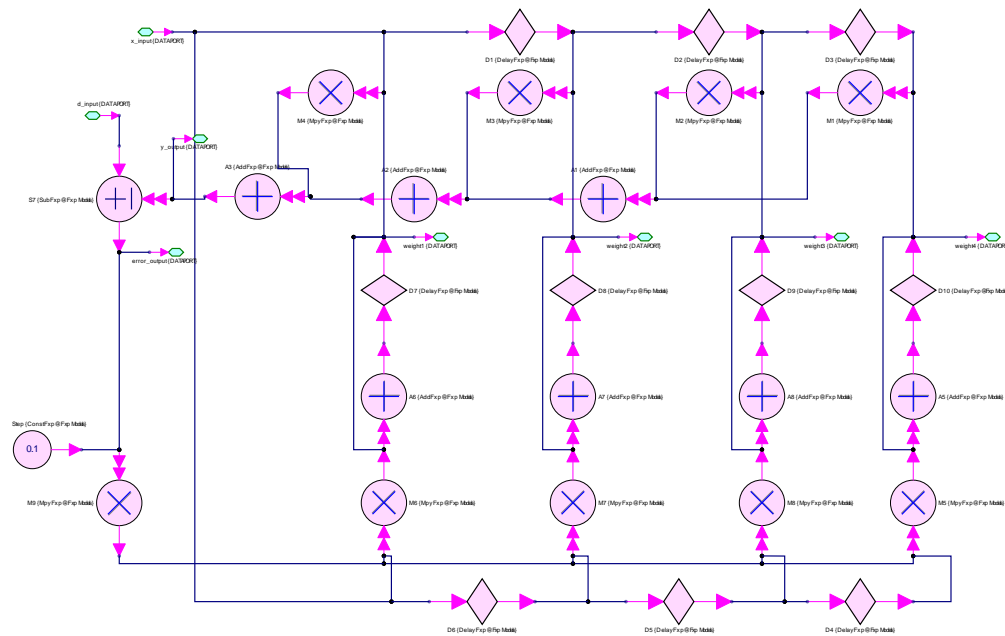
Figure 6-11: LMS Tap Calculator, low level block diagram, implemented in SystemVue HDL blocks

The SystemVue implementation of the LMS Tap Calculator in Figure 6-11 only uses SystemVue blocks that can be ported to Hardware Description Language (HDL). Therefore the blocks used to implement the LMS Tap Calculator in SystemVue are slightly different than those used to implement the feed-forward equalizer in Chapter 6.2 and require a fixed point number input. The fixed point number input in SystemVue requires a word length parameter specifying the number of bits represented by the value, the integer length to determine the position of the decimal point, and whether the value is signed or unsigned. These specific design decisions for the SystemVue implementation of the LMS Tap Calculator are used in order to allow the design to be ported to HDL.

6.3.2 Exporting SystemVue Design to HDL

SystemVue provides a tool for exporting a dataflow model to hardware description language (HDL) if the dataflow model only contains certain parts/blocks. Also all of the SystemVue blocks must operate on the fixed point datatype in order for the design to be exported to HDL.

A "HDL Code Generator" module must be added in the Workspace Tree and selected with the appropriate design in order to create the HDL code from the SystemVue dataflow model as seen in Figure 6-12. Then the "generate" button must be pressed to generate the HDL code in the directory set in the window (Figure 6-12).
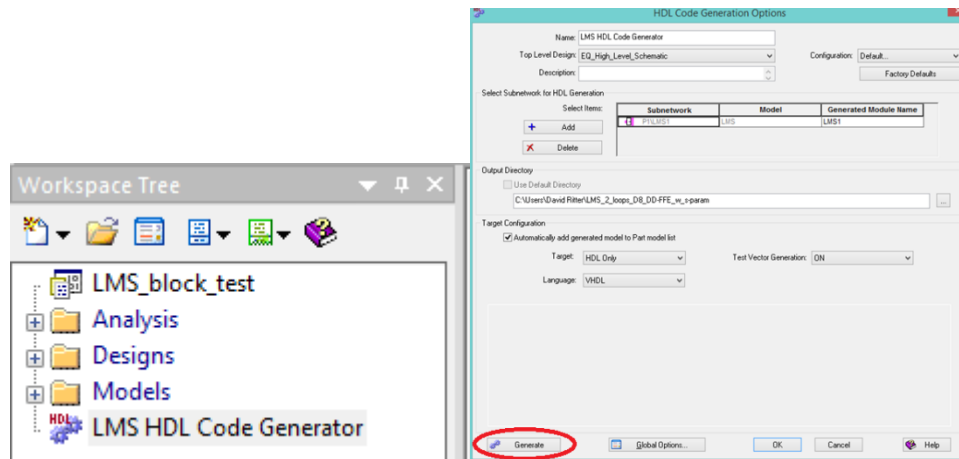
Figure 6-12: HDL Generation Module and Tab in SystemVue for exporting a SystemVue dataflow design to HDL

Test vectors can also be generated for HDL testing which will be used in the next Chapter 6.3.3. The HDL code corresponds to the SystemVue dataflow model and each block in SystemVue is represented by an HDL component. This thesis uses VHDL as the HDL language, but Verilog is also an option in SystemVue. In the next two sections the SystemVue dataflow model will be compared to the VHDL code produced from SystemVue for two different sets of inputs for x_input and d_input.

6.3.3 Testing of LMS Tap Calculator Dataflow Models in SystemVue

Two tests will be performed on both the SystemVue dataflow model and the VHDL model of the LMS algorithm for generating the channel tap valuess. The conditions for both tests are outlined in Table 6-1.

Table 6-1: LMS Filter Tap Calculator Testing Inputs

	x_input	d_input
Test 1	0.5	0.75
Test 2	-2	-0.000061

The SystemVue testing setup can be seen in Figure 6-13 which includes the LMS filter calculator's two inputs of the x_input (channel output), and the d_input (desired value input). The LMS filter calculator's output includes all the filter taps values, weight 1-4, the y_output, and the error. The two inputs require a generated signal is SystemVue and then converted to fixed point from an integer value. All the outputs are viewed by sinks.
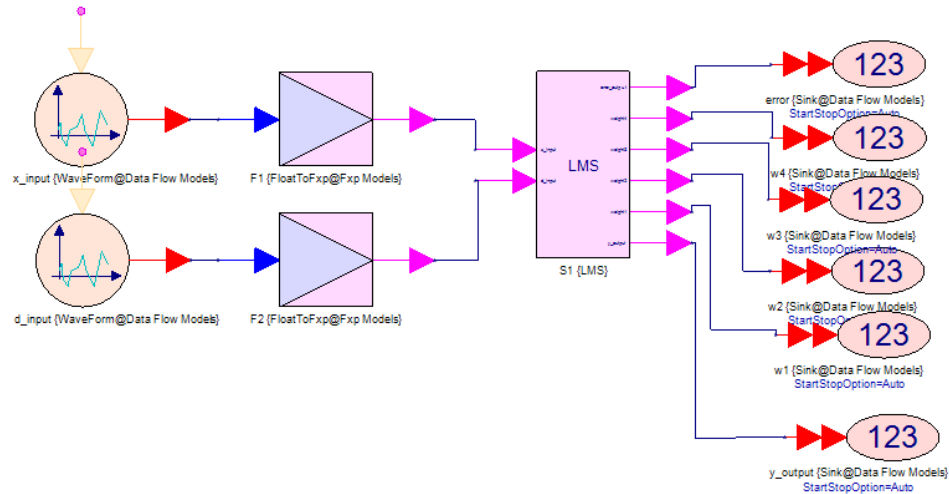
Figure 6-13: Testing in SystemVue of SystemVue dataflow model of LMS tap calculator

SystemVue LMS Tap Calc Test 1:

The first test sets x_input to 0.5 and d_input to 0.75. The final values of the y_output and error can be seen in Figure 6-14 which converge to 0.749 and 0.00122 respectively. The y_output should ideally equal the desired output (0.75) and the error should converge to 0. Both outputs are close to the expected/ideal values for test 1.
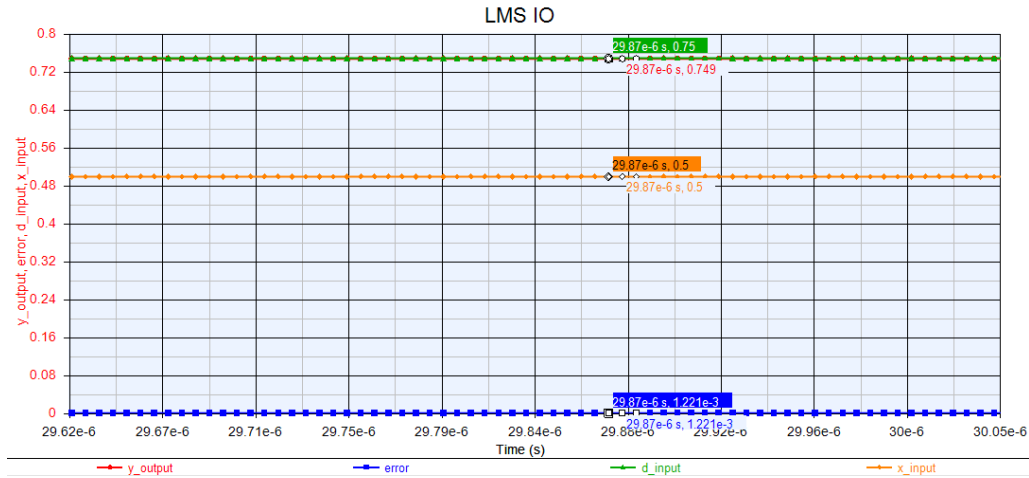
Figure 6-14: LMS Tap Calculator Test 1 y_output and error output final values for SystemVue implementation

The filter tap values are plotted in Figure 6-15 and are shown converging to the final values as calculated by the LMS filter calculator in SystemVue.

Figure 6-15: LMS Tap Calculator Test 1 filter taps values for SystemVue Implementation

The filter tap values converge to the following values: Tap 1 = .429, Tap 2 = .392, Tap 3 = .355, Tap 4 = .321 which when summed together equals 1.497. Since the y_output is a summation of the x_input multiplied by the taps, x_input * sum of taps = .5 * 1.497 = .7485 = y_output which is the correct value that should be set with the SystemVue model.

SystemVue LMS Tap Calc Test 2:

The second test sets x_input to -2 and d_input to -.000061. The final values of the y_output and error can be seen in Figure 6-14 which converge to -.0002441 and 0.0001831 respectively. The y_output should ideally equal the desired output and the error converge to 0. Both outputs are close to the expected/ideal values for test 2.

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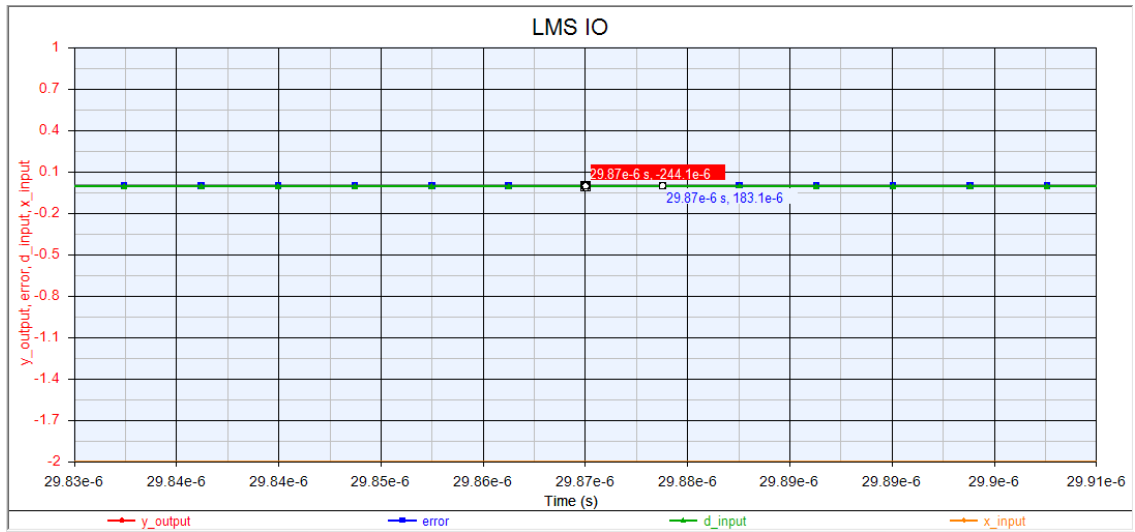
Figure 6-16: LMS Tap Calculator Test 2 y_output and error output final values for SystemVue implementation

The filter tap values are plotted in Figure 6-15 and are shown converging to the final values as calculated by the LMS filter calculator in SystemVue in Figure 6-16.

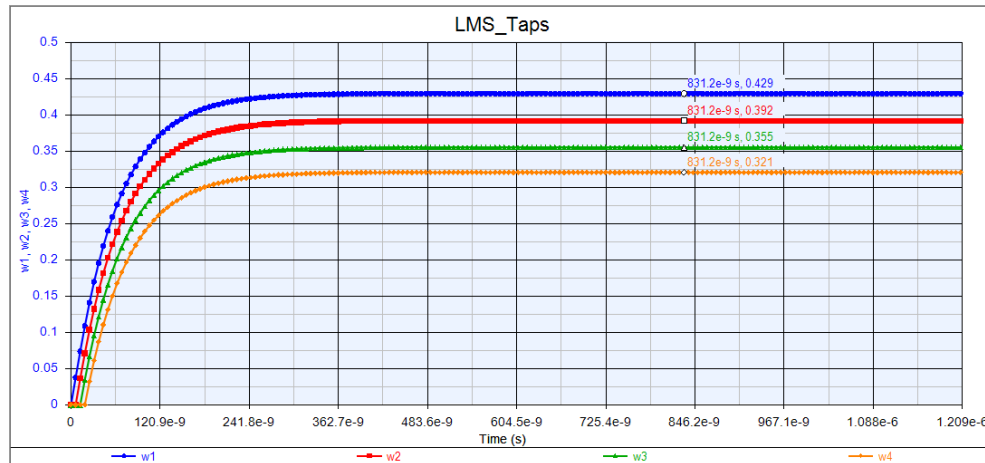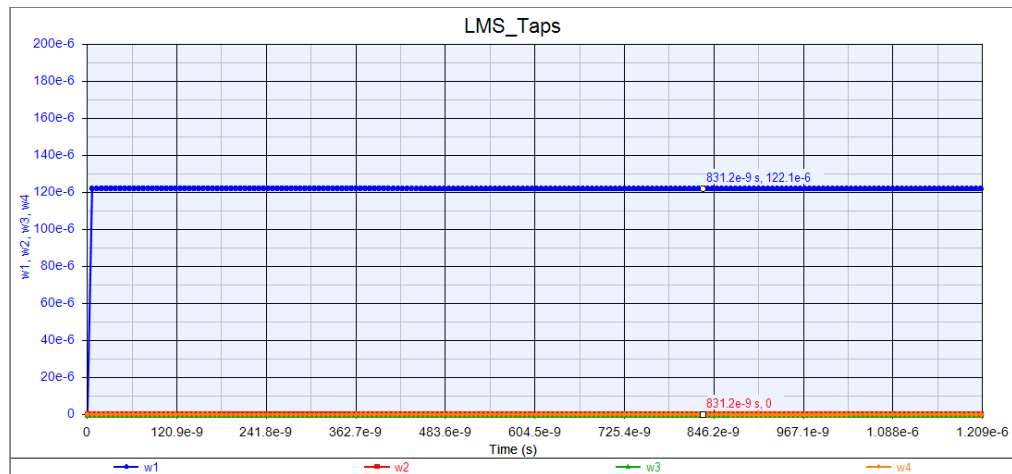**Figure 6-17: LMS Tap Calculator Test 2 filter taps values for SystemVue Implementation**

The filter tap values converge to the following values as seen in Figure 6-17: Tap 1 = .0001221, Tap 2 = 0, Tap 3 = 0, Tap 4 = 0 which when summed together equals .0001221. To check, x_input * sum of taps = -2 * .0001221 = -0002442 = y_output which is the correct value that should be set with the SystemVue model.

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6.3.4 Testing of LMS Tap Calculator VHDL Model in ModelSim

This section outlines the testing and results of the LMS Tap Calculator VHDL model in ModelSim, in order to verify that the VHDL model matches the behavior of the SystemVue model. The VHDL source are exported to on folder while the test bench files are exported to another. SystemVue also creates a .tcl "do" file to add the waveforms to ModelSim for testing. The x_input and d_input values must be changed in the "LMS_SimTB.vhd" file with the signal names UUT_x_input and UUT_d_input. Then make sure all files are included and compiled in ModelSim. The x_input and d_input values are changed and constant for each test. The VHDL module outputs are plotted in the ModelSim once simulation has been run.

ModelSim VHDL LMS Tap Calc Test 1:

All inputs and outputs of the LMS Tap Calculator VHDL ModelSim Test 1 can be seen in Figure 6-18 and are displayed in hexadecimal.

Figure 6-18: LMS Tap Calculator Test 1 all outputs for VHDL implementation

Only the final values of the outputs are considered for the test, in order to allow the LMS Tap Calculator to converge. The x_input and d_input are input values set to 0.5 and 0.75. The y_output, tap values, and error are the outputs of the VHDL module to be verified. The y_output should be equal to the summation of the taps multiplied by the x_input, since the x_input is fixed (non-time-varying). The y_output should also converge to the d_input.

The values are represented by a 16-bit fixed point number with 1 sign bit, 1 integer bit, and 14 fraction bits. The conversion from this fixed point representation to decimal follows:

x_input = x2000 = 0 0.10 0000 0000 0000 = .5

d_input = x3000 = 0 0.11 0000 0000 0000 = .75

y_output = x2803 = 0 0.10 1000 0000 0011 = .6251831055

error_output = x07FD = 0 0.00 0111 1111 1101 = .1248168945

Weight1 = x140A = 0 0.01 0100 0000 1010 = .3131103516

Weight2 = x1404 = 0 0.01 0100 0000 0100 = .3129882813

Weight3 =x13FF = 0 0.01 0011 1111 1111 = .3124389648

Weight4 = x13FA = 0 0.01 0011 1111 1010 = .3121337891

Check output values with other outputs:

error_output = .1248168945 ~ = 0.124817 = d_input − y_output

Sum of all weights = 1.250671387

x_input * sum of all weights= .6253356934 ~ .6251831055 = y_input

The LMS Tap Calculator VHDL ModelSim Test 1 values do not correspond with the SystemVue Test 1 results (within 1% error), but do check out with themselves, since the y_output converges to the d_input and the y_output equals a summation and multiplication of the x_input with the tap values (Weight1, Weight2, Weight3, and Weight4).

ModelSim VHDL LMS Tap Calc Test 2:

All inputs and outputs of the LMS Tap Calculator VHDL ModelSim Test 2 can be seen in Figure 6-19 and are displayed in hexadecimal.
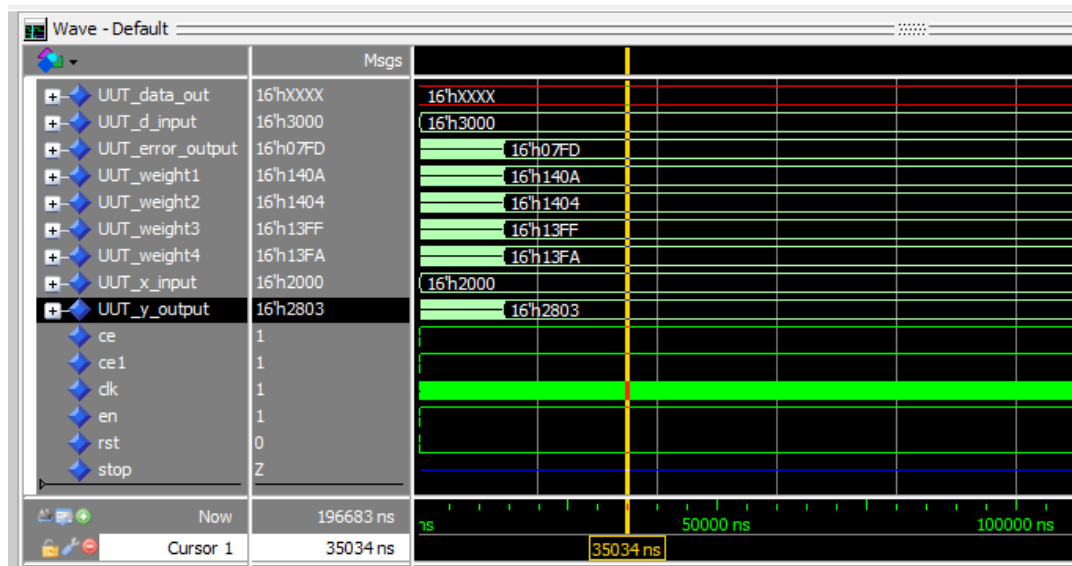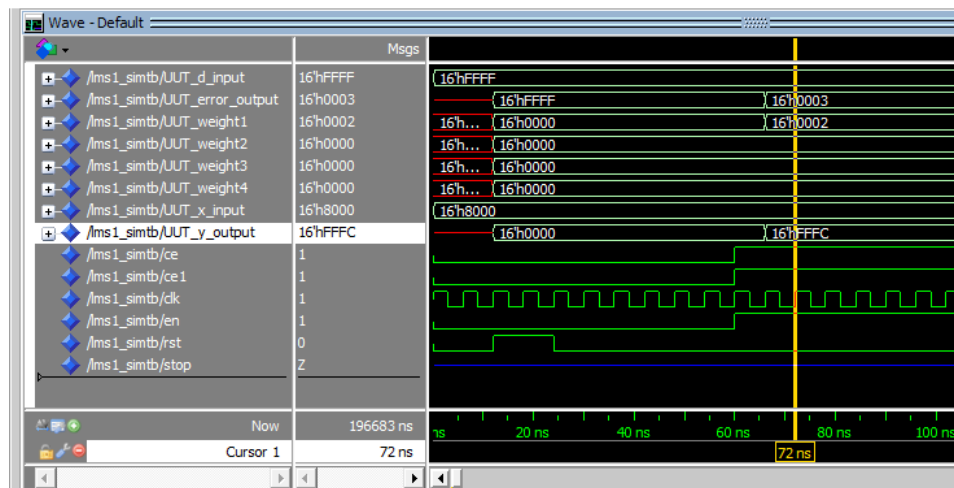

Figure 6-19: LMS Tap Calculator Test 2 all outputs for VHDL implementation

Only the final values of the outputs are considered for the test, in order to allow the LMS Tap Calculator to converge. The x_input and d_input are input values set to -2 and -.00061. The y_output, tap values, and error are the outputs of the VHDL module to be verified. The y_output should be equal to the summation of the taps multiplied by the x_input, since the x_input is fixed (non-time-varying). The y_output should also converge to the d_input.

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The values are represented by a 16-bit fixed point number with 1 sign bit, 1 integer bit, and 14 fraction bits. The conversion from this fixed point representation to decimal follows:

x_input = x8000 = 1 0.00000000000000 = -2

d_input = xFFFF = 1 1.11111111111111 = -.000061

y_output = xFFFC = 1 1.11111111111100 = -.000244140625

error_output = x0003 = 0 0.00000000000011 = .0001831

Weight1 = x0002 = 0 0.00000000000010 = .000122

Weight2 = x0000 = 0 0.00 0000 0000 0000 = 0

Weight3 = x0000 = 0 0.00 0000 0000 0000 = 0

Weight4 = x0000 = 0 0.00 0000 0000 0000 = 0

Check output values with other outputs:

error_output = .0001831 ~ 0.000183 = d_input − y_output

Sum of all weights = 0.000122

x_input * sum of all weights= -0.00024 ~ -.000244140625 = y_input

The LMS Tap Calculator VHDL ModelSim Test 2 values do correspond with the SystemVue Test 1 results (within 2% error), since the y_output converges to the d_input and the y_output equals a summation and multiplication of the x_input with the tap values (Weight1, Weight2, Weight3, and Weight4).

Conclusion and Summary of Two Tests:

The results of both test 1 and test 2 with the SystemVue and VHDL models of the LMS Tap Calculator show that the VHDL model does not match the SystemVue dataflow model, but both work independently correctly as seen in Table 6-2. However in test 2, the results of the VHDL and SystemVue dataflow model are within 2% error. The small error is likely the result of using extreme values for the x_input and d_input.

Table 6-2: LMS Filter Tap Calculator Testing Results for both SystemVue and VHDL models

		Inputs		Outputs						Sum of Taps	Check Y
	Model	X input	d input	y output	error	tap1	tap2	tap3	tap4		
Test 1	System Vue	0.5	0.75	0.749	0.00122	0.429	0.392	0.355	0.321	1.497	0.7485
Test 1*	VHDL	0.5	0.75	0.625183	0.12482	0.31311	0.313	0.312	0.312	1.250671	0.625336
Test 2	System Vue	-2	-6E-5	-2.4E-4	1.8E-4	1.22E-4	0	0	0	1.22E-4	-2.4E-4
Test 2*	VHDL	-2	-6E-5	-2.4E-4	1.8E-4	1.22E-4	0	0	0	1.22E-4	-2.4E-4

The LMS taps do not always converge to the same values for SystemVue and the HDL code, but their logical operations hold correctly. The signals are only represented within 2% error in HDL as SystemVue even when the WordLength and Integer Length are set. Some work needs to be done on the tools to ensure that the VHDL matches the SystemVue behavioral model (0% error), but the potential for streamlining HDL code is possible, and currently close to representative when generated automatically.

6.4 Other Block Comparison to Hardware

The SystemVue Equalization model in Chapter 6 also requires other blocks to complete its function other than just the feed-forward equalizer and the LMS Tap Calculator. The other components included in the design are data converters, ADCs and DACs, dataports, a wrapper block, and a comparator.

6.4.1 Standard Blocks and their Representations

The LMS Filter Tap Calculator discussed in Chapter 6.3 requires a fixed point (FXP) datatype which represents a digital signal so data converters are required. These data converters would be implemented by an ADC and a DAC since the floating point datatype represents an analog signal and the fixed point datatype represents a digital signal. The ADC corresponds to the floating to fixed point converter while the DAC corresponds to the fixed to floating point converter as seen in Figure 6-20.
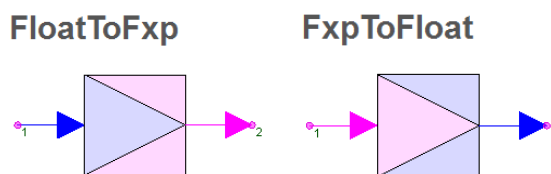
Figure 6-20: Float to Fixed point and Fixed Point to Float SystemVue blocks; model an ADC and DAC respectively

A dataport is used when a SystemVue model is used to simplify a complex design (Figure 6-21). A dataport can be either an input or an output to a SystemVue model.
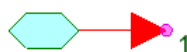
Figure 6-21: SystemVue DataPort block; for high level block input or output

6.4.2 Channel Tap Calculator

The Channel Tap Calculator model is a higher level model/wrapper for the LMS Tap Calculator as seen in Figure 6-22. The LMS Tap Calculator calculates the channel tap values for the Feed Forward Equalizer i.e. the "analog" portion of the design.
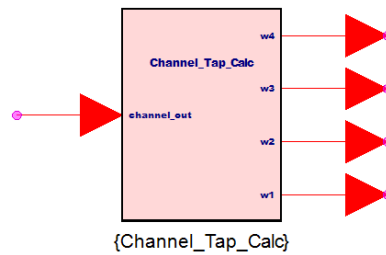
Figure 6-22: Channel Tap Calculator High Level Block Diagram; for combining ADC, DACs, LMS calc, and comparator

The Channel Tap Calculator model is implemented by a floating to fixed point converter at the input dataport and fixed to floating point converters at the outputs (Figure 6-23). This data conversion is required since the entire Channel Tap Calculator and LMS Tap Calculator is intended to be implemented in digital hardware. A comparator is also included for feeding back a decision directed d_input (desired input) from the y_output signal of the LMS Tap Comparator.
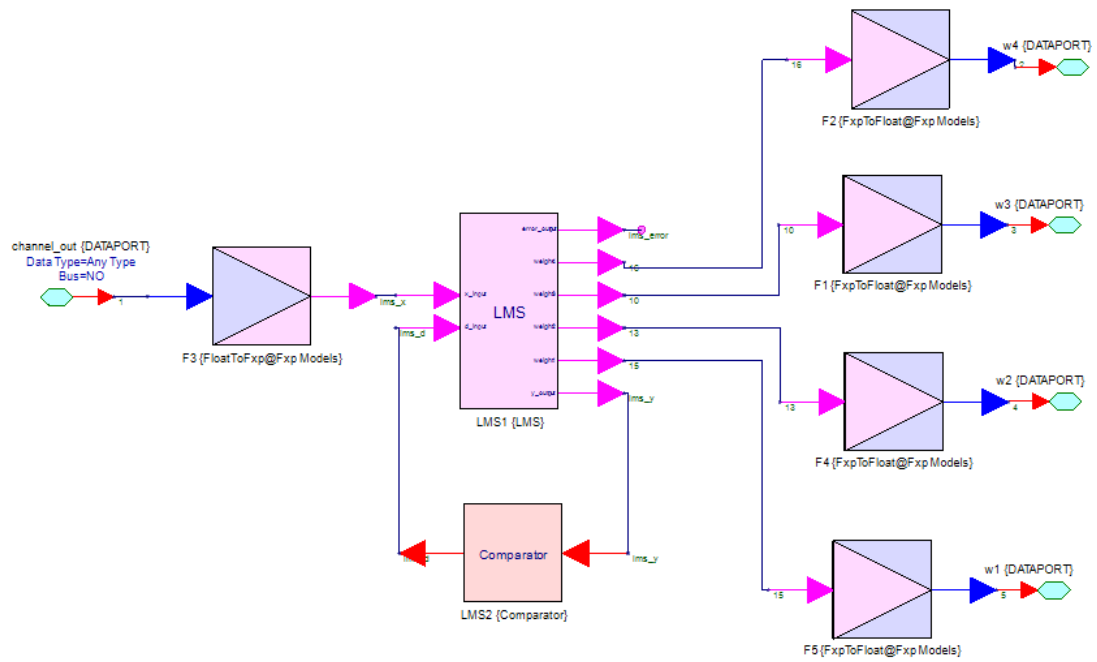
Figure 6-23: Channel Tap Calculator implementation in SystemVue; requires the LMS HDL block and Comparator

Overall the Channel Tap Calculator allows analog signals at the input and output of LMS Tap Calculator to interface with the rest of the equalizer.

6.4.3 Comparator

A comparator is implemented in the Channel Tap Calculator intended to be entirely in the digital domain, but could be implemented either in analog or digital hardware (Figure 6-24) [31].
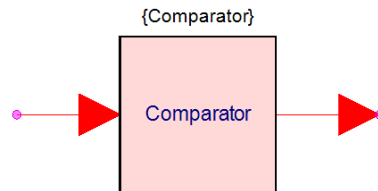
Figure 6-24: SystemVue Comparator High Level Block Diagram

However in order to implement the comparator in SystemVue, data converters are used to convert the LMS Tap Calculator y_output to a floating point, then set to a 1 or 0, and then converted back to fixed point (Figure 6-25).
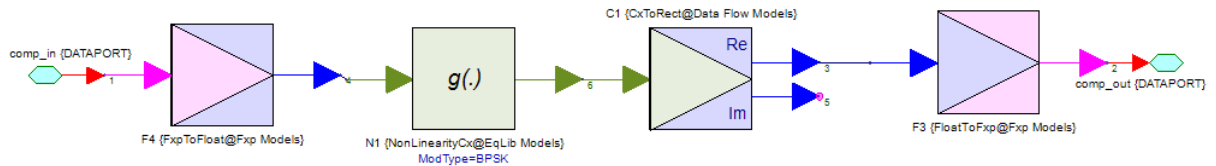
Figure 6-25: SystemVue Comparator Implementation (to be integrated with HDL SystemVue LMS block)

The comparator is used to determine if the incoming value is closer to a 0 or a 1, by comparing to the center level. In the case of BPSK, the center value is 0 and the 1 value corresponds to 1 and the 0 value corresponds to -1. The "g(.)" block takes the input and sets it to the closest value for the BSPK modulation scheme. The comparator is used in this design to implement the "decision directed" portion of the equalizer for generating the filter tap values to be used to equalize the input signal to the equalizer.

6.5 Integrating Analog and Digital Portions

The entire Transistor-Based SystemVue design for the equalization scheme of Chapter 6 is implemented and tested with a modified Equalization Verification setup that is entirely in simulation, using a simulated channel.

6.5.1 SystemVue Simulation for Integrated Design

The Equalization Verification SystemVue simulation as used in this thesis is used to evaluate the equalization scheme of Chapter 6 as seen in Figure 6-26.
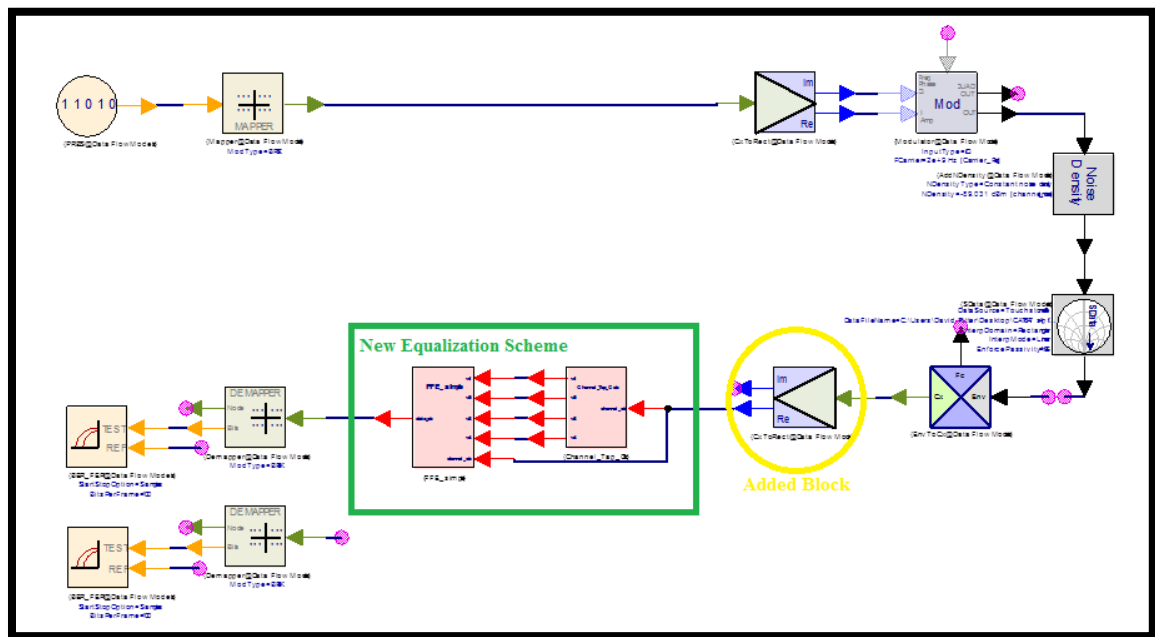
Figure 6-26: Equalization Verification SystemVue Design with slight adjustments for More Realistic Model of Equalization

The green square in Figure 6-26 signifies the portion of the SystemVue simulation under test, and is the equalization scheme of Chapter 6 including both the analog and digital portions. The yellow circle in Figure 6-26 is the addition of the complex to rectangular data converter since the equalization scheme only operates on real data components. The setup of Figure 6-26 will be used to evaluate the equalization scheme of Chapter 6 in Chapter 6.5.

6.5.2 Simulation of Entire Transistor-Based SystemVue Model

The setup of Figure 6-26 is used to produce the graphs of Chapter 6.5.2 according to the same procedures as Chapters 4 and 5. The simulated channel used for testing the transistor-based equalization scheme is the CAT7 15ft with the parameters outlined in Table 6-3.

Table 6-3: Simulation Parameters for transistor-based Equalization Scheme

TX Setup				Simulation Setup					LMS Param		BER Settings	
Input Data	P R B S	Ca-rr-ier	B W	Sim Ti-me	Sa-mple Rate	Num Sam-ples	Time Spa-cing	Freq Res	Num Taps	Step Size	BER start (delay)	BER delay bound
80 Mbps	7	2 GHz	160 MHz	80us	32768	12801	6.25E-3 us	12.499 kHz	4	0.0001	10000	10

The noise power of the noise density block is swept to produce the BER vs. Eb/N0 graph of Figure 6-27. The BER improves for all noise levels when the transistor-based equalization scheme is added to the link with the CAT7 15ft simulated channel, 2GHz carrier, and 80MBPS data.
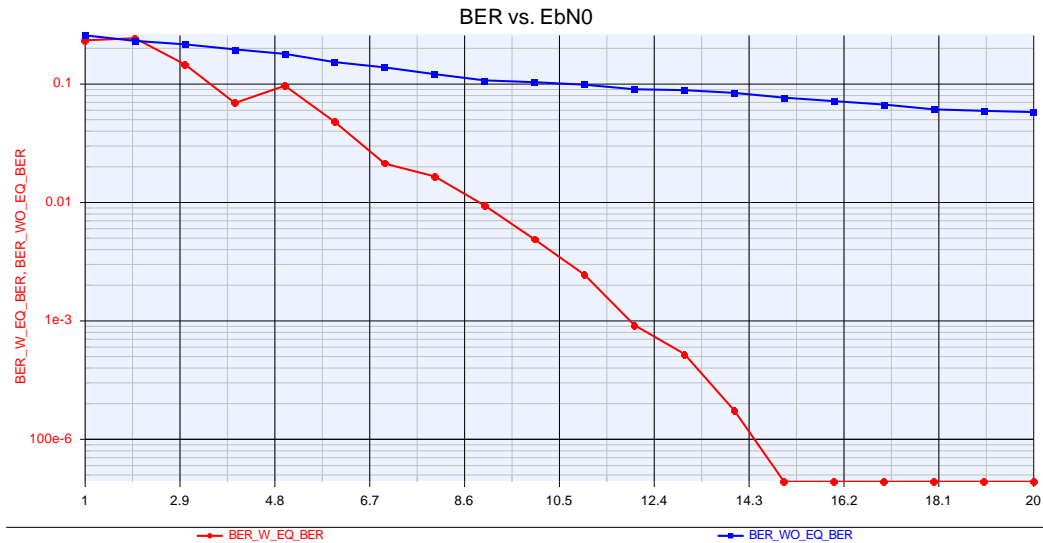
Figure 6-27: BER vs. Eb/N0 for Transistor-Based Equalization Scheme, for CAT7 15ft, 2GHz

carrier, 80MBPS data

When the noise power is set to 0, the BER improves with the addition of the transistor-based equalization scheme as seen in Table 6-4.

Table 6-4: BER Results for transistor-based Equalization Scheme

Cable Type	Length	Carrier	Sample Rate	Input Delay	VGA Gain	Eb/N0 for Real Channel	BER w EQ	BER wo EQ
CAT7	15ft	2GHz	160MHz	1411	-30	no noise	0.00E+00	3.2E-02

The following graphs are from the simulation with the same parameters as specified in Table 6-3 and Table 6-4 when using the transistor-based equalization scheme. The baseband signals can be seen in Figure 6-28 with the channel output baseband signal (blue) aligned with the channel input signal (red) and the equalized signal (green). The equalized (green) signal in Figure 6-28 has yet to converge to the final equalilzation coefficients.
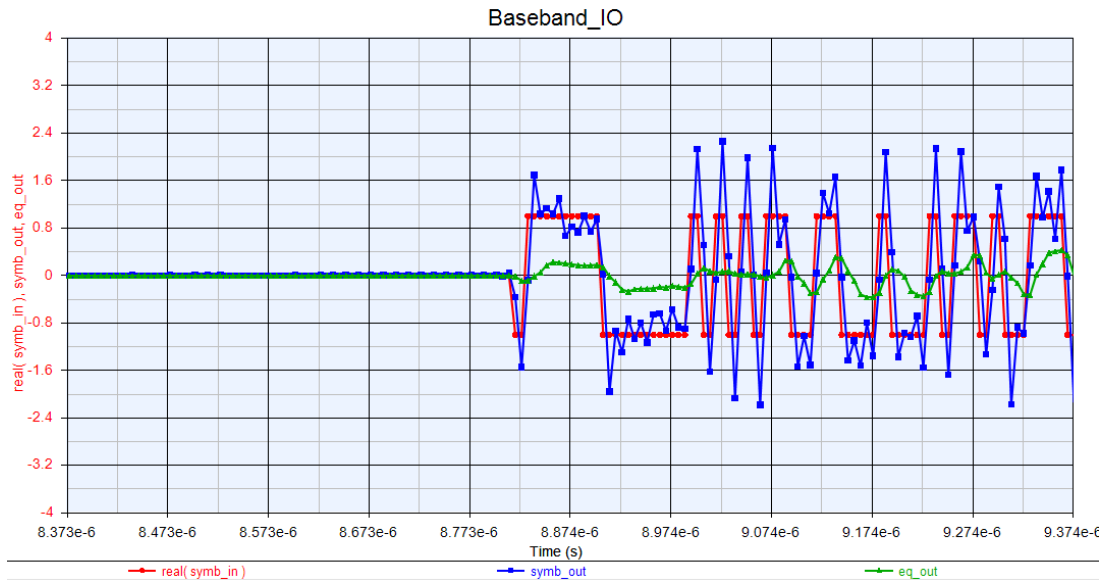
Figure 6-28: Integrated Equalization Design baseband input and output of channel, and equalization output, for CAT7 15ft simulated channel

The baseband signals are then zoomed out in Figure 6-29 to show that the equalized signal (green) converges to its final tap values after approximately 20us.
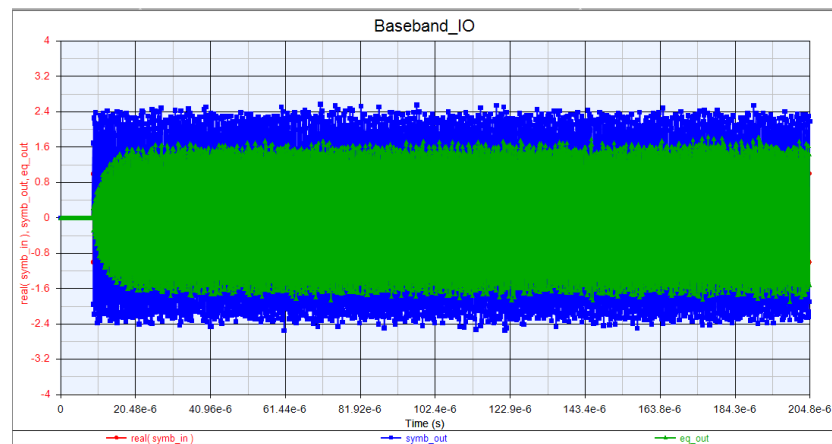
Figure 6-29: Baseband IO zoomed out for Integrated Equalization Design, note the LMS taps settling out at 20us

The equalized channel output is compared to the channel input data in Figure 6-30 to show how the transistor-based equalizer tracks the channel input data. The equalizer tap values are set to be close to the inverse of the channel in order for the output data to more closely follow the input data. In Figure 6-28 the equalization tap values have not

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convereged to their final value while in Figure 6-30 the equalization tap values have converged to their final value.
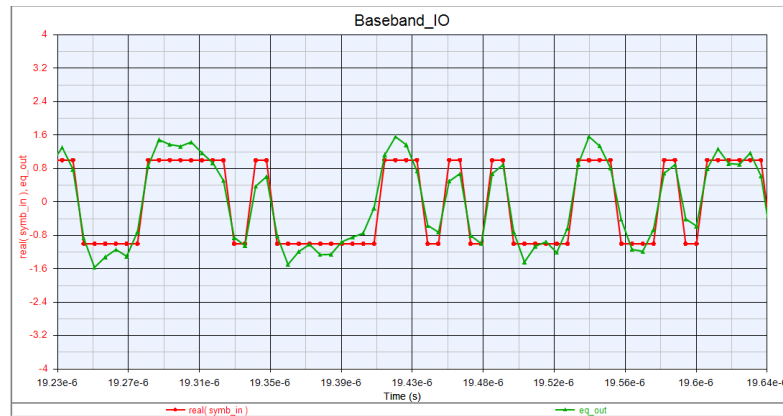
Figure 6-30: Baseband IO zoomed in for Integrated Equalization Design, the Equalization output follows the channel input

The channel input and output spectrums can be seen in Figure 6-31 which is across the simulated CAT7 15ft cable. The attenuation of the simulated channel corresponds to the attenuation of the real CAT7 15ft cable based on the S21 s-parameter measurements of the cable. The variation in attenuation distorts the signal and requires equalization.
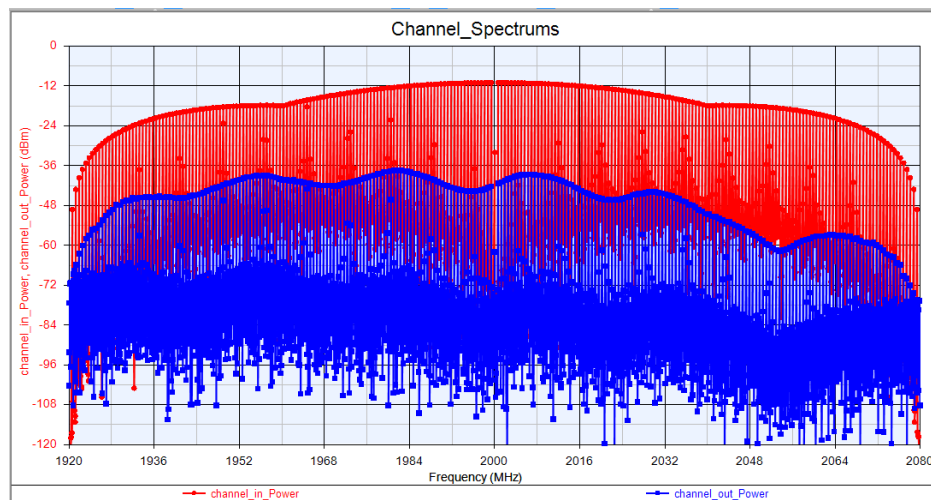
Figure 6-31: Channel Input and Output Spectrums for Integrated Equalization Design

The LMS error can be seen converging to a lower value Figure 6-32. This lower value is non-zero but settles out after approximately 20us, which is when the equalizer's tap values have settled.
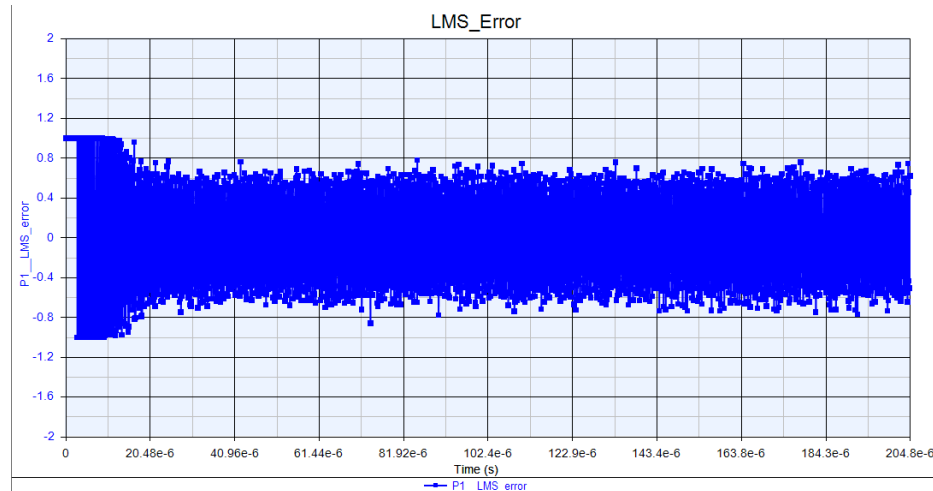
Figure 6-32: Integrated Equalization Design LMS error; converges at approx. 20us

The equalizer weights, or channel coefficients, are plotted in Figure 6-33 to show their final value when operating with a CAT7 15ft cable, at 2GHz carrier, and 80MBPS data rate. The equalizer tap values can be seen converging to their final value at approximately 20us in Figure 6-33 which corresponds to the LMS error in Figure 6-32.
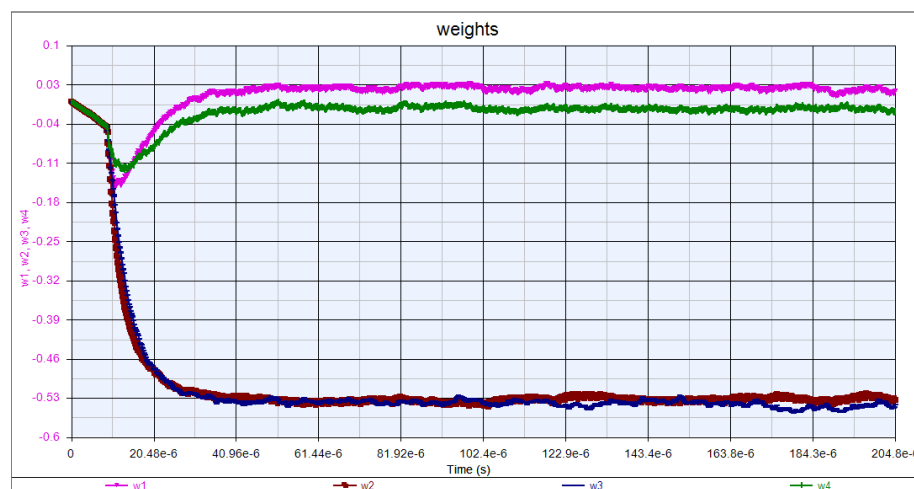
Figure 6-33: Integrated Equalization Design LMS Filter tap values (weights); for CAT7 15ft simulated channel

6.5.3 Conclusion of Chapter 6.5

The transistor-based Equalization Scheme improves (decreases) the BER for different channel noise power levels across a CAT7 15ft simulated cable. The results of Chapter 6 testing, with the SystemVue created feed-forward decision direction LMS equalizer, show an improvement in BER from $3.2*10^{-2}$ to 0 when adding equalization and no channel noise power. The transistor-based equalization scheme is more easily portable to integrated circuit design tools but still follows the same trends, a decrease in BER by over an order of magnitude, as the Chapter 4 and 5 equalization scheme. Chapter 6's goal was to show that the Equalization Verification testing procedure and setup could be used for an transistor-based equalization scheme. This goal has been successful for this a feed-forward decision directed LMS equalizer since the BER decreased (from $3.2*10^{-2}$ to 0) with the addition of the equalization scheme for a simulated channel.

7. Summary of Results and Conclusion

This final chapter of this thesis covers the main issue with this thesis's setup, future work, and overall analysis of results.

7.1 Main Limitation of Equalization Verification Setup

The main limitation in the Equalization Verification setup is the VSG and VSA interfacing with SystemVue. The VSG's sample rate is set by SystemVue, and for the same SystemVue simulation, the VSA sample rate is set to 1.28 times the VSG sample rate, potentially due to windowing [32]. Therefore the compatibility of Keysight's M9381A, M9391A, and SystemVue causes problems when trying to match all the three components sample rates, causing the VSA's PLL not to lock to the VSG's timing. The VSA's PLL phase noise is shown in Figure 7-1, when the correct loop bandwidth is set, however is not the case in this setup. The M9391A VSA datasheet also allows room for this large phase noise by specifying potential timing noise of greater than 400ps skew + 50ps jitter + 80ps repeatability, which is greater noise than this system can tolerate [5]. Other problems related to SystemVue, the VSA, the VSG and their integration can be found in Appendix D.
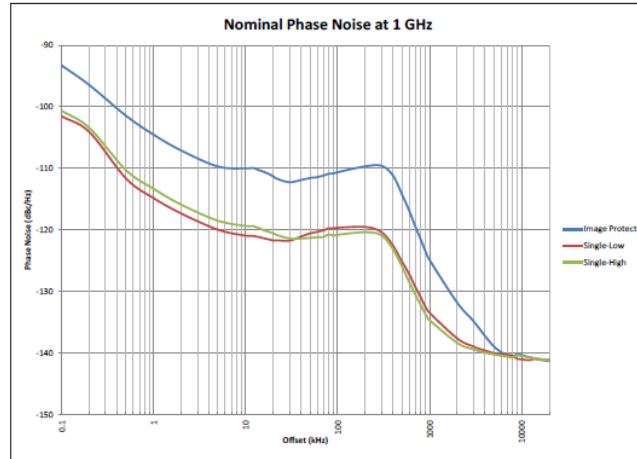
Figure 7-1: M9391A VSA PLL Phase Noise plot for correct Loop BW [5]

However, when the VSA does not have the same sample rate as the VSG, the VSA's PLL does not lock and causes excessive phase noise that must be modeled as white noise. This large amount of noise causes the BER results of the physical channels to not match the BER results of the simulated channels (in some cases). The main improvement on this thesis would be integrating the SystemVue Equalization Verification simulation with another VSA/VSG pair that would generate the same sample rate for the same simulation.

7.2 Future Work

The future work of this thesis should include integrating a VSA, VSG, and Equalization Verification SystemVue simulation to test a physical channel without excessive phase noise. A new combination of VSA and VSG other than the M9391A and M9381A should be tested to allow the VSA's PLL to lock to the VSG's output waveform. The Keysight equipment may not have been designed to support running a simulation through SystemVue on both the transmitting and receiving sides of a link, so other options should be explored. The goal of testing with different VSA/VSGs should be to match the simulated channel's results to the physical channel results. Also, to better integrate the

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system a "one-button" press simulation instead of having to run the simulation once to output to the VSG, and once to input from the VSA.

The main intent of this thesis is to test equalization schemes over specific physical channels. Therefore the intended future work with this Equalization Verification setup should be to model equalization schemes in SystemVue and then test them over existing physical channels, with the intended link parameters (data rate, frequencies, etc.). Also using SystemVue to output to different VSA/VSG combinations would allow for frequencies above 6GHz and equal to or less than 160MHz bandwidth. The Equalization Verification setup is intended to test equalization schemes over a variety of potential channels, either wireless or wired. Varying different equalization parameters, such as step size or number of taps, could be changed based on their performance over specific channels. The Equalization Verification setup is created to help the IC designer create an equalization scheme for a specific channel or set of channels.

7.3 Overall Conclusion

The Equalization Verification setup has been used to verify a decision-directed feed-forward LMS equalizer over a variety of channels, both simulated and physical, and both wired and wireless. The SystemVue behavioral equalization scheme (Figure 4-21), in Chapters 4 and 5, decreased the BER (improved the link), by an order of magnitude or greater, under the following channel conditions, all both simulated and physical:

CAT7 3ft, 15ft for 1GHz & 2GHz carrier, 80MHz data rate

CAT7 25ft for 1GHz carrier, 80MHz data rate

CAT6A 15ft, 25ft, 1GHz & 2GHz carrier, 80MHz data rate

CAT7 15ft, 2GHs carrier, 50MHz data rate

2.4GHz Dipole Antenna, 2.4GHz carrier, 80MHz & 50MHz data rate

The SystemVue behavioral equalization scheme (Figure 4-21), in Chapters 4 and 5, decreased the BER (improved the link), by less than an order of magnitude, under the following channel conditions, all both simulated and physical:

CAT7 25ft, 2GHs carrier, 80MHz data rate

CAT6A 3ft, 1GHz & 2GHz carrier, 80MHz data rate

CAT7 15ft, 1GHz carrier, 50MHz data rate
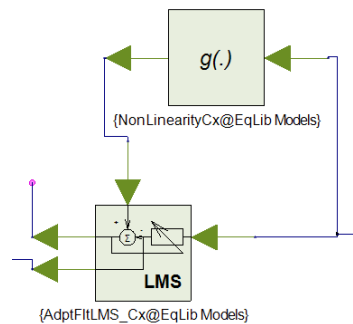
Figure 7-2: Decision Directed Feed Forward LMS Equalizer as implemented by SystemVue dataflow modeling blocks

The equalization scheme parameters were also changed including LMS step size and number of taps to show that the BER was still improved, by an order of magnitude or greater in most cases, with the equalization scheme added to the link. The simulated channel BER results did not match the same order of magnitude of the physical channel BER results, but in both cases the addition of the equalization scheme did decrease the BER by an order of magnitude or greater when adding the equalization scheme. Therefore the addition of the equalization scheme was shown to improve the overall

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quality of the link, by reducing the number of bit errors, under the chosen testing conditions.

Then in Chapter 6 a transistor-based SystemVue equalization model was created using HDL SystemVue components and blocks easily implemented by transistors (Figure 7-3). The design is still decision-directed feed-forward LMS equalizer, but implemented to be more easily ported to transistor design.
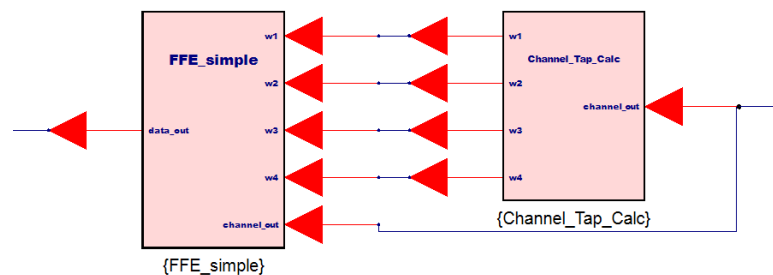
Figure 7-3: High Level Block Diagram of Transistor-Based Equalization Scheme Implemented in SystemVue; Analog (FFE simple) and Digital (Channel_Tap_Calc) portions

Only a simulated channel was tested (CAT7 15ft, 2GHz carrier) with the transistor-based equalization scheme, but the BER decreased with the addition of this equalization scheme. The analog and digital portions of the transistor-based equalization scheme were also verified with either HDL or Spice simulation.

Overall this thesis accomplished its goal of creating a testing setup, Equalization Verification, to show that adding a given equalization scheme can improve the quality of the link, decrease BER, over a specific physical channel. Even though there was the issue of the simulated channel results not matching the same order or magnitude BER of the physical channel results, the equalization scheme under test was shown to decrease the BER by an order of magnitude or greater in both cases. Further work would need to be

done to correctly integrate the VSA/VSG and SystemVue since the Keysight tools are not designed to be integrated all at once (conclusion from this thesis's work). However, as this thesis has shown, it is possible to evaluate a modeled equalization scheme over a physical channel, without the fabricated chipset. This potential to verify an equalization scheme before fabrication could potentially identify bugs in simulated silicon and save IC design companies millions of dollars in chip fabrication costs.

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APPENDICES

APPENDIX A: SystemVue Simulation Block Level Functionality

This appendix presents a step-by-step breakdown of the SystemVue simulation blocks to be used in the Equalization Verification SystemVue simulation of Figure 7-4, and their purpose for the data link.
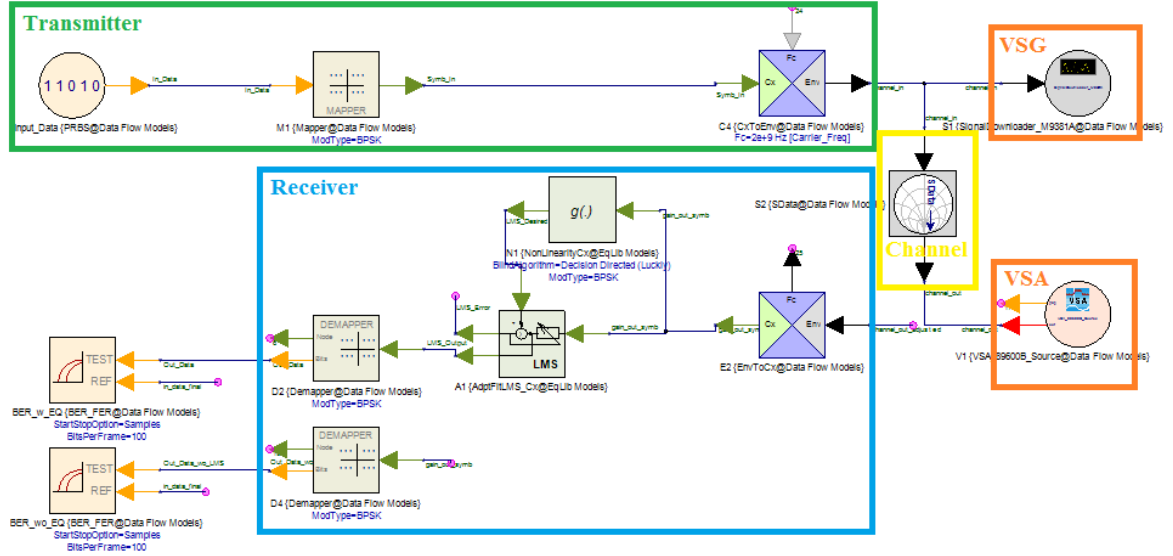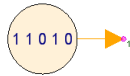

Figure 7-4: SystemVue Simulation: with S-parameter channel and VSA/VSG

(S-parameter channel and VSA/VSG not to be used at the same time)

Data Blocks:

Figure 7-5: PRBS and BER SystemVue blocks

The PRBS generator produces a pseudo random sequence of data. The output variable is of a bit type, and the data rate is specified in the block. The Bit Error Rate block compares the TEST bit input to the REF bit input, and the potential offset in samples can be set inside the block. The PRBS is used in the transmitter (green box in Figure 7-4) to produce the data bit stream. The BER block is used after the receiver (blue box in Figure 7-4) to determine the number of bit errors that have occurred as a result of channel ISI and noise.

High Level Equalizer Blocks:
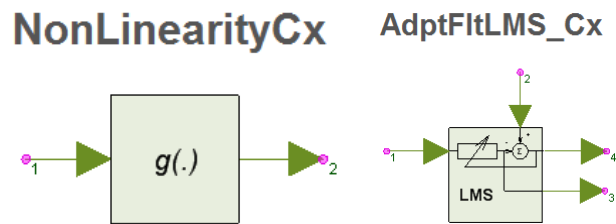
Figure 7-6: Nonlinearity and Adaptive Filter LMS SystemVue blocks

The NonLinearityCx block acts as a comparator and sets the input to either a 1 or -1 depending on which value the input is closest. The AdptFltLMS_Cx block takes the data input, a desired (reference) input, and outputs the error signal, and output data. The filter coefficients are calculated internally and the number of filter tap values are determined inside the block. The step size and initial conditions are also set inside the block. The non-linearity and LMS block comprise the high level equalization scheme to be tested in Chapters 4 and 5. Both of these blocks are in the receiver (blue box in Figure 7-4).

Modulator and Demodulator:
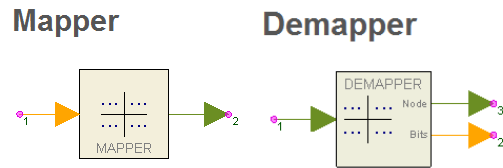
Figure 7-7: Mapper and Demapper SystemVue blocks

The mapper takes an input bit(s) and produces an output complex "symbol." The complex symbol corresponds to the IQ signal, so for NRZ/BPSK the signal is either 1 -> 1 or 0 - > -1.

The demapper performs the opposite of the mapper and takes an input symbol and outputs bit(s). For NRZ/BPSK, the demapper takes in a 1 -> 1 or a 0 -> -1. In this case the demapper acts like a comparator. The mapper is in the transmitter (green box in Figure 7-4) and the demapper is in the reciever (blue box in Figure 7-4).

Ideal Gain and Delay:
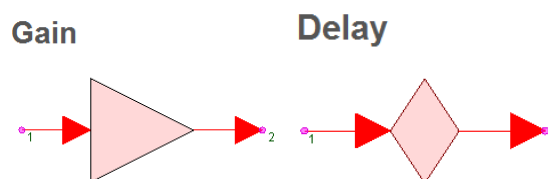
Figure 7-8: Ideal Gain and Delay SystemVue blocks

The gain block performs an ideal gain on any input data. In this simulation, the gain block represents a variable gain amplifier to adjust the input of the receiver's data for the channel's flat attenuation of the data's entire band. The delay block delays the input data an integer multiple as specified in the block's parameters. The gain and delay blocks are used throughout the Equalization Verification SystemVue simulation including the VGA in the receiver, and aligning the BER measurements (both input and output data).

Upmix and Downmix:
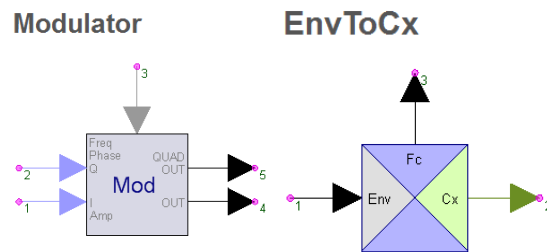
Figure 7-9: Upmix and Downmix SystemVue blocks

The Modulator acts as an upmixer because the center frequency is added to the complex signal in the baseband. The IQ inputs (real and imaginary) are mapped to a frequency over the given simulation sampling time. The IQ signal, over time, creates a baseband frequency that is then upmixed to a higher frequency. The frequency components around the center frequency corresponds to the baseband representation. The envelope data type can then be recorded and downloaded to the VSG.

The EnvToCx is then used to downmix the received signal in a higher band down to the complex signal in the baseband. The VSA outputs a envelope signal, so the signal must be downconverted to a complex signal for equalization in the baseband. The Modulator is in the transmitter (green box in Figure 7-4) and the EnvToCX is in the reciever (blue box in Figure 7-4).

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S-Parameter Block:

Figure 7-10: S-parameter data SystemVue block

The SData block takes a touchstone .snp file consisting of a series of s-parameter measurements and uses them in the dataflow simulation. The S21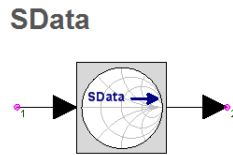 measurement is the only s-parameter measurement used in the dataflow simulation since dataflow simulation is single directional. The SData block is used to in a simulation without the VSA or VSG when testing the equalization scheme with a simulated channel (see Chapter 3.4). The results when running the simulation across the SData simulated channel are compared to the results using the VSA, VSG, and real channel in order to verify the testing setup. The SData block is in the "channel" portions of the Equalization Verification SystemVue simulation (yellow box in Figure 7-4).

Noise Density Block:
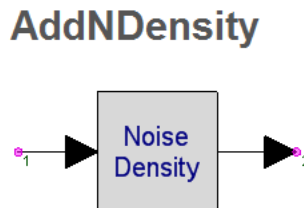
Figure 7-11: Noise Density SystemVue block

The AddNDensity or "Noise Density" block adds a Gaussian white noise at the set noise power level to an envelope signal. This noise density block is used to simulate the channel in the "channel" portions of the Equalization Verification SystemVue simulation (yellow box in Figure 7-4).

Spectrum Analyzer and Data Sink:
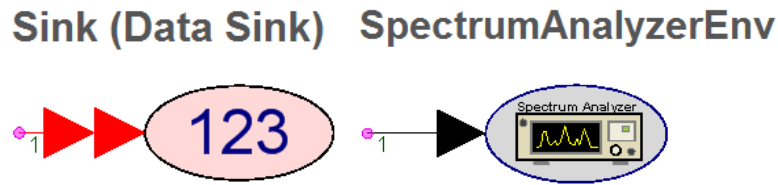
Figure 7-12: Data Sink and Spectrum Analyzer SystemVue blocks

The Data Sink and Spectrum Analyzer blocks record the data at their input nodes for the entire simulation. The Data Sink block records the data in the time domain while the Spectrum Analyzer block records the data in the frequency domain. The Spectrum Analyzer block can only record data from an envelope datatype. The recorded data includes the time of the data, and the value of the data, that can be graphed in SystemVue or exported to another software for processing. Many different Sinks and Spectrum Analyzers are used in the Equalization Verification SystemVue simulation in order to display time domain or frequency domain waveforms.

APPENDIX B: VSA Setup Notes

This appendix is for M9391A VSA setup conditions and notes. The VSA 89600 software simulation parameters must match the SystemVue simulation parameters in Table 7-1.

Table 7-1: SystemVue Simulation Parameters to VSA Parameters

SystemVue Param	Carrier Freq	Sample Rate	Num Samples	Stop Time	Freq Res
SystemVue Param Type	User Defined	Sim Defined	Sim Defined	Sim Defined	Sim Defined
VSA Param	Center	Span	Freq Points	Main Time Length	ResBW

Other steps for setting up the VSA89600 software include: set window to "Uniform (Rectangular)" [32]; ResBW Mode to Arbitrary BW in VSA software autosets to correct value; eg 125MHz span in VSA for 160MHz; sample rate in SV. The SystemVue VSA 89600 Source block should be set to "pause" in order to correctly view the input waveform in the 89600 software before recording (Figure 7-13).

Figure 7-13: VSA 89600 Software SystemVue block; set Pause to YES
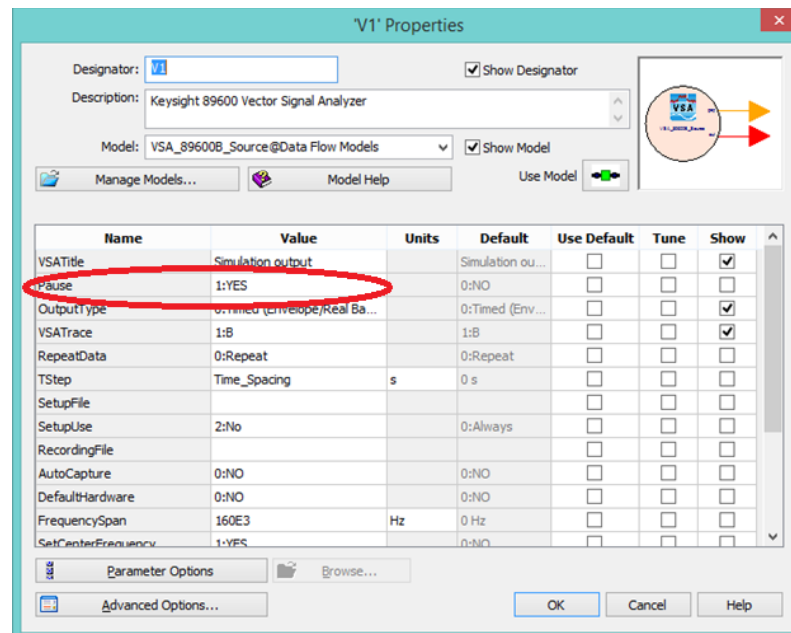
Also verify that the VSA 89600 range is set to 0dBm in order for all measurements to be uniform. The power range can be changed to a higher or lower value based on the equipment, but do not change throughout measurements. Do not use the "auto-range" button in the VSA89600 software or else the power levels, and the Eb/N0 will not be uniform for all measurements.

APPENDIX C: VSG Setup Notes

This appendix is for M9381A VSG setup conditions and notes. To correctly match the output power of the VSG to the input power of the VSA, add a "user correction" amplifier of 17 V/V gain in the VSA 89600 software by selecting Input – User Correction. The value of 17 V/V is equipment dependent and should be adjusted by the user to match the power levels. The User Correction amplifier is after the test point but before the analyzer hardware, used in this thesis to match the power levels of the VSG to VSA. Note that the VGA gain is added in SystemVue, and is not the same as the VSA 89600 user compensation amplifier. The User Correction Amplifier in the VSA must be set to 17V/V gain in order to match the output power of the VSG to the input power of the VSA (Figure 7-14), but may be different depending on the equipment used.
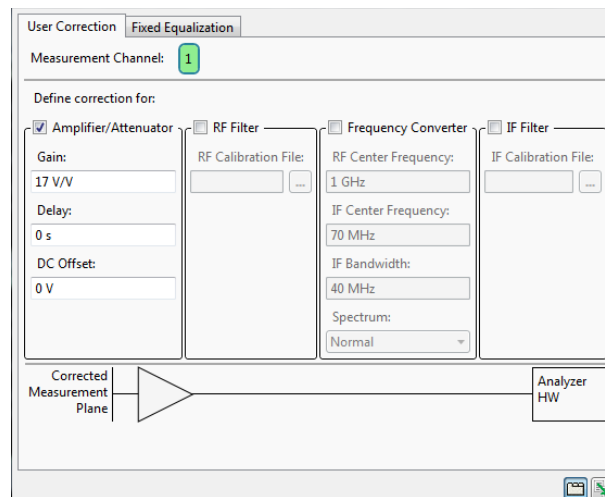
Figure 7-14: VSA89600 Software window to add a 17V/V gain before the VSA input

The power settings in the M9381A downloader need to be set as follows to match the SystemVue waveform levels: Advanced settings -> Amplitude 20 dBm (Figure 7-15).
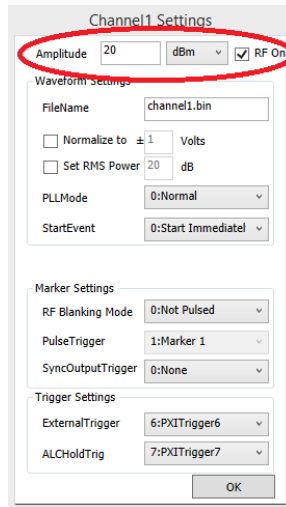
Figure 7-15: M9381A Signal Downloader Advanced Settings; amplitude to 20dBm

Verify that the VSG trigger is attached to the VSA trigger in order to properly align the waveforms in the VSA 89600 software (external trigger)

Figure 7-16: VSG output trigger to VSA input trigger to ensure alignment of waveforms

APPENDIX D: List of Solutions to Equalization Verification Setup Issues

This appendix presents a reference to known issues with the Equalization Verification system. This appendix is divided into sub-sections based on each issue's corresponding component.

SystemVue using VSA 89600 Software (with the M9391A VSA hardware):

The best way to debug using the VSA 89600 software with SystemVue is to set the "Pause" option to "1:YES" and then figure out the problem with the data in the VSA 89600 software.

Problem 1: Sometimes the input waveform is inverted in the baseband (polarity reversed), only over the carrier frequency range of 1.1GHz to 2.GHz

Solution 1: In VSA 89600 software, display the time domain on a trace from time 0, in order to see enough bits to determine if polarity is reversed. If the polarity is incorrect, use "Preset" button in input – extensions, to reset the input data until polarity is correct. Then capture the data as normal.

Problem 2: The bandwidth setting (frequency range) of the VSA software does not match the imported SystemVue frequency range, by a factor of 1.28 (e.g. 160MHz in SV is 125MHz VSA 89600 range).

Solution 2: Let the VSA 89600 software auto-set the bandwidth according to the connected node in SystemVue (auto-set by sampling rate). Then the timing will more accurately match the time domain measurements from the VSG. Allowing the VSA

89600 to auto-set the bandwidth is more accurate in the time domain than down sampling in SystemVue (after importing data from VSA 89600) to get the correct bandwidth.

Problem 3: A non-filtered pulse (BPSK) has infinite bandwidth and the recovered baseband signal is not ideal.

(Partial) Solution 3: Allow for twice (2x) the lowest bandwidth for BPSK signals, i.e. twice the datarate sample rate; SystemVue sample rate determines the RF bandwidth. Since the filtering of the data for the control case (BPSK modulation) is rectangular, a roll off factor (excess bandwidth) of at least 1 will more allow the demodulated signal in the time domain to more accurately match the input data.

Problem 4: There is significant jitter on the baseband (time domain) data, and is not time aligned to VSG output from SystemVue TX.

Identified Cause of problem 4: VSG plays a "recording" continuously of the output from SystemVue. The VSA knows the start of the recording based on the trigger connected from the VSG to VSA. The trigger, when observed on an oscilloscope, has a 4ns jitter peak to peak. Therefore the entire timing of the VSA input data could be off by +/- 2ns. The VSA samples the data based on its own clock, and thus is not adjusted to the trigger's jitter. Therefore the sampled data by the VSA may be sampled on the transition of the data, causing significant bit errors. Some solutions to this problem are presented below, but are the main crux of this thesis, at least for higher data rates close to the VSA/VSG bandwidth limit of 160MHz.

Problem 5: The VSA power levels continue to change when changing the cable after using "auto-range" button in VSA 89600 software.

Solution 5: Keep range constant over all measurements at 0dBm. The VSA 89600 auto-adjusts the level to be traditional modulation levels which are not realistic for TX/RX chipsets. The VGA gain in SV should be adjusted by the user to set the desired input power levels to the RX.

Problem 6: In VSA 89600 software, the trigger has a non-zero delay every time the SystemVue simulation is run.

Solution 6: Set the SystemVue VSA 89600 block "frequency span" to 0 Hz, or else the VSA 89600 Software sets the trigger delay to a non-zero value.

SystemVue using the M9391A VSG:

Problem 7: The VSG output power does not match VSA input power, and the VSG output power does not match its set amplitude power in SystemVue.

Solution 7: The VSG power setting was iteratively solved (as outlined in Chapter 3.2) to set the VSG SystemVue block to Amplitude 20 dBm; then in the VSA 89600 user correction amplifier to 17 V/V. The signal levels imported from the VSA (input power) should match the VSG output signal levels (output power) in SystemVue.

SystemVue Simulation Issues:

Problem 8: BER block "delay bound" only moves forward and often locks to incorrect value, resulting in a higher BER than expected.

Solution 8: Perfectly align the transmitted and received data when taking BER measurements. This is often a problem when in combination with the VSG trigger issue of problem 6.

Problem 9: When using the s-parameter block, the simulated delay is non-zero and based on the length/delay of the channel, while when running the simulation with a real channel the delay is zero. The BER rates do not match.

Solution 9: Since the VSA reads the waveform based on the VSG trigger, the start of the waveform is at time equals zero. Therefore to make an accurate comparison, the simulated (s-parameter) channel must have a non-zero input delay to match the input and output data for BER measurements, while the real channel measurements have a zero input delay. For accurate BER measurements, align the inputs iteratively graphically (for each frequency range and cable), and then set the BER block's delay-bound (in equations tab) to a non-zero value such as 10. More information, and example measurements, can be found in Chapters 4 and 5.

APPENDIX E: BER vs. Eb/N0 Power Sweep

To generate a BER vs. Eb/N0 graph in SystemVue, the following steps must be taken, all according to Equation 7-1:

    1) Calculate the input amplitude level (Mod_Gain) from input power (Mod_Power_dbm)

    2) Set the channel_noise for the current EbN0 term

    3) Set EbN0 as a tunable parameter (Figure 7-17)

    4) Run a Sweep on EbN0 (e.g. 1 to 20) (Figure 7-18), with a schematic that calculates BER for each simulation run; make sure "EbN0;" is in equations tab and not set to a value

    5) Graph BER vs. EbN0 (Figure 7-19)

Equation 7-1: SystemVue Power/Noise Equations for calculating Eb/N0

EbN0;

Mod_Power_dbm = 10;   %for 1V BSPK

Mod_Power_W = 10^((Mod_Power_dbm-30)/10);

Mod_Gain = sqrt(2*50*Mod_Power_W);   %amplitude is 1 for 10dBm input power

Eb_dbm = Mod_Power_dbm - 10*log10(Bit_Rate);   %for BPSK

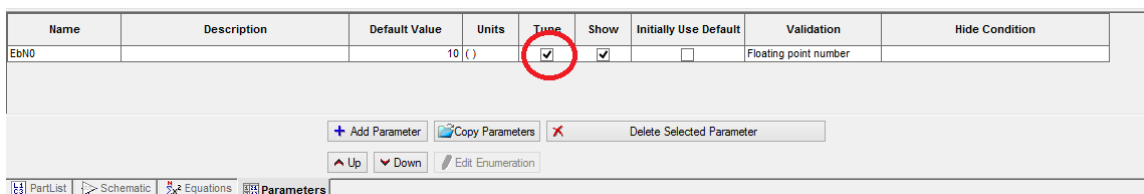channel_noise = Eb_dbm - EbN0;   %in dBm

Name	Description	Default Value	Units	Tune	Show	Initially Use Default	Validation	Hide Condition
EbN0		10	( )	✔	✔	☐	Floating point number	

+ Add Parameter   🗐 Copy Parameters   ✗   Delete Selected Parameter

∧ Up   ∨ Down   ✎ Edit Enumeration

PartList   Schematic   Equations   **Parameters**

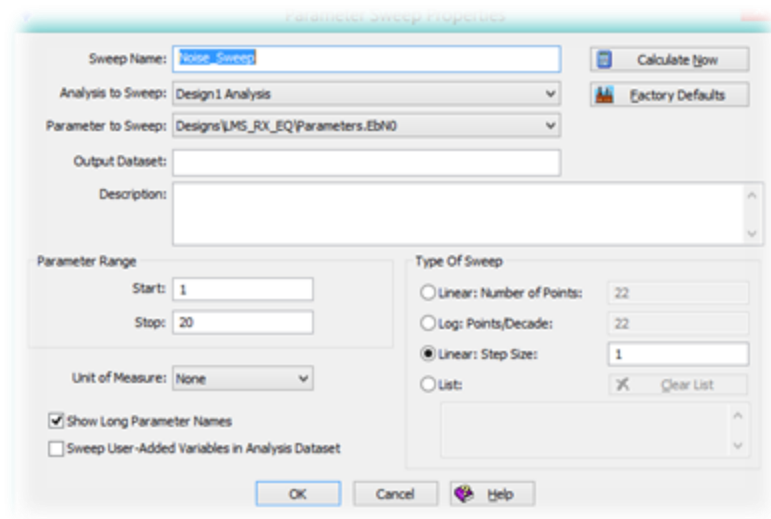**Figure 7-17: Parameters tab to set EbN0 as a tunable parameter**
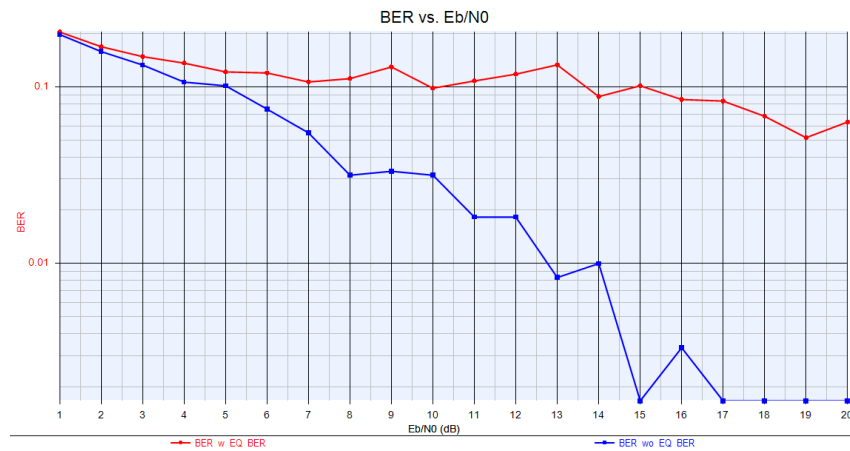
Figure 7-18: EbN0 sweep SystemVue window

Figure 7-19: Example BER vs. Eb/N0 graph for a EbN0 sweep