INQUIRY OF GRAPHENE ELECTRONIC FABRICATION

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Masters of Science in Electric Engineering

by
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ABSTRACT
Inquiry of Graphene Electronic Fabrication
John Rausch Greene

Graphene electronics represent a developing field where many material properties and devices characteristics are still unknown. Researching several possible fabrication processes creates a fabrication process using resources found at Cal Poly a local industry sponsor. The project attempts to produce a graphene network in the shape of a fractal Sierpinski carpet. The fractal geometry proves that PDMS microfluidic channels produce the fine feature dimensions desired during graphene oxide deposit. Thermal reduction then reduces the graphene oxide into a purified state of graphene. Issues arise during thermal reduction because of excessive oxygen content in the furnace. The excess oxygen results in devices burning and additional oxidation of the gate contacts that prevents good electrical contact to the gates. Zero bias testing shows that the graphene oxide resistance decreases after thermal reduction, proving that thermal reduction of the devices occurs. Testing confirms a fabrication process producing graphene electronics; however, revision of processing steps, especially thermal reduction, should greatly improve the yield and functionality of the devices.

ACKNOWLEDGMENTS

Thank you to the CP Connect committee for selecting the project for funding. Thank you Strasbaugh for supplying facility and consumables support. Thank you Matt Lin for spending hours in the fab with me creating these devices. Finally, thank you to the amazing faculty at Cal Poly who continually push me to be better; this project would not have succeeded without you guys.

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1. PROJECT DESCRIPTION

This project emphasizes Cal Poly's motto of learn by doing to develop a novel process to create graphene electronics. The project idea stems from a Nanotechnology article published in 2011 by Fairbanks et al. [1]. The article summarizes work simulating the effect side gates exhibits on a fractal Sierpinski carpet electronic network. The simulation shows the resistance of the network behaving non-linearly [1]. The interplay of local gating and the complex geometry of Sierpinski carpet dictate electron transport through the network, resulting in the non-linear behavior of the device [1]. The fractal scaling creates a complex network consisting of various sizes of conducting channels. The physics behind the reference paper initially motivates the research to construct fractal electronic devices but this project does not encompass analysis of the affects of fractal geometry on electronics. The fractals solely provide the proof of concept for complex patterning of graphene electronics. The project focuses on developing a process to produce graphene electronics at Cal Poly using readily available resources. The remainder of this report defends the following thesis statement.

THESIS STATEMENT

This thesis project designs and develops a process to prototype fractal graphene electronics using resources from multiple Cal Poly departments and colleges augmented by industry support.

The report begins by explaining the motivation for using graphene as the active material layer in the devices. Graphene exhibits phenomenal material characteristics that allow fabrication of a wide variety of devices [2, 3, 4, 5, 6]. The project aims to produce the device at Cal Poly; this requires networking throughout campus to obtain the necessary resources. Chapter 1 describes the

exploration of fabrication procedures that eventual lead to developing a fabrication process. The fabrication process requires several labs spread across campus and industry.

The report continues with Chapter 2 describing material selection for each layer of the device. The high temperature requirement of graphene oxide reduction creates a design constraint that greatly limits material selection. Chapter 3 describes the fabrication procedure in great detail, going through each fabrication step that Chapter 1 outlines. Chapter 3 concludes with the producing the first prototype and leads into Chapter 4, which characterizes the devices. Theoretical calculations in Chapter 4 provide expectations for the devices and experimental testing confirms operational devices. The report concludes by descripting future work in Chapter 5. This project represents a first step to eventually produce commercial grade graphene electronics.

1.1 GRAPHENE

Graphene was first produced in 2004 when scientists exfoliated graphene from graphite using tape [7]. Since then, research looking for ways to manipulate the material for application production results in several potentially viable and scalable fabrication techniques [2, 3, 4, 5, 6, 8, 9, 10, 11, 12]. Industry fears that Moores' law will fail within the coming years since current fabrication processes already push silicon near its material limitations [13]. Graphene provides an exciting new material capable of applications including transparent conductors, energy storage, and electrical transmission [3, 5, 6].

Graphene creates two-dimensional confinement of electron and hole transport. Graphene's aromatic structure forms because of SP^2 hybridization bonds [14, 15]. SP hybridization occurs when the S and P orbitals overlap to produce bonds, known as sigma bonds. This bonding mechanism reduces the energy necessary for bonding. In SP^2 hybridization, three sigma bonds form that bind each carbon atom to its neighboring carbon atom in the same plane [16]. Carbon has four valance electrons available for bonding; the fourth electron forms a Pi bond with its neighboring atoms where the P orbitals of the two atoms overlap [16]. The Pi bond protrudes perpendicular to the sigma bond, creating the two dimensional confinement for carriers [16]. The Pi bonding structure allows Van Der Waals attraction to bond graphene sheets to substrates [8]. Figure 1 displays the bonding structure of graphene.

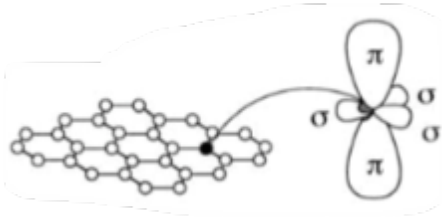

Figure 1. Graphene's bonding structure, emphasizing the three sigma bonds and the Pi bond protruding perpendicular from the atomic plane. The hexagonal pattern symbolizes the sigma bonds [16].

A secondary objective of this project is to determine applications for graphene structures to solve current societal engineering problems. One such problem is the depletion of Indium. ITO (Indium Tin Oxide) currently produces most transparent conductors used in photovoltaic cells and displays [18]. The depleting indium supply prevents producing the compound ITO; no obvious replacement for ITO currently exists [18]. The high transparency of graphene, reaching 97%, and abundance of carbon provides a solution to replace ITO [17]. Graphene provides a variety of solution ranging far beyond transparent conductors.

Dr. Kaner at UCLA uses graphene oxide to produce super capacitors to help solve energy storage needs [19]. The anisotropic heat conduction of graphene provides an entirely different application that could solve heat sink needs in space. Jeff Kendal at SLL, formally known as Space Systems Loral, explains that heat dissipation in space relies entirely on radiation and makes dissipating heat difficult [20]. Large heat sinks using ammonium transfers heat from components to radiating elements to cool the vehicle [20]. Graphene provides the potential to replace these large ammonium heat pipes.

Cooling optics in laser systems poses an entire different heat dissipation problem. As the founders of Cymer, Robert Akins and Richard Sandstrom explain, current optics use heat sinks that surround the perimeter of the optics and cannot directly cool the region the laser heats. Since graphene contains high transparencies and anisotropic heat conductions, it provides a potential solution to cool the optic directly at the point of heat introduction.

A wide variety of biosensors with high sensitivity becomes possibly using graphene transistors [4, 5]. The monolayer structure of graphene allows small impurities added to the system to cause current modulation through the device [4, 5]. A current biosensor project at Cal Poly stemming from this thesis includes detecting pulmonary surfactant in a Langmuir trough in the hopes to improve current synthesis of artificial pulmonary surfactant. Dr. Fernsler explains that roughly 150,000 people die annually because of defects in their pulmonary surfactant in their lungs, which prevents proper breathing mechanisms. Creating a sensor to improve the comprehension of pulmonary surfactant promises the capability to save hundreds of thousands of lives.

Graphene's exciting electrical characteristics arise because it is a zero band gap material and it is ideally one monolayer thick of carbon atoms [14, 16, 21]. The zero band gap causes the valance and conduction band to touch at one point called the Dirac point [16, 22]. The Dirac point aligns with the carbon atom location within the lattice [16, 22]. The two-dimensional structure of graphene causes two-dimensional confinement of electrons, which allows them to travel further distance than without scattering [16, 22]. The project focuses on reducing graphene oxide that consists of functionalized graphene into a pure form of graphene.

Graphene oxide contains additional functional groups that bond to the carbon lattice [5, 7, 14, 19, 23, 24]. The functional groups cause a band gap to form in the band structure, changing its

electrical and thermal properties [23, 25]. Functionalized graphene can act as a semiconductor or insulator depending on the number and type of functional groups bonding to the carbon lattice, producing poor electrical conduction [14, 25]. Producing devices with bottom gates can aid in determining the effects of thermal exposure to graphene oxide. Bottom gates should produce a greater response in graphene oxide device than in reduced graphene oxide devices. The wide variety of graphene forms allows several different potential applications.

Graphene provides a means to improve several technologies described above. This thesis project focuses on developing a repeatable, scalable, and adaptable process to produce any graphene electronic or device desired.

1.2 FABRICATION PROCESS EXPLORATION

Analyzing multiple fabrication procedures increases the probably of producing functioning devices. Mitigating post graphene deposition processing minimizes the risk of damaging the graphene film. Utilizing bottom gates, unlike side gates used in the reference 1, accomplishes this. A bottom gate device structure eliminates all post graphene deposition processing except metallic contact application. Semiconductor equipment in the micro-fabrication lab allows silicon doping and oxidation growth to create the bottom gates and the gate oxide layer that serves as the dielectric between the bottom gates and the graphene. Fabrication using both N and P type wafers tests distinctions between preferable wafer types, if any. Figure 2 displays the side profile of the final device to emphasize material layers, where GO represents the graphene oxide and Ag represents silver epoxy contacts.

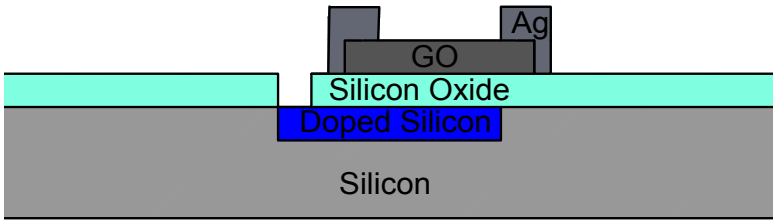

Figure 2. Cross sectional diagram of the fractal electronic prototype. Note colors distinguish various material layers.

Two categories of graphene device fabrication exist: graphene vapor deposition and GO (graphene oxide) reduction. Both fabrication processes exhibit benefits and constraints. Graphene vapor deposition easily achieves monolayer graphene sheets but requires extensive equipment capital such as chemical vapor deposition systems [24]. Patterning the monolayer graphene sheets requires equipment such as RIEs (Reactive Ion Etchers) utilizing hydrogen or oxygen plasma

[26]. The processing requires equipment that prevents batch processing (depending on the device size) and diminishes the viability for scalability. The necessary processing would prove exceedingly difficult to accomplish with available equipment.

1.2.1 PRISTINE GRAPHENE

ACS Materials produces Trivial Transfer Graphene™ that eliminates the need to perform CVD processing on campus [8]. No CVD equipment exists on campus; thus, performing CVD processing does not align with the objective to use resources found at Cal Poly. Monolayer and few layer graphene sheets CVD deposited onto water-soluble polymer allow users to deposit graphene sheets onto their own substrate. Submerging the graphene housing in water lifts off the graphene sheet, which then floats on the surface. Trivial Transfer Graphene™ solves the issue of film creation but leaves the issue of deposition and patterning using the RIE to obtain the fractal geometry. An alignment jig positions the graphene sheet above the bottom gates; Figure 3 displays the alignment jig. Outsourcing the design to Eric Veber, Cal Poly ME alumni, produces a better design and means to 3D print the alignment jig. Outsourcing the jig also saves time through implementing parallel processing.

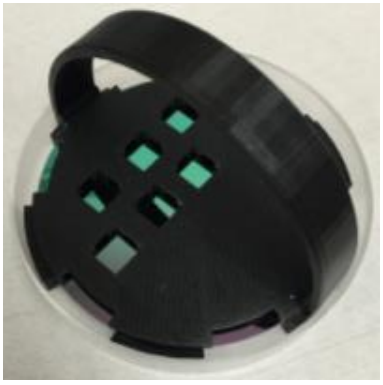

Figure 3. Alignment jig used to position graphene sheets above bottom gates. The jig contains an inner diameter of 100 mm to house the wafer.

Van der Waal forces bond the graphene sheet to the new substrate. The insurmountable issue arose during patterning the graphene sheet. The RIE requires a mask material to prevent regions from etching. Typically, the masking material consists of a metal layer bonded and patterned using chemical etching before RIE. Bonding a metal layer to the graphene sheet eliminates the possibility to isolate the graphene material layer as the sole conducting medium. RIE necessitates a bonded mask layer because the etching process utilizes plasma that seeps under masks not bonded to the substrate, causing under etching. The difficulties anticipated during patterning the pristine graphene causes the focus of fabrication to shift from using pristine graphene to using graphene oxide.

1.2.2 GRAPHENE OXIDE

The water solubility of GO (Graphene Oxide) allows patterning and deposition simultaneously. Numerous deposition methods for graphene oxide exist; however, available resources at Cal Poly yields three viable 3D printing techniques to deposit GO including ink jet printing, screen-printing, and microfluidic channel patterning. The variety of deposition methods and minimal cost of GO makes it an extremely attractive fabrication means that could easily scale to larger production. For comparison, $100 buys 250 mL of GO solution or one 1 cm x 1 cm monolayer Trivial Transfer Graphene™ sheet [4, 8]. The trouble with GO arises during the reduction process. GO typically consists of 50% oxygen and 50% carbon with trace amounts (<2%) of sulfur, hydrogen and nitrogen [4]. The oxygen functional groups prevent GO from exhibiting comparable electrical and thermal properties to metals. Removing the oxygen functional groups transforms GO to rGO (reduced GO); the process removes the oxygen functional groups and greatly improves electrical and thermal constructive of the thin film [25]. Two main reduction processes exist: chemical reduction and thermal reduction. The next section discusses reduction processing.

1.2.3 REDUCTION PROCESSES

Deciding on a reduction mechanism dictates future processing steps and constitutes one of the first design choices. Chemical reduction receives global recognition as one promising, cost efficient and scalable methods for GO reduction [27]. Unfortunately, most processes utilize harmful and toxic chemicals such as hydrazine [7]. Some research groups focus on green chemical methods and use caffeic acid, a non-toxic chemical, to reduce the GO [27]. The traditional use of toxic chemicals during chemical reductions discourages further research into this reduction process. Thermal reduction provides a safer reduction process but requires extreme temperatures. A reduction to 95% purity required 1000 °C thermal treatment [25]. Few materials remain in their solid state at this temperature, limiting possible substrates. At least three techniques manifest thermal reduction: laser heating, photonic sintering, and traditional furnace heating [3, 6, 26, 28].

Dr. Kaner at UCLA produces high performing super capacitors by reducing the GO samples using laser heating [19] A LightScribe unit (DVD label etcher) successfully reduces and simultaneously patterns the GO [19]. UCLA's process proves scalability and repeatability in producing graphene capacitors [19]. Laser reduction provides the first reduction process explored because of its low cost and proven repeatability. Problems integrating laser heating with the selected substrate and available resources prevents further developing this viable reduction method. Focus shifts to a similar reduction mechanism: photonic sintering.

Photonic sintering and laser heating both utilize electromagnetic energy to generate the necessary reduction temperatures. A NovaCentrix PulseForge® 1200 device on loan to Cal Poly permits photonic sintering on campus and establishes the second reduction method explored on campus. NovaCentrix provides data about their GO reduction experiments and confirms photonic

sintering as a viable reduction method. The PulseForge® product line contains several power capabilities options depending on the unit; the 1200 unit produces the least power, and proportionally, least light intensity and heat. The UV light capabilities of the 1200 limits the maximum temperature obtainable to around 600 °C, far below the necessary reduction temperature. Photonic sintering utilizes flash heating, potentially causing bubbling effects in the graphene sheet. NovaCentrix documents this problem in their experiments and provides Figure 4 [11]. The temperature limits of the 1200 unit causes dismissal of this reduction method. Traditional furnace heating provides the third exploration of thermal reduction methods.

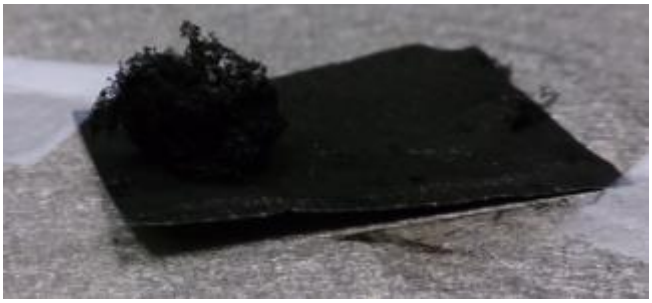

Figure 4: Failed GO reduction experiment performed by NovaCentrix that results in the GO bubbling off the substrate [11].

Traditional furnace heating provides the most viable reduction method with available resources. Extensive networking commences before acquiring a reduction furnace. First, an inquiry to use the oxidation and diffusion furnace in the Cal Poly Microfabrication Laboratory results in a denial of the request. Dr. Savage, director of the Cal Poly Microfabrication Laboratory, expressed concerns about chemical contamination in both the oxidation and diffusion furnaces. This prevents the use of the oxidation and diffusion furnaces. Next, the physics department provides a possible reduction furnace. Problems arose finding proper electrical infrastructure to power the furnace. The designs for the Baker building did not include electrical

infrastructure supplying 30 A, 125 V power capabilities. Installing such infrastructure costs several thousand dollars and does not provide an economical means for reduction experiments. Finally, networking with the Vice Present of Engineering at Strasbaugh, Bill Kalenian, results in acquiring a furnace already installed in a clean room. Strasbaugh generously permits access to their furnace and facilities for reduction processes. Thermal reduction requires a 1000 °C environment and an inert atmosphere to prohibit unwanted chemical reactions. Introducing nitrogen gas into the furnace prevents undesired chemical reactions during the reduction process. After selecting a reduction method, the deposition process represents the next design challenge.

1.2.4 GRAPHENE OXIDE DEPOSITION

Exploring several deposition methods results with one viable method. Screen-printing represents the first of the deposition methods. Screen-printing deposits material by forcing GO solution through a stencil mask [29]. The stencil mask permits GO solution in specific regions. Screen-printing wastes most the solution during deposition and small features prove elusive due to capillary action. The hydrophobic nature of water causes it to bead up and prevents the solution from transitioning through the stencil. The wasteful nature and self-limiting feature dimensions (50 μm) eliminate screen-printing as a viable option [29].

Ink jet printing provides an alternative deposition solution that limits material waste. The Dimatix printer in the Printed Electronics and Functional Imaging Department utilizes interchangeable, fillable ink cartridges, permitting GO ink printing. Achievable feature resolution ranges between 50 μm-100 μm. The dispensing nozzles vary between a 10 pL and 1 pL tip. The 10 pL tip provides the highest success probability. Dispensing nozzles clog easily; the 10 pL nozzles require ink solutions containing particles smaller than 0.45 μm. The dispensing head contains 16 nozzles, three of which must fire consecutively for the printer to operate. Graphenea GO particle sizes reach tens of microns [30], which exceed the maximum 0.45 μm permissible particles and clogs the printer nozzles, eliminating ink jet printing as a viable option.

The high surface tension and hydrophobic nature of water eliminates GO stamping as a solution. Reversing the polarity of the stamp to create microfluidic channels arose as a promising deposition method. Microfluidic channels guide the GO solution to specific regions and act as a frame for the GO solution during drying. Qiyuan He et. al produces graphene based biosensors utilizing microfluidic patterning in two separate fabrication attempts and reports reliability and

reproducibility of the devices [4, 5]. Microfluidic patterning became the primary method for GO deposition.

Creating PDMS stamps provide the means to pattern and deposit the GO solution. SU-8 molds first pattern the PDMS into the necessary channels. Removing the PDMS from the mold leaves indents in the PDMS that forms the channels that permit GO solution patterning. Punching holes in the PDMS creates inlets for the GO solution to enter the microfluidic channels once the PDMS contacts the substrate. Figure 5 displays the PDMS removal process and hole punching.

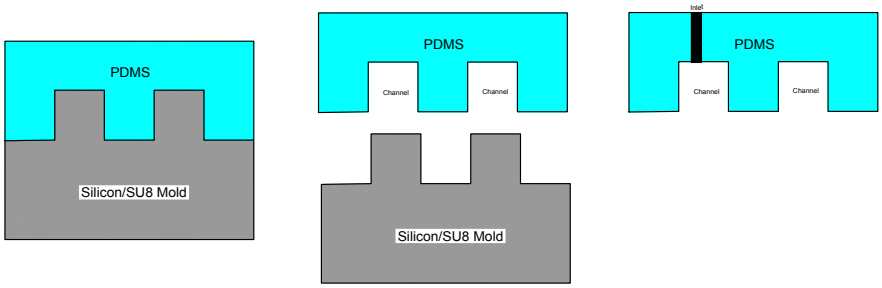

Figure 5. PDMS bonded to the SU8 mold (left). Removing the PDMS from the SU8 mold leaves channels in the PDMS (center). Inlet holes in the PDMS allow GO to flow through the PDMS channels (right).

Syringes create suction pressure that pulls the GO solution through the PDMS channels; however, this results in incomplete deposition. The unidirectional suction pressure prevents the side regions of the channel from experiencing GO volumetric flow. PDMS intrinsically self fills because of vacuum pressure subjection. This notion of self-filling channels became an option because a previous Cal Poly student studied this mechanism as a previous project [31]. Experimental testing confirms this intrinsic self-filling nature of PDMS channels, and Chapter 3 describes the process in more detail.

1.3 PROCESS FLOW

Processing steps have a wide variance in necessary temperatures, pressures, and cleanliness: which all affect the final device performance. This section provides a brief overview and sequencing of processing steps. Chapter 3 describes each processing step in-depth. The fabrication process requires a plethora of techniques, incorporating almost every facet in the micro-fabrication lab. Categorizing the fabrication steps condense the total procedure into easy to follow steps. Figure 6 displays the systematic addition of material layers that each stage encompasses.

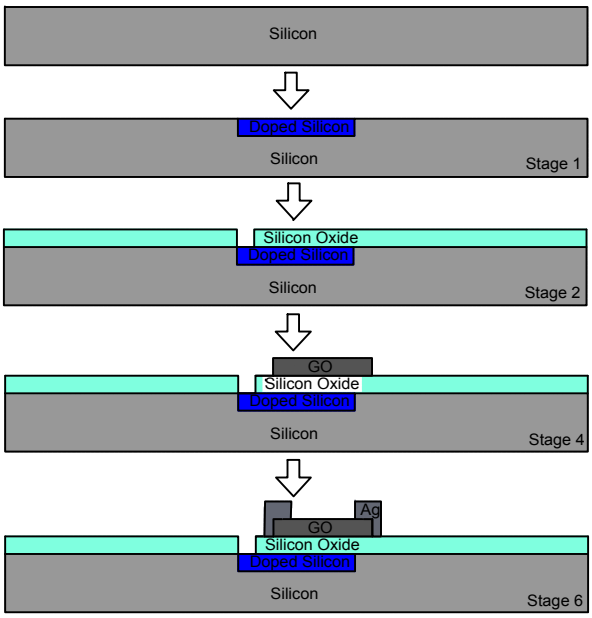

Figure 6. Device development denoting the addition of each material layer of the device.

Stage 1 encompasses bottom gate fabrication. Diffusion masks, utilizing silicon dioxide as the material layer, allow selective application of dopant atoms to create conductive channels within the 100 mm silicon wafer substrate. Selective doping entails a wide range of systematic

processes in the following order: oxide growth for diffusion mask, lithography, chemical etching, high temperature diffusion, and a couple intermediate material depositions using spin coaters.

Stage 2 encompasses creating the dielectric insulating layer. Silicon dioxide grown on the substrate serves this purpose. High temperature furnaces runs, under an oxygen atmosphere, facilitate silicon dioxide growth. Lithography and chemical etching creates vias permitting contact points to the bottom gates.

Stage 3 encompasses microfluidic channel creation. Figure 6 does not explicitly show Stage 3, because GO deposition includes Stage 3. Microfluidic channel creation separates into two subcategories: mold creation and channel creation. Mold creation requires several processing steps including material deposition, lithography and chemical development. PDMS first consists as a liquid solution that flows over the mold, adapting to each mold feature to create the microfluidic channel patterns. Mixing the PDMS solution creates air bubbles in the solution that requires vacuum treatment to remove the air bubbles before deposition onto the mold. Thermal curing of the PDMS transforms it into a solid.

Stage 4 encompasses graphene oxide deposition. Deposition entails vacuum treating PDMS channels for several hours and plasma treating the substrate. Appling PDMS channels onto the substrate create the framework to pattern complex graphene oxide designs. The graphene oxide air-dries for a minimum of 24 hours before subjection to a vacuum furnace or continuing air-drying. Once the water content in the GO solution evaporates, removal of the PDMS channels commences.

Stage 5 encompasses graphene oxide reduction. The entire substrate undergoes high temperature treatment in a nitrogen environment. The nitrogen atmosphere provides an inert

environment during the reduction process. Figure 6 does not explicitly show the reduction process, because the material layers do not change post the reduction process.

Stage 6 encompasses applying metallic contacts to the graphene electrodes. The thin nature of graphene creates the potential for probes to puncture the electrodes. Silver epoxy allows bonding of metallic contacts to graphene electrodes providing a mechanically robust and electrically conductive contact. Stage 6 concludes the device fabrication.

1.4 DESIGN OF EXPERIMENTS

Inherently, process development requires extensive experimentation to determine viable methods. The project consists of one experiment after another using a heuristic design approach. Prototype 1 uses several process variations including wafer type, GO drying conditions, physical device size, gate geometry, and GO solution to help tease out ideal processing procedures.

1.4.1 WAFER TYPE

All devices use either P or N type 100 mm wafers as their substrates. Scribing the wafers distinguishes them between P and N type. P type wafers contain a B scribing to denote boron-doped substrates; N type wafers contain a P scribing to denote phosphorus-doped substrates. The wafer types determine which, if either, gate channel type and bulk material produces better gating responses in the GO fractal. The bulk material doping creates concentrations of holes in P-type bulk substrates or electrons in N-type bulk substrates at the interface of silicon dioxide gate layer. The electrostatic interaction from these carriers provides the potential to induce contradicting responses and biasing of the graphene sheet.

1.4.2 DRYING CONDITIONS

Drying conditions create aggregating GO particles. The faster the process, the more the particles clump together resulting from the hydrophobic nature of water. Particle clumping produces poor devices, because electrical conductivity decreases with GO layer thickness. GO stacking produces graphite, a non-conducting material [16]. All devices experience drying for 24 hours at ambient room temperature and pressure. Half the devices remain in ambient pressure and temperature for an additional 24 hours before removing the PDMS stamps. The other half experiences 14 hours at 60 °C and 0.09 MPa. Table 1 documents which wafers experience which drying process.

Table 1. Drying methods for each device wafer. B (for boron doping) scribing represents P type wafers and P (for phosphorus doping) scribing represents N type wafers. The numbering distinguishes between specific groups of wafer type.

Wafers	48 Hours Air Drying	Vacuum Drying
	B1, B10, B11, P1, P9	B4, B7, B9, P2, P8

The vacuum oven drying method stems from a procedure used by Graphenea that produces highly conductive graphene sheets; however, they exclude pressure and duration in their documentation [25]. The drying methods produce fractal GO sheets on the substrates. The substrates contain several different scaling of fractals to determine how dimensions might affect the devices. The fractal patterning provides the proof of concept for the process to create complex GO patterns.

1.4.3 FRACTAL GEOMETRY

The physical size of the fractal changes the likelihood of gating the individual channels comprising the entire fractal. All sizes scale by factors of 2, using the largest fractal size (1 cm x 1 cm) as the base reference. The desire to compare CVD and rGO graphene sheets determines the fractal's maximum size. Trivial Transfer Graphene™ consists of 1 cm x 1 cm sheet. The fractal patterns scale by factors of 2 until reaching the 8000 dpi (3.175 μm) nominal printing resolution of the Dimatix Materials Printer. Equation (1) generalizes the calculation for minimum feature size and determines the maximum scaling factor. A maximum scaling factor of one-sixteenth doubles nominal resolution.

$$F_{minimum} = \frac{P}{3^n}, \tag{1}$$

where P represents the perimeter of the initial square, and n represents the desire sequencing number. Table 2 documents the minimum feature size of each fractal for printing characterization.

Table 2. Minimum feature size (channel widths) for the family of fractal with resolution to the nearest micrometer.

Scaling	Full	1/2	1/4	1/8	1/16
Minimum Feature Size [μm]	123	62	31	16	8

Scaling the fractal size also characterizes the lithography mask printing capabilities at Cal Poly discussed in *2.6 Photolithography Masks*. Figure 7 displays the family of fractals for size comparison relative to each other (not to scale) starting at the one-half scale and decreasing to the one-sixteenth scale. The red lines separate regions of GO deposition and locations of PDMS

posts. Any region enclosed by red lines represents a location of a PDMS post that prevents GO deposition in that region. The large white rectangular regions to the right and left of the fractal pattern represent GO electrodes that continually flow into the fractal pattern.

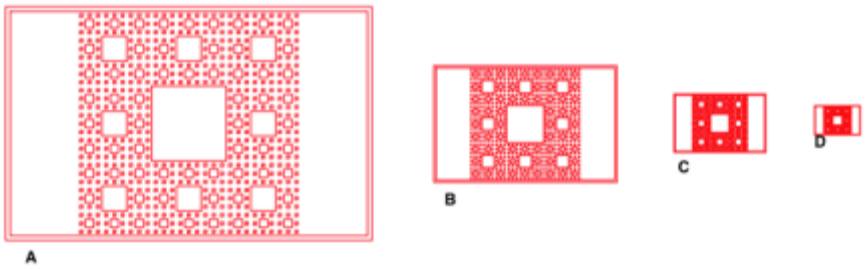

Figure 7. Fractal family relating the dimensions of each fractal to each other (not to scale). The scaling includes (A) one-half, (B) one-quarter, (C) one-eighth, and (D) one-sixteenth of the original 1 cm x 1 cm fractal. Regions encompassed by red lines (the squares within the fractal) represent regions where PDMS posts prevent GO deposition. Figure 11 contains an enlarged view of the fractal geometry.

Four distinct bottom gate geometries test orientation and thickness of the channels for their gating abilities. Figure 8 displays blue lines outlining the four gate patterns overlaid with the fractal pattern. Figure 8.A utilizes a diagonal gate pattern, producing the largest number of resistance regions. Figure 8.B contains the smallest channel width, and Figure 8.C provides the capability to gate the entire device width. Figure 8.D, arbitrarily chosen, adds variety. Table 3 documents the gate channels widths. These channel widths underestimate the actual size of the gates; reference *3.4 Stage 1: Bottom Gates* for more detail.

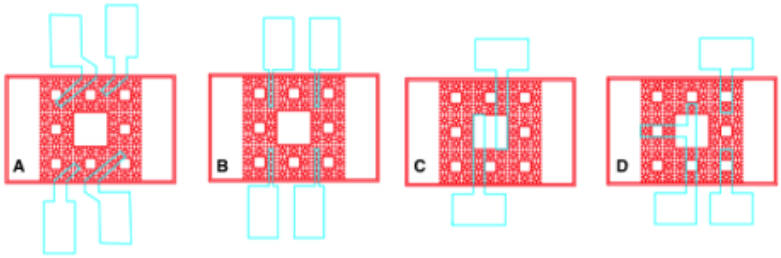

Figure 8. The four distinct gate patterns overlaid with the fractal pattern. The blue lines outline the gate patterning and the red lines outline the location of PDMS stamps that prevents GO deposition. The large square in the middle represents a PDMS post. White regions between PDMS post represent regions of GO deposition.

Table 3. Gate feature sizes for the family of fractals to the nearest micron. The gate designs references the blue outlines in Figure 7 above.

Gate Design [μm]	Scaling				
	Full	1/2	1/4	1/8	1/16
A	698-1358	349-679	175-340	87-170	44-85
B	370	185	93	46	23
C	1111	556	278	139	69
D	864-1110	432-555	216-278	108-139	54-69

The devices incorporate three GO solutions: Graphenea produces two of the GO solutions consisting at various weight percentages and Cal Poly chemistry department synthesizes a GO solution. The weight percentages produce GO films of different thicknesses. Each GO solution experiences all experimentations outlined above. The Graphenea and Cal Poly solutions differ in weight percentage and elemental content, described more in-depth in *3.3 GO Characterization* and *4.1 Graphene Sheet Characterization*.

1.5 CONTROL WAFER

A control wafer consisting of a known semiconductor would provide a means to isolate the gate and dielectric layer from the rest of the device to confirm the bottom gates operate as intended. Dr. Bob Echols in the physics department uses P3HT to produce solar cells. The known properties and wide acceptance in industry of P3HT quickly confirms the choice to use it for the control wafer [32]. The accessibility of P3HT and the ability to pattern the material using only high intensity UV light that the photolithography machines produces made it an ideal choice. P3HT degrades when interacting with normal atmospheric air, a property realized late in the design process that prevents constructing a control wafer. The solar cell fabrication that Dr. Echols conducts takes place in a glove box under nitrogen environment. The photolithography machines in the clean room do not provide the necessary nitrogen environment to sustain the P3HT solution. The facility limitations prevent fabricating a control wafer.

2. DEVICE DESIGN AND MATERIAL SELECTION

Available resource on campus limit the possible fabrication processes. Cal Poly lacks the reputation as a research school, finding resources and infrastructure for fabrication became one of the largest challenges to overcome. Despite inherent limitations, fabrication processes develop. The material layers necessitate compatibility with future processing steps; the necessary high temperature to reduce the GO to rGO limits material possibilities more than any other process during fabrication. Figure 9 displays a fishbone diagram relating fabrication processes to each material layer.

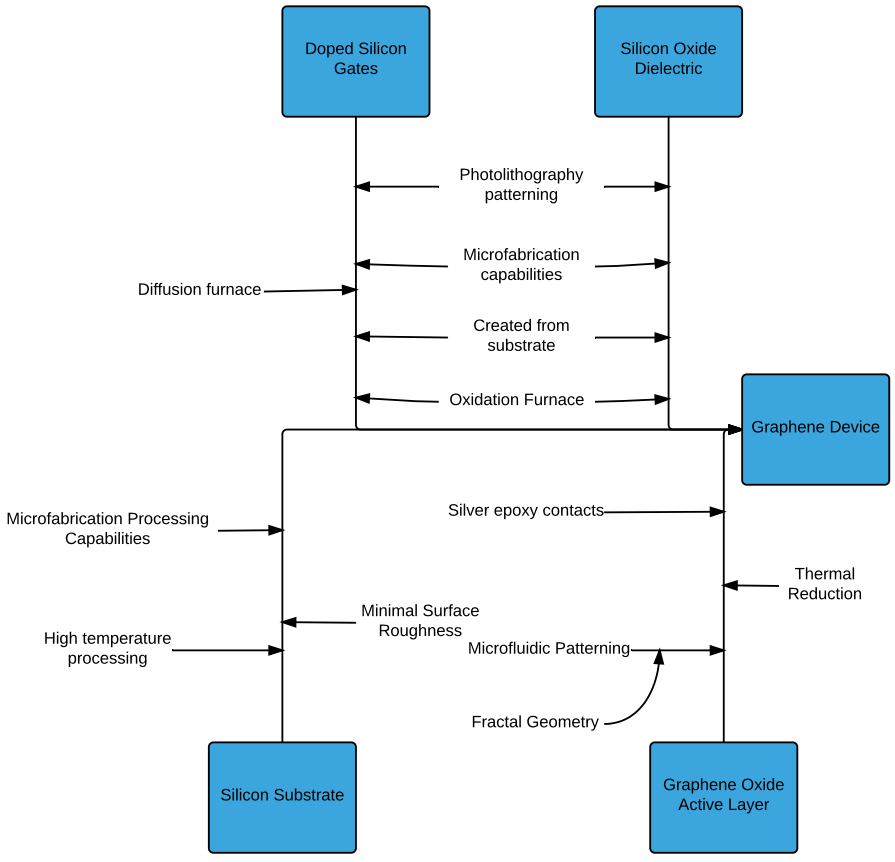

Figure 9. Fishbone diagram connecting fabrication processes to material layers in the graphene device.

The rest of the chapter delves into greater detail justifying material selection and design starting with the geometric fractal pattern of the GO solution. Considering several materials for each device layer results in selecting materials compatible with on campus fabrication techniques that promise to produce a functioning device. The remainder of this chapter discusses these considerations and selections; but first, the following section describes how to construct a Sierpinski carpet.

2.1 FRACTAL CONSTRUCTION

Selecting a geometric design to produce graphene electronics represents the first design constraint to overcome. The fractal Sierpenski carpet accomplishes two goals. Most importantly, the fractal pattern confirms complex patterning capabilities for future designs, a necessary proof of concept to create an adaptable process. Dr. Marlow desires a fractal Sierpenski carpet pattern to experimentally test theories suggested by her colleagues about the nonlinear response of gating a Sierpenski carpet [1]. The scope of this thesis does not include testing for the nonlinear responses. The 1cm x 1cm graphene sheets limit the maximum device size. Dr. Marlow desires a four sequence Sierpinski carpet, which provides the secondary design constraint.

Constructing of a Sierpinski carpet incorporates a repeatable pattern that divides a square into 9 congruent squares, creating a 3x3 grid matrix. Removing the center square leaves eight squares that encase the center square of the 3x3 grid matrix. Repeating this pattern for the remaining eight squares creates the fractal symmetry. Figure 10 displays the first two sequences to create a Sierpinski carpet.

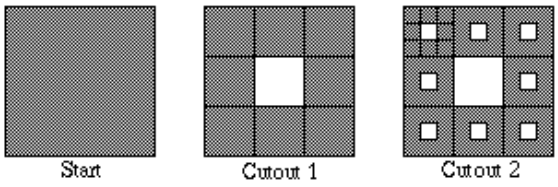

Figure 10. Forming a Sierpinski Carpet [12].

Electrical connection to the fractal necessitates electrode contact points. Extension of the fractal width creates GO electrodes. Horizontal extension of the fractal pattern allows electrical contact without damaging the fractal. Figure 11 displays the resulting pattern.

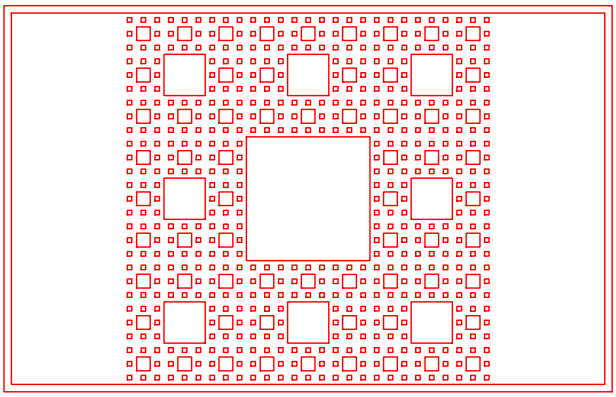

Figure 11. CAD rendered image of a Sierpinski carpet design that creates the photolithography mask. Extension of the fractal width provides a region for electrode contact. Image not to scale.

2.2 SUBSTRATE

The previous section discusses the geometric construction of the device; the next challenge encompasses choosing a substrate capable of surviving the reduction process that also provide a smooth surface for GO deposition. Ideally, monolayer graphene acts as the active material in the final device. A single atom thick sheet of carbon produces monolayer graphene [14, 15]; this makes the graphene sheets extremely easy to puncture. If the substrate contains surface roughness substantially greater than the film thickness, discontinuities form in the active layer. The substrate plays a critical role in the final device functionality.

Silicon wafers provide a low surface roughness substrate material. The micro-fabrication lab centralizes around 100 mm wafer processing, allowing use of the equipment already present on campus. Other material substrates, such as mica, would improve device performance but cause complications later in the fabrication process such as applying bottom gates with material characteristics that exhibit a melting temperature above the required 1000 °C for thermal reduction. Shi et al. use mica substrates because of its excellent surface roughness [26]. Shi et al. also documents that silicon dioxide substrates has a surface roughness capable of affecting the reliability of the device [26]. The traditional use of silicon in transistors and extensive documentation of processing procedures made it the obvious choice of substrate. The silicon wafer produces the substrate, gate, and dielectric layer of the devices.

Bryan Sennett at Strasbaugh generously provides 18 100 mm P-type silicon wafers that he processed to ensure surface roughness below 1nm. N-type wafers purchased from University Wafers provide the second wafer type. The wafers provide a planar surface to grow the gate oxide. Non-uniform oxide layers could arise due to poor thermal regulation of the oxidation furnace causing variance in oxide growth rates relative to wafer position and orientation. The gate

oxide thickness contains great variance depending on wafer position. The surface roughness resulting from poor thermal oxidation could cause discontinuities in the GO traces, producing defective devices. Chapter 3.5 contains Table 14 that documents oxide thickness ranges between perfectly uniform and a 15 nm difference. Wafers closest to the oxygen intake produce less oxide because the oxygen gas flow cools this wafer more than the other wafers. Calculating GO thickness in Chapter 4 confirms the GO thickness exceeds the surface roughness; thus, the surface roughness should not a play a factor in the device functionality.

Although silicon allows creating the gates and dielectric material layers, other material considerations arose. The next two sections document material considerations for the gate layer and dielectric layer.

2.3 GATE LAYER

Originally, silicon gates provide an unattractive gate layer because of the difficulty to quantify the conductivity and junction depth of the doped silicon. Stain and groove processing on campus do not produce useable measurements. Metal gates provide a more attractive option because of the controllability of metal deposition using the sputtering machines and known intrinsic conductivity of metals. Metal gates also provide a means to create gates on substrates such as mica. Aluminum represents the metal of focus, because the micro-fabrication lab already sputters aluminum for transistor gate contacts; however, it contains a melting temperature of 660 °C. Incompatibility of metals in the reduction process results in selecting doped silicon to produce the gates.

Doped silicon produces the gate channels. Silicon provides an attractive solution because of its doping ability, processing capabilities at Cal Poly, and high temperature capabilities. Potential issues using silicon as the gate layer arises when trying to isolate individual gates, because dopant atoms diffuse isotropically into the silicon substrate. Large channel between the gates promise to prevent shorting issues. Reverse biasing the PN junction can also eliminate shorting issues between the gates.

Each wafer type requires a separate dopant atom to create the gate channels. Boron dopant creates the gates in the N type silicon substrate, and phosphorus creates the gates in the P type silicon substrate. The micro-fabrication lab already uses both boron and phosphorus to dope silicon in the transistor fabrication course (BMED 435) [2]. Using boron and phosphorus allows using the micro-fabrication processing steps previously completed during BMED 435 [2]. The dopants diffuse into the substrate when subjected to high temperatures. *3.4 Stage 1: Bottom Gates* outlines the doping process. Vias in the dielectric layer permit electrical contact to the gates.

After gate creation using doped silicon, silicon dioxide produces the dielectric layer separating the gate channels from the GO material layer. The next section delves into details pertaining to selecting silicon dioxide as the dielectric layer.

2.4 DIELECTRIC LAYER

The dielectric insulating layer greatly affects the threshold voltage to obtain gating. Thick insulating layers diminish the electric field strength responsible for depleting regions of carriers. Thus, the major design constraint necessitates a thin dielectric layer. Industry maintains gate oxide thicknesses less than 100 nm and desires 2-3 nm. The other design constraint requires compatibility of the insulating layer with future processing steps.

The wide acceptance of parylene as an industrial insulator promotes parylene as a consideration for the dielectric layer. Vapor depositing Parylene creates very thin, precise film thicknesses. Previous interactions with Kisco Conformal Coatings (KCC) to produce a capacitive test chamber created a good relationship between John Greene and KCC that could allow for potentially free deposition. The melting temperature of parylene creates thermal limitations that prevent it from meeting all the material constraints. Consideration of PDMS, PMMA, and aluminum oxide proves futile, because their material layers also prevent subsequent processing steps. All the materials mentioned would melt during the thermal reduction processing of graphene oxide except for the aluminum oxide. Aluminum only forms a few nanometer thick sheet of oxide during oxidation [33]. Any residual aluminum would melt during the reduction process and destroy the device; thus, silicon dioxide surfaces as the material to use for the dielectric layer.

Silicon dioxide provides the best option as the dielectric layer because of its growth capability using the oxidation furnace. Integrated circuits primarily used silicon dioxide as the dielectric layer for decades after their invention, and it represents the dielectric layer chosen during transistor fabrication in BMED 435, confirming its high performance capabilities. The oxide growth temperature determines the dielectric quality of the oxide; high temperature growth

improves breakdown characteristics [17, 34]. Metrology limitations of the FilmMetrics F20 metrology unit prevent measurements of oxide films below 43 nm. Strasbaugh owns an ellipsometer producing similar minimum detectability thresholds. Reference Chapter 3 for information regarding the growth procedure. Growing oxide layers ranging between 40 nm-60 nm helps determine the effects of the dielectric layer thickness relative to device performance and threshold voltage. Equation (2) below calculates the threshold voltage of a silicon transistor [15],

$$V_T = \frac{Q}{C_{ox}} + 2\phi_F + \frac{Q_{ox}}{C_{ox}} + \phi_{ms}, \tag{2}$$

where Q equals depletion charge of the graphene, C_{ox} equals the oxide capacitance, ϕ_F equals built in potential between the intrinsic Fermi energy and the channel Fermi energy, ϕ_{ms} equals the metal-semiconductor work function, and Q_{ox} equals the oxide charge. Equation (3) only focuses on the first term in Equation (2).

$$V_T = \frac{Q}{C_{ox}} \tag{3}$$

Equation (4) calculates the depletion charge [15],

$$Q = \sqrt{2qN_A\mathcal{E}_s|2\phi_F|}, \tag{4}$$

where q equals the charge of an electron, N_A equals doping concentration of graphene, $\mathcal{E}_s$ equals the dielectric constant of graphene and ϕ_F equals built in potential between the intrinsic Fermi energy and the channel Fermi energy. A high doping concentration selection accounts for graphene's high conductivity; N_A equals 1 x 10^{20} atoms per cm^3. The dielectric constant of

graphene equals 3.3 [9]. The $2\phi_F$ term assumes a value of 1 eV. Using these values, the depletion charge equates to 3.05 x 10^{-6} C/cm^2. The equation above provides a rough estimate that may produce incorrect values, since its traditional use characterizes silicon transistors, not graphene devices. Equation (5) calculates the oxide capacitance [15],

$$C_{ox} = \frac{\mathcal{E}_{ox}}{t_{ox}}, \tag{5}$$

where $\mathcal{E}_{ox}$ equals the dielectric constant of silicon dioxide and t_{ox} equals the thickness of the silicon dioxide. The dielectric constant of silicon dioxide equals 3.9 times the dielectric constant of a vacuum. The oxide capacitance equals 8.63 x 10^{-11} F/cm^2 for an oxide thickness of 40 nm. Figure 12 plots threshold voltage against oxide thickness.

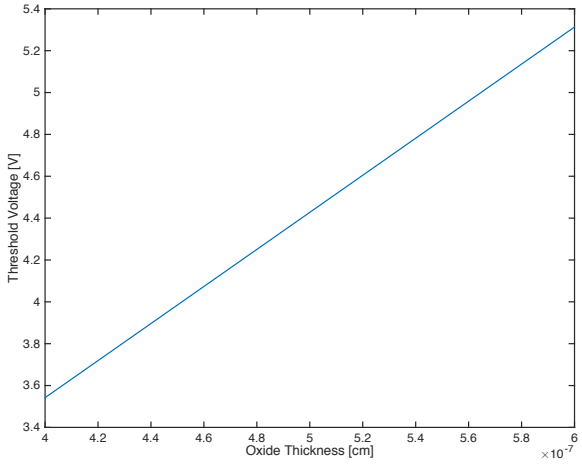

Figure 12. Theoretical threshold voltages for the devices relative to silicon dioxide thickness. The graph does not start at the origin.

Figure 12 produces large threshold voltage values. Difficulty arises calculating theoretical values of these devices, because graphene electronics have just begun emerging in the past decade [7, 15] and characterizing their properties requires experimental testing. The dielectric layer insulates the gates from the active GO layer. Once the silicon dioxide layer grows onto the substrate, depositing the active layer commences. The next section discusses characterizing the active layer.

2.5 ACTIVE LAYER

The active layer represents the main material layer under analysis. The silicon dioxide dielectric provides a planar surface for graphene deposition. Chemical vapor deposited (CVD) monolayer and several layer (6-8) graphene sheets, purchased from ACS materials, provide the purest form of graphene under analysis. CVD methods allow greater control of thin film production that ensures a pristine graphene sheet. Difficulties arose during graphene sheet patterning resulting from failure to produce an effective means to selectively etch the graphene sheet using the reactive ion etcher (RIE). RIE uses plasma to etch material layers. Since plasma remains in a gaseous state, the etch mask requires bonding to the substrate. This produces the potential to damage the graphene sheets. No devices use the graphene sheets from ACS Materials. Future experiments could use the sheet to test sensor capabilities. GO solution produces the graphene active layer. Graphenea provides one brand of GO solution, while Cal Poly provides the seconds brand. Both GO solutions contain different elemental content. Table 4 documents the elementals composing the Graphenea brand GO.

Table 4. Elements comprising the GO solution purchased from Graphenea [4].

Element	Composition Percent [%]
Carbon	49-56
Oxygen	41-50
Hydrogen	0-1
Nitrogen	0-1
Sulfur	0-2

Metrology using an EDS (Energy Dispersion Spectrometer) produces elemental content of the Cal Poly brand GO solution. Three analyses from the EDS confirm the elemental analysis.

Depositing the GO solution via syringe onto a silicon wafer that dries on a hot plate produces the sample for analysis. Table 5 documents the elemental composition results.

Table 5. Elemental results from the EDS measurements. The silicon content arises because of the substrate.

Trial	Element [Atomic %]						
	Carbon	Oxygen	Sodium	Silicon	Sulfur	Potassium	Manganese
1	72.84	25.07	0.17	1.4	0.47	0.02	0.03
1 Error [±]	0.54	0.25	0.01	0.01	0.01	0.00	0.00
2	73.19	24.44	0.16	1.72	0.43	0.04	0.02
2 Error [±]	0.53	0.24	0.03	0.01	0.01	0.01	0.00
3	72.58	24.57	0.16	2.05	0.57	0.04	0.02
3 Error [±]	0.57	0.24	0.03	0.01	0.01	0.01	0.00

Michaela Pfau, MS chemistry alumni, synthesizes GO solution using the Hummers Method below and explains the chemical mechanisms that produce it. The manganese oxide oxidizes the expanded graphite. Thermally treating the graphite-intercalated compounds (GIC) creates the expanded graphite (EG) that facilitates oxidation into single sheets of graphene.

Graphene Oxide-Hummers Method

Chemical Formulations:

$KMnO_4 + 3H_2SO_4 \rightarrow K^+ + MnO_3^+ + H_3O^+ + 2HSO_4^-$

$MnO_3^+ + MnO_4 \rightarrow Mn_2O_7$

Procedure:

1. *Mix sulfuric acid (30mL) and nitric acid (10mL) with a 3:1 volume ratio in an ice bath.*

2. *Mix Graphite flakes (1g) together with the solution in an ice bath. Remove from the ice bath; maintain the solution at room temperature under stirring for 24 hours.*
3. *Pour the mixture slowly into 200mL water to collect the solid by filtration. Wash the solid using water three times until pH reaches 5. Drying at 60°C for 24 hours produces the GICs.*
4. *Thermally treat the GIC powder at 1050°C for 15 seconds to get EG.*
5. *Mix EG (1g) and 200mL sulfuric acid in a flask submerged in an ice bath.*
6. *Add $KMnO_4$ (10g) drop-wise to keep the temperature below 20°C.*
7. *Remove the ice bath and keep the solution at 35°C under stirring for 3.5 hours or until the paste forms. The mix gradually becomes viscous and eventual becomes pasty.*
8. *Transfer the mix to an ice bath and add DI water (200mL) to quench the oxidization reaction under stirring for 30 minutes.*
9. *Pour 10 mL H_2O_2 (30%) slowly under stirring to the mix to reduce the residual permanganate and manganese dioxide to soluble manganese sulfate. After 30 minutes, a bright yellow solution results.*
10. *Centrifuge the solution to obtain a Filter yellow-brown cake. Wash with 1mL HCL. Disperse in water until the pH reduces to 5. This takes several washings.*

The active layer GO solution represents an important parameter of the device. If the starting solution is of poor quality, the fabrication process results in poor quality devices. Small feature sizes increase the probability of functional devices but photolithography masks limit the minimum feature resolution. The next section discusses creating photolithography masks.

2.6 PHOTOLITHOGRAPHY MASKS

Device fabrication requires several photolithography masks for various processing steps. The following processes require a photolithography masks: dopant diffusion, contact via etching, and microfluidic channel creation. The printed electronics and functional imaging department provides the equipment necessary for creating all the photolithography masks. The printed electronics department generally deals with macro-size features and never tested the true capability of the printer; thus, this project characterizes the smallest obtainable feature size. The nominal 8000 dpi printing resolution should produce minimum feature sizes reaching 3.175 μm; however, a minimum features size of 31 μm was achievable. Figure 13 shows unsuccessful SU-8 fractal molds resulting from poor photolithography mask printing.

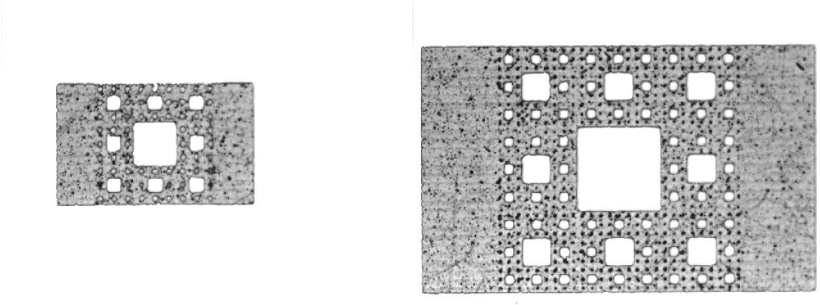

Figure 13. Unsuccessful SU-8 molds for the one-sixteenth scaling (left) and one-eighth scaling (right).

The photolithography masks consist of an opaque black carbon deposited onto a transparent substrate. Initially, the carbon coats the entire transparency. The CDI Spark 2530 Inline UV printer ablates carbon in the patterns dictated by an Adobe Illustrator file. Figure 14 displays the printer.

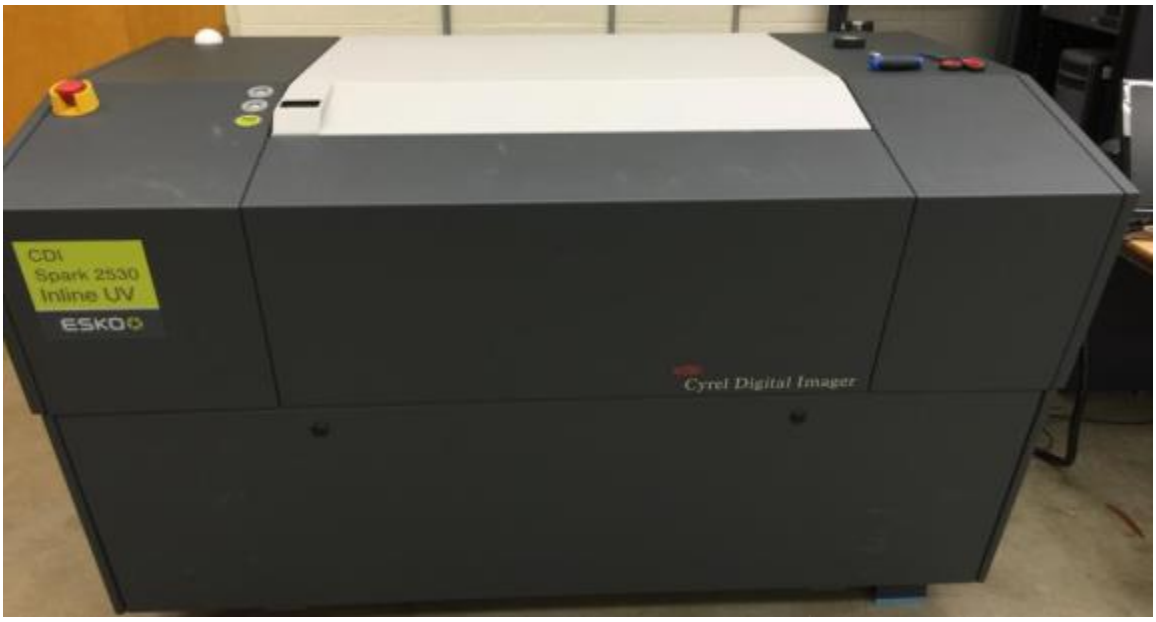

Figure 14. CDI Spark 2530 Inline UV printer that oblates carbon to create photolithography masks.

Horizontal streaks noticeable in the one-eighth scaling in Figure 13, documents a fundamental issue with the CDI Spark 2530 Inline UV printer. Figure 31 in Chapter 3.6 also documents the horizontal streaks. The laser leaves a residue where it hits and creates observable horizontal line patterning. Intensity of light and focus modulations on the printer could improve the print quality. These defects do not produce issues for rapid prototyping. Figure 15 displays the produced shadow masks.

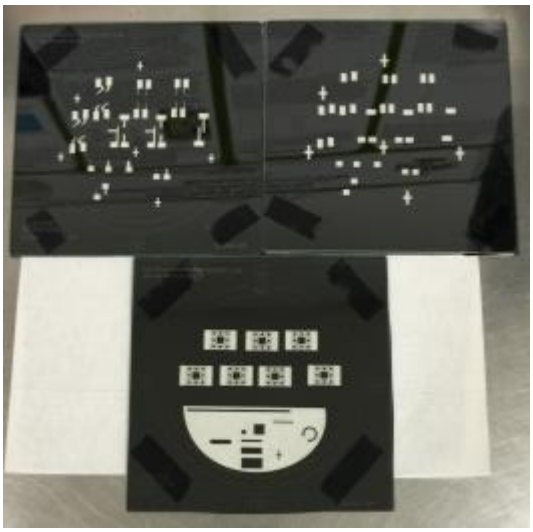

Figure 15. Photolithography masks produced by the printed electronics and functional imaging department. Top left produces the diffusion pattern for dopants. Top right produces the contact vias. Bottom produces the pattern in SU-8, creating the mold for the PDMS microfluidic channels for full-scale devices.

Handling the lithography masks requires care. Oils from human skin contaminate the emulsion (carbon) on the transparencies. Acetone and IPA also damage the carbon. Taping the transparencies onto glass blanks provides rigidity for the lithography mask. The plastic side of the transparency makes contact with the glass; this improves patterning because it limits diffracting light rays that could make features larger than desired.

Producing the lithography masks on campus greatly reduces lead-time waiting for the lithography masks. Producing the masks on campus saves minimum of one week in fabrication and greatly reduces the cost to obtain the lithography masks.

2.7 CLOSING REMARKS

The material layers of the devices represent an important design stage of the project. The available processing equipment and techniques on campus as well as the GO reduction provide great design constraints on the material layer selection. With known material layers, fabricating the device commences. Chapter 3 describes the fabrication steps to produce the device.

3. EXPERIMENTATION AND DEVICE FABRICATION

Fabricating graphene electronics requires a plethora of processing steps, some of which repeat for several of the stages described in Chapter 1. The previous chapter explains material selection for processing so that this chapter can delve into details of the fabrication processes. Summarizing the cleaning and lithography processes, which repeat several times throughout the fabrication, condenses these explanations into subsections. Fabrication uses a bottom up approach that first develops the bottom gates and gate oxide before depositing the GO solution. Prior to the GO deposition, fabricating the microfluidic channels creates the mold to pattern and deposit the GO solution. Depositing silver epoxy contacts after the reduction process allows probing of the GO fractals, concluding the processing steps necessary to create the devices. Chapter 4 deals with device characterization.

3.1 CLEANING PROCEDURE

The cleanliness of the wafers affects the device performance tremendously. Any foreign particle causes defects when depositing material layers that disrupt the performance of the device. Organic molecules present during furnace processing burn and cause vapor contamination on the wafers. Extensive cleaning procedures minimize the chance of contamination. All cleaning steps require Teflon cassettes and handles, because Teflon does not react with the piranha or hydrofluoric acid (BOE) solutions. Figure 16 displays the cleaning process.

Figure 16. Cleaning process for the wafers. BOE (Buffer Oxide Etch) represents hydrofluoric acid.

The cleaning procedure consists of submerging the wafers in piranha solution for 10 minutes at 70 °C. Piranha solution consists of a 9:1 ratio of sulfuric acid (98%) and hydrogen peroxide (30%). A glass beaker contains the piranha solution that sits on a hot plate to raise the temperature. Elevating the temperature increases the chemical reaction rate that dissolves organic particles. After the 10-minute duration, a quench rinse consisting of dunking the wafers four times into DI (deionized) water ensures harmful chemical removal. Stages 1 through 4 in Figure 6 require piranha cleaning. For stages 1 though 3, the wafers also undergo cleaning in hydrofluoric acid.

The hydrofluoric acid removes any non-organic contamination but does not damage the silicon substrates. A Teflon container houses the hydrofluoric acid. The solution remains at room

temperature, submerging the wafers for 35 seconds produces a clean surface. The duration of submersion changes depending on the processing step. Hydrofluoric acid dissolves silicon dioxide, thus, patterning the gate oxide necessitates a shorter duration of 5 seconds to create a clean surface before photoresist deposition. After the quench rinses, another rinse cycle in the sink using DI water from the faucet commences before placing the wafers into the SRD (spin rinse dry). The SRD contains an armature that spins at thousands of RPMs; the wafers are doused with DI water before heated compressed air aids in the drying process.

Piranha and BOE require extreme caution when handling. Operators must gown a chemical apron, face shield, and secondary gloves. Cleaning processes occur during every processing stage preceding GO deposition. Maintaining a clean environment and surface greatly improves the probability of producing functioning devices.

3.2 PHOTOLITHOGRAPHY

Photolithography allows photosensitive material patterning to produce an etch mask during oxide patterning. Shipley S1813 PR (photoresist) creates the etch mask. All processing related to photolithography commences in the alignment room that filters blue light. Blue light contains sufficient energy to cause the PR to begin reacting. PR storage requires low temperatures that make the solution viscous; remove the PR a day before processing to allow the PR to reach room temperature. Spin coating the PR onto the wafers ensures a planar surface. Figure 17 provides a high level diagram of the photolithography process.

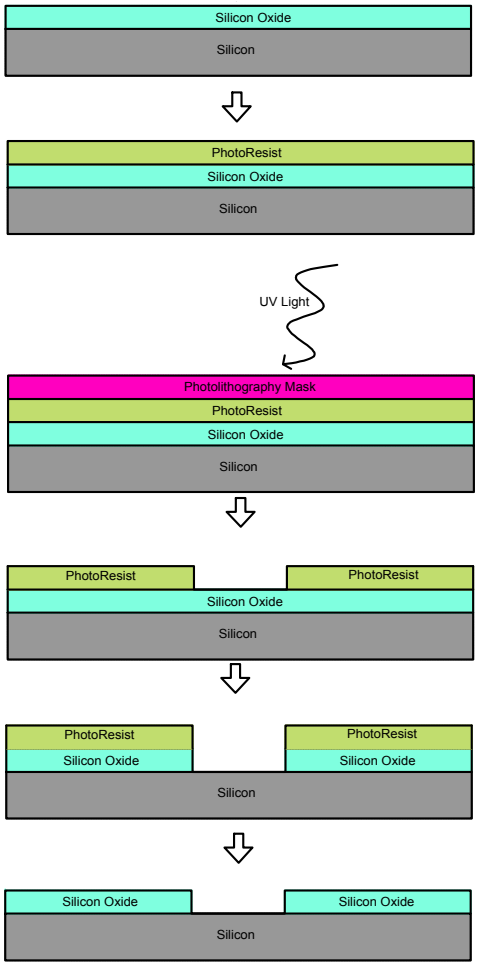

Figure 17. Wafer material layers during photolithography processing.

Photoresist (PR) spun onto the wafer produces the material layer for the etch mask. Figure 17 implements positive photoresist. Positive photoresist dissociates under UV light while negative photoresist cross-links. A photolithography masks selectively allows UV light to interact with the PR. HMDS MCC 80/20 primer improves the adhesion of the PR to the silicon dioxide surface. Spin coating consists of 4 major sequences: dispersing and planarizing the primer followed by dispersing and planarizing PR. Slower spin speeds disperse the material over the entire substrate. The planarization cycle follows the dispersion cycle, which uses high spin speeds to create a uniform surface. Table 6 documents the spin program for PR.

Table 6. Spin coating recipe for Shipley S1813.

Function	Duration [s]	Speed [rpm]
Spread HMDS	30	300
Planarize HMDS	20	3000
Deposit PR	30	0
Spread PR	60	600
Spread PR	10	500
Planarize PR	20	4000
Shut down	5	300

The Eppedorf Pipette dispenses the primer solution. Combining of a sterilized syringe and luer cap dispenses the PR. Apply 2.5 mL of primer to each wafer before starting the spin program. During the 30-second pause in the program, dispense 4-5mL of PR onto the wafer. After the program finishes, place the wafers on a hot plate at 90 °C for 60 seconds to evaporate the solvents out of the PR. Place the wafers on an aluminum heat sink to cool. The GAM aligner transfers the pattern printed onto the lithography masks to the PR.

The aligner lamp requires a half-hour warm up period to ensure consistent light intensity. House air, nitrogen, and vacuum lines all attach to the aligner; turn the valves for each gas line to the on position. The optics of the aligner rotates to permit access to load the photolithography

masks. Symmetrically align the mask vertically and horizontally by manual manipulation before securing it to the aligner via a vacuum chuck. After loading a wafer, the entire alignment stage moves together; the mask and wafer platforms move individually otherwise. A cross hair alignment pattern located on the left side of the alignment platform helps ensure consistent wafer location relative to the mask upon loading. Center the cross hair before loading wafers.

The GAM contains a seven-segment display that instructs the operator for processing steps. After pressing the wafer load button and the seven-segment displays load wafer, push the wafer stage into the alignment stage. The wafer lowers to several hundred microns for calibration before raising the wafer to -30 μm from the mask. Once the seven-segment displays reads -30 μm, position the wafer to the correct alignment relative to the mask. The right joystick controls the in plane (X-Y) position while the left joystick controls rotation (theta). The optics view two regions simultaneously, both fields of vision must align symmetrically with each other before exposure. The "Contact" button raises the wafer to -10 μm from the mask. The "Expose" button initiates the automatic removal of the optics and inserts the lamp. An analog timer sets the exposure duration.

An exposure matrix confirms theoretical exposure time. Equation (6) displays the equation that calculates the necessary exposure dose. The PR data sheet provides the necessary exposure dose of 150 mJ/cm^2 [2]. The lamp outputs UV light with an intensity of 14.8 mW/cm^2.

$$t_{exposure} = \frac{Exposure\ Dose}{Lamp\ Intensity} \tag{6}$$

$$= \frac{150\left[\frac{mJ}{cm^2}\right]}{14.8\left[\frac{mW}{cm^2}\right]}$$

$$= 10.1\ s$$

The exposure matrix partitions a wafer into eight quadrants that each receives a different exposure dose. Figure 18 displays a cartoon of the exposure matrix denoting the exposure time for each region. No noticeable difference between each quadrant arose; selecting the minimum exposure time (10s) decreases total processing time. Previous GAM operators turned off the shutter that enables precise duration of UV exposure; exposure duration of 20 seconds results due to the shutter confusion, and future wafers use a 20 second exposure time to keep consistent with previous wafers.

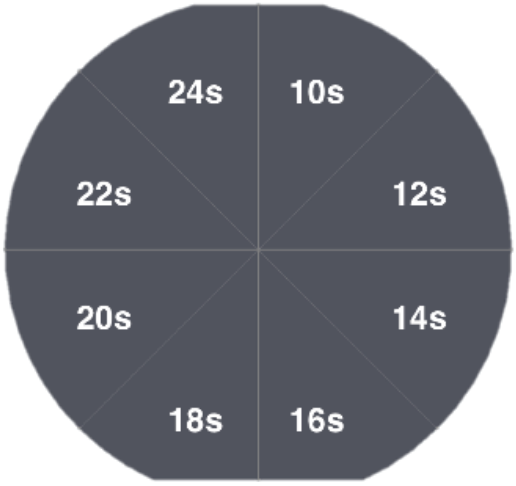

Figure 18. Exposure matrix used to determine optimal exposure dose.

Developing the PR removes PR that interacts with the UV light. A glass beaker houses the Microposit CD-26 developer. Submerging the wafers in the developer for 3 minutes at room temperature successfully removes the undesired PR. After rinsing the wafers four times in a DI water beaker, the wafers bake on a hot plate set for 150 °C for 1 minute to fully cure the PR. This concludes photolithography for oxide patterning. Submerging the wafers in BOE then transfers the pattern in the PR to the oxide. Submerging the wafers in PR stripper for 10 minutes at 60 °C removes the PR etch mask, leaving the patterned oxide.

Photolithography transfers all the desired features to the wafers and allows patterning of diffusion masks, gate oxide layers, and SU-8 microfluidic channels. Photolithography represents a key processing step at several stages of the project. The chapter continues with characterizing the GO solution.

3.3 GO CHARACTERIZATION

The composition of the GO solution plays a critical role in the performance of the electronics and possible fabrication methods. The Dimatix Material Printer in the printed electronics and functional imaging department utilizes a 10 pL nozzle that requires the solution to first pass through a 0.45 μm filter. The solution instantly clogs the filter indicating particle sizes exceeding the 0.45 μm maximum requirement. Consultations with Graphenea provide information about their GO solution.

Graphenea provides documentation about the graphene oxide particle sizes; Figure 19 displays their images of the particles. The GO solution contains particles exceeding 20 μm. Graphenea suggests sonicating the solution to reduce the particle size.

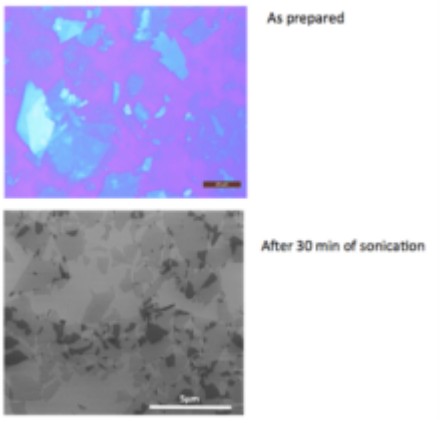

Figure 19. Graphene oxide particle size before and after sonication by Graphenea [30]. The top scale bar equals 20 μm and the bottom scale bar equals 5 μm.

The GO solution remains in its original container during sonication. The GO solution floats in a sonication water bath for one hour. The solution temperature noticeably rose as determined by sensory touch. Several bubbles formed in the solution. During sonication, the particles should have broken into smaller particles, potentially releasing oxygen functional groups that form the bubbles.

The Scanning Electron Microscope (SEM) promises the potential to characterize GO particle size post sonication. The SEM samples consist of approximately 50 μL of GO solution on a silicon wafer containing a top surface of silicon dioxide. SEM imaging provides an opportunity to explore drying method effects while characterizing particle size. Samples use two drying techniques: air-drying and hot plate (120 °C). The air-drying samples cure for one day; the hotplate evaporates the GO solvent (water) in 1 minute and 15 seconds and displays a coffee ring effect. All samples experiences one hour in a vacuum oven at 80-87 °C at a pressure of 0.09 MPa. Loading the samples lowers the oven temperature and causes the temperature fluctuations. The optical characteristics of the samples change after the oven processing, most likely resulting from reduction process initiation. Reduction changes the composition of the films and thus changes the optical properties. Figure 20 displays SEM images of the two sample types. The hotplate samples display many more defects than the air-dried samples. The hydrophobic nature of water causes it to bead up, resulting in GO particle aggregation. Air-drying the samples limits aggregation and produces vertically polarized (relative to picture orientation) defects. Air-drying became the dominant method of drying for this reason.

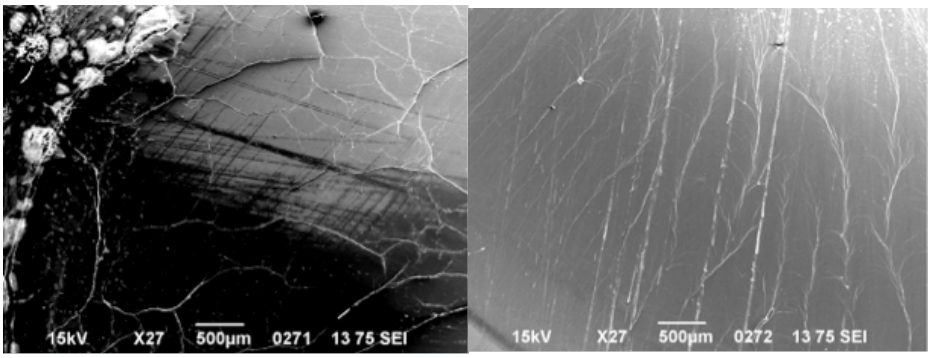

Figure 20. SEM images of GO samples. One sample utilizes drying on a hotplate at 60 °C (left) and the other uses air drying for one day (right). The air-drying samples produce more uniform GO sheets than the samples dried on the hotplate.

The SEM provides the most viable option for particle size characterization but fails to produce any useful measurements, suspension of future particle size characterization results. The Graphenea GO solution produces the SEM samples. Only the Graphenea solution experiences SEM imaging because the elemental composition provided by Graphenea ensures no damage to the SEM would arise.

Analysis of the drying method uses the Graphenea GO solution and two batches of Cal Poly GO solution. The three solutions experience the drying methods outlined above. Using a VKX250 Laser Confocal microscope provided by Keyence, images of the hotplate samples illuminate the terrain of the GO samples. The Keyence measurement was an unplanned, opportunistic resource that prevents imaging of the air-drying samples. The microscope allows terrain measurements of the graphene samples; Figure 21 displays the resulting images. Aggregating GO particles cause mountainous terrain to form in localized regions. Table 7 records the maximum height of each sample.

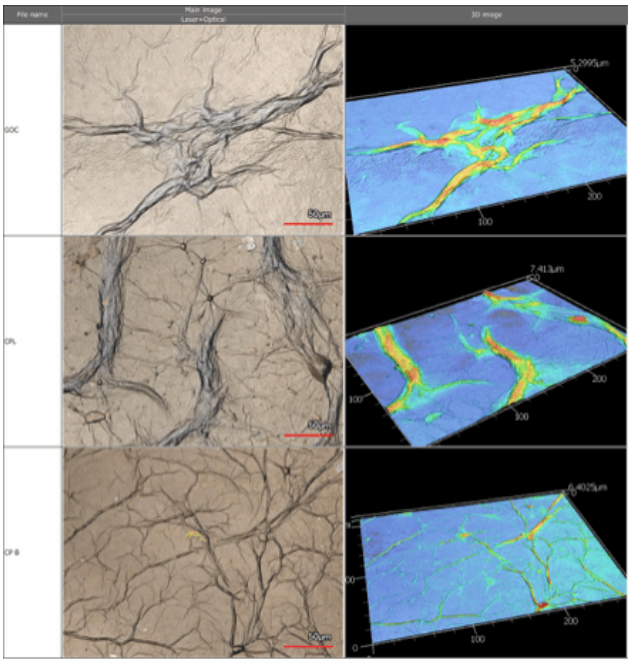

Figure 21. Images of hotplate dried samples using a VKX250 Laser Confocal microscope provided by Keyence. Three-dimensional imaging allows terrain topography measurements. The GOC sample corresponds to the GO sample using Graphenea GO. CPL sample corresponds to the GO sample produced using the GO solution produce by Cal Poly with a weight percentage of 0.34%. CPB sample corresponds to GO sample utilizing the GO solution produce by Cal Poly with a weight percentage of >0.4%.

Table 7. Measurements of GO cluster heights using the 3D imaging capabilities of a VKX250 Laser Confocal microscope provided by Keyence.

Sample	Height of GO Clusters [μm]
GOC	5.299
GPL	7.413
CPB	6.402

The GO characterization provides initial information about material properties of the solution. The quality of the solution ultimately determines the quality of the devices. Information about the particle size can illuminate how the GO solution will dry and the viable processes for deposition and patterning. An exact particle size characterization remains illusive because the SEM could not produce images of high enough resolution to depict a single GO particle. The information provided by Graphenea, and experimentally observing the Dimatix printer cartridges clogging, confirms the particle size exceeds 0.5 μm. Producing better particle size characterization remains a goal for future work on this project. Providing the right substrate for deposition represents another facet of this project that determines the quality of the devices. Creating bottom gates represents the first processing step to begin producing the substrate. The next section delves into the fabrication process of the bottom gates.

3.4 STAGE 1 BOTTOM GATES

The ability to control current through a transistor revolves around electrostatic gating of the device [31, 35]; gating modulates the current flow through the device by regulating the carriers in the material [31, 35]. Several application including sensors and antennas require bottom gate topography. Doping silicon produces the gates in the devices. An oxide layer acts as a diffusion mask to selectively dope the silicon substrate. Four-point probe measurements produce a base line sheet resistance of the wafers. Scribing numbers on the back of the wafers distinguishes wafers. B scribing symbolizes boron-doped substrates; P scribing symbolizes phosphorus-doped substrates. The wafers from University Wafers already contain a nominal oxide layer of 1 μm. Only a couple of the University Wafers experiences four-point probe measurements. Table 8 documents the four-point probe measurements. Equation (7) calculates the sheet resistance where V represents the voltage, and I represents the current. Multiplying the sheet resistance by the thickness of the wafer calculates the resistivity.

$$R_S = 4.53\left(\frac{V}{I}\right) \tag{7}$$

Table 8. Measured voltage during four point probe measurements and calculated sheet resistance using Equation (3).

Wafer	Voltage TL [mV]	Voltage C [mV]	Voltage BR [mV]	Average Voltage [mV]	Current [mA]	Sheet Resistance [Ω/sq]	Resistivity [Ωcm]
B1	813	838	814	822	10	373	19
B2	875	804	875	851	10	387	19
B3	1059	1010	1029	1033	10	469	23
B4	953	823	887	888	10	403	20
B5	822	862	897	860	10	391	20
B6	906	949	956	937	10	425	21
B7	844	836	843	841	10	382	19
B8	912	869	949	910	10	413	21
B9	813	847	825	828	10	376	19
B10	964	1139	946	1016	10	461	23
B11	741	756	751	749	10	340	17
B12	744	737	756	746	10	339	17
P1	327	308	321	319	10	145	7
P2	178	167	180	175	10	79	4
P3	315	292	309	305	10	139	7
P4	306	266	313	295	10	134	7
P5	213	176	221	203	10	92	5
P6	341	320	334	332	10	151	8

The wafers undergo a cleaning process before growing the oxide layer. The cleaning process ensures no contamination occurs while growing the oxide layer. The oxidation furnace reaches 900 °C before loading the wafers. Wafer position affects the oxidation growth rate because of thermal inconsistencies in the furnace. The wafers follow the order of P1-P12, B1-B11 with B11 closest to the gas intake. The gas intake cools the wafer closest and reduces the oxidation rate. Nitrogen gas flows at 6 Lpm, ensuring oxidation does not occur while the furnace ramps to 1100 °C. Wet oxygen gas (water vapor) produces a fast oxide growth rate [17, 34]. Initiating the water heating flask occurs when the furnace reaches 1000 °C. The water began to

boil when the furnace temperature reached 1037 °C. The nitrogen air ceases and the wet oxygen persists for 85 minutes. The Deal-Grove model in Figure 22 determines the oxygen duration.

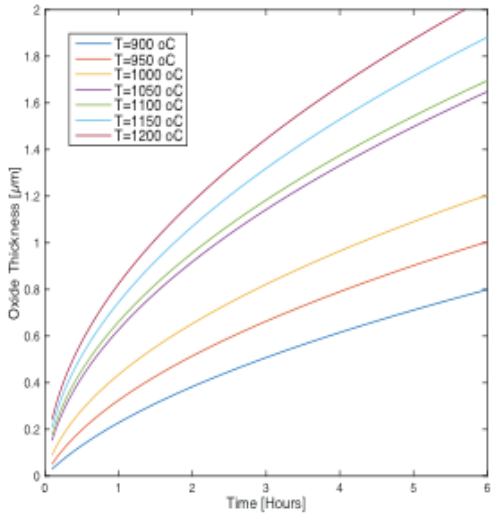

Figure 22. Deal-Grove model used to calculate oxidation time for several temperatures.

An 85 minute oxidation duration at 1100 °C theoretically produces an oxide around 750 nm. After 85 minutes, the furnace transitions into ramp down, power to the water heating flask ceases, and nitrogen gas initiates for 20 minutes at 6 Lpm to end oxidation reactions. The FilmMetrics F20 spectral reflectometer measures the resulting oxide thickness. Table 9 displays the results.

Table 9. Thickness of the diffusion mask oxide layer. Feature size designates the photolithography mask to transfer gate patterns. The oxide thickness of wafers P7-P12 exceeds the other wafers because University Wafers grew the oxide layer.

Wafer	Top Left 1[nm]	Center [nm]	Bottom Right [nm]	Feature Size Designation
P1	622	613	618	Large Features
P2	664	651	653	
P3	676	657	659	
P4	683	669	672	
P5	692	673	680	
P6	690	680	680	
B1	757	750	751	
B2	756	748	748	
B3	750	739	742	
B4	744	732	733	
B5	738	727	736	
B6	728	716	726	Small Features
B7	717	697	707	
B8	699	676	687	
B9	676	635	655	
B10	644	582	616	
B11	593	539	543	
P7	1026	1028	1028	
P8	1029	1026	1023	
P9	1028	1027	1028	
P10	1027	1028	1025	
P11	1031	1028	1028	
P12	1036	1032	1031	

Cleaning and photolithography processing transfers the gate patterns into a PR layer that serves the purpose of an etch mask to create the vias for dopant atoms to contact the silicon substrate. Using the BOE etch rate of 110 nm per minutes and oxide measurements in Table 9, Equation (8) calculates the required etch time.

$$T_{etch} = \frac{Oxide\ Thickness}{Etch\ Rate} \tag{8}$$

Wafers P1-P6 and B1-B11 etch in BOE for 7 minutes. Wafers P7-P12 etch in BOE for 10 minutes. Figure 23 displays a resulting wafer after oxide etching.

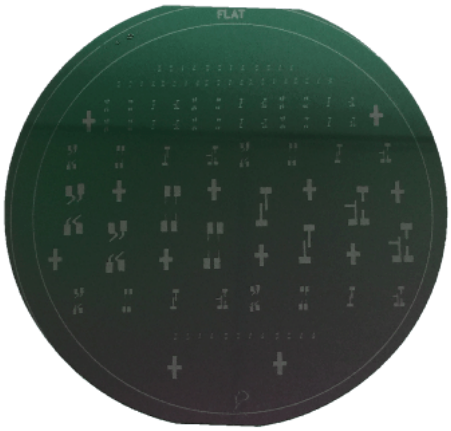

Figure 23. Resulting small feature gate patterns after etching of the oxide diffusion mask.

The spin coater evenly distributes the dopant atoms onto the wafers. Figure 24 displays the overall processing steps necessary to produce the silicon gates after the creating the silicon oxide diffusion mask. Both boron and phosphorus dopants use the same spin recipe that Table 10 displays. Deposit 4.5 mL of dopant onto the wafers. Only 5 P-type wafers receive boron dopant because the boron dopant supply ran out. Wafers P1, P2, P8, P9, and P12 receive boron dopant because oxide etching of these wafers produces the best gate patterns.

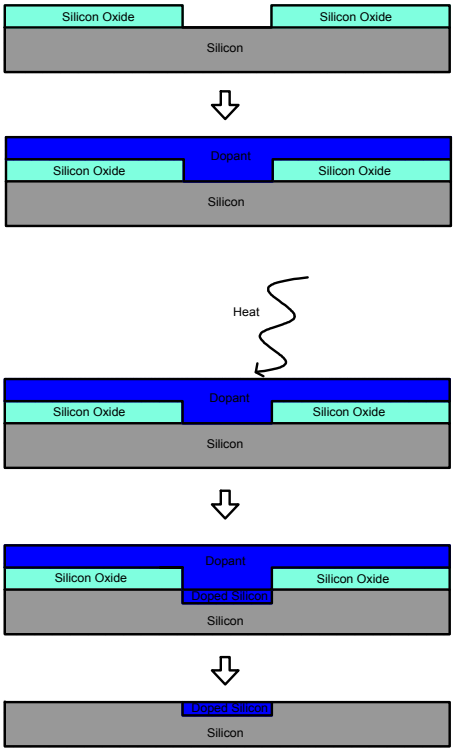

Figure 24. Processing steps that create the silicon gates.

Table 10. Spin program for spreading dopant atoms.

Function	Time [s]	Spin Speed [rpm]
Spread dopant	20	200
Spread dopant	10	500
Final Spin Planarization A	10	2000
Final Spin Planarization B	20	3000
Slow and Stop	5	300

After dopant deposition, the wafers bake on a 200 °C hotplate for 5 minutes and then chill on an aluminum heat sink for 1 minute to cool. Diffusion requires two separate furnace-processing runs to avoid contamination between phosphorus and boron dopants. The diffusion furnace processing remains the same for both dopant types. The furnace reaches 900 °C before inserting the wafers. Nitrogen gas initiates before wafer insertion. Nitrogen gas flow continues until the furnace reaches 1025 °C; oxygen flow then begins and persists for two hours. The

furnace continues to increase temperature to the set point of 1100 °C. After apply oxygen for two-hours, the furnace enters ramp down and nitrogen gas initiates for 20 minutes while the furnace begins to cool.

The high temperature necessary for diffusion changes the dopant material layer into a glass layer. Figure 25 displays resulting gate features before dopant glass etching. The FilmMetrics metrology tool measures the resulting glass layer thickness to determine BOE etch times. Table 11 documents boron glass thickness. Table 12 documents phosphorus glass thickness. BOE etches boron glass at 30 nm per minute and phosphorus glass at 20 nm per minute. Equation (8) calculates the required etch times of 36 minutes for boron glass and 44 minutes for phosphorus glass.

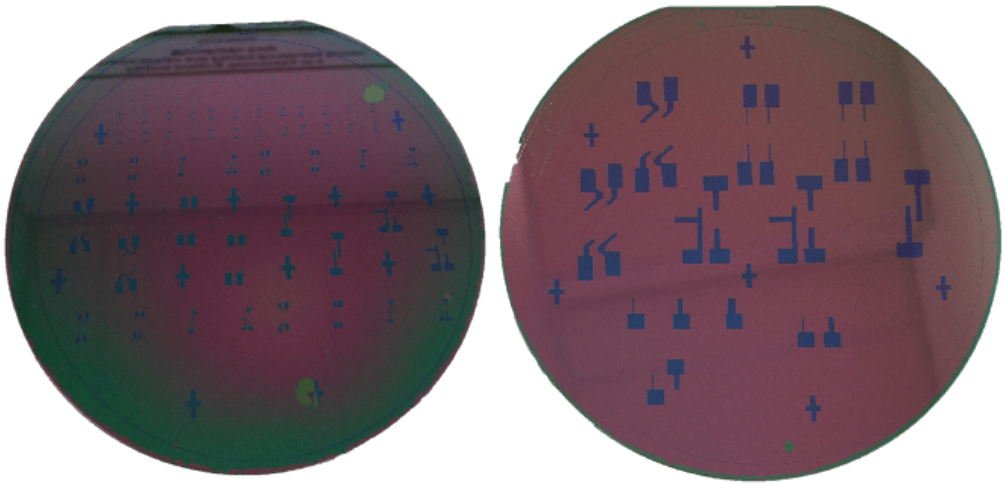

Figure 25. Wafers containing a boron glass layer after diffusion of boron into the wafer. Left displays the small feature pattern and right displays the large feature pattern.

Table 11. Boron glass thickness.

Wafer	Top Left [nm]	Center [nm]	Bottom Right [nm]
P12	1065	1051	1057
P8	1033	1038	1041
P1	657	652	668
P2	688	678	686
P9	1046	1042	1040

Table 12. Phosphorus glass thickness.

Wafer	Top Left [nm]	Center [nm]	Bottom Right [nm]
B6	836	833	833
B11	716	680	662
B10	790	756	777
B9	818	787	796
B3	848	847	834
B4	849	850	836
B1	866	861	855
B2	858	862	845
B7	836	824	830
B8	803	789	807

After the gate creation, an additional oxide layer serves as the dielectric layer insulating the gates from the GO. Silicon dioxide grown in a similar fashion to the diffusion mask produces this material layer. Silicon dioxide's high dielectric strength of 10^7 V/cm allows silicon dioxide to remain stable under high electric fields [36], making it an optimal electrical insulating layer. The subsequent section describes the thermal growth of silicon dioxide for the gate oxide layer.

3.5 STAGE 2 GATE OXIDE

Thermal growth of silicon dioxide represents an important processing step in the semiconductor industry [36]. Because silicon dioxide grows above the silicon substrate resulting from chemical reactions, very few mechanical and electrical defects form at the interface between the silicon and silicon dioxide [36]. Gate oxide growth differs from diffusion mask growth to improve the quality of oxide layer. Gate oxide growth uses dry oxygen gas instead of water vapor. Dry gas grows oxides containing higher atomic density that produces fewer impurities than wet oxidation [36]. Higher temperature growth also improves the quality of the oxide [34]. Dry oxidation reduces the growth rate allowing greater control of the film thickness.

The gate oxide provides a dielectric layer to insulate the gates from the graphene layer. Varying oxide layers thickness allows the study of the interplay between gating voltage and oxide thickness as Chapter 2 discusses. The minimum detectable film layer of 43 nm sets the minimum limit for the oxide layer thickness. The furnace reaches 900 °C before wafer insertion. The wafer position determines the oxidation rate because of thermal fluctuation in the furnace. The wafer position follows the order B11, B8, B7, B9, B6, B10, B2, P9, P2, P1, P8, P12, B1, B4, and B3 with B3 closest to the oxygen intake. Initiating nitrogen before wafer insertion prevents oxidation before reaching the desired furnace temperature.

Before oxygen initiation, nitrogen discontinues for 18 minutes. Failure to open the oxygen valve prevents oxygen application during the first attempt. The second attempt began once the furnace reaches 1078 °C by initiating dry oxygen gas for a second time. Oxygen flow persists for 18 minutes; the furnace reaches 1097 °C by the end of the oxygen flow. The furnace transitions into ramp down and initiating nitrogen gas ends the oxidation process. The wafers cool in the furnace over night.

The Deal-Grove model doesn't accurately describe thin film oxide growth as Hans Mayer and Dr. Savage explain. The 18-minute duration selection came from processing procedures that BMED 435 implements to produce 60 nm gate oxide films. The FilmMetrics F20 metrology tool measures the resulting oxide thicknesses; Table 13 displays the measurements.

Table 13. Gate oxide thickness measurements.

Wafer	Top Left [nm]	Center [nm]	Bottom Right [nm]
B11	170	173	168
B8	174	177	172
B7	175	175	175
B9	179	176	179
B6	182	195	179
B10	182	180	184
B2	182	180	201
B1	157	170	169
B4	155	136	158
B3	157	119	123
P8	140	131	132
P12	129	124	126
P9	147	145	156
P2	151	143	157
P1	140	136	141

The oxide thicknesses greatly exceed the target value. The duration between nitrogen discontinuation and oxygen initiation effectively extends the oxidation time to 36 minutes. The 36-minute duration underestimates the actual oxidation time, because programing the gas controller adds additional time to the set processing time. The P-type wafers oxidize at a faster rate than the N-type wafers. The wafers etch in BOE for 47 seconds to reduce the gate oxide. Table 14 displays the resulting gate oxide thicknesses.

Table 14. Final gate oxide thickness for devices. The resolution of the FilmMetrics F20 metrology tool limits the detectable film to 43 nm.

Wafer	Top Left [nm]	Center [nm]	Bottom Right [nm]
B3	< 43	< 43	< 43
B4	< 43	< 43	< 43
B1	54	< 43	52
B12	50	< 43	52
B8	58	49	53
P1	61	54	58
P2	61	58	56
P9	65	60	60
B2	72	68	68
B10	73	67	65
B6	71	60	66
P9	70	63	78
B7	74	60	61
P8	64	51	61
B11	60	53	55

Cleaning and lithography processing produce vias for contacting the gates. Figure 26 displays a wafer containing gate oxide and vias, providing contact points to the gates. Figure 27 displays a side view of the resulting device that distinguishes material layers.

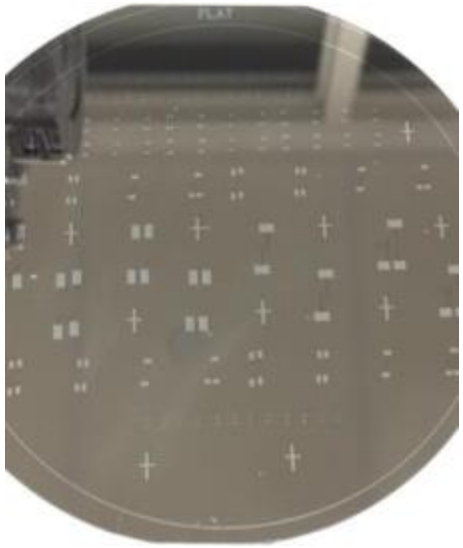

Figure 26. Device wafer after growing the gate oxide layer and patterning it with gate contact vias.

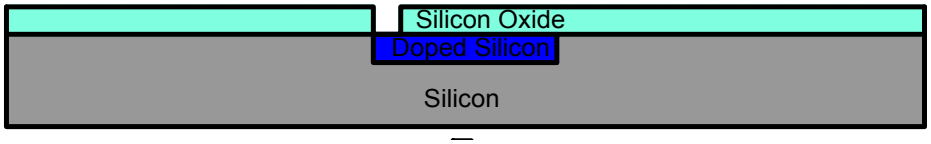

Figure 27. A side profile view of the resulting device after gate oxide growth and via etching.

The wafers await GO deposition to create the active layer. Before GO deposition, microfluidic channel creation occurs. PDMS Microfluidic channels deposit and pattern the GO solution on the wafers. Microfluidic channel creation takes several processing steps; the next section documents the processing steps that produce microfluidic channels.

3.6 STAGE 3 MICROFLUIDIC CHANNEL CREATION

The fabrication processing requires GO deposition to occur last out of all the processing steps to limit opportunities to damage the GO layer. The previous sections document the substrate preparation for GO deposition. Custom made microfluidic channels produce the deposition and patterning method. Hans Mayer explains that the micro-pores of PDMS allow microfluidic channels to self-fill after subjection to vacuum environments. PDMS consists of two liquid parts that combine to produce the desired material. After combining the two parts, the PDMS remains in a liquid form until thermal curing. Custom microfluidic channels necessitate a mold to pattern the PDMS. A photosensitive epoxy permits similar photolithography processes, described previously, to produce the PDMS mold. Figure 28 displays the processing steps to produce the PDMS mold and microfluidic channels.

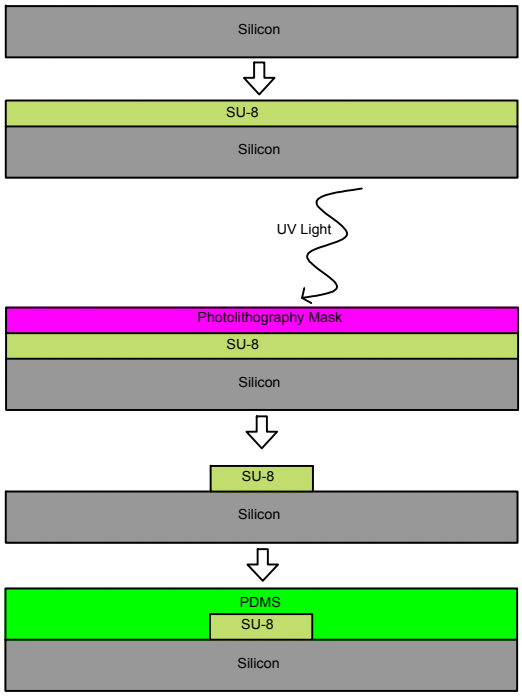

Figure 28. Processing steps to construct the PDMS mold out of SU-8 and constructing PDMS microfluidic channels.

A bare silicon wafer substrate allows SU-8, a photosensitive epoxy, patterning that creates the physical features in the microfluidic channels. The wafer experiences a cleaning cycle before SU-8 deposition. Spin coating the SU-8 produces a uniform surface, ensuring consistent microfluidic channel height. Channel height plays a critical roll in deposition. The first channels use SU-8 2007 that produces channel heights around 7 μm. The channels collapse during GO deposition. The second channel iteration uses SU-8 2050, allowing channel height exceeding 50 μm. Previous SU-8 characterization experiments determines the necessary spin speed to achieve desired channel height. Figure 29 displays a plot relating spin speed to SU-8 film thickness; 30 seconds at 3000 rpm produces the SU-8 layer. Table 15 documents the entire spin recipe.

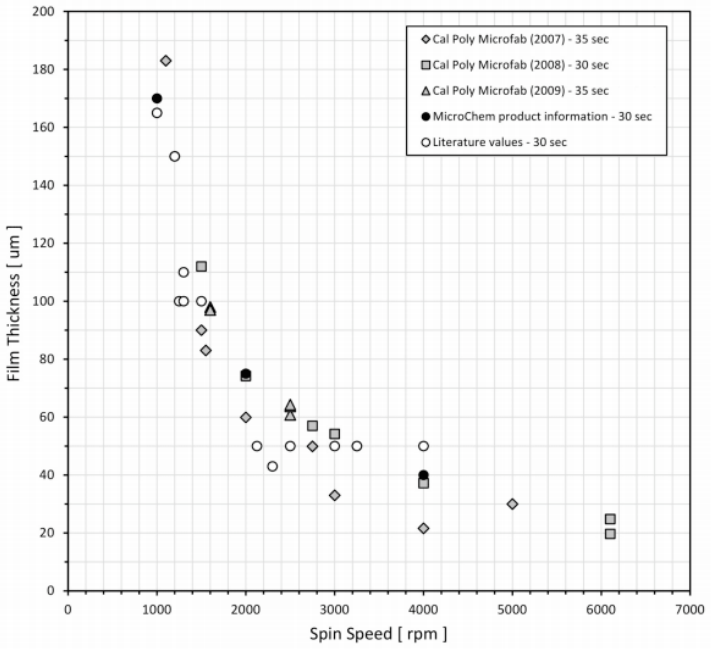

Figure 29. Previous Cal Poly SU-8 experimental data characterizing the obtained film thickness relative to spin speed [37].

Table 15. Spin recipe for SU-8.

Function	Duration [s]	Speed [rpm]
Dispense 80/20 Primer	30	300
Planarize 80/20 Primer	20	3000
Press Stop	Pour SU-8	0
Dispense SU-8	20	400
Planarize SU-8	30	3000
Slow and Stop	5	300

After SU-8 deposition, the wafers bake on a hot plate at 65 °C for 6 minutes. The wafer experiences a second baking at 95 °C for 9 minutes. Rotating the wafers every couple minutes during the soft bakes ensures uniform thickness [37]. A 150 mJ/cm^2 dose of UV light determines the necessary UV exposure time to cross link the SU-8 [37]. The SU-8 requires 365 nm light to cross-link [37]. An optical filter restricts the wavelength of light to the range of 320 nm-475 nm, ensuring only wavelengths near 365 nm transmits to the SU-8 [37]. Figure 30 helps calculate the UV light intensity that affects the SU-8.

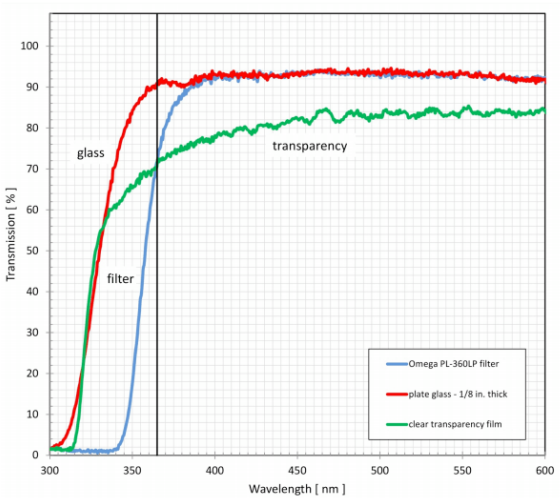

Figure 30. Transparency percent of the filter, transparency mask, and glass blank material layers that lie above the SU-8 during photolithography [37].

From Figure 30, 44.1% of the aligner light intensity reaches the SU-8. A 20% over exposure correction factor ensure the SU-8 properly cross-links. The correct factor arose from a 10 % correction recommend by the Cal Poly Microfluidics Process Traveler and a 10 % correction to account for an alternate transparency than what Figure 30 documents. Cal Poly photolithography mask transparency remains unknown. Equation (9) calculates the exposure time.

$$T_{exposure} = \frac{Required\ Dose}{UV\ Light\ Intensity} * Correction\ Factor \tag{9}$$

$$T_{exposure} = \frac{150\ mJ/cm^2}{14.8\ mW/cm^2(0.441)} * 1.2$$

$$T_{exposure} \approx 28s$$

After exposure, the wafer bakes at 65 °C for 2 minutes and then at 95 °C for 7 minutes. The wafer position rotates every couple minutes to promote uniform thickness. SU-8 developer removes excess SU-8. Submerging the wafers for 7 minutes in the SU-8 developer at room temperature removes the SU-8. The wafer hard bakes for 15 minutes at 150 °C post development to fully cure the SU-8 mold. The photolithography mask limits the success of mold creation. Poor printing of the one-sixteenth and one-eighth scale fractals prohibits successful patterning in SU-8. Figure 31 displays resulting SU-8 molds of the one-fourth, one-eighth, and one-sixteenth scale. Profilometer scans measure the SU-8 film thickness. Table 16 documents the results.

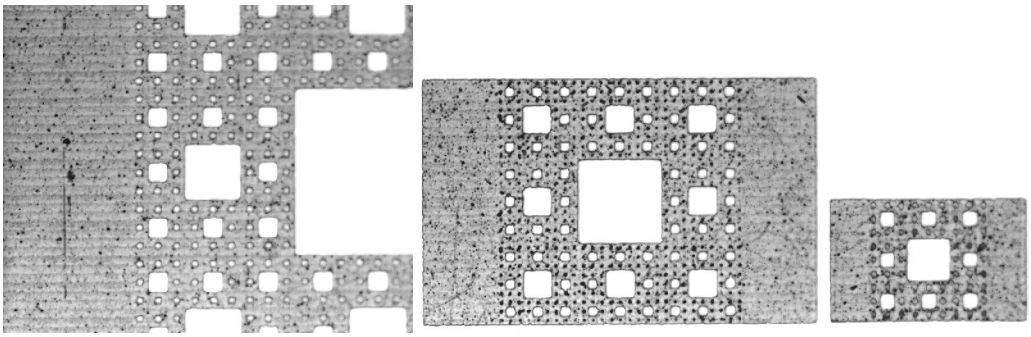

Figure 31. SU-8 mold patterning. Left displays the one-fourth scaling, center displays the one-eighth scaling, and right displays one-sixteenth scaling. The photolithography mask produces the horizontal defects seen. The center squares in each scaling contains an edge length of 83.33 μm, 41.66 μm, and 20.83 μm.

Table 16. Profilometer measurements for SU-8 PDMS mold. The data shows the center containing less SU-8 than the edge of the wafer. The measurements pertain to the small feature fractal mold.

Wafer Position	SU-8 Thickness [μm]
Top Right	60.2
Middle Right-Center	52.5
Middle Left-Center	52.4
Bottom Left	61.1

Now that a mold exists, the channel creation commences. PDMS consists of a 10:1 ratio of base and a curing agent to produce the material. Volumetric calculations determine the necessary amount of both parts. The petri dishes contain a diameter of 107.95 mm. Total PDMS thickness equates to 3 mm. Equation (10) calculates the necessary PDMS volume,

$$V = \frac{\pi D^2 t}{4} \tag{10}$$

$$V = \frac{\pi(0.10795)^2 0.003}{4}$$

$$V = 27.46\, mL,$$

where D represents the petri dish diameter and t represents desired PDMS thickness. Multiplying the resulting volume by the ratio 10:11 calculates the base volume, equating to ~25 mL. Multiplying the resulting volume by the ratio 1:11 calculates the cure volume, equating to ~2.5 mL. Mixing the PDMS parts creates many air pockets within the PDMS solution. The air pockets produce defects in the PDMS channels, subjecting the PDMS solution to vacuum pressures removes the air pockets. A minimum duration of 20 minutes at a vacuum pressure of 90 kPa removes air pockets. The vacuum time changes depending on the number of air pockets created during mixing.

A petri dish houses the SU-8 mold wafer to contain the SU-8 solution once poured over the SU-8 mold. The PDMS requires curing at 60 °C-70 °C for 80 minutes to solidify. Figure 32 displays the wafer after PDMS curing.

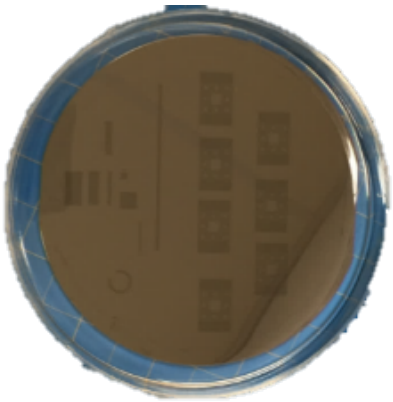

Figure 32. PDMS post curing on top of the SU-8 wafer mold. PDMS exhibits transparent characteristics allowing visual recognition of the SU-8 mold below.

Once cured, channel preparation concludes by cutting the individual channel out of the PDMS mold and puncturing GO intake points over the electrode region of the fractal. The self-filling potential of PDMS creates the mechanism that dispenses the GO solution through out the channels. This allows small features sizes. Several preparation steps ensure good adhesion and feature creation of the GO layer. The subsequent section describes these preparations and the process for GO deposition.

3.7 STAGE 4 GO DEPOSITION

The preceding sections describe preparing the substrate and microfluidic channels to climax at GO deposition. Further preparation of the substrate and the microfluidic channels ensure good adhesion and patterning of the GO solution. Hans Mayer and Dr. Zhang explain that plasma treating the substrate cleaves the top layer of bonds that produces a hydrophilic surface. Subjecting the channels to vacuum pressure elicits the self-filling response. The high solubility of air in a vacuum diminishes the air content in the PDMS micro-fluidic channels, creating a pressure gradient at the boundary of the PDMS once returned to atmospheric pressure [31, 35].

Testing the self-filling behavior of PDMS using food coloring to confirm this material characteristic. Subjecting the channels to 60 minutes at 90 kPa-v pressure allows the microfluidic channel to fill in 25 minutes. Figure 33 displays the resulting microfluidic channel.

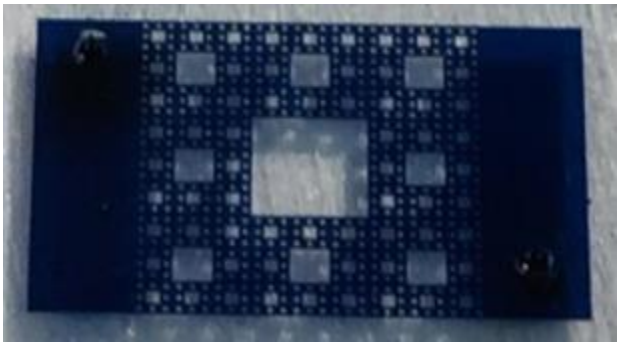

Figure 33. PDMS successfully self-filling with food dye to produce the fractal pattern.

Plasma treating effects deteriorate with time, reducing the GO patterning time produces superior adhesion to the substrate. The PDMS channels experience 120 minutes at 90 kPa before introducing to atmospheric pressure. The plasma treater limits the sample size; wafers broken into

smaller pieces permit insertion into the plasma treater. A scribe tool breaks the wafers using mechanical pressure. The wafers experience one minute of high RF field plasma treatment. Immediately after plasma treatment, applying PDMS channels creates the framework for the GO solution to flow through. Applying GO solution at the channel intakes begins the patterning process. Figure 34 displays the plasma treatment processing and GO deposition.

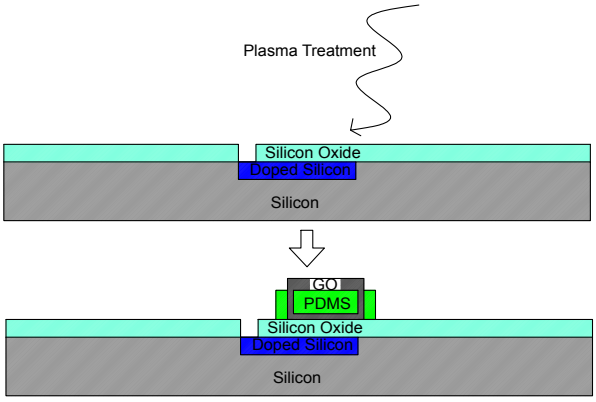

Figure 34. Plasma treatment processing and GO deposition using PDMS microfluidic channels.

Applying the PDMS channels to all the devices requires roughly 10-15 minutes per wafer. Wafers P2, P8, B4, B7, and B9 all experience vacuum oven drying as Chapter 1 describes. To limit necessary PDMS channel production, the vacuum drying samples complete processing before GO deposition on the air-drying wafers. Figure 35 displays wafer P8 before vacuum oven drying.

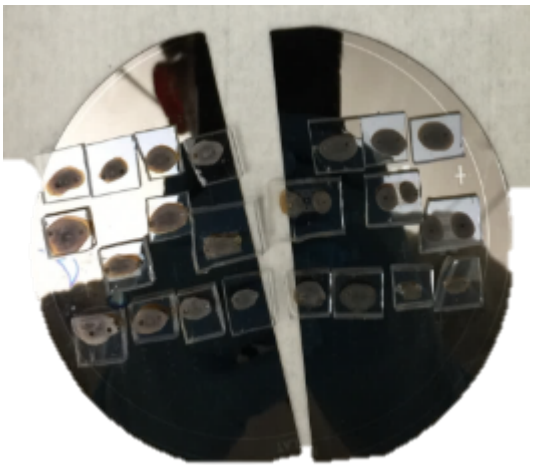

Figure 35. Wafer P8 before experiencing vacuum oven drying.

Wafers P1, P9, B1, B10, and B11 experience 48 hours of air-drying before removing the PDMS stamps. Wafers P8, P9, B1, and B4 both contain pure Graphenea GO solution; wafers P1, P2, P7 and B10 contain a 1:1 ratio of DI water to Graphenea GO solution; wafer B9 and B11 contain Cal Poly GO solution. Figure 36 displays the resulting fractal pattern after removing the PDMS stamps.

Figure 36. Fractal patterns after GO deposition and PDMS stamp removal.

As time elapses after PDMS stamp removal, it became harder to distinguish where GO deposition took place. The darker regions in Figure 36, representing areas touching PDMS, began to fade. Figure 37 shows a close up of successful and unsuccessful GO patterning using the vacuum drying method.

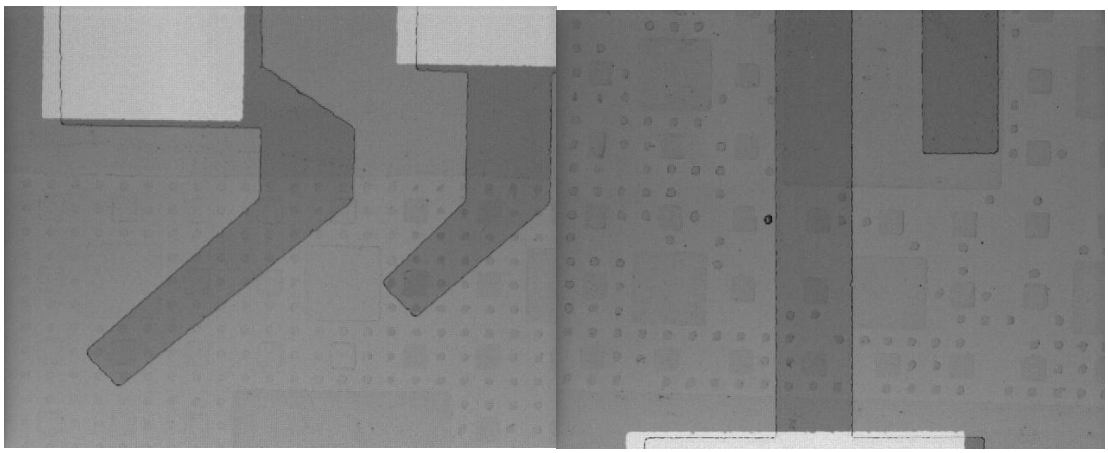

Figure 37. Left shows successful GO deposition of a single fractal pattern on wafer P8. Right shows an unsuccessful GO deposition of a single fractal also on wafer P8.

Unsuccessful patterning most commonly arose from poor contact between the PDMS stamp and the silicon substrate. The posts of the stamp route the GO solution. Air-drying fractals produces more defects than the vacuum drying samples. This arose from reusing PDMS stamps. Touching the channels can damage the channels and cleaning requires touching the channels. Cleaning consists of soaking the stamps in IPA (Isopropyl Alcohol) and rubbing with a chem wipe—very smooth paper towel. Figure 38 displays resulting air-drying GO fractals.

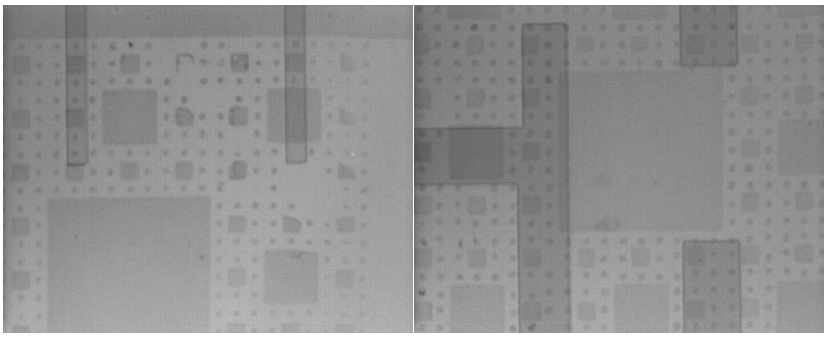

Figure 38. Air-drying fractal pattern resulting in unsuccessful fractals (left) and successful fractals (right).

The final processing step for the GO consists of thermal reduction. Thermal reduction chemically changes the GO, removing the oxygen functional groups leaving a carbon lattice behind [3, 6, 8]. Removing the oxygen greatly increases the electrical and thermal conductivity of the GO material layer [25]. Functionalized GO doesn't provide usable functionality besides that of an insulating layer as Dr. Kaner at UCLA uses it as the dielectric layer between their capacitor electrodes. The following section describes the reduction procedure.

3.8 STAGE 5 GO Reduction Process

The reduction procedure represents an important processing step. The reduction process transforms the GO solution into rGO (reduced graphene oxide), which greatly enhances the material properties [25]. This report uses a reduction process Graphenea provides in their documentation [25].

Loading the wafers into individual petri dishes helps maintain the cleanliness of the devices and prevents damage to the devices during transport between Cal Poly and Strasbaugh. Bill Kalenian at Strasbaugh permits the use of their furnace for reduction. Partitioning the wafers for GO deposition also separates the wafers into one half that experiences reduction and one half that does not experience reduction, providing a means to test before and after reduction material characteristics. Two separate reduction processes consisting of vacuum drying and air-drying wafers. Two separate reduction processes determines repeatability of the process.

A low profile quartz boat houses the wafers during reduction processing. Including test wafers in the air-drying wafer reduction processing produces wafers that experience all the furnace processing steps through the entire fabrication process. The test wafers accurately represent the drive in of dopant atoms and can be used to determine the conductivity of the bottom gates. Unfortunately, the probe tips of the four-point probe became damaged, producing inaccurate results. Nitrogen gas flows at 1 SCFM before heating initiates the reduction processing. The inert environment limits potential burning (oxidation) of the devices at high temperatures. The furnace increases the internal temperature at 10 °C per minute until reaching 1000 °C. The furnace dwells at 1000 °C for 60 minutes before heating discontinues. The wafers remain in the furnace over night to cool with continuing nitrogen gas flow. Dwelling at 1000 °C for 60 minutes should produce GO films of 95% carbon purity [25].

Upon analyzing the resulting GO fractals post reduction, several fractals disappeared. The nitrogen flow did not purge the chamber of oxygen gas. The oxygen gas causes the GO fractals to burn off. GO reduction also produces oxygen gas content responsible for burning the GO fractals. GO reduction necessitates greater nitrogen volumetric flow. Wafer P8, B7, B8, and B9 contained no fractals capable of testing. Dr. Zhang suggests purging the furnace with 30 SCFM initially of the reduction process and then decreasing the flow to 10-20 SCFM for the duration of the reduction process. Figure 39 displays a burn location on wafer P8. Not all fractal locations exhibit the burning signs.

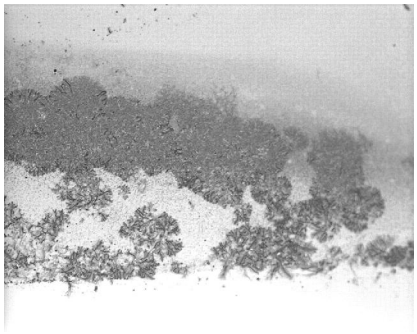

Figure 39. The dark region displays a GO burn location on wafer P8.

Both the air-drying and vacuum-drying samples produce successful GO reduction. Figure 40 displays images of rGO fractals. The air-drying fractal produces a greater number of rGO fractals. Figure 41 displays a side profile view of the resulting device.

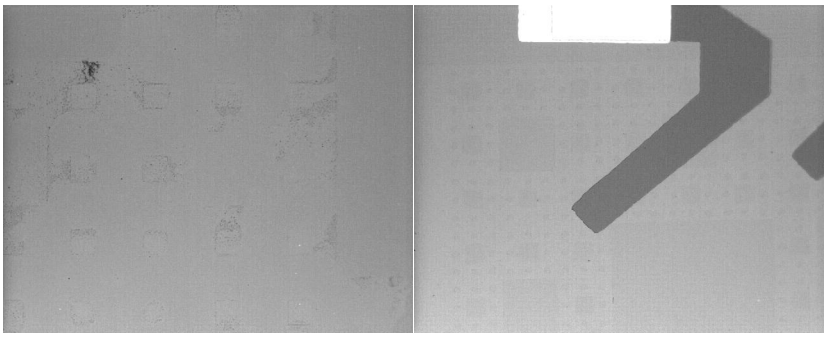

Figure 40. Left displays a vacuum dried fractal post reduction on wafer P2; it displays signs of defects between features most likely caused by burning effects. Right displays a successful reduction of one air-dried fractal on wafer B11.

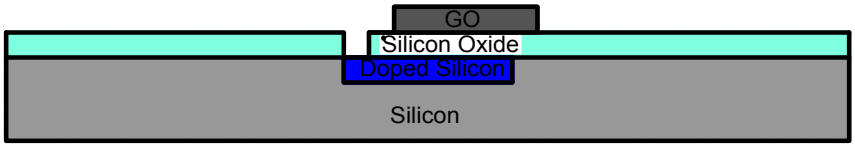

Figure 41. Side profile view of the device after GO deposition.

Testing the devices requires careful contact with the rGO fractals. Probe tips provide the potential to puncture and destroy the rGO films. Silver epoxy solves the issue of making contact. The epoxy base binds the silver particles to the rGO film, producing a robust mechanical and electrical contact. The next section describes silver contact application.

3.9 STAGE 6 SILVER CONTACTS

One of the greatest challenges of the project revolves around making contact to the rGO films. The preceding sections discuss the fabrication methods for the devices but exclude discussion on contacting the rGO sheets. Metallic contacts prevent damaging the rGO thin films during testing. Conductive epoxy solves the adhesion issue of making metallic contacts. The epoxy base binds the silver particles to the rGO films to create a mechanically robust electrical contact.

The silver epoxy consists of two parts mixed together that results in a 4 hour curing time. Mix equal parts together and apply to the rGO electrodes. A luer cap provides the means to glob epoxy onto the electrodes. This produces inconsistent epoxy amounts. This stage requires future improvements to quantify the silver epoxy deposited. Figure 42 displays the side profile of the final device.

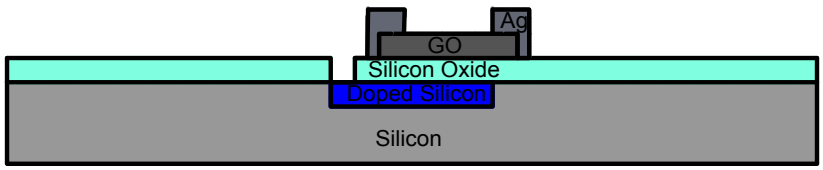

Figure 42. Side profile view of the final device.

This concludes the entire fabrication procedure. Testing the electrical characteristics teases out issues in the fabrication process. Creating good electrical contact to the devices persists as the most difficult facet of testing and prevents full characterizations of the devices. Several opportunities for error arise during the fabrication process that could result in the device failure. Chapter 4 discusses device testing and sources of error.

4. DEVICE ANALYSIS

The previous chapter encompasses device fabrication. Characterization testing of the devices confirms which processes produces functioning components of the device. First, theoretical calculations provide expectations for resistance values of the fractal devices and graphene sheet thickness. Experimental testing then measures actual characteristics of the devices. Testing consists of several intermediate tests to isolate specific parts of the device: gate contacts, gate diode characteristics and output characteristics. The gate voltage should produces electrostatic gating that modulates the current in the devices. This testing serves the purpose to validate fabrication processes for revisions during the next prototypes.

4.1 GRAPHENE SHEET CHARACTERIZATION

Theoretical calculations provide an estimate for the expectations of experimental results; however, these calculations only provide rough estimates for the Graphenea rGO fractals. Graphenea provides information about the sheet resistance of their non-reduced GO equating to 0.514 MΩ/sq and 2.13 Ω/sq for their rGO [25]. Graphenea's analysis produces sheet resistance values that pertain to a GO film thickness of 40 μm [25]. Graphenea uses van der Pauw technique to acquire sheet resistance measurements. By partitioning the fractal into individual "resistors", the equivalent resistance results. The fractal breaks down into groupings consisting of the blue highlight square in Figure 43.

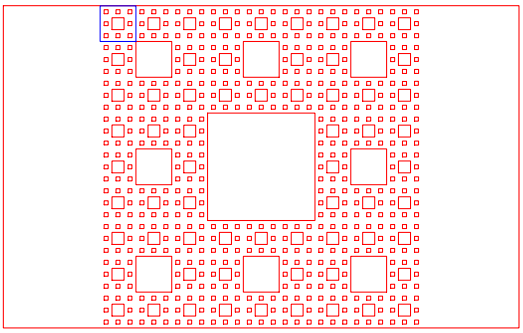

Figure 43. The blue square highlights the repeated pattern that comprises the entire device. The individual red squares that comprise the fractal represent the PDMS posts that prevent GO deposition.

The blue square breaks down even further by partitioning the blue square into groups of the smallest square, containing a feature size of 123 μm x 123 μm. The blue square contains the sequence groups of 9, 6, 9, 6, 4, 6, 9, 6, 9 small squares moving across the blue square left to right. Calculating the resistance of each collection of small squares and summing them results in

the resistance of the blue square. The blue square denoted in Figure 43 contains a theoretical resistance value equaling 32.9 MΩ/blueSQ for non-reduced GO and 136.32 Ω/blueSQ for rGO (reduced GO). Horizontally aligned blue squares represent series “resistor” connections and vertically aligned blue squares represent parallel “resistor” connections.

Nine blue squares connect the source and drain terminals. If each column containing these squares represents a separate resistor, the fractal network consists of nine resistors that alternate between four different component values. Figure 44 displays the nine columns denoting individual components where the square color distinguishes between column resistance values. Table 17 documents the total resistance of the fractal.

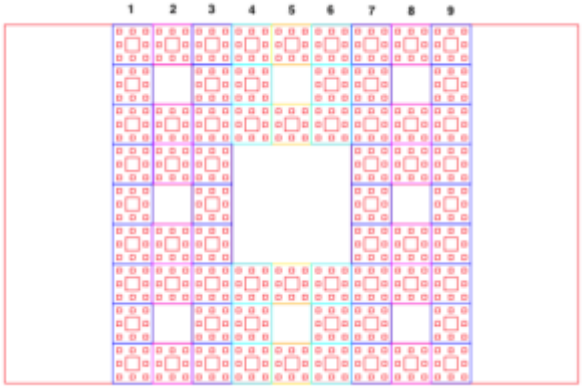

Figure 44. Partitions the fractal into nine columns denoting different “components” containing various resistances values. The squares grouped vertically with the same color represent one component. Color distinguishes component value.

Table 17. Number of blue squares pertaining to the nine columns in Figure 44 and the calculated resistance value. Although columns 2, 4, 6, and 8 all contain the same number of squares, the configuration differs and thus the purple and light blue color distinction between columns 2, 8 and columns 4, 6.

Column	Number of Blue Squares	GO Resistance [MΩ]	rGO Resistance [Ω]
1, 3, 7, 9	9	3.66	15.14
2, 8	6	5.48	22.72
4, 6	6	5.48	22.72
5	4	8.22	34.08
Total Resistance		44.78	109.80

The thickness of the GO sheet determines the resistance. Calculating anticipated sheet thickness derived from solution dilution provides a means to compare the GO sheets produced by Graphenea and the sheets produced during these experiments. Calculating the volume of the 123 μm x 123 μm square used to calculate the blue squares resistance allows GO weight deposition calculations. Calculations use channel heights of 50 μm and 60 μm to account for the minimum and maximum channel heights. Equation (11) calculates the mass per square.

$$Mass = Solution\ Dilution * Square\ Volume \tag{11}$$

Using the SSA (Specific Surface Area) of graphene equaling 2.63E15 $\mu m^2/g$ allows calculations of mass per sheet of GO in the square [21]. Equation (12) displays the number of squares calculation.

$$Number\ of\ Squares = \frac{SSA}{A_{sq}} * Mass \tag{12}$$

Graphene consists of a monolayer sheet of atoms. When graphene stacks, it forms graphite [16]. By multiplying the number of squares by the layer spacing characteristic to graphite produces the thickness of graphene sheet. The layer spacing equals 0.341 nm [3]. Table 18 records the calculate values.

Table 18. Results from Equations (7) and (8) along with the final graphene film thickness.

Sample	Dilution [g/ml]	Channel Height [μm]	Mass [ng/sq]	# of Squares	Thickness [nm]
Graphenea	0.004	50	3.026	526	179.366
		60	3.631	631	215.171
Graphenea	0.002	50	1.513	263	89.683
		60	1.816	315	107.586
Cal Poly	59	50	44.631E3	7.759E3	2.640E6
		60	53.557E3	9.310E6	3.170E6

The fabrication process produces graphene sheets much thinner than the graphene sheets used to calculate the total resistance values in Table 17. Thus, the fractal devices should contain resistance values less than the values in Table 17.

The above calculations provide general guidelines for experimental expectations. The devices require extensive testing because of the multitude of unknowns. How the fractal geometry interacts with electrical conduction and the conduction of the GO sheets both necessitate experimental testing. The output characteristic data raises questions about the proper functionality of the components within the device. Individually testing the device components tease out the functionality of the device.

4.2 OUTPUT CHARACTERISTICS

The thesis focuses on developing the fabrication process, which necessitates device testing to ensure the fabrication process produces functioning device components. GO contains a band gap because of the functional groups attaching to the carbon rings. The GO devices should behave as typical semiconducting devices, where they exhibit a threshold voltage that allows them to turn on and off. Thermally reducing the GO removes the functional groups of the GO, which makes the rGO more conductive and should reduce the effects of gating. Calculations predict the threshold voltage equaling 35 V for the rGO devices.

Conducting drain to source current measurements provide a means to confirm a GO layer still exists on the device and that the devices conduct. Figure 50 shows that the drain to source current increases with drain to source voltage, confirming functioning devices. Applying gate voltage did not affect the current measurements by much and the devices behave as expected of a material with no band gap. Testing uses a Keithley 2401 SourceMeter that supplies the drain to source voltage while measuring the current through the devices. An Elenco XP752 DC power supply powers the gates. All grounds connect to the Keithley 2401 earth ground. Figure 45 displays a cartoon of the testing configuration. Figure 46 displays the actual testing set up in the lab that shows the connections made from the equipment to the probing station. Fractal orientation does not matter because of the symmetrically consistent rGO and GO sheets.

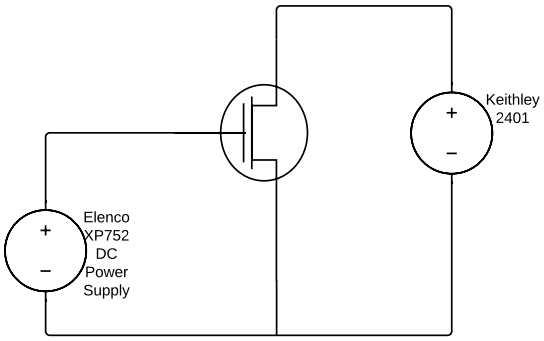

Figure 45. Fractal transistor testing set up.

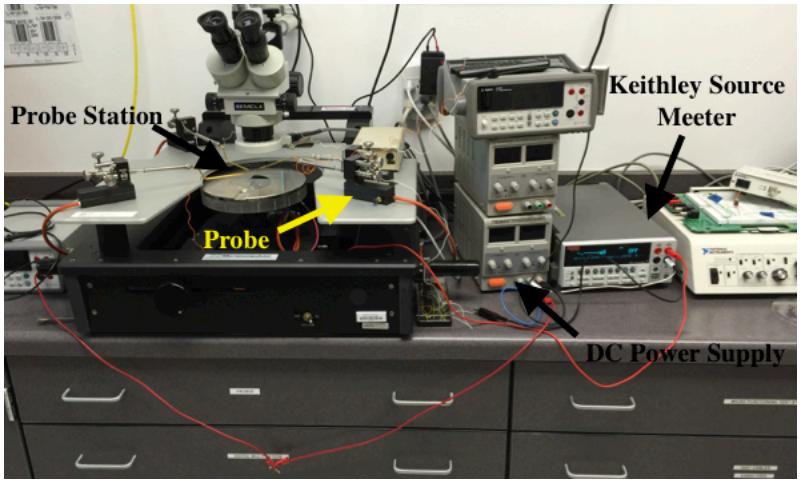

Figure 46. Experimental set up to test fractal device functionality.

Figure 47 displays four microprobes making contact to the fractal device: two contacting gates, and one each to the drain and source silver electrodes. The four available microprobes limit the ability to supply voltage to all the gates in the three and four gate terminal devices. Applying voltage to the largest geometric gates produces the best chance of causing current modulation.

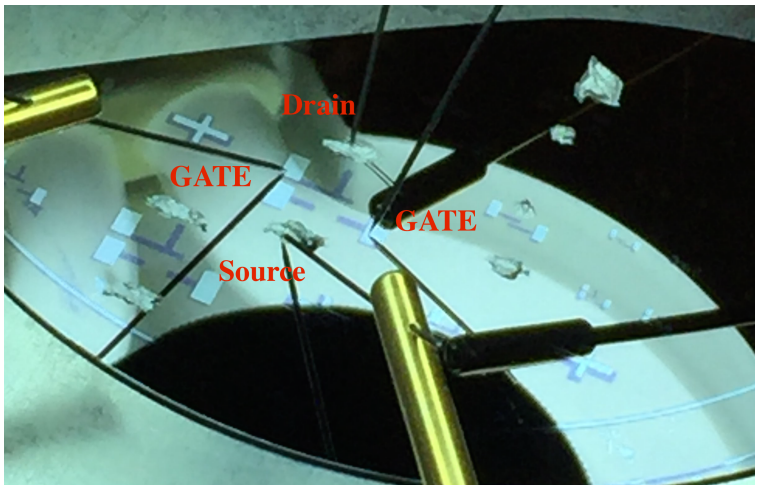

Figure 47. Microprobes contacting the fractal device.

The two gate probes connect to the same DC power supply producing equal voltage on both gates. All the microprobe wires connect to an O-ring electrical crimp that allows banana to mini-grabber cables to connect the microprobes to the power supplies. Figure 48 displays the connecting two gate microprobe wires. Figure 49 displays a top view and side profile view of the probes making contact to the device.

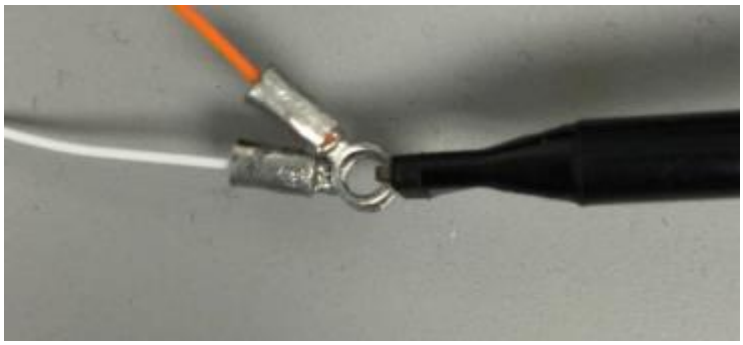

Figure 48. Connecting the mini-grabber cable to the two microprobe contacts that contact the gate terminals.

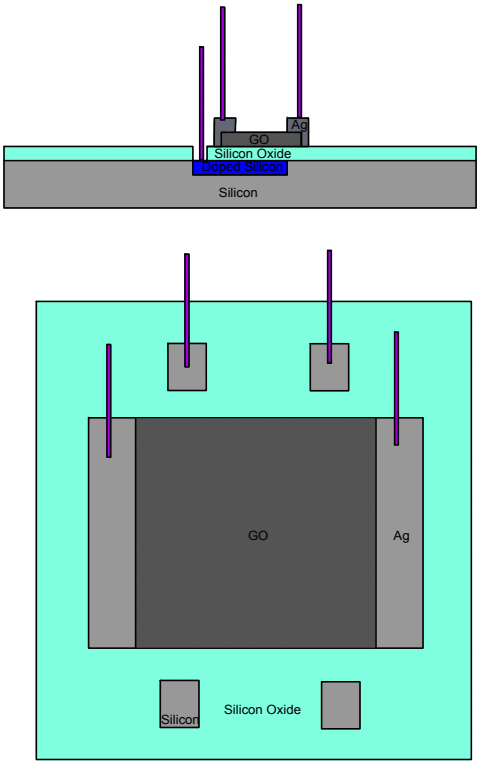

Figure 49. The purple rectangles represent the microprobes that make contact to the device during testing. The top Figure shows a side profile view while the bottom shows a top profile view.

A light shines on the microprobe station during probe contact, and a vacuum chuck holds the wafer in place. Once aligned, turning off all lights in the room, and surrounding rooms, produces the most consistent measurements. Placing a towel over the test structure accomplishes the same testing environment while leaving the lights on. An Agilent 34405A 5½ Digit Multimeter, operating as a voltage meter, confirms the actual voltage at the gate contacts equals the desired value for each gate voltage setting. When the DC power supply reads 0 V, it actually produces 15 mV at the gate contacts. Powering down the DC power supply during 0 V gate voltage measurements ensures no gate voltage.

Setting the compliance of the Keithley SourceMeter to 1.05 A ensures the maximum capability of the SourceMeter. The Keithley SourceMeter changes its internal resistance when it switches measurement ranges; turning off the auto range prevents the range from switching and the internal resistance from switching. The drain to source voltage sweeps from 0 V – 10 V for each gate voltage. The gate voltage ranges between 0 V – 5 V. The rGO fractals were tested first, because they represent the final devices that experience all processing steps. Figure 50 displays the resulting data for rGO fractals on wafer B11 and B4.

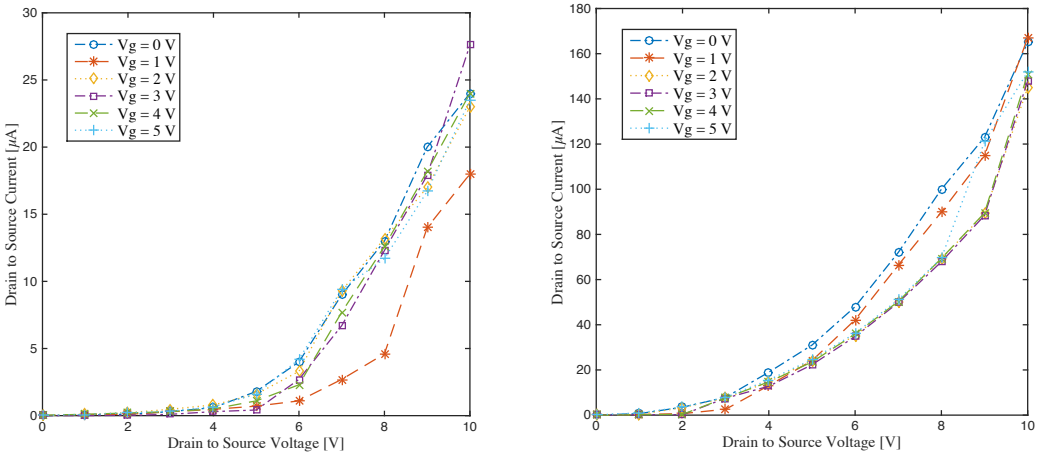

Figure 50. RGO fractals of wafer B11 (left) and B4 (right) transfer characteristics. B11 contains the air-drying Cal Poly GO solution, and B4 contains vacuum-drying Graphenea GO solution.

Both plots in Figure 50 show minimal response to gate voltage. This prompts checking the gates to ensure they function properly. Two microprobe tips contact a single gate contact to the Keithley SourceMeter to ensure good electrical contact to the doped silicon. Figure 51 displays the probe contacting the gates.

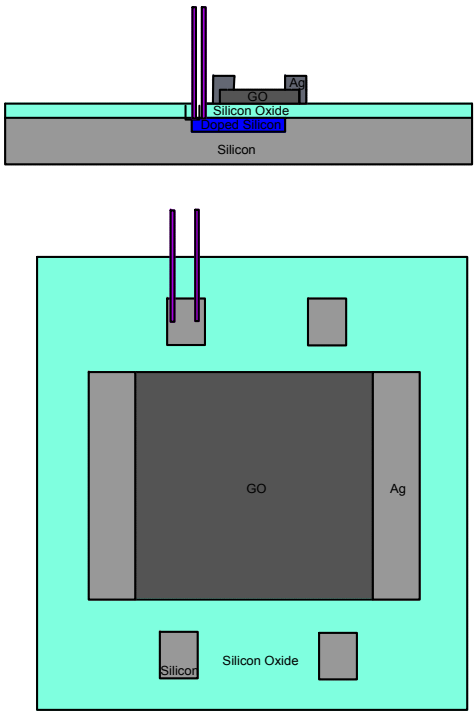

Figure 51. Probe contacting the same gate contact to test electrical connection to the silicon gates. Top Figure portrays a side profile view while the bottom Figure portrays a top view.

None of the rGO devices produces gate contacts with good electrical connections. The gate contacts should appear to be short circuits during this test but the measurements show they conduct little current between the probe tips. The current between the probe tips maintain a consistent reading around 10pA, the lower limit for the Keithley SourceMeter. Testing illuminates the cause of the open circuit electrical connections on rGO fractals. Both GO wafers B4 and P1 experience the same testing that the rGO fractals experience and produce currents orders of magnitude larger. The currents of the two GO wafers don't match each other, because they contain different dopants. Figure 52 displays the resulting current through a single gate contact.

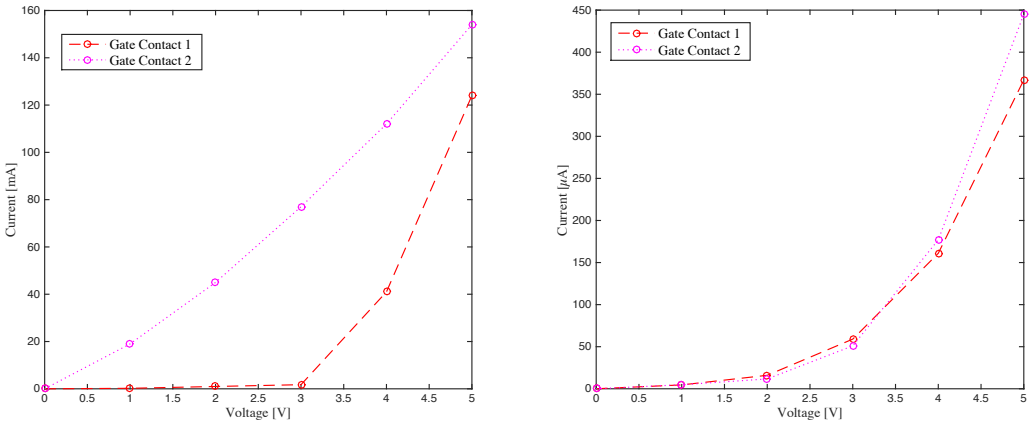

Figure 52. Current through gate contacts on wafer B4 (left) and wafer P1 (right). Note the different current scales.

Both B4 and P1 produce gate contacts that allow for electrical connection. Wafer P1 produces much smaller currents that follow each other closely. Wafer B4 better explains why the rGO gates conduct minimal current. A native oxide layer forms on silicon with a thickness around 2.5 nm. Silicon dioxide insulates the gates from making electrical contact with the probe tips. The presence of silicon dioxide explains why one of the gate contacts did not start conducting before applying a 4 V potential across the probe tips. The rGO fractals contain an even greater amount of silicon dioxide above the gate contacts that prevents electrical contact and explains why the output characteristics remain relatively constant over the applied gate voltages.

Ambient oxygen in the reduction furnace causes burning of the fractals during the reduction process and facilitates growth of silicon dioxide above the silicon gate contacts. The increase in silicon dioxide thickness prevents good electrical contact to the gates and prevents proper functionality of the gates. Testing the gates for isolation permits local gating abilities. Using the two gate contacts tested in Figure 52 to ensure good electrical connection to the gates, one probe tip contacts each gate while the Keithley SourceMeter supplies a voltage across the

probe tips. Figure 53 displays a top profile view of the probe tips making contact to the gate contacts.

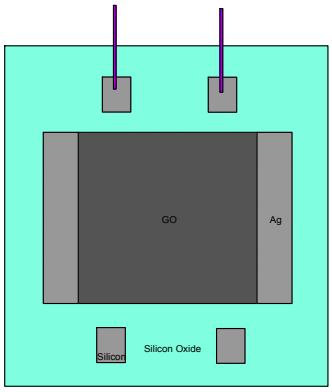

Figure 53. Top profile view of the probe tips contacting two separate gate contacts to test leakage current.

This confirms whether the gates localize electrostatic effects or if the gates act as one large bottom gate. No current should flow between the gates because one PN junction should always be reversed biased. Figure 54 displays the results.

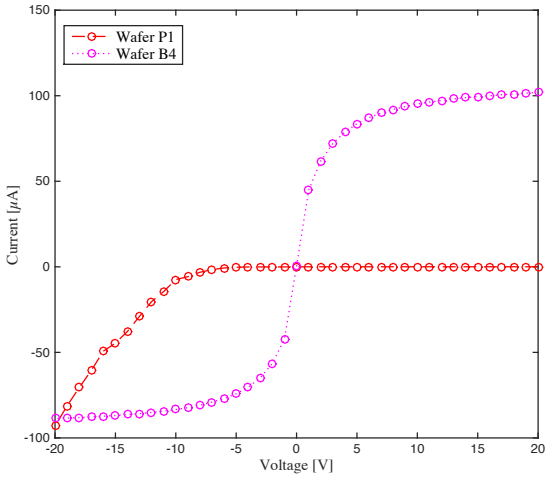

Figure 54. Leakage current between gate contacts on wafer P1 and B4.

Figure 54 shows that both wafers contain leakage current between gates with a negative potential. Wafer B4 also produces leakage current with a positive potential. Testing diode characteristics allows confirmations that Figure 54 displays the leakage current of the device. Substrates contacts don't exist on the device; the substrate makes contact with the microprobe station and allows biasing of the substrate. Good electrical contact on wafer P1 prevents these measurements for this wafer. Diodes prevent current flow in reverse biasing and allow current flow in forward biasing, so there should be no current flow with a negative voltage, and current flow with a positive voltage. Figure 55 displays the results for wafer B4. Grounding the gate terminals and applying voltage to the substrate forward biases the PN junction.

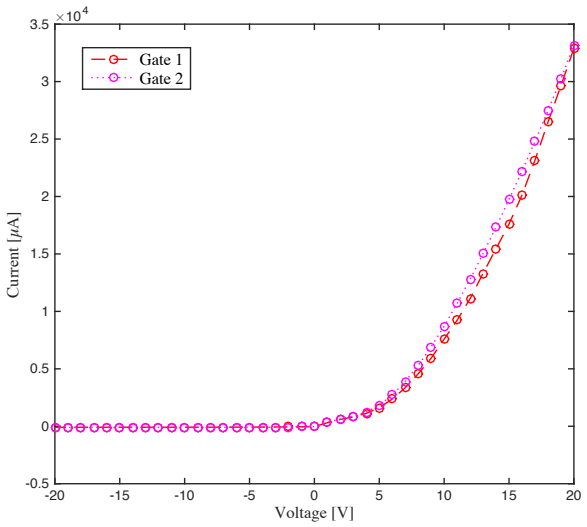

Figure 55. Diode characteristics for two gates on wafer B4.

The large forward current in Figure 55 confirms that the current measurements of Figure 54 pertain to leakage current between the gates. Leakage current between the gate contact and the GO contact could produce large measurement errors in the output characteristics. Testing of the leakage current between the gates and the GO electrodes consists of one probe tip contacting the

gate while a second probe tip contacts the silver epoxy GO electrode. The Keithley SourceMeter applies a potential between the two probe tips. Figure 56 displays the result for B4.

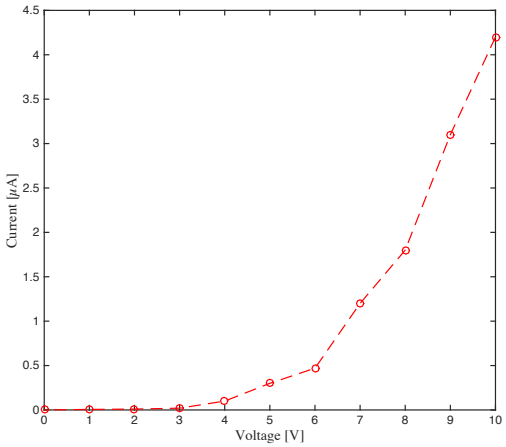

Figure 56. Leakage current for wafer B4.

The maximum leakage current of 4.2 μA confirms the silicon dioxide dielectric layer between the substrate and the GO electrode insulates the gates from the active part of the device. Confirming gate functionality allows output characteristic testing. The GO fractal on B4 experiences the same testing setup as the rGO fractals on B4 that Figure 49 displays. The gate current was not measured during the output characteristics, because a maximum gate voltage of 5 V produces 0.5 μA of leakage current. The device should conduct current with both positive and negative drain to source voltages, because graphene conducts both holes and electrons. The gate voltage should shift the plots as a response to electrostatic interaction. Figure 56 displays the resulting output characteristics for the GO fractals on wafer B4.

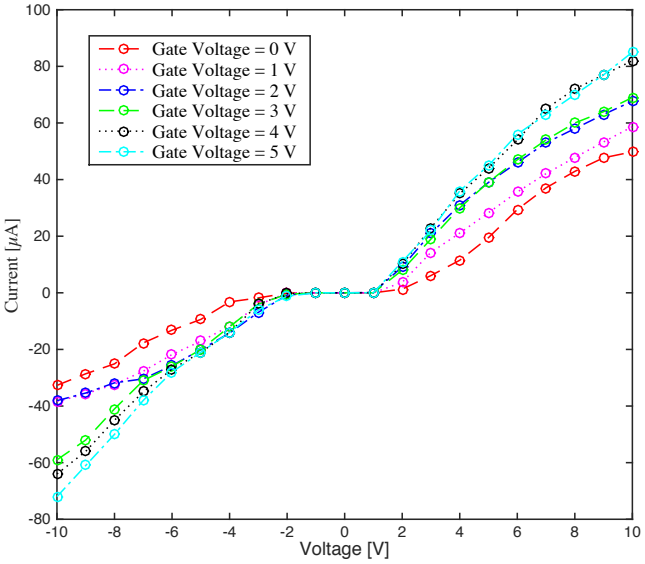

Figure 57. Output characteristics relative to gate voltage for a GO fractal on wafer B4.

Figure 56 shows that the drain to source current increases with the increase of gate voltage. The plot confirms that electrostatics affect the current flow through the device and that it conducts with both negative and positive drain to source voltages. Further output characteristics of the rGO fractals ceases, because the gates do not function properly. Comparisons of the rGO and GO fractals can occur at zero gate voltage on both devices. A drain-source voltage of 10 V produces the data points for resistance calculations for the rGO and GO fractals. Table 19 documents the minimum resistance and power dissipation.

Table 19. Minimum resistance values for each fractal device tested and the power dissipation.

Device	Drain to Source Voltage [V]	Resistance [kΩ]	Power Dissipation [mW]
B4 GO	10	202.0	0.5
B4 rGO	10	60.6	1.7
Percent Difference [%]	0	233.3	233.3

Table 19 further confirms theoretical predictions made previously in this chapter. Graphenea GO fractals (B4) produce a smaller resistance than calculated in the previous section. This agrees with anticipated results because of the reduction in film thickness. Graphene conducts through PI bonds and is in its ideal state at a monolayer thickness. Additional layers cause the PI bonds to break, the electrons are now needed to bond the layers together and do not participate in conduction. The greater than expected resistance values of the Graphenea rGO fractals suggest incomplete reduction of the device. The GO fractals contain 233.3 % higher resistance than the rGO fractal when all other parameters are held constant. This confirms that reduction took place during the intended reduction process. Future work includes an elemental analysis of the reduced fractal devices to confirm elemental composition to confirm the reduction percentage.

Testing determines that proper gate functionality necessitates improving contacts to the gates. Sputtering a metal with a high melting temperature could accomplish this. A metal such as tungsten could be used. Figure 56 confirms that gating can affect GO fractals and Table 19 confirms that thermal reduction of GO reduces the resistance of the GO fractals. The data confirms developing a fabrication process to create graphene electronics; however, improvements are needed in the fabrication process to obtain the complete range of functionality desired. The next chapter concludes the thesis report with a summary of the project and a discussion of future work to improve the devices.

5. CONCLUSION

This thesis report documents developing a process producing graphene electronics. The project brings together four Cal Poly colleges: College of Engineering, College of Math and Science, College of Liberal Arts, and Orfalea College of Business. The College of Business advises on structuring the project and provides many valuable connections and mentors to guide the project to eventually produce a marketable product. This report documents the efforts of the College of Engineering, College of Math and Science, and College of Liberal Arts to complete the proof of concept for the fabrication procedure to further improve it in the future.

Networking with all the colleges requires a great amount of time but results in acquiring most resources necessary to produce graphene electronics at Cal Poly. Networking with Strasbaugh acquires a reduction furnace to perform reduction procedures. Exploring several fabrication procedures results in adopting traditional silicon processing to produce the substrates for graphene deposition and microfluidic channel as the deposition methods for the graphene traces.

A full processing run confirms producing graphene electronics that display a reduction in resistance post GO reduction. Although poor gate contacts to the rGO fractals prevents full testing of the devices, it illuminates issues with material layers and fabrication processing that can be adapted in future processing runs. The GO fractals display current modulation because of the gate voltage. The report concludes with a section describing future work to continue developing the initial fabrication process documented within this report.

5.1 FUTURE WORK

Now that Greene Tec, the author's start-up, designed and tested the fabrication process, the next step is to refine the fabrication process to produce commercial grade devices. Refining the fabrication process first requires understanding possible sources of error. Figure 57 displays a fish-bone diagram accounting for all possible sources of error.

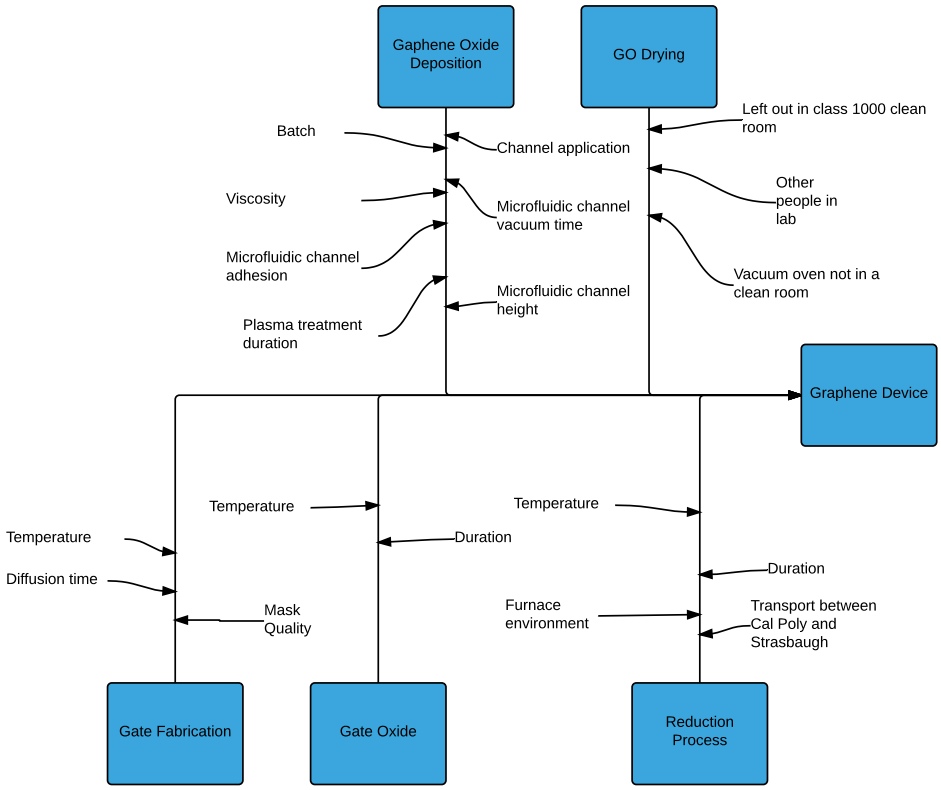

Figure 58. Fish-bone diagram documenting potential sources of error.

The biggest error during fabricating prototype 1 arose during the reduction process. Insufficient nitrogen flow causes some of the graphene fractals to burn off their substrates. The oxygen content also oxidizes the silicon gate contacts. The data also concludes incomplete

reduction took place in the Graphenea GO solution. Isolating the reduction process to improve it could greatly improve the final devices. By focusing solely on the output characteristics of the rGO without applying electrostatic gating provides a much quicker solution to rapidly test several parameters including nitrogen flow, reduction time, reduction temperature, and furnace temperature ramp rate. Continuing process development requires maintaining access to facilities acquired during the project

Bill Kalenian Strasbaugh generously permits continual access to their facilities for reduction experiments. Recruiting Conor Perry, a third year MATE student, ensures continued facility access to the Cal Poly infrastructure and resources. Perry will delve into individual process to optimize parameter settings as his senior project and characterizing the initial GO solution. Greene Tec hopes to produce a commercial grade fabrication process by the end of Perry's senior project.

5.2 QUOD ERAT DEMONSTRANDUM

This project brings together a multitude of backgrounds in the hopes to work on a device that pushes Cal Poly to its fullest potential. Few projects, if any, have incorporated the assembly of so many departments and colleges through out campus. The advanced search and development nature of this project forces everyone involved to push their creative abilities to adapt known fabrication processes for new applications. The accomplishments of this project not only show the engineering capability of Cal Poly but also its collaborative community that transcends any single department to work on projects to solve todays, and tomorrows biggest issues.

The developing printed electronic market pushes technology to create new fabrication methods as devices get smaller and thinner. Graphene provides an attractive material for printed electronics, because its purest state is a monolayer of carbon atoms. The abundance of carbon and the high electrical performance of graphene could allow it to take over the market space of electrical conductors, once a cost efficient method for productions arises. This project focuses on developing a repeatable, adaptable, and scalable graphene electronic fabrication method for any application desired. Centralizing around making fractal graphene transistors, a novel device emerges while testing key fabrication steps to produces devices of any geometric shape.

The fractal geometry of the devices proves that microfluidic channels can deposit and pattern graphene oxide solution into complex geometric configurations. Modifying channel height, and the weight percentage of the solution, creates films of different thickness; further exploring this process could produce monolayer sheets of graphene. Partial success of the reduction process proves that graphene oxide's electrical characteristics improve with the exposure to high temperatures. High temperatures dissociate functional groups along the carbon lattice, which decreases the materials band gap and increases its electrical conductivity. Ambient oxygen content in the furnaces results in device burning and destruction that shows creation of a

repeatable process requires further improving the reductions process. Even though function transistors were not produced, the goals of the project were achieved. The network and resources necessary to research and develop this technology has been assembled and prototyped the first design. It is now time to continue improving the fabrications process to bring this technology to its full capabilities.

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APPENDICES

APPENDIX A. BILL OF MATERIALS

The Cal Poly clean room and Strasbaugh provide most of the necessary material for fabrication. A CP connect grant provides the money necessary to purchase project supplies not supplied by Cal Poly or Strasbaugh. Table 20 below documents purchases and donations.

Table 20. Bill of materials and their use.

Index	Part	Use	Distributor	Part #	Quantity	Price [$/unit]	Total Price [$]
1	SiO2 wafers	Base substrate for all devices.	University Wafer	1435	25	21.5	537.5
2	Nitrogen Gas	Used in the spin coater, lithography, and furnace.	Supplied by Cal Poly (BMED) and Strasbaugh				0
3	Argon Gas	Used in the sputtering and dry etch machine.	Supplied by Cal Poly (BMED)				0
4	Positive Photo Resist	Used to pattern material layers.	Supplied by Cal Poly (BMED)	Shipley 1813			0
5	Photo Resist Primer	Promotes adhesion for the photo resist.	Supplied by Cal Poly (BMED)	HMDS			0
6	Photo Resist Developer	Used to develop the photo resist.	Supplied by Cal Poly (BMED)	CD-26 RohmHass/Shipley			0
7	Photo Resist Stripper	Removes excess photoresist after etching.	Supplied by Cal Poly (BMED)	Microposit remover 1165			0
8	SU-8-2007	Used to create microfluidic channel mold.	Supplied by Cal Poly (BMED)	MicroChem SU-8-2007			0
9	Gate Mask	Lithography mask for doping	Supplied by Cal Poly				0

		of gates.	(Printed Electronics)				
10	Microfluidic mask	Lithography mask for creating microfluidic mold.	Supplied by Cal Poly (Printed Electronics)				0
11	GO Solution	Graphene Oxide solution. 1000mL.	Graphenea	4mg/mL, Water dispersion	1	214	214
12	SU-8 developer	Used to develop SU-8.	Supplied by Cal Poly (BMED)	MicroChem SU-8-2007 Developer			0
13	Graphene Sheet 1cm-1 layer	Mono layer graphene sheet	ACS Materials	Trivial Transfer Graphene	8	100	800
14	Graphene Sheet 1cm-6-8 layers	Multi layer graphene sheet	ACS Materials	Trivial Transfer Graphene	2	130	260
15	Gold Target	Used for SEM prep.	Supplied by Cal Poly (BMED)				0
16	PDMS	Used to make microfluidic channels.	Supplied by Cal Poly (BMED)				0
17	P3HT	Used as the semiconductor in control wafer.	Supplied by Cal Poly (Physics)				0
18	Piranha	Used to clean wafers of organics.	Supplied by Cal Poly (BMED)				0
19	BOE	Oxide etchant.	Supplied by Cal Poly (BMED)				0
20	Corning Eagle Glass	Substrate.	Donated by Corning				0
21	Quarts Boat	Holds wafers during GO reduction.	A.M. Quartz Corporation	5” low profile boat	1	211.00	211.00
22	Graphene sheet alignment jig	Aligns graphene sheets over gated regions	Eric Veber, Cal Poly Alumni	Alignment Jig	1	150	150
Total							2172.5

APPENDIX B. ACKNOLEDGEMENTS

The below descriptions acknowledge considerable contributions and resources provided by Cal Poly departments and industry.

Cal Poly, Biomedical Engineering Department

The biomedical engineering department generously permits access to their class 1000 clean room in building 41. This facility provides the majority of equipment necessary for this project. This facility provides a clean environment to perform fabrication and equipment necessary for micro-fabrication. An oxidation furnace grows the gate oxide necessary for gate insulation from the graphene layer. The diffusion furnace provides the environment necessary to diffuse dopant atoms into silicon. Spin coaters uniformly distributes material layers. Photolithography alignment machineries patterns photosensitive materials. Several fume hoods provide a safe environment for chemical etching, cleaning, and material deposition. The Vacuum chamber produces low pressures to degas PDMS. The oven cures the PDMS after deposition. The plasma treatment device pretreats the silicon substrate before GO deposition to improve adhesion. The SEM produces GO sheet images. The testing facility adjacent to the clean room has a variety of metrology equipment specific for testing micro-electronic devices.

Printed Electronics and Functional Imaging Department

The printed electronics and functional imaging department generously supplies the CDI Spark 2530 Inline UV printer and materials to create photolithography masks. This expedites prototyping and generates new collaborations between their department and the clean room community.

Strasbaugh

Strasbaugh, based in San Luis Obispo, specializes in chemical-mechanical planarization (CMP). Strasbaugh conducts business with the semiconductor industry, requiring on site clean room facilities and equipment. Vice President of Engineering Bill Kalenian generously donates their entire facility to help fabricate the devices. The equipment includes the ellipsometer and furnace.

Cal Poly, Electrical Engineering Department

The electrical engineering department generously provides metrology equipment and intellectual guidance.

Cal Poly, Material Engineering Department

The material engineering department generously permits access to their vacuum oven necessary to dry the GO solution.

Cal Poly, Physics Department

The physics department generously supplies lab space access for research, and a variety of equipment and materials necessary for the project.

Cal Poly, Chemistry Department

The chemistry department generously permits access to their labs. Their labs contain equipment including ovens, centrifuges, vortex mixers, syringe pumps and other equipment useful for processing chemicals. They also supply their own GO solution for experimentation.

Cal Poly, Biology Department

The biology department generously permits access to their labs containing equipment including vortex mixers, centrifuges, chemicals and other equipment necessary for handling chemicals.

Cal Poly Center for Innovation and Entrepreneurship (CIE)

Cal Poly CIE permits access to their meeting rooms to provide a professional meeting atmosphere for conducting onsite interviews.