INVESTIGATION OF DEGRADATION EFFECTS DUE TO GATE STRESS IN GaN-ON-Si HIGH ELECTRON MOBILITY TRANSISTORS THROUGH ANALYSIS OF LOW FREQUENCY NOISE

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by

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DEDICATION

This thesis is dedicated to my best friend, Brittany, for the many months of unwavering support despite the neglect and frustration she had to endure while I completed my research, and to my parents for giving me an opportunity to get this far.

COMMITTEE MEMBERSHIP

TITLE:	Investigation of Degradation Effects due to Gate Stress in GaN-on-Si High Electron Mobility Transistors through Analysis of Low Frequency Noise
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ABSTRACT

Investigation of Degradation Effects due to Gate Stress in GaN-on-Si High Electron Mobility Transistors through Analysis of Low Frequency Noise

Michael Curtis Meyer Masuda

Gallium Nitride (GaN) high electron mobility transistors (HEMT) have superior performance characteristics compared to Silicon (Si) and Gallium Arsenide (GaAs) based transistors. GaN is a wide bandgap semiconductor which allows it to operate at higher breakdown voltages and power. Unlike traditional semiconductor devices, the GaN HEMT channel region is undoped and relies on the piezoelectric effect created at the GaN and Aluminum Gallium Nitride (AlGaN) heterojunction to create a conduction channel in the form of a quantum well known as the two dimensional electron gas (2DEG). Because the GaN HEMTs are undoped, these devices have higher electron mobility crucial for high frequency operation. However, over time and use these devices degrade in a manner that is not well understood. This research utilizes low frequency noise (LFN) as a method for analyzing changes and degradation mechanisms in GaN-on-Si devices due to gate stress.

LFN is a useful tool for probing different regions of the device that cannot be measured through direct means. LFN generation in GaN HEMTs is based on the carrier fluctuation theory of 1/f noise generation which states fluctuations in the number of charge carriers results in conductance fluctuations that produce a Lorentzian noise spectrum. The summing Lorentzian noise spectra from multiple traps leads to 1/f and random telegraph signal (RTS) noise. The primary cause of carrier fluctuations are electron traps near the 2DEG and in the AlGaN bulk. These traps occur naturally due to dislocations and impurities in the manufacturing process, but new traps can be generated by the inverse-piezoelectric effect during gate stress.

This thesis introduces noise and presents a circuit to bias the devices and measure gate and drain LFN simultaneously. Three measurements are performed before and after gate DC stress at three different temperatures: DC characterization, capacitance-voltage (C-V) measurements, and LFN measurements. The DC characteristics show an increase in gate leakage after stress caused by an increase in traps after degradation consistent with trap assisted tunneling. However, the leakage current on the drain and source side differ before and after stress leading to the conclusion that the source side of the gate is more sensitive to gate stress. Gate leakage current on the drain side is also sensitive to temperature due to thermionic trap assisted tunneling. Hooge parameter calculations agree with previous research. The LFN results show an increase in gate and drain noise power, $S_{Ig}(f)$ and $S_{Id}(f)$, in accordance with increased gate leakage current under cutoff bias. RTS noise is also observed to increase in frequency with increased temperature. Activation energies for RTS noise are extracted and qualitatively linked to trap depth based on the McWhorter trap model.

ACKNOWLEDGMENTS

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Table of Contents

LIST OF TABLES

LIST OF FIGURES

Chapter 1: Introduction

1.1 Why GaN?

Gallium nitride (GaN) high electron mobility transistors (HEMTs) are recognized as the most promising technology for development of next generation communication and microwave products due to their high power, temperature, and operating frequency capabilities. As a result, GaN HEMTs could potentially replace silicon (Si) and Gallium Arsenide (GaAs) based transistors in the near future in military and commercial applications in areas such as radar, phased array antennas, power amplifiers, and cellular, broadcast, and satellite communications. As the demand for these types of devices has increased, more research is being conducted to improve device reliability and reduce cost. However, the reliability and manufacturing issues are still not well understood. GaN technology poses a serious risk of failure in applications where high reliability and consistent, long-term high power performance is required. New research into GaN HEMT reliability seeks to discover the physics of failure mechanisms, how the mechanisms affect device performance, how device performance changes with time and use, and minimize the effects of these failure mechanisms.

1.2 Purpose

This thesis investigates the Low Frequency Noise (LFN) spectra of a representative GaN-on-Si device before and after applying high electric field stress to the gate. The data is then used to observe, quantify, and establish patterns linking gate high field stress, biasing conditions, temperature, and changes and anomalies in LFN to gain insight into electron trapping mechanisms which underlie the degradation of GaN HEMTs. In addition, successful

application of LFN spectroscopy will provide further evidence to the validity of the technique as a low cost device reliability test which can be integrated into a design cycle for future GaN products. The goal of this research is to add to the body of knowledge to improve the manufacturing, reliability, performance, and cost of GaN technology.

1.3 Thesis Summary

Using a custom made LFN amplifier, the LFN of each device under test (DUT) was recorded under different bias conditions and temperatures. In addition, device DC performance was also recorded before and after stressing to correlate changes in DC and noise performance. Finally, Capacitance-Voltage (C-V) testing was performed to evaluate how the physical characteristics of the HEMTs change with gate high field stress. These complementary characterization techniques yield information about both DUT degradation and data veracity.

Chapter 2 provides an overview of GaN HEMT technology and theory of operation. The characteristics and physical composition of the device are discussed in detail to address the purpose of each component of the epitaxial stack and the corresponding effect on the HEMT performance and reliability. Chapter 3 provides a survey of noise and noise sources, and an equivalent noise model for the GaN HEMT is introduced. Although a variety of noise sources will be introduced, the focus will be on noise sources dominant at low frequencies (<100 kHz). Chapter 4 introduces the hardware used to collect LFN data including the LFN test circuit and the measurement equipment used during the

experiment. The LFN test circuit design process is explained and the overall performance and validation method is presented. The test equipment used to perform LFN noise measurements, DC characterization, C-V test, and DC stress are evaluated with a description of how each piece of equipment is used. Chapter 5 gives a detailed explanation of the procedure for the various tests reported in this work including unofficial test results used to design the LFN test procedure and test results from various iterations of testing. Finally, Chapter 6 presents the results and provides analysis of the data and Chapter 7 summarizes the results, highlights important findings, and provides suggestions for future work.

This thesis presents results that support three main conclusions. First, LFN amplifier circuit can be made cheaply out of op amps with sufficient dynamic range to measure LFN to at least 100 kHz. Second, gate stress on GaN HEMTs causes defect formation in the AlGaN bulk due to the inverse piezoelectric effect causing increased gate leakage current via trap assisted tunneling and more ideal 1/f noise trends. Third, the temperature based investigation reveals RTS noise and gate leakage current are temperature dependent. The next section introduces GaN HEMT technology and degradation mechanisms.

Chapter 2: GaN HEMT Technology

2.1 Gallium Nitride HEMT Properties

Gallium nitride is a wide band-gap (WBG) semiconductor with an energy gap of 3.39 eV [1]. As shown in Table 2-1, GaN has an energy gap over three times that of Si. Generally, WBG semiconductors are superior to semiconductor materials traditionally used in RF and power applications in the following ways [1], [2]:

- Capable of withstanding higher voltages due to the high critical electric field breakdown (GaN has a breakdown field of 5 MV/cm).
- Higher operating power due to high voltage tolerance means power amplifiers with higher gain and output power.
- Higher thermal conductivity for dissipating heat so devices can operate at higher temperature and power without sustaining damage.
- High electron mobility (900 cm^2/V-s in GaN) coupled with the ability to withstand high voltages allows for higher saturation velocities ($2.7 \cdot 10^7$ cm/s in GaN) and higher operating frequency.

Advances in epitaxial growth of GaN on Al_2O_3 and Si substrates led to commercial GaN-on-Si HEMTs that can operate up to 3.5 GHz (although a theoretical cut-off frequency of 150 GHz has been reported with some GaN-on-SiC devices reported to have cutoff frequencies over 100 GHz) [3], [4], [5]. A two dimensional electron gas (2DEG) (discussed in §2.2.1) exists at equilibrium (no bias) due polarization created at the AlGaN/GaN heterojunction [6]. The electron density of the AlGaN/GaN 2DEG is an order of magnitude larger than that of similar GaAs pHEMTs [7]. The 2DEG characteristics of GaN

HEMTs, combined with the high breakdown field of GaN, make GaN devices extremely attractive for high power, high frequency applications. Current commercial GaN HEMT power amplifiers can operate at over 120 W CW power and over 900 W pulsed power levels [8], [9].

Table 2-1: Property Comparison of Common Semiconductors [1], [2]

	Si	**GaAs**	**InP**	**4H-SiC**	**GaN**
Bandgap (eV)	1.1	1.41	1.35	3.26	3.49
Electron Mobility (cm^2/V-s)	1500	8500	10000	700	900
Saturated (peak) electron velocity ($x10^7$ cm/s)	1.0	2.1	2.3	2.0	2.7
2DEG sheet electron density (cm^{-2})	N/A	$< 4 \times 10^{12}$	$< 4 \times 10^{12}$	N/A	20×10^{12}
Critical breakdown field (MV/cm)	0.3	0.4	0.5	2	> 1.7
Thermal Conductivity (W/cm-K)	1.5	0.5	0.7	4.5	> 1.7
Relative dielectric constant (ε_r)	11.8	12.8	12.5	10	9.0

2.2 High Electron Mobility Transistors

2.2.1 Theory of Operation

Like other types of field effect transistors (FETs), the HEMT, also known as a modulation doped FET (MODFET) or a heterojunction FET (HFET), has three terminals: a gate, drain, and source. Figure 2-1 shows the generic HEMT cross section. The gate voltage controls the channel resistance between the drain and source [10]. In basic terms, the gate and channel act like two plates of a capacitor: by introducing an electric field between the plates (a vertical electric

field), charge on one plate (the gate) builds up while equal and opposite charge accumulates on the other plate (the channel). FETs take advantage of the channel charge by applying another electric field between the drain and source (a horizontal electric field) that utilizes the charge carriers already present in the channel to conduct current [11]. An abundance of majority carriers causes the channel resistance to be low while an absence of majority carriers creates high channel resistance. In this way, the gate voltage controls the number of carriers present in the channel and the channel resistance. In the case of HEMTs, the drain-source channel consists of a thin, dense sheet of electrons that form in the GaN material near the AlGaN/GaN heterojunction called the two dimension electron gas (2DEG). The AlGaN layer, which consists of an alloy of GaN and AlN has a wider bandgap than GaN and thus acts functionally like the oxide of a MOSFET.

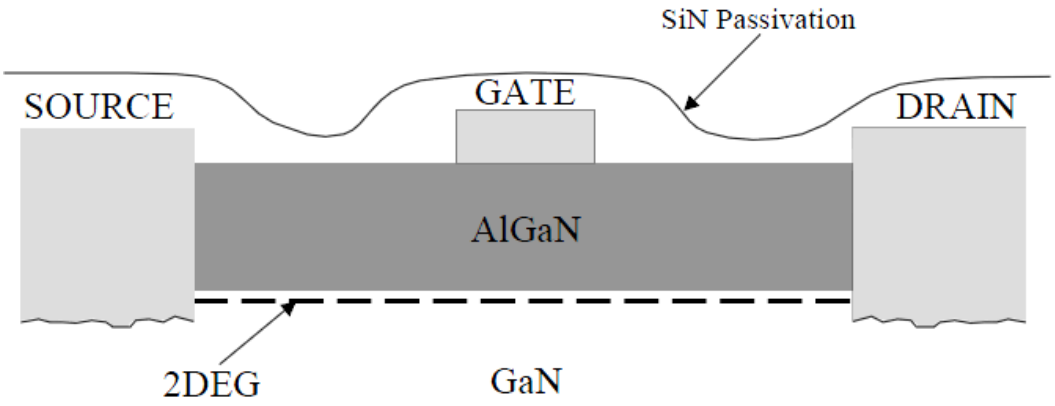

Figure 2-1: Generic cross section of an HEMT.

The name "high electron mobility" comes from the fact that electrons can reach significantly higher electron mobility in the HEMT channel compared to other FET devices. When the 2DEG fills with electrons, a quantum well confines

electrons to the narrow 2DEG region allowing electrons to move from drain to source only (hence the "two-dimensional" nature of the channel electrons). This prevents scattering from impurity states located outside the quantum well. Doping typically involves adding column III or V (sometimes II-VI) impurities to the semiconductor (usually Si) to create n-type (column V) or p-type (column III) material to change the net concentration of carriers in specific regions. However, doping the material can also limit carrier mobility due to impurity scattering where charged ions created by dopants repel charge carriers flowing through the material [11]. Impurity scattering increases the average time it takes for a charge carrier to travel through the channel which limits the material's saturation velocity and lowers the maximum operating frequency. Unlike other FETs, the HEMTs in this research do not utilize intentional doping to increase the number of carriers in the semiconductor. Instead, accumulation of electrons at the AlGaN/GaN heterojunction (hence the other name "heterojunction" FETs) creates the channel by spontaneous and piezoelectric polarization due to the lattice mismatch of the AlGaN grown on the GaN epitaxial layer [6], [12],. Lattice mismatch occurs because the crystalline structures of AlGaN and GaN differ in size (a 17% lattice misfit), so the atomic structure of the two materials stretches or compresses during the bonding process to match that of the adjacent material creating mechanical stress at the bonding site [13]. Equation (2-1) through Equation (2-5) approximate the piezoelectric polarization [14].

(2-1) $$P^{pz}_{Al_xGa_{1-x}N}(x) = xP^{pz}_{AlN}[\varepsilon(x)] + (1-x)P^{pz}_{GaN}[\varepsilon(x)]$$

(2-2) $$P_{\mathrm{AlN}}^{pz} = -1.808\varepsilon + 5.624\varepsilon^2, \text{for } \varepsilon < 0$$

(2-3) $$P_{\mathrm{AlN}}^{pz} = -1.808\varepsilon - 7.888\varepsilon^2, \text{for } \varepsilon > 0$$

(2-4) $$P_{GaN}^{pz} = -0.918\varepsilon + 9.541\varepsilon^2$$

(2-5) $$\varepsilon(x) = [a_{subs} - a(x)]/a(x)$$

x = Al ratio of the AlGaN

a_{subs} = unstrained alloy lattice constant

a(x) = unstrained substrate lattice constant

The spontaneous piezoelectric polarization effect, on the other hand, is a distinct mechanism from the strain induced piezoelectric effect. Spontaneous polarization is due to inherent differences between the electronegativities of the N and Ga/Al atoms and the lack of inversion symmetry in the GaN wurtzite crystal structure. The polarization exists without mechanical stress and is temperature dependent [6]. Equation (2-6) approximates the spontaneous polarization [14]. The net piezoelectric effect induces a positive sheet charge at the 2DEG causing electrons to accumulate in the region.

(2-6) $$P_{Al_xGa_{1-x}N}^{pz} = -0.090x - 0.034(1-x) + 0.019x(1-x)$$

The difference in valance, E_V, and conduction, E_C, band energies at the heterointerface causes E_V and E_C to bend as shown in Figure 2-2. A quantum well forms on the GaN side of the AlGaN/GaN heterointerface where the

conduction band dips below the Fermi level, E_F, limiting electron movement. The result is a dense sheet of trapped electrons known as the 2DEG. The higher energy states on either side of the 2DEG prevent electrons from diffusing to other parts of the material.

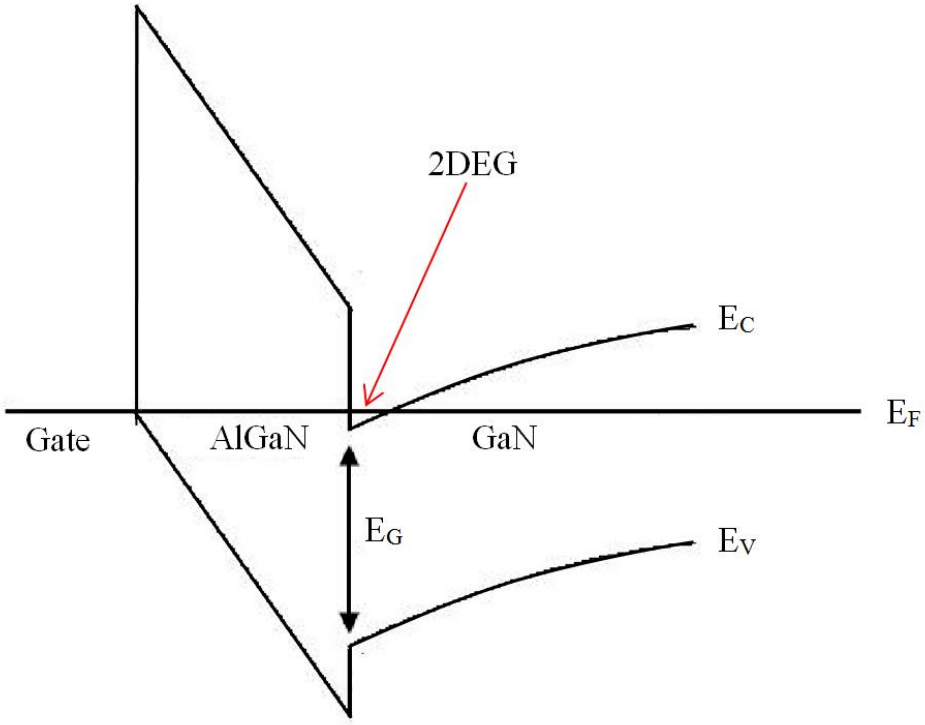

Figure 2-2: GaN HEMT band gap diagram [6].

2.2.2 Nitronex NPTB00004 GaN HEMT Physical Composition

The Nitronex GaN HEMT features the less commonly used Si substrate, which makes the device significantly less expensive than similar devices with SiC substrates. The devices in these experiments are packaged in an 8 pin SOIC package with a source pad on the bottom of the package. The device is rated to operate from DC to 6 GHz and output 5 W CW power at V_{ds} = 28 V with a typical 15.5 dB power gain [15].

The HEMTs used throughout the testing are grown on a 150 μm Si (111), high resistivity (10 MΩ-cm) substrate using metal organic chemical vapor deposition (MOCVD) [13]. An AlN nucleation layer on top of the Si acts as a transition material to address the lattice and thermal mismatch between Si and GaN [13]. An additional AlGaN transitional layer on the AlN absorbs stress created by the thermal expansion coefficient mismatch [13]. A 0.8 μm thick GaN layer and a 17.5 nm $Al_{0.26}Ga_{0.74}N$ layer form the heterojunction, followed by a 1.5 nm GaN cap. The Ni/Au Schottky gate contact has a width of 0.5 μm and length of 150 μm and is offset to the source side with a 1.5μm gate-source separation and a 3.5 μm gate-drain separation. The gate offset reduces the gate-source resistance and increases the gate-drain breakdown [16]. Ti/Al/Ni/Au ohmic contacts form the source and drain. These devices also incorporate a source-connected field plate (SCFP). The SCFP is used to reduce the vertical electric field component at the drain edge of the gate created by high drain bias allowing the device to withstand higher bias voltages. This lessens the strain in the device when the vertical electric fields in the AlGaN layer piezoelectrically couple to the strain of the layer inducing degradation past a certain field value as discussed in §2.3.1. The SCFP connects to the source and stretches to the drain side of the gate; a thin insulating layer prevents the gate from shorting to the source. A SiN_x passivation layer encapsulates the device surface [17]. Figure 2-3 shows a cross sectional illustration, and Figure 2-4 shows the actual device layout.

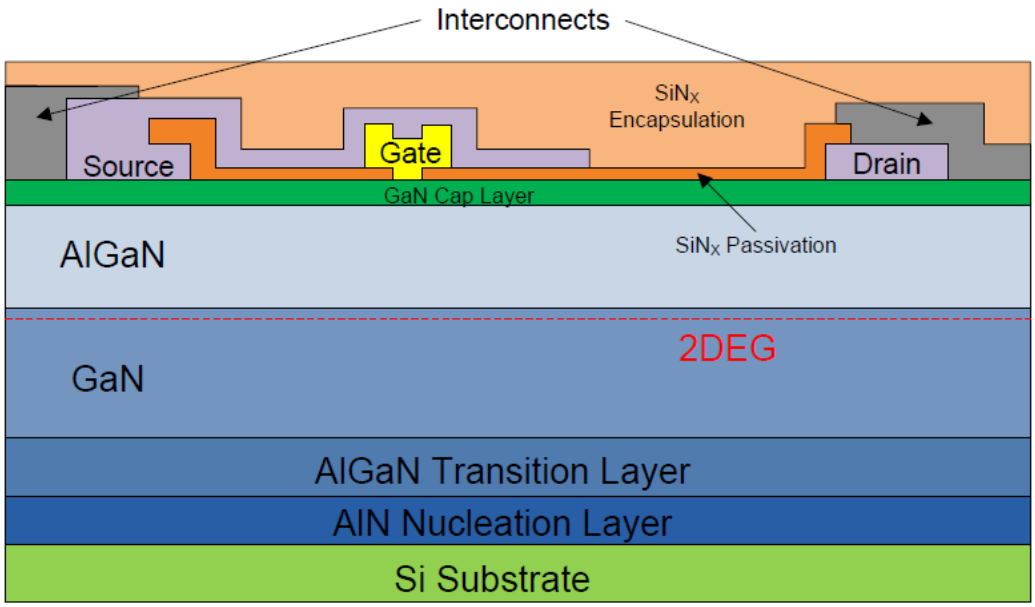

Figure 2-3: Nitronex NPTB00004 GaN-on-Si HEMT cross-section (not drawn to scale) [18].

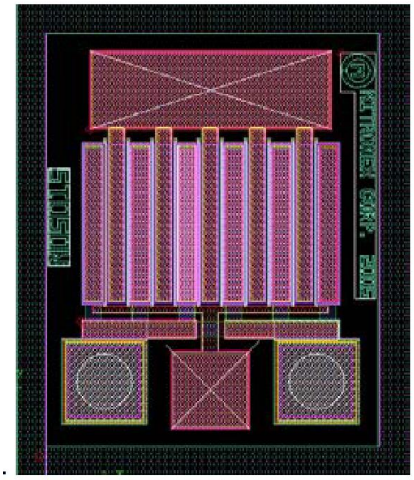

Figure 2-4: Nitronex NPTB00004 GaN-on-Si HEMT single 2mm transistor layout [17, 19].

2.2.3 GaN HEMT Substrates

GaN devices are most commonly grown epitaxially on foreign substrate wafers due to the cost of growing bulk GaN crystals and the low thermal conductivity of GaN compared to other semiconductors. By growing GaN on a

different substrate, thermal conductivity improves which reduces self-heating effects while minimizing fabrication cost. Commercially, GaN is primarily grown on SiC or diamond substrates, although other materials such as Si, sapphire, and aluminum nitride have also emerged [10]. The Nitronex NPTB00004 GaN-on-Si HEMTs cost $18 compared to similarly performing GaN-on-SiC HEMTs which cost $50 or more [3], [20], [21], [22].

2.3 HEMT Reliability and Degradation Terminal Characteristics

Although GaN-on-Si HEMTs show superior frequency, power, and thermal characteristics compared to GaAs devices, these devices are not widely used due to a lack of full understanding of the degradation physics of GaN HEMTs and conflicting mean time to failure (MTTF) data on existing device designs. Recent research has presented greater insight into the causes of device degradation which will be addressed in the following section and referenced in the data analysis in Chapter 6: to link LFN to device degradation.

The purpose of semiconductor reliability studies is to determine the physical mechanisms underlying degradation that will lead to improved system performance and lifecycle costs. Device degradation is accelerated by exposing the device to harsh conditions such as high electric fields and temperatures. One of the most easily observable signs of degradation is increased gate leakage current. Previous research has shown that gate leakage current, I_g, increases when exposed to a high electric field (for reasons that will be discussed in subsequent sections) [18], [23]. The change in gate leakage current was found to be dependent on both the gate stress voltage and the amount of time the gate was

exposed to the stress [23]. Investigations into the effects of gate stress with V_{ds} = 0 V show a two order of magnitude increase in I_g after stress exceeds V_{crit} that does not recover to pre-stress levels after removing stress and allowing the device to sit unused [24]. Another well documented and thoroughly studied phenomenon is drain current collapse. One cause of drain current collapse is when a sudden, negative voltage is applied to the gate terminal (different experiments use V_{gs} from -6 V to -70 V) which can result in a 20% or more decrease in drain current [23], [25]. This is especially detrimental to GaN based power amplifiers (PA) where the drain current dictates the output power. Other measurable types of degradation include changes in the I_{ds}-V_{ds} characteristics, the I_{ds}-V_{gs} transfer characteristics, and shifts in the threshold voltage, V_{th}, and transconductance, g_m. Degradation effects can be classified as either permanent or reversible with some traits experiencing partial or full recovery to the pre-stress state over time [18].

The clearest way to demonstrate degradation is through micrographs of the affected region after a stress period. Some examples of these images are shown in Figure 2-5 and Figure 2-6. Typical imaging techniques include atomic force microscopy (AFM), scanning electron microscopy (SEM), and transmission electron microscope (TEM) [26]. In Figure 2-5, electric field induced gate stressing causes damage to the drain and source edges of the gate contact at the GaN cap layer which protects the AlGaN surface [26] [27].

Degradation also manifests in a change in the I_{ds} vs. V_{ds} family of curves, discussed more in §5.2, that shows an increase in I_{ds} due to a negative shift in the

threshold voltage, V_{th} (this trend is also observed in data presented in §6.1) [18]. Figure 2-6 shows that mass is being transported away from the region nearest to the gate edge. This process must be driven by a corresponding gradient in either electrostatic potential (an electric field) or by a gradient in chemical potential. The reigning theory that explains the degradation in Figure 2-5 and Figure 2-6 is that the vertical electric fields induce a mechanical strain in the AlGaN layer eventually causing structural defect formation which act as electron trap levels beyond a critical field level. This mechanism is known as the inverse piezoelectric effect. The inverse-piezoelectric effect and surface and bulk electron traps have been used to explain how the changes in performance and physical structure occur.

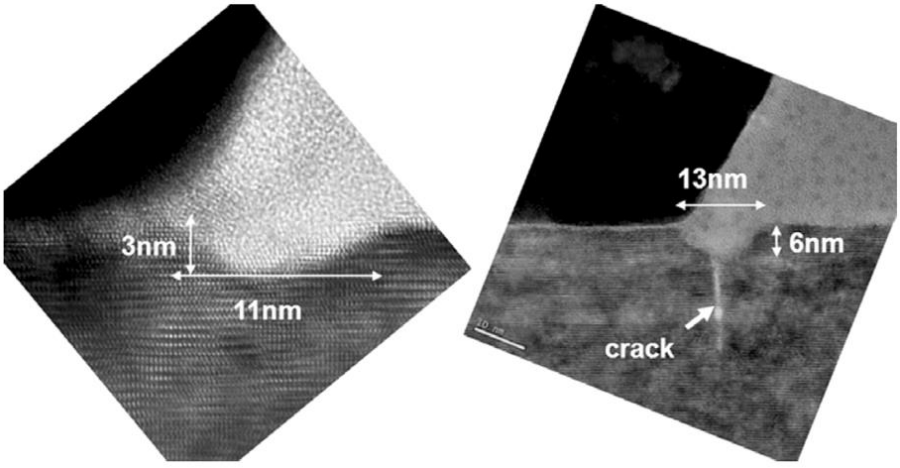

Figure 2-5: TEC image of GaN HEMT gate with signs of degradation on the gate edge [27].

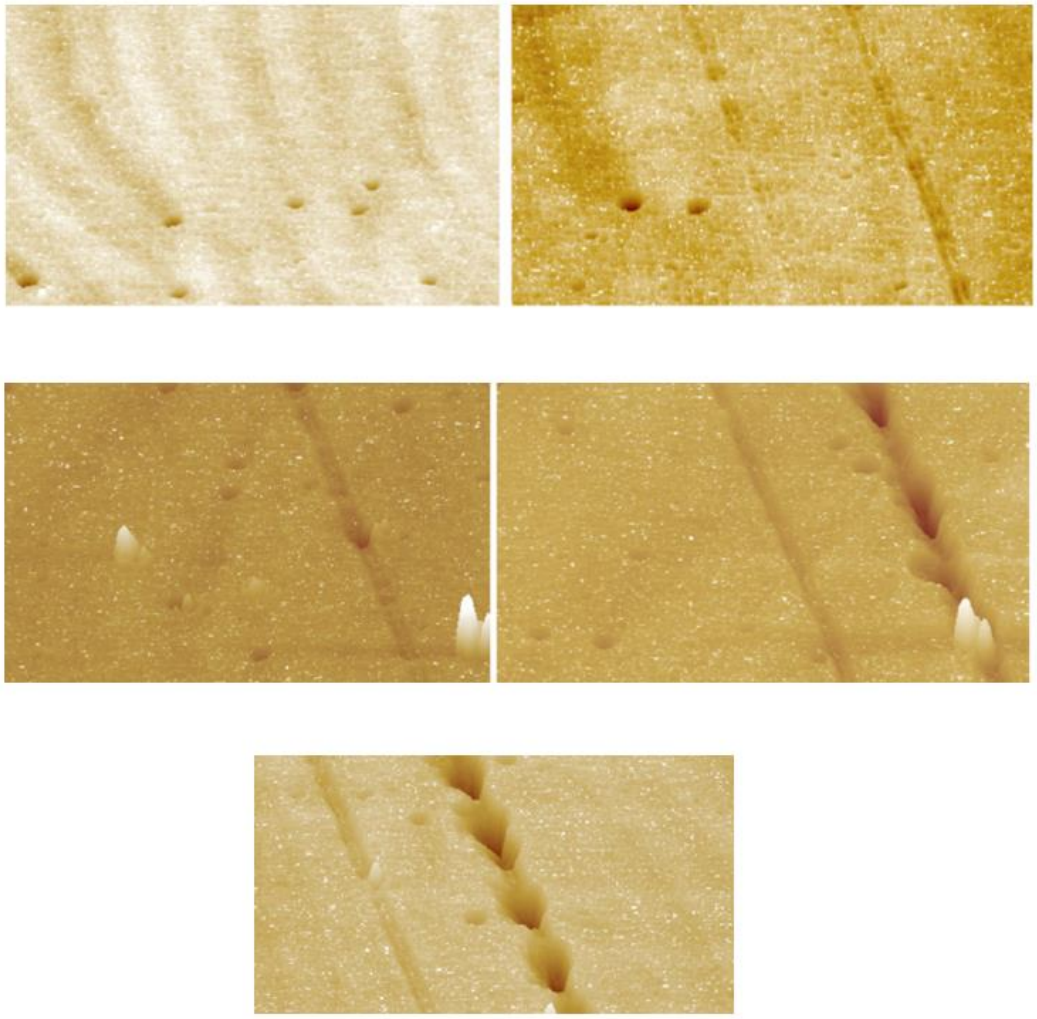

Figure 2-6: Example AFM image of progressive structural damage unstressed (top left), at V_{dg} = 15 V (top right), V_{dg} = 20 V (middle left), V_{dg} = 42 V (middle right), and V_{dg} = 57 V (bottom left) [26].

2.3.1 Inverse Piezoelectric Effect

III-nitride materials in the wutzite crystal structure are highly piezoelectric materials; it is this property that creates the 2DEG region which makes AlGaN/GaN HEMTs superior to doped semiconductors in terms of electron saturation velocity [23]. However, the piezoelectric force also induces a large mechanical stress on the material lattice that can cause crystallographic defects if added stress, such as an electric field, exceeds its tolerance. The strain and

subsequent defects that occur due to the mechanical strain introduced by an electric field is known as the inverse piezoelectric effect [23]. Applying a negative electric field to the gate creates a high tensile strain on the drain side of the gate with the largest force in the AlGaN near the gate contact [23]. The stress near the gate surface leads to the formation of pits and cracks in Figure 2-5 and Figure 2-6 [26]. The resulting pits and cracks can contribute to an increase in surface electron traps that lead to drain current collapse and an increase in gate leakage current due to the formation of bulk electron traps.

2.3.2 Bulk and Surface Electron Traps

Electron traps are interruptions to the perfect periodicity of the crystalline structure of a material that create intermediate energy states electrons can occupy within the normally forbidden bandgap. This process is illustrated in Figure 2-7 where an electron suddenly loses energy and falls from the conduction band to the trap level. The electron remains trapped until it acquires enough energy to re-enter the conduction band (the converse of this process is the electron falling from the trap level to the valence band; this is more conveniently pictured as the trap level capturing a hole). An electron may attain the requisite energy through a variety of ways including electric field, thermal, or optical excitation. Because the exact position of each electron in a material at a finite temperature is unknown, the exchange of energy between particles, and thus the release of electrons from traps, is characterized by probability. This is done by associating a time constant, τ, with each trap to characterize the average amount of time it takes for an electron to trap and detrap.

Traps are located in one of two regions: the bulk or the surface [28], [29]. Bulk traps are present throughout the material due to impurities or defects in the crystalline structure. Surface traps, on the other hand, are only present at the surface of a material or at the interface of two materials where lattice mismatches and imperfect bonding between two materials occurs [12]. Each type of trap is suspected of playing a role in GaN HEMT degradation. Surface electron traps occur at the AlGaN surface near the gate. When a negative voltage is applied to the gate, such as $V_{gs} < V_{th}$, an electron can become trapped at the surface. As V_{gs} increases, the trapped electrons add negative charge to the extended trap states along the surface. This has the effect of increasing the length of the gate, thus suppressing the 2DEG over a larger region. The result is fewer electrons in the 2DEG and lower I_{ds} which reduces the maximum output power. This scenario is depicted in Figure 2-8. Due to the bias conditions of the tests presented in this thesis, the effect of surface traps on device performance after gate stress is not explored. This thesis focuses on the effects bulk trap creation in the AlGaN layer have on device performance and LFN.

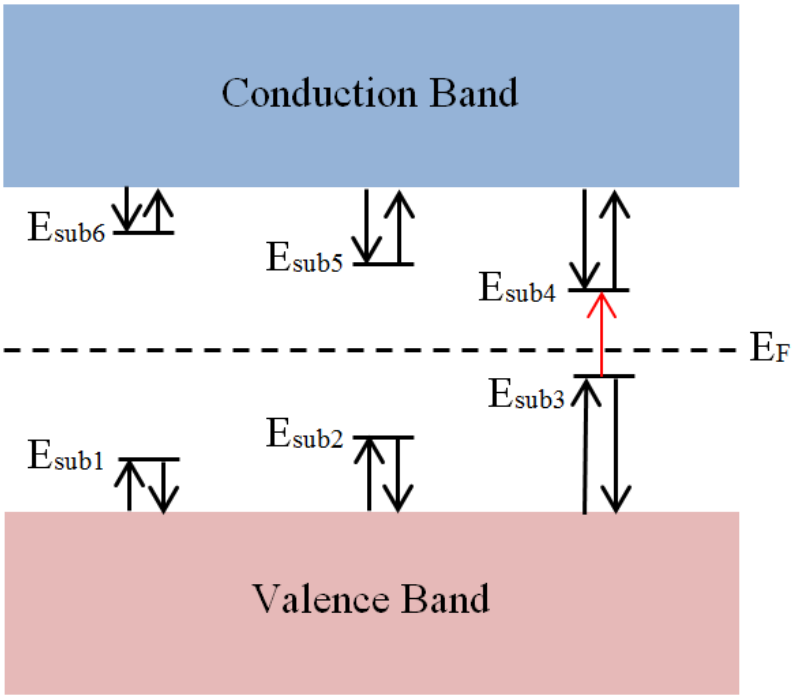

Figure 2-7: Bandgap diagram depicting electron trapping and detrapping. In some cases, electrons can travel between sub-energy traps.

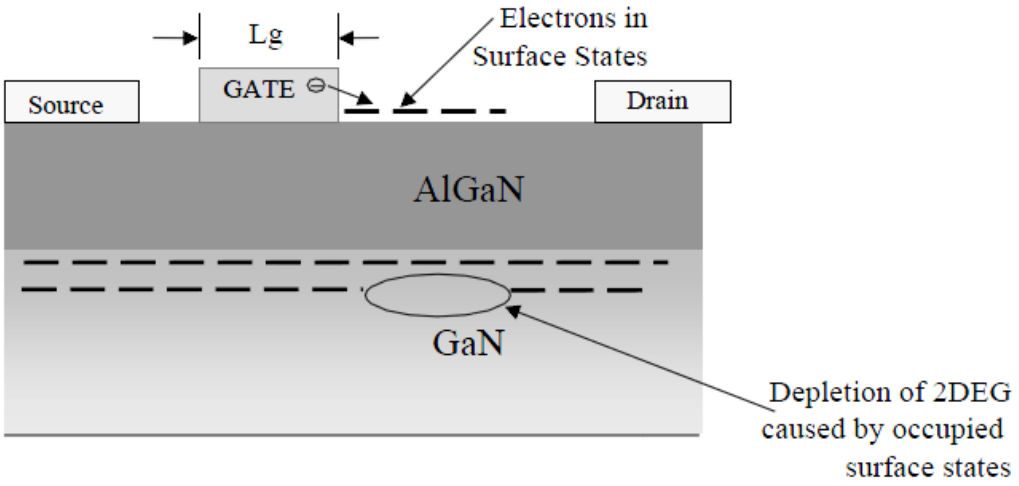

Figure 2-8: Surface traps in the AlGaN near the gate deplete the 2DEG of electrons which can reduce I_{ds} and limit output power. Electric field and thermal excitation can cause detrapping [10].

It is difficult to differentiate the effects of surface and bulk traps since the application of heat or electric field affects both types. Research has shown the

existence of these traps by applying a high negative V_{gs} to induce trapping which causes the DC performance to degrade. Detrapping is then performed by applying increasing steps of V_{gs} or temperature while the resulting current from the detrapping electrons is measured. After detrapping, DC performance reverts back to the pre-trapped state [18]. Other variations of this experiment have been used to measure the decrease in I_{ds} with more negative V_{gs} to induce more trapping [23].

2.3.3 Trap Assisted Tunneling

Bulk traps in the AlGaN layer are suspected of causing gate leakage current, I_g. Previous investigations applying high field stress have speculated that an increase in I_g after stress is due to stress induced defects formed through the inverse piezoelectric effect [18] [30]. The defects created in the AlGaN buffer act as electron traps at intermediate energy states which allow electrons to hop from trap to trap through the AlGaN to the 2DEG. The cross sectional illustration of a GaN HEMT in Figure 2-9 depicts gate electrons leaking through the AlGaN to the 2DEG. Figure 2-10 shows the band diagram representation of the same mechanism where electrons "hop" to lower energy defect states to reach the 2DEG.

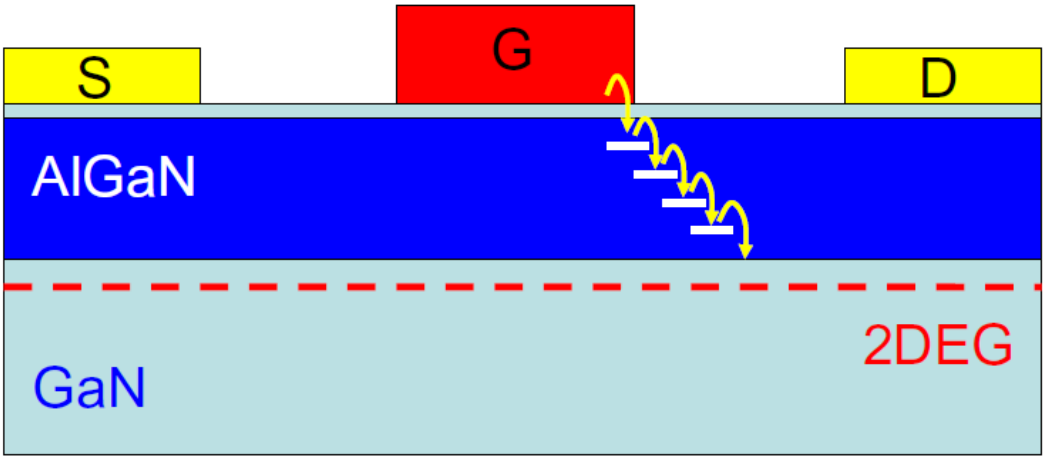

Figure 2-9: Physical representation of electron traps forming a conduction path from the gate to the 2DEG causing gate leakage current. This process is thought to be intensified by the inverse piezoelectric effect due to high vertical field stress [23].

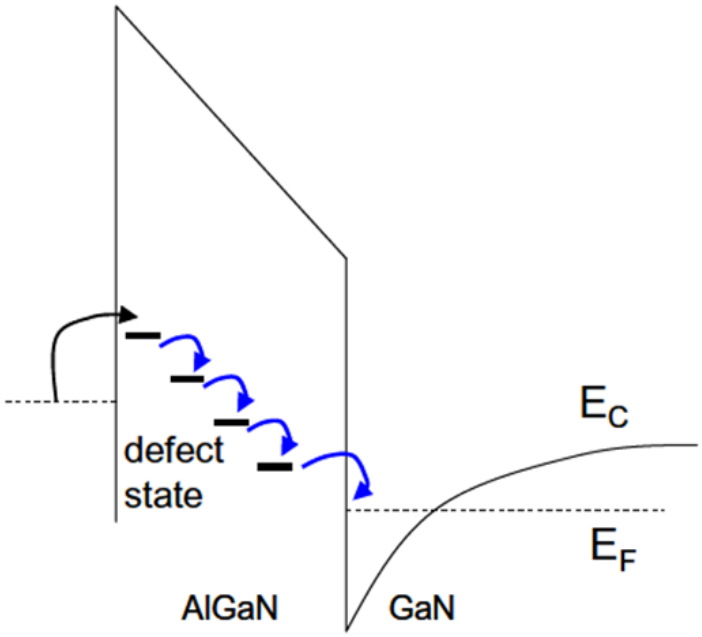

Figure 2-10: Band diagram representation of electrons "hopping" from electron traps through the AlGaN buffer to the 2DEG [23].

McWhorter speculated that the trap time constant is related to the depth in the material based on Equation (2-7) which is based on the theory that 1/f noise is generated by thermionic emission [29], [31].

(2-7) $$\tau = \tau_0 e^{Ax}$$

τ = trap time constant

τ_o = constant dependent on the upper and lower time constant limits, τ_1 and τ_2

x = trap depth from the gate contact

A = tunneling process characteristic constant

If the number of traps with time constants between the range of (τ,τ+dτ) is defined as dN_{trap}, then Equation (2-8) shows that $g(\tau) = dN_{trap}/d\tau$ will be proportional to $1/\tau$ if dN_{trap}/dx is constant over the distance of the AlGaN (where C is a constant). Therefore, if the material has a homogenous distribution of traps, then $g(\tau) = 1/\tau$ will result; any deviation from a homogenous distribution will result in a non-constant dN_{trap}/dx and a different $g(\tau)$ distribution.

(2-8) $$dN_{trap} = \frac{dN_{trap}}{dx}\frac{dx}{d\tau}d\tau = \mathrm{C}\frac{dx}{d\tau}d\tau$$

The relationship between time constant and distance is very important because it provides a new way to characterize the trap locations that are observed through the LFN measurements. This relationship will be referenced more in §6.3 when discussing the LFN results.

2.3.4 Gate Contact Degradation (Gate Sinking)

Gate contact degradation, also known as gate sinking, occurs when the gate contact metal diffuses into the GaN/AlGaN material beneath it. Introducing a conductive material into the AlGaN allows electrons to leak through to the

2DEG more easily. These effects have been widely reported as the major contributor of gate leakage in GaAs and InP HEMTs but it has yet to be proven if gate sinking plays a significant role in gate leakage in GaN HEMTs [32]. Elevated temperature life-testing at junction temperatures as high as 390˚C have indicated that no detectable gate contact degradation occurs [33]. Since the highest junction temperatures in this research are approximately 100˚C, gate contact degradation is not a contributing factor to device degradation and gate leakage current.

Chapter 3: Low Frequency Noise

Noise is present in all electrical devices and is caused by fluctuations in voltage or current generated within both active and passive devices. The study and reduction of noise in passive components, semiconductors, circuits, and systems is important because noise represents the lower limit at which signals can be detected. Excess noise can disrupt or degrade signal integrity in digital and communication technology resulting in higher bit error rates or lost signal information. Low frequency noise can be especially detrimental because it is typically orders of magnitude larger than thermal or shot broadband noise and is easily injected into communications systems through phase-locked loop architectures. This thesis focuses on the 1/f noise and generation-recombination noise components of LFN as applied to low frequency noise spectroscopy. Because noise is directly related to fluctuations in charge flow, such as the random movement of electrons leading to thermal noise, it can be used to probe semiconductor devices to characterize behaviors that cannot otherwise be detected. Some of these mechanisms, such as the trapping and detrapping of electrons, occur at slower rates and thus appear at low frequencies.

The work in this report focuses on intrinsic noise, which is noise generated internally by the random motion of charge, as opposed to extrinsic noise which is radiated noise received by a device from an external source. This chapter provides an overview of noise theory and noise sources.

3.1 Noise Theory

Noise is considered a random signal because the signal does not have a repeatable period and therefore cannot be predicted. Noise is modeled as a

random variable which allows overall noise characteristics, such as the mean and variance, to be quantified. Two common ways of representing a noise voltage or current is root-mean-square (RMS) or mean square, $e_n^2(t)$ using Equations (3-1) and Equation (3-2) for voltage and current noise [34]. Note that throughout this report, noise is always referred to in RMS values in units of V, A, V/√Hz, or A/√Hz or in mean square values in units of V^2/Hz or A^2/Hz. These values can also be represented in decibels using Equations (3-3) and (3-4), where dBV and dBA are the same as dBV_{rms} and dBA_{rms} (the Dynamic Signal Analyzer used for LFN measurements outputs dBV_{rms} values, so this conversion is used extensively in data post-processing). RMS values can be easily converted to power in dBm using Equation (3-5) (the Spectrum Analyzer used for LFN measurements outputs dBm values in a 50 Ω system, so this conversion is also used extensively in data post-processing). The dB conversions in Equations (3-3) and (3-4) are equivalent to Equation (3-5) for R = 1 Ω. Finally, total noise power, E_{Tot}, between m incoherent noise signals is calculated using the root-sum-squared (RSS) formula in Equations (3-6).

(3-1) $$E_{rms} = \sqrt{\frac{1}{T}\int_0^T e_n^2(t)\,dt} = \sqrt{\overline{e_n^2(t)}}$$

(3-2) $$I_{rms} = \sqrt{\frac{1}{T}\int_0^T i_n^2(t)\,dt} = \sqrt{\overline{i_n^2(t)}}$$

(3-3) $$\text{dBV} = 20\log(E_{rms})$$

(3-4) $$\text{dBA} = 20\log(I_{rms})$$

(3-5) $$dBm = 10\log\left(\frac{E_{rms}^2}{R}\right) = 10\log(I_{rms}^2 \cdot R)$$

(3-6) $$E_{Tot} = \sqrt{E_1^2 + E_2^2 + \cdots + E_m^2}$$

E_{Tot} = Total output noise power [W]

E_i = Noise power for signal *i*, where $i = 1,2,3,\ldots m$ [W]

3.2 Types of Noise

3.2.1 Thermal (Johnson) Noise

Thermal noise, also called Johnson noise, is a type of broadband white noise, meaning that it is independent of frequency and has consistent mean-squared values at all frequencies. Thermal noise is produced by the random thermal movement of electrons within a material and is typically associated with resistors or resistive materials. Resistors used in FET and BJT small signal models are also modeled to produce thermal noise. Thermal noise is directly proportional to the resistor temperature and is modeled as a series voltage or parallel current noise source with values calculated from Equations (3-7) and Equation (3-8) [35]. Unlike shot noise (discussed in the next section) thermal noise is not dependent on current (as long as the current does not induce significant self-heating).

(3-7) $$\overline{v^2} = 4kTR\Delta f$$

(3-8) $$\overline{i^2} = \frac{4kT\Delta f}{R}$$

k = Boltzmann's constant = $1.38 \cdot 10^{-23}$ [J/K]

T = Temperature ≈ 300 K at room temperature

R = Resistor value [Ω]

Δf = measurement bandwidth [Hz] (for spectral noise, Δf = 1 Hz)

3.2.2 Shot Noise

Shot noise is produced by the random movement of electrons across a material junction such as a p-n junction. When a p-n junction is operating in forward bias mode, charge carriers move through the depletion region in discrete packets as holes and electrons. However, traversing the depletion region is a random event that relies on a charge carrier reaching a high enough energy state to enter the conduction band. Charge carriers cross the depletion region in bursts of charge (as carriers "shoot" across the depletion region) instead of at a constant rate that manifests as current noise. The resulting mean-squared noise current is therefore dependent on the current that flows through the junction as indicated in Equation (3-9). Like thermal noise, shot noise is also a type of broadband white noise. Shot noise occurs in devices with potential barriers such as diodes, BJTs, and MOS transistors [35].

(3-9) $$\overline{i^2} = 2qI_D\Delta f$$

q = electron charge = $1.6 \cdot 10^{-19}$ [C]

I_D = DC junction current [A]

Δf = measurement bandwidth [Hz] (for spectral noise, Δf = 1 Hz)

3.2.3 Generation-Recombination and Random Telegraph Signal (Burst) Noise

Generation-recombination (G-R) noise is a type of low frequency noise created by the random fluctuation of charge carriers as they move between different energy bands. Transitions can occur between the valence and conduction band or between the conduction/valence band and intermediate energy states [36]. In the case of GaN HEMTs, G-R noise is typically associated with traps (although G-R noise in general is not generated solely by trapping) which can be observed in the time domain as 1/f noise or random telegraph signal (RTS) noise. RTS noise has a square wave time domain waveform with varying duty cycles as shown in Figure 3-1. The sudden increase of current in the time domain is due to the sudden detrapping of electrons that causes a brief surge in current. The trap time constant, τ_{rts}, is the sum of the trapping, τ_{trap}, and detrapping, τ_{detrap}, averaged over multiple cycles since trapping and detrapping does not occur at exactly the same rate each time.

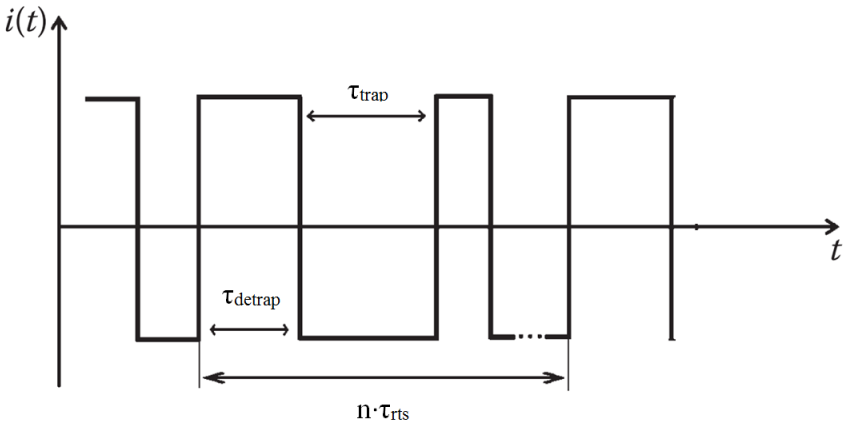

Figure 3-1: Time domain waveform of RTS noise where $\tau_{rts} = \tau_{trap} + \tau_{detrap}$ [37].

The RTS noise spectral density has a Lorentzian distribution form defined by Equation (3-10) where the trap time constant, τ_{rts}, represents the time constant of the RTS noise or the amount of time it takes an electron to trap and detrap [37]. τ_{rts} is a summation of individual trap time constants that results in an overall Lorentzian distribution which typically appears as a bump on the 1/f spectrum.

(3-10) $$\frac{S_V}{V^2} = \frac{S_I}{I^2} = \frac{S_N}{N^2} = \frac{\overline{(\Delta N)^2}}{N^2} \frac{4\tau_{rts}}{1+\omega^2\tau_{rts}^2}$$

$\overline{(\Delta N)^2}$ = variance of carrier fluctuation

N = number of carriers

ω = circular frequency [rad/s] = $2\pi f$

τ = trap time constant [s]

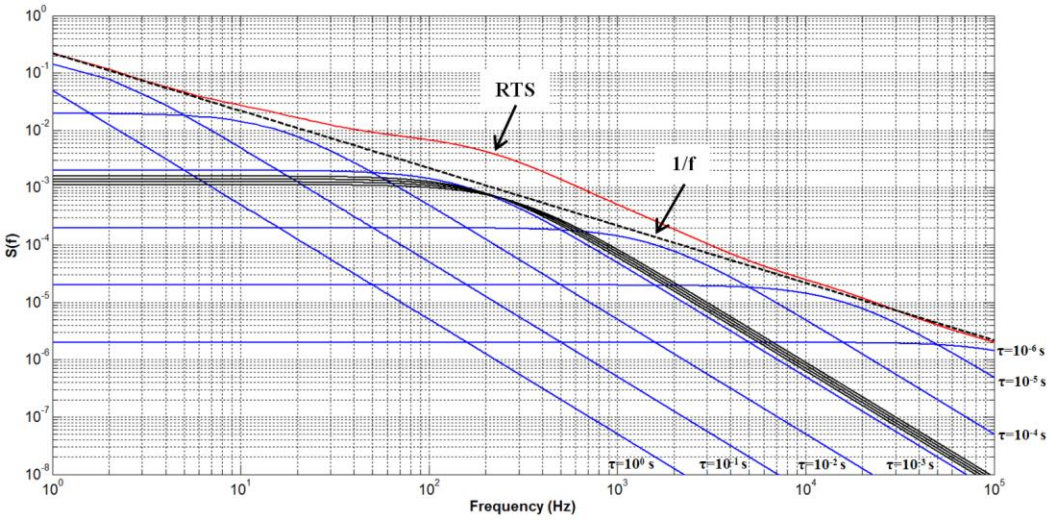

Figure 3-2: Simulation of frequency domain representation of 1/f noise with a G-R noise component due to trap RTS noise. The RTS "bump" is created by traps with $10^{-3.1}$ s $\leq \tau \leq 10^{-3.25}$ s in $10^{-0.05}$ s increments shown in black.

An example group of discrete Lorentzians with time constants of 1 s, 0.1 s, 0.01 s, 1 ms, 0.1 ms, 0.01 ms, and 0.001 ms are labeled in Figure 3-2. The

individual Lorentzians follow the trap time constant distribution $g(\tau) = 1/\tau$ which is necessary to create 1/f noise (discussed further in §3.2.4), but have additional traps between $10^{-3.1}$ s and $10^{-3.25}$ s. A summation of these spectra reveal a bump localized around $10^{-3.2}$ s. This shows that the bump in the 1/f spectrum may actually be caused by the summation of multiple traps with similar time constants that do not adhere to $g(\tau) = 1/\tau$ distribution, and that τ_{rts} does not necessarily correlate to a specific trap but a group of traps. Previous theories have stated that RTS noise is actually created by the interaction of traps where electrons move between different trap energy states [31]. As demonstrated in Figure 2-10, trap assisted tunneling through the AlGaN is likely a major contributor to gate leakage as electrons tunnel to lower energy trap states in the AlGaN before ultimately exiting the device through the drain (or source, as we will see later). If a large inverse piezoelectric force created by gate stress does cause dislocation in the AlGaN leading to new electron traps, then gate stress should also change the RTS noise. This could manifest in three ways: the appearance, disappearance, or movement in the frequency domain of an RTS noise component. The effect of stress and temperature on RTS noise is explored in more detail in §6.3.5.

3.2.4 1/f Noise

1/f noise, also called pink or flicker noise, is another type of G-R noise that occurs at low frequencies in active components and some passive components. 1/f noise is unique in that it has been observed in other biological and man-made systems such as heart beat rhythm, music, neural activity, and the stock market. The diversity of 1/f noise indicates that there are many causes even among electrical components [38]. The name is derived from the characteristic

$1/f^{\gamma}$ spectrum, where $\gamma = 1.0 \pm 0.1$ (in electronics). Mathematically, the spectrum is represented by Equation (3-11) [35], [39]. 1/f noise is typically observable at frequencies < 100 kHz and is eventually overwhelmed by thermal or shot noise at high frequencies as shown in Figure 3-3 [31].

(3-11) $$\overline{\imath^2} = K_1 \frac{I^a}{f^{\gamma}} \Delta f$$

K_1 = device constant (later redefined as the Hooge parameter)

I = DC current [A]

a = exponential relationship of DC current to noise current (constant)

γ = slope constant ($\gamma = 1$ for 1/f noise)

Δf = measurement bandwidth [Hz] (for spectral noise, $\Delta f = 1$ Hz)

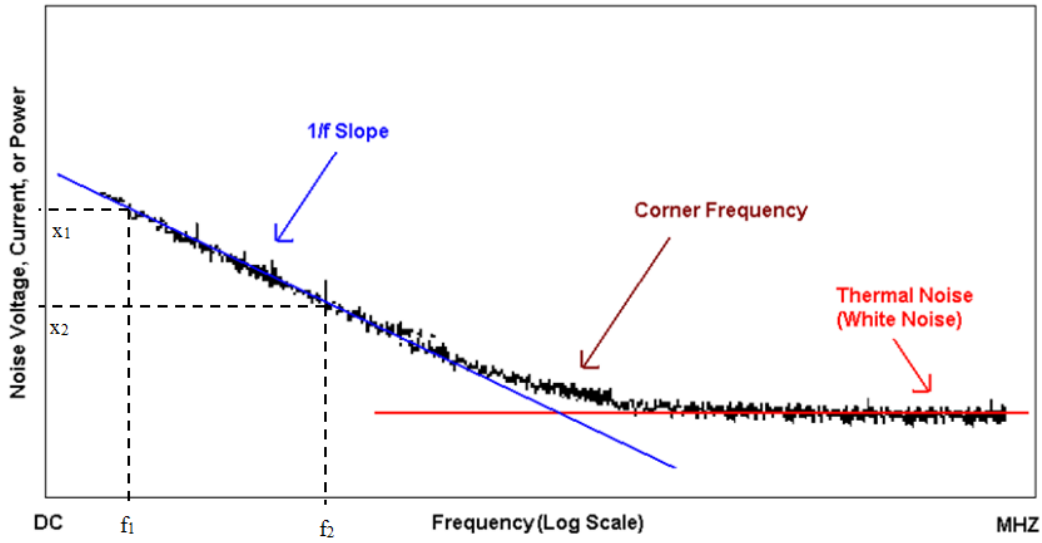

Figure 3-3: Generic 1/f Noise spectrum [39].

The 1/f noise slope factor, γ, can be found by superimposing a line on the 1/f noise on a log-log plot and using Equation (3-12) and the markers in Figure 3-3 where x_1 and x_2 are linear values.

(3-12) $$\gamma = \frac{\log(f_2/f_1)}{\log(x_2/x_1)}$$

The 1/f noise trend is thought to naturally occur in systems that have memory where the current state is dependent on the previous state or states. This is derived from the theory that 1/f noise is a nonstationary process leading to time dependent process characteristics [40]. There are conflicting theories on the physical mechanisms that cause 1/f noise in semiconductors; however, research has shown that defects in the semiconductor material's crystalline structure are most likely the source [31]. Defects can take multiple forms; imperfections in the crystalline structure, unintentional dopants that enter the material during the manufacturing process or dangling bonds due to mechanical stress. The presence of electron traps created by these defects supports the original idea that the system has memory; in the case of semiconductors, the current state is determined by whether an electron trap contained an electron or not at a previous time. Hooge postulates that 1/f noise is due to fluctuations in the material conductance, σ, defined in Equation (3-13) which leads to two theories of 1/f noise generation: carrier fluctuation, Δn, and mobility fluctuation, Δμ, theories. In GaN HEMTs, electron traps near the channel and in the AlGaN buffer are thought to create the necessary Δn fluctuations resulting in 1/f noise.

(3-13) $$\sigma = nq\mu$$

n = number of carriers

q = electron charge

μ = carrier mobility

The Δn theory of 1/f noise is supported by applying the McWhorter model for electron traps that states an individual electron trap with time constant, τ, creates a Lorentzian noise spectrum described in Equation (3-14) [29] [31]. This is the same distribution in Equation (3-10) that is used to generate RTS noise.

(3-14) $$S(f) = \frac{4\tau}{1+(2\pi f\tau)^2}$$

Similar to the RTS noise, 1/f noise is the summation of all Lorentzian spectra produce by all traps. However, 1/f noise is unique in that it requires $g(\tau) = 1/\tau$, which was not the case for RTS noise in Figure 3-2 [41]. This is mathematically verified in Figure 3-4 where five discrete τ values are selected: 100 ms, 10 ms, 1.0 ms, 0.1 ms, and 0.01 ms. The resulting spectrum (red) closely follows the ideal 1/f spectrum (it deviates at frequencies > 10 kHz because no τ values shorter than 0.01 ms are used). In this example, the required trap distribution calculated by McWhorter, $g(\tau) = 1/\tau$, satisfies the requirements to produce 1/f noise [41].

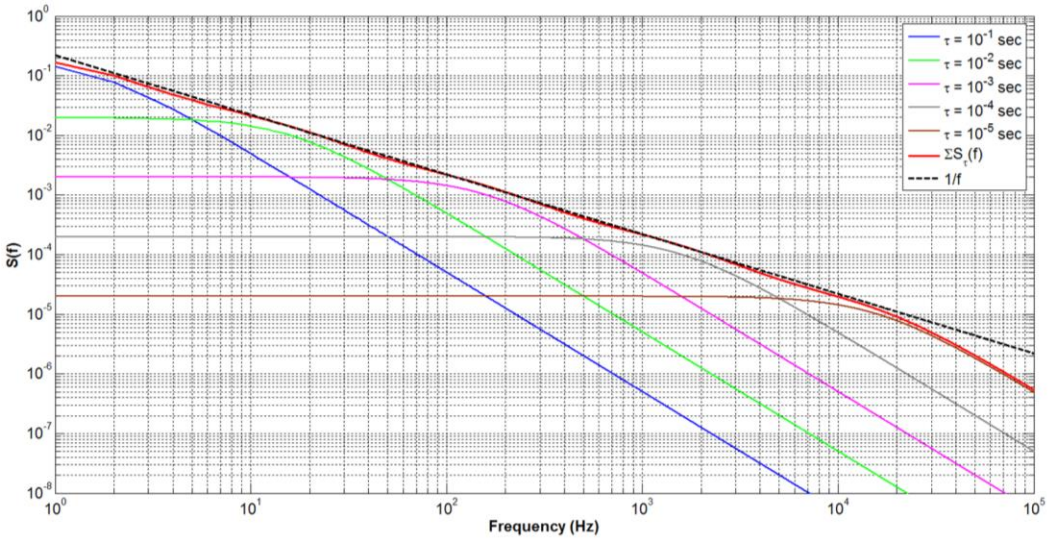

Figure 3-4: Example simulation of Lortenzian spectra with varying time constants and $g(\tau) = 1/\tau$. The resulting 1/f summation spectrum (red) closely follows the ideal 1/f spectrum (black dashed).

The Hooge parameter, α, in Equation (3-15) compares compare 1/f noise in different materials and devices [42]. This unitless parameter is calculated using the normalized noise spectrum, $S_I(f)/I^2$, or its equivalents. The Hooge parameter is a figure of merit to compare the relative material quality in different materials at different temperatures. Material defects, such as those that produce electron traps, and scattering mechanisms lead to higher α. Materials with fewer defects and less scattering have a lower α. Hooge based his equation on the idea that electrons act independently when producing 1/f noise and that 1/f noise is dependent on the frequency at which it is measured. The parameter 1/N averages the contributions from each electron. In FET devices, α is calculated with the device biased in the triode region where current is conducting through the channel. This region is selected because N can be easily calculated from C-V measurements, and the low I_{ds} current under triode bias mitigates the effects of device self-heating.

(3-15) $$\frac{S_V(f)}{V^2} = \frac{S_I(f)}{I^2} = \frac{S_R(f)}{R^2} = \frac{\alpha}{fN}$$

α = Hooge parameter

f = frequency (Hz)

N = total number of conduction electrons in the channel

The Hooge parameter is not a constant and has been shown to vary in GaN HEMTs depending on gate and drain bias [43]. Typical values for GaN HEMTs range from 10^{-4} to 10^{-2}. This figure of merit is used in this experiment to compare the relative quality of the material before and after stress.

3.3 HEMT Noise Model

Various HEMT noise models exist such as the Van der Ziel model, the Fukui model, the Kondoh model used to calculate GaN amplifier noise figure [44]. The much simpler model in Figure 3-5 introduced by Rao, et al., addresses the necessary LFN generating sources and is used in this research [43]. This noise model differs from other models in that it does not include the numerous parasitic capacitances, inductances, and other resistances that are necessary to create a functional model of the device. This model does, however, illustrate the key LFN producing locations in the HEMT. Data presented in this thesis requires a small modification of this model which is introduced in §6.1.1.

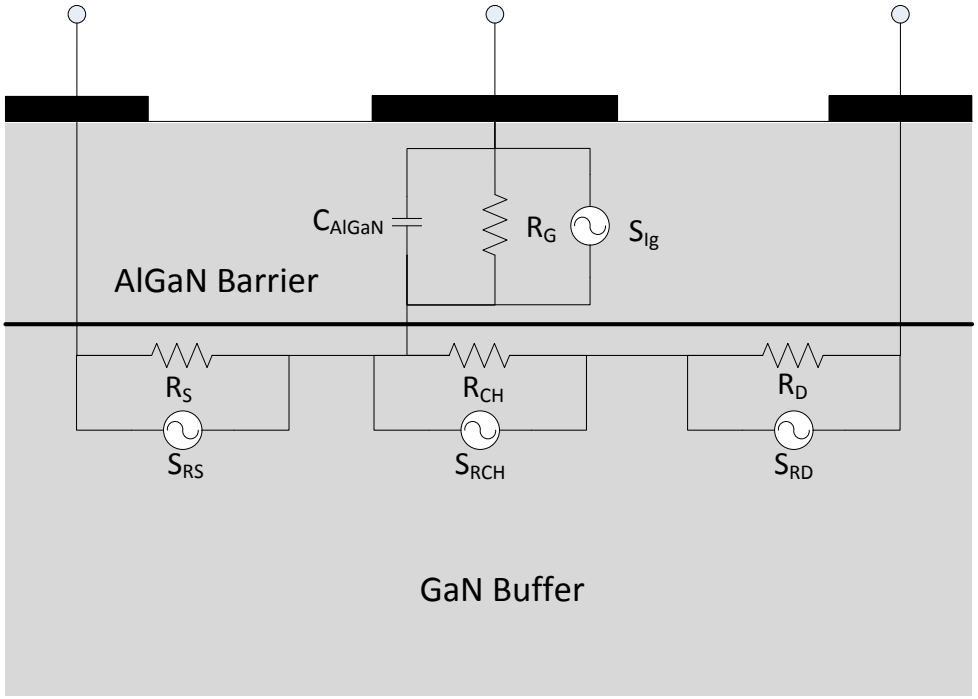

Figure 3-5: GaN HEMT noise model depicting basic LFN creating components.

The HEMT noise model in Figure 3-5 simplifies the noise generating regions into four sections. R_S and R_D represent the source and drain contact resistances and do not generate a significant amount of LFN as will be shown. An increase in R_S and R_D signifies contact degradation. R_{CH} is a variable resistance dependent on V_{gs} and is suspected of generating LFN due to traps near the 2DEG. Due to the large bandgap of AlGaN, R_G is made primarily of the AlGaN resistance. This region contains the electron traps that produce gate LFN especially under cutoff conditions. The noise producing regions will be evaluated further in §6.3.1. The next section introduces the LFN measurement circuit that amplifies the LFN.

Chapter 4: LFN Measurement Circuit

This chapter introduces the LFN test circuit used to amplify LFN. This section discusses the theory of operation, design, performance qualification, and troubleshooting methods and results. There were three pertinent versions of this circuit used to collect data. While the original test procedure involved measuring drain LFN only, data for both the gate and drain was measured by using the Version 2 design to measure the gate and Version 3 to measure the drain. Although there are some design changes (using SMT components rather than through-hole and build the circuit on a specially fabricated PCB rather than soldered to copper-clad board), the two versions are functionally the same. The GaN HEMT breakout boards used to mount the HEMTs and SMA connectors is also introduced in this chapter.

4.1 Theory of Operation

The low frequency noise test circuit was derived from a previous design for a generic FET/BJT LFN test circuit with adjustable bias and amplification [39]. This method was selected due to the low cost, simple implementation, and gate and drain bias flexibility. The circuit schematic and bill of materials are shown in Figure 4-1 and Table 4-1. Metal film resistors are used when available because they do not produce LFN like other types of resistors. The original design accommodated high currents (up to 15 mA) from the drain bias source, but this requirement was subsequently removed so lower power resistors can be used.

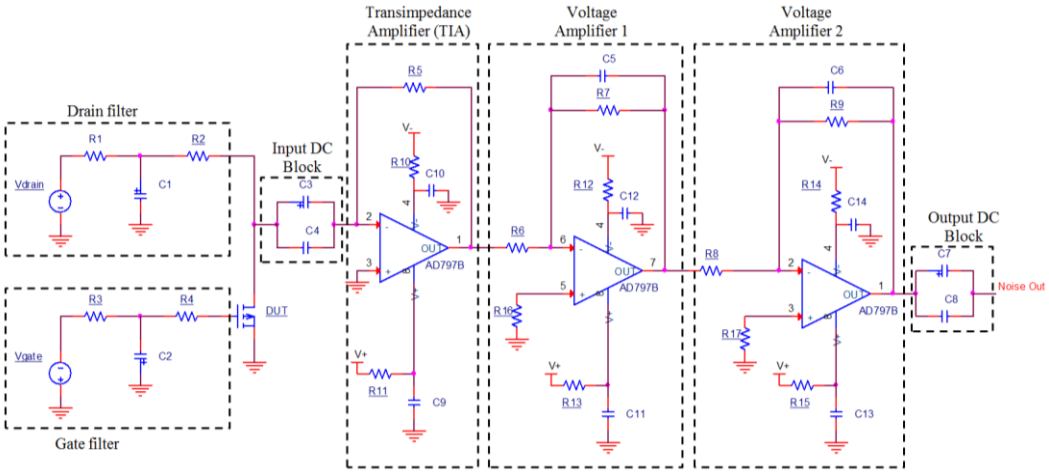

Figure 4-1: LFN test circuit schematic. Component values and descriptions are indicated in Table 4-1.

Table 4-1: LFN Test Circuit Component Values and Descriptions

Reference	Description
R1	100 Ω, 1/4 W, 1%
R5, R6, R8, R10, R11, R12, R13, R14, R15, R16, R17	100 Ω, 1/4 W, 1%, metal film
R2	500 Ω, 1/4 W, 1%
R3, R4	200 Ω, 1/4 W, 1%, metal film
C1	4700 µF, 50 V, 20%, Al electrolytic
C2	4700 µF, 10V, 20%, Al electrolytic
C3, C7	2200 µF, 25V, 20%, Al electrolytic
C4, C8	0.15 µF, 25V, 10%, ceramic
C5, C6	27 pF, 25V, 20%, Al electrolytic
C9, C10, C11	10 nF, 10V, 10%, ceramic
U1, U2, U3	AD797B Op Amp
V+, V-	6.5 V rechargeable battery

The left side of Figure 4-1 shows the gate and drain bias filters that filter power supply noise. These filters are a key part of the design because variable supply voltages generate large amounts of low frequency noise from the internal switching architectures that generate the range of voltages necessary for this testing. However, the power supplies also enable quick and easy HEMT biasing that would otherwise significantly increase testing time. The drain bias filter

requires a minimum 500 Ω resistor between the filter capacitor and the DUT to provide a high impedance path to ground for higher frequency signals. This forces the noise current produced at the drain terminal to take the lower impedance path to the amplifiers rather than the higher impedance path through the resistor and filter capacitor. The gate filter serves a dual purpose of filtering power supply noise and dampening oscillations caused by the gate terminal [18]. While the manufacturer suggests adding a 200 Ω resistor in series with the gate, it was determined experimentally that two 100 Ω resistors do not sufficiently dampen the oscillations in this application, so two 200 Ω resistors are used instead [45]. The drain and gate filter frequency response simulations are shown in Figure 4-2.

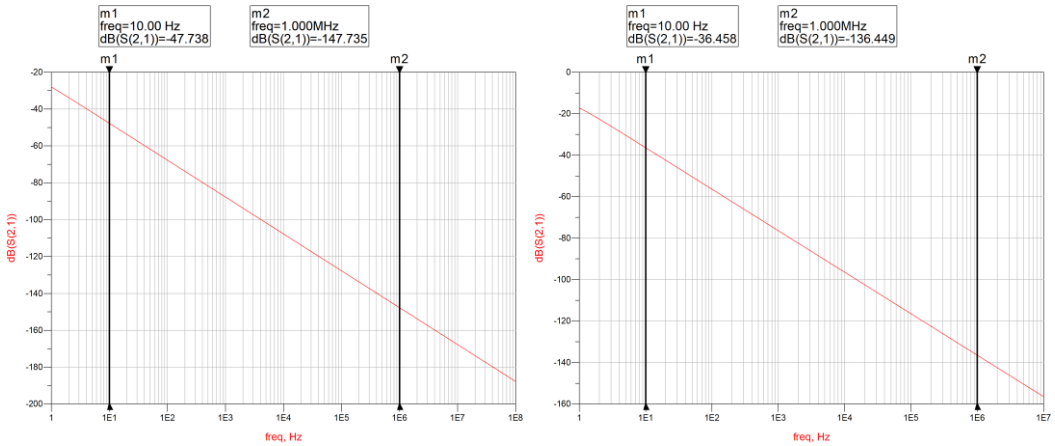

Figure 4-2: Drain (left) and gate (right) bias filter frequency response. The gate bias filter is simulated using 100 Ω resistors.

The first amplifier stage consists of a transimpedance amplifier (TIA) to convert the noise current produced by the drain and gate terminals to a voltage. Subsequent inverting op amp stages then boost the noise voltage signal further to a measureable level. It was determined that a TIA gain of 100 V/A and voltage

gain of 10 V/V per voltage amplifier is needed to boost the LFN noise signal above the noise floor of the HP 35665A Dynamic Signal Analyzer and the Agilent N9000X Spectrum Analyzer. The AD797B op amp from Analog Devices was selected due to the superior noise performance (0.9 nV/√Hz and 2 pA/√Hz) compared to other low noise op amps. This op amp meets the gain bandwidth product requirement of at least 100 MHz, can operate with a rail-to-rail supply voltage, and has low current draw (8.5 mA max). The AD797*B* was chosen rather than the AD797*A* because the lower input offset voltage (10 μV compared to 25 μV) improves op amp sensitivity when dealing with small signals. The op amps are supplied by rechargeable 6.5V batteries to prevent additional noise from entering the system. A comparison of potential op amps and the key performance specifications is shown in Table 4-2.

Table 4-2: Summary of Low Noise Op Amps

	AD797B	**AD8597**	**LMH6624**	**LME49990**	**LT6200**
Input Voltage Noise (nV/√Hz)	0.9	1.1	0.92	0.9	1.1
Input Current Noise (pA/√Hz)	2.0	4.2	2.3	2.8	2.2
Gain BW Product (MHz)	110	10	95	110	165
Slew Rate (V/μs)	20	16	400	22	42
Max Rail Voltage (V)	± 15	± 15	± 6	± 18	± 6

DC blocks consisting of a parallel 2200 μF electrolytic capacitor and 0.15 μF ceramic capacitor are included before and after the amplifier stage. The

first DC block ensures proper biasing of the DUT and prevents a DC voltage from saturating the amplifiers. The second DC block ensures any stray DC voltage does not inadvertently damage the measurement equipment input ports. The original design includes DC blocks between each amplifier stage, but they were removed in subsequent versions because they were deemed unnecessary.

4.2 Amplifier Noise Calculations

The equivalent noise from an Op Amp circuit is calculated by inserting the equivalent noise model in Figure 4-3 into the circuit and calculating the noise contribution of each noise source at the output (or input) using superposition [46]. When calculating each noise component (see Equations (4-2) to (4-6)) the other components are assumed to be noiseless (for instance, when calculating thermal noise produced by the R_1, the feedback resistor R_f and op amp are assumed to be noiseless).

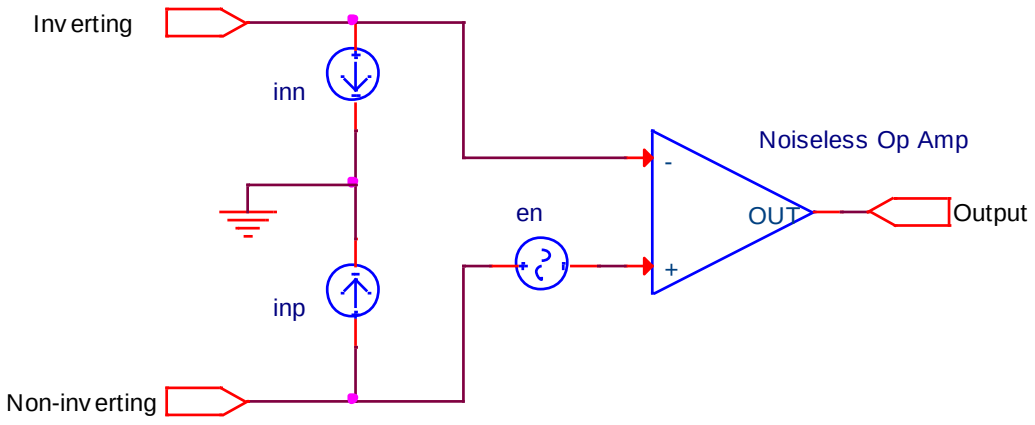

Figure 4-3: Op Amp noise model with two noise current sources at each input (i_{nn} and i_{np}) and a noise voltage source at the non-inverting terminal (e_n).

The AD797B Op Amp is assembled in the inverting Op Amp circuit configuration using $R_1 = 100\ \Omega$ and $R_f = 1\ k\Omega$. The entire circuit with noise sources is shown in Figure 4-4. For these calculations, it is assumed that each noise source is independent. A resistor produces primarily thermal (or Johnson) noise and is calculated using Equation (4-1) for voltage noise where k is Boltzmann's constant, $1.38 \cdot 10^{-23}$ m^2kg/s^2-K, T is the temperature (297 K at room temperature), and R is the resistor value. Using superposition, the noise contributions from each source are calculated using Equations (4-2) through (4-6) [46]. The resulting noise components for the input resistor (E_1^2), feedback resistor (E_f^2), inverting terminal (E_{nn}^2), non-inverting terminal (E_{np}^2), and input differential (E_n^2) noise are represented as power spectral densities referred to the op amp output. The total output noise spectral density referenced to the output, E_{Tot}^2, and the noise floor, N_v, are calculated using Equations (4-7) and (4-8).

(4-1) $$\overline{e_R^2} = 4\text{kTR}\ [V^2/Hz]$$

(4-2) $$E_1^2 = \overline{e_1^2}\left(\frac{R_f}{R_1}\right)^2\ [V^2/Hz]$$

(4-3) $$E_f^2 = \overline{e_f^2}\ \ [V^2/Hz]$$

(4-4) $$E_n^2 = \overline{e_n^2}\left(\frac{R_1+R_f}{R_1}\right)^2\ \ [V^2/Hz]$$

(4-5) $$E_{np}^2 = \overline{\imath_{np}^2}(R_3)\left(\frac{R_1+R_f}{R_1}\right)^2\ \ [V^2/Hz]$$

(4-6) $$E_{nn}^2 = \overline{i_{nn}^2}(R_f)^2 \ [V^2/Hz]$$

(4-7) $$E_V = \sqrt{E_1^2 + E_f^2 + E_n^2 + E_{np}^2 + E_{nn}^2} \ \left[V/\sqrt{Hz}\right]$$

(4-8) $$N_V\ (dBm) = \ 10 \cdot \log(E_{Tot}^2 \times 1000) \ \ [dBm/Hz]$$

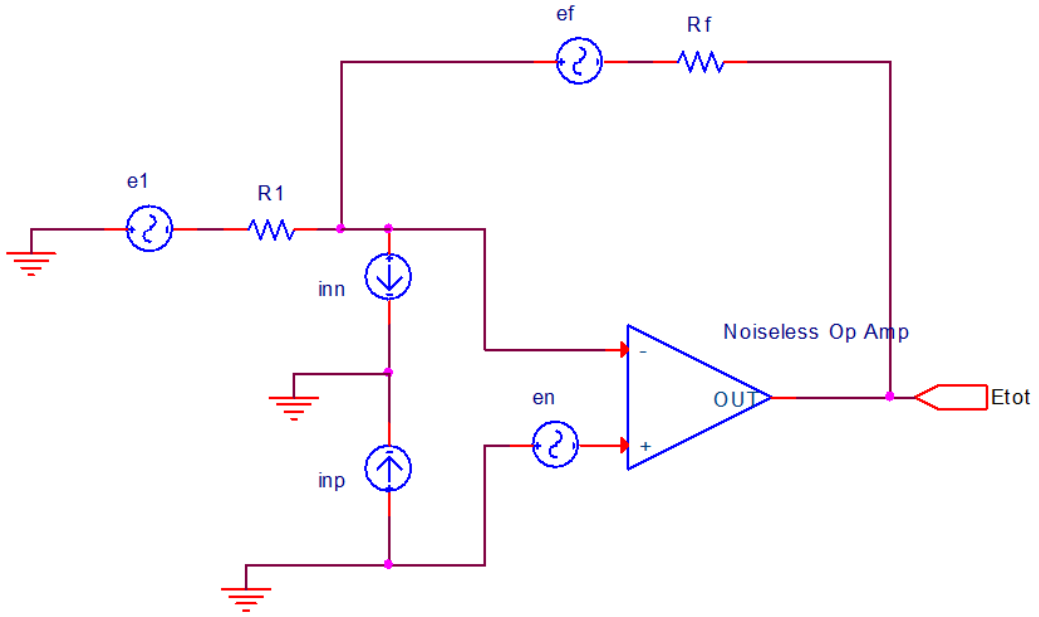

Figure 4-4: Inverting Op Amp configuration with noise sources.

The noise produced by a single transimpedance amplifier and a single voltage amplifier is summarized in Table 4-3. For two cases where the voltage amplifiers have a gain of 10 V/V, the op amp noise model shows that reducing the inverting op amp resistor values also reduces the total output noise generated by the circuit. Equation (4-9) calculates the total output noise from the amplifiers assuming no input noise. By reducing the resistor values by a factor of 10, the theoretical inverting amplifier noise floor decreases from 433.7 nV/√Hz

(-127.3 dBV_{rms}/Hz) to 220.0 $nV/\sqrt{Hz}$ (-133.2 dBV_{rms}/Hz). The AD797B datasheet specifications also state that $R_1 < 1\ k\Omega$ for optimal noise performance. As a result, the final inverting op amp configuration uses $R_1 = 100\ \Omega$ and $R_f = 1\ k\Omega$.

Table 4-3: Noise Calculations for the Transimpedance and Voltage Amplifiers

Noise Source	**Transimpedance Amplifier (V^2/Hz)**	**Voltage Amplifier (V^2/Hz) (R_1 = 1000, R_f = 10000)**	**Voltage Amplifier (V^2/Hz) (R_1 = 100, R_f = 1000)**
E_1^2	0	$1.639 \cdot 10^{-15}$	$163.9 \cdot 10^{-18}$
E_f^2	$1.656 \cdot 10^{-18}$	$163.94 \cdot 10^{-18}$	$16.39 \cdot 10^{-18}$
E_n^2	0	$98.01 \cdot 10^{-18}$	$98.01 \cdot 10^{-18}$
E_{np}^2	0	≈ 0	≈ 0
E_{nn}^2	$40 \cdot 10^{-27}$	$400.0 \cdot 10^{-18}$	$4.0 \cdot 10^{-18}$
E_{Tot}^2	$1.656 \cdot 10^{-18}$	$2.30 \cdot 10^{-15}$	$2.82 \cdot 10^{-16}$

(4-9) $$E_{Out} = \sqrt{(E_{TIA}^2 A_V^2 + E_V^2)A_V^2 + E_V^2}\ \ [V/\sqrt{Hz}]$$

The values in Table 4-3 are ideal noise calculations based on the manufacturer's datasheet. Figure 4-5 shows measured noise data from the measurement equipment and the amplifier stage with connected power supply. The data shows that the actual noise floor is slightly higher than the theoretical noise floor at 620 $nV/\sqrt{Hz}$ or 9.1 dB above the calculated noise floor. Added noise from the op amps and radiated noise from the wires connected to the batteries likely raises the noise floor. This deviation from expectation does not negatively affect the performance, however, because LFN is typically observed to be >500 $nV/\sqrt{Hz}$ at the amplifier output.

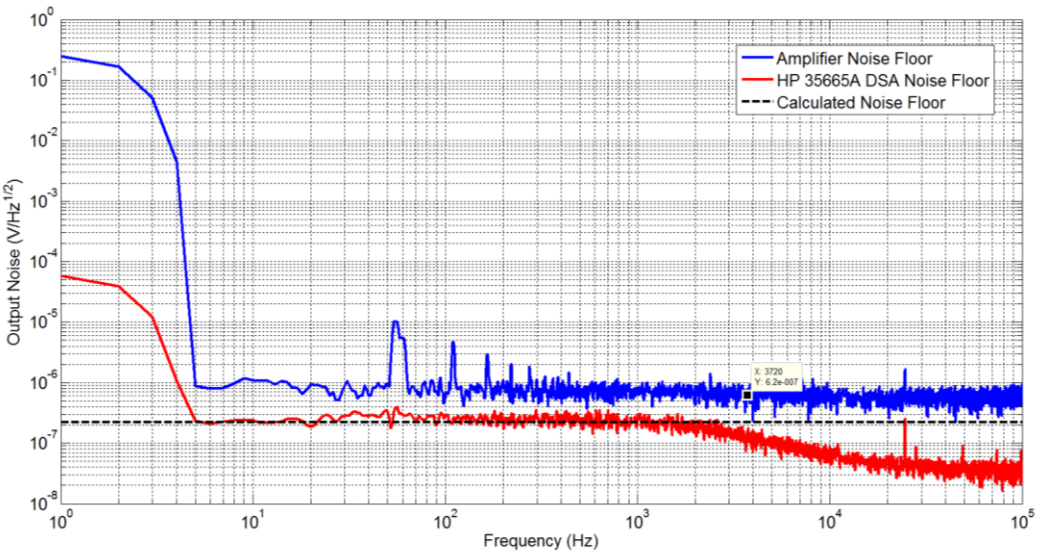

Figure 4-5: Theoretical and experimental amplifier output noise spectral density.

4.3 Iterations and Final Design

Three LFN test circuits were made; the first was done on perforated board (Figure 4-6), the second (Figure 4-7 and Figure 4-8) was made on double sided copper clad board, and the final board was manufactured on an FR4 PCB (Figure 4-9 and Figure 4-10).

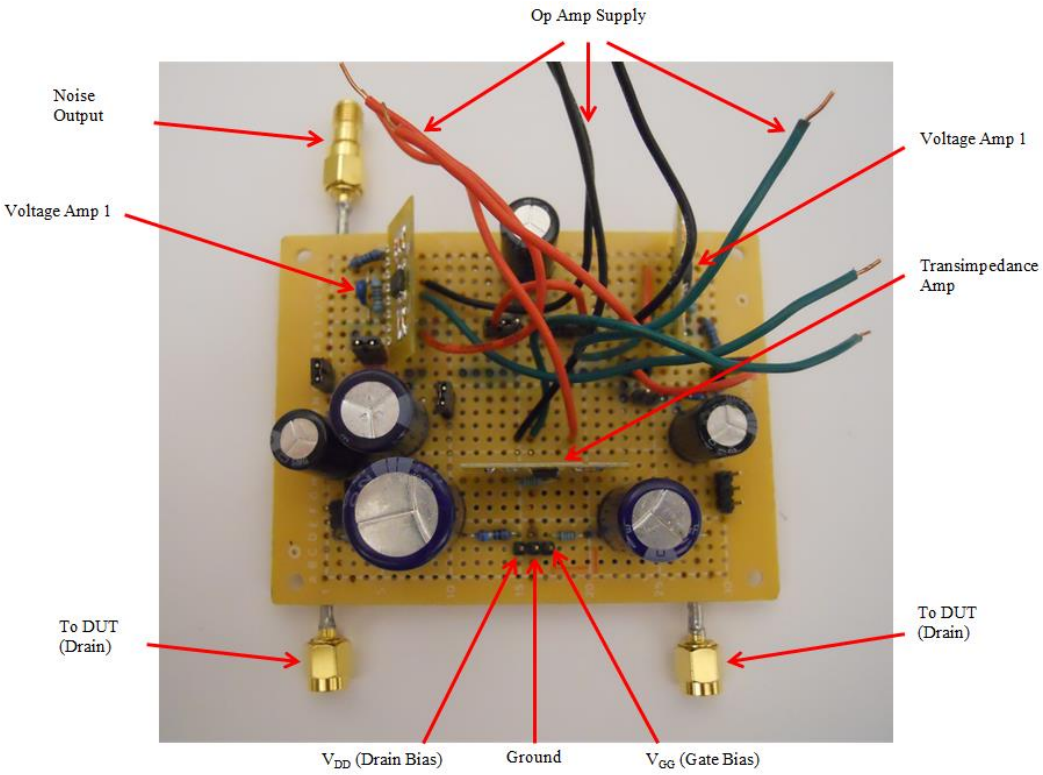

Figure 4-6: Version 1 LFN test board.

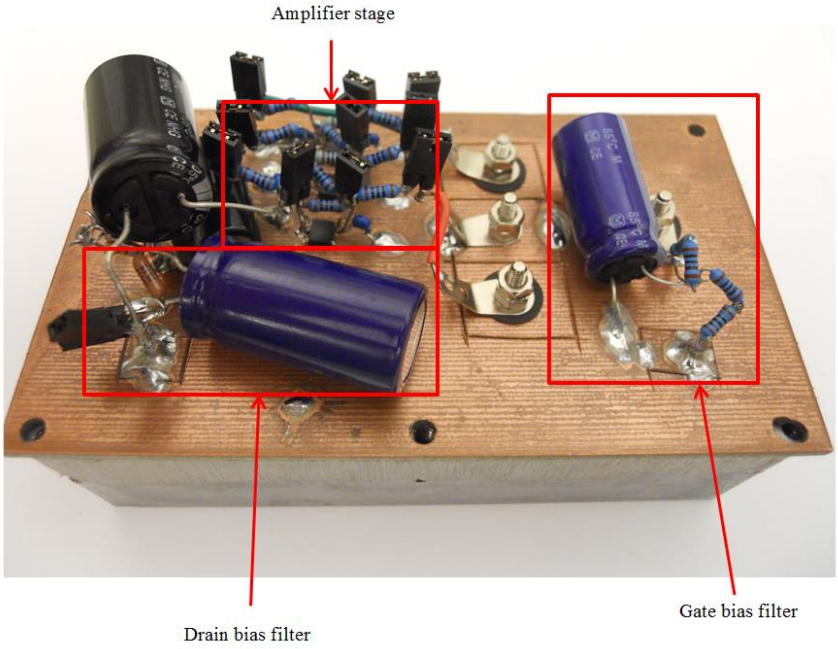

Figure 4-7: Component side of the Version 2 LFN test circuit. The circuit is essentially the same as Version 3, and was used to collect gate LFN data during testing.

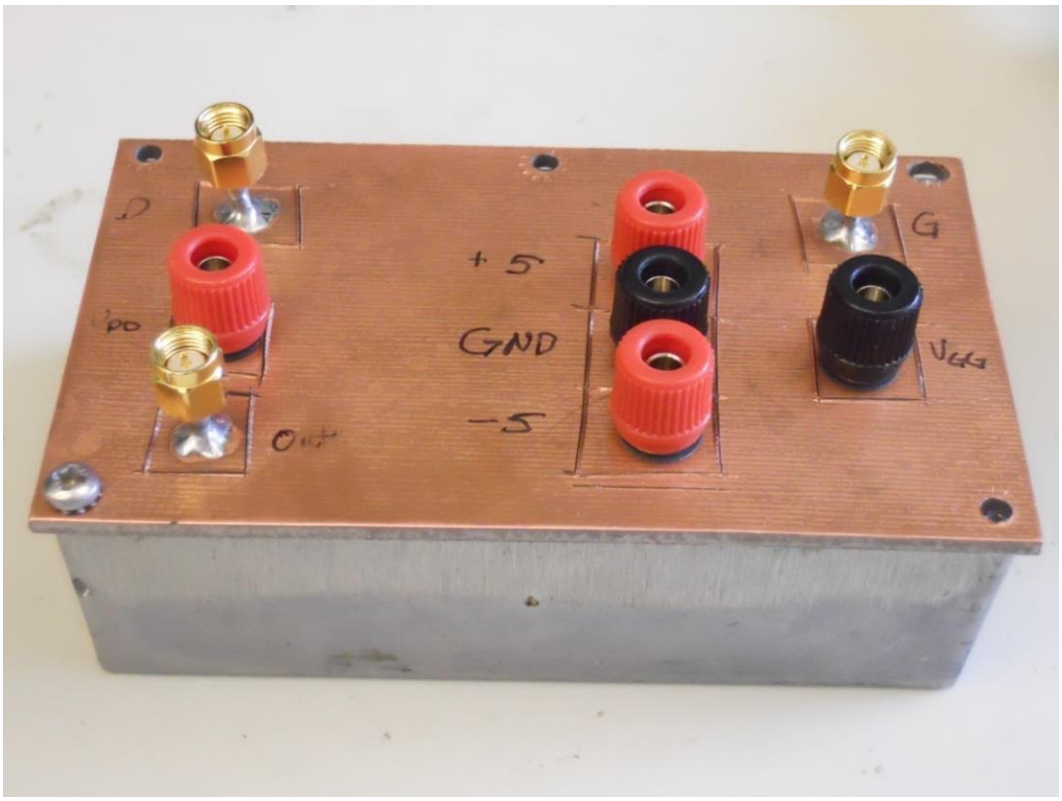

Figure 4-8: Connector side of the Version 2 LFN test board with aluminum cover.

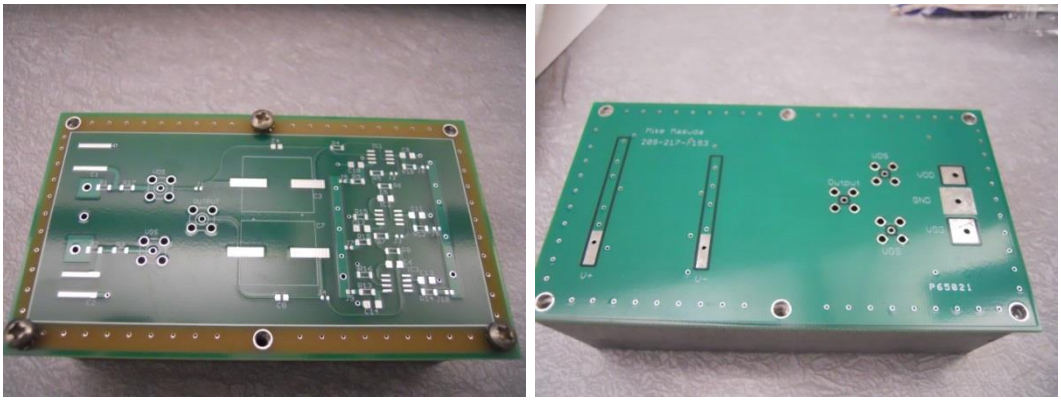

Figure 4-9: Unpopulated component side (left) and connector side (right) of Version 3 and final LFN test board.

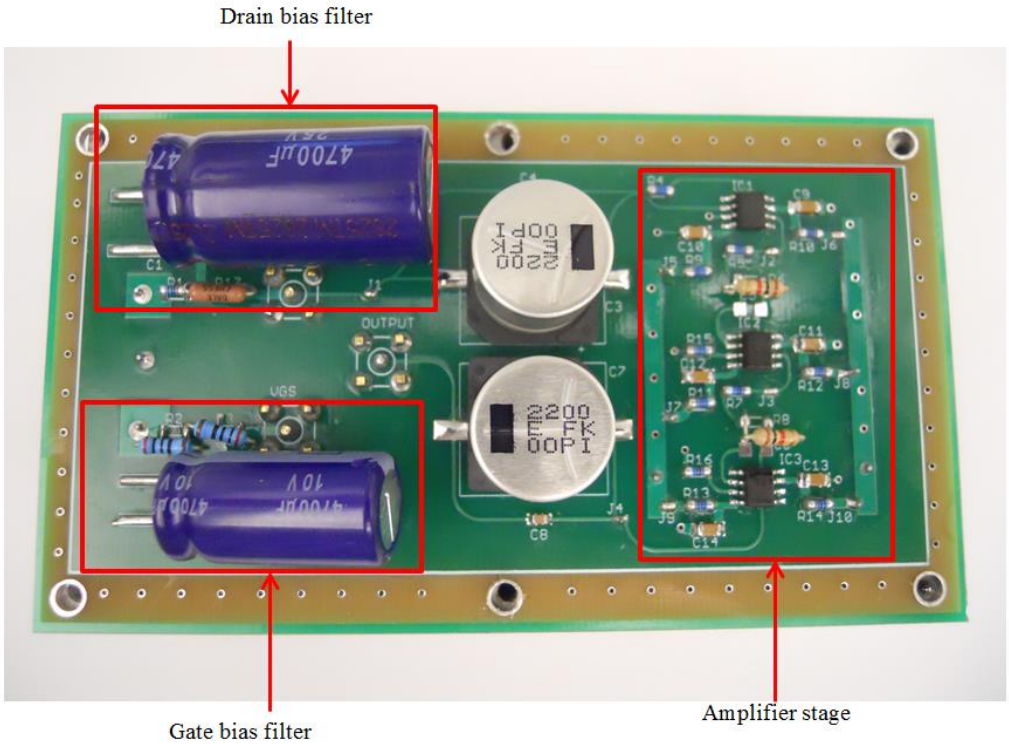

Figure 4-10: Populated component side of the Version 3 LFN test board.

The final component values are included in Table 4-1 with part numbers referenced to Figure 4-1. Improvements from Version 1 to Version 3 are highlighted in Table 4-4. One of the major changes from Version 1 to Version 2 is the addition of an RC filter at each of the op amp supply inputs to provide additional noise attenuation. Op amp power supply source noise is discussed in more detail in §4.4.1. Lastly, an aluminum shield, shown in Figure 4-8, was added to prevent radiated noise from interfering with the LFN measurements and to protect the circuit.

Table 4-4: Description of Changes from Version 1 to Version 3

Change	Original	Description/Purpose
Copper clad board/FR4	Perforated board	• Improved noise shielding. • Easily accessible ground plane • Easy surface for soldering and construction.
Op Amp power supply filter	None	• A simple RC low pass filter located as close as possible to the op amp +/- supply pins. • Filters any excess noise produced by the source or received by the leads.
EM Shielding	None	• Aluminum shield that covers the entire circuit. • Blocks noise radiated from other sources.
Op Amp non-inverting terminal resistor	None	• Added 82 Ω resistor to the voltage op amp non-inverting terminal which is approximately equal to the parallel combination of the inverting terminal resistors. • Provided better current balance for the op amp input terminals.
DC Blocks between amplifiers removed	Present	• DC blocks between op amp stages were found to be unnecessary. Introduced loss as low frequencies and are not needed to block DC offset. • Removed from design.
Gate bias filter resistors	100 Ω resistors	• Replaced with 200 Ω resistors. • Experimentally found that 100 Ω resistors were not sufficient to dampen gate oscillation.

Version 3 of the LFN Test Board contains the same component values as the previous iteration with some through hole components replaced with SMT components. Version 3 contains three SMA connectors for DC biasing and AC signal input and output. There are five pads with through hole connectors to supply op amp power, HEMT bias power, and system ground. The top side of the board (Figure 4-9, right) is completely covered in copper except at power supply points to provide additional shielding from outside noise. Like Version 2, this iteration is also covered by an aluminum shield during testing to limit the effects

of radiated noise. On the bottom side, plated vias and screw holes surround the perimeter of the board to provide a ground contact for the aluminum shield.

4.4 Verification and Characterization

Verification was performed at the sub-circuit and then at the circuit level. As previously mentioned, LFN is typically < 100 kHz, but to ensure that all the LFN data is collected, the LFN test circuit was designed and verified up to 4 MHz. First, the op amp currents were individually measured to ensure they met their specification (8 mA typical). Next, each sub-circuit (TIA, voltage amplifiers, and DC blocks) were characterized individually from DC to 4 MHz using the basic setup shown in Figure 4-11. To calculate the sub-circuit gain at low frequencies, a sine wave input was applied to the circuit and the output amplitude was measured. At low frequencies, the Agilent 33220A Function Generator was used as the source and a digital multimeter (DMM) was used to measure the output AC RMS voltage. However, at about 100 kHz, the Function Generator waveform becomes too distorted, so a Fluke 6060B Synthesized RF Signal Generator is used instead. The DMM also cannot measure AC RMS voltages at high frequencies, so an Agilent DSO1052B Oscilloscope is used to display the waveform and manually measure the output waveform amplitude. Both the Agilent 33220A and Fluke 6060B were verified to have 50 Ω source impedances which was utilized when characterizing the TIA where the input signal is connected to the op amp virtual ground.

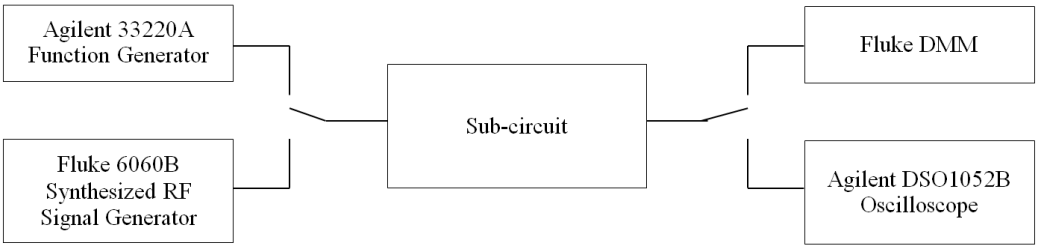

Figure 4-11: Sub-circuit test block diagram.

The resulting stages are multiplied together to get a complete characterization of the low noise amplifier stage including the DC blocks. The transimpedance gain for the Version 3 LFN test board is shown in Figure 4-12. With a TIA theoretical gain of 100 V/A and two voltage amplifiers with a combined 100 V/V theoretical gain, the expected system gain is 10000 V/A. The actual gain is approximately 12500 V/A. This deviation is most likely due to non-idealities in both the op amp and the external resistors that produced a slightly higher voltage gain. The measured gain is acceptable, however, because a gain of precisely 10000 V/A is not necessary; the gain only needs to be sufficiently high to overcome the measurement device noise floor. A completely flat gain response over the requisite frequency range is also not necessary because the LFN test circuit gain is eventually removed in data post-processing to convert the amplifier output noise to input noise from the DUT. The amplifier 3 dB cutoff occurs at approximately 2.5 MHz which exceeds the typical cutoff frequency of 100 kHz for LFN. The sharp decrease in gain < 10 Hz is due to the DC blocks and is also removed during data post-processing.

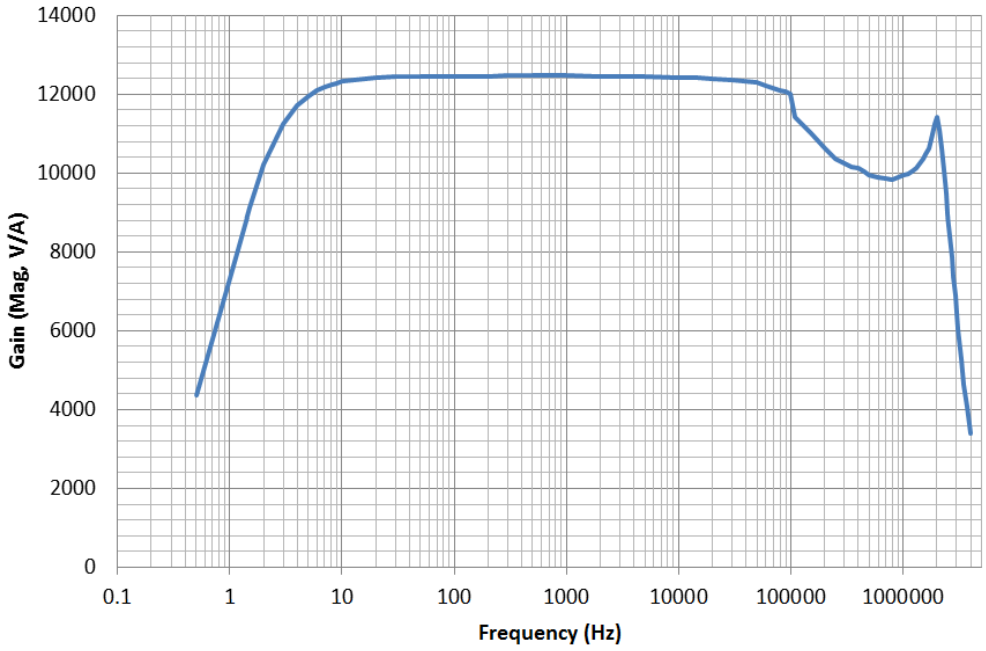

Figure 4-12: LFN test system transimpedance gain.

4.4.1 Troubleshooting

One major problem that occurred in the Version 1 design was op amp power supply noise. To get power to the op amps, two unshielded cables of approximately 2.5 feet were used per supply (the first went from battery to ammeter and the second from ammeter to test board). Initial measurements using the HP35665A showed no problems with the amplifier stage with an avalanche noise input. However, when the Agilent N9000X was connected, the amplifier output amplitude was much higher (around 3 V_{pp}) as shown in the oscilloscope capture in Figure 4-13 causing the final op amp to draw around 26 mA instead of the rated 8.5 mA maximum. The N9000X, which has a 50 Ω input impedance, created a low impedance for the noise signal as compared to the high impedance (>10 MΩ) HP35665A input impedance causing the op amp to oscillate and the supply currents, I^+ and I^-, to increase.

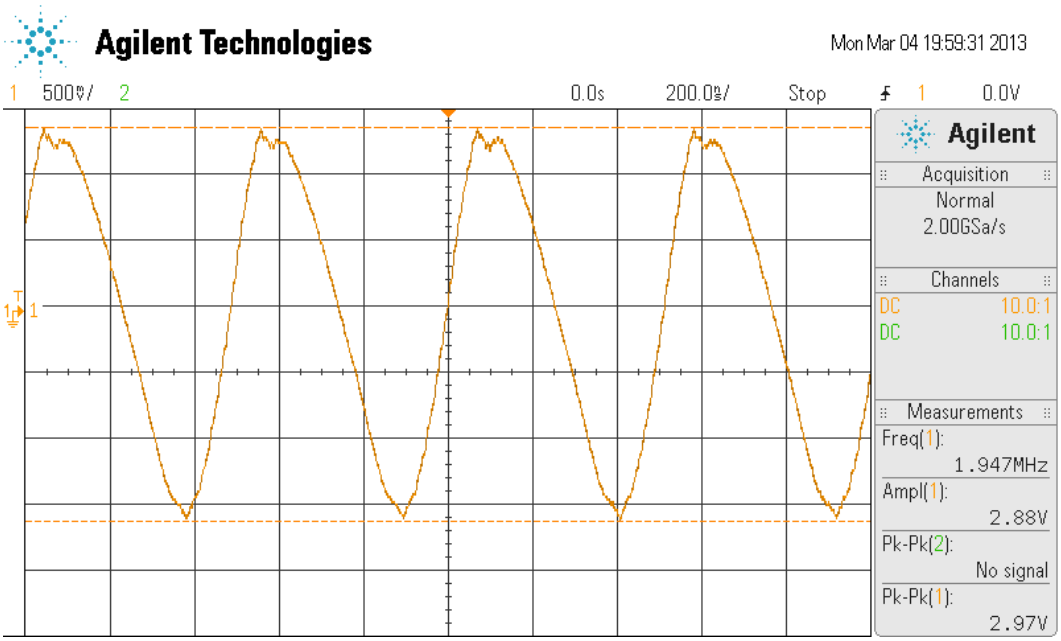

Figure 4-13: Amplifier output with long leads shows a 2.97 V_{pp} output voltage with an avalanche noise input.

To fix this issue, the op amp power supply lead lengths were reduced from approximately 5 feet to approximately 8 inches. This reduced the output noise to <50 mV_{pp} as shown by Figure 4-14 and also caused I^+ and I^- to decrease to rated values. The cause of this problem is likely due to noise being received by the unshielded power leads. The noise is injected into the op amp power rails and then amplified at each stage to produce a large noise signal at the output that causes an oscillation in the final op amp. By reducing the noise from the supplies, the output noise is reduced and the DC current drawn from the batteries decreases to the rated levels. Subsequent implementations of the circuit minimized op amp supply lead lengths, and the final circuit was implemented on a custom PCB with sufficiently short op amp supply trace lengths. The RC low pass filters were added close to the op amp supply pins to remove any leftover noise from supply lines.

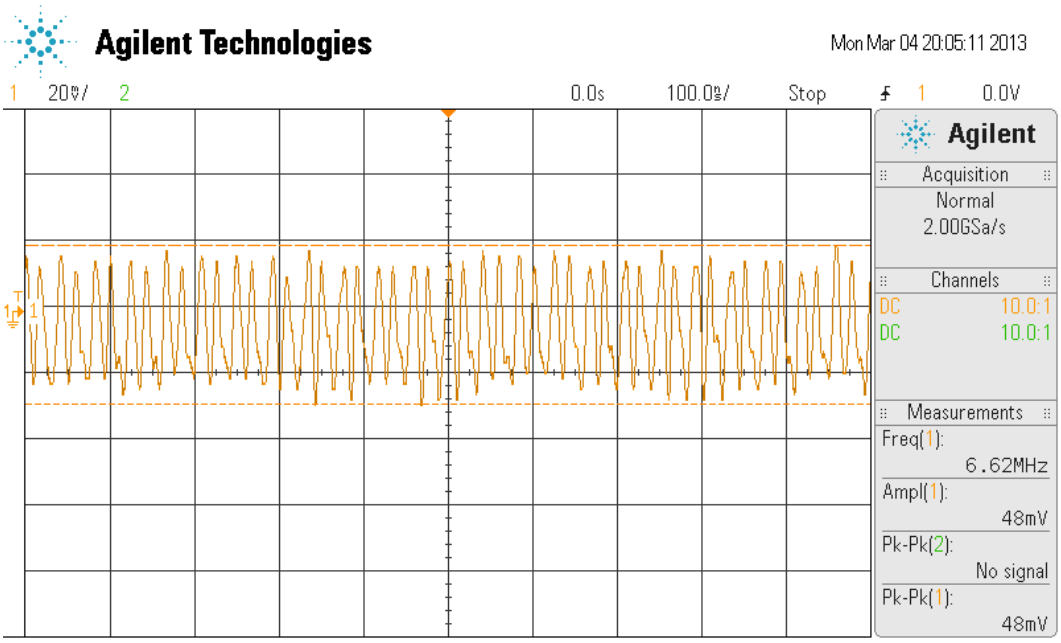

Figure 4-14: After reducing the op amp supply lead lengths, the noise signal is reduced to approximately 48 mV_{pp}.

One unresolved problem with the final design is failure of the TIA. During the first phase of LFN testing, a high current, high voltage (I_{ds} = 10 mA and V_{ds} = 15 V) was applied to the DUT that resulted in consistent failure of the drain LFN test circuit TIA. After troubleshooting, the AD797B in the TIA was found to be permanently damaged, so the part was replaced. This failure occurred three consecutive times under these test conditions. The root cause was not determined, but the test under these bias conditions was eventually removed since it was not critical. No other TIA failures occurred after removing this test. This problem only occurs on the drain LFN test circuit and may be due to transient voltages that occur when the drain voltage is suddenly increased or decreased when transitioning between biasing states. These transients may exceed the rated op amp input terminal voltage or current ratings resulting in op amp failure. Since this problem was easily detected, had a binary state (either the device works

or it does not), and was easily fixed, it was concluded that the problem does not affect the LFN measurements, and no additional fault analysis was performed.

4.5 HEMT Breakout Board

The HEMT breakout boards are designed to be economical, easily assembled and physically compatible with Version 3 of the LFN test board. As shown in the populated and unpopulated boards in Figure 4-15 and Figure 4-16, the boards contain pads for an 8 pin SOIC package HEMT with the source pad on the bottom of the package. There are two through hole SMA connector slots with spacing that matches the Version 3 LFN test board as shown on the right side of Figure 4-9. Two additional through holes are included on the gate and drain traces to accommodate voltage measurements near the DUT pins during testing. Vias are placed sporadically near the HEMT source pad to facilitate heat transfer to the opposite side of the board. Larger screw holes in the corners allow for a heat sink to be attached for temperature stabilization as necessary during testing.

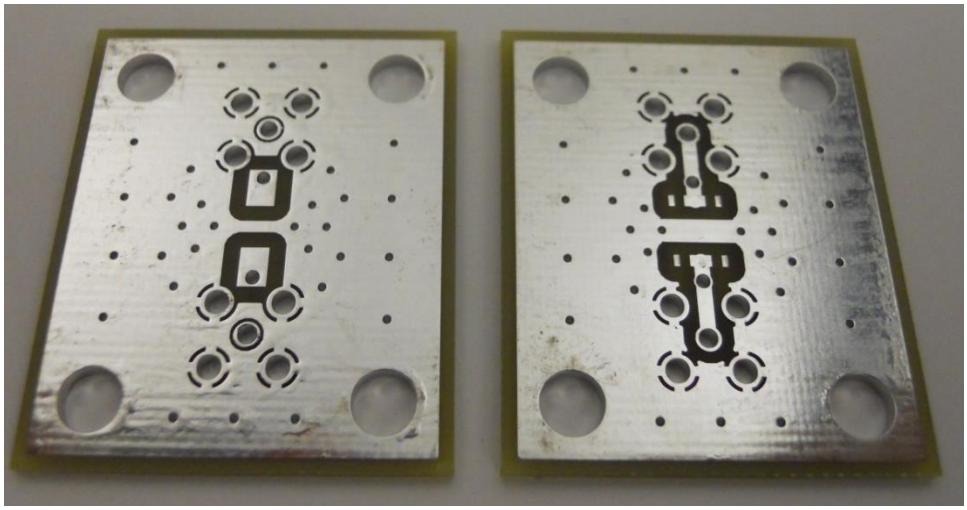

Figure 4-15: Bare HEMT breakout board Version 1.

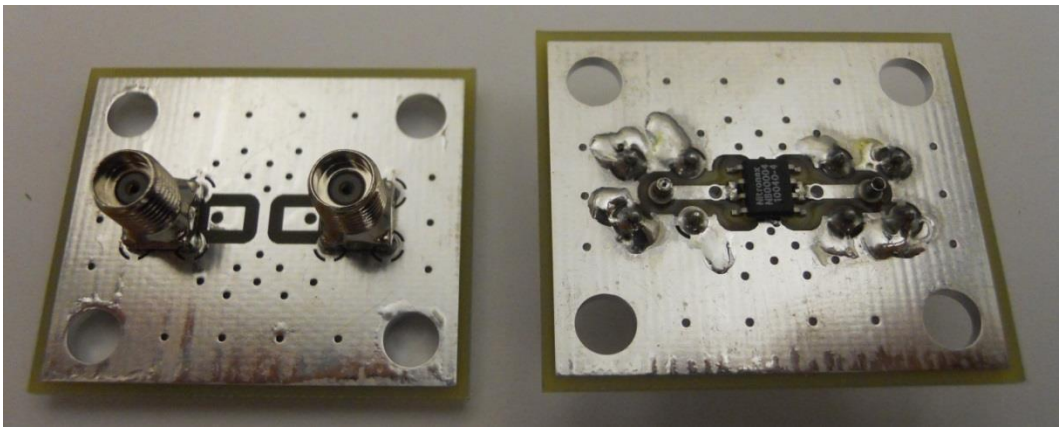

Figure 4-16: Populated HEMT breakout board Version 1.

4.5.1 Future Improvements

While the final LFN test board was tested and verified to perform correctly, some improvements on performance and usability are listed as follows:

- Determine the source of the TIA op amp failure as described in §4.4.1. This may involve replacing the AD797B with a different op amp or protecting the op amp
- Adjust the DC voltage inputs (bias power supplies and op amp supplies) to create a single cable assembly to improve testing efficiency and reduce wire clutter.
- Improve SMA connector spacing to make connecting cables easier and prevent output noise cable and DUT breakout board from interfering (See Figure 4-9).
- Layout the gate and drain amplifier circuits on the same PCB by improving the layout space efficiency or increasing the PCB size.
- Encase the DUT and breakout board inside the existing aluminum box.

- Add voltage measurement pins to the HEMT breakout board for easy access and quicker measurements.

The LFN amplifier circuit is the most crucial part to the experimentation. The next section describes the experiment background and procedure

Chapter 5: Experiment Background and Procedure

5.1 Measurement System Overview

The block diagram in Figure 5-1 shows the LFN test system block diagram. Several instruments were assembled to form the complete LFN measurement and DC characterization system. To optimize test efficiency, a majority of the test equipment is controlled using Agilent VEE v9.3. This section highlights the test equipment and set up used to perform the necessary measurements.

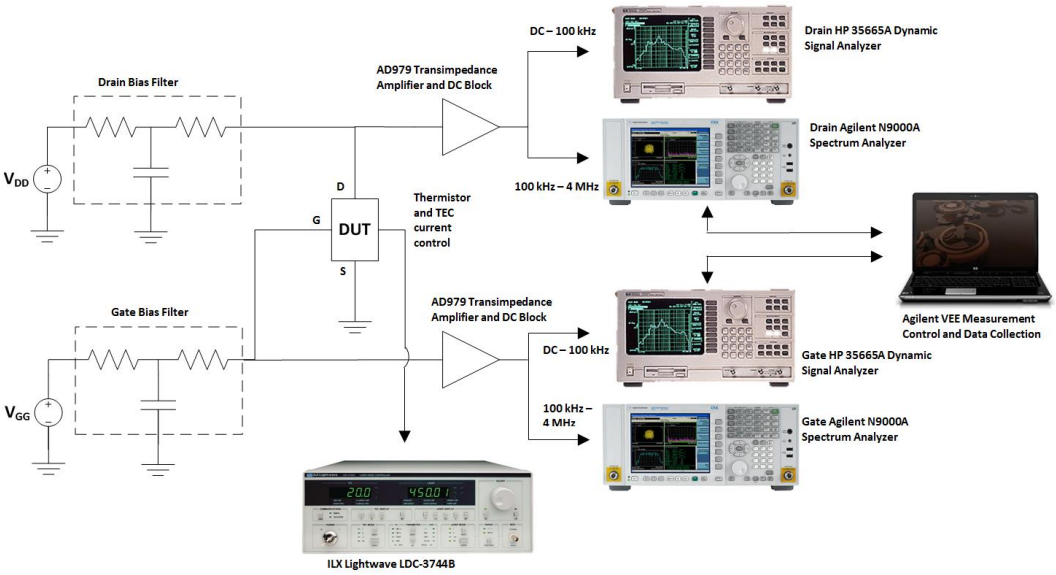

Figure 5-1: LFN test system block diagram.

5.1.1 Measurement Equipment

Three main pieces of test equipment were used to collect data: the HP4155A Semiconductor Parameter Analyzer (SPA), the HP 35665A Dynamic Signal Analyzer (DSA), and the Agilent N9000A Spectrum Analyzer (SA). The HP4155A SPA is capable of quickly sweeping output voltage to bias the device under test (DUT) at various states while simultaneously measuring the current

from each output. The unit is configured to automatically sweep V_{gs} and V_{ds} to produce a complete family of I_{ds} vs. V_{ds}, I_{ds} vs. V_{gs}, transconductance, g_m, vs. V_{gs}, and I_g vs. V_{ds} curves. This data is used to determine safe operating voltage, ensure output power does not exceed device specifications, set specific bias values for the LFN tests, and compare pre- and post-stress DC device characteristics. The test process is described in more detail in §5.2 and the results are presented in §6.1. The HP 35665A DSA and Agilent N9000A SA are used together to collect LFN data from the LFN Test Board. The DSA is an FFT based device capable of converting a voltage time domain signal into a frequency spectrum from DC to 100 kHz. The DSA performs the majority of the LFN data collection. The SA records the power spectrum from 100 kHz to 4 MHz. The upper frequency bound is selected to ensure all pertinent LFN data is collected. However, a majority of the results presented in this thesis are <100 kHz. The raw voltage (dBV_{RMS}) and power (dBm) measurements are converted in Microsoft Excel to the necessary units. Two sets of DSAs and SAs are used to measure the gate and drain noise simultaneously. During LFN measurements, accurate DUT temperature control is required to perform the experiment (See §5.4). To do this, the ILX Lightwave LDC-3744B Laser Diode Controller is used to control a thermoelectric cooler (TEC) unit. The LDC-3744B monitors the DUT temperature using a thermistor and varies the TEC current to adjust the temperature. A more detailed description is included in §5.4.2. The HP 6555A DC Power Supply, capable of reaching voltages up to 110 VDC, is used to perform the gate stress tests. Finally, two digital DMMs are used to record

voltage and current measurements as necessary. An illustration of the LFN laboratory test setup is shown in Figure 5-2.

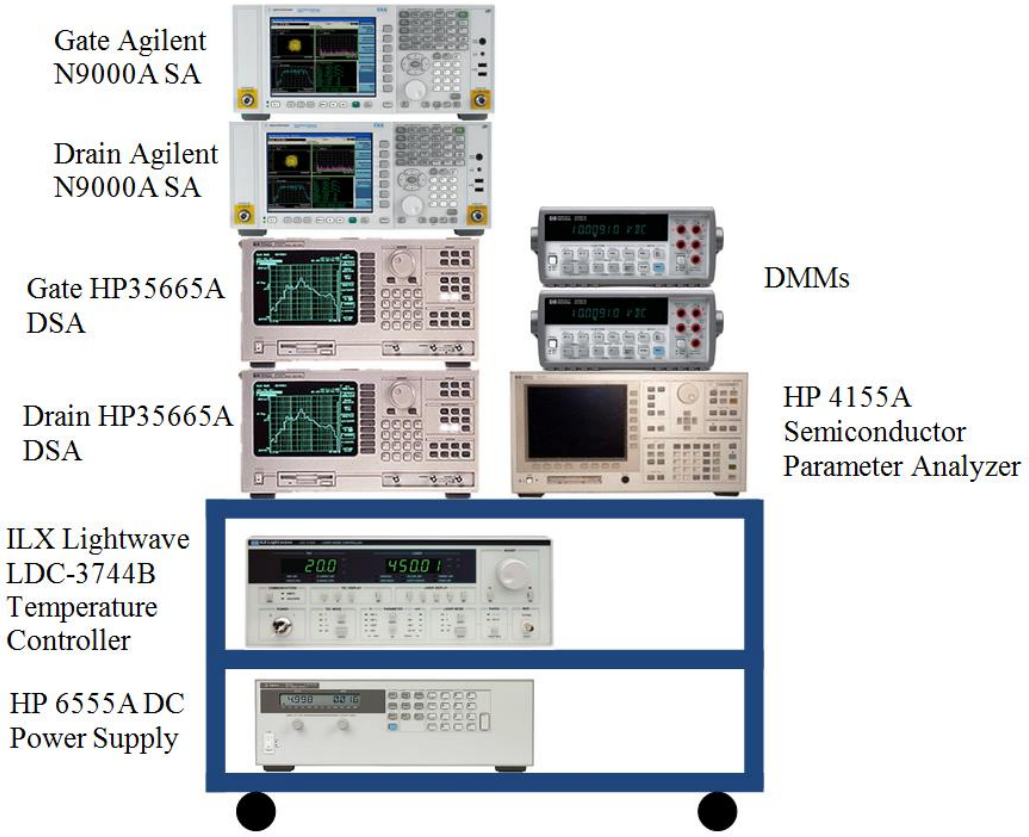

Figure 5-2: LFN and DC characterization stress test equipment.

5.1.2 Measurement Equipment Capability

Prior to collecting any LFN data or DC characteristic data, the measurement equipment must first be understood to design the test procedure. Since low frequency signal collection is the core of the experiment, the capability of the HP 35665A was evaluated first. The entire spectrum (DC to 100 kHz) cannot be viewed on the DSA at one time with sufficient resolution, so data is collected in smaller frequency bands. Research performed in [43] spaced these frequency bands by decades, but it was determined that the most efficient method

is to use the frequency cutoffs designated by the DSA software. In each frequency band, the maximum 800 data points are recorded. The resulting frequency bands are listed in Table 5-1.

Table 5-1: DSA Frequency Band Settings for LFN Measurements

Band	**Frequency**	**FFT Equivalent RBW (Frequency Spacing Between Points)**
1	0 Hz – 800 Hz	1 Hz
2	800 Hz – 4 kHz	4 Hz
3	4 kHz – 10.4 kHz	8 Hz
4	10.4 kHz – 36.0 kHz	32 Hz
5	36.0 kHz – 61.6 kHz	32 Hz
6	61.6 kHz – 87.2 kHz	32 Hz
7	87.2 kHz – 112.8 kHz	32 Hz

Observations show that raw data from each frequency band does not necessarily equate to the same level when plotted with other frequency bands. This is analogous to the data mismatch that occurs when using an SA with different resolution bandwidth (RBW) settings. Since the DSA is an FFT based device, it does not have an RBW like a spectrum analyzer where the signal power at a particular frequency is dependent on the measurement filter bandwidth. However, the data still requires a conversion to retrieve the spectral density (dBV_{rms}/Hz). The data points are converted to the spectral density using Equation (5-1) where the FFT "RBW" is the frequency spacing between data points. The results in Figure 5-3 visually confirms the accuracy of this method and demonstrates agreement between the DSA and SA at the 100 kHz transition frequency.

(5-1) $$dBV_{rms}/Hz = dBV_{rms} - 10\log(RBW)$$

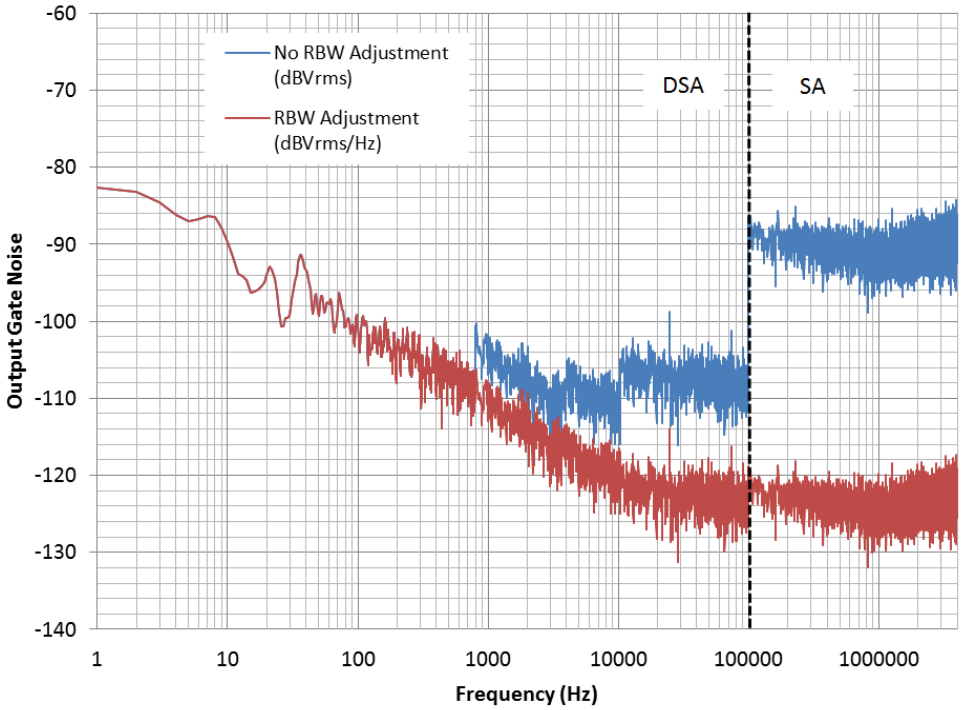

Figure 5-3: DSA and SA output noise data with and without post-processing spectral density conversion. The DSA/SA frequency cutoff shows amplitude agreement with the post-processing conversion.

5.1.3 Test Automation

Agilent VEE Student v9.3 software is used throughout this testing. In additional to having previously used the software for test automation, Agilent and HP equipment integrates seamlessly with VEE which reduces complexity and eliminates potential compatibility issues. IEEE-488 communication standard General Purpose Interface Bus (GPIB) is used to control and collect data from the DSAs, SAs, and SPA. A GPIB to Universal Serial Bus (USB) adaptor is used to interface a PC with Windows 7 to the test equipment.

Test automation played a key role in ensuring timely and consistent data collection. Although the DC characterization test data could have been collected without test automation, the LFN data collection is not practical without

automation. VEE allows the computer to program the HP 4155A, execute the program, retrieve the data, and save the data to a custom Excel template so it can be plotted immediately. Automation is even more crucial using the DSA where settings, such as the frequency band, are changed multiple times during the test. With the exception of GPIB, no other method for retrieving raw data for the DSA is known which makes test automation a necessity. The data retrieved from the DSA and SA are also stored to an Excel template where post-processing calculations, such as adjusting the measurements to account for resolution bandwidth (RBW) and converting dBm to dBV_{rms}, are completed. Test automation also ensures consistent measurements by removing the human element. By running the tests via an automated program, there is greater reliability that measurement settings will be the same for each test as opposed to a human operator who may forget to adjust a particular setting. The DC characterization and LFN automated measurement flowcharts are shown in Figure 5-4 and Figure 5-5.

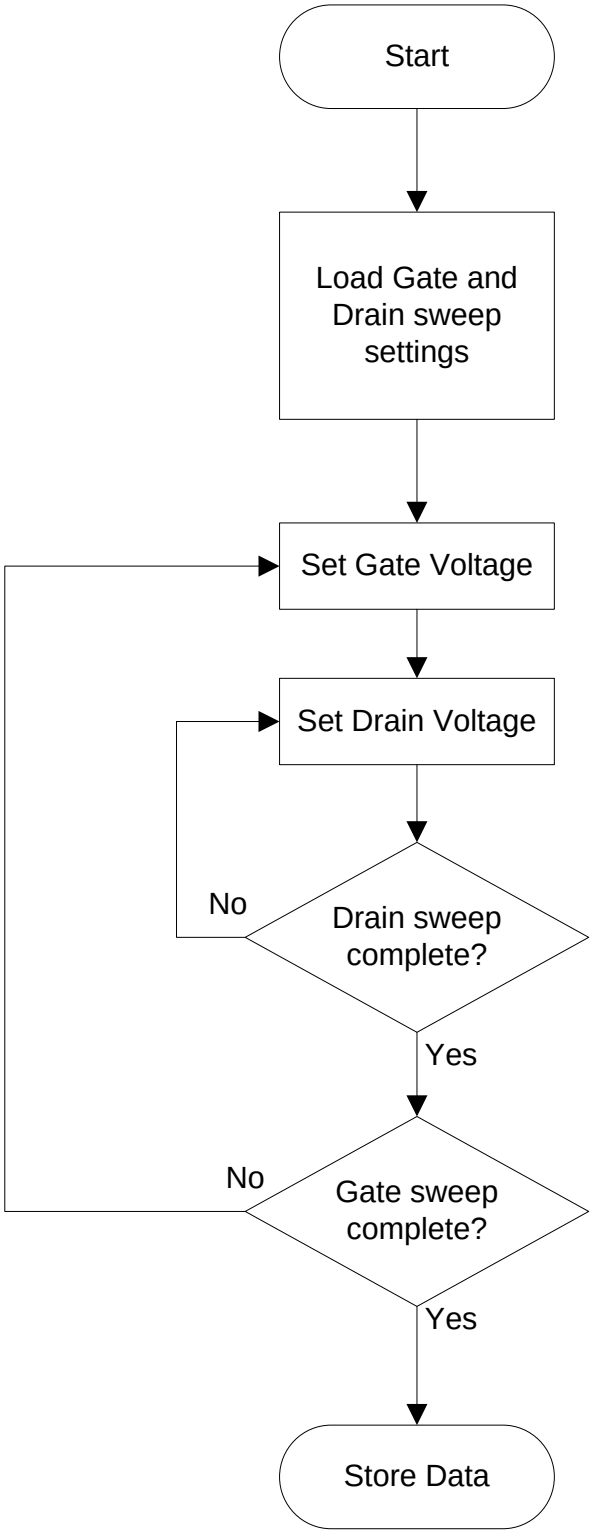

Figure 5-4: DC characterization automated measurement flowchart.

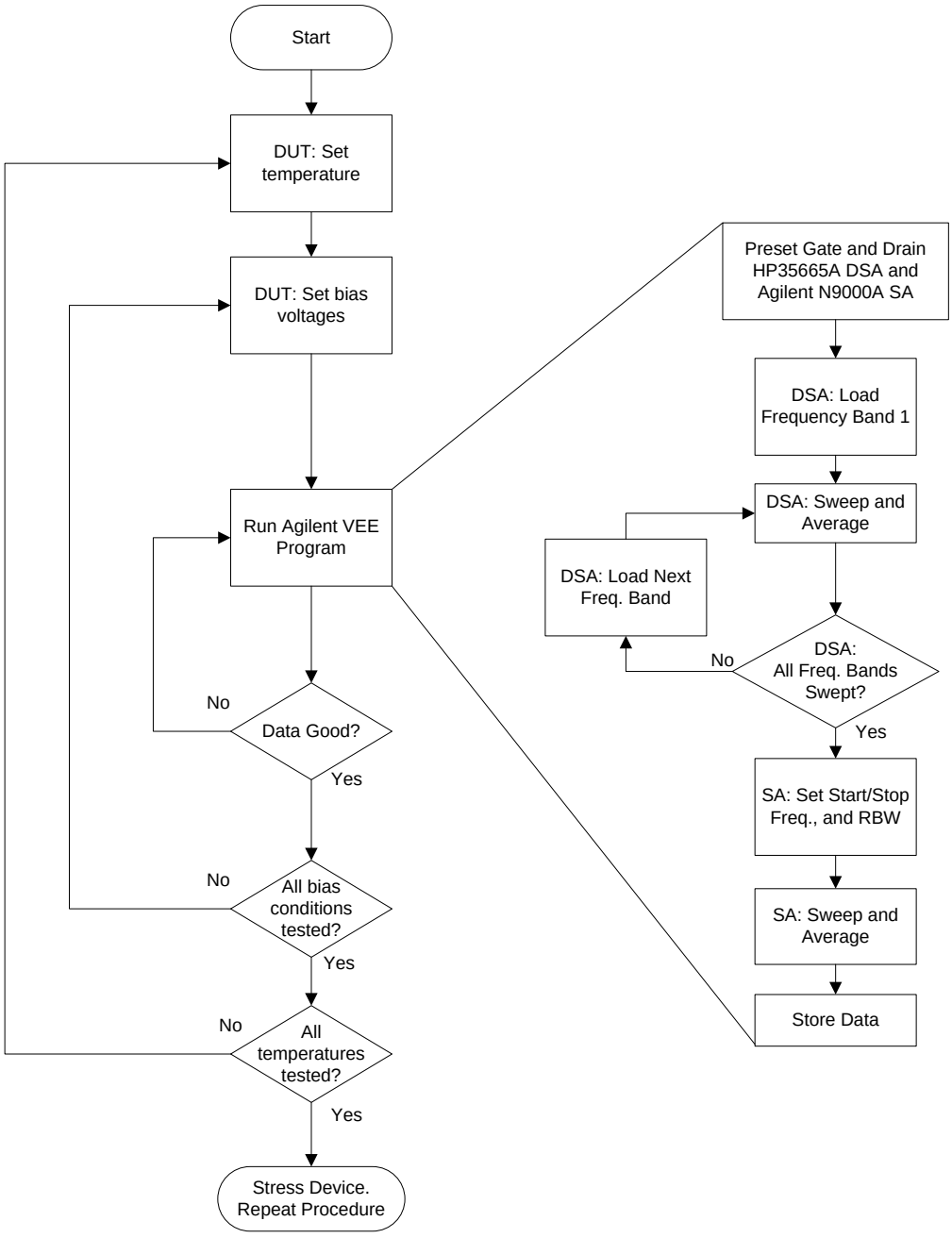

Figure 5-5: LFN measurement flowchart.

5.2 DC Characterization

DC characterization involves obtaining plots for I_{ds} vs. V_{ds} and I_g vs. V_{ds} for different V_{gs} values and I_{ds} vs. V_{gs} and g_m vs. V_{gs} for different V_{ds} values. Each plot provides important information regarding the device characteristics and

DC performance which is compared before and after stress in §6.1. The sweep parameters are listed in Table 5-2 where ΔV is the voltage step with $\Delta V < 0$ indicating a decreasing sweep and $\Delta V > 0$ indicating an increasing sweep. The reason for an increasing or decreasing sweep is discussed in preliminary testing in §5.5. Pre-stress example plots are shown in Figure 5-6. For all test cases, $I_{ds,max}$ = 100 mA, and curves that exceeded this were removed from Figure 5-6 for clarity.

Table 5-2: DC Characterization Sweep Parameters

	I_{ds} vs. V_{ds} **I_g vs. V_{ds}**	**I_{ds} vs. V_{gs}** **g_m vs. V_{gs}**
$V_{ds,max}$ (V)	20.0*	20.0
$V_{ds,min}$ (V)	0*	5.0
ΔV_{ds} (V)	-0.2*	1.0
$V_{gs,max}$ (V)	-1.3	-1.25*
$V_{gs,min}$ (V)	-2.0	-2.0*
ΔV_{ds} (V)	0.05	0.01*

* Indicates the inner sweep parameter.

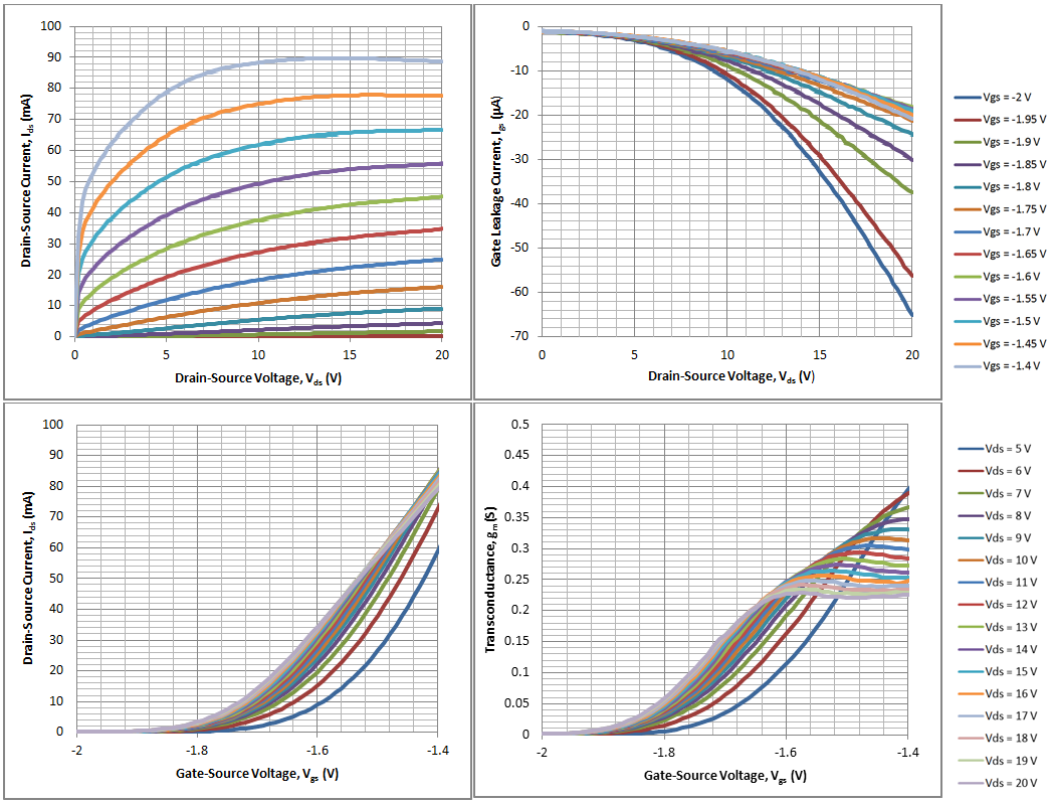

Figure 5-6: Pre-stress example I_{ds} vs. V_{ds} (top left) and I_g vs. V_{ds} (top right) for varying V_{gs} and I_{ds} vs. V_{gs} (bottom left) and g_m vs. V_{gs} (bottom right) for varying V_{ds}.

The I_{ds} vs. V_{ds} plot illustrates I_{ds} performance under various V_{ds} and V_{gs} settings. While the shape of the I_{ds}-V_{ds} curves are consistent for different parts, I_{ds} under the same bias conditions can vary substantially as shown in Figure 5-7 where two parts differ by about 66 mA for the same bias conditions. Although the physical cause of this is not investigated, it is most like due to manufacturing variations that create different threshold voltages, V_{th}, from device to device as shown in Figure 5-8 where V_{th} differs by about 0.3 V between two different devices. Variations in V_{th} and $I_{ds,max}$ in unstressed GaN-on-Si HEMTs have been previously reported that shows an inverse relationship between V_{th} and $I_{ds,max}$ [24]. To minimize the effect of this variable parts were tested by finding I_{ds} at the

arbitrarily chosen V_{gs} = -1.45 V and V_{ds} = 10 V bias condition. Each sample part used in these experiments is categorized as "high I_{ds}", "medium I_{ds}" and "low I_{ds}" where "high I_{ds}" is loosely defined as I_{ds} > 70 mA, "medium I_{ds}" defined as 70 mA ≥ I_{ds} ≥ 30 mA and "low I_{ds}" defined as I_{ds} ≤ 30 mA. The "high I_{ds}" parts have lower V_{th} compared to the other categories as shown in Figure 5-8 where Part 1 turns on 0.3 V less than Part 2 (this also accounts for the large difference in I_{ds} at V_{gs} = -1.45 V and V_{ds} = 10 V). Only parts with similar I_{ds} vs. V_{ds} plots and V_{th} were selected for LFN testing to ensure parts perform consistently under the same bias conditions.

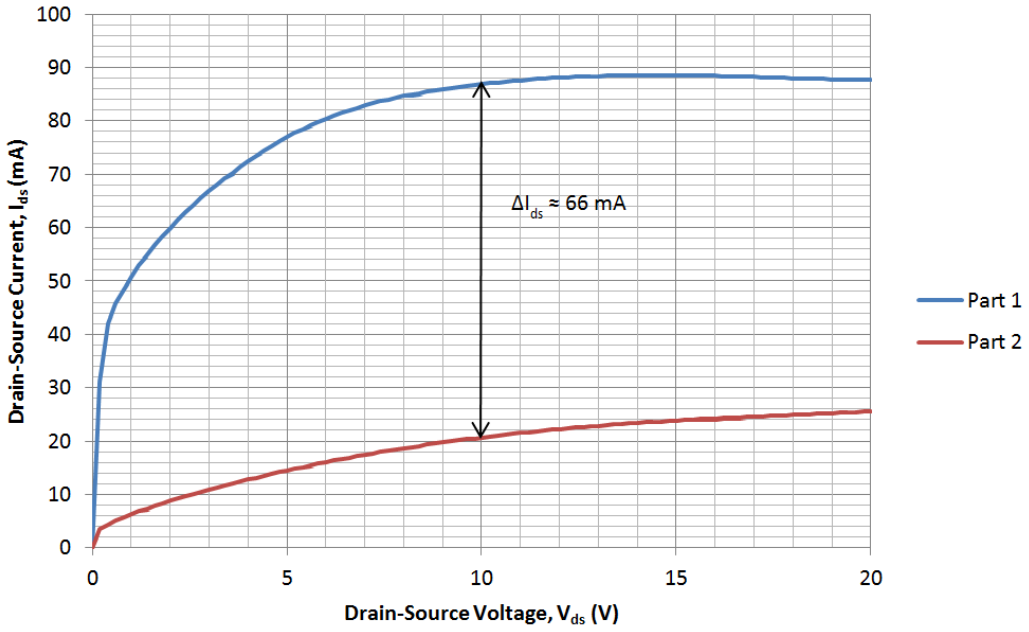

Figure 5-7: Comparison of I_{ds} vs. V_{ds} for two different parts at V_{gs} = -1.4 V shows a large difference in the I_{ds} curves under the same bias conditions.

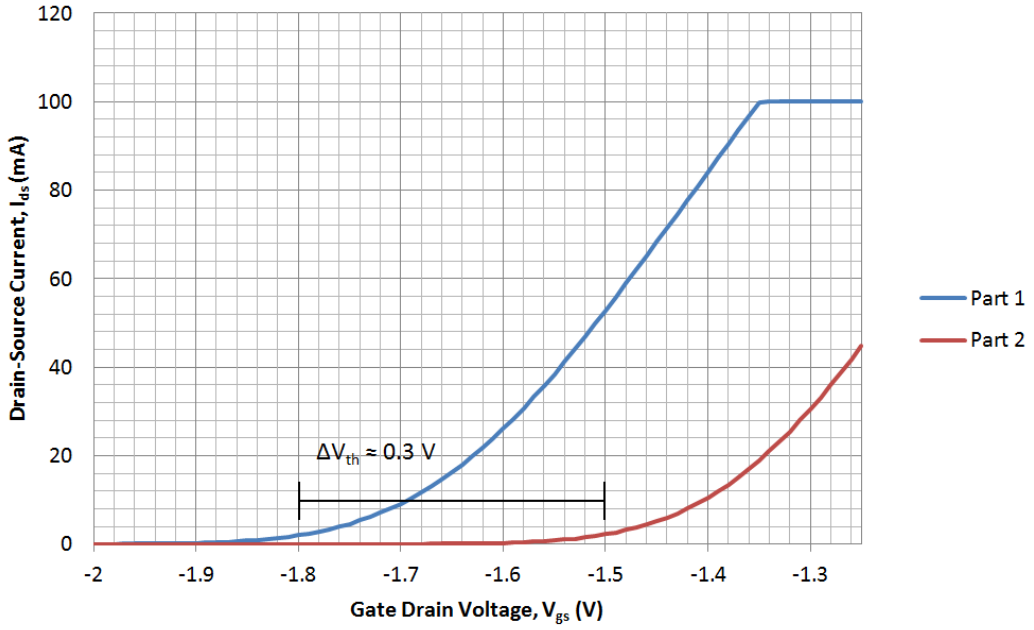

Figure 5-8: Comparison of threshold voltage, V_{th}, between the parts in Figure 5-7 for V_{ds} = 10 V (Note: I_{ds} current limit was set to 100 mA to prevent damaging the devices).

5.2.1 HEMT Pre-test DC Characterization

Prior to testing, the DC performance was characterized and used to establish LFN bias points and identify potential DC biasing issues. The I_{ds}-V_{ds} curves for a typical "high I_{ds}" device was measured to select the bias voltages to be used during LFN testing. From this information it was determined that V_{gs} = -3 V keeps the device in cutoff mode and sufficiently limits I_{ds}, so this bias condition was selected for LFN measurements under cutoff conditions. V_{ds} values of 0.5V, 3V, 5V, 10V, and 15V were selected to provide a large range of low, intermediate, and high V_{ds} bias points along the I_{ds}-V_{ds} curve. Triode bias mode was next found to be between -1.8 V $\leq V_{gs} \leq$ -1.2V when $V_{ds} \approx$ 20 mV while preventing excessive current flow that may lead to device heating. The bias values are summarized in Table 5-3. Previously reported gate oscillation issues

were not experienced when the advised 200 Ω gate oscillation dampening resistor was added while testing [18], [45].

While performing DC characterization, two previously observed phenomenon, the kink effect and I_{ds} peaking at high V_{gs}, on the I_{ds} vs. V_{ds} curves were observed [18]. Four different I_{ds} vs. V_{ds} curves were recorded to illustrate the effects of these phenomenon: fast and slow increasing V_{ds} sweeps and fast and slow decreasing V_{ds} sweeps. During these sweeps, V_{gs} is set, then V_{ds} is set, the HP4155A SPA holds for a user specified time, the data is collected, and then the next V_{ds} value is set. The hold time determines the difference between the "fast" and "slow" sweeps (10 ms for the fast sweeps and 300 ms for the slow sweeps). The results for a single, representative device are shown in Figure 5-9.

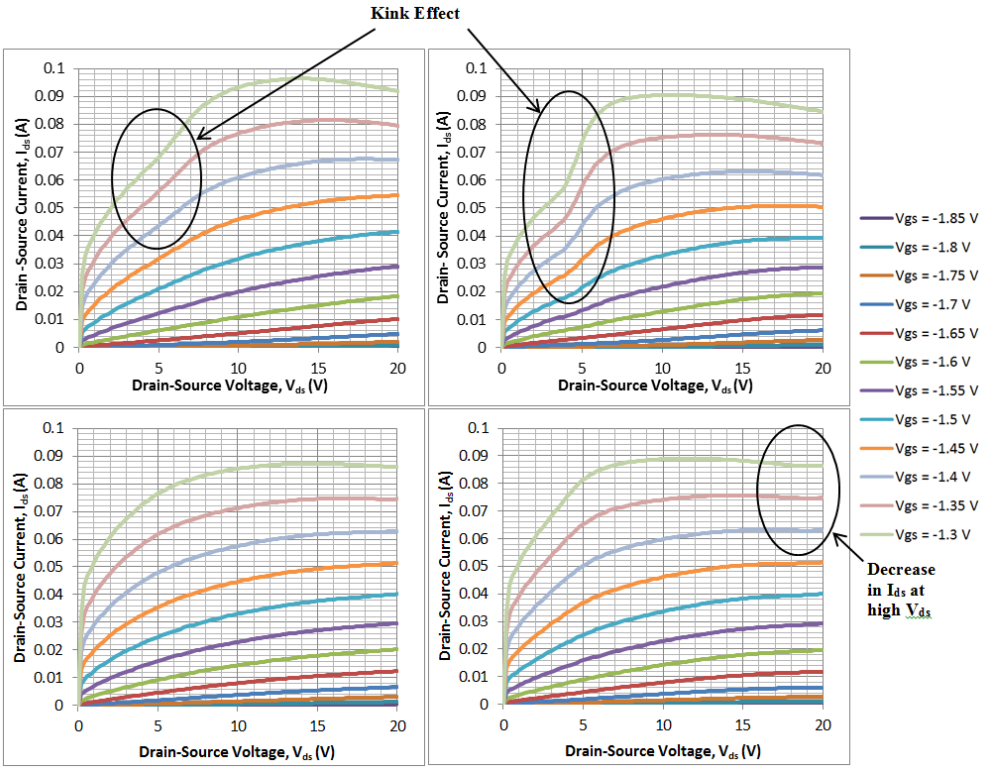

Figure 5-9: I_{ds} vs. V_{ds} sweeps for fast increasing (top left) and slow increasing (top right) V_{ds} and fast decreasing (bottom left) and slow decreasing (bottom right) V_{ds}.

The kink effect shown in Figure 5-9 can be explained by electron traps in the bulk [18]. During increasing V_{ds} sweeps (top of Figure 5-9), electron traps are occupied and the electrons do not have enough energy to reach the conduction band. However, as V_{ds} increases, the horizontal electric field in the AlGaN and GaN material provides enough energy for the electrons to tunnel to the conduction band and flow through the channel. This is in contrast to a similar kink effect which occurs in the I_{ds}-V_{ds} characteristics of Silicon-on-Insulator (SOI) MOSFETs. The SOI kink is due to impact ionization freeing holes trapped at the drain edge of the gate. The increase in I_{ds} is more dramatic during the slow sweep from V_{ds} = 4V to 6V because the electrons have more time to detrap; however, the peak I_{ds} current is lower because electrons are detrapping at different times while the device waits to record data. On the other hand, when the increasing V_{ds} sweep is fast, some lower energy traps do not detrap as soon as they could and end up detrapping at a higher V_{ds} value resulting in higher I_{ds} between V_{ds} = 1V and 4V. A peak $I_{ds} \approx 96$ mA during the fast V_{ds} sweep compared to $I_{ds} \approx 90$ mA was measured for the slow V_{ds} sweep. The decreasing V_{ds} sweeps (bottom of Figure 5-9) do not exhibit the kink effect because electrons stored in bulk trap states quickly detrapped at high V_{ds}. Under the typical common-source amplifier configuration, the device would be biased in saturation mode so the most accurate DC characteristic curve is one of the decreasing V_{ds} curves assuming the electron traps that create the kink effect are void of electrons shortly after applying drain bias.

The other effect highlighted in Figure 5-9 is a decrease in I_{ds} at higher V_{ds}. This phenomenon commonly occurs in other FET devices, such as JFETs, and is cause by device self-heating. Initially, the device temperature is equal to the ambient temperature. As current flows, channel resistances create losses in the form of heat causing the device temperature to increase. An increase in channel temperature leads to a decrease in mobility and an increase in channel resistance resulting in lower I_{ds}. This phenomenon is more evident during the slow decreasing V_{ds} sweep because the device is operating at high power longer and dissipates more heat; as V_{ds} decreases, the power ($P = I_{ds} \cdot V_{ds}$) decreases and there is a slight increase in I_{ds} as the mobility increases.

Gate leakage current, I_g, has been shown to increase after gate stress, so I_g vs. V_{ds} data was also collected to observe the change due to stress [18]. As described in §2.3.2, an increase in the number of electron traps in the AlGaN buffer region leads to trap assisted tunneling. I_g vs. V_{ds} is recorded to observe how I_g changes under various bias conditions before and after stress leading to a way to loosely quantify how much degradation has occurred and to ensure similar device degradation occurs between different sample parts.

5.3 Semiconductor Interface Characterization Using C-V Measurements

A capacitance-voltage (C-V) test is a non-invasive, non-destructive method of examining the internal structure of a semiconductor especially the gate region of field effect devices. The gate region of field effect devices is similar to a capacitor where the gate and channel form the two plates of a parallel plate capacitor with the barrier layer forming the insulating dielectric as shown in

Figure 5-10. For GaN HEMTs, the AlGaN takes the role of the insulating dielectric and the GaN of the semiconductor.

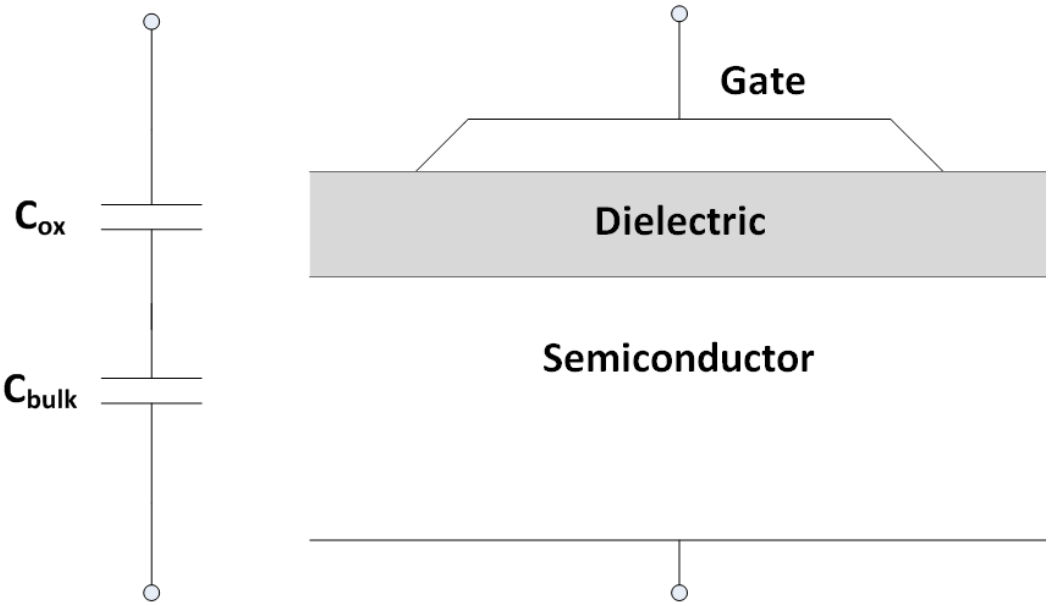

Figure 5-10: Basic MOS semiconductor structure with equivalent circuit [47].

The equivalent capacitance, C_{eq}, in a GaN HEMT is composed of C_{para}, C_{AlGaN}, and C_{depl} where C_{para} is the total parasitic capacitance (gate-source capacitance, gate-drain capacitance, etc.), C_{AlGaN} is the AlGaN capacitance based on Equation (5-2) for a parallel plate capacitor (where t = 17.5 nm, A is the gate area where A = 0.5 μm x 150 μm, and $\varepsilon_r \approx 9$ for AlGaN), and C_{depl} is the gate bias dependent capacitance created by the width of the space charge region that forms when the device is in depletion.

(5-2) $$C = \varepsilon_0 \varepsilon_r \frac{A}{t}$$

C = Capacitance [F]

ε_0 = Permittivity in free space = $8.854 \cdot 10^{-12}$ [F/m]

ε_r = Relative permittivity of the dielectric

A = area of capacitor plate [m^2]

t = dielectric thickness [m]

The cross sectional illustrations in Figure 5-11 depict the location of electrons in the device under varying V_{gs} that create the resulting C-V curve in Figure 5-12. The capacitances in the HEMT model in Figure 5-11 create C_{eq} in Equation (5-3), which is the actual capacitance that is measured during the C-V test.

(5-3) $$C_{eq} = \frac{C_{AlGaN} \cdot C_{depl}}{C_{AlGaN} + C_{depl}} + C_{para}$$

When the device is in cutoff and $V_{gs} << V_{th}$, the 2DEG is depleted of charge and the dominant capacitance is C_{depl}. When a negative charge is applied to the gate, the charge is offset by positive charge in the device to maintain charge neutrality. However, since the materials are not intentionally doped with donor atoms, the resulting space charge region must increase in size to encompass sufficient charge to balance the negative charge at the gate. A wide space charge region causes C_{depl} to become very small based on Equation (5-2) resulting in $C_{eq} \approx C_{para}$. When $V_{gs} > V_{th,}$ the 2DEG begins to fill with charge causing C_{depl} to increase. When $V_{gs} >> V_{th}$, the 2DEG is fully populated with electrons causing $C_{depl} >> C_{AlGaN}$ and $C_{eq} \approx C_{AlGaN} + C_{para.}$

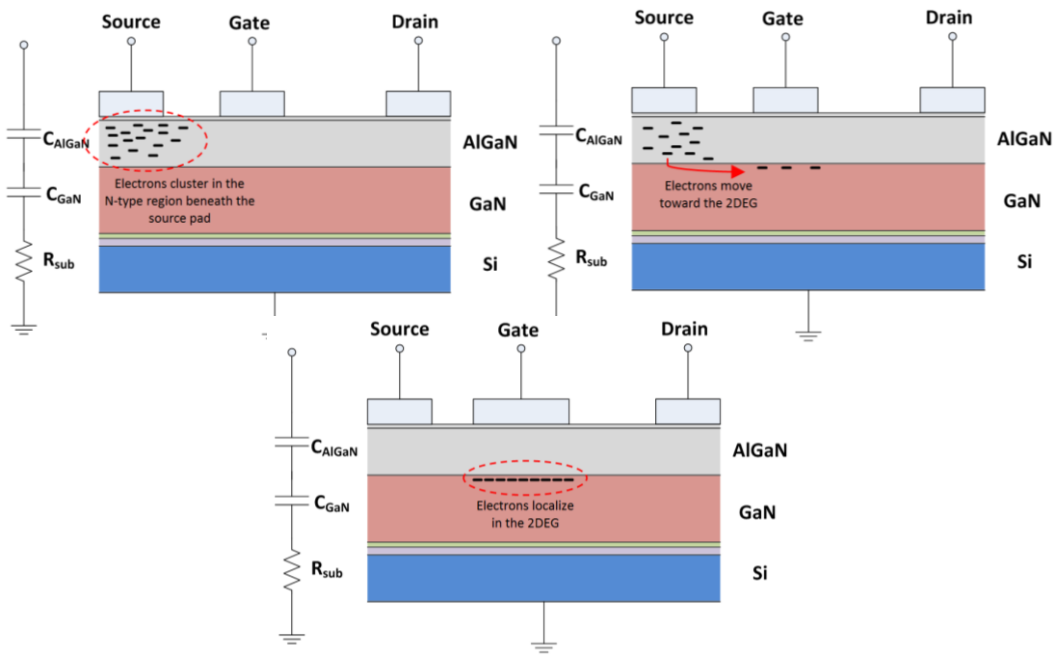

Figure 5-11: Cross section illustration of depletion ($V_{gs} << V_{th}$) (top left), the transition from depletion to inversion ($V_{gs} > V_{th}$) (top right), and inversion ($V_{gs} >> V_{th}$) (right)

Based on this performance, the parameters C_{para} and C_{AlGaN} can be extracted from the C-V curve in Figure 5-12 measured from a sample part where the minimum point on the graph is C_{para} and the maximum point is $C_{AlGaN} + C_{para}$.

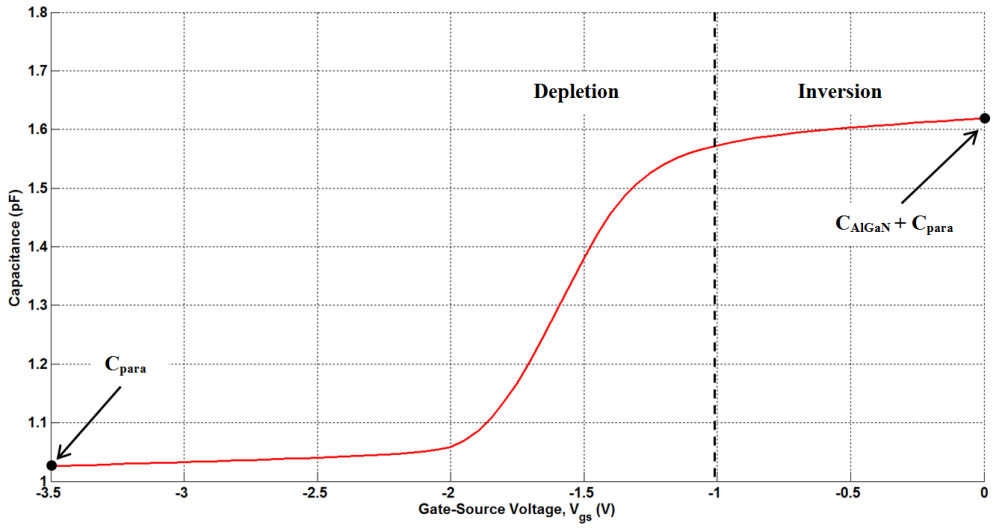

Figure 5-12: Example GaN HEMT C-V characteristic curve.

GaN HEMTs deviate substantially from MOS structures. First, HEMTs are not intentionally doped (although there are some material impurities that cause the GaN to be slightly N-type) and electrons are generated due to the electric field that is created by the piezoelectric effect at the AlGaN/GaN junction. As such, holes do not accumulate near the AlGaN surface and the accumulation region does not experience an increase in capacitance at either high or low frequency as there are effectively no minority carriers in the GaN bulk regions. Second, the HEMTs used in this experiment lack the bulk terminal that typical MOS devices have that sets the bulk to a particular voltage. Instead, HEMTs have a layer of AlN and a high resistivity Si between the gate contact and the backside of the wafer. This prevents the bottom of the GaN from being grounded as would occur in Figure 5-10. In this case, the bulk voltage is floating leaving the source and drain contacts to provide a grounding terminal directly above threshold and indirectly (to the sides of the GaN region) below threshold. The high resistivity GaN layer and Si substrate can also leak current which can reduce the accuracy of C-V testing. It is assumed, then, that the Si substrate conducts a negligible amount of current so that $R_{sub} \rightarrow \infty$ and the bottom of the GaN layer is ground.

To measure the capacitances, a DC bias and small AC signal is applied to the gate with the drain and source shorted together. The gate bias is then incremented to transition the device capacitance between inversion and depletion. At each V_{gs} step, the capacitance is calculated by measuring the phase shift between the AC voltage and current induced by the device capacitance. The test setup block diagram is shown in Figure 5-13. The test settings were determined

experimentally by observing which settings produce the clearest C-V curve. It was found that $V_{AC} = 0.5\ V_p$ was sufficient to create the C-V curves. Frequencies of 1 kHz, 10 kHz, 100 kHz, and 1 MHz were selected to create C-V curves at a variety of frequencies. V_{DC} varies from -3V to 0 V in 0.05 V increments. C-V data is also averaged to minimize measurement variation. All tests are performed under room temperature settings. The results are presented and analyzed in §6.2.

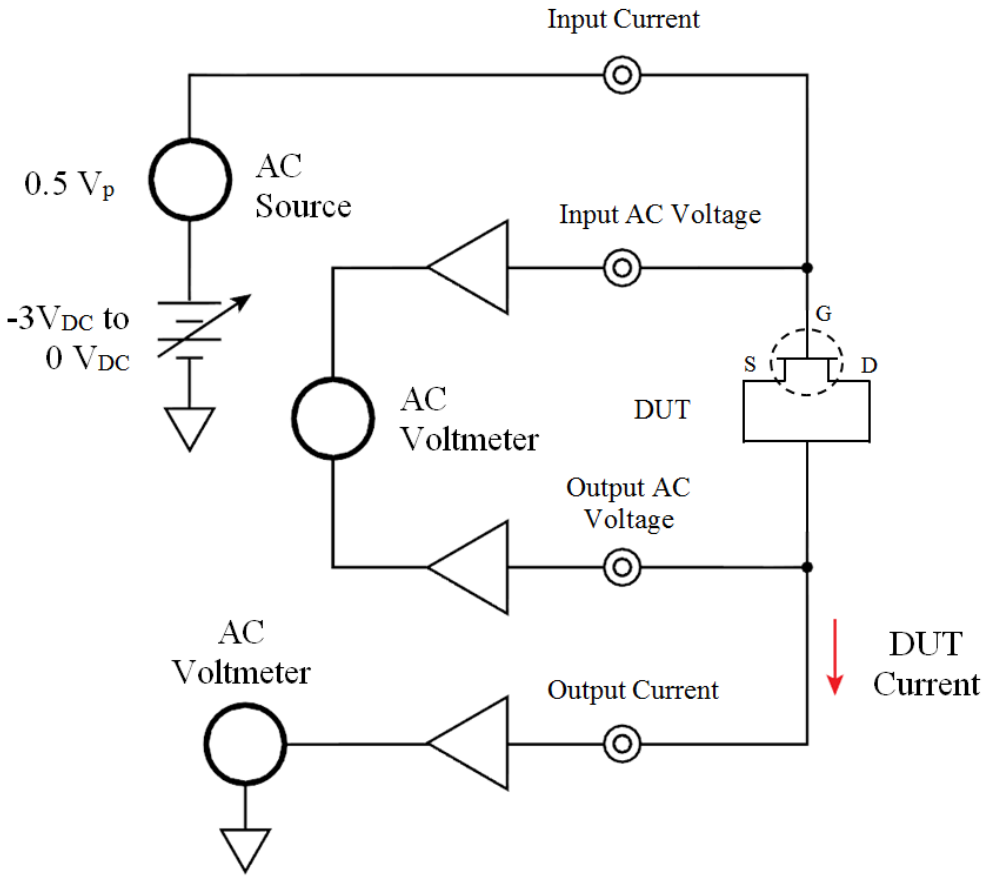

Figure 5-13: C-V test block diagram [48].

5.4 LFN Testing

LFN data is collected under different bias conditions to isolate the location and effects of electron traps in the bulk and channel. Each bias condition is tested

at three different device temperatures: 27˚C, 50˚C, and 100˚C. DC current and voltage at the gate and drain are recorded at each bias condition and temperature. Each test is performed again after applying a high vertical field stress.

5.4.1 LFN Data Collection and DUT Biasing

Gate and drain noise data was collected under a variety of bias conditions to isolate the LFN generation in different regions of the device. The tests and bias conditions under which LFN data was collected are summarized in Table 5-3. Initially, each test set consisted of four different tests: the cutoff, triode, high varying I_{ds}, and high constant I_{ds} tests. However, the high I_{ds} tests were removed after the first test iteration to focus on the bias conditions thought to provide the most useful data. Additionally, the high drain current may alter the device performance by increasing the number of hot electrons or the temperature of the device. A total of three rounds of LFN testing occurred with Rounds 1 and 2 serving to refine the testing procedure. Only the cutoff and triode tests are included in the final results.

Table 5-3: LFN Test Summary and Bias Conditions

Test Name	**DUT Operation Mode**	**Test Rounds Used In**	**V_{ds} (V)**	**V_{gs} (V)**	**I_{ds} (mA)**
Cutoff	Cutoff	1,2,3	0.5, 3, 5, 10, 15	-3	Varying
Triode	Linear	1,2,3	0.02±0.005	-1.8, -1.6, -1.4, -1.2	Varying
High, Varying I_{ds}	Saturation	1	10	Varying	10, 20, 40, 60
High, Const. I_{ds}	Saturation	1	5, 8, 10	Varying	10

The cutoff test sets V_{gs} = -3 V for all the drain bias conditions. In cutoff mode, only small amounts of current flow through the channel, so the resulting noise measurements are the result of the gate leakage current, I_g, flowing through the AlGaN bulk from the drain and source terminals to the negative gate terminal. Previous studies have shown I_g increases by a factor of 100 after gate stress, so this test is re-used while also applying temperature variation to observe the effects that heat has on trap assisted tunneling.

The triode test sets $V_{ds} \approx 20$ mV with varying V_{gs}. Precisely 20 mV is difficult to achieve under V_{gs} = -1.8 V and -1.6 V, so the tolerance is adjusted to $V_{ds} = 20 \pm 5$ mV for this test. Increasing V_{gs} to operate the device in linear mode allows current to flow through the channel. LFN measurements probe the surface traps in the 2DEG region particularly on the GaN side since the negative gate bias repels electrons to the GaN side of the 2DEG. Although it was outside the scope of this research, future work could investigate LFN on the AlGaN bulk by setting $V_{gs} > 0$ V with a small V_{ds} bias. This could provide insight into electron traps in the AlGaN near the 2DEG which are hypothesized to increase in number after gate stress. Further explanation on how LFN probes different regions of the device under different bias conditions is provided in §6.3.1.

5.4.2 DUT Temperature Control

Thermal variations in the device junction temperature can be used as a diagnostic tool. Semiconductor traits can be either dependent or independent of temperature, and both qualities can help better characterize the component. The trap assisted tunneling process in HEMTs is shown to have a temperature dependent component leading to thermionic trap assisted tunneling [49], [50].

Since temperature increases the probability of trapping/detrapping, changes in temperature should lead to increased I_g and LFN spectrum. Based on this hypothesis, each device is tested at a package temperature of 27˚C, 50˚C, and 100˚C. The device junction temperature can be calculated using Equation (5-4). Due to the low current nature of the cutoff and triode tests used in Rounds 2 and 3 of the LFN testing, $P_{Diss,max}$ occurs at $I_{ds} \approx 0.5$ mA at $V_{ds} = 15$ V resulting in $\Delta T_{max} = 0.003$˚C. Self-heating does not significantly change the junction temperature so $T_j \approx T_{base}$.

(5-4) $$T_j = T_{base} + \Delta T = T_{base} + \theta_{jc} \cdot P_{Diss}$$

T_j = junction temperature (˚C)

T_{base} = baseplate temperature (˚C)

θ_{jc} = Thermal resistance between the junction and case (˚C/W)

P_{Diss} = Dissipated power (W) = $V_{ds} \cdot I_{ds}$

The temperature is controlled by the ILX Lightwave LDC-3744B Laser Diode Controller that sources current to two TEC units, on either side of the DUT. A TEC is a solid state heat pump that uses the Peltier effect to produce a temperature gradient between the two ceramic plates based on the amount of current that flows through the unit [19]. In this application, the hot plate contacts the metal surface of the HEMT breakout board while the cold plate contacts the aluminum heat sink. The thermistor contacts the HEMT breakout board near the HEMT to accurately measure the package temperature with thermal grease

supplementing heat transfer to the thermistor from the device. A small piece of styrofoam is added between the aluminum heat sink and the thermistor to thermally insulate the thermistor and the aluminum heat sink. Nylon screws, rather than metal screws, hold the entire assembly together while preventing heat transfer between the breakout board and the aluminum heat sink. The test fixture is shown in Figure 5-14 and is reused from previous research [18]. The desired temperature is set via the ILX Lightwave front panel and is maintained throughout the test set. At 27˚C and 50˚C the temperature fluctuates by ±0.5˚C, and at 100˚C the temperature fluctuates by ±1˚C.

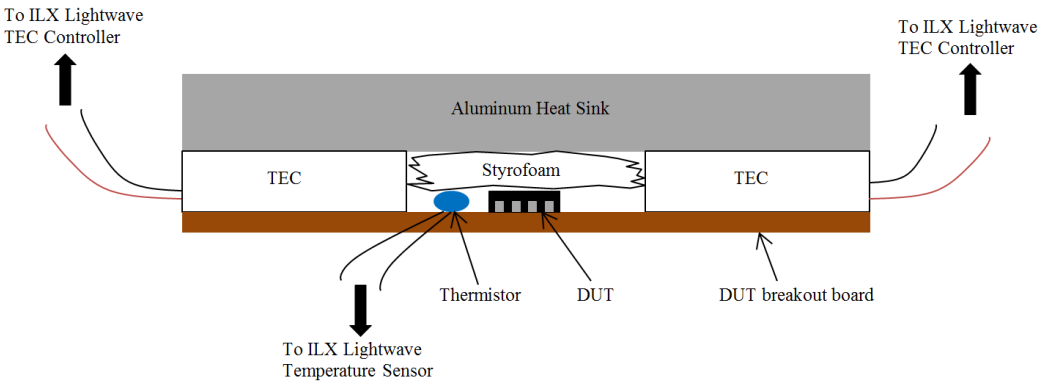

Figure 5-14: Cross sectional illustration of the temperature control apparatus [18].

5.5 Critical Voltage and Gate Stress Profile

The gate critical voltage, V_{crit}, expected due to inverse piezoelectric coupling has been evaluated for the Nitronex NPTB00004 GaN HEMTs before, but initial testing showed different results than those previously reported [18]. Previous research defined V_{crit} as the voltage at which permanent defects or dislocations in the AlGaN crystal structure occur leading to an increase in I_g that eventually leads to device failure at V_{crit} = -70 V [18]. However, new test results

show that the previously reported V_{crit} is dependent on the gate stress profile. In [18], each device was stressed from V_{gs} = -10 V to device failure with -1 V decrements every minute. This stress profile was verified and the DUT experienced critical failure at V_{gs} = -68.9 V as shown by the example test part in Figure 5-15. However, when the experiment was reproduced with a different stress profile, V_{crit} occurs at -75.9 V and -79.0 V. Figure 5-15 shows that two parts with the same stress profile have very different V_{crit} and $I_{g,max}$ tolerances. These results show that although the V_{crit} in [18] does cause degradation, V_{crit} = -70V is not a hard cutoff between safe operation and degradation. Figure 5-16 highlights how I_g increases at V_{gs} < -70V which suggests that degradation actually occurs at lower voltages than V_{crit} = -70V although this degradation occurs at a slower rate. The results in Figure 5-16 also suggests that, if given sufficient time, device failure could occur at any voltage where I_g steadily increases. Unlike [18], identifying a precise V_{crit} value is less important in this research. Instead, a V_{crit} voltage that causes permanent device degradation without causing uncontrollable I_g increase should be selected. This resulted in the decision to use V_{gs} = -70 V as the maximum stress voltage.

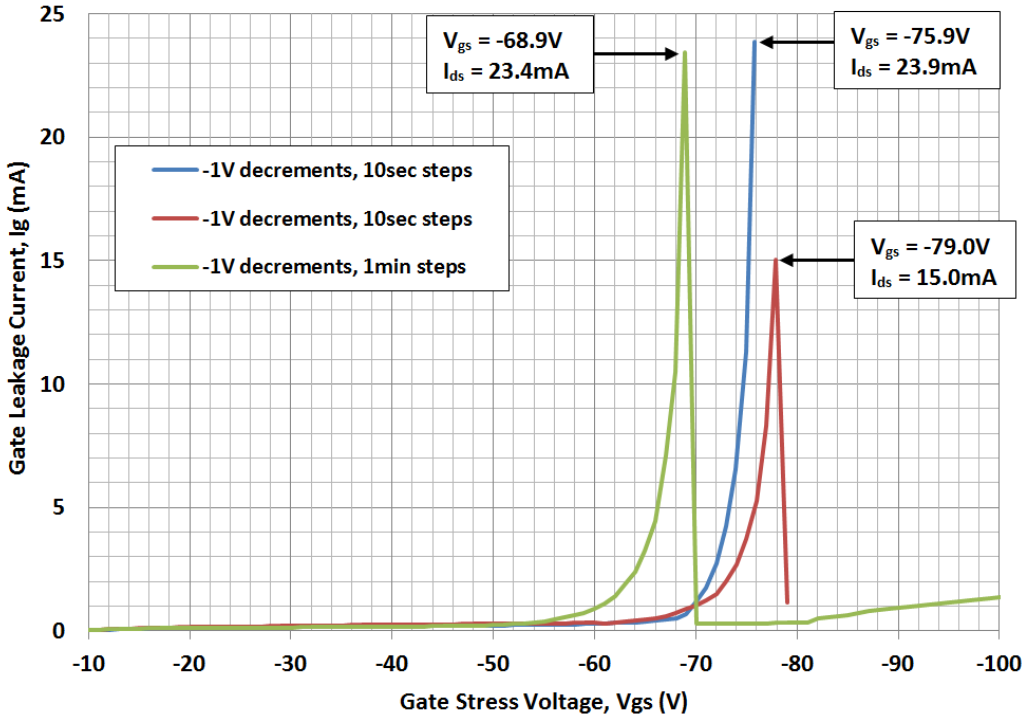

Figure 5-15: Comparison stress profiles and the resulting critical voltage, V_{crit}, where device failure occurs.

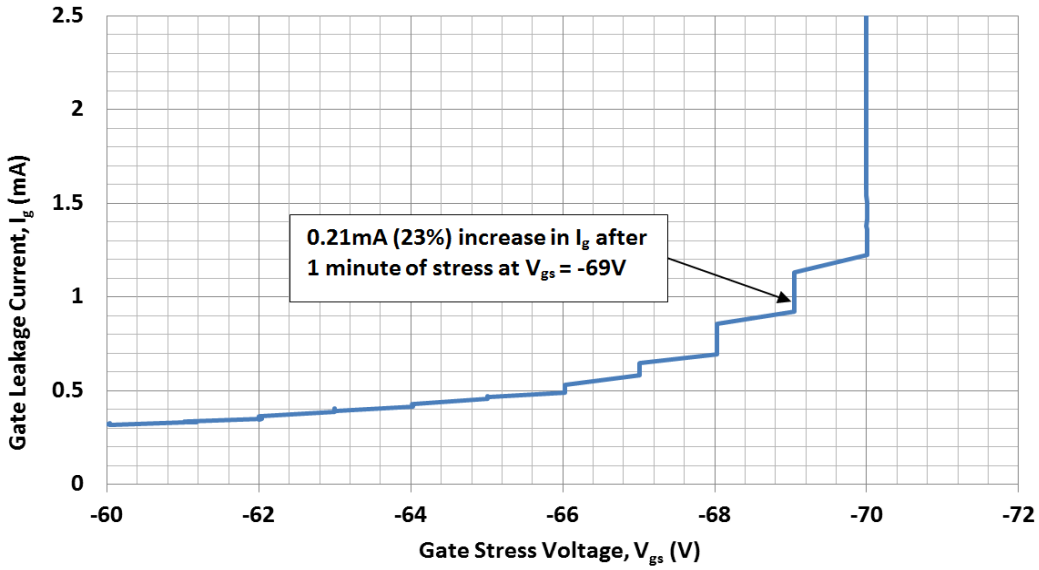

Figure 5-16: Stress profile showing a 0.21mA increase in I_g prior to reaching V_{gs} = -70V.

Gate stress is performed at V_{ds} = 0 V by shorting the source and drain terminals and applying the negative voltage to the gate as shown by the circuit diagram in Figure 5-17. This is referred to as a symmetric field stress because the electric field between the drain and source is nearly symmetrical (the actual electric field, however, is asymmetrical because the Nitronex NPTB00004 gate is offset to the source side as shown in Figure 2-3 which creates a slightly asymmetric electric field. Actual "asymmetric" field stress, another form of high field stress, involves applying high field stress between the drain and source while in cutoff mode).

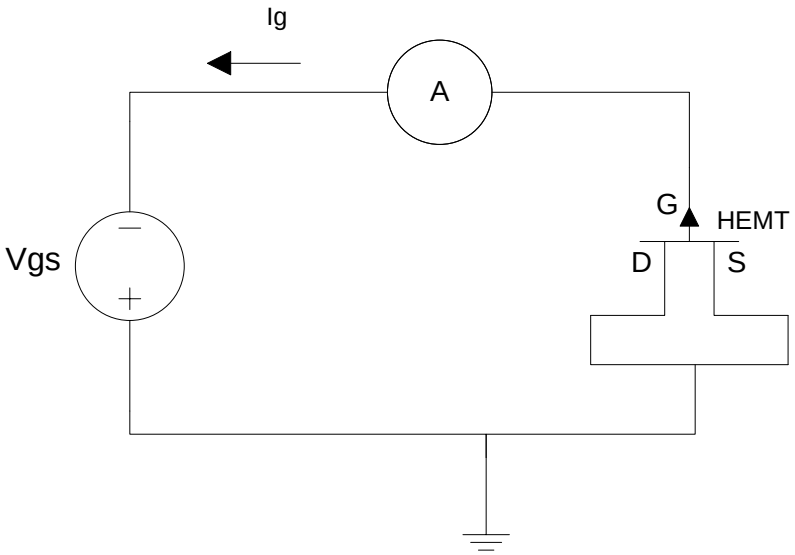

Figure 5-17: Gate stress schematic.

The stress method used in these experiments is different than other methods in that it quantifies stress based on I_g. Previous investigations into gate stress use continuous DC or step-stress methods and time to quantify stress [18], [23], [24]. This typically involves setting V_{gs} to the appropriate stress voltage and allowing the device to sit for a pre-determined time before either turning off the

DC stress or incrementing the device to the next voltage level until reaching the predetermined maximum stress voltage. However, some samples were more resilient to a timed voltage stress, as demonstrated in Figure 5-15, so using a timed voltage stress profile may not stress each device to the same extent. Variations in V_{crit} and indication that electron traps in the AlGaN buffer region increase I_g through trap assisted tunneling led to the conclusion that I_g can be used to quantify stress [23].

The gate stress profile in this experiment involves adjusting V_{gs} continuously from -10 V to -70 V over a 30 second time span followed by constant V_{gs} = -70 V until I_g = 10 mA. These values are verified to cause permanent degradation and changes to the DC, C-V, and LFN characteristics without causing immediate device failure. A typical stress profile is shown in Figure 5-18.

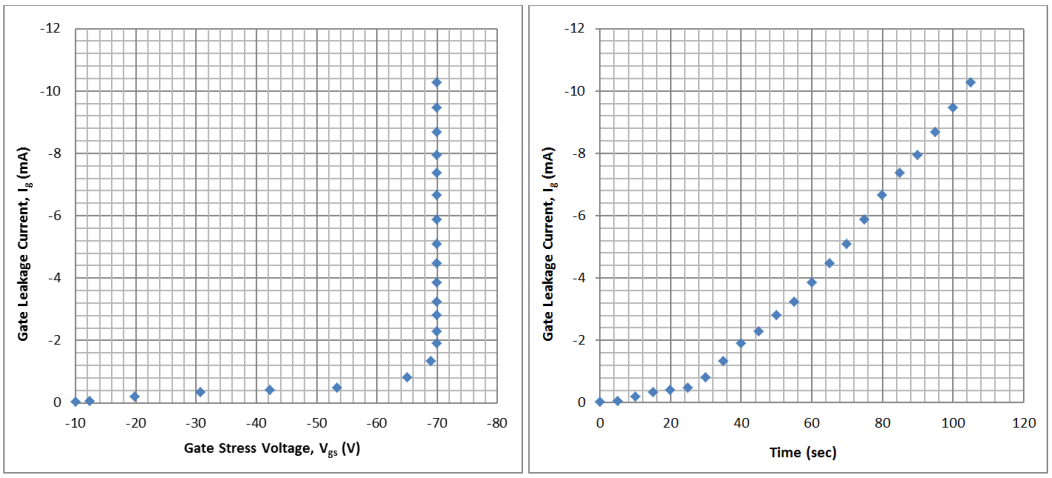

Figure 5-18: Gate stress profile showing I_g changing with increasing stress (left) and with time (right). In both plots, data points are spaced in time by 5 sec.

5.6 Comparison to Previous Research

The research presented in this work is based on portions of previous research from different authors. The work is primarily based on the work by Rao and Bosman who also investigated LFN at the gate and drain under different bias conditions [43], [51]. One test scenario stressed the gate up to -20 V in induce piezoelectric defects similar to this research; however, gate stress performed in this research goes up to V_{gs} = -70 V. Their analysis in [43] provides the basis for isolating the device noise generating region based on the DC bias mode. The major difference between this research and [43] is the stress profiles; Rao and Bosman stress the device for a predetermined time whereas this research stresses the device until I_g reaches 10 mA. Quantifying stress using I_g is unique to this research. This research also expands on the investigation into the time dependent aspects of LFN observed in [43] but also investigates RTS noise temperature dependence.

P. Valizadeh and his colleagues have researched many different aspects of AlGaN/GaN MODFETs. Their findings show degradation mechanisms caused by frequency independent stress which supports electron trap related degradation. This conclusion is based on the DC and RF stressed tests that resulted in similar post-stress DC and LFN changes [52]. A temperature-based investigation by Valizadeh also showed estimated trap time constants ranging from 0.07 eV to 1.55 eV based on G-R noise from the LFN measurements. This research focuses on RTS noise temperature dependence and shows trap activation energies of similar values [53].

DC characteristic measurements are based on previous research by M. Bloom who investigated how DC and RF characteristics change due to the symmetrical and asymmetrical stress [18]. The same Nitronex devices (although most likely different revisions) are used, so similar response to DC stress is expected. The next section presents the pre-stress and post-stress DC characteristics, C-V, and LFN results and analysis.

Chapter 6: Results and Analysis

Three testing iterations were performed with the first two iterations used to get a better understanding of LFN in the sample devices, improve the testing procedure, and ensure all necessary data between the pre- and post-stress parts is collected. With the exception of the DC characterization, the data presented in this section is from the third and final test iteration consisting of four sample parts. Only "high I_{ds}" parts (defined in §5.2) are used. All sample parts were tested and stressed under similar conditions.

6.1 Effects of Gate Stress on DC Characterization

The effect of gate stress on device DC characteristics was explored in previous research on the same manufacturer and model part [18]. It is important to re-characterize the new batch of parts because manufacturing process changes, design changes, or manufacturing variations between the new and old sample sets may lead to slightly different performance. Using a new set of parts, similar DC characteristics were recorded, and the results are consistent with those found in [18].

The DC characterization test consists of 8 parts stressed until I_g = 10 mA using the gate stress profile defined in §5.5. The average I_{ds}-V_{ds} characteristic and transfer characteristic of the sample set are illustrated in Figure 6-1 and Figure 6-2. Figure 6-1 shows that I_{ds} increases after gate stress. One explanation for the overall increase in I_{ds} after stress is a negative shift in V_{th} which would cause the stressed device to conduct more current for the same gate voltage. This theory is supported by Figure 6-2 where the stressed transfer characteristic shifts more negative by approximately 0.04 V.

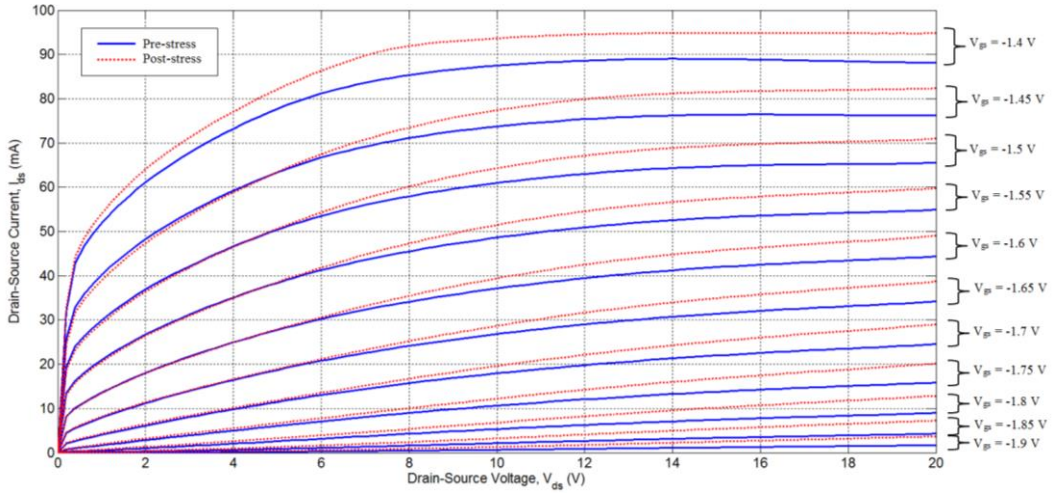

Figure 6-1: Average I-V characteristic before (solid) and after (dashed) gate stress.

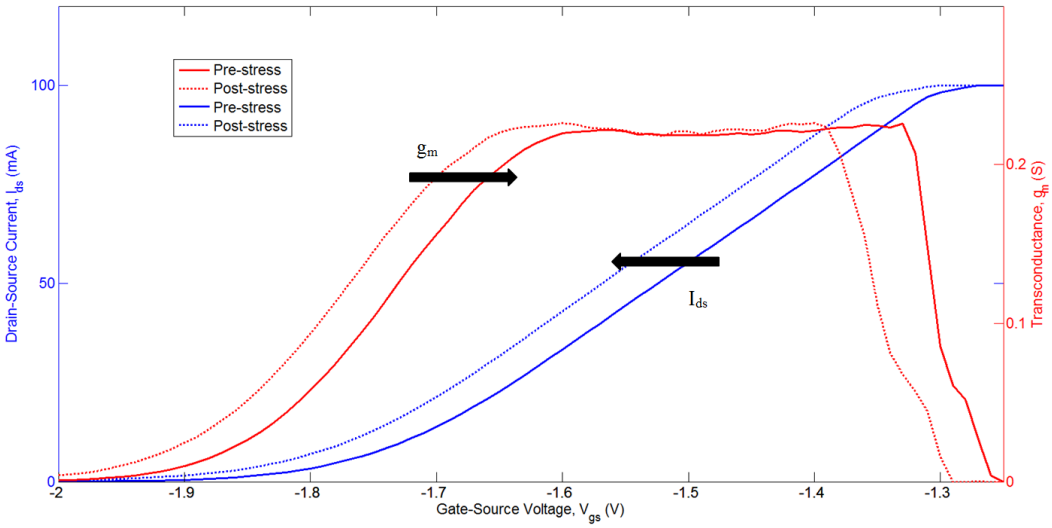

Figure 6-2: Average transfer characteristic (blue) and transconductance (red) before (solid) and after (dashed) gate stress for V_{gs} = 20 V.

Another interesting trend in Figure 6-1 is the average increase in I_{ds} after stress is much larger in the saturation region than the linear region. For instance, when V_{gs} = -1.5 V, I_{ds} increases by approximately 5.2 mA (7.8%) at V_{ds} = 20 V while I_{ds} is approximately the same at V_{ds} = 2 V. This phenomenon is most likely caused by the same mechanism that causes the kink effect in Figure 5-9. Electron

traps on the AlGaN surface near the gate creates a residual negative charge at the gate that is released at higher V_{ds} causing I_{ds} to increase.

Gate leakage also increases by up to 235% after stress as indicated by Figure 6-3. This increase was previously reported in [18] and is thought to be caused by trap assisted tunneling through defects formed by the inverse piezoelectric effect [23]. Other research into the cause of gate leakage has suggested multiple theories including impact ionization in the channel, thermionic trap assisted tunneling, hot electron defect generation, Poole-Frenkel emissions, and electron field emissions [54]. More analysis on gate leakage mechanisms will be presented in subsequent sections.

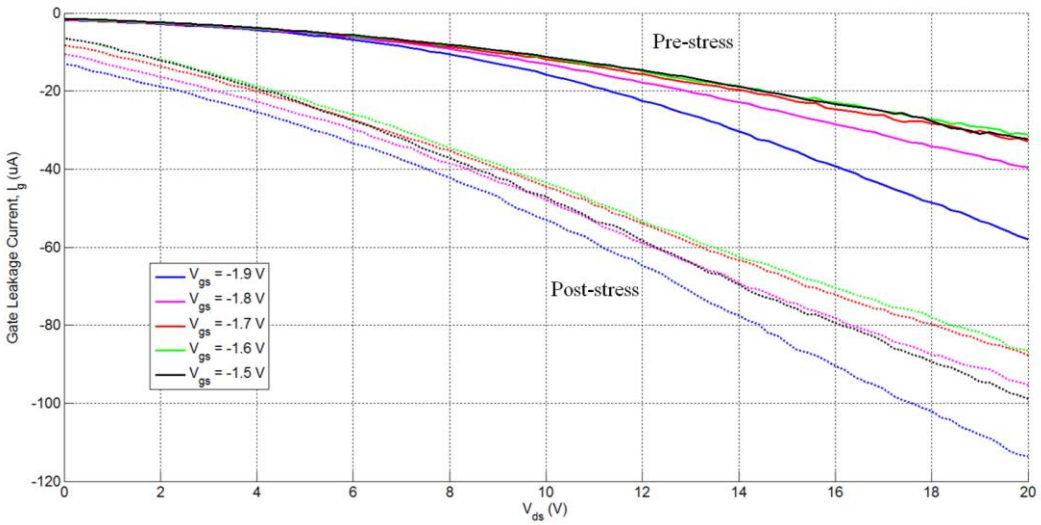

Figure 6-3: Gate leakage current, I_g, before and after gate stress.

6.1.1 Cutoff Bias DC Current and a Modified Low Frequency Noise Model

DC current measured during LFN under cutoff conditions reveals how gate stress increases after stress. A plot of the ratio of drain current to gate current, I_d/I_g, before and after stress in in Figure 6-4 reveals that between 24% to 35% of the gate currents originates at the drain when V_{ds} = 0.5V and V_{gs} = -3 V

for this particular sample (in other samples, the ratio ranges from 8.6% to 35%). This means that the remaining 65% to 76% of the gate current originates from the source, which is at 0 V. However, when V_{ds} = 15 V, the ratio increases to 97%. The ratio is expected to increase because V_{dg} increases from 3.5 V to 18V resulting in an increase in I_d. I_g increases at approximately the same rate as I_d because I_s is approximately constant at all V_{ds} as shown in Figure 6-6.

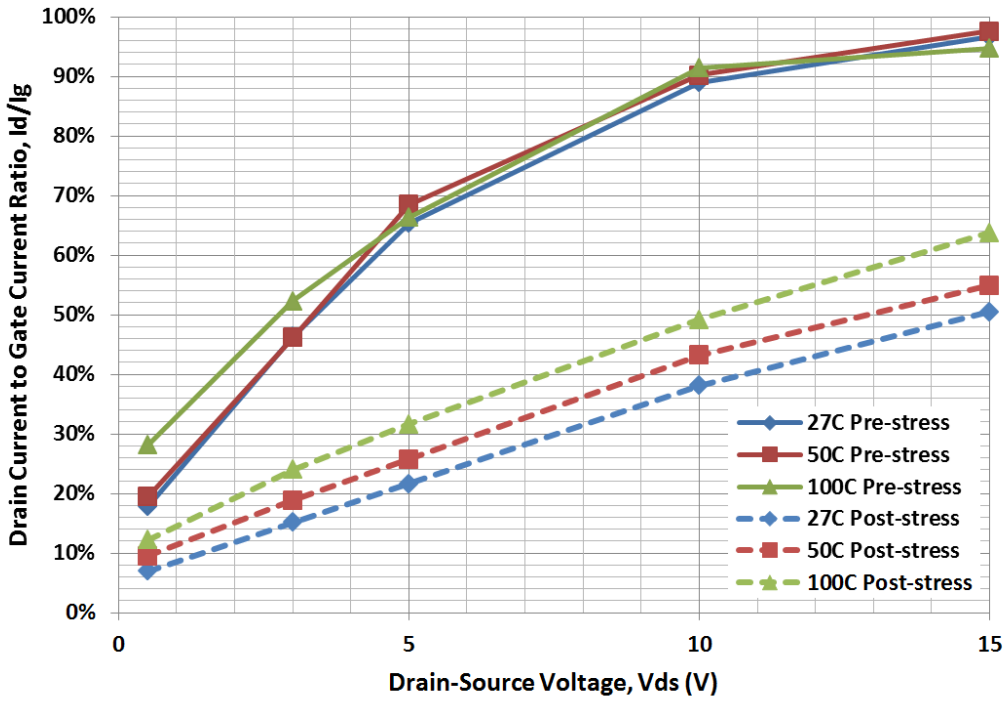

Figure 6-4: The average ratio of drain current to gate current, I_d/I_g, measured during cutoff LFN testing decreases after stress because I_g increases much more than I_d.

After stress, the ratio decreases significantly ranging from 9% to 14% when V_{ds} = 0.5V and from 52% to 65% when V_{ds} = 15V. Because the HEMT is a three terminal device, the increase in I_g and disparity in I_d/I_g before and after stress is due to an increase in source current. When the stress is performed, more degradation is occurring on the source side resulting in more defects, lower gate-

source resistance and higher I_g. High stress on the source side can be explained by the fact that the gate is offset to the source side (1.5μm source-gate spacing compared to 3.5μm drain-gate spacing [13]) resulting in a higher electric field strength over the gate-source distance. The source connected field plate (SCFP) is included in GaN HEMTs to distribute this high gate electric field across a wider area thus preventing localized stress beneath the gate that may increase degradation due to the inverse-piezoelectric effect. The results show that degradation is occurring between the gate and source in spite of the SCFP, and that the AlGaN on the source side is just as susceptible to defects even with the SCFP. It is not clear if the gate-source and gate-drain junctions have distinct V_{crit} values above which degradation occurs. While the DC currents at each terminal does not necessarily reflect higher LFN, it does suggest there may be a higher correlation between the gate and drain LFN before stress at higher V_{ds} since a majority of the current travels through both the drain and gate and experiences similar trapping and detrapping mechanisms. This correlation may be lower when the I_d/I_g ratio is lower since a higher portion of I_g travels through the source.

The results show a need to modify the existing low frequency noise model in Figure 3-5. The new LFN model in Figure 6-5 splits R_{AlGaN} into two different resistors: R_{gs} and R_{gd}. These new resistors reflect the fact that I_d and I_s change independently of each other after stress. While all the resistors produce thermal noise, R_{ch}, R_{gs}, and R_{gd} are the dominant LFN sources because these locations contain the traps that produce LFN. This model will be referenced in §6.3.1 to identify the noise producing regions under the LFN test bias conditions.

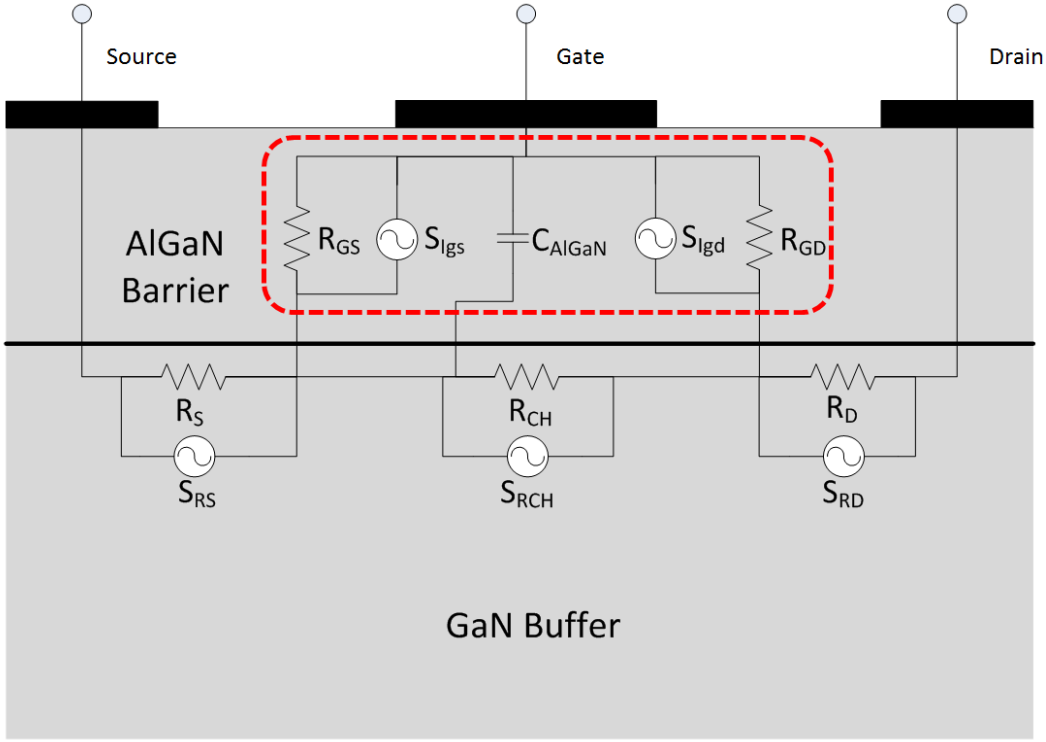

Figure 6-5: Modified LFN model for GaN HEMTs.

6.1.2 Temperature Dependence of DC Measurements

Another look at leakage current in Figure 6-6 under cutoff bias condition during the LFN test reveals a different I_g and I_d dependence on temperature after stress. Under cutoff bias, I_d represents the leakage component of I_g on the drain side as will be justified in §6.3.1. Research has shown both an exponential increasing and decreasing relationship between I_g, I_d and temperature at high V_{ds} (between 40 V and 50 V) [55]. S. Arulkumaran et al., concluded below 80˚C, I_g and I_d leakage is due to impact ionization which decreases with increasing temperature. At temperature above 80˚C, I_g and I_d increase exponentially with temperature due to thermionic trap assisted tunneling. Because $V_{ds,max}$ = 15 V (instead of 40 V or 50 V) and only two temperatures were recorded below 80˚C, the effects of impact ionization are difficult to observe compared to the research

in [55]. Figure 6-7 does reveal a decrease in I_d current between 27˚C and 50˚C at V_{ds} = 3 V, 5 V, and 10 V which indicates that the data supports previous findings but is insufficient to draw further conclusions.

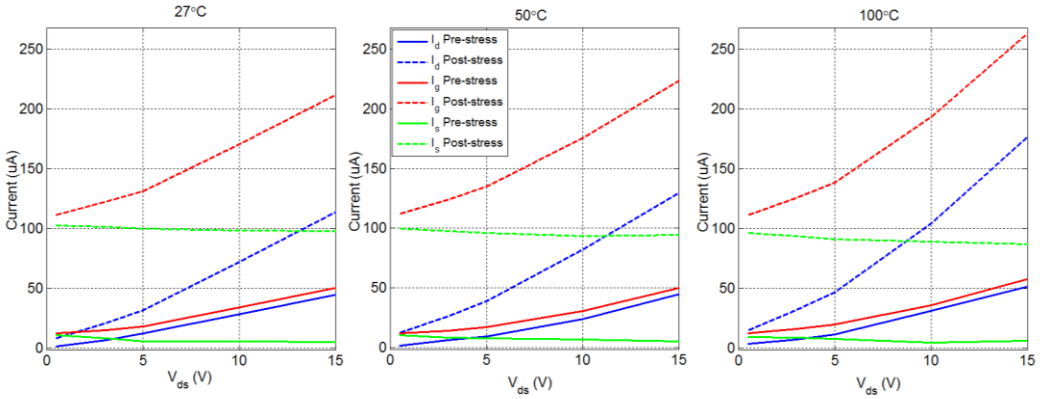

Figure 6-6: LFN gate, drain, and source current measurements at V_{ds} = 0.5 V, 3 V, 5 V, 10 V, and 15 V and V_{gs} = -3 V. I_g and I_d reveal a positive temperature dependence after stress.

After stress, I_d increases with temperature even at 27˚C and 50˚C which indicates stress changes the dominant gate leakage mechanism. The resulting activation energies range from 0.62 eV to 0.67 eV which are lower than previously reported 0.99 eV for trap-assisted tunneling mechanisms [55]. This shows that leakage current is due to a temperature dependent mechanism. If traps cause I_g, then stress reduces the amount of energy required to induce tunneling by increasing trap density and creating new traps in the AlGaN near the gate. Temperature dependence also suggests that these traps are close in proximity and the change in energy (only about ΔkT = 6.3 meV or about 1% change) produced by the change in temperature from 27˚C to 100˚C is sufficient to activate new traps.

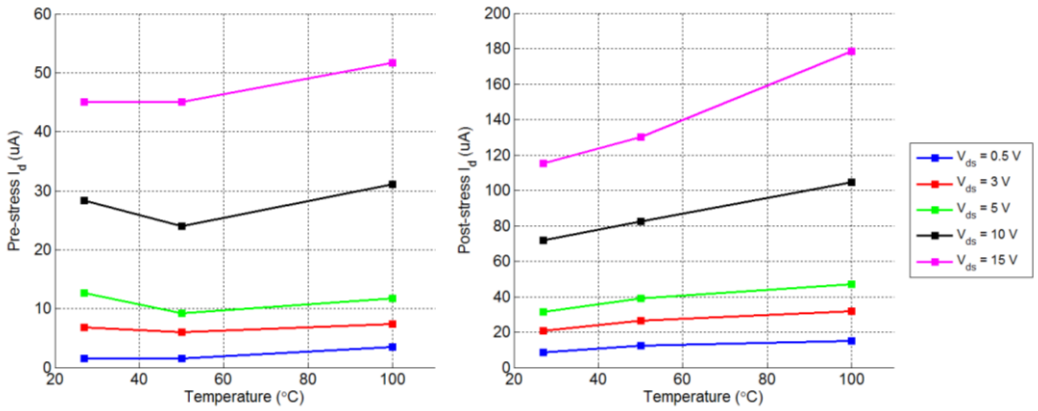

Figure 6-7: Pre- and post-stress LFN drain current from the same part in Figure 6-6.

Temperature dependence of I_d and I_g is apparent after stress at the gate-drain conduction path only (because V_{gs} was not varied during testing, it is unclear if the gate-source resistance, R_{gs} is temperature dependent. The explanation for separate gate-source and gate-drain resistances is in §6.1.1). For all sample parts, the gate-drain resistance, R_{gd}, decreases linearly with temperature by between 584 Ω/˚C and 769 Ω/˚C as shown in Figure 6-8. This suggests that a temperature dependent gate leakage current is significant after stress. Thermionic trap assisted tunneling (TTT) has been reported as a major contributor to gate leakage current; however, TTT typically occurs at temperatures greater than 100˚C [54], [55], [56]. Defect formation due to gate stress leading to new traps likely produces traps that require less energy, which are therefore located closer to the gate by the McWhorter model, making temperature related trapping and detrapping events more common. Temperature dependence in LFN will be addressed in §6.3.

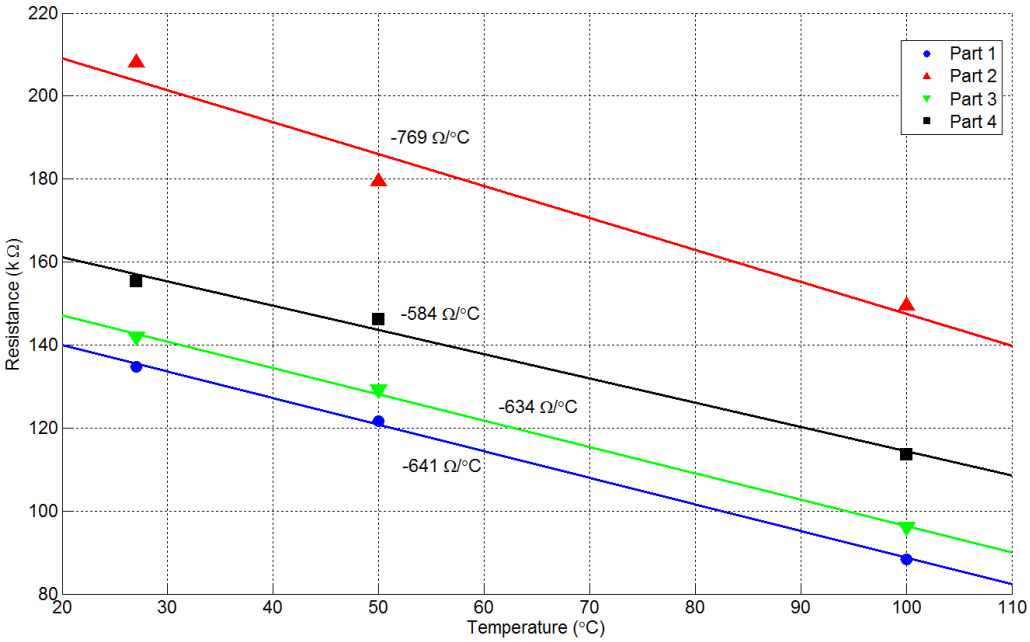

Figure 6-8: Gate-drain resistance decreases with increasing temperature after stress.

Research has shown that the dominant gate leakage mechanism is temperature dependent and referred to as thermionic trap assisted tunneling (TTT) [49], [50]. The current density for the TTT model, J_{TTT}, is shown in Equation (6-1) [50]. The Fermi-Dirac function is shown in Equation (6-2), and barrier lowering due to image charge and temperature is shown in Equation (6-3).

(6-1) $$J_{TTT} = \frac{qC_tN_t}{E}\int_{\varphi_t}^{\varphi_B+\varphi_F}\left(\frac{1}{f_{FD}P_1}+\frac{1}{P_2}\right)^{-1}d\varphi$$

C_t = trap energy dependent rate constant

N_t = trap density

E = Peak electric field at the gate junction

φ_t = trap energy level

φ_B = Schottky barrier height at the gate

φ_{fb} = difference between the conduction band and fermi level in the GaN bulk

f_{FD} = Fermi-Dirac fuction

$P_{1,2}(\varphi)$ = probability of tunneling to the Fermi level (P_1) and conduction band (P_2)

(6-2) $$f(E) = \left[1 + e^{(E-E_F)/kT}\right]^{-1}$$

E = Schottky barrier Energy (eV)

E_F = Fermi Energy (eV)

T = Temperature (K)

k = Boltzmann's constant = $1.381 \cdot 10^{-23}$ [m^2kg/s^2K]

(6-3) $$\varphi_B = \varphi_{B0} - \gamma_I\sqrt{\frac{qE}{\pi\varepsilon}} - \gamma_T T$$

φ_{B0} = Original Schottky barrier height

γ_I = fitting constant due to barrier lowering caused by image charge at the barrier edge

γ_T = barrier height change due to temperature [V/K]

Both φ_B and f_{FD} depend on temperature. An increase in temperature leads to a decrease in the Schottky barrier (as described in Equation (6-3)) which increases the tunneling probabilities, $P_1(\varphi)$ and $P_2(\varphi)$, resulting in higher leakage current, $I_{TTT} = SJ_{TTT}$, where S is the gate area. An increase in temperature also causes f_{FD} to increase leading to an increase in the weighted tunneling probability $f_{FD}P_1$

resulting in higher I_{TTT}. These equations approximate the AlGaN conduction band shape to be triangular and assume an even distribution of traps which is necessary to produce 1/f noise in the AlGaN region [41], [49]. A positive relationship between temperature and I_g further supports the notion that trap assisted tunneling is the primary cause of gate leakage current, and future references to trap assisted tunneling in this thesis assume a temperature dependence.

6.2 Effects of Gate Stress on C-V Characteristics

C-V measurements were performed at 1 kHz, 10 kHz, 100 kHz, and 1 MHz. However, the 1 kHz and 10 kHz data after stress in Figure 6-9 is revealed to be faulty due to the increase in I_g after stress. C-V measurements assume that leakage current through the capacitor dielectric is negligible, but all non-ideal capacitors have a small amount of leakage current. Since AlGaN has a much smaller band gap compared to the oxide layer in MOS devices (6.3 eV compared to approximately 8 eV for SiO_2 typically used in MOS devices), electrons are more likely to leak through the AlGaN dielectric especially after high field stress [57], [58]. If too much current leaks through the dielectric, the measurement equipment will not get an accurate capacitance reading.

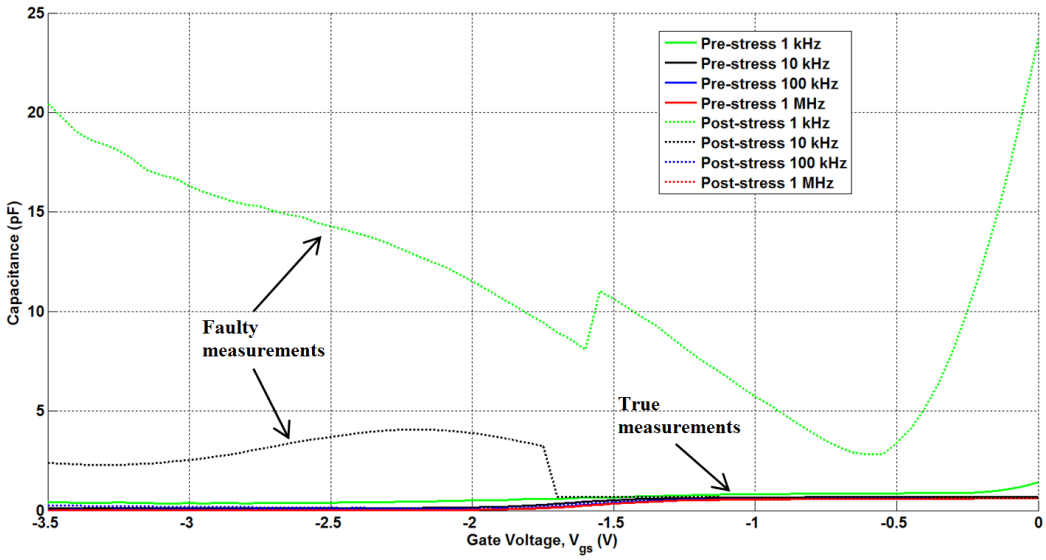

Figure 6-9: Pre- and post-stress C-V measurements with faulty measurements.

The occurrence of faulty data at low frequencies indicates the gate leakage mechanism is time dependent and more prominent at low frequencies. This could be achieved by electron traps with varying time constants; at 1 kHz and 10 kHz, the electrons have more time to travel through the AlGaN. At 10 kHz, the sine wave AC input half period is 0.05 ms, so the conduction mechanism must respond in less time. LFN of >20kHz ($\tau < 0.05$ ms), so multiple trap events leading to electron conduction through the AlGaN is possible.

Consistent results in each sample indicate that the same mechanism is causing the change. All four samples had similar post-stress 1 kHz C-V curves characterized by an approximately linear decrease in capacitance from -3.5V to -2V followed by an abrupt increase between -1.85V and -1.55V, another linear decrease between -2V and -0.6V, and concluding with a linear increase in capacitance between -0.4V and 0V. Additionally, three of the four parts had post-

stress 10 kHz C-V curves that increased slightly between -3.5V and -1.8V before decreasing over a 0.05V span.

Analysis of the DC characteristics in §6.1 show that before stress, $|I_{g,max}| = 60.8$ μA whereas after stress, $|I_{g,max}| = 265.3$ μA, so substantially more DC current is conducted through the AlGaN. Measuring the real component of the impedance presented at the gate terminal (the leakage conductance of the AlGaN barrier) gives additional information on the density trap states in the barrier. Further investigation into these observations needs to be conducted to determine the mechanism responsible by using smaller frequency steps. The 1 kHz and 10 kHz measurements are not used in future analysis.

Stress induces a lesser change in the 1 MHz and 100 kHz C-V measurements in Figure 6-10. For all samples, the post-stress C-V curve at 1 MHz saw a maximum increase ranging from about 0.02 pF to 0.05 pF (1.70% to 4.58%). In some cases, the measured capacitance actually decreased slightly after stress, as is the case for the 100 kHz C-V measurements in Figure 6-10 between $V_{gs} = 0$ V and -1 V , but this could have been caused by changes in the parasitic capacitance in the measurement setup and does not indicate a significant change. Since C_{AlGaN} is approximately the same before and after stress, the physical composition of the device does not change indicating that gate sinking does not occur at temperatures $\leq 100^{\circ}$C. Unlike the other faulty curves, the 100 kHz post-stress curve is similar to the pre-stress curve between $V_{gs} = 0$V and -1.2V, but deviate from the pre-stress curve as $V_{gs} < -1.25$ V. The precise cause of this is unknown, although the fact that the increase in depletion mode occurs at 100 kHz

and not 1 MHz again indicates a time dependent mechanism. This trend resembles hole generation in MOS devices (although the mechanisms are most likely different) when the device enters accumulation [47]. This indicates that as V_{gs} decreases, positive charge is accumulating near the channel through a mechanism that was not present before stress. The cause of this is a topic for future research.

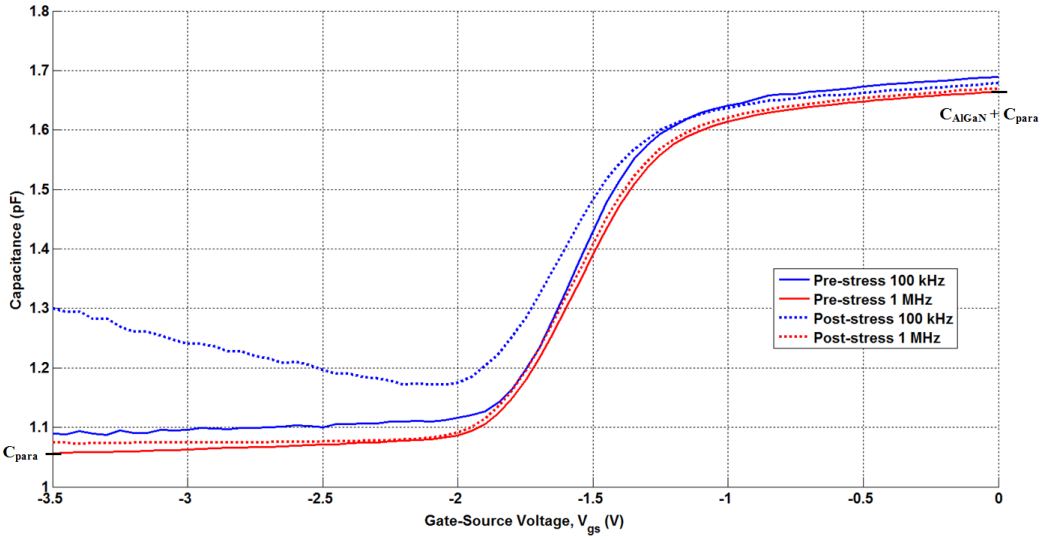

Figure 6-10: Pre- and post-stress C-V curves at 100 kHz and 1 MHz.

The 1 MHz C-V curve in Figure 6-10 shows two additional parameters. C_{para} is the sum of all the parasitic capacitance due to the physical structure of the device such as the gate-source capacitance and gate-drain capacitance which offsets the capacitance curve. The average C_{para} = 1.057 pF. C_{AlGaN} is the capacitance of the AlGaN when the 2DEG is fully populated. Using ε_{AlGaN} = 9, t_{AlGaN} = 17.5 nm, and a gate area of 150 µm x 0.50 µm in Equation (5-2), then the theoretical AlGaN capacitance is $C_{AlGaN,th}$ = 0.342 pF [13]. The measured C_{AlGaN} ranges from 0.549 pF to 0.614 pF which supports $C_{AlGaN,th}$ when considering

small dimensional deviations in the manufacturing process, stray capacitances from the measurement setup, and a non-ideal, leaky AlGaN dielectric.

6.2.1 Number of Charge Carriers in the Channel

For an ideal voltage dependent capacitance, the total charge on one side of the capacitor is calculated using Equation (6-4) where C(V) is the voltage dependent capacitance without the C_{para} offset. Integrating Equation (6-4) results in the total charge, Q_{tot}, over the range V = V_1 to V_{gs} in Equation (6-5). Dividing Q_{tot} by q results in the total number of electrons in the channel under a particular bias condition. Figure 6-11 shows the resulting N(V_{gs}) plot derived from the C-V characteristic curve if V_1 = -3.5 V where the channel is in cutoff and approximately depleted of carriers. N will be used in §6.3.4 to calculate the Hooge parameter from Equation (3-15).

(6-4) $$dQ = C(V)dV$$

Q = Total charge [eV]

C(V) = Voltage dependent Capacitance [F]

V = Voltage [V]

(6-5) $$N(V_2) = \frac{Q_{tot}}{q} = \frac{1}{q}\int_{V_1}^{V_2} C\, dV_{gs}$$

N = Number of electrons

q = electron charge [eV]

V_{gs} = Gate-source voltage [V]

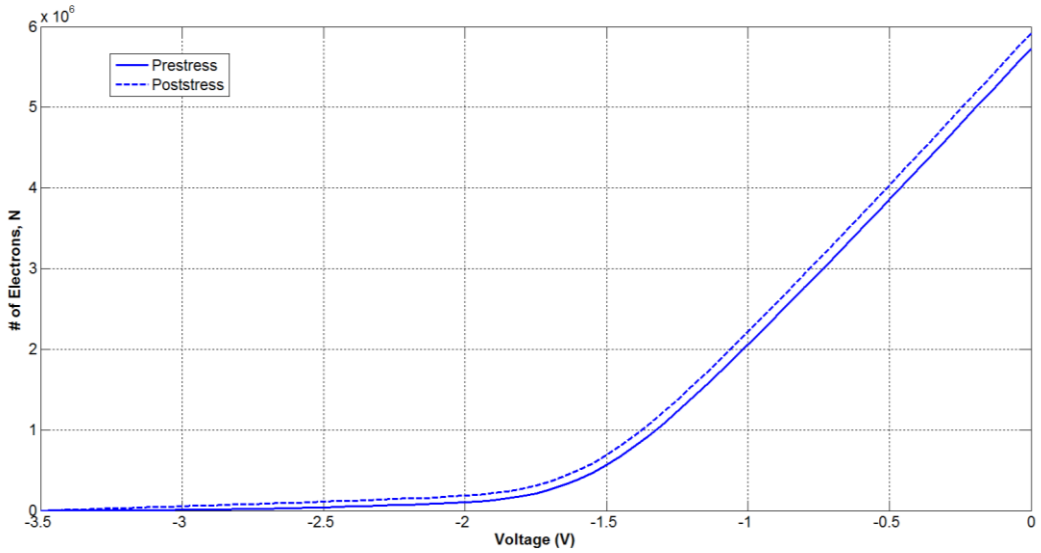

Figure 6-11: $N(V_{gs})$ from Equation (6-5) where N(0) is the total number of electrons in the channel at V_{gs} before and after stress.

From Table 2-1, GaN HEMTs have sheet carrier concentrations in the range of 10^{13} electrons/cm^2. A quick estimate using a gate width of 0.5 μm and length of 150 μm results in 75 μm^2 gated area. The approximate number of channel electrons is $7.5 \cdot 10^6$ electrons and consistent with the magnitude in Figure 6-11.

6.3 Effects of Gate Stress on Low Frequency Noise

This section presents LFN using two different metrics, $S_{Ix}(f)$ and $S_{Ix}(f)/I_x^2$ where I_x represents the drain current, I_d, or the gate current, I_g. $S_{Ix}(f)$ is the absolute noise power density in A^2/Hz while $S_{Ix}(f)/I_x^2$ is the *normalized* power spectral density in units of 1/Hz. $S_{Ix}(f)$ is used to compare absolute power changes and for comparing LFN between temperature and bias such as in noise factor calculations. $S_{Ix}(f)/I_x^2$ compares LFN while removing the effect of current. Both types will be used in this section to establish patterns between gate stress, LFN, and other measurements. Under cutoff bias conditions, the 1 Hz intercept,

or the value at f = 1 Hz of the trend line applied to each spectral data set, is used to quantify the magnitude of $S_{Id}(f)/I_d^2$ instead of the Hooge parameter, because no method for extracting N is known when the device is operating in cutoff mode.

This section starts by justifying how LFN probes each region of the device in various bias modes utilizing the modified LFN model in Figure 6-5. Observations and analysis of LFN under cutoff and triode bias are presented.

6.3.1 Identifying the LFN Generating Regions Based on Device Bias

LFN can be used to probe different regions of the HEMT material to identify electron traps and measure the quality of the materials, but with multiple regions within the HEMT that generate LFN, how do we know which region is being probed? The LFN model change in Figure 6-5 complicates the explanation from [43], so a modified proof must be introduced to justify the LFN analysis.

LFN Origins Under Cutoff Bias

Under cutoff bias conditions, we assume R_s, $R_d << R_{gs}$, R_{gd}, R_{ch} which simplifies Figure 6-5 to a Δ configuration. With known I_d, I_g, V_{ds}, and V_{gs}, I_s and V_{gd} can be calculated; however, the linear system of equations results in an infinite solution set for R_{gs}, R_{gd} and R_{ch}. Because these values are unknown, no assumptions can be made using a mathematical circuit analysis approach to determine which resistances, if any, dominate. However, the current measurements from Figure 6-12 before and after stress show that I_s does not increase with V_{ds} as would be expected if current was conducting through R_{ch}. This indicates $R_{ch} >> R_{gs}$ and $R_{ch} >> R_{gd}$ allowing R_{ch} to be modeled as an open circuit when the device is in cutoff. Since a negligible amount of current flows through R_{ch} compared to R_{gs} and R_{gd}, LFN under cutoff conditions is probing the

AlGaN region where electrons flow from gate to source and gate to drain as demonstrated in Figure 6-13. The location of the noise generator when measuring gate and drain noise (drain side or source side) is not known using this analysis.

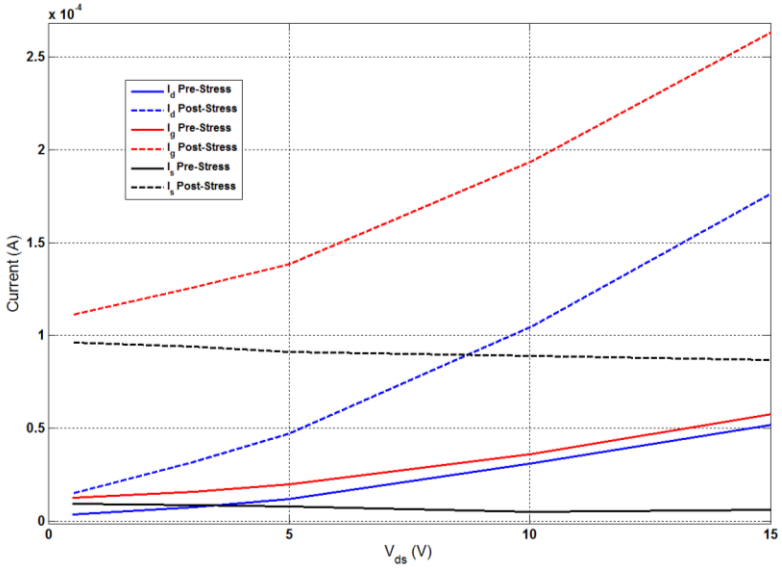

Figure 6-12: I_d, I_g and I_s with varying V_{ds} shows that I_s is independent of V_{ds}.

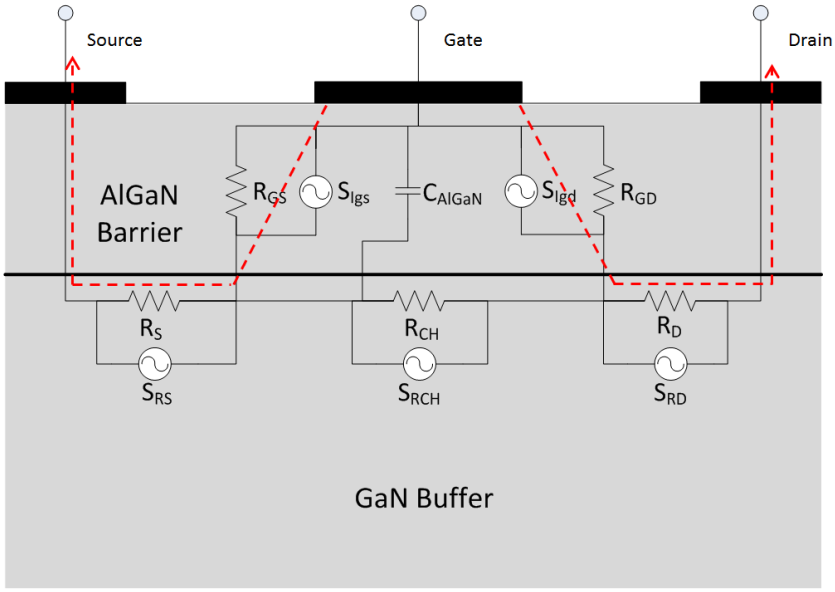

Figure 6-13: Current flow through the equivalent circuit model under cutoff conditions assuming $R_{ch} >> R_{gs}$, R_{gd} (Note: path does not represent the physical path electrons follow).

Assuming that the noise sources for the remaining resistors (S_{Rgs} and S_{Rgd} for R_{gd} and R_{gd}) are uncorrelated, the short circuit gate current noise is found using Equation (6-6) and the short circuit drain current noise is found from Equation (6-7).

(6-6) $$\frac{S_{Ig}}{I_g^2} = \frac{S_{Rgd}}{R_{gd}^2}\left[\frac{R_{gd}^2}{\left(R_{gs}||R_{gd}\right)^2}\right] + \frac{S_{Rgs}}{R_{gs}^2}\left[\frac{R_{gs}^2}{\left(R_{gs}||R_{gd}\right)^2}\right]$$

S_{Rgd} = uncorrelated gate-to-drain noise

S_{Rgs} = uncorrelated gate-to-source noise

(6-7) $$\frac{S_{Id}}{I_d^2} = \frac{S_{Rgd}}{R_{gd}^2}$$

The remaining resistor values are calculated before and after stress in Table 6-1. Since R_{gd} and R_{gs} are similar in value, no assumptions can be made to simplify Equation (6-6) and no method is known for isolating the 1/f noise sources in the AlGaN even with Equation (6-7). One possible way to differentiate between the drain and source noise components is looking at the Lorentzian components generated by RTS noise. If the RTS noise appears in S_{Id} then the RTS noise generator is located between the gate and drain side of the channel. If RTS noise appears in S_{Ig} and not S_{Id}, then the RTS noise is located on the source side of the AlGaN. Unfortunately, too few RTS noise components were observed in the sample devices to confirm or reject this hypothesis. Future research should pursue separating the gate-source and gate-drain noise to narrow down where

defects are generated. This could possibly be done by varying both V_s and V_d and observing the changes in LFN and the presence of RTS noise.

Table 6-1: Equivalent Circuit Model Gate Resistance Values Before and After Stress

	Before Stress		After Stress		Decrease Due to Stress	
	Range	Average	Range	Average	Range	Average
R_{gd}	296 kΩ – 405 kΩ	325 kΩ	88 kΩ – 208 kΩ	139 kΩ	86 kΩ – 257 kΩ	187 kΩ
R_{gs}	281 kΩ – 10.25 MΩ	1.20 MΩ	26.8 kΩ – 42.8 kΩ	32.4 kΩ	251 kΩ – 10.21 MΩ	409 kΩ

LFN Origins Under Triode Bias

Under triode bias conditions, the analysis in [43] can still be applied despite the change in noise model. $S_{Id}(f)$ probes the drain noise because it is assumed that when the device is operating in the triode region, that $R_{ch}, R_s, R_d << R_{gs}, R_{gd}$, so a majority of the current flows from drain to source. Based on I_{ds} and V_{ds} measurements during LFN, $R_{ch} + R_s + R_d$ reaches a maximum of 113 Ω at V_{gs} = -1.6 V compared to the findings in Table 6-1 (under different bias conditions, the order of magnitude difference of Table 6-1 still support the statement that $R_{ch}, R_s, R_d << R_{gs}, R_{gd}$). Since LFN is due to conductance fluctuations, Δσ, and current is required to reveal the low frequency Δσ deviations, LFN is generated in R_{ch}, R_d, and R_s. Assuming the remaining noise sources are uncorrelated, the normalized drain noise is found from Equation (6-8) [43].

$$\frac{S_{Id}}{I_d^2} = \frac{S_{Rch}}{R_{ch}^2}\left[\frac{R_{ch}^2}{(R_s+R_d+R_{ch})^2}\right] + \frac{S_{Rd}}{R_d^2}\left[\frac{R_d^2}{(R_s+R_d+R_{ch})^2}\right] + \frac{S_{Rs}}{R_s^2}\left[\frac{R_s^2}{(R_s+R_d+R_{ch})^2}\right] \quad (6\text{-}8)$$

S_{Rch} = Uncorrelated channel resistance noise.

S_{Rd} = Uncorrelated drain resistance noise.

S_{Rs} = Uncorrelated source resistance noise.

Based on Equation (6-8), it is clear that R_{ch}, and therefore S_{Rch}, is the only term dependent on V_{gs}, which can be exploited to show that drain noise dependency on V_{gs} indicates noise generated in the channel by R_{ch} [59]. Two important relationships must first be introduced. The first relation, in Equation (6-9), shows that $R_{ch} \propto V_{gs}^{-1}$ based on the basic calculation for calculating R_{ch} for a FET device operating in the triode region. Second, Equation (6-10) shows the method for calculating the total number of electrons in the channel, N, which shows $N \propto V_{gs}^{1}$.

(6-9) $$R_{ch} = \frac{V_{ds}}{I_{ds}} = \frac{V_{ds}}{\frac{W}{L}\mu C_{AlGaN}(V_{gs}-V_{th}-V_{ds})} \propto \frac{1}{V_{gs}}$$

(6-10) $$N = \frac{C_{eq}}{q}\left(V_{gs} - V_{th}\right) \propto V_{gs}$$

Rewriting Equation (3-15) for calculating the Hooge parameter results in Equation (6-11) where S_{Rt} is the sum of the uncorrelated noise sources comprised of the component in Equation (6-12).

(6-11) $$\frac{S_{Id}}{I_d^2} = \frac{S_{Rt}}{R_t^2} = \frac{S_{Rd}+S_{Rch}+S_{Rs}}{(R_s+R_{ch}+R_d)^2}$$

(6-12) $$S_{Rd} = \frac{\alpha_d R_d^2}{N_d f}, \qquad S_{Rch} = \frac{\alpha_{ch} R_{ch}^2}{N_{ch} f}, \qquad S_{Rs} = \frac{\alpha_s R_s^2}{N_s f}$$

If S_{Rch} is the dominant LFN noise source ($S_{Rch} > S_{Rd}$ and $S_{Rch} > S_{Rs}$) but $R_s + R_d > R_{ch}$, then reducing Equation (6-11) and substituting Equation (6-12) results in Equation (6-13). This shows, based on the relations in Equations (6-9) and Equation (6-10), LFN dominated by the channel is predicted to have the form $S_{Id}/I_d^2 \propto V_{gs}^{-3}$.

(6-13) $$\frac{S_{Id}}{I_d^2} = \frac{S_{Rch}}{(R_s+R_d)^2} = \frac{\alpha_{ch} R_{ch}^2}{N_{ch} f (R_s+R_d)^2} \propto V_{gs}^{-3}$$

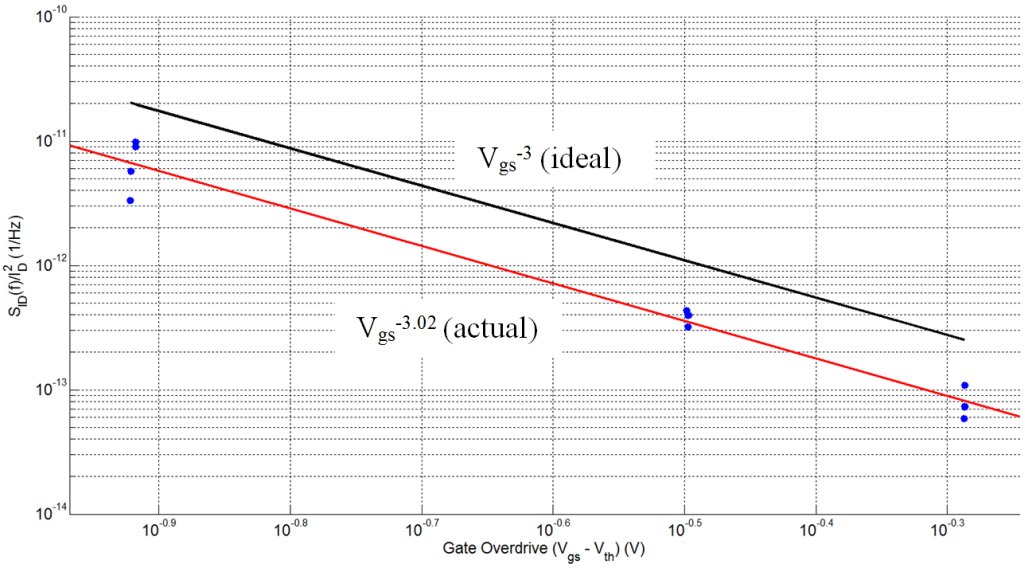

Figure 6-14: Example plot of S_{Id}/I_d^2 at 200 Hz shows $S_{Id}/I_d^2 \propto V_{gs}^{-3.02}$.

The results of S_{Id}/I_d^2 versus gate overdrive voltage, $V_{gs} - V_{th}$, in Figure 6-14 depict the trend predicted by Equation (6-13). This trend occurs at all temperatures before and after stress. At 200 Hz, the slopes range from $V_{gs}^{-2.54}$ to $V_{gs}^{-3.18}$ and at 1 kHz, slopes range from $V_{gs}^{-2.4}$ to $V_{gs}^{-3.2}$. Stress is not expected to alter this relationship since, even after stress, R_{gd} and R_{gs} are much larger than R_{ch} based on DC current measurements under triode bias conditions where I_d is 100 to

1000 times greater than I_g. Deviations from V_{gs}^{-3} are expected since there are RTS noise components that disrupt the pure 1/f noise trend. The occurrence of RTS noise and the frequency at which it is centered is not consistent, and RTS noise is not related to V_{gs}^{-3} [31]. This analysis only applies to the device when it is operating in the triode region where $V_{gs} > V_{th}$, which, in this testing, only consisted of three V_{gs} values. More V_{gs} bias voltages should be selected in future research to more reliably demonstrate this point. An additional case that was expected but not observed due to the lack of V_{gs} resolution is $S_{Id}/I_d^2 \propto V_{gs}^{-1}$ when $R_{ch} > R_d + R_s$ [59]. This occurs when V_{gs} is close to V_{th} in the triode region where fewer electrons are populating the 2DEG causing R_{ch} to increase. Again, smaller V_{gs} increments would confirm this relationship.

The justification for gate noise probing the AlGaN region beneath the gate contact under triode bias conditions only changes slightly from [43] with the modified HEMT noise model in Figure 6-5. Under triode bias conditions, current flows from the gate to the drain through the AlGaN. Since it has been previously shown that $R_{ch} << R_{gs}$ and $R_{ch} << R_{gd}$, the analysis of the original noise model in Figure 3-5 where $R_{g,eq} = R_{gs} \parallel R_{gd}$ can be applied. Assuming the noise is comprised of uncorrelated noise sources, the gate noise is calculated from Equation (6-14). Assuming that $R_{g,eq}$ is the dominant resistance and S_{Rg} is the dominant LFN source, then this equation reduces to Equation (6-15) which shows that, under triode bias conditions, S_{Ig}/I_g^2 probes the gate stack region.

(6-14)
$$\frac{S_{Ig}}{I_g^2} = \frac{S_{Rg,eq}}{R_{g,eq}^2}\left[\frac{R_{g,eq}^2}{(R_s+R_{g,eq})^2}\right] + \frac{S_{Rd}}{R_d^2}\left[\frac{R_d^2}{(R_d+R_{g,eq})^2}\right]$$

(6-15) $$\frac{S_{Ig}}{I_g^2} = \frac{S_{Rg}}{R_{g,eq}^2}$$

In summary, this analysis has concluded that noise produced under cutoff bias conditions originates in the AlGaN and is composed of noise on the source and drain side of the gate stack. Under triode bias conditions, drain noise probes the channel region while gate noise probes the AlGaN region.

6.3.2 LFN Under Cutoff Conditions

A sample pre- and post-stress drain LFN spectrum under cutoff conditions (which probes the drain side of the gate stack region) is shown in Figure 6-15. The pre-stress $S_{Id}(f)$ 1 Hz intercept point varies from $3.41 \cdot 10^{-17}$ A^2/Hz^{-1} to $2.16 \cdot 10^{-14}$ A^2/Hz^{-1} for all bias conditions and temperatures. The post-stress 1 Hz intercept points range from $4.34 \cdot 10^{-16}$ A^2/Hz^{-1} to $1.1 \cdot 10^{-13}$ A^2/Hz^{-1} and is characterized by more uniform 1/f spectra than the pre-stress case. There is a clear increase in the 1 Hz intercept point which is due to the increase in I_d after stress illustrated in Figure 6-6 and Figure 6-12. Also, the 1 Hz intercept point also increases with increasing V_{ds} in both the pre- and post-stress spectra, but this is due to the increase in I_d associated with higher V_{ds} bias. Increased 1/f uniformity and high noise magnitude after stress due to the creation of new traps during stress and will be explored more in §6.3.3.

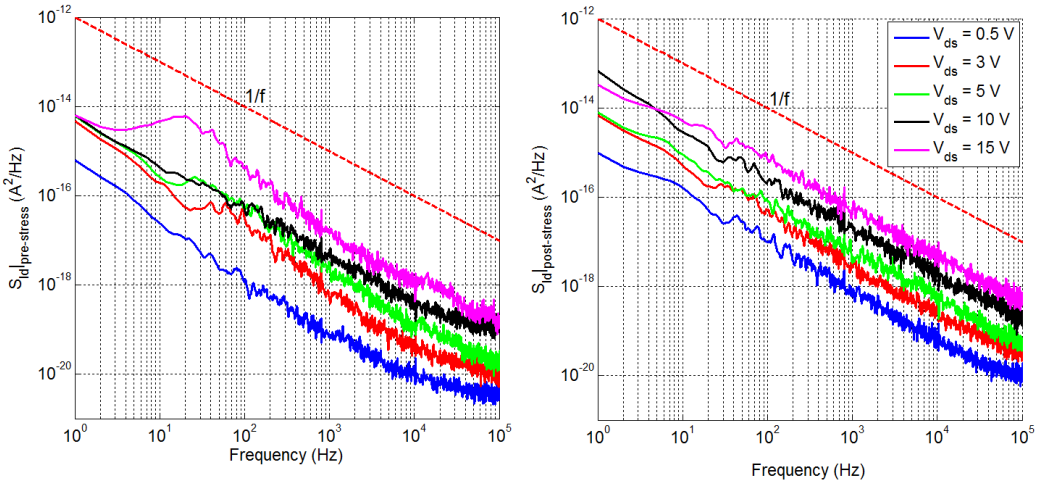

Figure 6-15: Drain LFN, $S_{Id}(f)/I_d$, under cutoff conditions before (left) and after (right) gate stress.

Figure 6-16 clearly demonstrates an increase in $S_{Id}(f)$ due to stress where $S_{Id}(f)|_{post\text{-}stress}/S_{Id}(f)|_{pre\text{-}stress} > 1$, as expected, so it was predicted that after stress, $S_{Id}(f)/I_d^2$ would be higher, quantified by a higher 1 Hz intercept point since more traps would lead to more noise generation as is the case when calculating the Hooge parameter. This is not true, however, as shown in Figure 6-17 where the data ranges from a maximum increase of 10^1 to a maximum decrease of 10^{-1} which suggests $\Delta S_{Id} \propto \Delta I_d^2$ where deviations from this relationship are due to the variations in noise measurements and presence of RTS noise before or after stress. This relationship is different than the Hooge parameter relations (where $S_{Id}(f)/I_d^2$ increases as the material degrades) because the primary mechanism for gate leakage is trap assisted tunneling as opposed to electrons moving to the conduction band through electric field excitation. Since a majority of electrons tunnel through the AlGaN via traps under cutoff bias conditions, an increase in I_d means more trapping and detrapping events are occurring leading to higher S_{Id}. A method for comparing I_d and $S_{Id}(f)$ between devices could not be established

based on the data collected which suggests that the trap distribution, g(τ), and density also affects the noise magnitude.

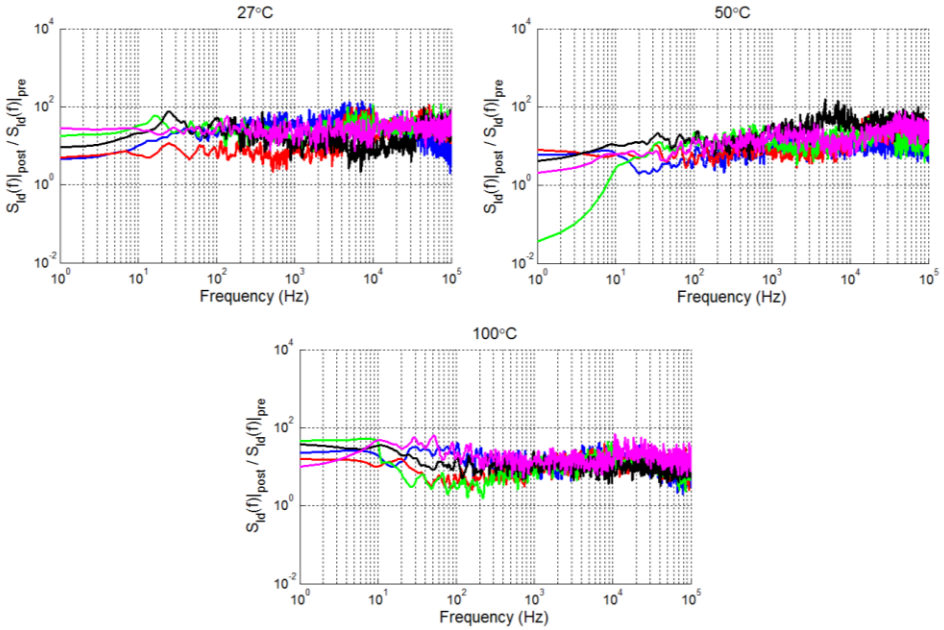

Figure 6-16: The ratio $S_I(f)|_{post\text{-}stress} / S_I(f)|_{pre\text{-}stress}$ shows a net increase in noise power after stress but no pattern with bias condition or temperature.

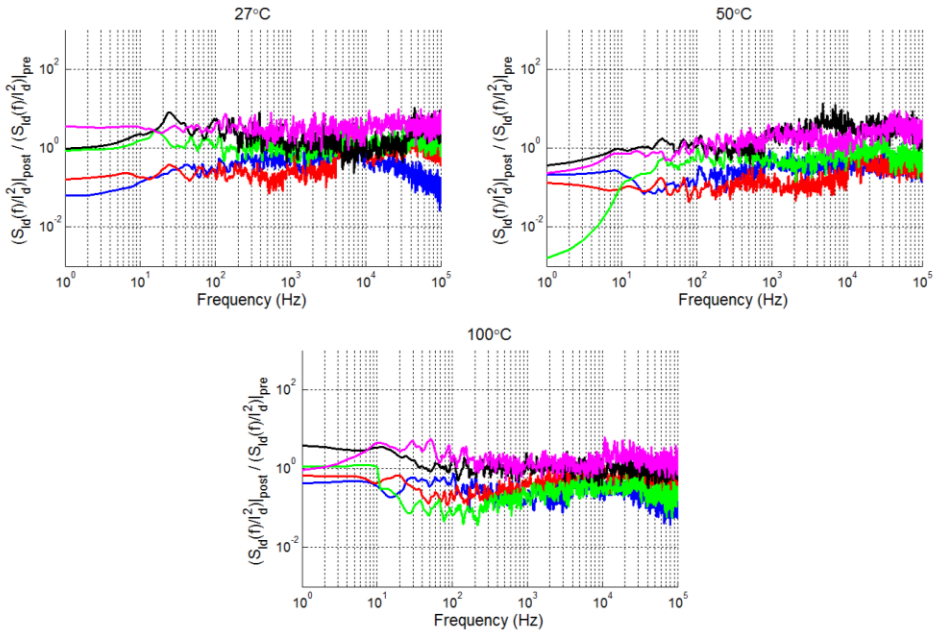

Figure 6-17: Ratio $[S_{Id}(f)/I_d^2]|_{post\text{-}stress} / [S_{Id}(f)/I_d^2]|_{pre\text{-}stress}$ stays near 1 with no clear pattern due to stress, bias condition, or temperature.

The gate LFN, $S_{Ig}(f)$, changes similarly to $S_{Id}(f)$ after stress. $S_{Ig}(f)$ increases after stress which is due to the increase in I_g after stress. The sample LFN spectra in Figure 6-18 clearly shows an increase in the 1 Hz intercept point after stress. In general, $S_{Ig}(f)$ increases more after stress than $S_{Id}(f)$ which is consistent with leakage current changes where I_g increases more than I_d. The measured pre-stress 1 Hz intercept points range from $3.3 \cdot 10^{-18}$ A^2/Hz to $6.07 \cdot 10^{-14}$ A^2/Hz while the post-stress 1 Hz intercept points range from $3.46 \cdot 10^{-17}$ A^2/Hz to $9.29 \cdot 10^{-12}$ A^2/Hz. The largest increases occurs at $V_{ds} = 0.5$ V which also coincides with the largest I_g increase as shown in Figure 6-19. It makes sense that the greatest change would occur at the lowest bias point, because those conditions experience the largest relative increase in I_g after stress, shown on the right axis of Figure 6-19. While higher V_{ds} results in higher noise magnitude due to higher I_g, this pattern is less prominent in the $S_{Ig}(f)$ spectra than the $S_{Id}(f)$ spectra because I_s is more significant compared to I_d after stress as displayed in Figure 6-6 and Figure 6-12. I_s only changes by about 10% from $V_{ds} = 0.5$ V to $V_{ds} = 15$ V resulting in $S_{Ig}(f)$ spectra similar in magnitude. The similar shape of the 1/f trend is due to trap formation after stress similar to $S_{Id}(f)$.

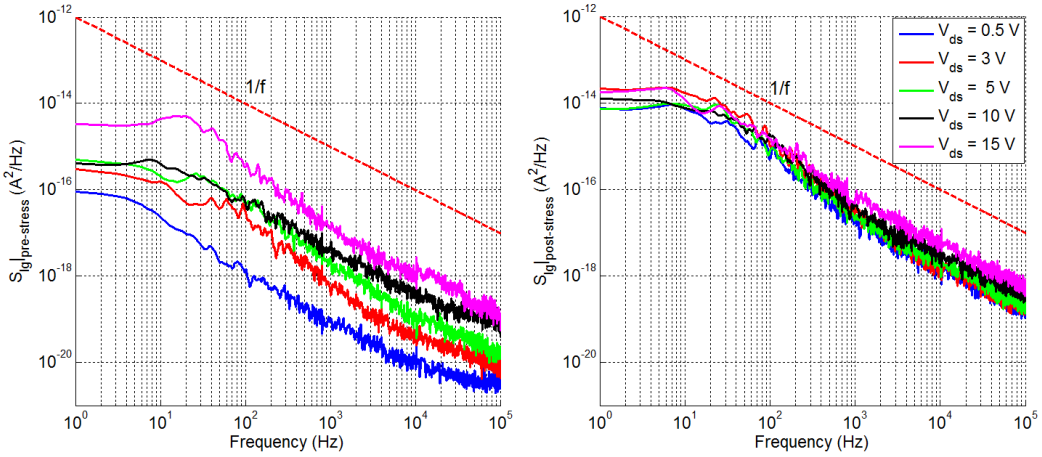

Figure 6-18: Gate LFN, $S_{Ig}(f)$, under cutoff conditions before (left) and after (right) gate stress.

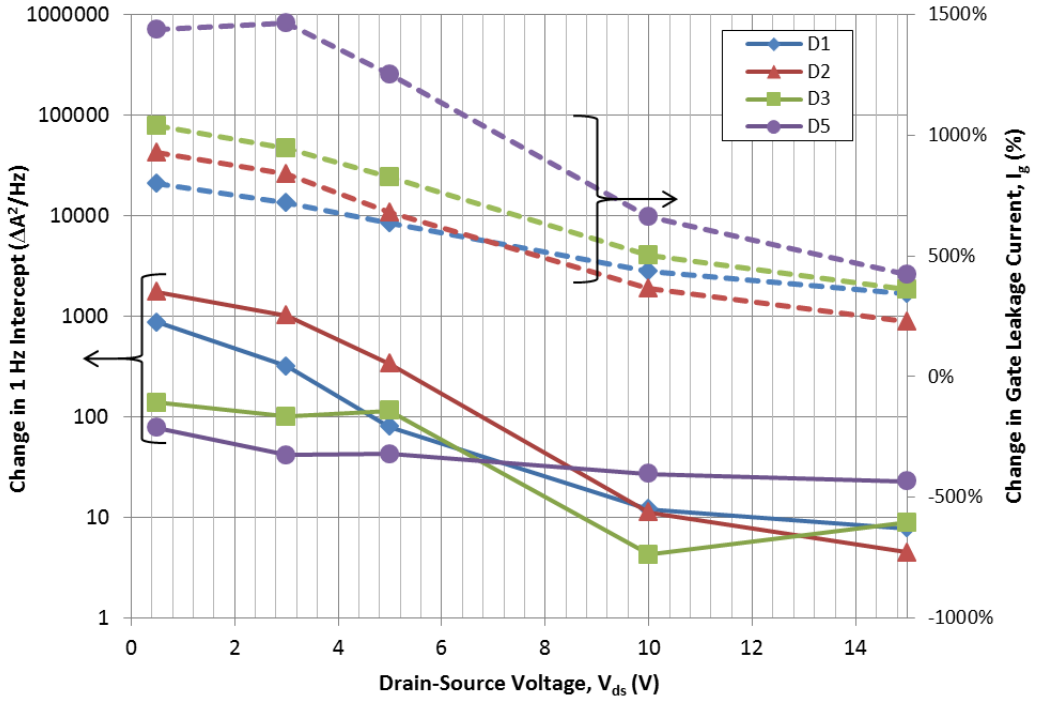

Figure 6-19: A comparison of the change in 1 Hz intercept point and change in gate leakage current, I_g, show similar decreasing trends with increasing V_{ds}.

One distinction between $S_{Ig}(f)$ and $S_{Id}(f)$ is the bump in the 1/f noise at frequencies below 100 Hz that only occurs in $S_{Ig}(f)$ as shown in Figure 6-18. This trend occurs consistently in all gate LFN measurement under cutoff and forward

active biasing. The data suggest the plateau below 20 Hz is actually stable, low frequency RTS noise which has been previous observed by Bosman and Rao [43]. The nature of this particular RTS noise is different, however, in that similar spectrums occur in different devices under different bias and temperature condition. The effect is not thought to be caused by the external circuitry, because the plateau magnitude varies between parts and by bias condition. The nature of RTS noise will be explored more in §6.3.5.

6.3.3 1/f Noise Characteristics of LFN Under Cutoff Conditions

Average γ measurements for gate and drain LFN in Figure 6-20 and Figure 6-21 show the LFN is closer to 1/f noise (γ=1) after stress which is also clear from observable trends of sample drain and gate LFN spectra in Figure 6-15 and Figure 6-18. At the drain, γ ranges from 0.80 to 1.34 before stress and from 0.85 to 1.28 after stress; the gate γ ranges from 0.79 to 1.33 before stress and 0.95 to 1.29 after stress. Recall from §2.3.3 that the trap time constant, τ, is thought to be related to the dislocation or defect depth behaving as a trap. Following this model, the change in LFN illustrated by $S_{Id}(f)$ is attributed to the creation of new traps that change the electron trap distribution, $g(\tau)$. The measured γ range before stress illustrates how trap creation during the manufacturing process leads to varying $g(\tau)$ distributions and γ values. After stress, however, the creation of traps changes γ to be closer to 1. McWhorter postulated that a homogeneous distribution of traps within the material would naturally create $g(\tau) = 1/\tau$ and $\gamma = 1$, so the change of γ indicates that gate stress creates new traps leading to a more homogeneous distribution of traps [41]. From a mechanical standpoint this makes sense because traps are defects or dislocations in the material crystalline

structure which naturally occur in the manufacturing process due to imperfect crystal creation through the introduction of foreign atoms and unintentional dopants into the material and, over time, by the inverse piezoelectric effect. A dislocation in the structure serves to relieve that particular area of mechanical stress and gives the atom more flexibility to move in the crystalline structure because it is missing a bond (or bonds) to neighboring atoms. Applying gate stress increases the mechanical forces on atoms that still have all (or most) of their bonds while the atoms missing bonds are free to move in space to reach static equilibrium. Meanwhile, excess force on the bonded atoms causes bonds to break resulting in additional defects and traps. These traps are mostly likely to form in areas where more bonds are intact because that material is more rigid creating more traps and changing $g(\tau)$ to be more homogenous.

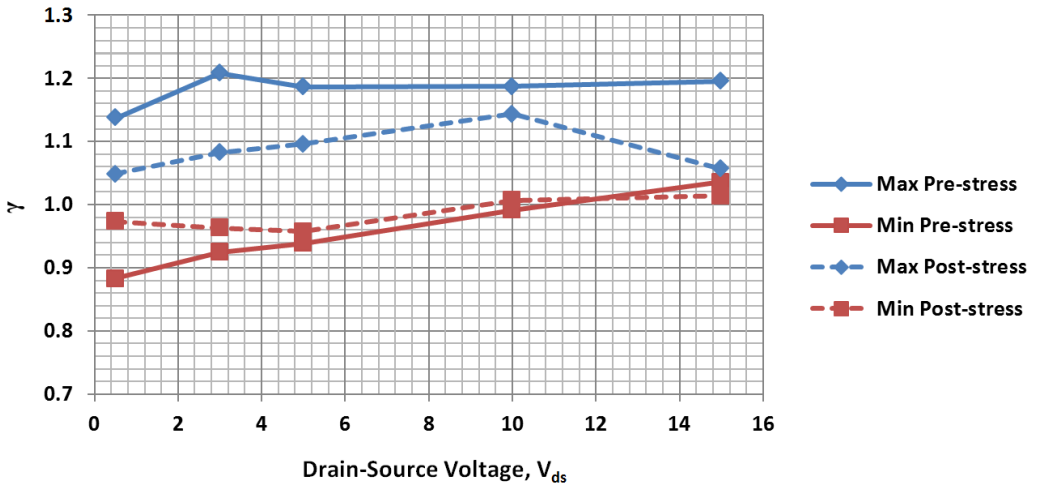

Figure 6-20: Drain average γ versus V_{ds} shows less deviation from ideal 1/f noise (γ=1) in LFN after stress.

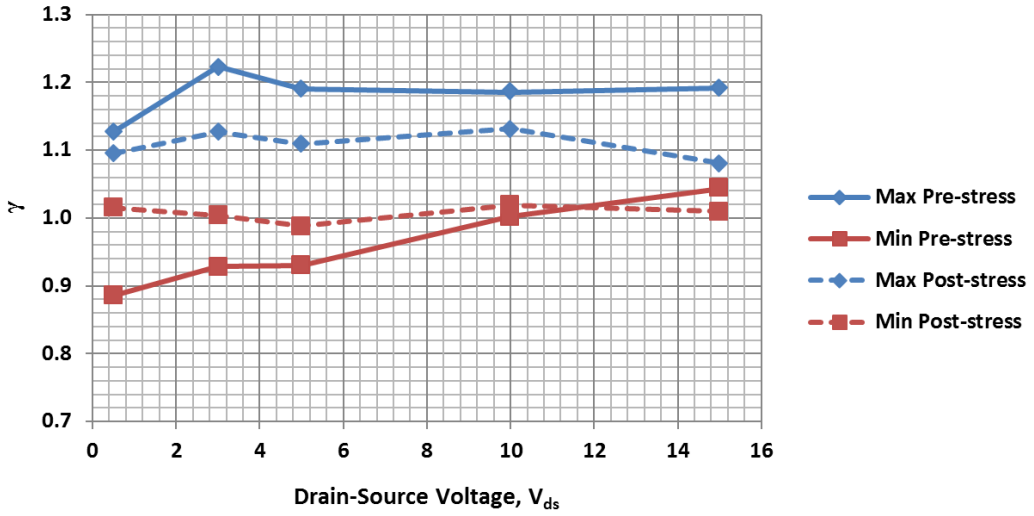

Figure 6-21: Gate average γ versus V_{ds} shows less deviation from ideal 1/f noise (γ=1) in LFN after stress.

If a device has a largely non-homogenous distribution of defects characterized by a LFN spectrum that deviates from γ = 1, then the device may be more susceptible to performance changes over its lifetime because regions in the AlGaN experience higher mechanical loads than other regions. If those mechanical loads experience additional stress, defects are more likely to form resulting in more traps, higher gate leakage due to trap assisted tunneling, and DC and RF performance changes associated with higher gate leakage (Q-point shift, lower drain saturation current, lower maximum output power, etc.). On the other hand, devices that start with γ ≈ 1 should experience fewer new defects when exposed to the same bias and environmental condition resulting in a more stable electrical performance. This suggests that in cases where consistent, long-term performance is crucial (such as in space applications), performing a burn-in on the device (at lower voltages than those used in this testing) prior installing the device may allow the circuit to perform more consistently. Future testing could

investigate this by performing two separate stress tests. The first low voltage stress (10 V to 30 V) breaks the bonds in regions already under high stress due to the manufacturing process resulting in a more homogenous distribution of trap energies. The second high voltage stress serves to further degrade the material. LFN would be measured before and after each stress and changes in LFN would be compared to the pre-stress LFN.

The pre-stress and post-stress gate and drain γ values in Figure 6-20 and Figure 6-21 are also remarkably similar to each other which suggests there may be a high correlation between gate and drain LFN. This supports the data presented in Figure 6-4 where a correlation between gate and drain noise under cutoff conditions exists because a high percentage of the gate current originates at the drain (under certain bias conditions).

6.3.4 Triode Bias and Hooge Parameter

Extracting the Hooge parameter, α, can only be done at the drain under triode bias conditions using existing methods. This is because the number of electrons in the channel, N, can be easily calculated using C-V measurements, whereas a method for determining the number of electrons conducting through the AlGaN to the gate is not known.

The Hooge parameters calculated from the LFN and C-V measurements range from $1.8 \cdot 10^{-5}$ to $1.8 \cdot 10^{-3}$ before stress and from $1.8 \cdot 10^{-5}$ to $3.5 \cdot 10^{-3}$ after stress, which are consistent with previously reported ranges for GaN HEMTs [43], [44], [60]. The average α values in Table 6-2 reveals that α increases after stress (except at V_{gs} = -1.2 V). Even though [43] used the same model parts,

proprietary design improvements by the manufacturer like contribute to slightly differing results in this research (the previous research occurred in 2009) [43].

Table 6-2: Average Hooge Parameters Before and After Stress

	Pre-Stress			**Post-Stress**		
V_{gs} (V)	**27˚C**	**50 ˚C**	**100 ˚C**	**27˚C**	**50 ˚C**	**100 ˚C**
-1.6	7.0E-04	7.0E-04	3.9E-04	1.1E-03	1.3E-03	8.8E-04
-1.4	8.4E-05	8.9E-05	7.9E-05	9.4E-05	1.1E-04	9.3E-05
-1.2	2.9E-05	3.3E-05	2.9E-05	3.3E-05	3.1E-05	3.1E-05

The Hooge parameter is inversely dependent on V_{gs} as shown in Figure 6-22 which has been observed in other research [43]. The influx of electrons dilutes the noise contributions of bulk traps in the AlGaN and surface traps near the 2DEG at the GaN/AlGaN heterojunction as $|V_{gs}|$ decreases and more electrons enter the 2DEG. As the device enters saturation, the amount of noise produced per electron decreases resulting in lower normalized noise ($S_I(f)/I^2$) and a lower α. α change before and after stress at the same V_{gs} has a negative feedback component; an increase in post-stress trapping/detrapping events leads to higher noise production and a decrease in α while a negative V_{th} shift due to stress causes α to decrease for the same V_{gs} bias. This means that modest α increases represent more degradation in the material. A way to offset this effect would be to adjust post-stress V_{gs} bias so the number of 2DEG electrons is equal to the pre-stress measurements.

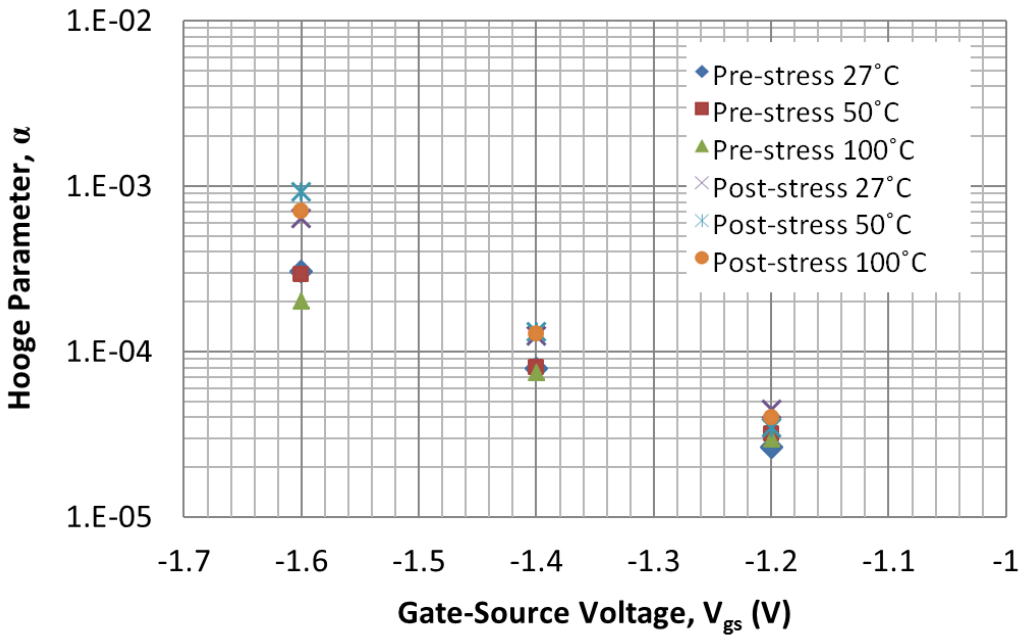

Figure 6-22: Hooge parameter dependence on V_{gs}.

6.3.5 RTS Noise, Activation Energy, and Trap Location

RTS noise observed in LFN is not necessarily created by a single trap or a group of traps with the same τ values but by a particular trap distribution, $g(\tau)$, which results in an overall RTS spectrum. With this in mind, references in this section to RTS noise with defined corner frequencies, f_o, and τ_{rts} values actually refer to the combination of traps that produce the RTS noise.

RTS noise is present in some of the gate and drain noise measurements at a variety of frequencies and in all of the gate LFN measurements below 20 Hz. It is helpful to present the noise as $f \cdot S_I/I^2$ so Lorentzian noise components appear as bumps on a horizontal spectrum with the center of the bump as the Lorentzian corner frequency, f_o. Figure 6-23 shows the typical S_I/I^2 representation of LFN and Figure 6-24 shows the $f \cdot S_I/I^2$ representation of the same data at 27˚C, 50˚C, and 100˚C. The red arrows show the approximate location of f_o for each

Lorentzian component. τ_{rts} is calculated from these estimates using Equation (6-16).

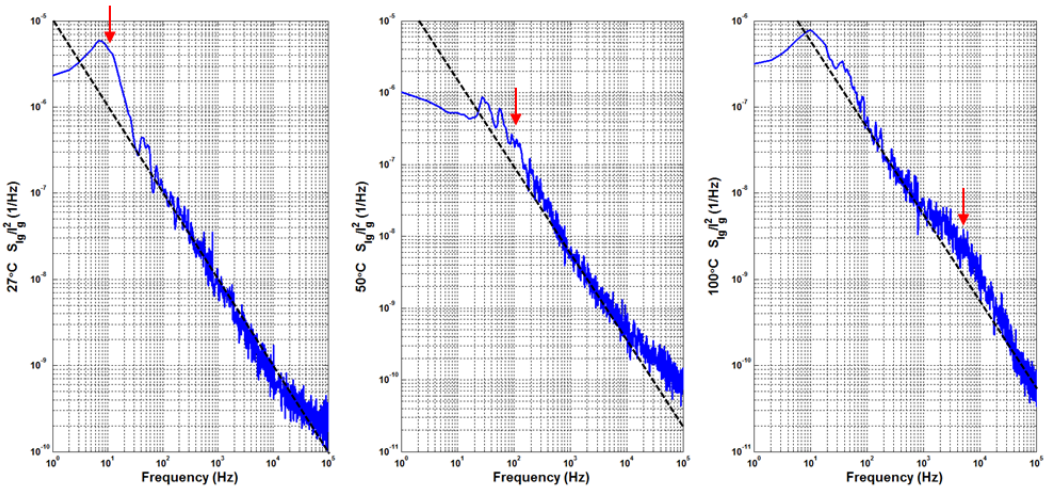

Figure 6-23: Typical LFN spectrum representation with a Lorentzian spectral component due to RTS noise present at all temperatures.

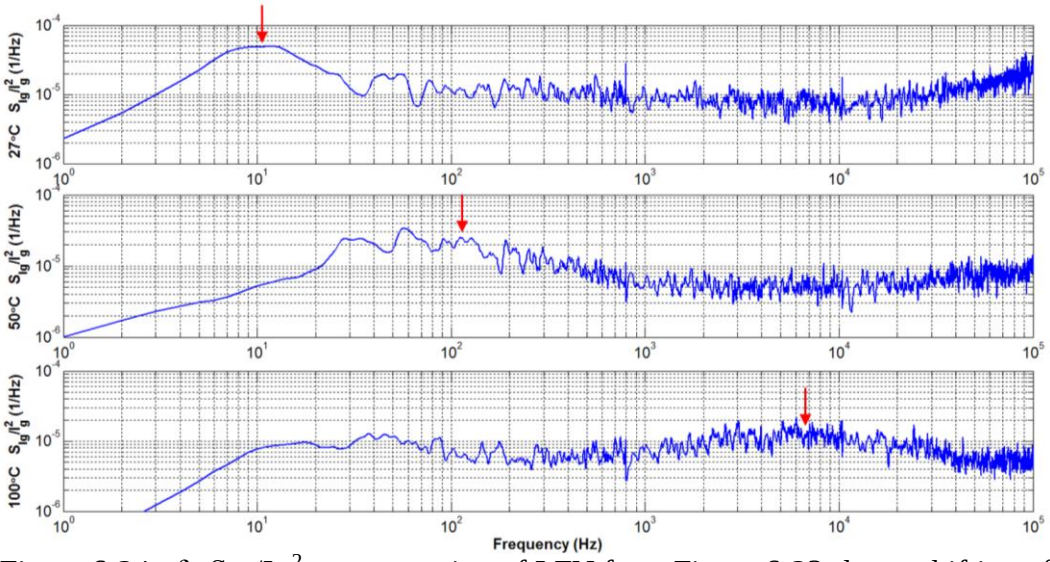

Figure 6-24: $f \cdot S_{Ids}/I_{ds}^2$ representation of LFN from Figure 6-23 shows shifting of RTS noise in the frequency domain with changing temperature.

(6-16) $$\tau_{rts} = \frac{1}{2\pi f_o}$$

Figure 6-24 shows a temperature dependent Lorentzian component that increases in frequency with increased temperature. This pattern is consistently repeated in cases where RTS noise is present at all three temperatures for the same bias condition. As mentioned in §6.3.2, the bumps on the gate LFN below 20 Hz are thought to be RTS noise due to the Lorentzian nature of the spectra. These bumps are used to identify the temperature dependent trends in this section.

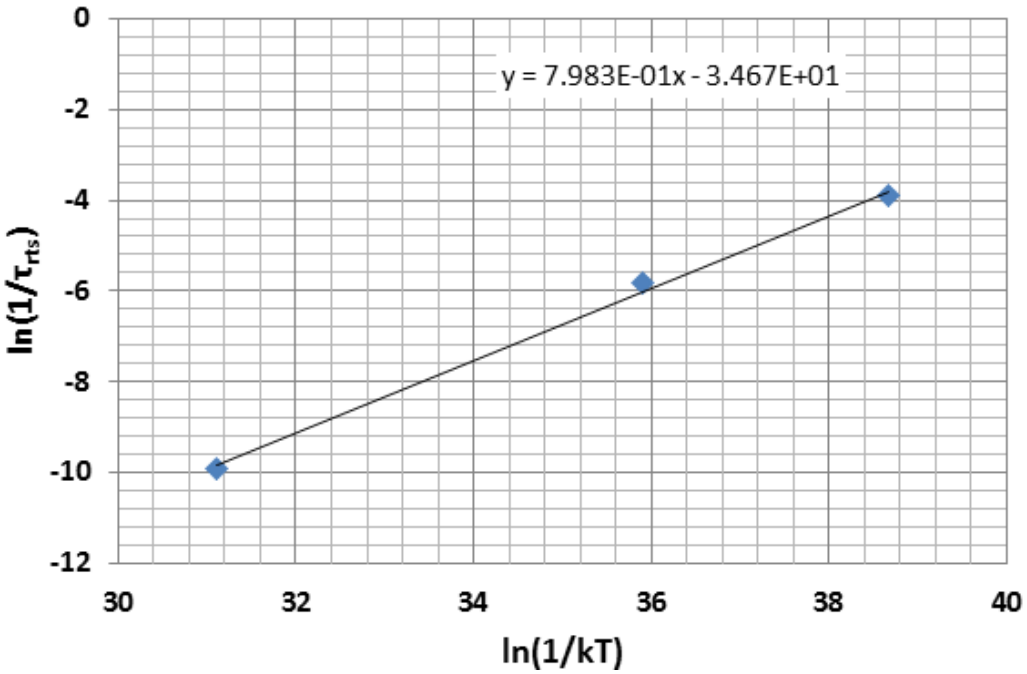

Figure 6-25: Arrhenius plot of the τ_{rts} values extracted from Figure 6-24 shows E_a = 0.7983 eV.

Table 6-3: Summary of RTS Noise Measurements

ID #	Conditions					RTS Corner Frequencies, f_o (Hz)			E_a (eV)
	Part Num.	Stress State	Term.	V_{gs} (V)	V_{ds} (V)	27˚C	50 ˚C	100 ˚C	
1	D1	Post	Gate	-1.8	0.02	6770	28400	74500	0.304
2	D1	Post	Gate	-1.6	0.02	4780	17000	70600	0.349
3	D1	Post	Gate	-1.4	0.02	4060	11400	66700	0.370
4	D1	Post	Gate	-1.2	0.02	3260	6940	84400	0.441
5	D2	Pre	Gate	-3.0	0.5	3	11	68	0.409
6	D2	Post	Gate	-3.0	0.5	920	4850	8200	0.269
7	D3	Pre	Drain	-3.0	0.5	12	110	7090	0.846
8	D3	Pre	Gate	-3.0	0.5	12	74	7040	0.855
9	D3	Pre	Gate	-3.0	3	12	185	6860	0.829
10	D3	Pre	Drain	-1.8	0.02	8	54	3200	0.798
11	D3	Post	Drain	-1.8	0.02	10	100	4910	0.818
12	D3	Pre	Drain	-1.6	0.02	6	36	2860	0.826
13	D3	Post	Gate	-1.8	0.02	10	66	3700	0.798
14	D3	Post	Gate	-1.6	0.02	10	33	3380	0.792
15	D3	Post	Gate	-1.4	0.02	7	40	2860	0.805
16	D3	Post	Gate	-1.2	0.02	6	41	2990	0.829
17	D5	Post	Gate	-1.2	0.02	560	1280	10400	0.392

The activation energy, E_a, of the trap can be found by calculating the slope of the Arrhenius plot data (plotting the $\ln(1/\tau_{rts})$ vs. $\ln[1/(kT)]$). The three temperatures used during testing, 27 ˚C, 50 ˚C and 100˚C, provide sufficient data to create the Arrhenius plot, although more temperatures should be included for higher accuracy. The trend line applied to the Arrhenius plot in Figure 6-25 based on the RTS noise in Figure 6-24 shows E_a = 0.798 eV. Table 6-3 summarizes the RTS noise found in all sample parts. This table only includes parts where RTS noise is clearly visible at all temperatures. There are more instances of RTS noise in addition to Table 6-3, but these RTS noise components were not found at each temperature so E_a could not be calculated. Table 6-3 reports *all* cases where RTS noise occurred at all three temperatures, and no E_a outliers were excluded.

Table 6-3 reveals a number of important observations about RTS noise. First, all calculated E_a range from 0.304 eV to 0.855 eV which falls within the range of the AlGaN band-gap (~6.3 eV) therefore making these measurements plausible. RTS noise E_a is also consistent with the thermionic trap assisted tunneling activation energies found in §6.1.1. E_a appears to be relatively similar within each device (ID#1-4, 5-6, 7-16). For instance, D3 ranges from 0.798 eV to 0.855 eV under varying bias conditions before and after stress. This suggests the traps that create RTS noise are unique to each device and most likely created by manufacturing variations. The fact that E_a in D3 only deviates by 0.057 eV when considering all D3 RTS noise (ID# 7-16) even after stress suggests that there may be a stress independent factor or mechanism creating the noise such as a cluster of dislocations or an unintentionally doped region. This is supported by the simulation of a group of traps with similar τ values, and therefore similar depths according to the McWhorter model, in Figure 3-2 where a group of τ values causes $g(\tau)$ to deviate from $1/\tau$. Furthermore, the fact that E_a only deviates by a total of 0.55 eV between all the devices suggests there are certain depths where RTS noise producing defect clusters tend to form. It is possible that certain regions of the AlGaN are more prone to defect creation or certain times during the manufacturing process where impurities have a higher probability of being introduced into the system. As mentioned in §2.3.1, tensile strain is strongest on the drain side of the gate near the gate contact so more defects are likely to form in this area which could contribute to the similar E_a values [23].

In the case of D3 under cutoff conditions, E_a is similar regardless of the measured terminal with RTS noise corner frequencies in similar locations (ID# 7, 8). The occurrence of RTS noise in both the gate and drain is likely if the RTS noise component is on the drain side of the gate stack causing the RTS noise to appears in both $S_{Ig}(f)$ and $S_{Id}(f)$ as discussed in §6.3.1.

The data from D2 under cutoff conditions (ID# 5,6) and D3 under triode bias conditions (ID# 10,11) indicates that the gate is more sensitive to gate stress than the region near the 2DEG. Gate E_a in D2 under cutoff conditions (V_{gs} = -3 V, V_{ds} = 0.5 V) *decreases* by 0.14 eV after stress as shown in Figure 6-26. This can be explained by the formation of new electron traps closer to the gate contact due to high field stress induced by the inverse piezoelectric effect. In this case, less energy would be required for an electron to tunnel through the AlGaN and enter the shallower trap resulting in a lower E_a. In addition, the frequency at which the RTS noise occurs is approximately two orders of magnitude higher after stress, which shows that the electron traps producing RTS noise are trapping and detrapping at a much faster rate. More frequent trapping and detrapping is consistent with lower energy; electrons have a higher probability of interacting with the trap and thus the events occur more frequently. On the other hand, drain E_a in D3 under triode conditions (V_{gs} = -1.8 V, $V_{ds} \approx$ 20 mV) *increases by* 0.0199 eV after stress. Since the drain LFN under triode bias conditions is probing traps near the 2DEG, this suggests that the channel is insensitive to gate stress. These occurrences were only documented once each, so more data is required to establish a pattern.

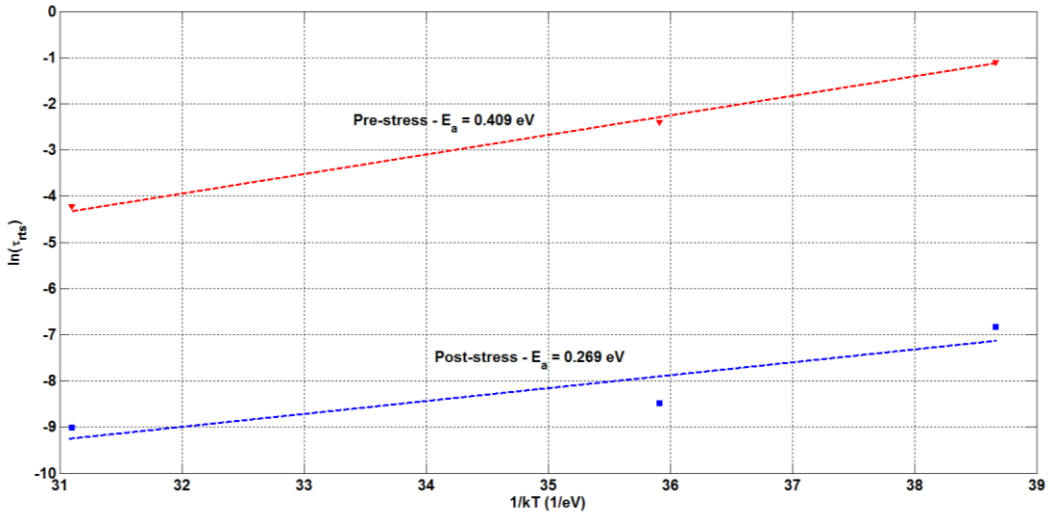

Figure 6-26: Arrhenius plot D2 RTS noise before (top) and after (bottom) stress.

RTS noise also appears to depend on bias voltage. The highlighted cells in Table 6-3 show a full set of V_{gs} values for D1 and D3 when the devices are under triode bias (ID# 1-4, 13-16). Figure 6-27 shows decreasing $|V_{gs}|$ leads to an increase in E_a. Decreasing $|V_{gs}|$ decreases the electric field magnitude the electrons at the gate are exposed to thereby requiring higher energy to tunnel to traps in the material. This is consistent with the decrease in I_g with decreasing $|V_{gs}|$ measured during LFN testing.

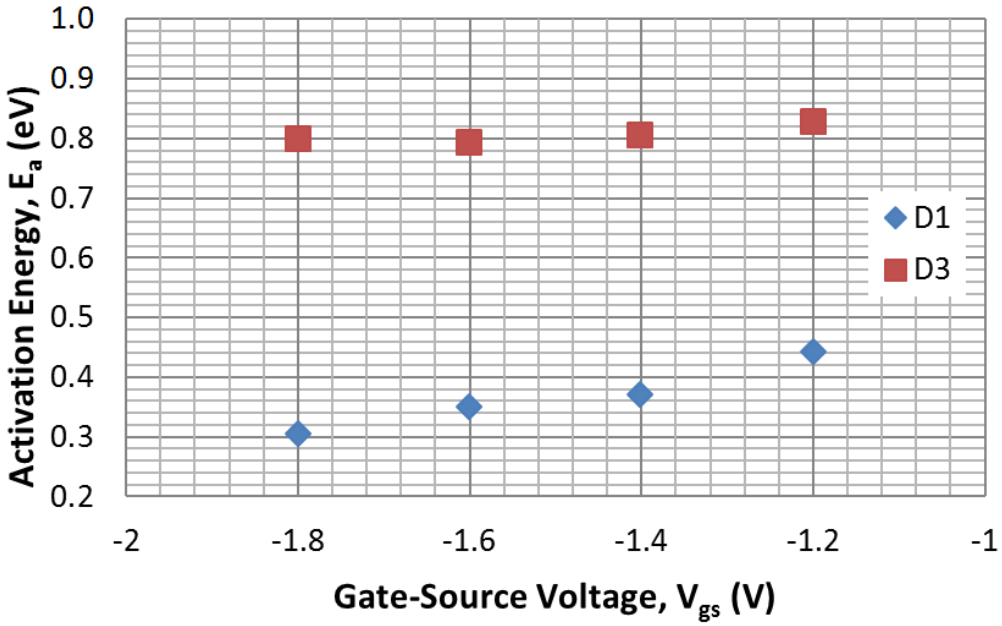

Figure 6-27: E_a increases with decreasing $|V_{gs}|$ for RTS noise measured at the gate under triode bias conditions.

Overall, 13 out of 17 of the RTS noise sources reported occur at the gate (ID# 1-6, 8-9, 13-17). This is most likely due to a combination of surface traps near the gate contact and traps in the AlGaN bulk, particularly under cutoff conditions, which would make RTS noise more common in $S_{Ig}(f)$. The reason RTS appears under certain temperature and bias conditions and not others is unknown. In some cases, the Lorentzian components may not be visible because they are too small in magnitude and covered by the 1/f noise or too high in frequency and covered by the thermal noise floor. Transient RTS noise has also been reported, so the Lorentzian components may just appear and disappear in time [43]. These causes are merely speculation and more research in this area needs to be conducted.

6.4 Miscellaneous Observations: Gate and Drain Noise Correlation

More investigation should be conducted into the existence of gate and drain noise correlation. As Figure 6-28 shows, in certain cases the gate and drain LFN have similar spectral shapes. One way this could happen is if the current flowing through the device under cutoff conditions flows through both the gate and drain. However, I_d only comprises 24% to 35% of I_g under the bias conditions in Figure 6-28 (V_{gs} = -3 V and V_{ds} = 0.5 V before pre-stress). The correlation between gate and drain noise could be due to exposure to the same traps in the AlGaN, but that correlation is expected to decrease as the I_d/I_g ratio decreases. More research needs to be conducted into this relationship to establish if the correlation is due to a common path traversed by the electrons from the gate to the drain or due to a different mechanism.

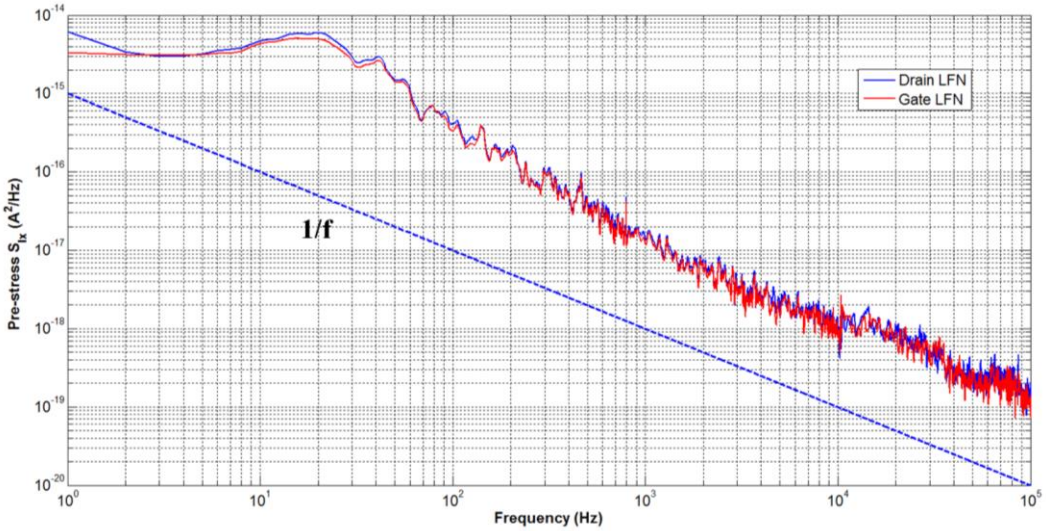

Figure 6-28: Comparison of S_{Ids} and S_{Ig} before stress shows correlation between gate and drain noise after stress when V_{gs} = -3 V and V_{ds} = 0.5 V.

Chapter 7: Conclusion

7.1 Conclusion

The focus of this research was to investigate the effects of gate stress on GaN-on-Si HEMTs by analyzing on changes in LFN under different bias conditions and junction temperatures before and after stress. The DC performance, C-V measurements and LFN data supports previous theories of degradation mechanisms through trap assisted tunneling. Results are consistent with the carrier fluctuation, Δn, theory of 1/f noise where the number of electrons fluctuates as they enter and exit electron traps producing Lorentzian noise spectra that sum to create 1/f noise.

The cutoff bias condition (V_{gs} = -3 V) probes the AlGaN bulk region which contains defects and impurities that act as electron traps leading to trap assisted tunneling. Gate leakage increases after gate stress due to additional trap generation caused by the inverse-piezoelectric effect. I_g increases by a factor of between 3 and 6 after stress. A comparison of drain and source current revealed that I_g primarily originates from the drain before stress (>90% at V_{ds} = 15 V), but has significant contributions from both drain and source after stress (approximately 50% each at V_{ds} = 15 V). This indicates that the drain and source side degrade at different rates due to gate stress, and that the source is more sensitive to high field stress most likely due to the shorter distance between the gate and source compared to the gate and drain. As a result, a new LFN model was generated to treat the source and drain sides of the gate stack as different resistances. LFN under cutoff bias also increase after stress due to the creation of new traps. It was found that $S_{Id}(f) \propto I_d^2$ which makes sense if traps are the

dominant noise source; an increase in I_g means more trapping/detrapping must occur as electrons tunnel from trap to trap in the AlGaN. This leakage mechanism is also time dependent, as shown by the C-V measurements taken at different AC frequencies, which is also consistent a trap assisted leakage mechanism where electrons remain trapped for a period of time before re-entering the conduction band.

McWhorter formulated that traps produce a Lorentzian spectrum and the resulting summation of the Lorentzian contributions from each trap result in the LFN spectrum. He also speculated that trap τ values can be related to trap depth in the material with higher time constants a result of higher energies required to trap and detrap. To produce a 1/f spectrum, $g(\tau) = 1/\tau$ which requires a homogeneous distribution of traps in the AlGaN. LFN measurements under cutoff conditions probed the AlGaN region and found that 1/f trends are more ideal after stress where γ at the drain ranges from 0.80 to 1.33 before stress and 0.85 to 1.28 after stress, and γ at the gate ranges from 0.79 to 1.33 before stress and 0.95 to 1.29 after stress. The change to a more ideal 1/f trend ($\gamma = 1$) indicates a shift in the $g(\tau)$ towards a more homogenous distribution of traps in the AlGaN which supports the theory that new traps are being created during stress.

Gate leakage was also found to have a temperature dependent component previously modeled as thermionic trap assisted tunneling. Pre-stress measurements support previously reported findings but are insufficient to draw further conclusions; however, a clear increasing I_g and I_d trend with temperature

appeared after stress. Temperature sensitivity has been recorded in other research, but this is usually at temperatures above 80˚C whereas the post-stress thermionic trap assisted tunneling was observed from 27˚C to 100˚C. The change is likely due to new, low energy traps created near the gate contact that make thermal excitation more probable.

The Hooge parameter, α, was calculated using the C-V measurements. The results show that α increases after stress; however, the cause of this change is inconclusive due to the V_{th} shift the devices experienced after stress. α is dependent on the number of electrons in the channel; as more electrons enter the 2DEG, the average noise produced by an electron decreases, because the increase in electrons dilutes noise generated by trapping and detrapping events. This means α depends on $V_{gs} - V_{th}$. The negative shift in V_{th} observed from the DC measurements could account for the slight increase in α observed after stress rather than the gate stress itself.

RTS noise in the form of bumps in the 1/f noise spectra were observed, and the corner frequencies and τ_{rts} values were found to increase at higher temperatures. Mathematical simulations show that RTS noise could actually be the product of a group of traps with similar τ values; as the temperature increases, the trapping and detrapping frequency increases, because less energy is needed to induce trapping or detrapping. As a result, the RTS noise corner frequency increases with increasing temperature. The resulting E_a values only vary by 0.55 eV which suggests RTS producing traps are located in similar regions between devices. The range of E_a values is also consistent with the thermionic

trap assisted tunneling mechanism observed in the DC measurements suggesting a common root cause.

7.2 Future Work

There are many areas from this work that can be expanded upon and many new questions that arise from these results that require further investigation. Many have already been introduced at various points in this thesis. In retrospect, the data collected in this thesis had a few shortcomings. First, this experiment should be reproduced with more temperature points spanning a wider range of temperatures. Previous works have explored GaN HEMT performance from 200 K to 500 K. A broader range of temperatures with more data points will provide more detail on the temperature related effects presented here. The triode bias test should also be conducted with more V_{gs} data points to obtain more clarity on bias related affects. This research could also be reproduced by applying a high asymmetric field stress with the device in cutoff mode and evaluating how the LFN, particularly of the channel, changes.

Other ideas were generated from this research but not tested. Based on the results here, this work can also be expanded by attempting to isolate the source and drain components of noise under cutoff bias conditions. This could be done by measuring gate, drain *and* source LFN and comparing the spectra to each other. Measuring the drain and source components of I_g under varying V_{gs} and V_{gd} biases would supplement the source LFN by varying V_s and leaving V_d and V_g constant. LFN data from all three terminals can also be compared to determine if a correlation exists. There is a clear gate and drain correlation based

on the evidence provided in this thesis, so additional work should be performed to determine if this correlation is a side-effect of the current flow or caused by another mechanism that causes noise sources to actually be correlated.

The findings for V_{crit} from the pre-test also introduce the need to determine how the device actually breaks down with stress. Although the inverse-piezoelectric effect is thought to be the main factor contributing to breakdown of the AlGaN, it is unclear what amount of stress causes breakdown and why some devices are more resilient to gate leakage current and stress than others.

One of the most interesting areas for future research is measuring C-V characteristics in small frequency steps. Data presented here show a frequency dependent mechanism that leads to drastically different capacitance measurements. However, too few frequencies were measured here to develop an understanding of why this is happening. This task has multiple components. First, identifying how the C-V characteristic changes with frequency before and after different gate stress will help identify how quickly the gate leakage mechanism is occurring. This can also be done at different temperatures to identify how the leakage mechanism changes with temperature. Next, the reason for the increase in capacitance at more negative V_{gs} presented in Figure 6-10 should be identified by performing C-V measurements at $V_{gs} < -3.5$ V. Characterizing the C-V curve at lower V_{gs} bias could provide addition insight into the presence of a hole generating mechanism, like in doped FET devices, or some other mechanism.

The research presented in this thesis shows many questions about GaN HEMT devices still linger. More investigation into the degradation mechanisms needs to be conductor. As this technology matures, cost and reliability will improve allowing for greater application of these devices.

References

[1] M. Shur, R. Gaska, A. Khan and G. Simin, "Wide Band Gap Electronic Devices," in Fourth IEEE International Caracas Conference on Devices, Circuits and Systems, Aruba, 2002.

[2] B. Ozpineci and L. M. Tolbert, "Comparison of Wide-Bandgap Semiconductors for Power Electronics Applications," Oak Ridge National Laboratory, 2003.

[3] Nitronex, LLC, "Nitronex.com," Nitronex, LLC, [Online]. Available: http://www.nitronex.com/products.html. [Accessed 16 July 2013].

[4] F. A. Marino, N. Faralli, D. K. Ferry, S. M. Goodnick and M. Saraniti, "Figures of Merit in High-Frequency and High-Power GaN HEMTs," Journal of Physics, vol. 193, p. 012040, 2009.

[5] W. Lu, J. Yang and I. A. M. Asiif Khan, "AlGaN/GaN HEMTs on SiC with over 100 GHz f_t and Low Microwave Noise," IEEE Transactions on Electron Devices, vol. 48, no. 3, pp. 581-585, 2001.

[6] W. S. Newham, "Development of AlGaN/GaN High Electron Mobility Transistors (HEMTs) on Diamond Substrates," Naval Postgraduate School, Monterey, CA, 2006.

[7] T. R. Lenka and A. K. Panda, "Characteristic study of 2DEG transport properties of AlGaN/GaN and AlGaAs/GaAs based HEMT," Semiconductors, vol. 45, no. 5, pp. 650-656, 2011.

[8] RFMD, "RFMD GaN Power Amplifiers," RFMD, [Online]. Available: https://estore.rfmd.com/RFMD_OnlineStore/Browse.aspx?Family=Amplifiers%20Family. [Accessed 16 7 2013].

[9] E. Mitani, M. Aojima, A. Maekawa and S. Sano, "An 800-W AlGaN/GaN HEMT for S-band High-Power Applications," in CS MANTECH, Austin, TX, 2007.

[10] U. Mishra, P. Parikh and Y. Wu, "AlGaN/GaN HEMTs: An Overview of Device Operation and Applications".

[11] B. G. Streetman, Solid State Electronic Devices, 4th ed., Englewood Cliffs, NJ: Prentice Hall, 1995.

[12] R. Vetury, "Polarization Induced 2DEG in AlGaN/GaN HEMTs: On the origin, DC and transient characterization," University of California, Santa Barbara, 2000.

[13] Nitronex, LLC, "AN-011: Substrates for GaN RF Devices," Nitronex, LLC, 2008.

[14] J. Osvald, "Polarization effects and energy band diagram in AlGaN/GaN heterostructure," Applied Physics A, vol. 87, pp. 679-682, 2007.

[15] Nitronex, LLC, "NPTB00004 Datasheet, NDS-002, Rev 6," Nitronex, LLC, Durham, NC, 2012.

[16] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard and W. L. Pribble, "A Review of GaN on SiC High Electron Mobility Power Transistors and MMICs," IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 6, 2012.

[17] Nitronex, LLC, "NPTB00004C Qualification Document, NGD-045, Rev. 1," Nitronex, LLC, 2007.

[18] M. Bloom, "DC, RF, and Thermal Characterizations of High Electric Field Induced Degradation Mechanisms in GaN-on-Si HEMTs," M.S. Thesis, Cal Poly, SLO, San Luis Obispo, 2013.

[19] Deltron AG, "Introduction of Thermoelectric Coolers," Deltron AG, Kirchberg, Switzerland.

[20] R. Ltd., "TriQuint RF Power Transistor: T1G6000528-Q3," TriQuint Semiconductor,[Online].Available: http://www.rfmw.com/ProductDetail/T1G6000528-Q3-TriQuint/403410/. [Accessed 13 February 2014].

[21] RFMD, "RFMD FR3930D 10W GaN on SiC Power Amplifier Die," RFMD, [Online]. Available: www.rfmd.com. [Accessed 13 February 2014].

[22] I. Cree, "Cree CGH40006P 8V RF GaN HEMT," Cree, Inc., [Online]. Available: www.cree.com. [Accessed 13 February 2014].

[23] J. A. d. Alamo and J. Joh, "GaN HEMT reliability," Microelectronics Reliability, vol. 49, pp. 1200-1206, 2009.

[24] S. Demirtas and J. A. d. A. Jungwoo Joh, "High voltage degradation of GaN High Electron Mobility Transistors on silicon substrate," Microelectronics Reliability, vol. 50, pp. 758-762, 2010.

[25] T. Mizutani, Y. Ohno, M. Akita, S. Kishimoto and K. Maezawa, "A Study on Current Collapse in AlGaN/GaN HEMTs Induced by Bias Stress,"

IEEE Transactions on Electron Devices, vol. 50, no. 10, pp. 2015-2020, 2003.

[26] P. Makaram, J. Joh, J. A. d. Alamo, T. Palacios and C. V. Thompson, "Evolution of structural defects associated with electrical degradation in AlGaN/GaN high electron mobility transistors," Applied Physics Letters, vol. 96, no. 233509, 2010.

[27] S. Y. Park, C. Floresca, U. Chowdhury, J. L. Jimenez, C. Lee, E. Beam, P. Saunier, T. Balistreri and M. J. Kim, "Physical degradation of GaN HEMT devices under high drain bias reliability testing," Microelectronics Reliability, vol. 49, no. 5, pp. 478-483, 2009.

[28] P. Dutta and P. M. Horn, "Low-frequency fluctuations in solids: 1/f noise," Reviews of Modern Physics, vol. 63, no. 3, pp. 497-516, 1981.

[29] R. H. Kingston and A. L. McWhorter, "Relaxation Time of Surface States on Germanium," Physical Review, vol. 103, no. 3, pp. 534-540, 1956.

[30] F. Li-Hua, L. Hai, C. Dun-Jun, Z. Rong, Z. You-Dou, W. Ke and L. Xin-Yu, "High-field-induced electron detrapping in AlGaN/GaN high electron mobility transistors," Chinese Physics B, vol. 21, no. 10, p. 108503, 2012.

[31] F. N. Hooge, "1/f Noise Sources," IEEE Transactions on Electron Devices, vol. 41, no. 10, 1994.

[32] D. J. Cheney, E. A. Douglas, L. Liu, C.-F. Lo, B. P. Gila, F. Ren and S. J. Pearton, "Degradation mechanisms for GaN and GaAs High Speed Transistors," Materials, vol. 5, pp. 2498-2520, 2012.

[33] Y. Chou, D. Leung, I. Smorchkova, M. Wojtowicz, R. Grundbacher, L. Callejo, Q. Kan, R. Lai, P. Liu, D. Eng and A. Oki, "Degradation of AlGaN/GaN HEMTs under elevated temperature life testing," Microelectronics Reliability, vol. 44, pp. 1033-1038, 2004.

[34] J. Choma, "Technical Report #USC 02-0511: Electronic Noise Characterization - Part 1: System Concepts and Theory," University of Souther California Viterbi School of Engineering, 2011.

[35] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 5th Edition, Hoboken, NJ: John Wiley & Sons, Inc., 2009.

[36] V. Mitin, L. Reggiani and L. Varani, Noise and Fluctuations Control in Electronic Devices, American Scientific Publishers, 2002.

[37] A. Konczakowska and B. M. Wilamowski, "Noise in Semiconductor Devices," in Fundamentals of Industrial Electronics, Boca Raton, FL, Taylor and Francis Group, 2011, pp. 11-5.

[38] L. M. Ward and P. E. Greenwood, "Scholarpedia: 1/f Noise," Scholarpedia,[Online]. Available: www.scholarpedia.org/article/1/f_noise. [Accessed 26 July 2013].

[39] C. Toro, "Improved 1/f Noise Measurements for Microwave Transistors," University of South Florida Scholars Commons - Theses and Dissertations, 2004.

[40] M. S. Keshner, "1/f Noise," Proceedings of the IEEE, vol. 70, no. 3, pp. 212-218, March 1982.

[41] A. L. McWhorter, "1/f Noise and Related Surface Effects in Germanium," Massachusetts Institute of Technology, 1955.

[42] F. Hooge, "1/f noise is no surface effect," Physics Letters A, vol. 29, no. 3, pp. 139-140, 1969.

[43] H. Rao and G. Bosman, "Simultaneous Low-Frequency Noise Characterization of Gate and Drain Currents in AlGaN/GaN High Electron Mobility Transistors," Journal of Applied Physics, vol. 106, pp. 1-4, 2009.

[44] C. Sanabria, "Noise of AlGaN/GaN HEMTs and Oscillators," M.S. Thesis, University of Santa Barbara, 2006.

[45] Nitronex, LLC, "AN-009: Bias Sequencing and Temperature Compensation for GaN HEMTs," 2008.

[46] Texas Instruments Inc., "Noise Analysis in Operational Amplifier Circuits, Application Report SLVA043B," 2007.

[47] Hewlett Packard, "Analysis of Semiconductor Capacitance Characteristics - Application Note 322," Hewlett Packard, 1989.

[48] Stauffer, Lee, "Fundamentals of Semiconductor C-V Measurements," Keithley Instruments, Inc., 2009.

[49] S. Karmalkar, D. M. Sathaiya and M. S. Shur, "Mechanism of the reverse gate leakage in AlGaN/GaN high electron mobility transistors," Applied Physics Letters, vol. 82, no. 22, pp. 3976-3978, 2003.

[50] D. M. Sathaiya and S. Karmalkar, "Thermionic trap-assisted tunneling model and its application to leakage current in nitride oxides and

AlGaN/GaN high electron mobility transistors," Journal of Applied Physics, vol. 99, no. 093701, 2006.

[51] H. Rao and G. Bosman, "Device reliability study of AlGaN/GaN high electron mobility transistors under high gate and channel electric fields via low frequency noise spectroscopy," Microelectronics Reliability, vol. 50, pp. 1528-1531, 2010.

[52] P. Valizadeh and D. Pavlidis, "Effects of RF and DC Stress on AlGaN/GaN MODFETs: A Low-Frequency Noise Based Investigation," IEEE Transactions on Device and Materials Reliability, vol. 5, no. 3, pp. 555-563, 2005.

[53] P. Valizadeh, "High-Temperature Very Low Frequency Noise-Based Investigation of Slow Transients in AlGaN/GaN MODFETs," IEEE Transactions on Device and Materials Reliability, vol. 8, no. 2, pp. 265-271, 2008.

[54] S. Turuvekere, N. Karumuri, A. A. Rahman, A. Bhattacharya, A. DasGupta and N. DasGupta, "Gate Leakage Mechanisms in AlGaN/GaN and AlInN/GaN HEMTs: Comparison and Modeling," IEEE Transactions on Electron Devices, vol. 60, no. 10, pp. 3157-3165, 2013.

[55] S. Arulkumaran, T. Egawa, H. Ishikawa and T. Jimbo, "Temperature dependence of gate-leakage current in AlGaN/GaN high-electron-mobility transistors," Applied Physics Letters, vol. 82, no. 18, pp. 3110-3112, 2003.

[56] D. Yan, H. Lu, D. Cao, D. Chen, R. Zhang and Y. Zheng, "On the reverse gate leakage current of AlGaN/GaN high electron mobility transistors," Applied Physics Letters, vol. 97, no. 153503, 2010.

[57] Y. A. Xi and E. Schubert, Determination of Al mole fraction in AlGaN by X-ray diffraction and optical transmittance, Lecture Notes, Rensselaer Polytechnic Institute.

[58] B. El-Kareh, "Properties and Structions of SiO2 and SiO2-Si Interface," in Fundamentals of Semiconductor Processing Technologies, Springer, 1994, p. 40.

[59] J.-M. Peransin, P. Vignaud, D. Rigaud and L. K. J. Vandamme, "1/f Noise in MODFETs at Low Drain Bias," IEEE Transactions on Electron Devices, vol. 37, no. 10, pp. 2250-2253, 1990.

[60] S. S. Hsu, P. Valizadeh and D. Pavlidis, "Characterization and Analysis of Gate and Drain Low-frequency Noise in AlGaN/GaN HEMTs," IEEE Lester Eastman Conference on High Performance Devices, 2002.