# HIGH VOLTAGE PULSE MEASUREMENT SYSTEM

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Master of Science in Electrical Engineering

by

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ABSTRACT

High Voltage Pulse Measurement System

Angelo J. Ballungay

Using isolation and noise immunity techniques, this thesis designs and constructs a low cost measurement system to safely and accurately measure high voltage, high frequency pulses in harsh EM environments. High voltage pulses apply to medical, plasma, and food industries. The difficulty of accurately measuring high voltage pulses continues to pose an issue. Measuring high voltage systems can cause damage to the system, the measurement system, and the user. High voltage and high frequency pulses create a harsh environment of electromagnetic fields that can disrupt the circuitry of the measurement system and harm the user. Implementing isolation from the high voltage system protects the measurement and user. An ideal pulse has sharp rising and falling edges, introduction high frequencies that prove difficult to sense and characterize. The measurement system requires a sufficiently large bandwidth to accurately measure the pulse edges. Commercial off the shelf pulse measurement systems such as oscilloscopes and multimeters cost thousands of dollars. Cheaper but simpler designs fail to provide isolation for safety. The measurement system in this thesis addresses all of these issues, allowing people to measure and characterize high voltage pulses.

Technologies used in this measurement network include optocouplers, transimpedance amplifiers, and analog-to-digital converters. The development process describes design, simulations, characterizations, construction, testing, and troubleshooting. Simulations show expected operations of components and characterizations assist in determining performance parameters of the system. Testing involves performing a low voltage test and a high voltage test and identifying limitations of the design. Finally, this thesis suggests future work to improve performance and lower cost of the measurement system.

ACKNOWLEDGMENTS

I would like to thank my committee for giving me the opportunity to present my thesis. I would like to especially thank Dr. Prodanov for mentoring me and offering his knowledge on the subject. Without him I would not have learned nearly as much through the development process of my thesis. I'd also like to thank my parents for their continued support throughout my college career.

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# 1. INTRODUCTION

## 1.1 Statement of Problem

High voltage pulse measurement applies to pulsed power machines such as rail guns and klystrons and pulse generators used for radar, medical technology, and food processing. Accurate measurements of systems and equipment provide important information for analyzing system waveforms including, shape, overshoot, ringing, peak voltages and frequencies. Good analysis allows determination of the measured systems performance, reliability, and efficiency parameters.

A pulse measurement instrument must therefore have high enough resolution along with bandwidth to accurately measure a signal with sharp edges at high voltages. The high currents at which the system operates at produce large magnetic fields according to Ampere's Law. Pulsed power tends to create harsh electrical and magnetic environments which make measurement systems susceptible to wave propagation effects, pickup of extraneous signals, stray capacitance, and residual inductance effects that distort the measurements of fast transients [1]. The measurement instrument needs to operate under these harsh conditions with accuracy and precision and provide protection from the measured system to avoid damage to the instrument and harm to the user.

Measurement instruments that address all of these issues prove difficult to find and tradeoffs generally occur. The pulsed power industry needs a low cost instrument that can address all of these problems to offer an alternative to expensive commercial instruments.

## 1.2 Motivation

The idea for a high voltage pulse measurement system originated with the Cal Poly Pulsed Power Club. The club constructed a rail gun powered by a pulse forming network (PFN), shown in Figure 1.1, that operates with system currents of 100 kA and voltages of 450 V.

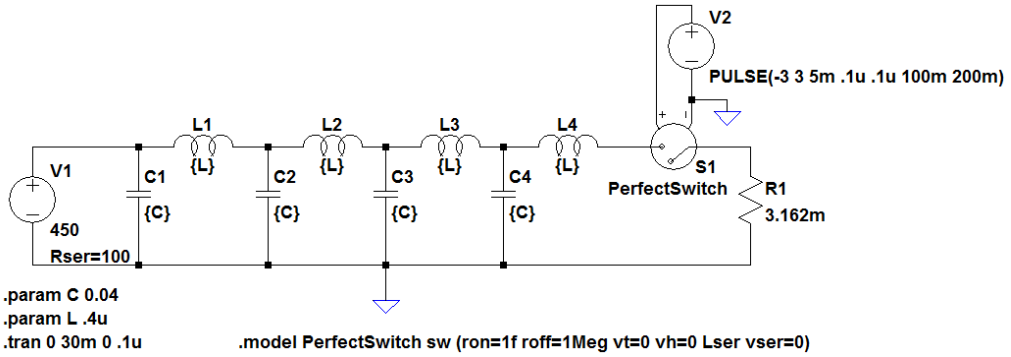


Figure 1.1: Rayleigh Pulse Forming Network. Cal Poly Pulsed Power Club designed this network to power a rail gun. All of the capacitors have a value of 40 mF and all of the inductors have a value of 0.4 μH, with a 3.162 mΩ load resistance. [2][3]

The 450 V source voltage has a 100 Ω series resistance and charges all of the capacitors initially. When the switch closes, all of the capacitors release their charge through the load resistance $R_1$. Each capacitor's charge arrives at the load at different times due to delays provided by the inductors, creating a pulse-like waveform, as shown in Figure 1.2.

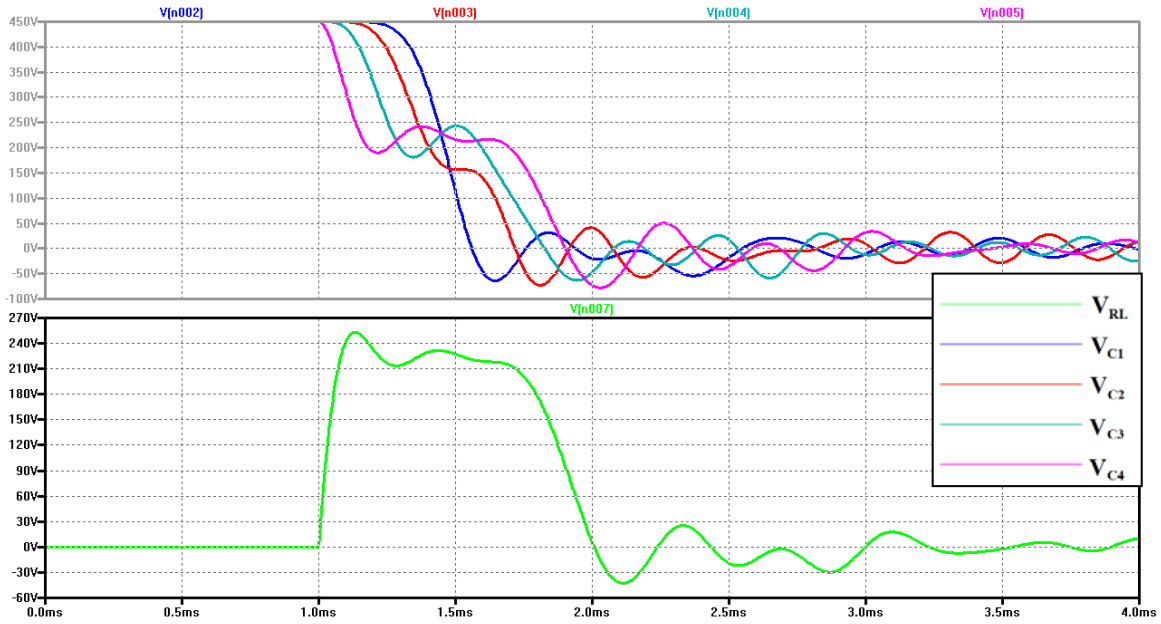


Figure 1.2: Simulations of Pulse Forming Network in Figure 1.1. The switch closes at 1ms and the capacitors release their built up charge. Each capacitors charge arrives at the load at different times, resulting in a pulse like waveform across the load. Top – Voltages across capacitors C1 (blue), C2 (red), C3 (turquoise), and C4 (pink). Bottom – Voltage across load resistor R1 (green).

The club did not possess an accurate means to measure these high voltages across the capacitors and load and could only measure one node at a time. They attempted a simple resistive divider but did not receive accurate results, most likely due to parasitic capacitances. During testing, the PFN failed to produce a "clean" pulse. The club theorized the PFN experienced reflections due to mismatched load impedance, creating voltage dips in the generated pulse. Without accurate measurements to characterize the PFN's waveforms, they could not completely verify the theory and determine component values for optimum performance.

All of the capacitor voltages start at the source voltage of 450 V and drop to as low as about -75 V. The output pulse has a rise time of 75 μs, a rising edge that increases

at a rate of 3403 kV/s, and duration of about 1ms. This thesis aims to provide a way to characterize the PFN by safely measuring these fast changing, high voltage nodes.

## 1.3 System Block Diagram

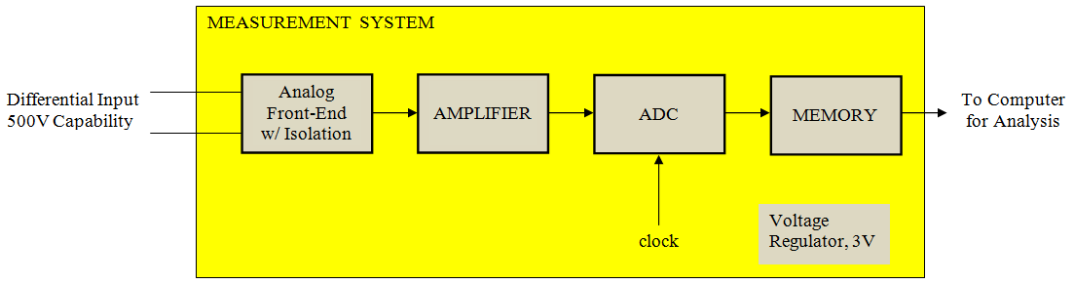


Figure 1.3: Measurement System Block Diagram. The analog front-end measures a 500 V differential input and provides isolation. The signal passes through an amplifier which amplifies the signal to the input voltage range of the ADC. The ADC samples the signal and stores the data to onboard memory for output to user and analysis.

Figure 1.3 shows the block diagram of the implemented system. The system senses a 500 V differential input at the analog front end where isolation of the signal occurs. The amplifier converts the signal produced from the front end to the full scale range of the analog-to-digital converter (ADC). The ADC samples the signal and stores data into onboard memory where it can outputted to the user for analysis.

This thesis implements two analog front-end designs during the design process. Design #1 explains the initial design, however this design needed modification for final design due to inaccurate results. This thesis describes the function of each component, specifications taken into account in choosing each specific component, theoretical calculations, simulations, and characterizations.

## 1.4 Requirements and Specifications

The system voltage characteristics of the simulated PFN above served as a basis for the requirements of the measurement system. This thesis designs a system that can

operate under harsh conditions and accurately sample a pulse with voltages ranging from -500 V to 500 V. The analog front end should provide isolation, 1 kV+ voltage insulation for proper operation under the high voltage environment, and have a 1 MHz system bandwidth. The analog front-end allows “hardware programming” of the maximum sense voltage, accomplished by changing the value of a few resistors. Altering the maximum sense voltage based on specific applications optimizes the resolution of the measurement system.

A 3.0 V source must power all active components. Analog, digital, and mixed mode ICs commonly use a 3.0 V supply voltage. With a 3.0 V supply voltage, two 1.5 V batteries (AA, AAA. C, or D batteries) can power the measurement system.

The system samples the signal with a 12 bit ADC, giving a resolution of 0.122 V at a 500 V maximum voltage. To satisfy the Nyquist rate, the sampling rate must achieve at least 2 MSPS in order to sample a pulse containing frequencies up to 1 MHz. This would result in 150 samples for the rising edge of the simulated PFN pulse, a sufficient amount of samples to characterize a pulse. The user can program the ADC to different sampling rates and specify the number of probes used to change the sampling rate. Measuring pulses with sharper edges and higher frequencies require higher sampling rates. Measuring pulses of longer duration require lower sampling rates, as the limited memory space only allows storage of a maximum number readings.

The ADC should output data to onboard memory, as opposed to instantly transmitting each reading directly to the computer. This avoids data corruption during transmission due to the harsh EM environment. The memory must also have enough space to store enough readings for a 1ms pulse sampled at 2 MSPS.

A single channel measurement system would need a test fire for each measurement at different nodes. The Power Pulse Club's rail gun performed differently from one test fire to another due to the physical toll from each test fire. A measurement system needing a test fire for each measured node makes the combined measurements less informative and accurate. The measurement system designed in this thesis implements multiple probes to simultaneously sample multiple nodes of the measured network if desired, such as the different capacitor voltages of the PFN. The design minimizes the cost of the measurement system to less than $100 per channel.

REQUIREMENTS

1. Measure high voltages, both positive and negative
2. High system bandwidth for high frequency signals
3. Able to operate under harsh electromagnetic environments
4. Provide isolation between the high voltage system and the measurement system
5. Multiple probes for simultaneous node measurements
6. Full system powered by single low voltage source
7. High resolution for high voltages
8. "Hardware programming" for adjustable resolution
9. Adjustable sampling rate
10. Onboard memory
11. Sufficiently large memory
12. Minimize cost

SPECIFICATIONS:

1. Measure voltages within the range of -500 V and +500 V
2. System bandwidth of 1 MHz
3. 1 kV+ voltage insulation front-end
4. Implement two probes
5. Full system powered by single 3.0 V source
6. Adjustable resolution with minimum resolution of 0.15 V when measuring 500 V
7. Adjustable sampling rate up to 2 MSPS
8. Onboard memory with enough space for sampling a 1 ms pulse at a sampling rate of 2 MSPS
9. Less than $100 per channel

## 1.5 Existing Technologies

The existing technologies commercially available do not meet all of the desired requirements. These technologies have inadequate bandwidth and tend to be expensive.

### 1.5.1 Keithley 2657A High Power Source Measurement Unit [4]


Figure 1.4: Keithley 2657A High Power Source Measurement Unit

The Keithley 2657A can measure pulses up to 3000 V at a resolution of 80 mV. For a 500 V pulse, it can measure with a resolution of 10 mV. This instrument can accomplish 2200 readings per second via GPIB interface. It also has burst mode which

uses a high speed ADC that samples at 1MSPS, a bandwidth of 500 kHz, and has 16MB of memory. This instrument performs much better than the Keithley 2410. However, it costs more than $18,000 and still does not have a high enough sampling rate to meet our requirements.

### 1.5.2 Agilent InfiniiVision 2000 X-Series [5]

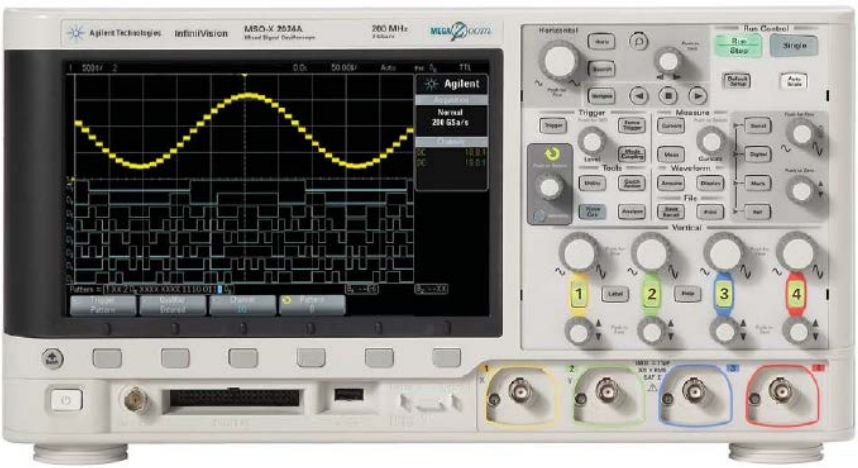


Figure 1.5: Agilent InfiniiVision 2000 X-Series Oscilloscope

The InfiniiVision2000 X-Series Oscilloscopes can measure pulses up to 400 V at a resolution of 1.953 V and can store 100,000 readings. The oscilloscope has system bandwidth of 70 MHz and costs about $1250 for a 2 channel system. At $625 per channel, this is the cheapest test bench oscilloscope Agilent offers. The system has plenty of bandwidth, but fails to reach the required voltage of 500 V and also has poor resolution.

### 1.5.3 Agilent U1610A Handheld Digital Oscilloscope [6]

Figure 1.6: Agilent U1610A Handheld Digital Oscilloscope

This oscilloscope measures peak voltages of 600 V, but only at a 2.34 V resolution. It can store 2,000,000 readings and has a system bandwidth of 100 MHz. At a cost of $1400, this instrument provides the closest performance to the requirements. However, the poor resolution of the oscilloscope hinders the user's ability to precisely measure waveforms.

### 1.5.4 Existing Technologies Drawbacks

Existing technologies not only cost thousands of dollars, but also fall short in fulfilling at least one of the requirements. The Keithley 2657A only has a bandwidth of 500 kHz, the Agilent InfiniiVision 2000 X-Series can only measure up to 400 V with poor resolution, and the Agilent U1610A only has a resolution of 2.34 V. Using high voltage probes can increase the maximum voltage of oscilloscopes such as Agilent InfiniiVision 2000 X-Series oscilloscopes, but the resolution worsens. This thesis aims to meet all of the requirements at a much lower cost.

# 2. BACKGROUND

An overview of pulse generators, existing high voltage measurement methods, and optocoupler technology assists in understanding the development process of this thesis.

## 2.1 Pulse Generators

Applications for pulse generators include ultrasound, sterilization, and radar. Some pulse generators use MOSFET switching connected to high voltage rails and some use stored energy in inductors and capacitors to create high voltage pulses. This thesis designs, constructs, and uses a high voltage pulse generator to test the pulse measurement system. The following examples explain different pulse generator designs considered in the design of the pulse generator used for testing in this thesis.

### 2.1.1 Complementary High Voltage Switched Current Source Integrated Circuit [7]

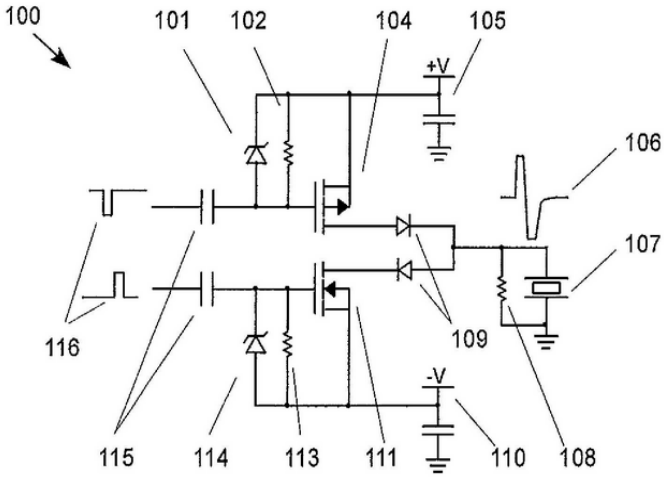


Figure 2.1: Complementary High Voltage Switched Current Source Integrated Circuit. The circuit takes in two inputs, negative pulses and positive pulses. The two inputs offset their pulses as to activate different parts of the circuit at different times. The negative pulse input creates a positive high voltage pulse at the output and the positive pulse input creates a negative high voltage pulse at the output.

The high voltage pulse generator in Figure 2.1 relates to an ultra sound scanning image system. The design has a digital logic level control interface circuit coupled to a complementary current source pair and to the positive and negative voltage rails. The top control waveform 116 drives a negative pulse to the PMOS 104. The PMOS conducts and drives the output to the positive high voltage rail for the duration of the control waveform. When the bottom control waveform of 116 drives a positive pulse to the NMOS 111, the NMOS conducts. This drives the output to the negative high voltage rail for the duration of the control waveform. Zener diodes 101 and 114 protect the MOSFET gate to source voltages from overvoltage. Diodes 109 provide reverse voltage blocking and ultrasound receiver isolation. Resistors 102 and 113 DC bias the MOSFETS and

resistor 108 discharges the capacitance of the transducer 107, back to zero voltage. The overall circuit provides a square pulse 106 with amplitude of voltage rails V.

### 2.1.2 High Voltage Pulse Generating Circuit [8]

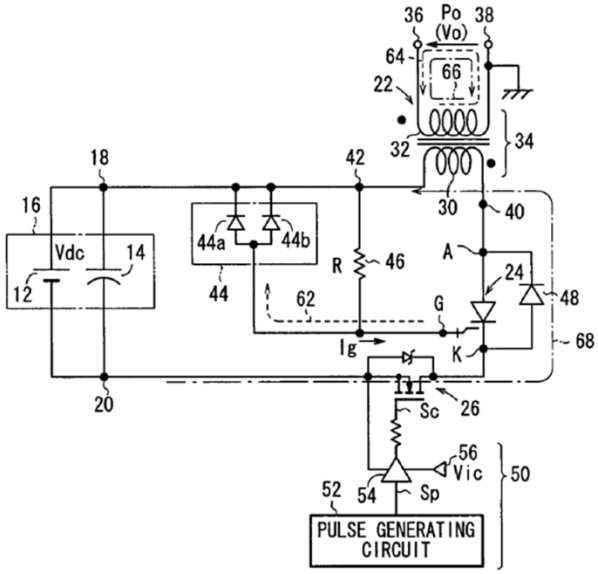


Figure 2.2: High Voltage Pulse Generating Circuit. A pulse generating circuit, 52, creates a pulse that first causes the current to travel in a clockwise direction, and then cause the current to travel in a counterclockwise direction. The transformer, 34, uses this current to create a high voltage pulse at the output, Vo.

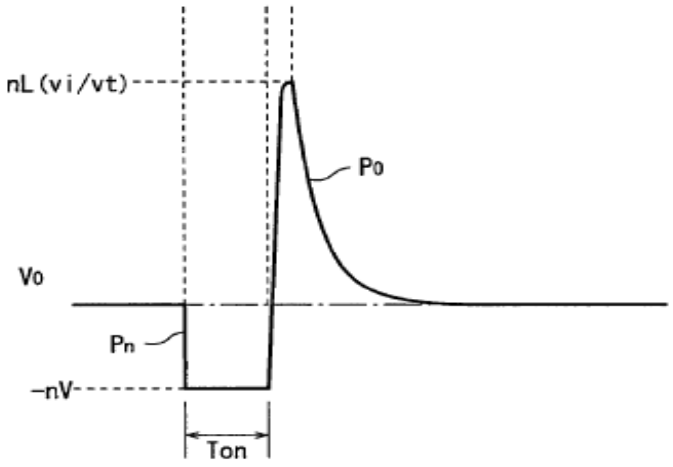


Figure 2.3: High Voltage Pulse Generating Circuit Output Waveform. A clockwise current creates the negative pulse Pn. The switch to a counterclockwise current creates the positive pulse Po.

The high voltage pulse generator in Figure 2.3 develops plasma used in technologies for deodorization, sterilization, and toxic gas decomposition. The low voltage input pulse generating circuit 10 turns on the NMOS 26. This creates a current Ig starting at Vdc and flowing through resistor 46, through the gate and cathode of the semiconductor switch 24, and returns back to $V_{dc}$ through the NMOS. The current flowing through the gate and cathode causes the anode-to-cathode voltage $V_{AK}$ to drop and turns on semiconductor 24. The transformer 34 assumes the voltage $V_{dc}$ and transfers this voltage to output $V_o$. The output equals –nV and has a duration of $T_{on}$, seen in Figure 2.3. When the input pulse drops to zero, the NMOS turns off and the current from the cathode K goes to zero. The primary winding 30 then generates a reverse induced voltage based on the remaining electromagnetic energy. The new current path 62 flows through the primary winding to the anode A, to the gate G, and through diodes 44. This causes the output voltage Vo to rise. In addition, diode 48 allows the Vdc capacitance 14 to discharge through the inductor 30. Figure 2.3 shows the resulting waveform Po after the NMOS turns off.

### 2.1.3 Pulse Generator Summary

These high voltage pulse generators use a low voltage pulse generator to toggle MOSFETs, along with some resistors, capacitors, and diodes. The high voltage pulse generator used in this thesis also implements a low voltage pulse generator, MOSFETs, resistors, and capacitors. The implemented generator also requires a high rail that dictates the peak voltage of the generated pulses. This limits the testing performed on the

measurement network, as the laboratory's equipment only provides a maximum of 125 V. Section 7 discusses more on the design of the pulse generated used for testing.

## 2.2 High Voltage Measurement Methods

Current methods for measuring high voltage tend to be bulky and/or unsafe. Bulky equipment limits portability. Equipment that does not provide complete safety precautions can cause harm to users and require special care for operation. The following explains various high voltage measurement methods and their drawbacks.

### 2.2.1 Electrostatic Voltmeter [9]

Electrostatic voltmeters serve as a direct way to measure high voltages. Electrostatic voltmeters utilize two parallel conducting plates to sense a potential voltage difference. The voltage on one plate forms this difference and creates a force measured by meter. Figure 2.4 shows an Abraham electrostatic voltmeter, one of the most commonly used instruments for high voltage testing.

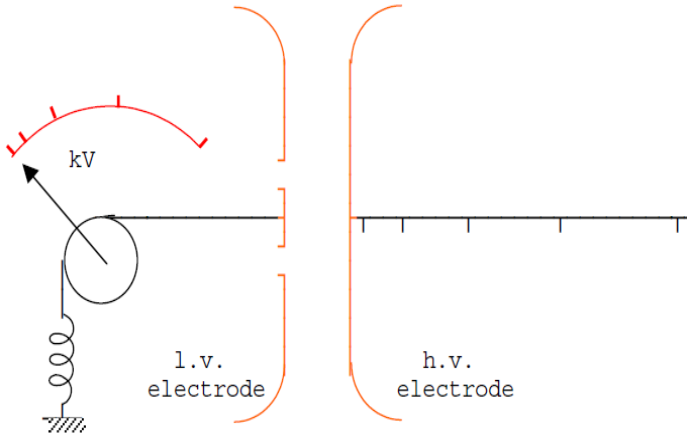


Figure 2.4: Abraham Electrostatic Voltmeter. This voltmeter uses to mushroom shaped hollow metal discs and a meter. The right disc senses the high voltage and the center portion of the left disc moves in relationship to the force produced by the applied voltage. Adjusting the right disc at pre-marked distances sets the voltage range of the instrument.

The two plates have a cross section area A, spacing x, and capacitance C. A voltage creates a potential difference V across the two plates. Equation 2.1 shows resulting energy stored W.

$$W = \frac{1}{2}CV^2 \tag{2.1}$$

Equation 2.2 shows the change in work and also relates it to force F.

$$dW = \frac{1}{2}V^2 dC = Fdx \tag{2.2}$$

Solving for F gives:

$$F = \frac{1}{2}V^2 \frac{dC}{dx}\ [Newtons] \tag{2.3}$$

For uniform field capacitance C:

$$C = \frac{A\varepsilon}{x} \tag{2.4}$$

Equation 2.5 gives the change in capacitance with respect to x.

$$\frac{dC}{dx} = -\frac{A\varepsilon}{x^2} \tag{2.5}$$

Substituting Equation 2.5 into Equation 2.3:

$$F = -\frac{1}{2}A\varepsilon\frac{V^2}{x^2}[Newtons] \tag{2.6}$$

A meter senses the force and thus the voltage and can measure up to about 200 kV. Electrostatic voltmeters give accurate measurements for high voltage tests. However, they not only require a large amount of space but they present a safety hazard.

Electrostatic voltmeters use an exposed charge between parallel plates to measure the voltage and do not provide complete isolation to the user. This method introduces a dangerous safety issue if used by the CPPP club and therefore is not used in the design in this thesis.

### 2.2.2 Transformers [9]

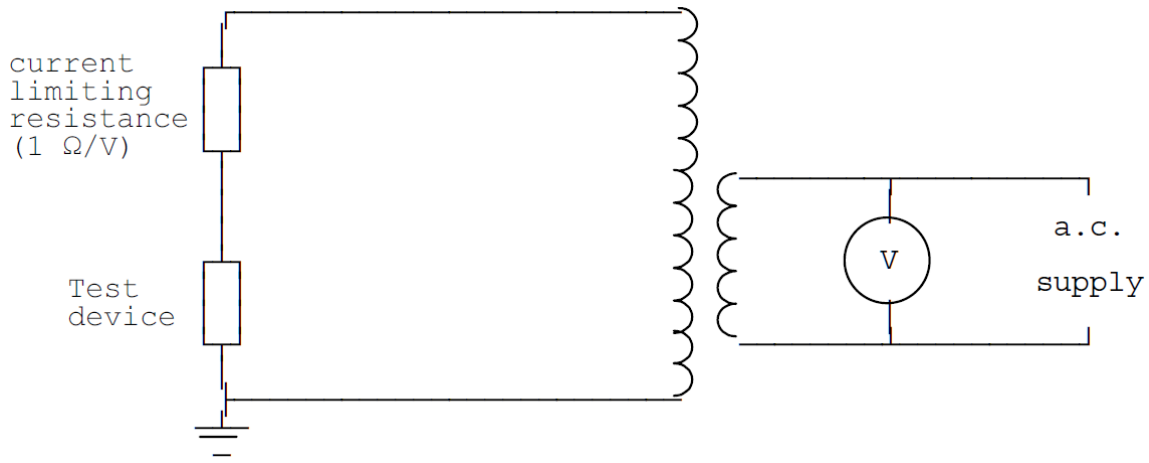


Figure 2.5: Transformer. This setup limits the current using a resistor and then down converts the high voltage to a voltage measureable by a voltmeter. The resulting voltage can be used for as an AC voltage supply.

Transformers provide an indirect method to measuring high voltages by stepping down the high voltage. Transformers use two inductive coils to transfer energy. In this case, a transformer down converts a high voltage test device. A voltmeter on the low-side measures the voltage and in this case, the transformer supplies an AC voltage. Equation 2.7 relates the primary and secondary windings of the transformer, where N equals the number of turns in each winding.

$$\frac{V_P}{V_S} = \frac{N_P}{N_S} \tag{2.7}$$

Transformers do provide isolation unlike an electrostatic voltmeter. However, they require a large amount of space and do not produce precise results. Due to their lack of their mobility and non-precise results, a transformer method is not used.

### 2.2.3 Capacitive Divider

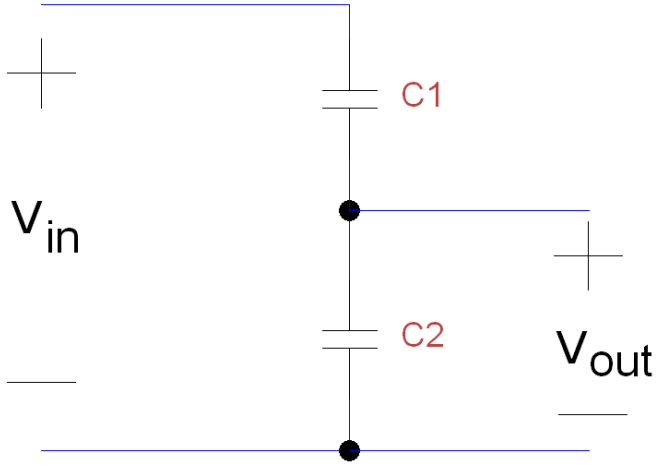


Figure 2.6: Capacitive Divider. The size of the capacitors determine the relationship between the input and output voltages.

A capacitive divider offers a low cost design for high voltage measuring. The design works similar to a resistive divider in that the output and input voltage is related by Equation 2.8.

$$V_{out} = \frac{C_1}{C_1 + C_2} V_{in} \tag{2.8}$$

An oscilloscope can measure the output voltage for continuous signals or an analog-to-digital converter can be used to measure a single pulse. With limited values of capacitors available, finding two capacitors with the correct ratio to down convert the high voltage to an appropriate lower voltage for an oscilloscope or ADC to read proves difficult, especially for the narrow range an ADC operates at. The capacitive divider also lacks isolation between the high voltage side and control side, a major safety issue.

Spontaneous voltage spikes can damage the measurement device used to measure to the output voltage and can also injure the user operating the measurement device. Additionally, the PFN is a capacitor and inductor based network and the use of capacitors for measurements can alter the PFN's performance and give bad results.

### 2.2.4 High Voltage Measurement Summary

These high voltage measurement methods either do not provide isolation for safety and/or require too much space, limiting its mobility. This thesis aims to rectify both of these issues using optocoupler technology. The implemented design uses optocoupler technology to measure high voltages. In addition, optocouplers provide isolation and compactness at a low cost.

## 2.3 Optocoupler Technology

The key component of the measurement system designed and constructed in this thesis is the optocoupler. Optocouplers provide a compact, low cost method to implement isolation, as opposed to unsafe, bulky, and costly alternatives. In situations when two subsystems operate at very different voltage ranges, implementing isolation protects the low voltage subsystem from overvoltage damage [10]. Optocouplers provide this isolation while minimizing loss of signal integrity. They achieve excellent noise immunity, characterized by high common mode transient immunity and power supply rejection specifications, allowing these devices to operate in noisy industrial environments [11]. Applications include sensing circuits, power supply feedback, and motor controls.

### 2.3.1 Applications

Many high voltage applications use optocouplers such as AC/DC converters, gate driving, and voltage and current sensing. They provide the necessary isolation while maintaining system performance.

#### 2.3.1.1 AC/DC Converter [12]

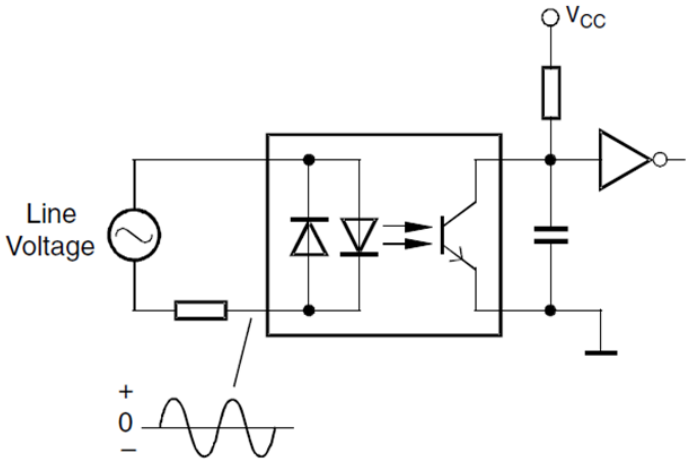


Figure 2.7: AC/DC Converter Design with Optocoupler [12]. The line voltage inputs an AC signal into the optocoupler. The optocoupler isolates and amplifies the signal. The resulting signal passes through a low pass filter and converted into a DC signal.

Numerous everyday electronics and appliances use AC/DC converters. Figure 2.7 shows a simple AC/DC converter that features optical isolation. The AC line voltage drives the LED – resistor network and produces a linearly related current across the collector and emitter of the phototransistor. The collector current passes through a low pass filter and converted into a DC voltage. Though commercial AC/DC converters are a little more complex than this simple example, the theory applies to many electronics that convert high voltage from the power grid to a usable DC voltage including vacuums, washing machines, and telephones. Design #1 in Section 3 uses this concept to sense the AC characteristics of the high voltage signals.

### 2.3.1.2 Isolated Integrated Gate Driver for IGBT/MOSFET [13]

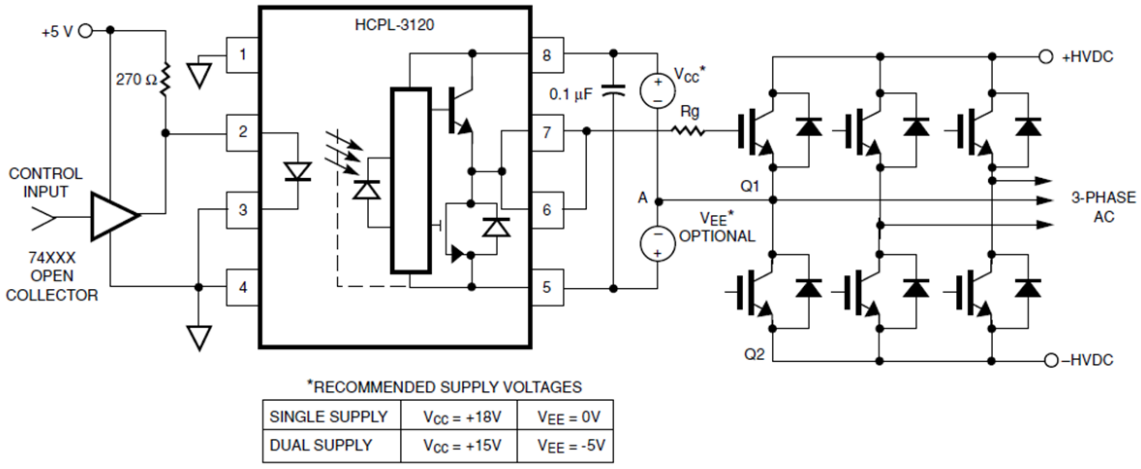


Figure 2.8: Isolated Integrated Gate Driver for IGBT/MOSFET Schematic [13]. The optocoupler provides isolation between the low voltage control signals and the high voltage 3-phase signal.

The gate driver circuit in Figure 2.8 provides isolation between the control and high voltage power systems. This uses a bit more complex optocoupler, HCPL-3120, but the idea still functions in the same general way. The control system operates from a low voltage source, 5 V in this example, and isolation must protect from the high voltage rails that can cause harmful overvoltage damage to the control systems. The example regulates a high voltage three phase AC signal for power grid applications. The measurement system must also have isolation between a low power and high power system in which optocoupler technology can provide.

### 2.3.1.3 Inverter Design Using Gate Drive and Current Sense Optocouplers [13]

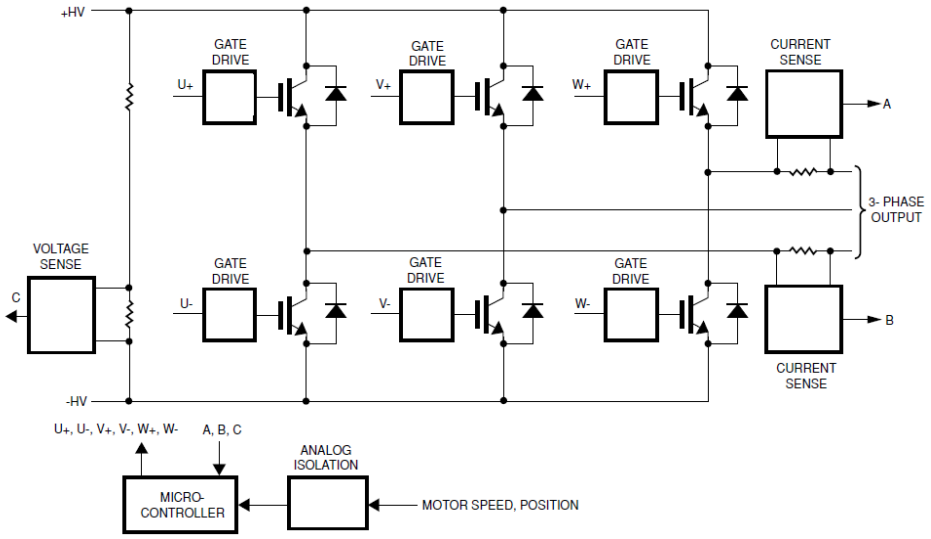


Figure 2.9: Isolation Circuits for Power Control - System Overview [13]. The microcontroller measures high voltage signals created by a vehicles motor speed and position. The microcontroller also controls the three phase variable voltage and variable frequency power source to the vehicle. Optocouplers provide isolation for both sensing and gate driving.

Figure 2.9 shows a typical motor drive and power control system. The control's microcontroller and the high voltage devices require isolation between each other. Many motor drive and power control systems use pulse width modulation switching of power devices to generate three phase variable voltage and variable frequency power sources. Optocouplers provide analog isolation for motor current sensing, voltage sensing, speed measurements, and position measurement and also used to drive gates based on these input measurements. The measurement system also measures high voltage signals using optocoupler technology.

#### 2.3.1.4 Applications Summary

Applications use optocouplers for AC signals, measuring, and isolation, all of which apply to measuring high voltage signals. The measurement system needs to measure a continuously changing, high voltage signal ranging from -500 V to +500 V. In addition, the system provides isolation between the high voltage system and the measurement system for user safety. Optocouplers provide the ideal functions for measuring high voltages and are used in this design.

### 2.3.2 Analog Configurations

In a basic schematic of an optocoupler, an LED drives a photodetector. A current drives the LED causing it to emit light. The photodetector detects this light and produces a linearly related current. Specific application designs implement optocouplers based on certain performance parameters such as bandwidth, linearity, and current transfer ratio (CTR).

Optocouplers use two common photodetectors (Figure 2.10), a photodiode and phototransistor, each with their advantages and disadvantages. Photodiodes tend to have a greater bandwidth and linearity whereas phototransistors have a larger current transfer ratio (CTR)

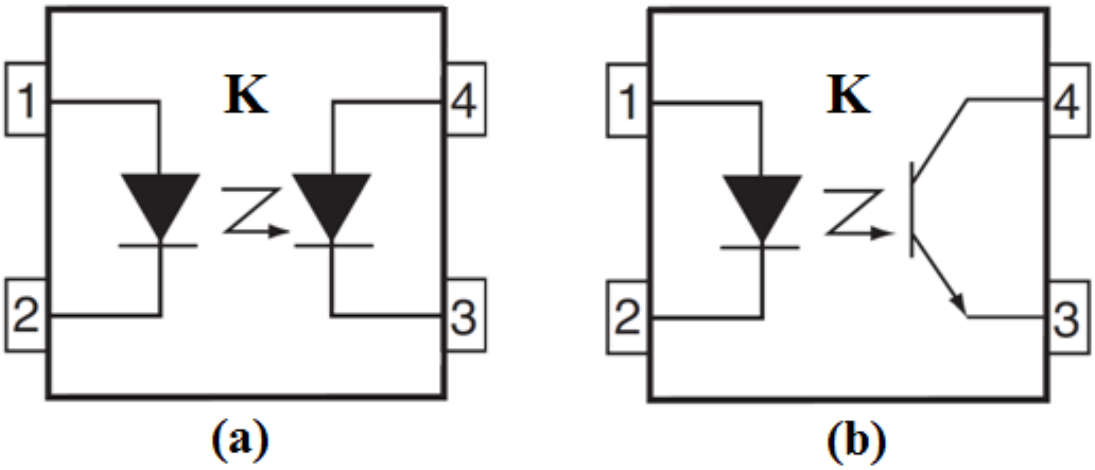


Figure 2.10: Optocoupler Configurations. A current drives the LED on the left and the photodetector on the right produces a current linearly related by K. (a) Photodiode photodetector configuration. (b) Phototransistor photodetector configuration.

Photodiode bandwidth can reach 30 MHz but the CTR reduces considerably to fractions of a percent. On the other hand, the phototransistor could have CTR >100% but the bandwidth reduces to the kHz range [10]. Phototransistors contain higher input capacitances, causing a longer charge time to activate the photodetector and thus lower bandwidth. Photodiodes have much less inherent capacitance and can activate much faster, but they do not have the capability of amplifying the signal anywhere close to the magnitude a transistor has the ability to do.

Larger CTR also comes at the cost of linearity, especially near the lower and higher ends of the current range [14]. Figure 2.11 illustrates this fact by graphing the output current produced by the photodiode and phototransistor with respect to the illuminating light incident upon them.

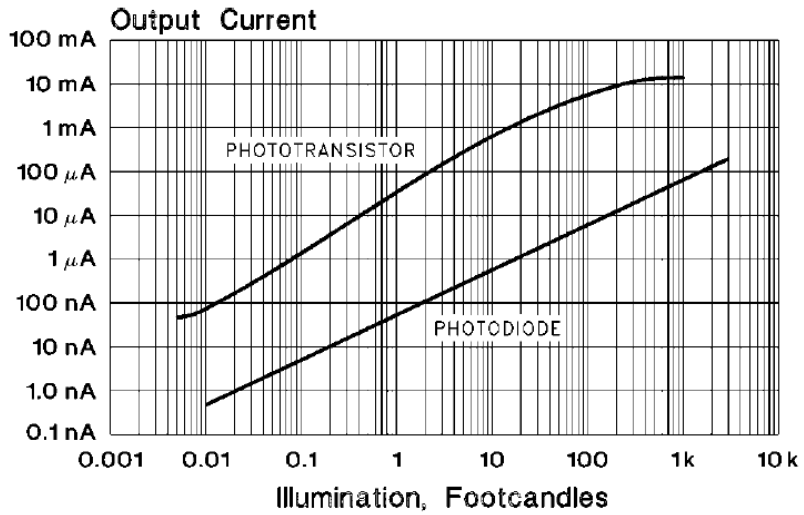


Figure 2.11: Output Current of Photodiodes and Phototransistors with Respect to Incident Illumination [14]. The graph shows the tradeoff between CTR and linearity. Photodiodes have much better linearity throughout the input range, but experiences about 100x less CTR than the phototransistor.

The photodiode has about 100x less CTR than the phototransistor but experiences much better linearity throughout the incident illumination range. The photodiode also has less susceptibility to temperature, another advantage they have over phototransistors.

Temperature alters current gain and transistor leakage current in transistors. As temperature increases, transistor current gain (β) and leakage current also increase. In addition, $V_{BE}$ decreases about 7.5 mV per degree Celsius increase and the reverse saturation current ($I_{CO}$) doubles in value for every 10 degrees Celsius increase [15]. Figure 2.12 shows how an $I_{CO}$ and $V_{BE}$ change as temperature increases.

| Variation of Silicon Transistor Parameters with Temperature | | | |
|---|---|---|---|
| $T\ (°C)$ | $I_{CO}\ (nA)$ | $\beta$ | $V_{BE}(V)$ |
| −65 | $0.2 \times 10^{-3}$ | 20 | 0.85 |
| 25 | 0.1 | 50 | 0.65 |
| 100 | 20 | 80 | 0.48 |
| 175 | $3.3 \times 10^{3}$ | 120 | 0.3 |

Figure 2.12: Effect of Temperature on a Transistor. As temperature increases, the reverse saturation current ($I_{CO}$) and current gain (β) increases and the base-emitter voltage ($V_{BE}$) decreases. [15]

$I_{CO}$ equals 0.1 nA at room temperature and equals 20 nA at 100ºC, 200 times larger. For the same temperature variation, β increases from 50 to 80 and $V_{BE}$ decreases for 0.65V to 0.48 V. All of these can significantly change the output current of an optocoupler. A phototransistor based optocoupler used in the measurement system makes the whole system susceptible to temperature. Not only does temperature affect photodetectors, but they also degrade the optocoupler's LEDs.

### 2.3.3 LED Type [13]

LEDs tend to degrade due to temperature of the environment and operating current, with some LEDs degrading more than others. Over time, LEDs produce less light output and thus decrease the current transfer ratio of an optocoupler. Figure 2.13 shows light output degradation over time for two different types of LEDs commonly used in optocouplers, Gallium Arsenide Phosphide and Aluminum Gallium Arsenide LEDs. The solid line graphs the LEDs' mean light output over time and the dotted line graphs

the LEDs' worst case light output over time, defined as three standard deviations less than the mean.

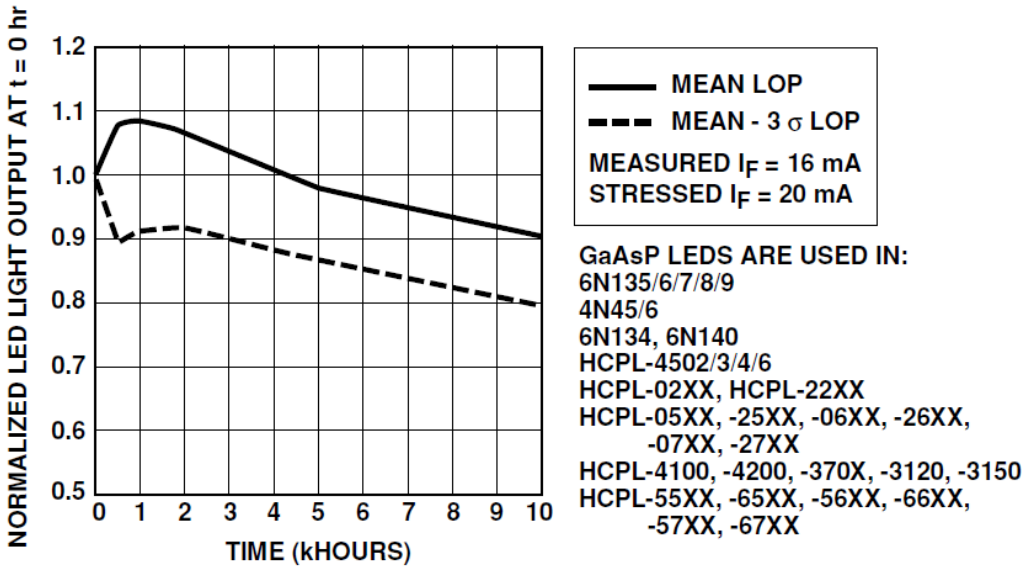


Figure 2.13a: Normalized LED Light Output vs. Time for GaAsP LED [13]. A GaAsP LED emits about 10% less light after 10KHours on average and as much as about 20% less light in a worst case.

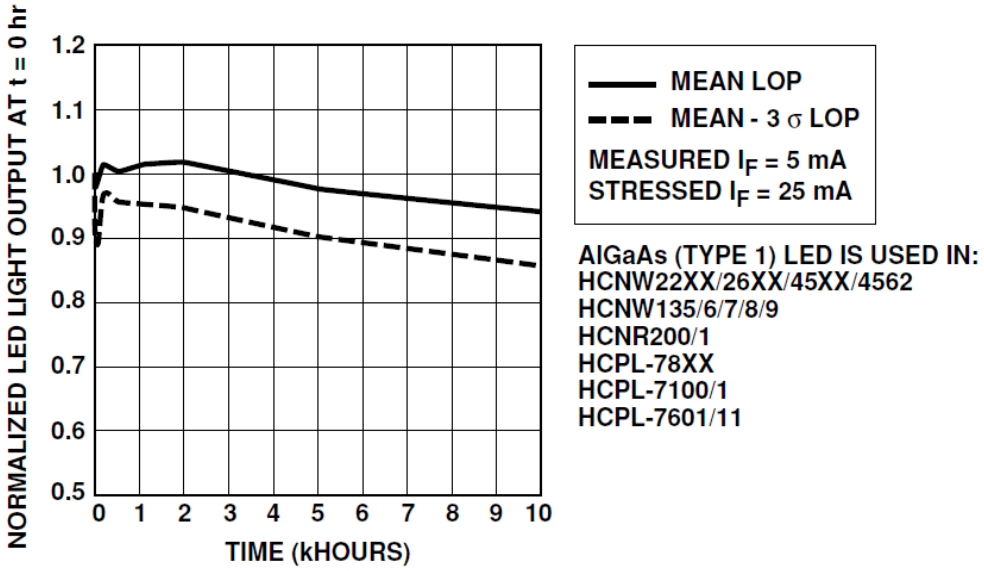


Figure 2.13b: Normalized LED Light Output vs. Time for AlGaAs LED [13]. A GaAsP LED emits about 6% less light after 10KHours on average and as much as about 14% less light in a worst case. A AlGaAs LED light output degrades much less than a GaAsP LED, making them more reliable throughout time.

The GaAsP LED light output can increase by about 8% on average and decrease by as much as about 10% after only 500 hours of use. Whether the LED light output increases or decreases, the change alters the overall gain of the measurement system, resulting in inaccurate readings. The AlGaAs LED maintains a more consistent light output over time and has a smaller standard deviation from its mean. Its light output stays close to the original light output for a longer period of time and does not degrade as much. With LED degradation in mind, recalibration should occur every once in a while.

Despite light output degradation over time, optocouplers maintain linearity fairly well. Figure 2.14 shows the LED light output versus LED forward current at 0 khours and 10 khours of operation.

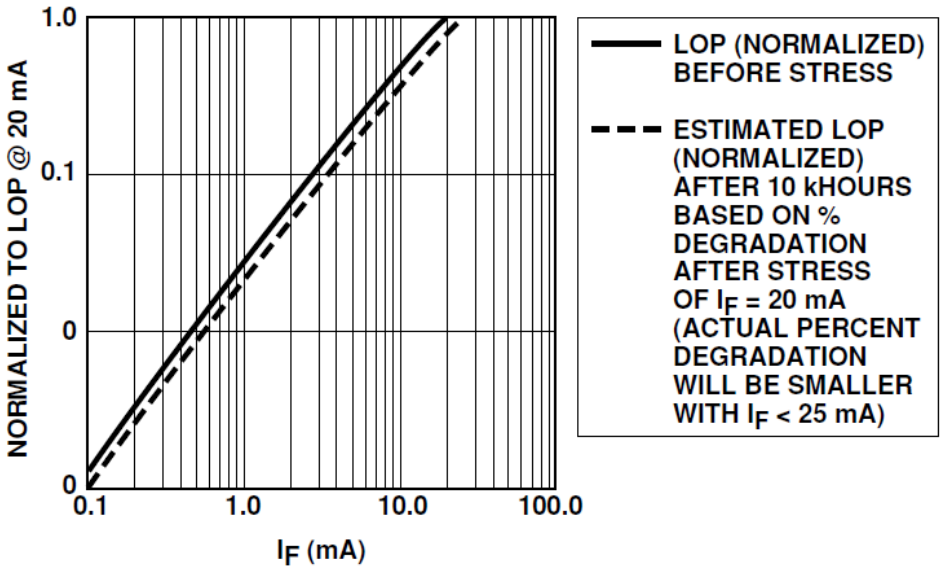


Figure 2.14a: GaAsP LED Light-Output vs. $I_F$ (logarithmic scale) after 0 khours and 10 khours of Continuous Operation [13]. The LED maintains very good linearity and loses little CTR after 10 kHours.

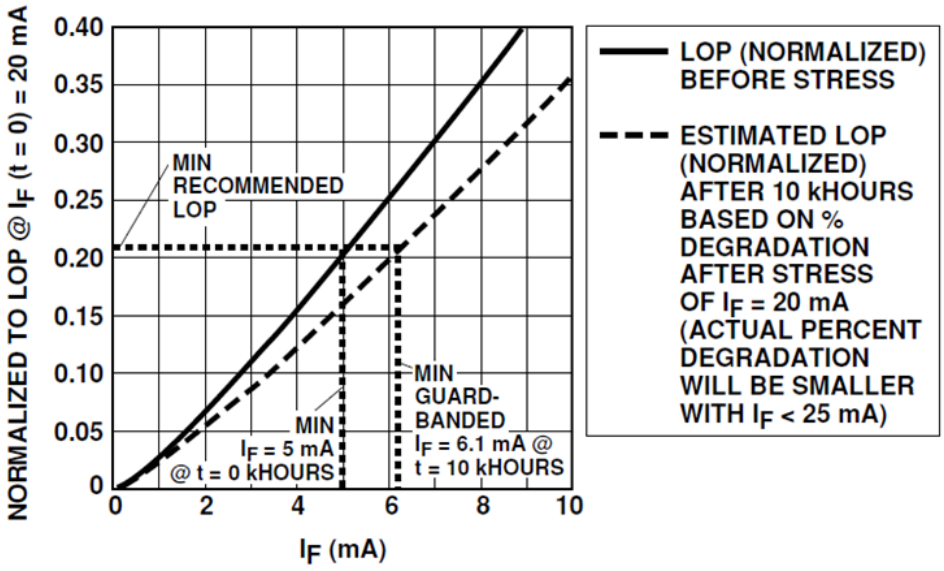


Figure 2.14b: GaAsP LED Light-Output vs. $I_F$ (linear scale) after 0khours and 10 khours of Continuous Operation [13]. The LED maintains very good linearity and loses little CTR after 10 khours.

Again, the LED produces less output after 1 khour of operation, but still outputs a linear light output with respect to the forward current. This keeps the data processing stage of the measurement system simple by still only needing to multiply the data by a scale factor. The figure also recommends a guardband, a minimum value for the forward current to ensure linearity. Forward current below this guardband still shows decent but less linearity, causing lower voltage to experience some error. Figure 2.14 shows data for GaAsP LEDs, however AlGaAs LEDs have better linearity than GaAsP LEDs and display less degradation over time than GaAsP [13].

### 2.3.4 Maximum Working Insulation Voltage

Insulation is defined as the ability to protect surrounding circuitry, as well as itself, against physical damage resulting from different voltage potentials [13]. The maximum working insulation voltage determines at what voltage potentials the

optocoupler can maintain functionality including prevention against signal distortion. The optocoupler needs to function properly when operated in high voltage environments.

### 2.3.5 Optimum Optocoupler

The optimum optocoupler for a high voltage measurement system application uses a photodiode, an Aluminum Gallium Arsenide LED, and has a high maximum working insulation voltage. A photodiode ensures the highest linearity and thus highest precision when measuring high voltages. An AlGaP LED protects the optocoupler from degradation over time. Lastly, a high insulation voltage ensures proper functionality under the harsh electromagnetic environment the optocoupler will need to operate in. The HCNR200 optocoupler contains all of these features, making it the ideal optocoupler for the measurement system design.

## 3. Design #1: Analog Front-End Using Pair of Optocouplers

The front-end depicted in Figure 3.1 comprises of two optocouplers in series with resistors, a differential, TIA operated from a single 3 V supply, and an ADC. The analog front end provides optical isolation to preserve both the measured and measurement system. During this process, the measured signal splits into its positive and negative components and converted into an isolated current. The LEDs' anti-parallel configuration protects each other from overvoltage, similar to the AC/DC converter in Figure 2.7. The TIA then converts the isolated current to a differential voltage range the ADC can read.

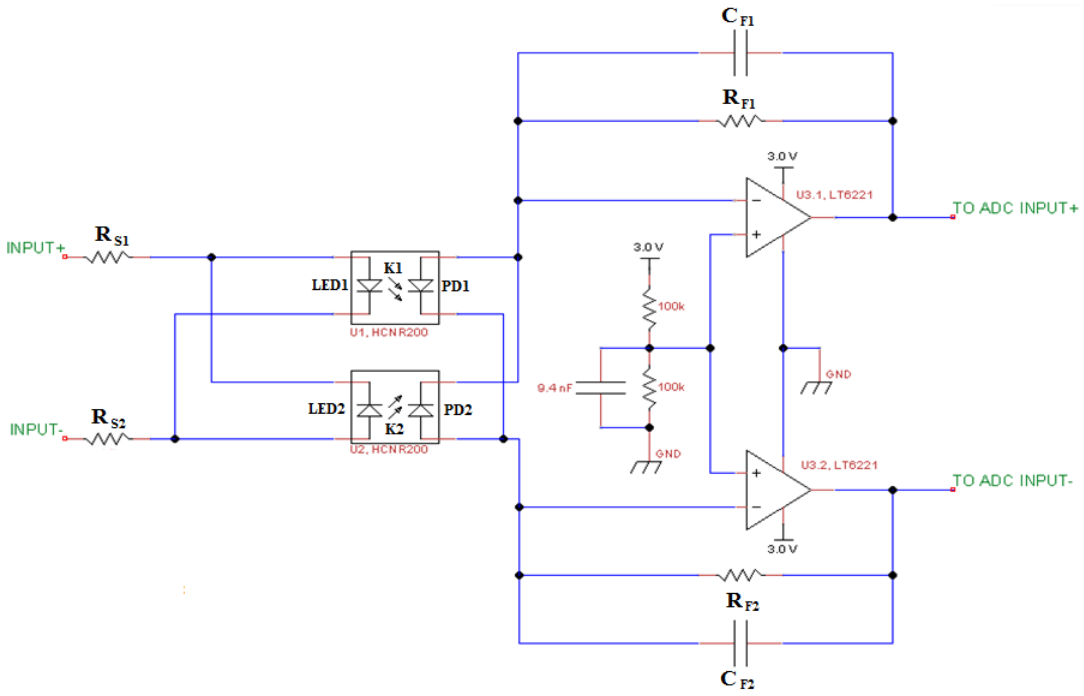


Figure 3.1: Design #1 Schematic. The design consists of two front-end resistors, two optocouplers, and a differential transimpedance amplifier. An ADC samples the TIA's output and stores the data for the user to read and analyze.

## 3.1 HCNR200 Optocoupler

The HCNR200 optocoupler is a high linearity optocoupler that provides stability, linearity, and bandwidth at a low cost [13]. It has a maximum working insulation voltage of 1414 V, more than enough to withstand the maximum pulse voltage of 500 V. This optocoupler offers high accuracy with a low nonlinearity of 0.01% and high bandwidth of 1.5 MHz, meeting the 1 MHz bandwidth system requirement. The HCNR200 uses an AlGaAs LED for increased lifespan and linearity and a standalone photodiode to produce an output current resulting in a low CTR of 0.5%. The photodiode has a small 22 pF zero-bias depletion capacitance. As mentioned before, higher CTR optocouplers have lower bandwidth and less linearity because of parasitic capacitances. These effecting parasitic capacitances occur between the LED and photodetector and prove difficult to offer correction. With phototransistor based optocouplers that contain internal circuitry for amplification, the optocoupler's input and output terminals do not see these capacitances. However, the output can see the depletion capacitance of a standalone photodiode and the design can "correct" this capacitance with a transimpedance amplifier.

The HCNR200 provides isolation between the measured network and the measurement system by transferring an input current to a linearly related output current. A current drives an LED causing the LED to emit light. A photodiode, PD, senses the produced photons resulting in a linearly related current. The current transfer ratio, K, gives the relationship between the input and output current as seen in the Equation 3.1:

$$I_{PD} = K \times I_{LED} \tag{3.1}$$

Datasheets specify a maximum current for any optocoupler – in our case 40 mA. Exceeding this limit could damage the LED. From Equation 3.1, the photodiode should produce a current of 200 μA given the maximum input current.

$$I_{PD} = K \times I_{LED} = 0.005 \times 40mA = 200\ \mu A$$

## 3.2 Front-End Resistors

The front end resistors convert the high voltage signal to a current ranging from 0-40 mA, the input current range of the optocouplers. The derivation for the front end resistors follows:

Applying KVL to the front-end:

$$V_{SOURCE} + V_{R1} + V_{LED} + V_{R2} = 0 \tag{3.2}$$

Both front-end resistors have the save value and therefore the same voltage across them:

$$V_R = V_{R1} = V_{R2} \tag{3.3}$$

Substituting Equation 3.3 into Equation 3.2:

$$V_{SOURCE} + 2V_R + V_{LED} = 0 \tag{3.4}$$

Solving for $V_{R:}$

$$V_R = \frac{V_{SOURCE} - V_{LED}}{2} \tag{3.5}$$

Applying Ohm's Law to the resistor:

$$R_S = \frac{V_R}{I_{LED}} \tag{3.6}$$

Substituting Equation 3.5 into Equation 3.6:

$$R_S = \frac{V_{SOURCE} - V_{LED}}{2I_{LED}} \tag{3.7}$$

This gives the theoretical value of the front end resistor. With the LED on-voltage equal to 1.6 V and the maximum input current equal to 40 mA, the front-end resistor equals 105 Ω (for the 10 V sensing case).

$$R_{S,10V} = \frac{10V - 1.6V}{2(40mA)} = 105\,\Omega \tag{3.8}$$

The user can change the value of the front-end resistors based on the maximum sense voltage, $V_{SOURCE}$, in order to maximize the measurement system's resolution.

In addition, the user must determine the maximum power rating to choose appropriate resistors that can handle the power situations they must undergo. Equation 3.9 calculates the power dissipated through the each resistor:

$$Power_R = I_{LED} \times V_R = {I_{LED}}^2 \times R \tag{3.9}$$

$R_1$ and $R_2$ have a power rating of 0.336W for a 10V peak voltage, used in early-stage prototyping only.

$$Power_{R,10V} = (40mA)^2 \times 105\Omega = 0.168\,W$$

Similar calculations for the 500 V case leads to $R_{S,500V}$ = 6230 Ω and $Power_{R,500V}$ = 9.968 W.

## 3.3 Differential, Single Supply Transimpedance Amplifier

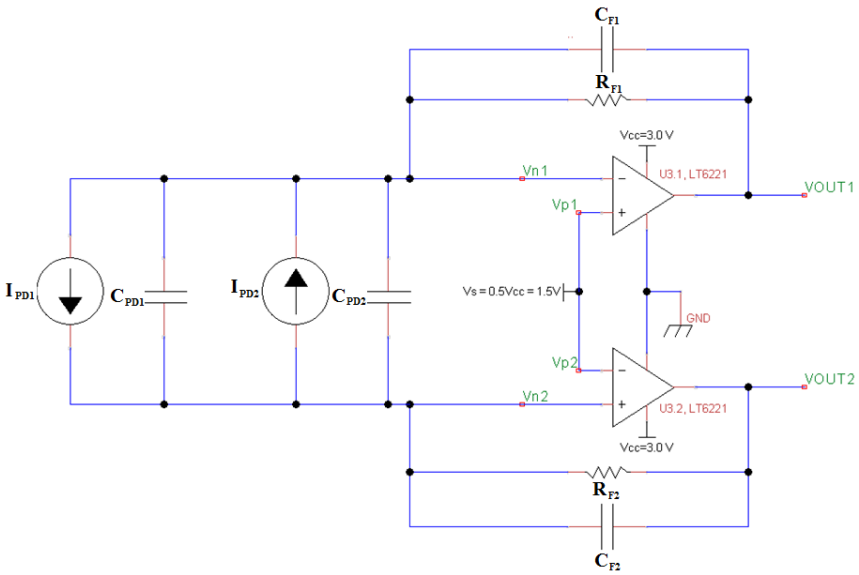


Figure 3.2: Design #1 Transimpedance Amplifier Setup. The two photodiodes PD1 and PD2 drive a current through TIA. The TIA converts the current to a voltage using two operational amplifiers, two feedback resistors, and two feedback capacitors. The TIA outputs a voltage range equal to the input range of the ADC. The design utilizes a differential, single supply setup to minimize the effect of noise.

Since the PDs of the optocouplers output a small current, the design uses a transimpedance amplifier (TIA) to translate this current into a voltage range the ADC can read. A TIA incorporates the photodiodes' capacitances, allowing compensation and correction for increased bandwidth. The measurement system uses the two transimpedance amplifiers with single supply setup as shown in Figure 3.2. Both amplifiers have a supply voltage of 3.0 V and bias $V_S$ of half the supply voltage, 1.5 V. A resistive divider using equal valued resistors power from the supply voltage produces the half supply voltage. The supply voltage of 3.0 V constrains the output of each op-amp to 3.0 V, translating to a -3.0 V to +3.0 V differential voltage range of the TIA.

When the measurement system measures a positive signal, photodiode 1, PD1, outputs current to the TIA. When the measurement system measures a negative signal, photodiode2, PD2, outputs current to the TIA. When the measurement system measures a zero valued signal, neither photodiode conduct and $V_{OUT1}$ and $V_{OUT2}$ equal the half supply voltage $V_S$. The feedback resistors conduct the current produced by the photodiodes. The left hand terminals of the feedback resistors hold at 1.5 V by the action of the op-amps and the right hand terminals of the resistors depart in opposite direction, reusing in a differential output voltage. When positive current drives the TIA from PD1, $V_{OUT1}$ drops and $V_{OUT2}$ rises in voltage. When negative current drives through the TIA from PD2, $V_{OUT1}$ rises and $V_{OUT2}$ drops in voltage. The differential voltage produced from two outputs falls in the voltage range of -3.0 V and +3.0 V. This output range then requires a bipolar ADC with an input voltage range of -3.0 V and +3.0 V.

Differential amplifiers' increased output voltage swing and their ability to provide increased noise immunity to external common-mode noise make them ideal for low voltages systems [16]. For a single TIA, the environment superimposes noise on the power supply and ground reference voltage and thus alters the output voltage. Figure 3.3 shows a single TIA with "noise" added to the supply voltage, Vcc, and the ground reference, GND_noise. Figure 3.4 shows the simulated input current signal and the output of the single TIA. As expected, the output signal experiences noise due to the noise in the ground reference.

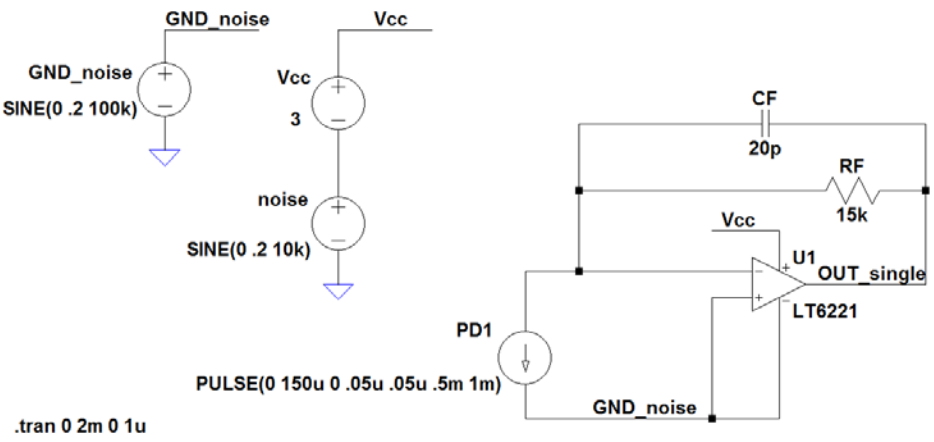


Figure 3.3: Simple TIA Simulation Schematic of Noise Immunity. The 3 V supply contains a 0.2 V, 10 kHz sine wave and the ground reference contains a 0.2 V 100 kHz sine wave to simulate noise. The simple TIA uses only one op-amp, one feedback resistor, and one capacitor to convert PD1's current to a voltage.

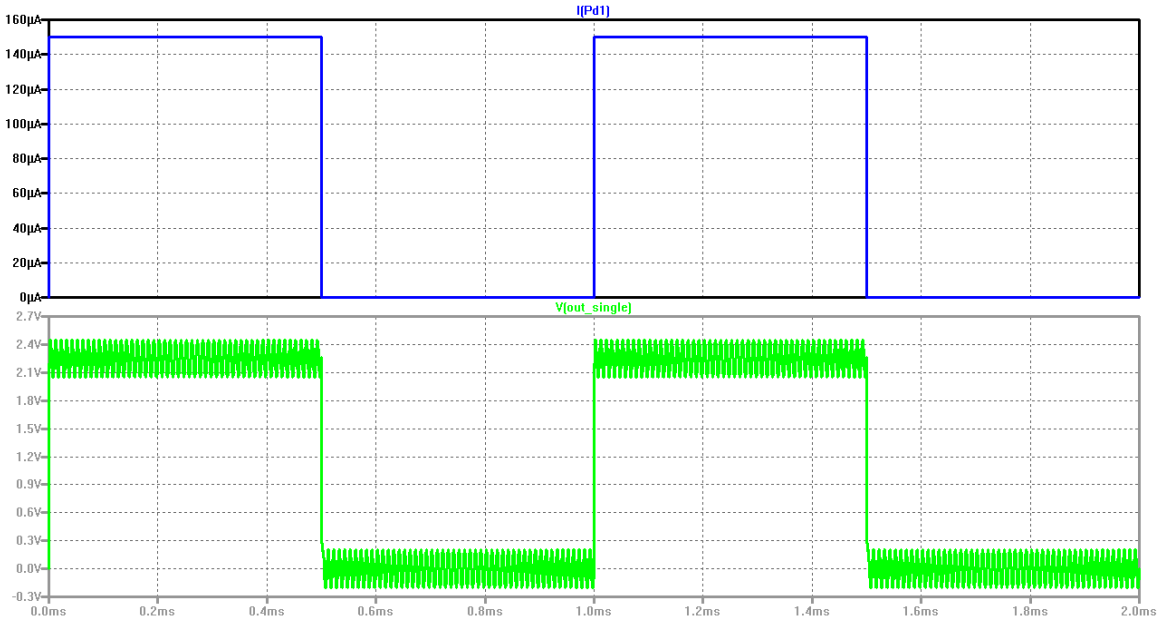


Figure 3.4: Single TIA Simulation. The TIA output experiences the 100 kHz noise added to the ground reference. Top - Input photodiode current, Bottom - TIA output.

In the case of the dual, single supply TIA, the noise of the supply voltage becomes irrelevant. Both outputs amplify with respect to the half supply voltage. A change in the half supply voltage due to noise affects both amplifiers in the same way and the differential output maintains the same value. Figure 3.5 shows the dual, single supply TIA schematic and Figure 3.6 shows its simulation. The lower frequency noise represents noise added to the supply voltage and the higher frequency noise represents the noise added to the ground reference. The individual outputs experience the added noise however the differential output outputs an accurate, noiseless signal. The noise affects the individual outputs in the same way and the TIA maintains the same differential voltage with respect to the input signal. The simulations in Figures 3.4 and 3.6 make the increased noise immunity for the differential TIA evident. Therefore the measurement system benefits substantially by using the differential design, as it needs to function in a noise harsh environment of EM waves.

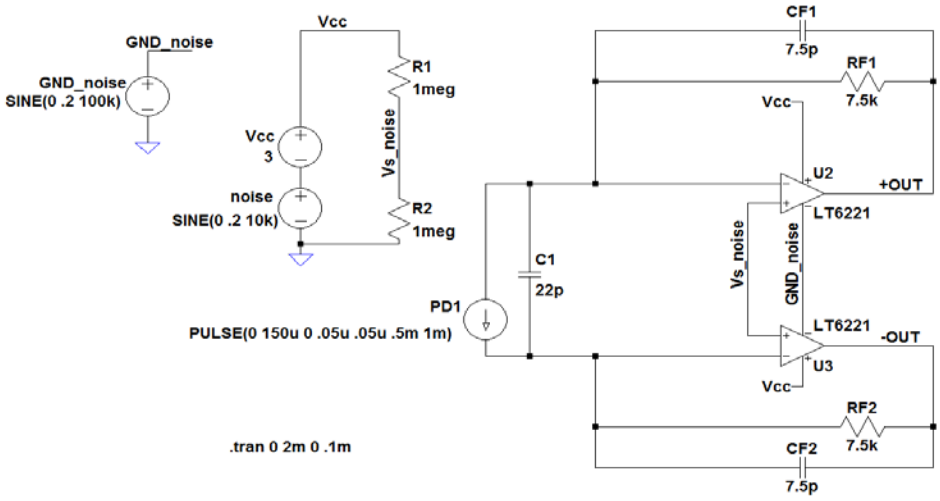


Figure 3.5: Differential, Single Supply TIA Schematic. The 3 V supply contains a 0.2 V, 10 kHz sine wave and the ground reference contains a 0.2 V, 100 kHz sine wave to simulate noise. The differential TIA uses two op-amps, two feedback resistors, and two capacitors to convert PD1's current to a voltage.

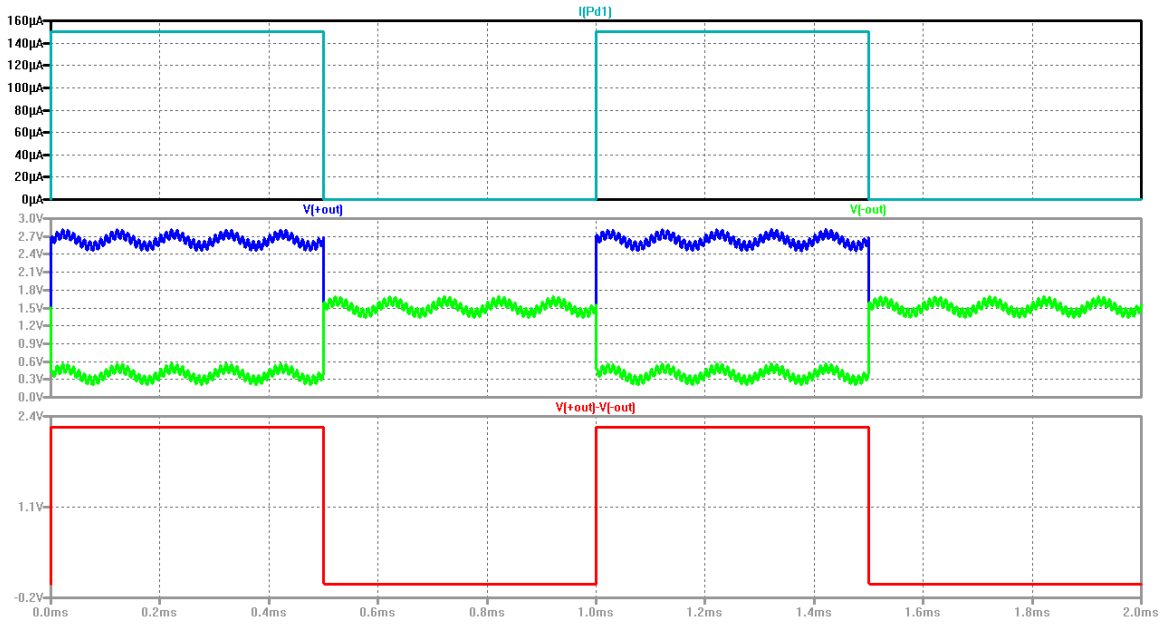


Figure 3.6: Differential, Split Supply TIA Simulation. Individually, the outputs of the TIA experience the noise added to the supply voltage and the noise added to the ground reference. However, the noise does not affect the differential TIA output. Top - Input photodiode current, Middle - Individual TIA outputs, Bottom - Differential TIA output

The derivation of the feedback resistor $R_F$ for amplification and the feedback capacitor for close-loop feedback stability follows. In the derivations, one source represents the two photodiodes. The source can output positive and negative current and has double the junction capacitance due to the parallel connection of the two photodiodes.

Operational amplifiers' positive inputs $V_P1$ and $V_P2$ and negative inputs $V_N1$ and $V_N2$ in Figure 3.2 have equal voltages.

$$V_P = V_N \tag{3.10}$$

Also in the dual, single supply transimpedance amplifier configuration in Figure 3.2, all of the voltages of the input terminals, $V_P1$, $V_P2$, $V_N1$, and $V_N2$, equal the half supply voltage $V_S$.

$$V_S = V_P1 = V_P2 = V_N1 = V_N2 \tag{3.11}$$

The current into both inputs of the operational amplifier equal zero.

$$I_P = I_N = 0A \tag{3.12}$$

The current produced by the $I_{pd}$ equals the current that passes through R of each transimpedance amplifier. Using Ohm's law:

$$V_s - V_{OUT1} = R_F(I_{PD}) \tag{3.13}$$

$$V_s - V_{OUT2} = R_F(-I_{PD}) \tag{3.14}$$

Solving for $V_{OUT1}$ and $V_{OUT2}$:

$$V_{OUT1} = R_F I_{PD} + V_S \tag{3.15}$$

$$V_{OUT2} = -R_F I_{PD} + V_S \tag{3.16}$$

The differential output of the dual, split supply transimpedance amplifier equals the difference of $V_{OUT1}$ and $V_{OUT2}$:

$$V_{OUT} = V_{OUT1} - V_{OUT2} \tag{3.17}$$

Substituting Equations 3.15 and 3.16 into Equation 3.17 gives the transfer function of the dual, split supply.

$$\frac{V_{OUT}}{I_{PD}} = 2R_F \tag{3.18}$$

Solving for $R_F$, Equation 3.18 calculates the feedback resistor for the TIA to provide a differential output of ±3.0 V when the photodiode outputs ±200 μA.

$$R_F = \frac{V_{OUT}}{2I_{PD}} = \frac{3.0V}{2 \times 200\mu A} = 7.5k\Omega \tag{3.19}$$

The issue of loop stability in the TIA is similar to that of an op-amp based differentiator. Maintaining stability ensures accurate readings produced by the measurement system. $R_F$ forms a low-pass network with $C_{PD}$. This additional parasitic

pole reduces the phase margin and compromises the stability of the loop. As seen in Figure 3.7, the feedback factor, 1/β, begins to increase at $f_Z$ at a rate of 20 dB/dec. $A_{VOL}$ graphs the open loop gain of the operational amplifier.

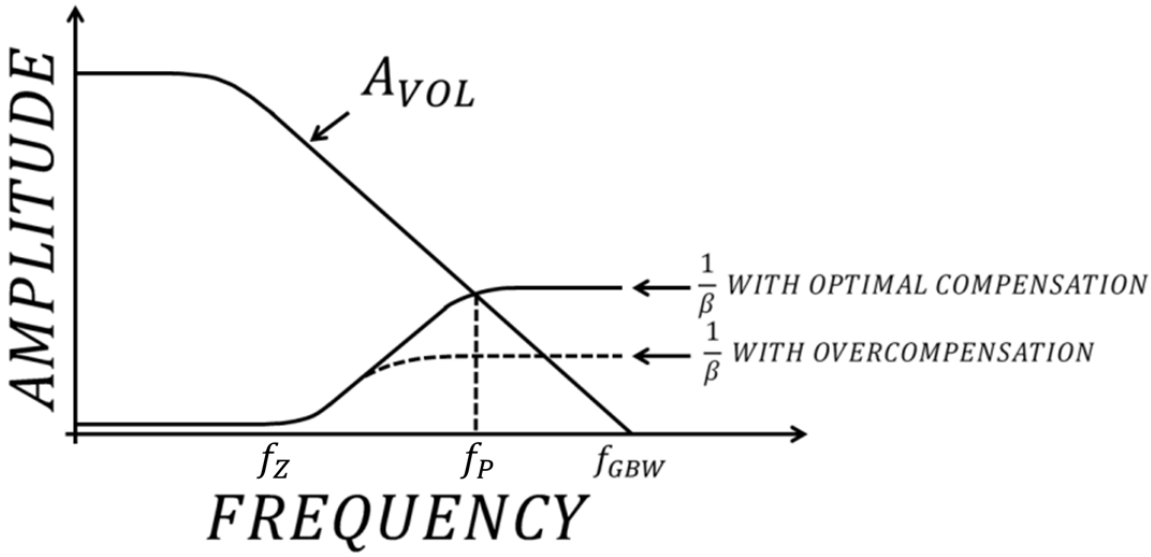


Figure 3.7: General TIA Frequency Response [17]. The plot shows the open loop gain $A_{VOL}$ and the feedback factor 1/β. The feedback factor begins to increase at the zero frequency $f_Z$ and then becomes constant again at the pole frequency $f_P$. The feedback capacitor dictates the pole frequency. To optimize gain and bandwidth, the ideal pole frequency lies in the middle of the gain bandwidth frequency $f_{GBW}$, and the zero frequency $f_Z$.

Without a feedback capacitor, the open loop gain and feedback factor have a rate of closure (ROC) of 40 dB/dec, implying very small phase margin [18]. A feedback capacitor, $C_F$, adds a pole in 1/β (zero in β) reducing the ROC and stabilizing the loop. However too large of a $C_F$ overcompensates for stability and the bandwidth of the TIA reduces unnecessarily. Determining a feedback capacitor that prevents instability but still maximizes bandwidth plays a crucial role in creating an accurate high frequency measurement system. This optimal feedback capacitor creates a pole in 1/β when the open loop gain and feedback factor intersect.

The ADC measures the differential output, calculated by the difference of the two individual TIA outputs.

$$V_{OUT} = V_{OUT1} - V_{OUT2} \tag{3.20}$$

Equation 3.21 calculates the transfer function, solved using a voltage divider across the photodiode's capacitance.

$$V_{PD} = \frac{Z_{PD}}{2Z_F + Z_{PD}} V_{OUT} \tag{3.21}$$

where the photodiode impedance $Z_{PD}$ and feedback impedance is:

$$Z_{PD} = \frac{1}{sC_{PD}} \tag{3.22}$$

$$Z_F = \frac{\frac{R_F}{sC_F}}{R_F + \frac{1}{sC_F}} = \frac{R_F}{sR_FC_F + 1} \tag{3.23}$$

Substituting Equations 3.22 and 3.23 into Equation 3.21 and solving for $V_{PD}/V_{OUT}$ which equals to 1/β:

$$\frac{1}{\beta} = \frac{V_{PD}}{V_{OUT}} = \frac{1 + sR_F(C_F + 2C_{PD})}{sR_FC_F + 1} \tag{3.24}$$

1/β indicates a zero and a pole as follows:

$$f_Z = \frac{1}{2\pi R_F(C_F + 2C_{PD})} \tag{3.25}$$

$$f_P = \frac{1}{2\pi R_F C_F} \tag{3.26}$$

As seen in Figure 3.7, the geometric mean of $f_Z$ and $f_{GBW}$ corresponds to the optimal frequency to place the compensating pole.

$$f_P = \sqrt{f_Z \cdot f_{GBW}} \tag{3.27}$$

Substituting Equation 3.25 into 3.27:

$$f_P = \sqrt{\frac{f_{GBW}}{2\pi R_F(C_F + 2C_{PD})}} \tag{3.28}$$

Equating Equations 3.28 and 3.26:

$$\sqrt{\frac{f_{GBW}}{2\pi R_F(C_F + 2C_{PD})}} = \frac{1}{2\pi R_F C_F} \tag{3.29}$$

Solving for $C_F$ results in the optimal value of the feedback capacitor:

$$C_F = \frac{1 + \sqrt{1 + 16\pi R_F C_{PD} f_{GBW}}}{4\pi R_F f_{GBW}} \tag{3.30}$$

Maxim Integrated recommends a little overcompensating by using a 40% tolerance of the gain bandwidth to ensure stability [17]. From the datasheets, the one photodiode has a capacitance of 22 pF and the operational amplifiers have a gain bandwidth product of 60 MHz. Because of the parallel connection of the two photodiodes in Design #1, the photodiode capacitance doubles to 44 pF. Calculating the measurements systems optimal feedback capacitor:

Use 60% of GBW: GBW = 60 MHz => $f_{GBW}$ = 36 MHz

$$C_F = \frac{1 + \sqrt{1 + 16\pi(7.5k\Omega)(44\text{pF})(36\text{MHz})}}{4\pi(7.5k\Omega)(36\text{MHz})} = 7.5\ pF$$

The frequency at which the pole occurs in Figure 3.7 also approximately equals the TIA bandwidth. With a feedback resistor of 7.5 kΩ, feedback capacitor of 7.5 pF and using Equation 3.26 the TIA bandwidth equals 2.83 MHz.

$$BW \approx f_P = \frac{1}{2\pi(7.5K\Omega)(7.5pF)} = 2.83\ MHz$$

### 3.3.1 Design #1 TIA Simulation

LTspice IV simulates the functionality and performance of the TIA using the schematic in Figure 3.8. Current sources PD1 and PD2 represent the photodiodes of the optocouplers and Figure 3.9 shows the simulated outputs, measured individually and differentially.

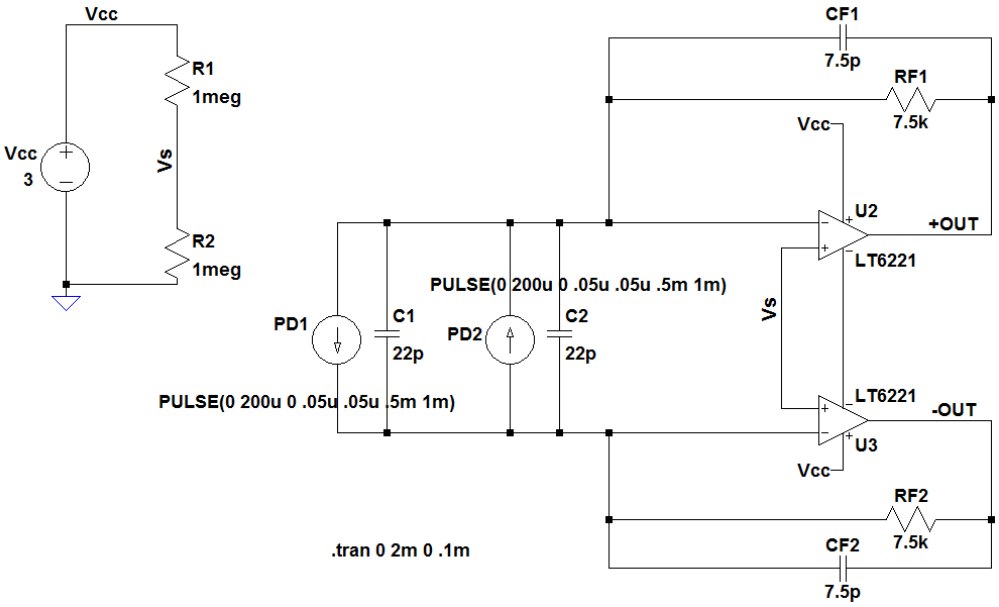


Figure 3.8: Design #1 TIA Simulation Schematic. The schematic simulates the two photodiodes as current sources with capacitances of 22 pF. The current sources drive the differential TIA and the outputs are measured to show functionality and frequency response.

The simulated photodiodes produce square waves with a 180 degree phase shift, as seen in Figure 3.9. This simulates the effect of a square wave containing both positive and negative signal driving the input of the full design. Only one photodiode conducts at a time depending on if the input signal consists of positive or negative voltage.

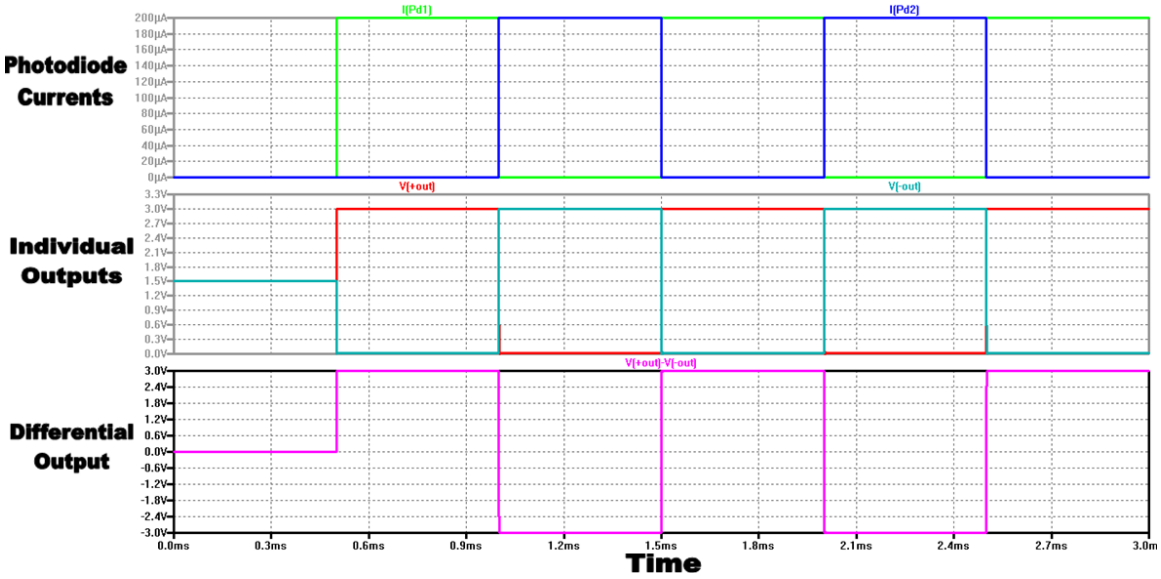


Figure 3.9: Design #1 TIA Simulation Plots. The photodiodes output a 180 degree out of phase pulses. This simulates a pulse containing covering the full input range of the system. The individual outputs swing from 0 V to 3 V depending on which photodiode outputs current. Thus the differential output swings from -3 V to 3 V. Top – photodiode 1 current source (green), photodiode 2 current source (blue). Middle - +OUT (red), -OUT (turquoise). Bottom – differential output (pink)

The center plot of Figure 3.9 plots the individual outputs +OUT and –OUT. With no signal driving the TIA, both outputs hold at 1.5 V. When a positive signal drives the measurement system, photodiode 1 conducts and the top amplifier amplifies the signal positively to +OUT and the bottom amplifier amplifies negatively to -OUT. The differential output produces a voltage ranging from 0 V to +3 V. When a negative signal drives the measurement system, photodiode 2 conducts and the top amplifier amplifies the signal negatively to +OUT and the bottom amplifier amplifies the signal positively to –OUT. The differential output produces a voltage ranging from 0 V to -3 V. Therefore, the differential output ranges from -3 V to +3 V for an input signal spanning the full input voltage range.

## 3.4 Design #1 Optocoupler Characterization

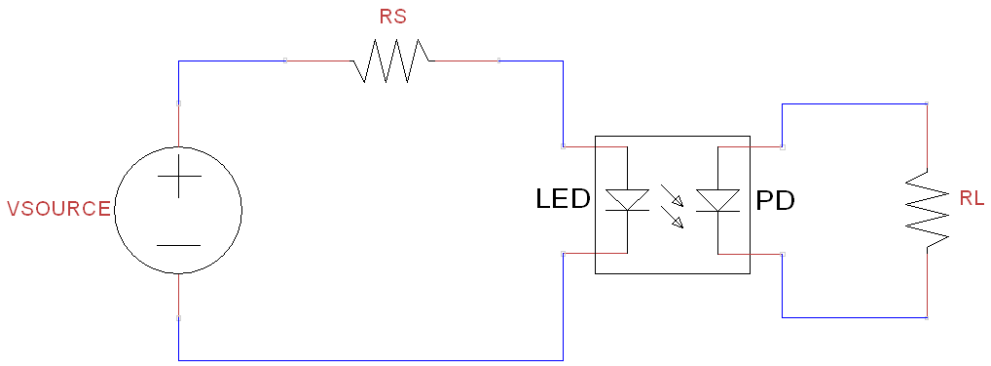


Figure 3.10: Optocoupler Characterization Setup. VSOURCE varies from 0 V to 10 V and the current through the load RL is measured. Rs = 220 Ω, RL = 1 kΩ

The setup in Figure 3.10 characterizes the two optocouplers used in Design #1. The actual CTR of each optocoupler determines the values of the front-end resistors for compensations. Utilizing the full input current range of 0-40 mA produces the largest output current range. Outputting the widest range of current translates to maximum resolution and minimum quantization error at the measurement systems output. The input series resistance $R_S$ dictates the amount of current driven through the input LED. The optimal value of $R_S$ maximizes the current range without exceeding 40 mA. The $R_S$ has a theoretical value of 105 Ω as in Design #1 for the test pulse with peak value of 10 V. A 120 Ω resistor is the closest available resistor and used as $R_S$ during characterization along with a 1 kΩ resistor as $R_L$. Note: $R_L$ equals a small value to avoid forward biasing the PD.

Figure 3.11 plots the photodiode current versus source voltage. This shows a dead zone where the LED voltage has not yet reached the turn on voltage for the LED in the optocoupler. Current does not begin to transfer until the input voltage reaches about

1.5 V. This dead zone does not pose much of a problem because when inputting hundreds of volts, the small amount of voltage needed to turn on the LEDs becomes negligibly small compared to the input drive. However, it can cause delays in the system response when the input signal switches polarities due to the time needed to charge the LEDs to their forward voltages.

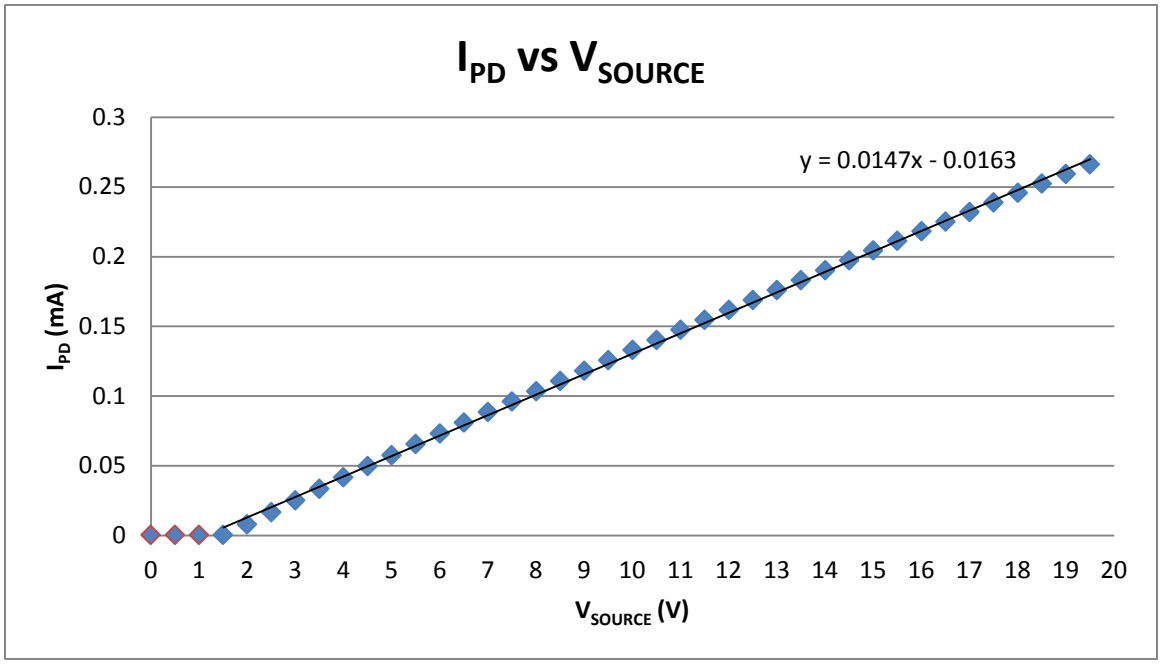


Figure 3.11: Optocoupler Photodiode Current Versus Source Voltage Characterization. The plot shows the existence of a dead zone and then a linear relationship between voltage source and photodiode current.

To determine the transfer ratio K of the optocouplers, the power supply $V_{SOURCE}$ varies from 0-10 V and two ammeters measure the input and output current of the optocouplers. Figure 3.12 plots the optocouplers' photodiode output current versus the LED's input current and applies linear fit line. The slopes of the line indicate the actual transfer ratio K of the optocouplers and equal 3.6 μA/mA and 4.1 μA/mA. Using Equation 3.1, a maximum input current of 40mA through the LEDs results in a maximum output current of 144 μA and 164 μA through the photodiode 1 and photodiode 2.

$$I_{PD1} = 0.0036 \times 40mA = 144\ \mu A$$

$$I_{PD2} = 0.0041 \times 40mA = 164\ \mu A$$

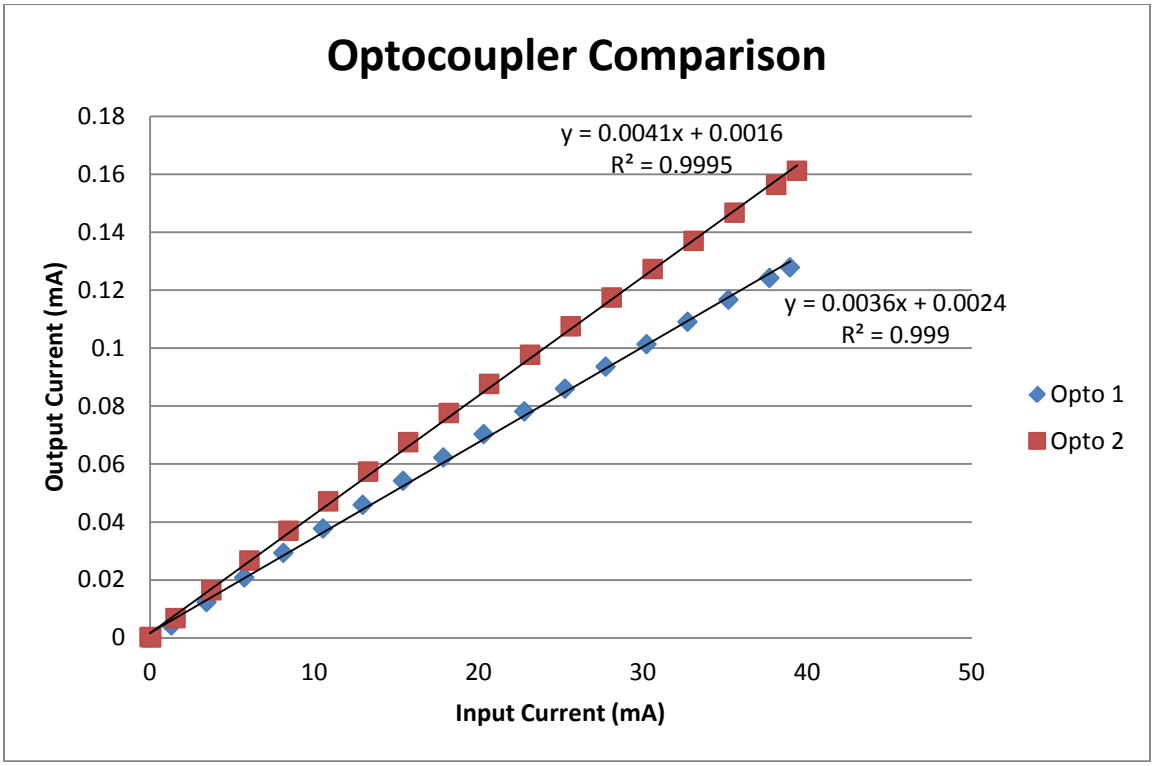


Figure 3.12: Optocouplers' Transfer Characteristics. Both optocouplers are characterized by measuring and graphing their output current in response to a DC current input. The slope of the each characterization equals the CTR of each optocoupler.

The difference in CTRs due to the optocouplers' mismatched diodes pose a significant problem. Photodiode 1 outputs less current for a positive signal than photodiode 2 outputs for a negative signal of equal magnitude. This translates to smaller magnitude in differential TIA output voltage for positive signals than negative signals of equal magnitude. Therefore, the ADC produces disproportionate data that requires slope correction during digital post-processing.

## 3.5 Design #1 Low Voltage Test

A low voltage test is applied to Design #1. Figure 3.13 displays the input voltage varied from -8.0 VDC to 6.6 VDC, the range the input current does not exceed ±40 mA, and the resulting output voltage.

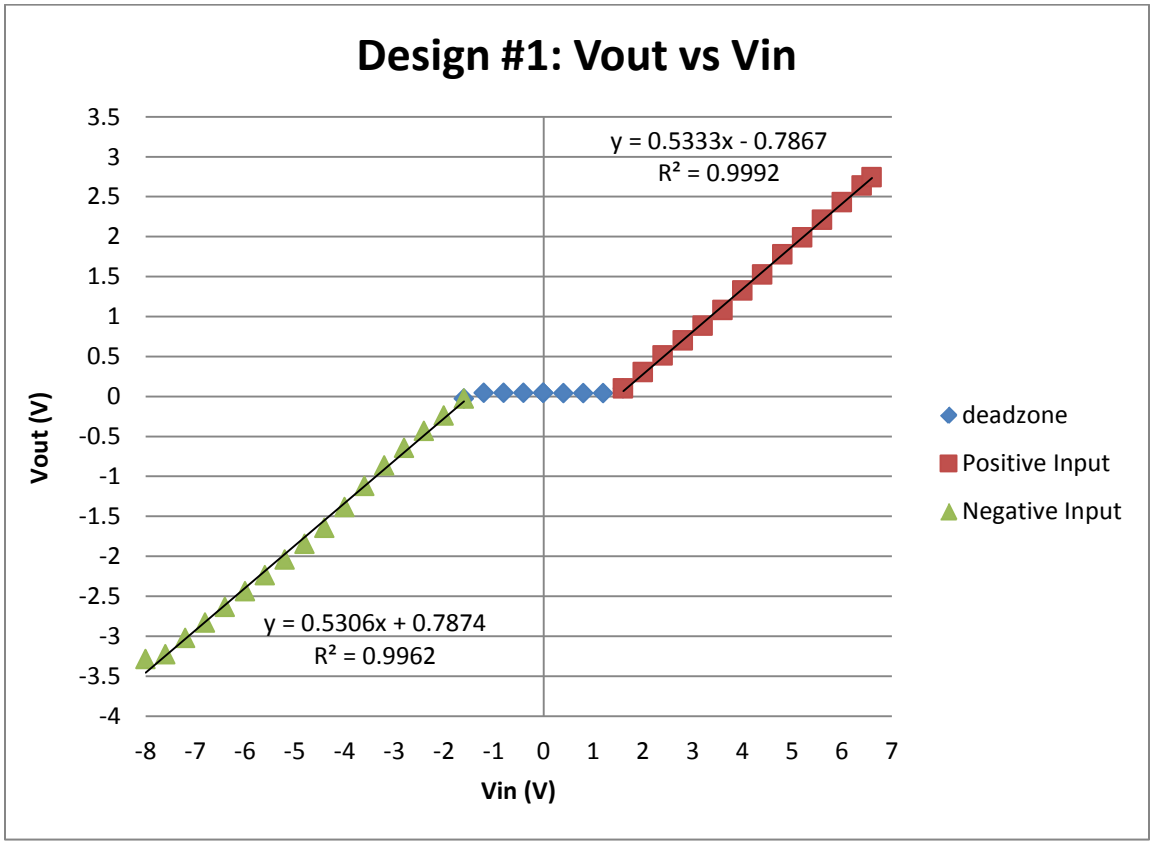


Figure 3.13: Design #1 Transfer Characteristics for DC Test. The plot shows the differential output $V_{OUT}$ response when the input voltage varies from -8 V and 6.6 V.

Ideally the positive and negative and portions of a signal have the same gain in order to maintain gain linearity for positive and negative signals of equal magnitude. A positive input has a gain of 0.5333 and a negative input has gain of 0.5306. With an acceptable 0.51% error in gain, digital data processing can easily correct the error.

Additionally, both polarities would have the same y-intercept magnitudes to ensure more offset does not occur for one optocoupler than the other. Each trendline has

very similar y-intercepts, -0.7867 for a positive input and 0.7874 for a negative input. The resulting 0.089% offset error is also acceptable and a small adjustment digitally.

When a 1 kHz, 0-10Vpp square wave drives the system, the individual outputs of the amplifiers show different gains as seen in Figure 3.14. The TIA measured by channel 1 outputs a peak-to-peak voltage of 1.844 V and the other TIA measured by channel 2 outputs a peak-to-peak voltage of 3.219 V. For a photodiode current of 144 μA, this translates to gains of 12806 V/A and 22354 V/A for channel 1 and channel 2 TIAs, a 74.5% increase in gain from the first TIA to the second.

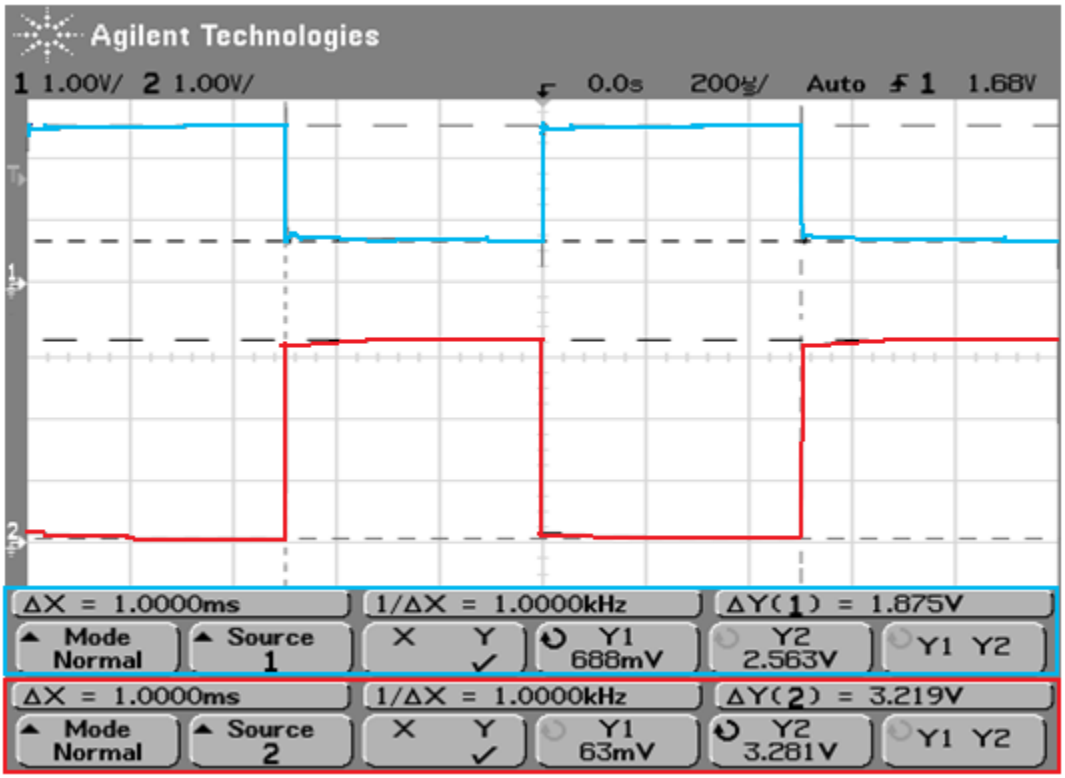


Figure 3.14: Outputs of the Two Amplifiers Used in the Design #1 TIA, VOUT1 and VOUT2. Channel1 produces a square wave with a peak-to-peak voltage of 1.844 V and Channel2 produces a square wave with a peak-to-peak voltage of 3.219 V.

These insufficient results led to the decision to redesign the system and use only one optocoupler.

# 4. Final Design: Improved Analog Front-End Using Single Optocoupler

The final design is similar to Design #1, but uses only one optocoupler instead of two. The final design in Figure 4.1 makes use of a pair of resistors, a full bridge rectifier, one optocoupler, a dual, single supply TIA, and an ADC. The front-end of the measurement system consists of two resistors, a full-bridge rectifier and a high linearity optocoupler. The front end provides optical isolation to preserve both the measured and measurement system. During this process, the measured voltage rectified and converted into an isolated current. The TIA then converts the isolated current to the input voltage range of the ADC.

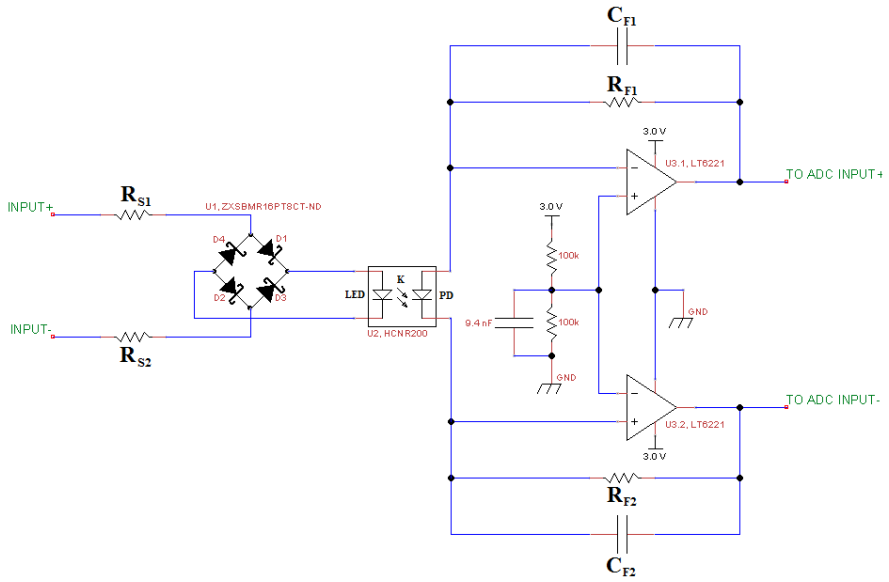


Figure 4.1: Analog Front-End Using Single Optocoupler and Bridge Rectifier. The design consists of two front end resistors, one full bridge rectifier, one optocoupler, and a differential TIA. An ADC samples the TIA's output and stores the data for the user to read and analyze.

## 4.1 Final Design Optocoupler

The optocoupler for the final design functions in the same way as in Design #1, provides isolation by producing a linearly related current from its input to its output. As stated before, a diode based optocoupler only allows current in one direction. Therefore, a full bridge rectifier converts the signal to purely positive for a single optocoupler to isolate the entire signal.

One advantage of using only one optocoupler instead of two as in Design #1 is that the design no longer needs optocoupler matching. Generally, any two optocoupler have different transfer ratios along with voltage drops across them, producing disproportionate results. Using one optocoupler ensures the same gain for both positive and negative signals and thus more accurate results. The single optocoupler simplifies digital post-processing by only requiring an inversion (multiplication by -1).

Using one optocoupler also provides the advantage of a decreased switching time when the signal switches between positive and negative voltages. Design #1 uses one optocoupler for positive signal and another for negative signal. During the switching time, the measured signal does not translate to the output and thus the system does not output any relevant data. With a forward LED voltage of 1.6 V, the two parallel optocoupler LEDs have a voltage of +1.6 V across them when a measurement system measures a positive signal. The voltage across the LEDS must change to -1.6 V to activate the other LED when the signal switches to a negative signal. Therefore, the LEDs must swing 3.2 V when the signal switches polarities. This swing takes time and

introduces a delay. This also affects the bandwidth of the system as this delay limits the system from fast switching signals.

Using one optocoupler to handle both polarities nearly eliminates switching time for fast changing signals. For a slow changing signal, the LED would conduct for a positive signal, stop conducting when the signal drops below the forward voltage as it transitions to negative signal, then must charge back up to the forward voltage to begin conducting again for the negative signal, a 3.2 V swing. Because the signal changes slowly, delays will not be very apparent. For a fast changing signal the LED conducts for an initial positive signal. As the signal transition from positive to negative, the LED begins to discharge and drops below its forward voltage. But before the LED fully discharges to zero, the negative signal creates enough voltage across the LED to continue conduction. For slow switching signals, the LED experiences a 3.2 V swing but if the polarity switch occurs fast enough, the LED experiences nearly no delay. Whereas in the two parallel LED case in Design #1, the optocoupler always needs a 3.2 V swing and produces a delay.

## 4.2 Full Bridge Rectifier

The full bridge rectifier allows the use of a single optocoupler. The full bridge rectifier takes in an AC input voltage and outputs the absolute value of the signal, creating a purely positive AC signal.

$$V_{OUT} = |V_{IN}| \tag{4.1}$$

When a sufficiently positive signal drives the system, the signal starts at INPUT+ and passes through D1, then through the LED, through D1, and returns back to the source at

INPUT-. When negative, the signal starts at INPUT- and passes through D3, then through the LED, through D4, and returns back the source at INPUT+. Both the positive and negative parts of the signal pass through the LED in same direction, from the anode to the cathode, and therefore the signal appears purely positive across the LED.

The rectifier also needs to accurately reproduce the absolute value of a high frequency signal. It does this by implementing a configuration using Schottky diodes. Schottky diodes find an important role in high-power circuits and fast switching applications [19]. As opposed to a regular pn junction diode, Schottky diodes replace the p-doped region with a metal contact. This gives them faster reverse recovery times and smaller turn-on voltages. In order to handle a 1 MHz signal, the Schottky diodes must have a reverse recovery time of much less than 1 μs. The measurement system uses a ZXSBMR16PT8CT Schottky full bridge rectifier to meet these requirements.

### 4.2.1 Full-Bridge Rectifier Characterization

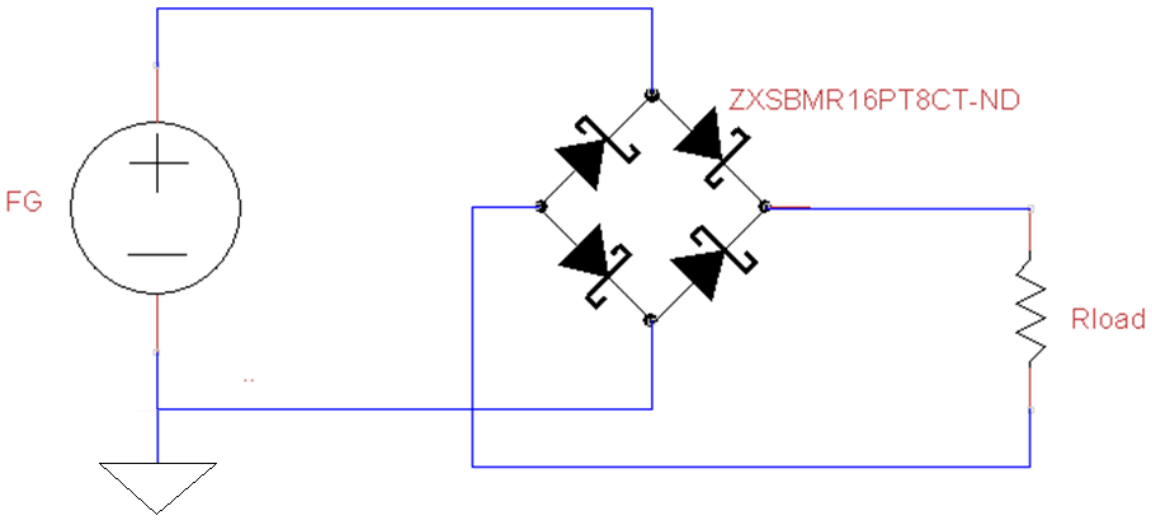


Figure 4.2: Full-Bridge Rectifier Characterization Setup. The function generator FG drives a sinusoidal signal through the rectifier and an oscilloscope measures the voltage across the load resistance.

Figure 4.2 displays the setup used to characterize the full-bridge rectifier. The function generator drives a 9.55 Vp, 1 kHz sinusoidal wave through the rectifier and the oscilloscope measures the voltage across the load resistance. Figure 4.3 displays the fully rectified signal at the output as expected with 9.06 Vp amplitude. The difference in amplitude between the input and output equals the voltage drop across two of the Schottky diodes. Therefore one Schottky diode has voltage drop of 245 mV.

$$V_{F,Schottky} = \frac{V_{P,in} - V_{P,out}}{2} = \frac{9.55V - 9.06V}{2} = 245\ mV \tag{4.2}$$

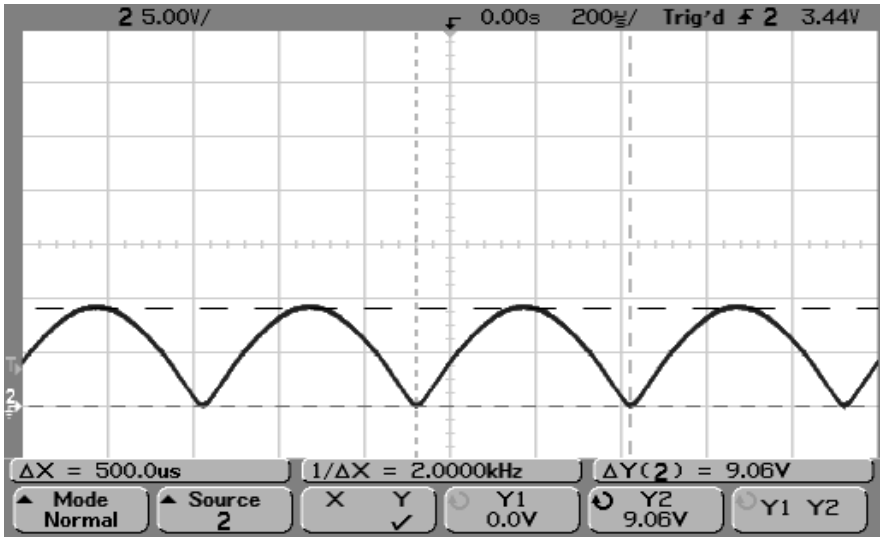


Figure 4.3: Full-bridge Rectifier Characterization Output. The function generator drives a 19.2Vpp, 1 kHz sinusoidal input and the rectifier outputs a 9.06Vp, 2 kHz rectified sinusoid.

## 4.3 Front-End Resistors

The two resistors convert the high voltage signal to a current ranging from 0-40 mA for the LED of the optocoupler. As opposed to the Design #1, the front-end resistor calculations must take into account the voltage drop from the full bridge rectifier and the fact the signal no longer splits into positive and negative parts. The following derives the value of the front-end resistors for final design.

The two resistors in this system have the same current, I, passing through them and have equal resistance:

$$R_S = R_{S1} = R_{S2} \tag{4.3}$$

Using Ohm's Law:

$$R_S = \frac{V_R}{I_{LED}} \tag{4.4}$$

Applying KVL to the front end gives:

$$V_s + V_{R1} + V_{D1(D3)} + V_{D2(D4)} + V_{LED} + V_{R2} = 0 \tag{4.5}$$

Because the front end resistors equal each other, they also have same voltage drop across them:

$$V_R = V_{R1} = V_{R2} \tag{4.6}$$

All of the Schottky diodes in the rectifier have the same forward voltage:

$$V_D = V_{D1(D3)} = V_{D2(D4)} \tag{4.7}$$

Substituting Equations 4.6 and 4.7 into Equation 4.5:

$$V_s - 2V_R - 2V_D - V_{LED} = 0 \tag{4.8}$$

And solving for $V_R$:

$$V_R = \frac{V_s - 2V_D - V_{LED}}{2} \tag{4.9}$$

Now substituting Equation 4.9 into 4.4:

$$R_S = \frac{V_s - 2V_D - V_{LED}}{2I_{LED}} \tag{4.10}$$

From the rectifier and optocoupler's datasheets, $V_D$ = 305 mV and $V_{LED}$ = 1.6 V. And given the desired source voltage of 500 V and the LED's maximum LED input current of

40 mA, Equation 4.10 calculates the resistance of each resistor, $R_{S1}$ and $R_{S2}$, to have a value of 6222 Ω.

$$R_S = \frac{500V - 2(305mV) - 1.6V}{2(40mA)} \approx 6222\ \Omega$$

Equation 3.9 calculates the power rating of each resistor, R1 and R2, as 9.96 W.

$$Power = (40mA)^2 \times 6222 \approx 9.96\ W$$

For final design, the front-end resistors have a value 7.5 kΩ with a power rating of 25 W.

## 4.4 Final Design Differential, Single Supply Transimpedance Amplifier

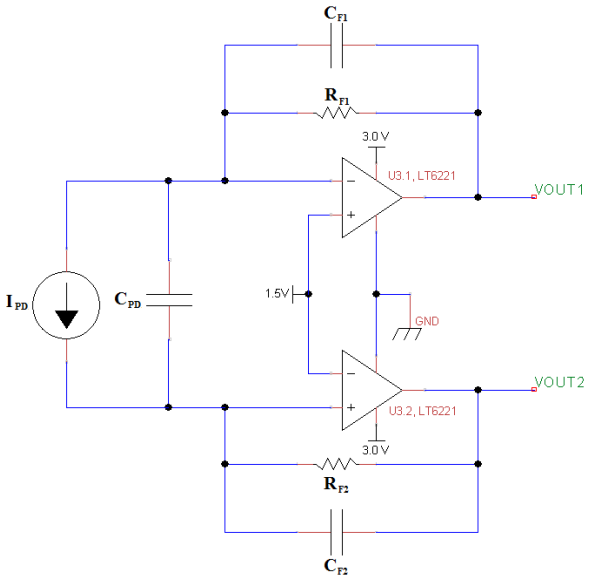


Figure 4.4: Final Design Transimpedance Amplifier Setup. A single photodiode supplies a current through the TIA and the differential output is measured.

The TIA for final design has the same design as the TIA in Design #1, but driven by only one photodiode instead of two. The feedback resistors maintain the same values of 7.5 kΩ, but the feedback capacitors have slightly different values. Equation 3.30 still calculates the optimum feedback capacitor, but because the design uses only one photodiode, the photodiode capacitance now equals 22 pF.

$$C_F = \frac{1 + \sqrt{1 + 16\pi(7.5k\Omega)(22\text{pF})(36\text{MHz})}}{4\pi(7.5k\Omega)(36\text{MHz})} = 5.40pF$$

With a feedback resistor of 7.5kΩ, a feedback capacitor of 5.40 pF and Equation 3.26 the TIA has an approximate bandwidth of 3.93 MHz.

$$BW \approx f_P = \frac{1}{2\pi(7.5K\Omega)(5.40pF)} = 3.93\ MHz$$

### 4.4.1 Final Design TIA Functionality Simulations

The final design uses the same TIA setup however only PD drives the circuit, resulting in only positive signal at the output.

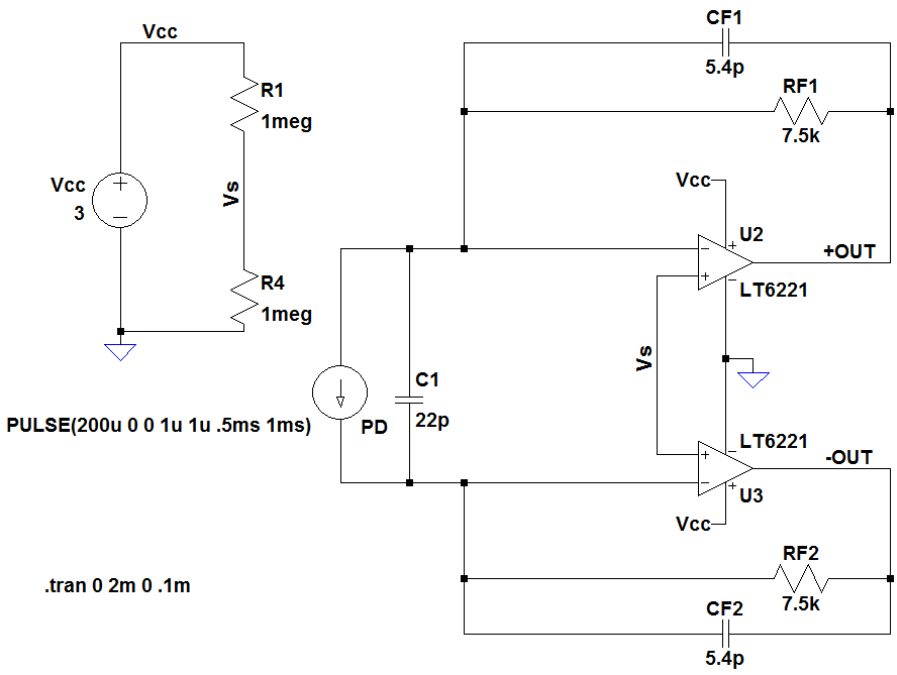


Figure 4.5: Final Design TIA Simulation Schematic: A single photodiode drives a pulse train ranging from 0 µA to 200 µA. A 3V source supplies the operational amplifiers and half the supply source drives the positive inputs. The simulator measures the individual and differential outputs.

The TIA still functions the same as in Design #1, just without a second source to provide opposite current. The output plot in Figure 4.6 shows the result of the given photodiode current and successfully converts the current to a 0-3 V range for the ADC to read.

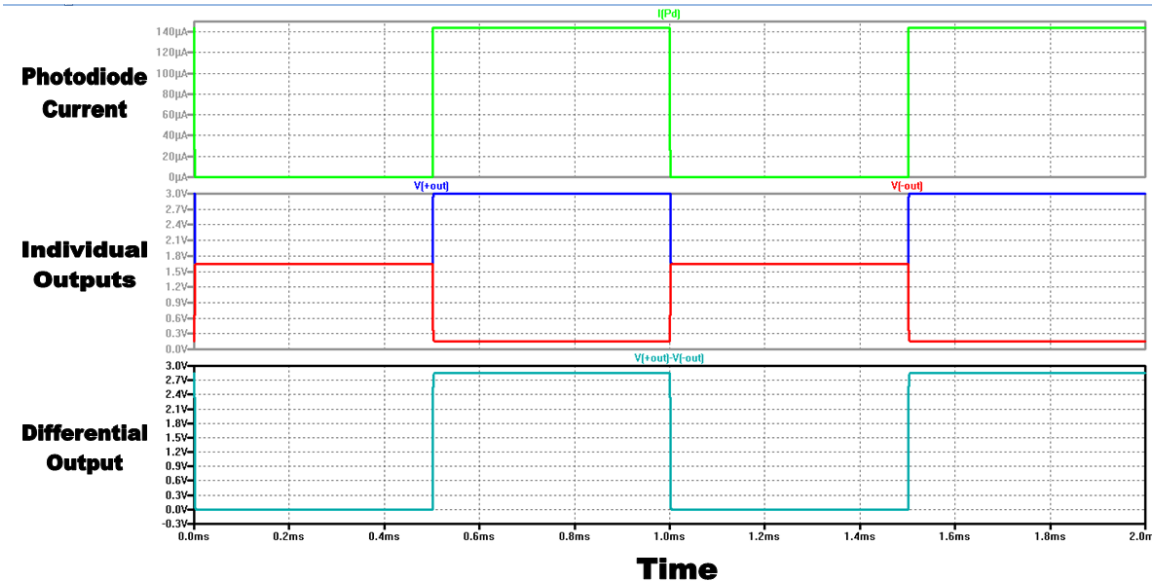


Figure 4.6: Final Design TIA Simulation Plots. In response to the photodiode current, $V_{+OUT}$ varies from 1.5 V to 3 V and $V_{-OUT}$ varies from 0 V to 1.5 V. Therefore, the differential output has a range of 0 V to 3 V. Top – Photodiode Current (green). Middle - +OUT (blue), -OUT (red). Bottom – Differential Output (turquoise)

### 4.4.2 Final Design TIA Frequency Response Simulation

Figure 4.7 simulates the frequency response of the TIA using various feedback capacitors. This assists in determining the TIA's bandwidth. The value of the feedback capacitor dictates the bandwidth and must be optimized to ensure the TIA can handle 1 MHz signals. The optimal feedback capacitor maximizes bandwidth while still maintaining system stability. While a small feedback capacitor like 1pF creates peaking and possible oscillation, a larger feedback capacitor like 15 pF begins to decrease gain at earlier frequencies.

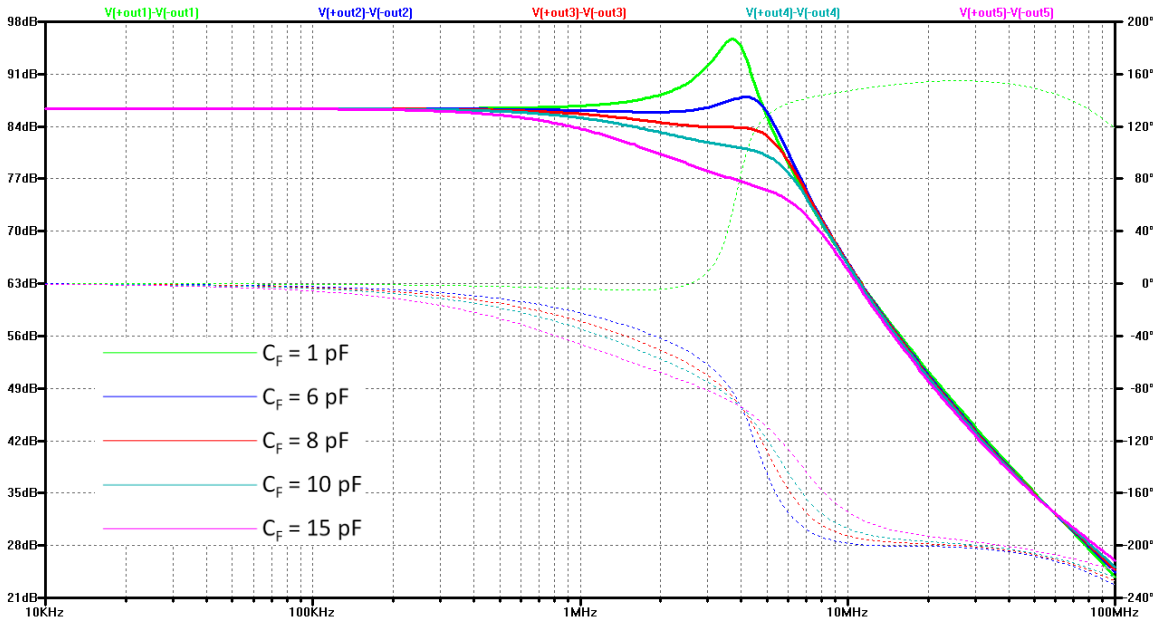


Figure 4.7: Transimpedance Amplifier Frequency Response. The simulation plots the TIAs frequency response for different values of feedback capacitors.

### 4.4.3 Final Design TIA Step Response Simulation

Figure 4.8 shows the step response of the TIA. The use of a small feedback capacitor (1pF) results in unstable (oscillatory) closed-loop behavior. A larger feedback capacitor (15pF) leads to a longer rise time and results in inaccurate results for fast varying signals.

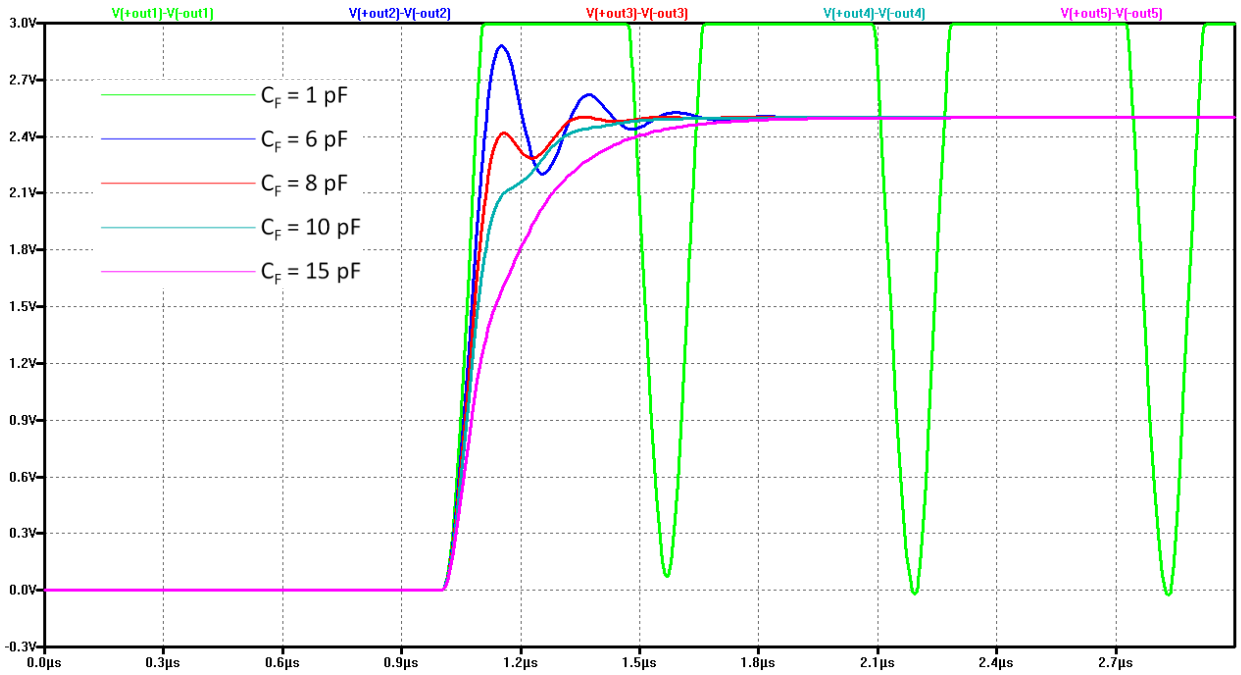


Figure 4.8: Transimpedance Amplifier Step Response. The simulation plots the TIAs frequency response for different values of feedback capacitors.

The frequency response and pulse response indicates an 8 pF feedback capacitor performs best. The 8 pF capacitor satisfies the 1 MHz bandwidth requirement and results in minimal overshoot and ringing when a pulse occurs.

### 4.4.4 Final Design TIA Characterization

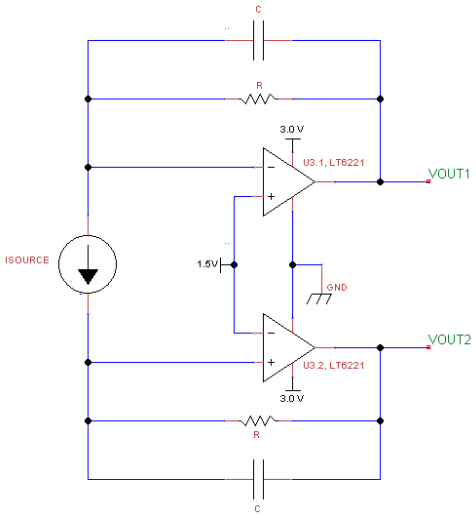


Figure 4.9: Transimpedance Amplifier Characterization Setup. A Keithley 2400 SourceMeter acts as the current source and a Agilent 34401A Multimeter measures the outputs, both individual and differential.

Figure 4.9 displays the setup used to characterize the final design TIA. In the overall final design, the output of the optocoupler connects to the TIA meaning the each operational amplifier needs to convert the 144 µA output current from the optocoupler to 1.5 V, to result in a 3.0 V differential output. Equation 3.19 calculates the feedback capacitor to have a value of 10417 Ω and there for the measurement system uses an 11 kΩ resistor.

$$R_F = \frac{V_{OUT}}{2I_{PD}} = \frac{3.0\ V}{2 \times 144\mu A} = 10417\ \Omega$$

Because the system uses a larger feedback resistor than required, the supply voltage increases to 3.3 V during characterization to prevent railing and to observe the full output range of the TIA. The power supply returns to 3.0 V for implementation in order to protect the ADC channels from any overvoltage damage.

Initially, the TIA does not contain feedback capacitors. As expected, this results in oscillation. An 8.2 pF feedback capacitor in parallel with the feedback resistor eliminates this oscillation.

The input current $I_{SOURCE}$ varies from 0 to 144 µA and the output voltages at each operational amplifier, $V_{OUT1}$ and $V_{OUT2}$, is measured along with the differential output $V_{OUT}$. Figure 4.10 plots $V_{OUT1}$ and $V_{OUT2}$ against $I_{SOURCE}$ and verifies each operational amplifier operates independent from one another.

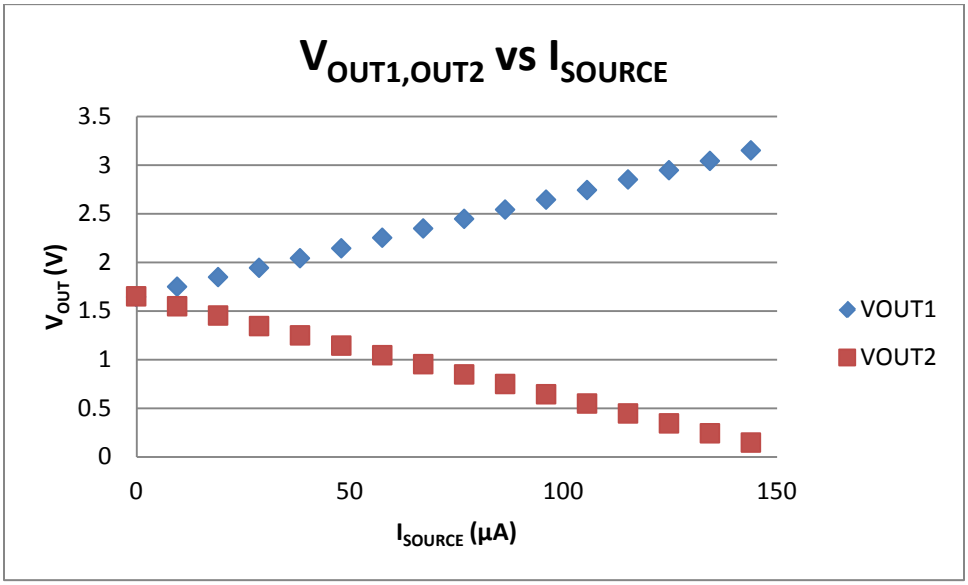


Figure 4.10: Transimpedance Individual Output Voltages Versus DC Source Current Characterization. The DC source current varies from 0µA to 144µA and the individual outputs vary by 1.5V.

$V_{OUT1}$ has a positive linear relationship with $I_{SOURCE}$, increasing from 1.5 V to 3 V as the $I_{SOURCE}$ increases from 0 to 144 µA. $V_{OUT2}$ has a negative linear relationship with $I_{SOURCE}$, decreasing from 1.5 V to 0 V as the $I_{SOURCE}$ increases from 0 to 144 µA. The difference between these two inputs would suggest the output voltage $V_{OUT}$ increases

from the full range of 0 V to 3 V as $I_{SOURCE}$ varies from 0 to 144 µA. Figure 4.11 plots $V_{OUT}$ versus $I_{SOURCE}$, verifying this operation.

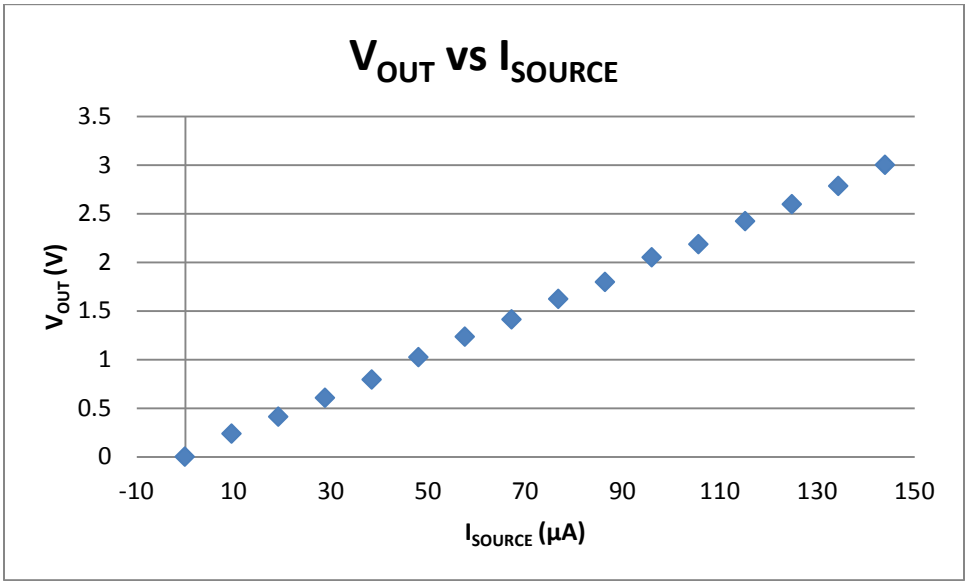


Figure 4.11: Transimpedance Amplifier Differential Output Voltage Versus Source Current Characterization. The current source varies from the 0µA to 144µA and the differential output $V_{OUT}$ linearly increases to about 3V.

Finally, a square wave ranging from 0 µA to 144 µA drives the final design TIA, and the differential output produces a well define square wave ranging from 0 V to 3.15 V.

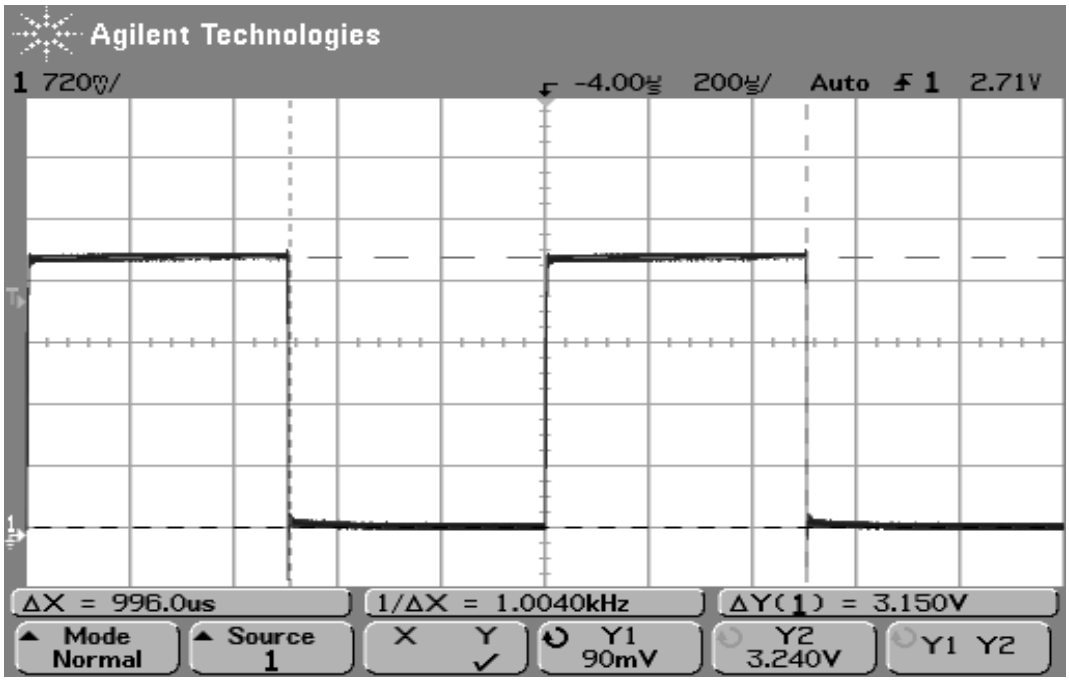


Figure 4.12: Transimpedance Amplifier AC Current Input Characterization. The Keithley 2400 SourceMeter drives a 1 kHz square wave ranging from 0 µA to 144 µA through the TIA. The TIA outputs a 1 kHz square wave ranging from 0V to 3.15 V.

## 4.5 Final Design Low Voltage Test

Figure 4.13 shows the output voltage when a DC voltage varied from -10 V to 10 V drives the full system. Weather the input voltage is positive or negative the system outputs a positive voltage. The positive and negative parts have close gain magnitudes of 0.4073 and 0.4062, a 0.27% difference. They also have close offset of -0.7301 and -0.7238, a 0.86% difference. This proves close to equivalent outputs for inputs of the same magnitude.

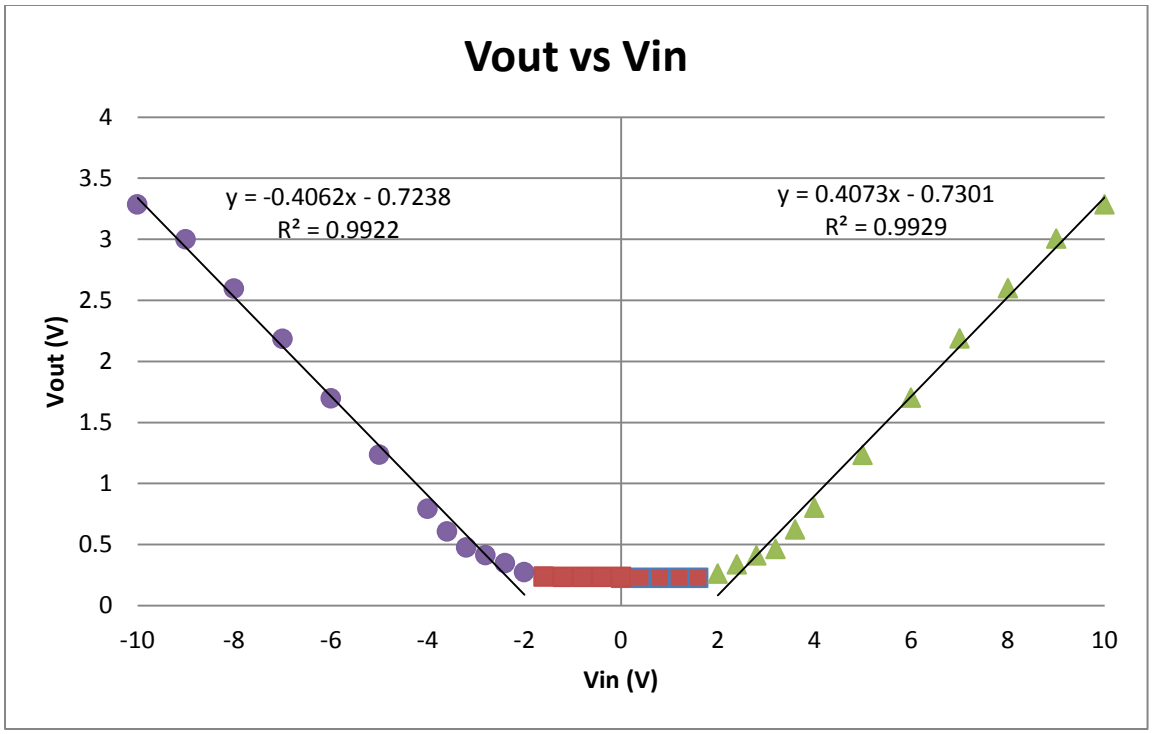


Figure 4.13: Final Design Transfer Characteristics for DC Test. A DC voltage varying between -10 V and 10 V drives the full design and the graph plots the differential output voltage, $V_{OUT}$. Purple – Negative input voltage, Red – Deadzone, Green – Positive input voltage.

With success using DC inputs to the measurement system, a time-varying input signal is applied. Figure 4.14 displays the system analog response of a 0-10 V, 1 kHz square wave. A square wave contains high frequency content on its rising and falling edges and allows better analysis of the systems limitations. As expected, the system converts the 0-10 V square wave to a 0-3.150 V square wave. This confirms functionality to convert a signal to voltage range the ADC can read.

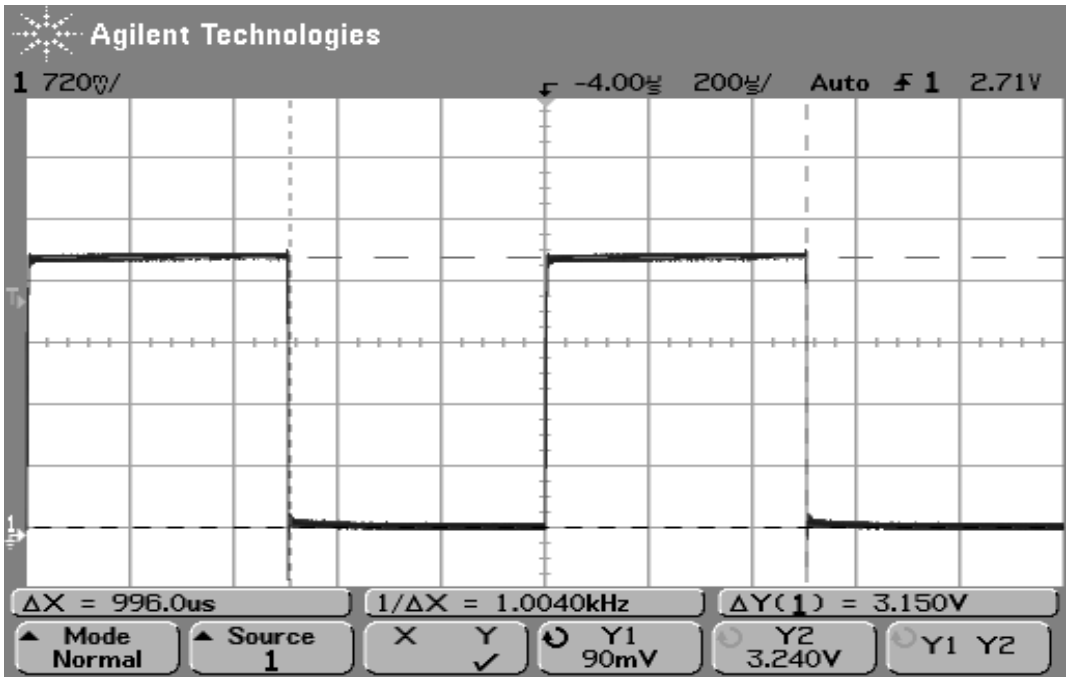


Figure 4.14: Final Design Full System Response to a 0-10V, 1 kHz Square Wave. The function generator drives a 0-10 V, 1 kHz square wave through the system and the oscilloscope measures differential output. The differential output outputs a 0-3.15V, 1 kHz square wave.

The rising edge of the system response in Figure 4.15 shows some attenuation and ripple effect for the fast switching pulse. The rising edge has a 2.5 µs rise time, limiting our bandwidth to about 400 kHz. However, when measuring a 1ms duration pulse, a 2.5 µs rise time becomes quite insignificant, as it makes up 0.25% of the pulse. There also exists a small 500 ns voltage spike at the beginning of the rising edge. Again, because of the short duration of the spike along with the fact that it does not introduce a voltage higher the peak voltage of 3.150 V, the spike becomes insignificant.

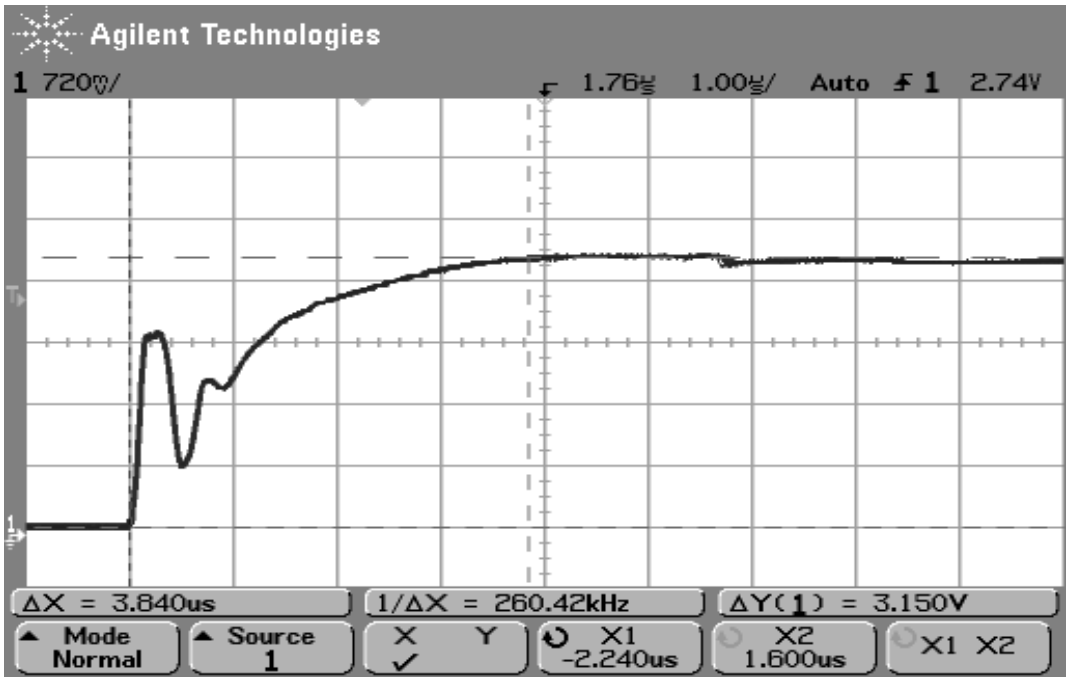


Figure 4.15: Final Design Rising Edge of Full System Response to 0-10 V, 1 kHz Square Wave. The figure shows the zoomed in rising edge of the differential output to identify any overshoot or ringing.

# 5. Analog-to-Digital Converter (ADC) and Memory

The TMS320F28335 microcontroller has an ADC and onboard memory to sample signal on the differential TIA output and store the data. The ADC reads a differential voltage and outputs a corresponding quantization level to memory. The user can then read out the data and normalize it for analysis.

## 5.1 Analog-to-Digital Converter

The ADC samples the signal at the output of the transimpedance amplifiers and stores the data in memory. The ADC has a full scale range of 0.0 V to 3.0 V. To meet the requirement of Nyquist sampling a 1 MHz signal, the ADC needs a sampling rate of at least 2 MSPS. The system uses a TMS320F28335 microcontroller containing an ADC with a 12.5 MSPS sampling rate and the ability to simultaneously sample two channels at a time or sequentially sweep up to 16 channels. The TMS320F28335 currently sweeps 2 channels at about 2 MSPS for each channel, but can sweep up to 6 channels at about 2 MSPS.

The measurement system can operate in EM harsh conditions which could corrupt data upon transmission to the computer if the system transmits data in real time. Therefore the microcontroller stores the data to onboard memory verses instant transferring of data to a remote computer.

### 5.1.1 ADC Characterization

The TMS320F288335 microcontroller contains both the ADC and memory. The microcontroller interfaces with the user with the program Code Composer Studio 5.3.0 where the user can modify and implement code.

The ADC program samples 2 channels at a rate of 2.18 MSPS. It also stores only relevant data in the acquisition window. The program begins when the user presses start. The program continuously samples the signal and stores the data into the memory buffer in a circular fashion. When storing the readings reach the end of the memory buffer, the readings begin to store at the beginning of the memory buffer. The program continues to sample and store data in this circular fashion until it detects the rising edge of the pulse. Once the program detects the rising edge, the program takes continues to take samples until the memory loops and reaches the point in memory where it began to detect relevant data. The microcontroller contains a limited amount of memory and this detection process ensures the storage of only the most relevant data. Appendix A shows the code for the described pulse sampling method.

To characterize the ADC, channels 1 and 2 sample a 2.8 V square wave of 10 kHz with 50% duty cycle produced by a function generator. Each channel of the ADC detects and captures one pulse of the square wave and Equation 5.1 calculates the sampling rate from the sampled data.

$$Sampling\ Rate = 2 \times (\#\ high\ points) \times frequency \tag{5.1}$$

The data in Figure 5.1 shows the pulse contains 109 samples and using Equation 5.1,

$$Sampling\ Rate = 2 \times (\#\ high\ points) \times frequency$$

$$= 2 \times 109\ points \times 10kHz = 2.18\ MSPS$$

the ADC samples at a rate of 2.18 MSPS.

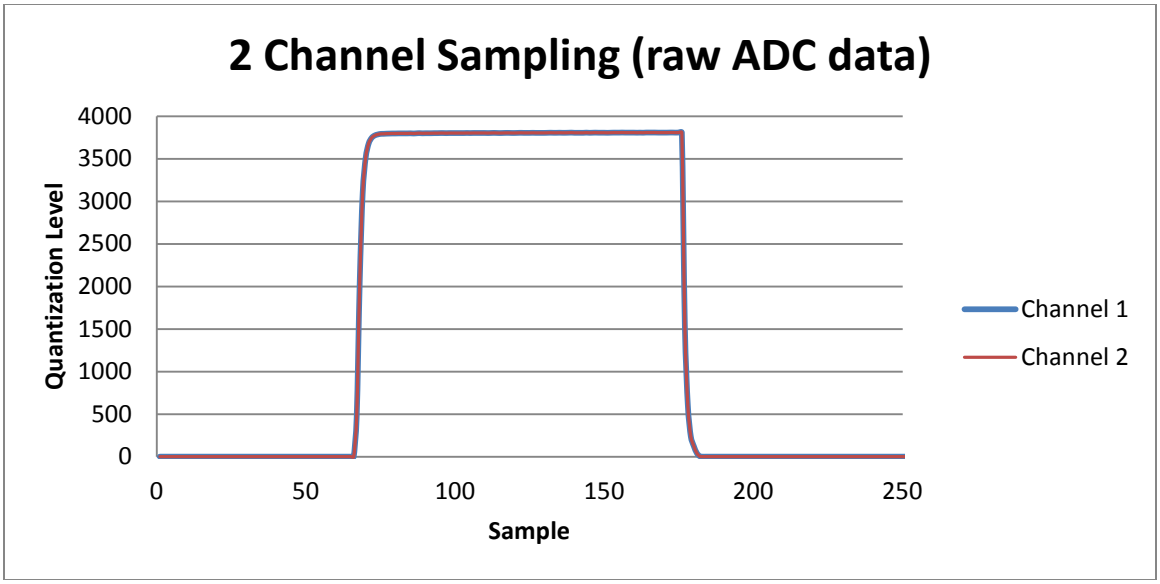


Figure 5.1: Channel 1 and Channel 2 Pulse Sampling. Channel 1 and Channel 2 both sample a 2.8 V, 10 KHz square wave. For one pulse, the channels output 109 points at a quantization level of about 3806. The channels appear directly on top of one another.

## 5.2 Memory

To meet the requirement of measuring a 1 ms pulse, microcontroller must provide a sufficient amount of memory to store enough samples required for the duration of the pulse. Using a 2.18 MSPS sampling rate for the ADC, Equation 5.2 calculates the size of the memory.

$$Memory\ Size = (pulse\ duration)x(ADC\ sampling\ rate) \tag{5.2}$$

$$= 1ms\ x\ 2MSPS = 2180\ readings$$

### 5.2.1 Memory Characterization

The ADC uses the Direct Memory Access (DMA) module to transfer data from the ADC to the on board memory of the microcontroller. As seen in Figure 5.2, the microcontroller has four blocks of 4 K x 16 memory at addresses 0x00C000, 0x00D000, 0x00E000, and 0x00F000. The microcontroller does not permit the user to create a memory buffer larger than the memory block. Therefore, two memory buffers of 3000

elements are created in L4 SARAM and L5 SARAM, one to store data from Channel 1 and one to store data from Channel 2.

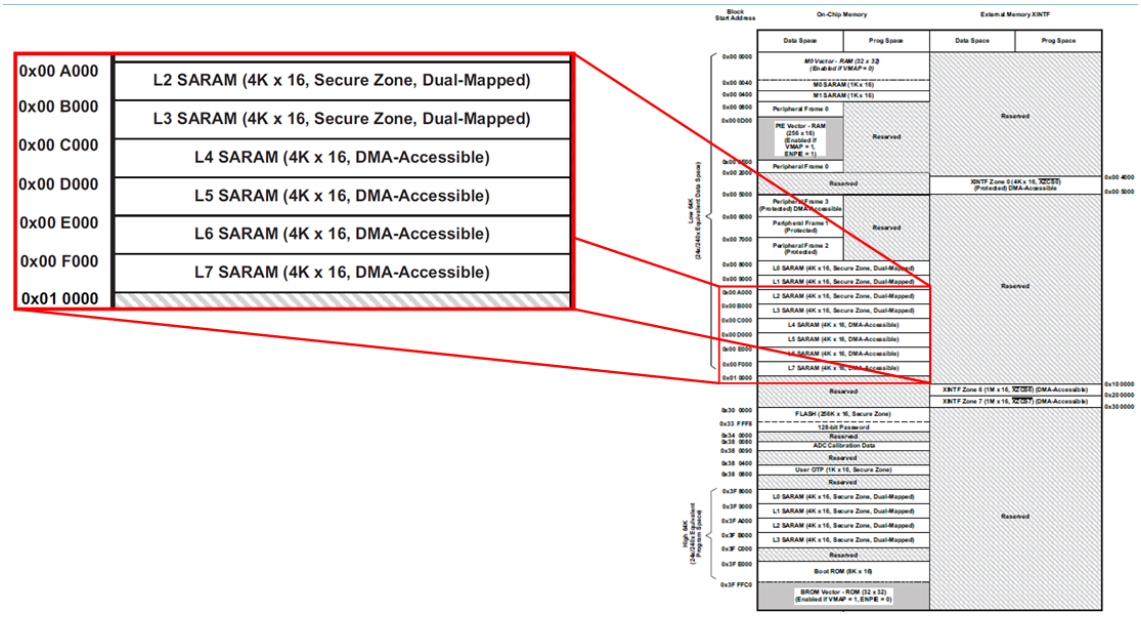


Figure 5.2: Microcontroller Memory Map. The microcontroller allows the user to store data in the four DMA-Accessible memory blocks, L4, L5, L6, and L7. The program used stores 3000 readings from Channel 1 into L4 and 3000 readings from Channel 2 into L5.

By default, the memory contains random values ranging from -32768 to 32767. As seen in Figure 5.3, the memory buffer for Channel 1 goes up to 3000 and then the rest of the block through element 4096 contains random values. The memory buffer for Channel 2 begins at 4097 and again, after 3000 more elements the memory block contains random values through element 8192.

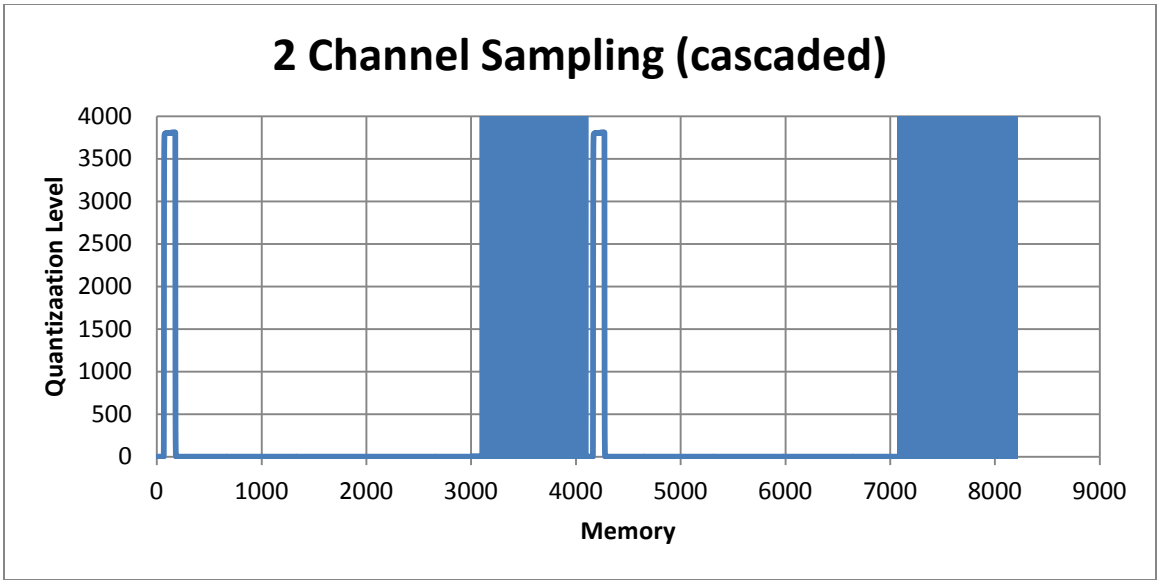


Figure 5.3: ADC Characterization Data as Seen in Memory of the Microprocessor. The plot shows data from Channel 1 and Channel 2 in memory blocks L4 and L5. The first 4096 elements plot memory block L4 and the next 4096 elements plot memory block L5. The memory blocks originally contain random values from -32768 to 32767. Because the program only initializes the first 3100 elements of each block, the seemingly solid blocks shown in the plot consist of these random values.

Additionally, Code Composer only allows the user to export data by specifying the beginning address of the desired data and the number of elements after that address. In this case, the beginning address of 0x00C000 and the 8192 elements following is exported. This exports memory blocks L4 and L5 that contain Channel 1 and Channel 2 ADC data. Because of this data export setup, the default random data elements at the end of each memory block must also be exported. Code Composer writes the list of elements into a user specified text file; where the user can copy and paste the values into excel for interpretation and analysis. From there, an Excel spreadsheet plots only the memory buffers where relevant data is contained.

## 5.3 Data Analysis

The ADC outputs data based on quantization level. A 12 bit ADC has 4096 quantization levels to represent the input voltage of the measurement system. The Excel spreadsheet then uses Equation 5.3 to convert the data to respective voltages to analyze the data in a more meaningful manner.

$$Sample\ Voltage = \frac{(Quantization\ Level)}{4096} \times (Peak\ Voltage) \tag{5.3}$$

The Peak Voltage equals the designed maximum voltage the system, based on the front end resistors. During characterization, the Peak Voltage of the input equals 3.0 V.

Lastly, each sample is given a corresponding time at which each sample occurred. Taking the inverse of the sampling rate of the ADC calculates the amount of time between each sample.

$$Seconds\ per\ sample = \frac{1}{Sampling\ Rate} = \frac{1}{2.18MSPS} = 458.72\ ns \tag{5.4}$$

For Channel 1 data, the first sample occurs at time 0secs and each consecutive sample occurs at about 458.72 ns later than the previous sample. The same amount of time separates but the first sample occurs at about time 229.36 ns, half the amount of time between each sample. The ADC samples the two channels sequentially and not simultaneously, causing this delay for Channel 2. Sequential sampling allows oversampling of the same node if desired by connecting multiple channels to the same node. However, the data will need to be graphed appropriately in Excel. The normalized data in Figure 5.4 shows accuracy and precision of the ADC with a measured peak voltage of 2.79 V and pulse duration of 49.998μs, a 0.36% and 0.004% error.

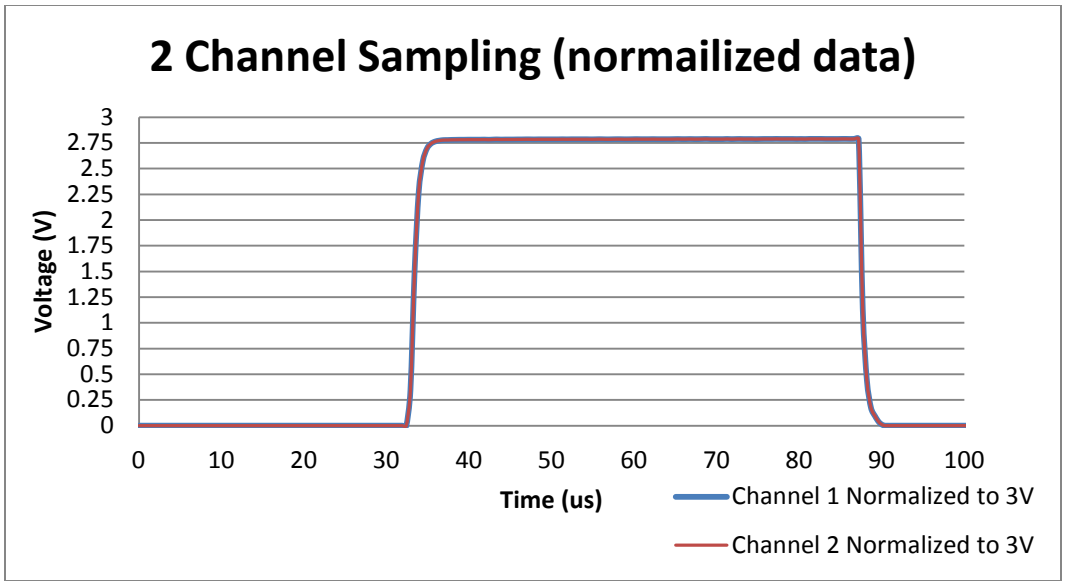


Figure 5.4: Normalized Characterization ADC Data. The ADC samples a 2.8 V peak pulse with duration of 50 µs. After normalization, the data shows a 2.79 V peak pulse with duration 49.998 µs.

## 6. Final Design Part Summary

| PART | COST | PARAMETER | REQUIREMENTS | DESIGN |
|---|---|---|---|---|
| Front End Resistors | $4.45 (each) | Resistance (kΩ) | 6.2 | 7.5 |
| | | Maximum Power (W) | 10 | 25 |
| Full Bridge Rectifier ZXSBMR16PT8 | $1.73 | Maximum Current (mA) | 40 | 400 |
| | | Reverse Recovery Time (ns) | 1000 | 3.0 |
| Optocoupler HCNR200 | $4.27 | Bandwidth (MHz) | 1.0 | 1.5 |
| Operational Amplifier LT6221 | $3.72 | Bandwidth (MHz) | 1.0 | 3.93 |
| | | Supply Voltage (V) | 3.0 | 3.0 |
| ADC | $99.00 | Sampling Rate (MSPS) | 2.0 | 2.0 |
| | | Supply Voltage (V) | 3.0 | 3.0 |
| Memory | | Size (readings) | 2000 | 3000 |
| Total Cost | $113.17+tax | | | |

Table 1: Final Design Part Summary. States cost, minimum requirements for specific part parameters, and the parameters of the parts implemented in the final design. A single channel system costs a total of $113.17+tax.

Table 1 summarizes the parts used in the final design. All of the parts satisfy the minimum requirements with some head room. The system costs a total of $113.17+tax, far less than the thousands of dollars for a commercial instrument to measure high voltage pulses.

# 7. Full System Pulse Testing

A high voltage pulse test allows analysis of the measurement system's accuracy, linearity, and speed. A function generator capable of outputting a high voltage pulse is not available. However, a 125 V DC source is available and used to create a high voltage pulse via a tri-state HV inverter for testing. Unfortunately, this means the test pulse has a maximum peak voltage of 125 V and a true 500 V pulse cannot be tested.

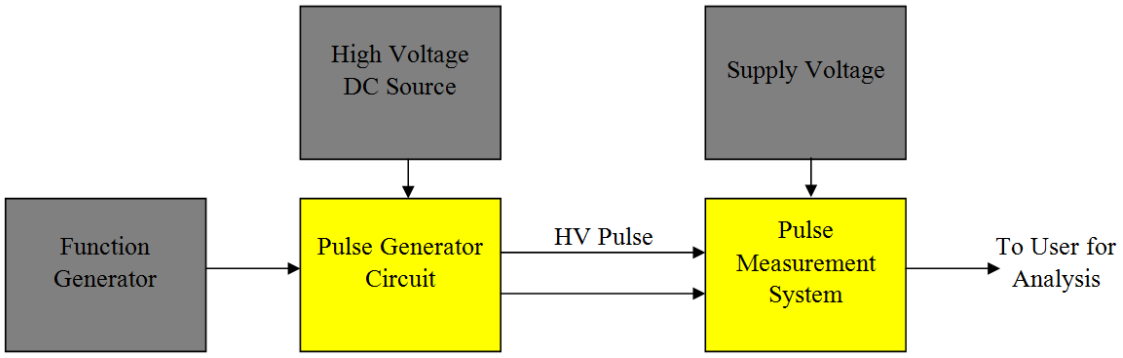


Figure 7.1: Test System Block Diagram. To test the pulse measurement system, a pulse generator inputs a high voltage pulse and the resulting data shows the accuracy of the system. The high voltage DC source and function generator operate the pulse generator.

## 7.1 High Voltage Positive Pulse Source

In order to implement a high voltage test, a circuit is designed to create a high voltage pulse using a high voltage DC source, a function generator, PMOS transistor, NMOS transistor, resistor, and capacitor, shown in Figure 7.2. The 15 kΩ load resistor emulates the input resistance of the measurement network, derived from the two 7.5 kΩ front end resistors in series, and the output is the voltage across this resistor.

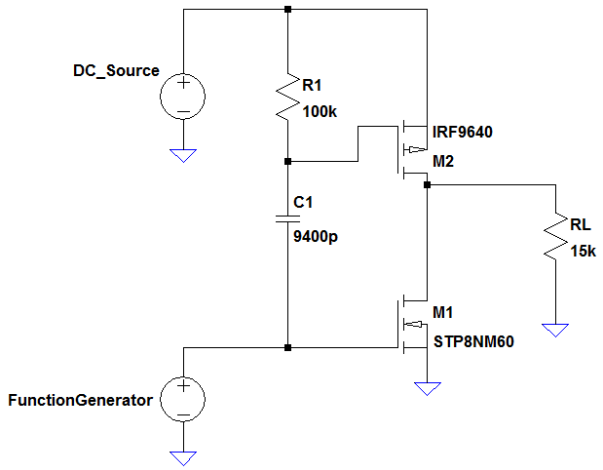


Figure 7.2: Positive Pulse Source Schematic. The circuit generates pulses using a DC source, function generator, a PMOS and NMOS transistors, a 100 kΩ resistor, and 9400 pF capacitor. The DC source defines the peak voltage of the generated pulse and the value of the resistor and capacitor define the pulse duration.

The source design above creates pulses at a frequency of the function generator, a peak voltage of the DC source, and pulse width determined by the resistor and capacitor. Both transistors have high drain-source voltages and relatively high gate-source voltages to prevent undesired switching in a high voltage environment. Additionally, the PMOS transistor needs to have a maximum drain-source current of at least 40 mA, the maximum input current of the optocoupler and thus the measurement system. The resistor and capacitor are chosen iteratively by simulating different values using LTspice.

Crowbar conditions should be kept in mind when changing the resistor and capacitor values to create different pulse widths. If the time constant, determined by resistor and capacitor, becomes comparable to the period of the function generator, the circuit becomes a crowbar circuit. If a crowbar circuit occurs, the PMOS does not turn off before the NMOS turns on, creating a direct path from the high voltage DC source to ground. A large amount of power dissipated through the devices occurs, resulting in terminal damage.

| Component | Parameters |
|---|---|
| DC Source | DC Voltage Max : 125 V |
| Function Generator | Wave Type: Square<br>Frequency: 1 kHz<br>Amplitude: 5 V<br>Offset: 2.5V |
| PMOS | Drain-Source Voltage, $V_{DSS}$: -500 V<br>Drain Current, $I_D$: -1.5 A<br>Gate-Source Voltage, $V_{GSS}$: ± 30 V<br>Gate Threshold Voltage, $V_{GS(th)}$: -5.0 V<br>Input Capacitance: 270 pF |
| NMOS | Drain-Source Voltage, $V_{DSS}$: 600V<br>Drain Current, $I_D$: 1A<br>Gate-Source Voltage, $V_{GSS}$: ± 30V<br>Gate Threshold Voltage, $V_{GS(th)}$: 4.0 V<br>Input Capacitance: 130 pF |
| Resistor | Resistance: 100 kΩ |
| Capacitor | Capacitance: 9400 pF |

Table 2: Pulse Source Circuit Components and Parameters.

### 7.1.1 Positive Pulse Simulation

Figure 7.3 shows the simulations of the positive pulse source. When the function generator initially sits in a low state of 0 V, the NMOS and PMOS do not conduct and the voltage across the capacitor holds at the DC source voltage. When the function generator switches to a high state $V_H$, the NMOS turns on and the PMOS gate voltage increases to $V_{DC}+V_H$. The capacitor discharges to the difference of the DC source and function generator, $V_{DC}-V_H$ and therefore brings the PMOS gate back to $V_{DC}$. Because the PMOS gate always has a higher voltage than the source voltage, the PMOS does not turn on yet. On the falling edge of the function generator, the NMOS turns off. The PMOS gate drops to $V_{DC}-V_H$ and because the PMOS gate now has less voltage than the PMOS source voltage $V_{DC}$, the PMOS conducts. With the NMOS in an off state, the output drives up to the $V_{DC}$ and all of the current flows to the load, the measurement system in this case. During the low state, the capacitor now begins to charge back up to $V_{DC}$. When the

capacitor increases the PMOS gate voltage enough to make the PMOS gate-source voltage greater than the PMOS gate threshold voltage, the PMOS turns off and current stops flowing to the load. A pulse with the duration of when the PMOS turned on and then off, and a peak voltage of the DC source results at the output.

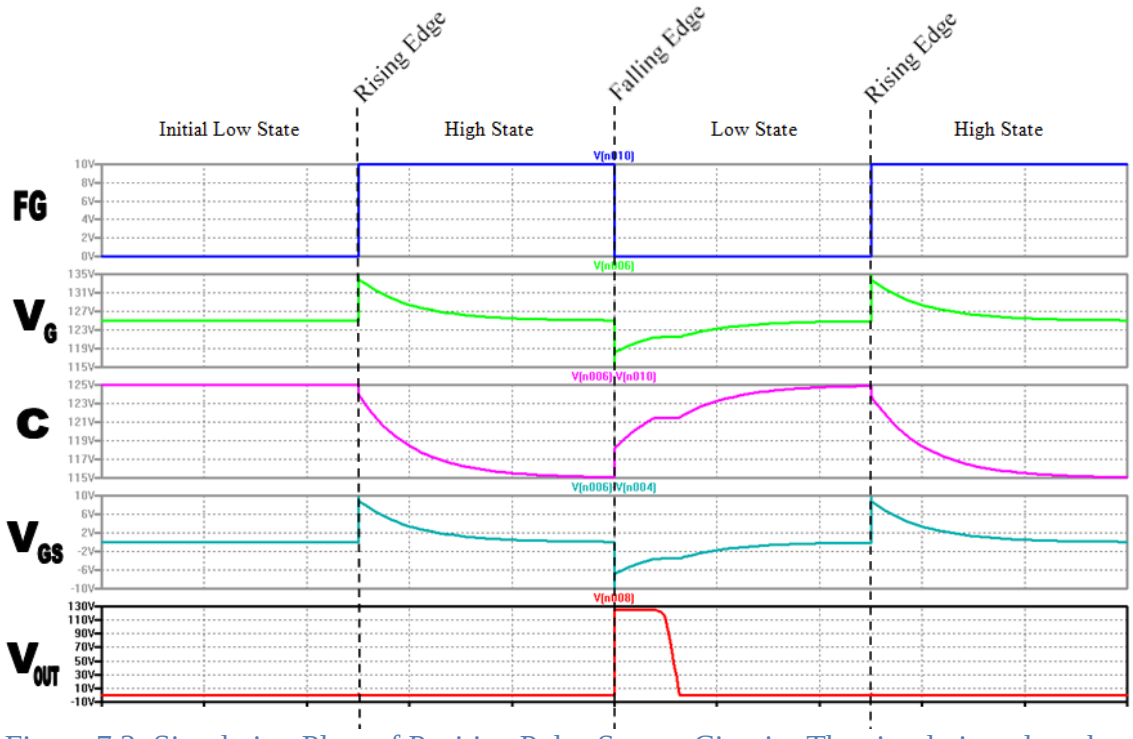


Figure 7.3: Simulation Plots of Positive Pulse Source Circuit. The simulation plots the PMOS gate voltage, capacitor voltage, the NMOS gate-source voltage, and the output voltage in response to the function generator's square wave.

### 7.1.2 Positive Pulse Test

The pulse source circuit first goes through a test to ensure functionality. All components have the values shown in Table 2 and the DC source has a voltage of 30 V. Figure 7.4 displays the function generator output on Channel 1 (yellow) and the PMOS gate voltage on Channel 2 (blue). The PMOS gate voltage behaves similarly to that of the simulations of Figure 7.3. The gate voltage centers around the DC source of 30 V,

jumps in voltage on the rising edge of the function generator, discharges toward 30 V during the high state, drops in voltage on the falling edge, and charges toward 30 V during the low state.

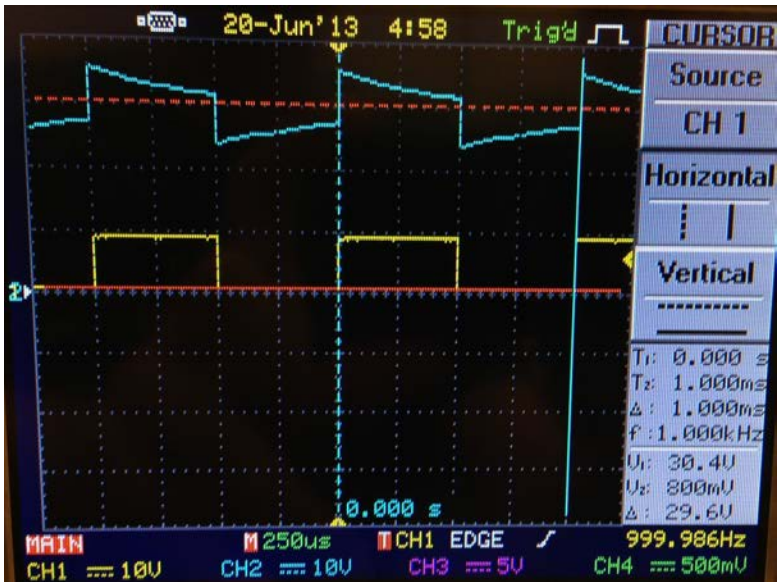


Figure 7.4: Function Generator (Channel 1: yellow) and PMOS Gate Voltage (Channel 2: blue) Plot for 30V Pulse Source. The rising edge of the function generator causes the PMOS gate voltage to jump in voltage and discharge towards the DC source voltage of 30V through the capacitor. The falling edge of the function generator causes the PMOS gate voltage to drop in voltage and charge towards the DC source voltage of 30V through the capacitor.

When the DC source increases to 50 V, the PMOS gate voltage behaves the same as seen in Figure 7.5.

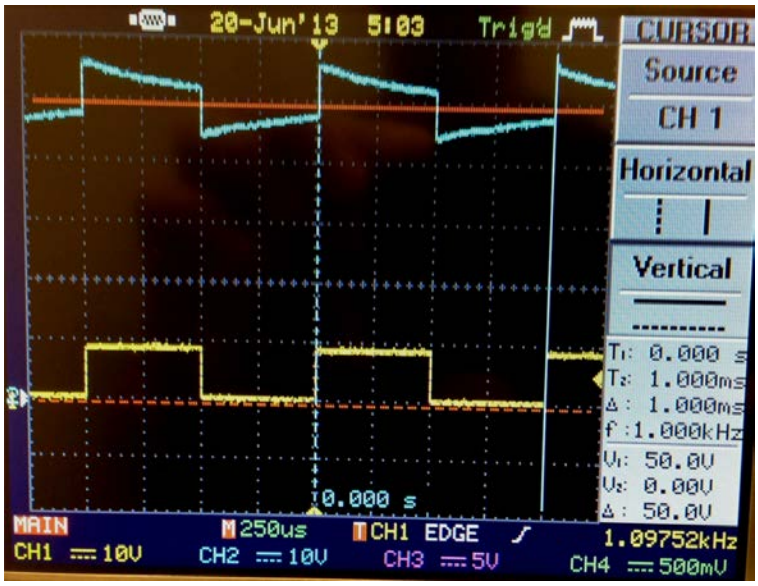


Figure 7.5: Function Generator (Channel 1: yellow) and PMOS Gate Voltage (Channel 2: blue) for 50 V Pulse Source. The rising edge of the function generator causes the PMOS gate voltage to jump in voltage and discharge towards the DC source voltage of 50 V through the capacitor. The falling edge of the function generator causes the PMOS gate voltage to drop in voltage and charge towards the DC source voltage of 50 V through the capacitor.

Channel 1 switches to measure the output of the pulse source circuit and displayed in Figure 7.6. As expected, the pulse occurs when the PMOS gate voltage drops, and thus on the falling edge of the function generator as well. The pulse reaches a peak voltage equal to the DC source, 50 V, and has a pulse width of about 250 μs

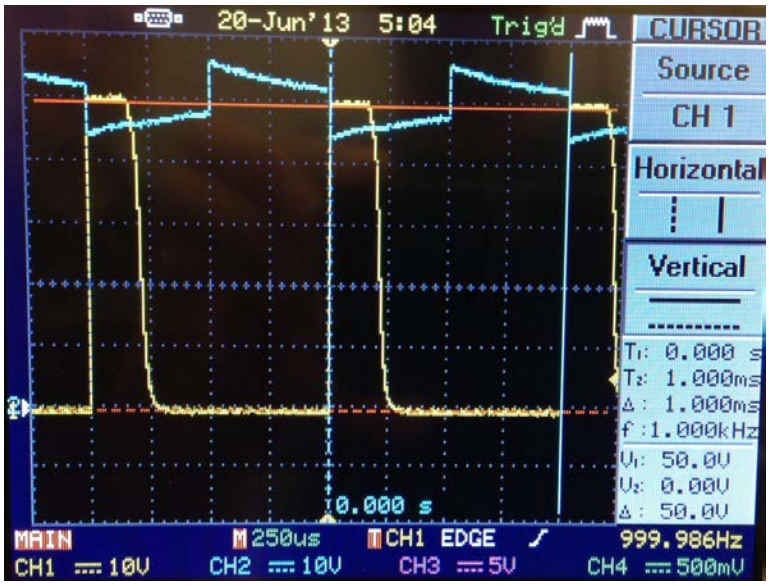


Figure 7.6: Output Voltage (Channel 1: yellow) and PMOS Gate (Channel 2: blue) of 50 V Pulse Source. When the PMOS gate voltage drops, the PMOS conducts and circuit outputs DC source voltage of 50 V. The PMOS gate voltage rises as the capacitor charges. When the gate voltage reaches the forward voltage of the PMOS, the PMOS stops conducting and the output drops to 0 V.

The DC source then increases to 125 V and Figure 7.7 displays the resulting pulse. The pulse has a peak voltage of 125 V and a pulse width of 250 µs.

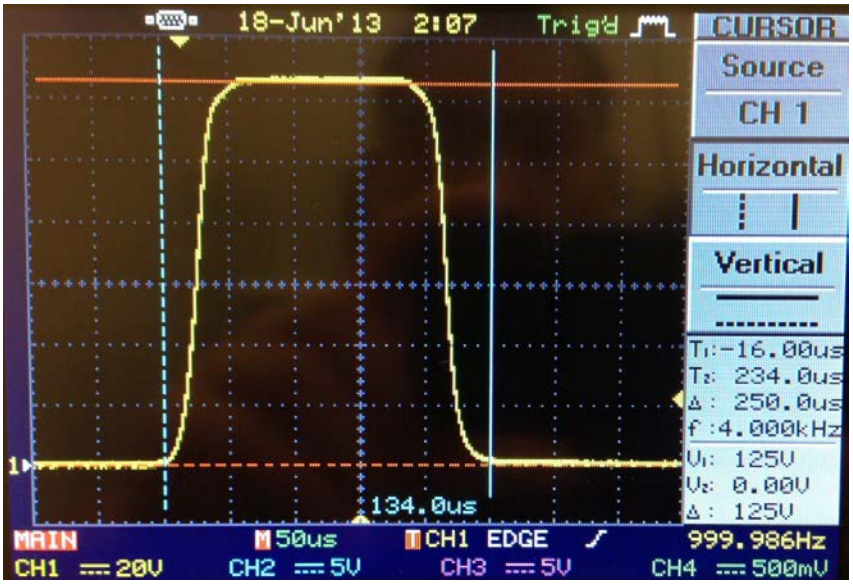


Figure 7.7: 125 V Pulse with Pulse Width of 250 µs Generated by Positive Pulse Source.

This waveform drives through the full system and ADC samples and collects data. Throughout pulse testing, only Channel 1 is active because only one measurement channel was constructed. Figure 7.8 shows the raw data of the ADC, displaying the data as quantization level versus sample number.

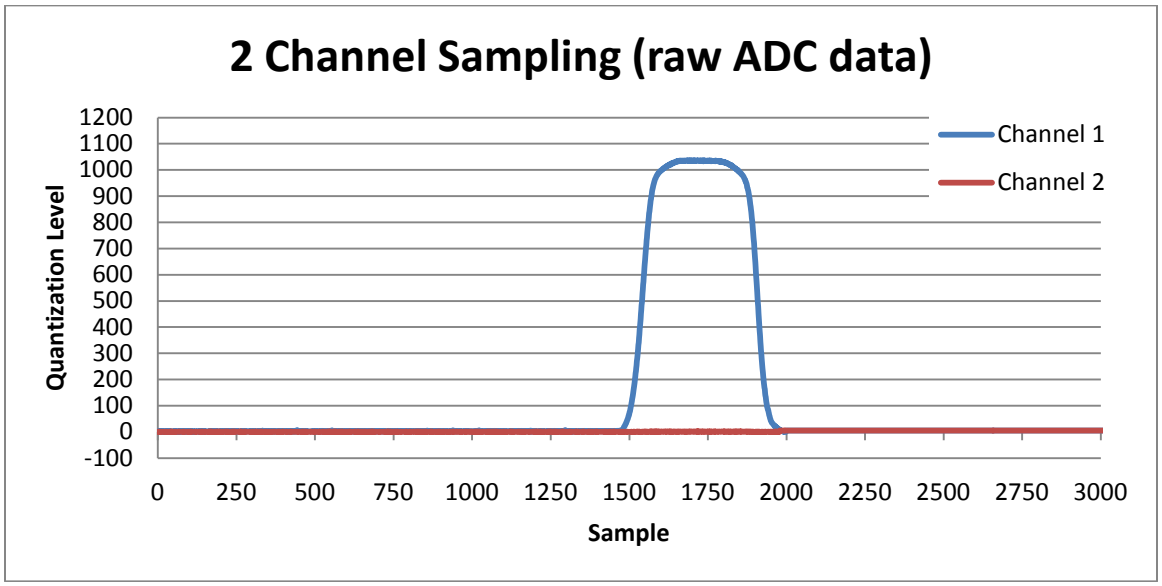


Figure 7.8: 125 V Positive Pulse Raw ADC Data. The pulse lasts for 538 samples and has a peak quantization level of 1036.

Figure 7.9 shows the data normalized to the respective voltage versus time. To normalize the data, the maximum source voltage the measurement system can handle must first be calculated. This value produces 3 V on the output of the dual TIA and, therefore, corresponds to quantization level 4096 of the ADC. Solving for $V_S$ in Equation 3.10 calculates the maximum source voltage of the measurement system.

$$R_S = \frac{V_s - 2V_D - V_{LED}}{2I_{LED}} \Rightarrow V_S = 2I_{LED}R_S + 2V_D + V_{LED} \tag{6.1}$$

Again, optocoupler has a maximum input $I_{LED}$ of 40mA, the chosen front end resistor has a value of 7.5 kΩ, each diode in the full bridge rectifier has a voltage drop of 305 mV,

and optocoupler's LED has voltage drop of 1.6 V. The system has a maximum source voltage of 602.2V.

$$V_S = 2(40mA)(7.5k\Omega) + 2(305mV) + 1.6V = 602.2V$$

Equation 5.3 converts the quantization levels to their respective voltages where the Peak Voltage equals 602.2 V. The blue plot in Figure 7.9 shows the converted quantization levels.

$$Sample\ Voltage = \frac{(Quantization\ Level)}{4096} \times 602.2\ V$$

Figure 7.9 displays another approach used to normalize the data represented by the green plot. The average quantization level of the flat top of the pulse has a quantization level of 1036. Normalization forces the quantization level to correspond to the sample voltage 125 V, and therefore changes the Peak Voltage the measurement system can handle. Solving for $V_S$ in Equation 5.3 calculates this.

$$Sample\ Voltage = \frac{(Quantization\ Level)}{4096} x(Peak\ Voltage)$$

$$\Rightarrow Peak\ Voltage = \frac{4096}{(Quantization\ Level)} x(Sample\ Voltage) \quad (6.2)$$

$$= \frac{4096}{1036}\ x\ 125V = 494.2\ V$$

Using 494.2 V as the Peak Voltage, Equation 6.3 normalizes the rest of the data.

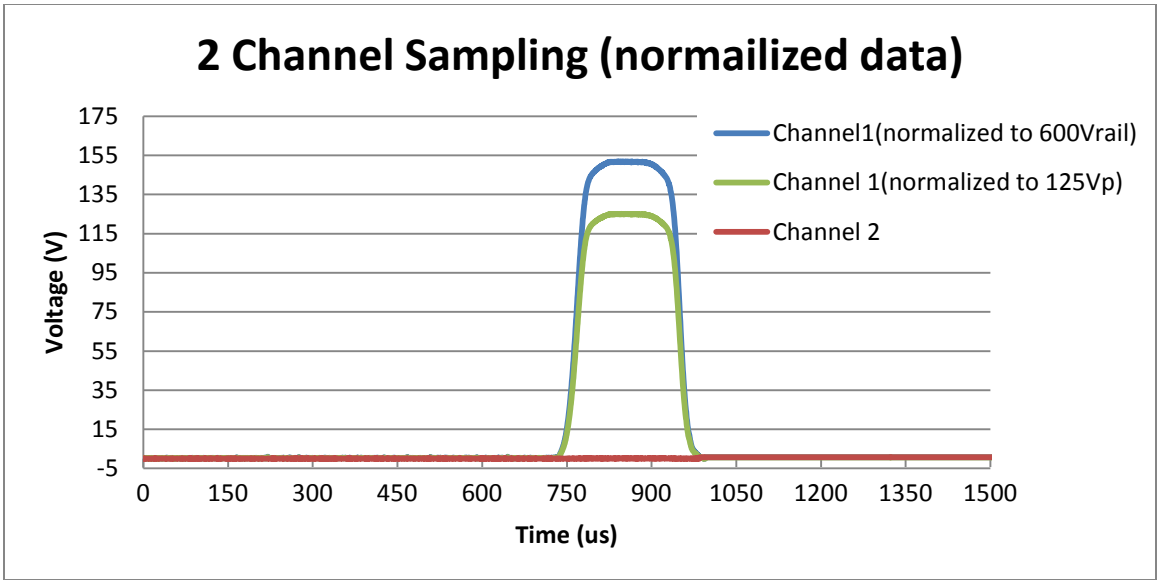


Figure 7.9: 125 V Positive Pulse Normalized ADC Data. Normalization of the data to the designed 600 V rail results in a 152 V peak pulse reading (blue). An alternative normalization can force the peak quantization to read 125 V (green).

The data also shows the pulse has a width of 247 µs, a 1.17% error from the expected 250 µs measured by the oscilloscope. User error can easily cause this pulse width error. The user has subjective judgment to where the cursors on the oscilloscope should be placed to indicate the beginning and end of the pulse and measure the actual pulse width.

## 7.2 Accuracy

The peak voltage varies across voltages between 0 V and 125 V to determine linearity. Figure 7.10 shows a very high linearity across the voltages. However, there exists an offset in the trendline suggesting error. The 1.5 V x-intercept of the trendline indicates that if a 1.5 V pulse drives the system, the ADC would read the pulse as value 0 quantization level and not detect a pulse.

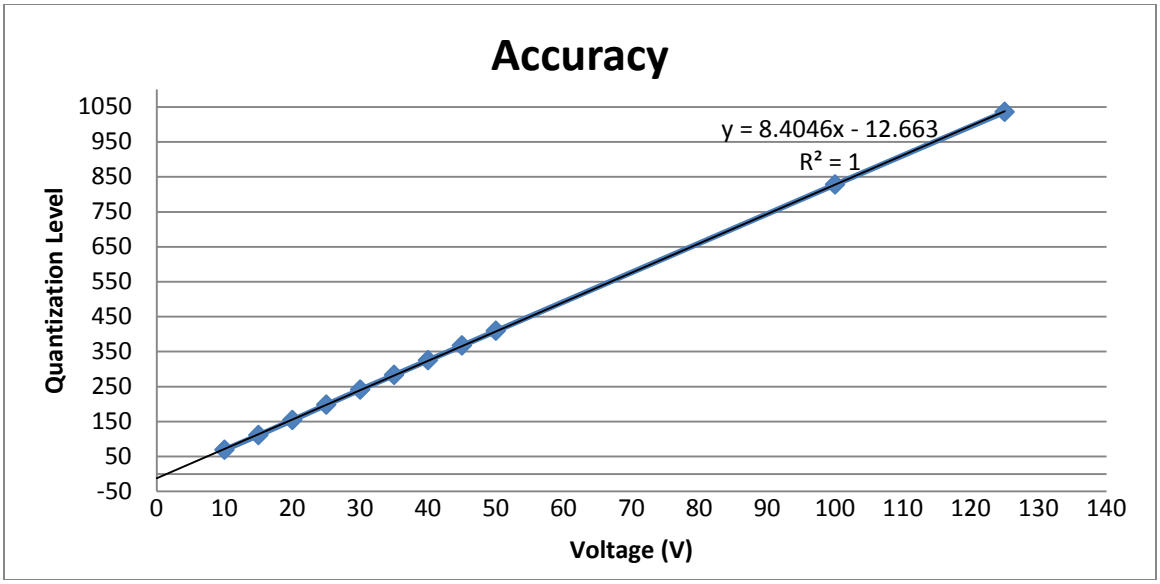


Figure 7.10: ADC Quantization Levels of Various Peak Pulse Voltages. The plot shows a strong linear relationship with an $R^2$ value of 1.

The forward voltage required to turn on all of the diodes on the front-end causes this error. The signal must turn on two Schottky diodes and an LED before the system senses any type of signal at the output. As measured previously, the Schottky diodes have a forward voltage of approximately 245 mV and the LED has a forward voltage of approximately 1.6 V, resulting in a minimum input voltage of 2.09 V to activate the system. The 1.5 V x-intercept suggests the actual sum of turn on voltages to activate the system has a value lower than the theoretical 2.3 V and closer to 1.5 V.

Figure 7.11 shows an oscilloscope capture measuring a 10V pulse driving the measurement system on Channel 2 and the voltage across one of the front-end resistors on Channel 1. Channel 2 has a vertical scale of 2 V/div and by setting Channel 1 to half of this, 1 V/div, Channel 1 acts like the voltage across both front end resistors combined on a 2 V/div scale. The difference between the 10 V pulse and the “voltage across the

two front end resistors" equals 1.84 V and according to KVL, equals the sum of the voltage drops across all of the diodes of the front end.

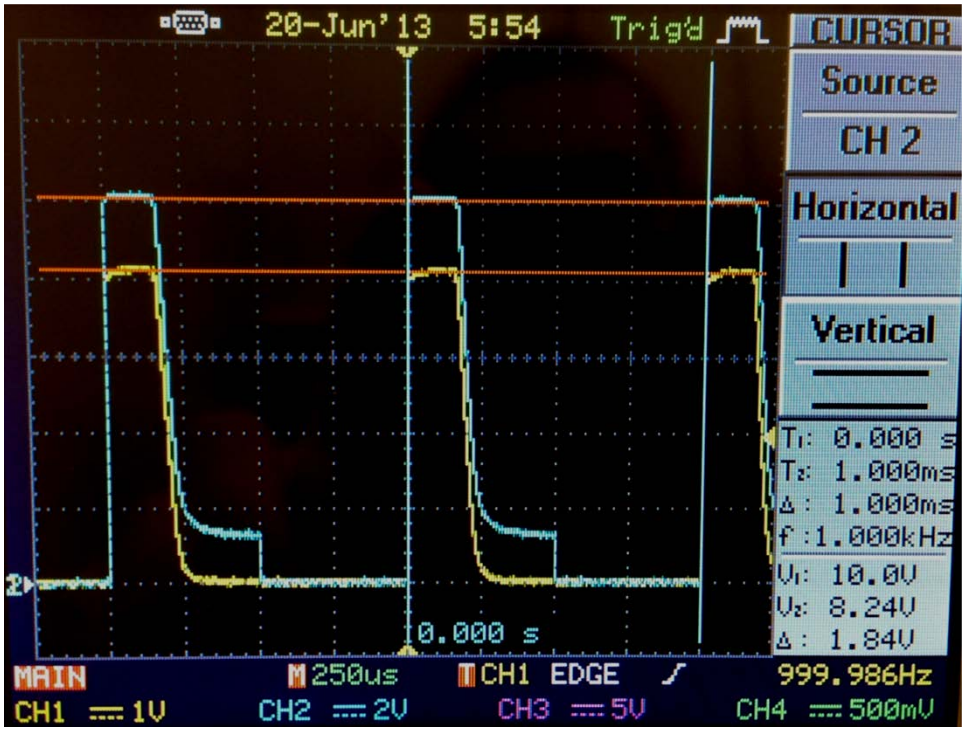


Figure 7.11: Offset Error Due to Front-End Diodes. Channel 2 measures an 10V pulse input and Channel 1 measures the voltage across one of the resistors. Channel 1 has half the vertical scale of Channel 2 to simulate the voltage drop across both resistors on a 2V vertical scale. The difference between peak voltages of the two channels represents the required turn on voltage to activate the system, 1.84V.

Figure 7.11 clearly shows the presence of the offset error exists and would cause significant error in the measurement system's readings for low voltages. However, Figure 7.10 does not make this error easily identifiable. To expose the effect of the offset error, Figure 7.12 normalizes the quantized data to 125 V and plots the percent error.

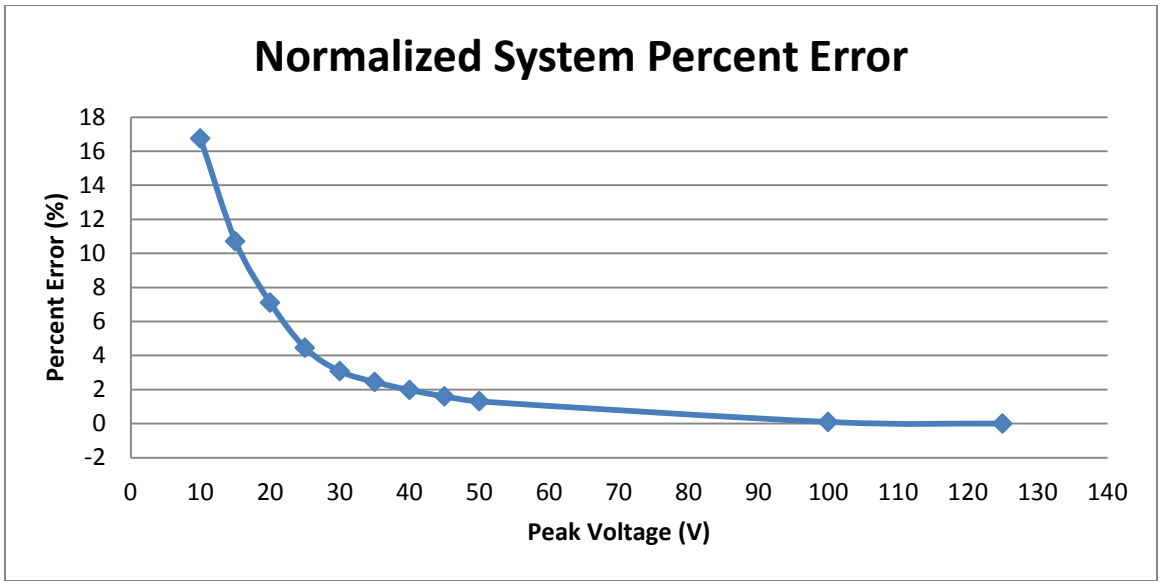


Figure 7.12: System Percent Error After Normalization of Quantization Levels to 125V Peak Pulse. The graph illustrates an exponential percent error increase as the peak voltage decreases.

The now evident offset error affects the system readings exponentially as peak voltage lowers. If the user wants less than 1% error in the readings, the measured pulse should have a peak voltage of at least 60 V.

One way to assist in correcting this offset error is to add 1.5 V to the normalized voltage. As shown in Figure 7.13, the percent error stays under 2% for voltages greater than 10 V. For even finer tuning, only add 1.5 V to normalized voltages below 60 V.

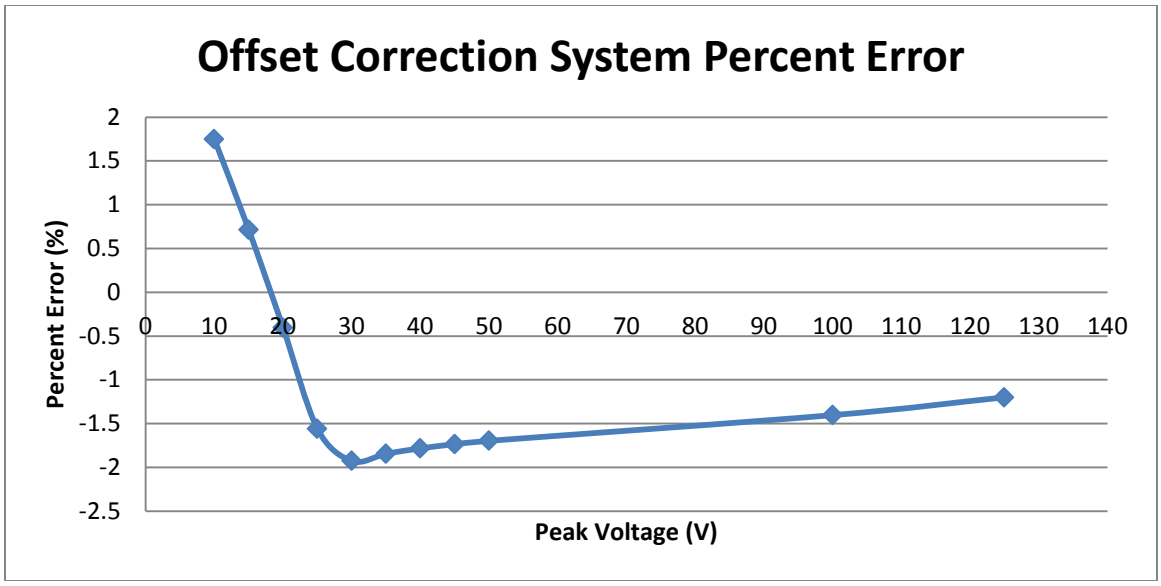


Figure 7.13: System Percent Error After Normalization of Quantization Levels to 125V Peak Pulse and 1.5V Offset Correction. The offset correction maintains the percent error under a magnitude of 2%.

## 7.3 Pulse Containing Positive and Negative (PN) Components Test

A modified pulse circuit, shown in Figure 7.14, tests the performance of the measurement system when a signal containing both positive and negative parts drives the system. Instead of connecting the negative input of the measurement system to the ground, the modified design connects the negative input to a DC offset source.

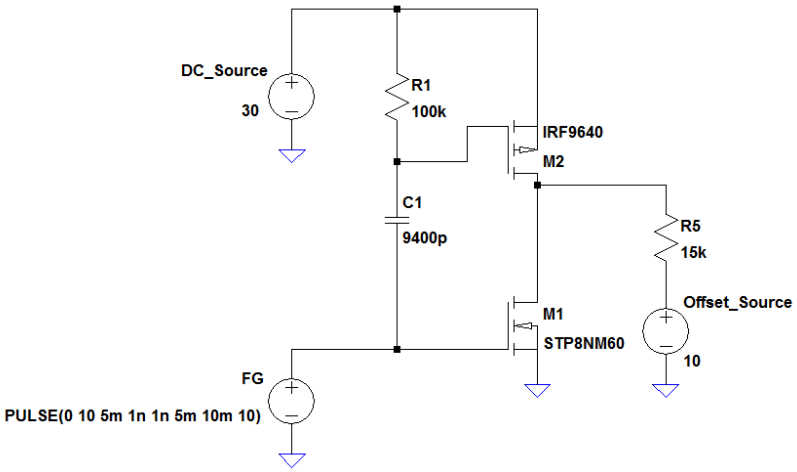


Figure 7.14: PN Pulse Source Schematic. The schematic has the same basic design as the positive pulse circuit previously, but with a 10V DC offset source on the other end of the load.

### 7.3.1 PN Pulse Simulation

Using LTspice, Figure 7.15 shows the simulation of the new pulse source. The new pulse source behaves the same as before except when the function generator is in a high state, the output does not drop down to 0 V but instead drops to the negative of the offset source voltage, $-V_{OFF}$.

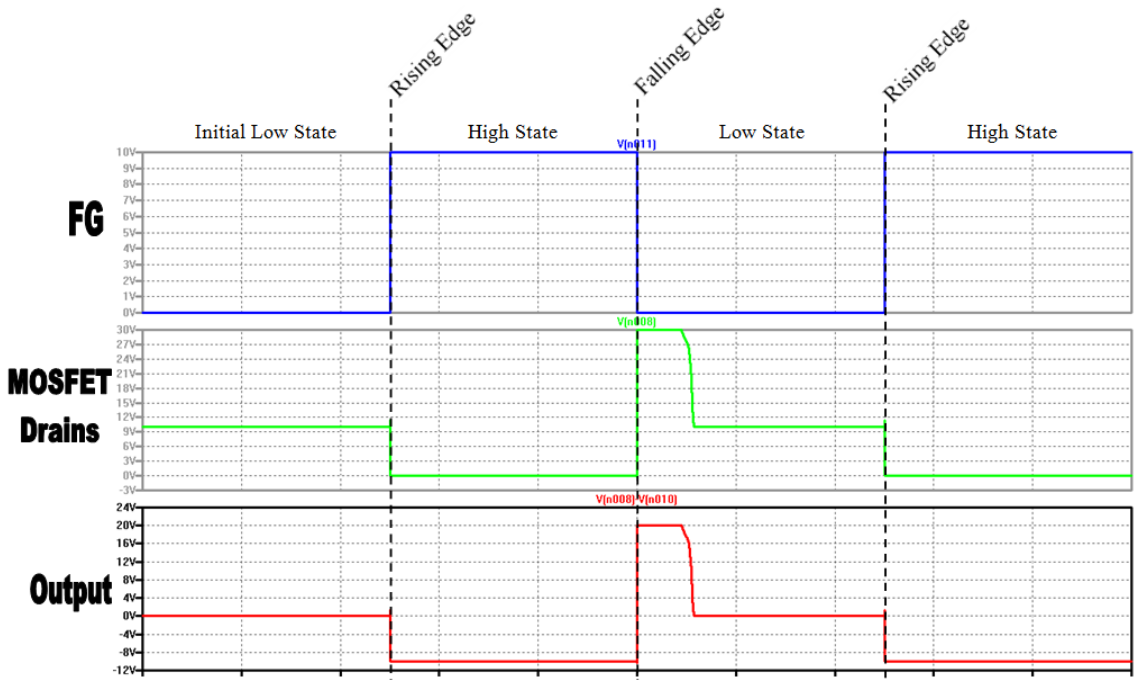


Figure 7.15: PN Bipolar Pulse Source Simulation Plots. In the initial low state of the function generator, the MOSFET drain voltages equal the DC source voltage of 10 V and the output equals 0 V. The rising edge of the function generator activates the PMOS and grounds the MOSFET drains. In result, this drives the output down to -10 V. Upon the falling edge of the function generator, the PMOS activates and creates a pulse across the output load equal to the difference of the DC source and the offset source, 20 V.

When the function generator is in its initial low state, the MOSFET drain node holds at the Offset Source voltage of 10 V. The function generator switches to a high state and activates the NMOS, thus grounding the MOSFET drain node and creating a negative voltage across the 15 kΩ resistor. Upon the arrival of the falling edge of the function generator, the NMOS turns off and the PMOS turns on, causing the MOSFET drain node to jump to the DC source voltage of 30 V. Because of the 10V on the other end of the load resistor from the Offset source, the voltage across the load resistor equals 20 V, the difference between the DC source and Offset source, $V_{DC} - V_{OFF}$. The PMOS turns off due to the capacitor charging as in the previous pulse source circuit, creating the falling edge of the pulse. With the PMOS and NMOS off, the MOSFET drain node holds

at the Offset source voltage 10 V and thus 0 V across the 15 kΩ load resistor. Again, when the function generator switches to a high state the NMOS activates, grounds the MOSFET drain node, and creates a negative voltage across the 15 kΩ load resistor.

### 7.3.2 PN Pulse Test

This pulse waveform drives the measurement system and the voltage across the LED is first measured, shown in Figure 7.16. The dip in voltage after the zero region of the pulse waveform suggests a switching delay with duration of 5.6 μs. However the voltage does not dip directly before the pulse where the pulse waveform changes from a negative to positive signal, suggesting the LED has such a small delay that makes it not observable (under these test conditions).

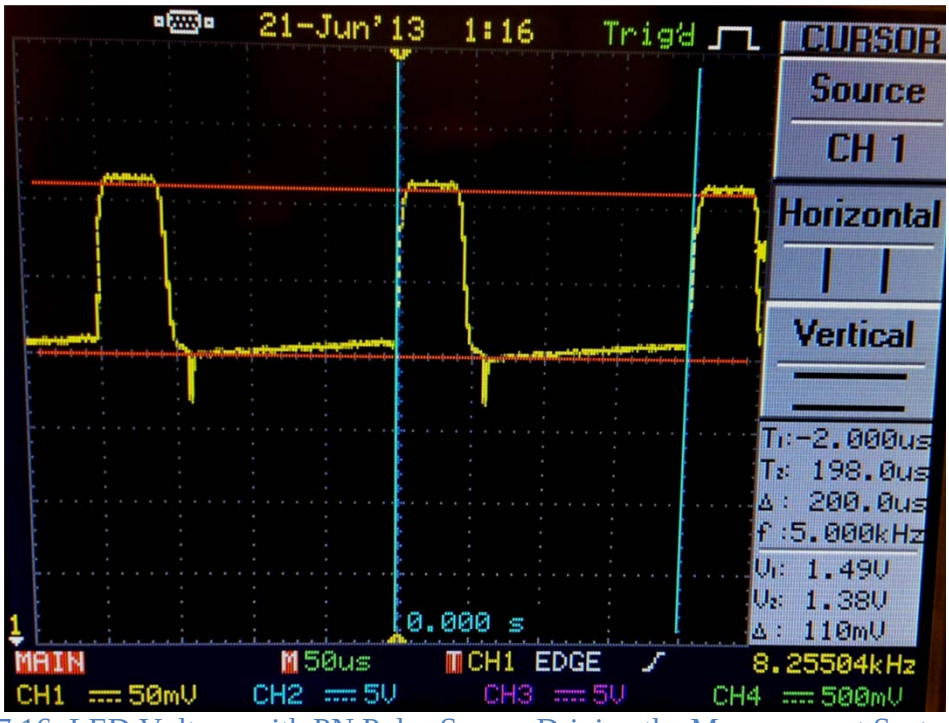


Figure 7.16: LED Voltage with PN Pulse Source Driving the Measurement System. The LED shows a dip in voltage directly after the pulse, implying a delay in the system.

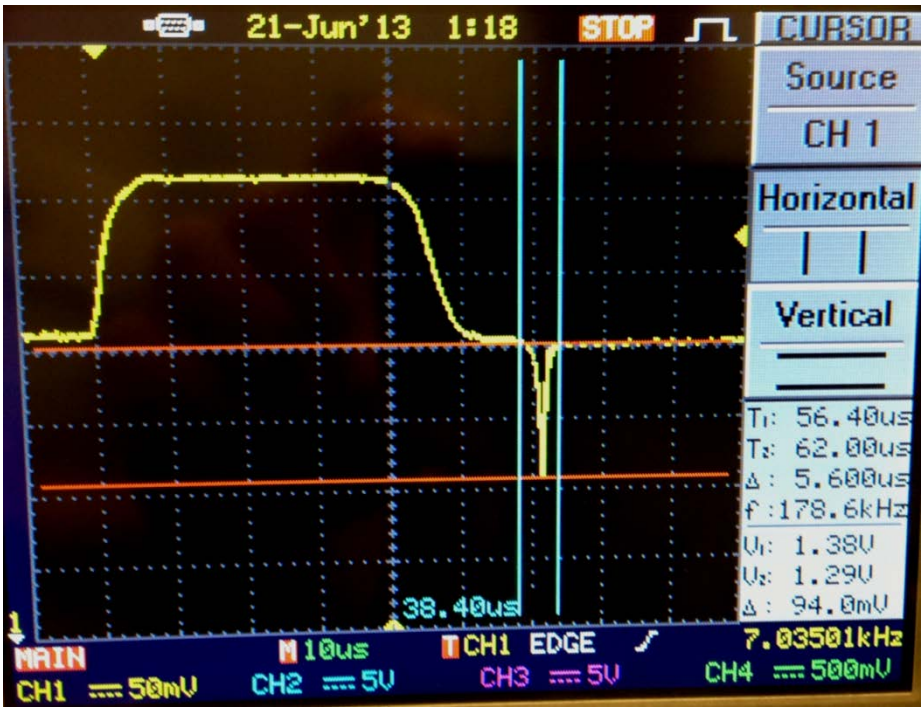


Figure 7.17: LED Voltage Zoomed When PN Pulse Source Driving the Measurement System. The delay response of the system lasts for about 5.6 µs.

One theory for the unobservable delay is the constant signal flowing through the diode to keep the LED conducting. Diodes must charge to their forward voltage to begin conducting. The LED conducts when a negative signal drives the system. When the signal increases to 0V as it enters a positive voltage, the LED "ideally" turns off and then begins conducting again when enough positive signal drives the system. However, because the signal switches from negative to positive at such a steep rate, the LED voltage begins to drop but it the positive signals picks it up before it can fully discharge.

The signal remains at 0 V in the zero region (high impedance state of the pulse generator) The dip after the zero region can be explained by the fact that the signal remains at 0 V in the zero region (high impedance state of the pulse generator), allowing the LED to discharge completely. When the signal turns negative, the LED needs time to charge back up to its forward voltage and start conducting, causing a short delay. It is

assumed the LED causes the delay and not the photodiode because it has a larger capacitance of 80 pF versus the photodiodes 22 pF.

With the same pulse waveform driving the system, the oscilloscope measures the differential output of the TIA as in Figure 7.18.

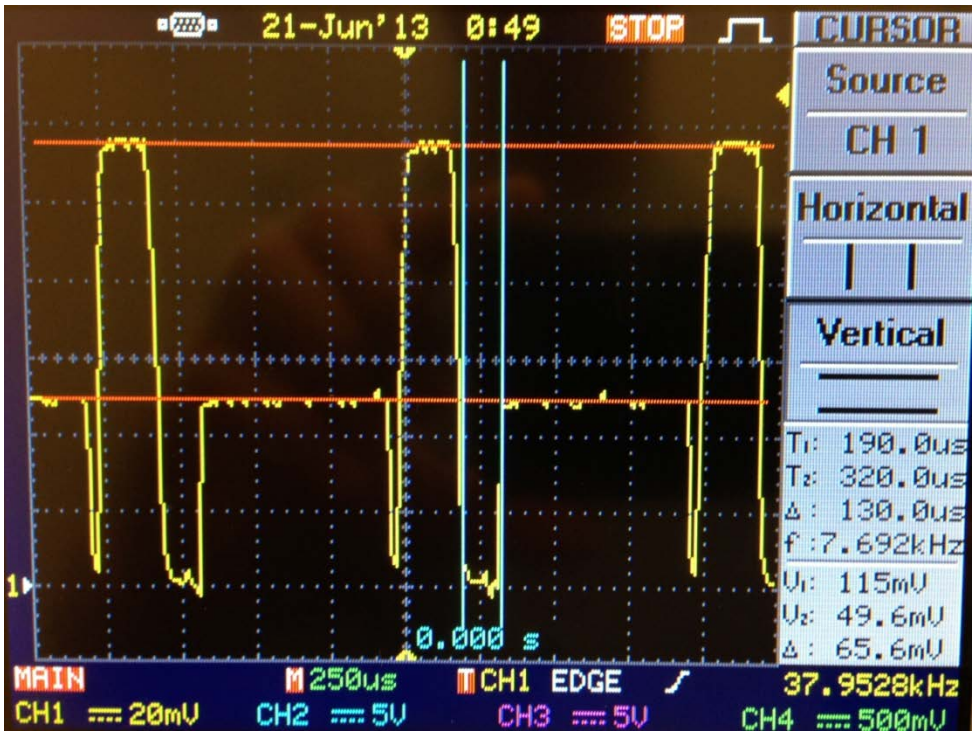


Figure 7.18: System Output When 20 V Pulse Waveform Containing Both Positive and Negative Signal Driven at Input. As expected, the system outputs the absolute value of the input signal and a peak pulse voltage of 115 mV.

The TIA differential output represents the simulated waveform well. Delays are expected when the signal switches polarities, but appear unidentifiable in the screen capture. The dip after the pulse has a zero region before switching negative and is difficult to differentiate a delay, which would be represented by a span of 0 V, from the zero region. The dip just before the pulse does not appear to even reach 0 V in the screen capture suggesting the theory before, the LED voltage is picked up before it can reach 0 V.

The pulse source is set to produce a 40 V pulse with a -10 V region and driven through the measurement system.

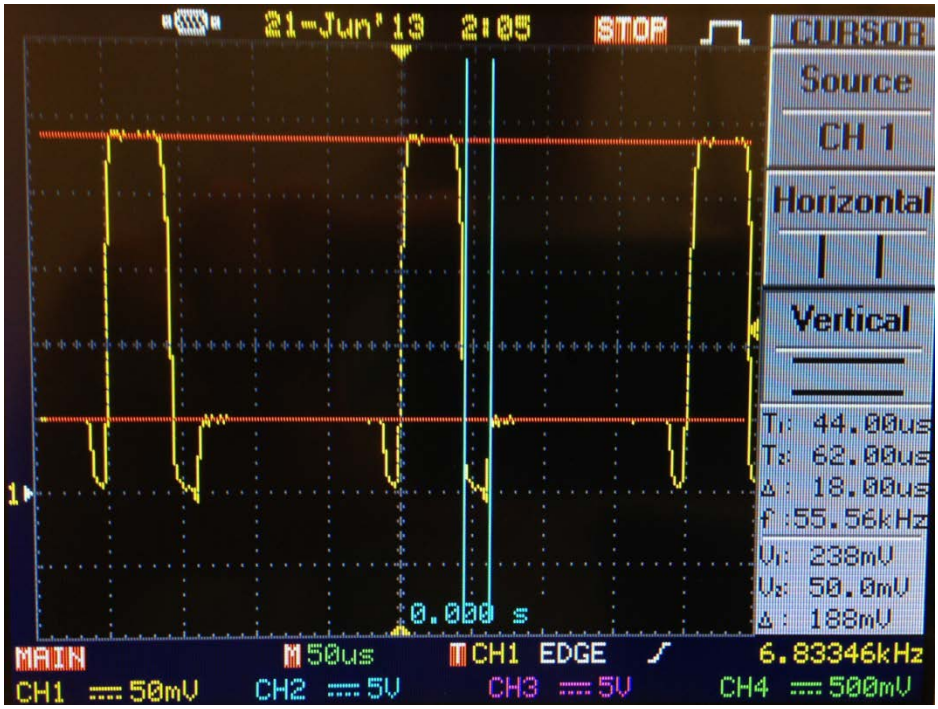


Figure 7.19: System Output with 40 V Pulse Waveform Containing Both Positive and Negative Signal Driven at Input. The system outputs the absolute value of the input signal and a peak pulse voltage of 238 mV.

Similar results occur in which the output mimics the simulations and no discernible delays occur. The ADC then samples the waveform and Excel normalizes the data, shown in Figure 7.20.

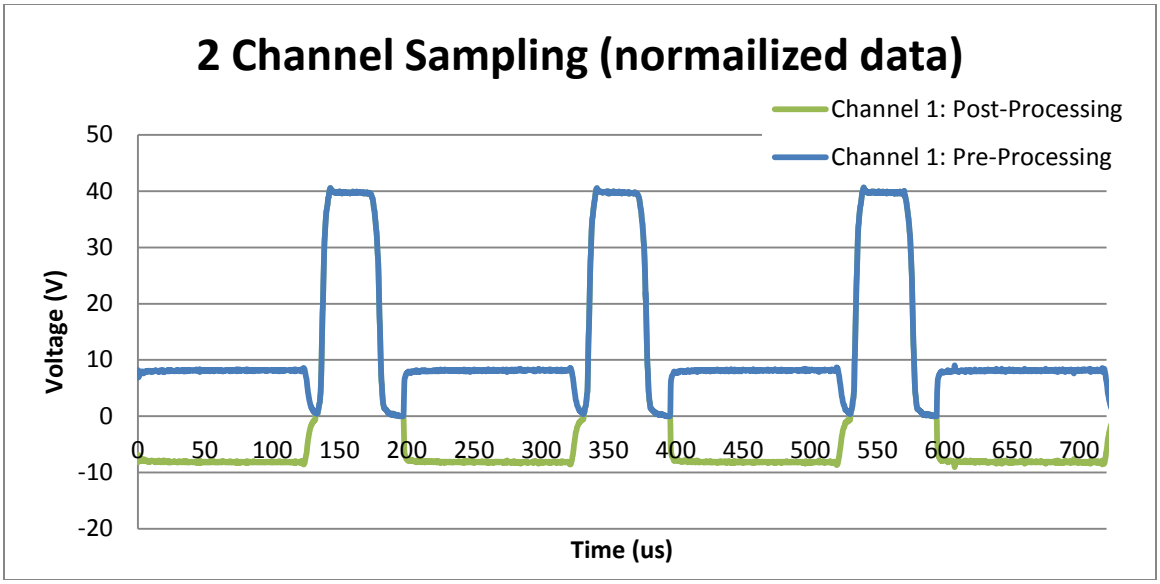


Figure 7.20: Post-processed and Pre-processed Data from PN Pulse. After normalization, the data shows a 40 V pulse. The graph also shows the data before (blue) and after (green) the data has been processed for polarity.

The ADC data samples the signal very accurately with peak voltages of 39.8 V and period of 197 µs. This data has 0.5% error in voltages and 1.5% error in time, again easily contributed to user error as it is subjective where points of measurement are located. The edge of the pulse rises at a rate of 10262 kV/s and shows the system can easily measure the Cal Poly's PFN, which rises at a rate of 3403 kV/s, without any overshoot or ringing. However, focusing on the transition from negative to positive voltage just before each pulse, a delay occurs as the data does not appear to have smooth, continuous transition across 0 V.

# 8. SUMMARY

This section summarizes the results and makes conclusions about the system's capabilities. It also provides recommendations on future work for improvements on the measurement system's performance.

## 8.1 Conclusion

The designed system has the capability to accurately measure the pulse produced by the Pulse Power Club's PFN. It has proven to measure a pulse containing voltages from -125 to +125, with the potential of peak voltages of -490 V and +490 V, and width of 250 μs at a resolution of 0.12 V. The system allows the user to adjust and optimize resolution by changing the value of the front end resistors, implying the system has the capability of measuring higher voltages. The ADC currently samples two channels at 2.18 MSPS and stores 3000 readings per channel to onboard memory, a 1.37 ms acquisition window. Altering the ADC's sampling rate allows the user to change the acquisition window and therefore increase the amount of relevant data stored. These adjustable features allow the user to tailor the measurement system for their specific applications. A 3 V supply powers the entire system to allow a battery power feature if desired. The system operates under harsh environments containing strong electrical and magnetic signals, similar to ones that pulse powered systems create.

The system does fall short on the system bandwidth requirement. The system fails to sample frequencies higher than 400 kHz, where the requirements desired 1MHz. Signals that have frequencies higher than 400 kHz will appear attenuated, verified by Figure 4.15. The figure shows an 8pF feedback capacitor results in the TIA to begin

slightly attenuating around 400 kHz. The system also fails to meet the cost requirement for a one channel system. A single channel system costs $113.17+tax, falling about $13.17 short of the $100 or less requirement. However, each additional channel would only cost $19.82. A two channel system costs $138.64, significantly reducing the per channel cost to $69.32 and now meeting the requirement. Otherwise, the system meets all of the set out requirements to measure a high voltage pulse. It provides the everyday electrical engineer a way to measure PFNs without having to spend thousands of dollars on commercial products, when most products do not even have the capabilities as the design presented in this thesis.

## 8.2 Future Work

As mentioned earlier, the system can only measure frequencies less than 400 kHz due to the TIA's bandwidth. Replacing the operational amplifiers with a higher bandwidth product could increase the system's bandwidth. If system improvements increase bandwidth higher than 1 MHz, the ADC must sample at least sample at twice the system bandwidth to fulfill the Nyquist rate. The ADC has a maximum sampling rate of 12.5 MSPS for single channel sampling, giving the system a design potential 6.25MHz bandwidth.

On the other hand, the construction of a second system allows for a two channel system. Theoretically, the ADC has the ability to simultaneously sample six channels at 2 MSPS. The tradeoff between the number of channels and the sampling rate limits the system bandwidth. Each additional channel costs $18.62+tax, making a 6 channel system cost only $210.72+tax.

A 3.0 V source power all of the parts to allow the system to become battery powered for mobile measurements. Lastly, the microcontroller used for analog-to-digital conversion and memory storage has many unused capabilities. Cost significantly reduces for a more tailored microcontroller that only uses the necessary functions.

## References


[1] FitzPatrick, Gerald J., and Edward F. Kelley. “Comparative High Voltage Impulse Measurement.” *Journal of Research of the national Institute of Standards and Technology* 101.5 (1996): 639-58. Web

[2] Akemoto, M., S. Gold, A. Krasnykh, and R. Koontz. *Design of a PFN for the NLC Klystron Pulse Modulator*. Proceeding of 1998 First Asian Particle Accelerator Conference, Tsukuba, Japan

[3] Maniglia, Jeff, Jordan Smiroldo, Alex Westfall, and Guy Zohar. "Design, Fabrication, and Testing of an Electromagnetic Rail Gun for the Repeated Testing and Simulation of Orbital Debris Impacts." Thesis. California Polytechnics State University, San Luis Obispo, 2010. Print.

[4] Keithley Instruments Inc., “Model 2657A: High Power System SourceMeter Instrument Specifications”, May 2012

[5] Agilent Technologies, “InfiniiVision 2000 X-Series Oscilloscopes Data Sheet”, March 2013

[6] Agilent Technologies, “Agilent U1610A/U1620A Handheld Digital Oscilloscope Datasheet”, February 2013

[7] Choy, Benedict, and Ching Chu. Complementary High Voltage Switched Current Source Integrated Circuit. Supertex, Inc., assignee. Patent 07956653. 2 June 2011. Print.

[8] Takayuki Sekiya, Nissin, and Takeshi Sakuma, Nagoya. High-Voltage Pulse Generating Circuit. NGK Insulators, LTD., assignee. Patent 7649284. 19 January 2010. Print

[9] Lucas, Rohan. High Voltage Engineering. University of Moratuwa, Sri Lanka, 2001. Available: http://www.dee.hcmut.edu.vn/vn/bomon/bmhethong/tailieu/tienganh/High%20Voltage%20Engineering.pdf

[10] Electus Distribution, “Optocouplers: When & How To Use Them”, 2001. Available: www.jaycar.com.au/images_uploaded/optocoup.pdf

[11] Fairchild Semiconductor, “Optocoupler Solutions”, 2010. Available: https://www.fairchildsemi.com/products/optoelectronics/high-performance-optocouplers/

[12] Vishay Semiconductors, “Optocouplers and Solid-State Relays: Application Examples”, November 2011

[13] Avago Technologies, “Optocoupler: Designer’s Guide”, June 2006. Available: http://www.avagotech.com/docs/5989-0802EN

[14] PerkinElmer, “Phototransistor and IRED Selection Guide”, pgs. 80-151

[15] Boylestad, Robert L., and Louis Nashelsky. "Chapter 4: DC Biasing-BJTs." *Electronic Devices and Circuit Theory*. 11th ed. Upper Saddle River: Pearson Education, 2012. 143-210. Print.

[16] Karki, James, “Fully-Differential Amplifiers”, Texas Instruments, 2002. Available: http://www.ti.com/general/docs/lit/getliterature.tsp?baseLiteratureNumber=sloa054&track=no

[17] Bhat, Akshay. "Stabilize Your Transimpedance Amplifier." - *Application Note*. Maxim Integrated, 3 Feb. 2012. Web. 24 June 2013. <http://www.maximintegrated.com/app-notes/index.mvp/id/5129>.

[18] Franco, Sergio. *Design with Operational Amplifiers and Analog Integrated Circuits*. 3rd ed. New York: McGraw-Hill Companies, 2001. Print.

[19] Jaeger, Richard C., and Travis N. Blalock. *Microelectroics Circuit Design*. 4th ed. New York: McGraw-Hill, 2011. Print.

# Appendix A: Code Composer Code

```
//###########################################################################
//
// FILE:   Example_2833xAdcSeqModeTest.c
//
// TITLE:  DSP2833x ADC Seq Mode Test.
//
// ASSUMPTIONS:
//
//    This program requires the DSP2833x header files.
//
//    Make sure the CPU clock speed is properly defined in
//    DSP2833x_Examples.h before compiling this example.
//
//    Connect the signal to be converted to channel A0.
//
//    As supplied, this project is configured for "boot to SARAM"
//    operation.  The 2833x Boot Mode table is shown below.
//    For information on configuring the boot mode of an eZdsp,
//    please refer to the documentation included with the eZdsp,
//
//      $Boot_Table:
//
//        GPIO87   GPIO86     GPIO85   GPIO84
//         XA15     XA14       XA13     XA12
//          PU       PU         PU       PU
//       ==========================================
//          1        1          1        1    Jump to Flash
//          1        1          1        0    SCI-A boot
//          1        1          0        1    SPI-A boot
//          1        1          0        0    I2C-A boot
//          1        0          1        1    eCAN-A boot
//          1        0          1        0    McBSP-A boot
//          1        0          0        1    Jump to XINTF x16
//          1        0          0        0    Jump to XINTF x32
//          0        1          1        1    Jump to OTP
//          0        1          1        0    Parallel GPIO I/O boot
//          0        1          0        1    Parallel XINTF boot
//          0        1          0        0    Jump to SARAM       <- "boot to SARAM"
//          0        0          1        1    Branch to check boot mode
//          0        0          1        0    Boot to flash, bypass ADC cal
//          0        0          0        1    Boot to SARAM, bypass ADC cal
//          0        0          0        0    Boot to SCI-A, bypass ADC cal
//                                  Boot_Table_End$
//
// DESCRIPTION:
//
//    Channel A0 and A1 is converted for pulse duration and logged in buffers, SampleTable1 and Sample
Table2, respectively
//
//    Open a memory window to SampleTable1 and SampleTable2 to observe the buffer
//    RUN for a while and stop and see the table contents.
```

```
//
//      Watch Variables:
//        SampleTable1 - Log of Channel A1 converted values.
//        SampleTable2 – Log of Channel A1 converted values.
//
//###########################################################################
//
// Original source by: S.S.
//
// $TI Release: 2833x/2823x Header Files and Peripheral Examples V133 $
// $Release Date: June 8, 2012 $
//###########################################################################

#include "DSP28x_Project.h"     // Device Headerfile and Examples Include File

// ADC start parameters
#if (CPU_FRQ_150MHZ)     // Default - 150 MHz SYSCLKOUT
  #define ADC_MODCLK 0x3 // HSPCLK = SYSCLKOUT/2*ADC_MODCLK2 = 150/(2*3)   = 25.0
MHz
#endif
#if (CPU_FRQ_100MHZ)
  #define ADC_MODCLK 0x2 // HSPCLK = SYSCLKOUT/2*ADC_MODCLK2 = 100/(2*2)   = 25.0
MHz
#endif
#define ADC_CKPS   0x0   // ADC module clock = HSPCLK/2*ADC_CKPS = 25.0MHz/(1*2) =
12.5MHz
#define ADC_SHCLK  0x0   // S/H width in ADC module periods = 1 ADC clock
#define AVG        3000  // Average sample limit
#define ZOFFSET    0x00  // Average Zero offset
#define BUF_SIZE   3100  // Sample Table buffer size
#pragma DATA_SECTION(SampleTable1,"DMARAML4");  // Store Channel A0 data in S4 SARAM
memory block
#pragma DATA_SECTION(SampleTable2,"DMARAML5");  // Store Channel A1 data in S5 SARAM
memory block


// Global variable for this example
Uint16 SampleTable1[BUF_SIZE];   // Buffer for Channel A0
Uint16 SampleTable2[BUF_SIZE];   // Buffer for Channel A1

main()
{
   Uint16 i;
   Uint16 k;
   Uint16 extra=0;
   Uint16 end_samples;
   Uint16 relevant = 0;


// Step 1. Initialize System Control:
// PLL, WatchDog, enable Peripheral Clocks
// This example function is found in the DSP2833x_SysCtrl.c file.
   InitSysCtrl();
```

```
// Specific clock setting for this example:
   EALLOW;
   SysCtrlRegs.HISPCP.all = ADC_MODCLK;         // HSPCLK = SYSCLKOUT/ADC_MODCLK
   EDIS;

// Step 2. Initialize GPIO:
// This example function is found in the DSP2833x_Gpio.c file and
// illustrates how to set the GPIO to it's default state.
// InitGpio();  // Skipped for this example

// Step 3. Clear all interrupts and initialize PIE vector table:
// Disable CPU interrupts
   DINT;

// Initialize the PIE control registers to their default state.
// The default state is all PIE interrupts disabled and flags
// are cleared.
// This function is found in the DSP2833x_PieCtrl.c file.
   InitPieCtrl();

// Disable CPU interrupts and clear all CPU interrupt flags:
   IER = 0x0000;
   IFR = 0x0000;

// Initialize the PIE vector table with pointers to the shell Interrupt
// Service Routines (ISR).
// This will populate the entire table, even if the interrupt
// is not used in this example.  This is useful for debug purposes.
// The shell ISR routines are found in DSP2833x_DefaultIsr.c.
// This function is found in DSP2833x_PieVect.c.
   InitPieVectTable();

// Step 4. Initialize all the Device Peripherals:
// This function is found in DSP2833x_InitPeripherals.c
// InitPeripherals(); // Not required for this example
   InitAdc();  // For this example, init the ADC

   InitFlash();

// Specific ADC setup for this example:
   AdcRegs.ADCTRL1.bit.ACQ_PS = ADC_SHCLK;
   AdcRegs.ADCTRL3.bit.ADCCLKPS = ADC_CKPS;
   AdcRegs.ADCTRL1.bit.CPS = 0;
   AdcRegs.ADCTRL1.bit.SEQ_CASC = 1;       // 1  Cascaded mode
   AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0x0;   // Convert Channel A0
   AdcRegs.ADCCHSELSEQ1.bit.CONV01 = 0x1;   // Convert Channel A1
   AdcRegs.ADCMAXCONV.bit.MAX_CONV1 = 0x1;  // Convert 2 Channels
   AdcRegs.ADCTRL1.bit.CONT_RUN = 1;       // Setup continuous run



// Step 5. User specific code:
```

```
// Clear SampleTables
  for (i=0; i<BUF_SIZE; i++)
  {
   SampleTable1[i] = 0;
   SampleTable2[i] = 0;
  }


  // Start SEQ1
  AdcRegs.ADCTRL2.all = 0x2000;

  // Take ADC data and log the in SampleTable arrays
   for (i=0; i<AVG; i++)
   {
                    while (AdcRegs.ADCST.bit.INT_SEQ1== 0) {} // Wait for interrupt
                    AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1;
                    SampleTable1[i] =((AdcRegs.ADCRESULT0>>4) );  // read Channel A0
                    SampleTable2[i] =((AdcRegs.ADCRESULT1>>4) );  // read Channel A1

                    if(SampleTable1[i]>100 && relevant==0)  // indicates pulse rising edge
                    {
                              relevant = 1;
                              end_samples = i-50
                    }
                    if(SampleTable1[i]<50 && relevant==1)  // indicates pulse falling edge
                    {
                              k = i+1;
                              i=AVG;
                    }
                    if(i==(AVG-1))  // wraps readings in buffer
                    {
                              i=0;
                    }

    }
//  continue sampling without relevant data overlab
    for (extra=k; extra<end_samples; extra++)
    {
          while (AdcRegs.ADCST.bit.INT_SEQ1== 0) {} // Wait for interrupt
          AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1;
          SampleTable1[extra] =((AdcRegs.ADCRESULT0>>4) );
          SampleTable2[extra] =((AdcRegs.ADCRESULT1>>4) );

                    if(k==(AVG-1))
                    {
                              k=0;
                    }
    }

//===========================================================================
// No more.
//===========================================================================
```

```
//---------------------------------------------------------------------------
// InitSysCtrl:
//---------------------------------------------------------------------------
// This function initializes the System Control registers to a known state.
// - Disables the watchdog
// - Set the PLLCR for proper SYSCLKOUT frequency
// - Set the pre-scaler for the high and low frequency peripheral clocks
// - Enable the clocks to the peripherals

void InitSysCtrl(void)
{

   // Disable the watchdog
   DisableDog();

   // Initialize the PLL control: PLLCR and DIVSEL
   // DSP28_PLLCR and DSP28_DIVSEL are defined in DSP2833x_Examples.h
   InitPll(DSP28_PLLCR,DSP28_DIVSEL);

   // Initialize the peripheral clocks
   InitPeripheralClocks();
}



//---------------------------------------------------------------------------
// InitPieCtrl:
//---------------------------------------------------------------------------
// This function initializes the PIE control registers to a known state.
//
void InitPieCtrl(void)
{
    // Disable Interrupts at the CPU level:
    DINT;

    // Disable the PIE
    PieCtrlRegs.PIECTRL.bit.ENPIE = 0;

          // Clear all PIEIER registers:
          PieCtrlRegs.PIEIER1.all = 0;
          PieCtrlRegs.PIEIER2.all = 0;
          PieCtrlRegs.PIEIER3.all = 0;
          PieCtrlRegs.PIEIER4.all = 0;
          PieCtrlRegs.PIEIER5.all = 0;
          PieCtrlRegs.PIEIER6.all = 0;
          PieCtrlRegs.PIEIER7.all = 0;
          PieCtrlRegs.PIEIER8.all = 0;
          PieCtrlRegs.PIEIER9.all = 0;
          PieCtrlRegs.PIEIER10.all = 0;
          PieCtrlRegs.PIEIER11.all = 0;
          PieCtrlRegs.PIEIER12.all = 0;
```

```
        // Clear all PIEIFR registers:
        PieCtrlRegs.PIEIFR1.all = 0;
        PieCtrlRegs.PIEIFR2.all = 0;
        PieCtrlRegs.PIEIFR3.all = 0;
        PieCtrlRegs.PIEIFR4.all = 0;
        PieCtrlRegs.PIEIFR5.all = 0;
        PieCtrlRegs.PIEIFR6.all = 0;
        PieCtrlRegs.PIEIFR7.all = 0;
        PieCtrlRegs.PIEIFR8.all = 0;
        PieCtrlRegs.PIEIFR9.all = 0;
        PieCtrlRegs.PIEIFR10.all = 0;
        PieCtrlRegs.PIEIFR11.all = 0;
        PieCtrlRegs.PIEIFR12.all = 0;


}



//---------------------------------------------------------------------------
// InitAdc:
//---------------------------------------------------------------------------
// This function initializes ADC to a known state.
//
void InitAdc(void)
{
   extern void DSP28x_usDelay(Uint32 Count);


   // *IMPORTANT*
        // The ADC_cal function, which  copies the ADC calibration values from TI reserved
        // OTP into the ADCREFSEL and ADCOFFTRIM registers, occurs automatically in the
        // Boot ROM. If the boot ROM code is bypassed during the debug process, the
        // following function MUST be called for the ADC to function according
        // to specification. The clocks to the ADC MUST be enabled before calling this
        // function.
        // See the device data manual and/or the ADC Reference
        // Manual for more information.

           EALLOW;
                SysCtrlRegs.PCLKCR0.bit.ADCENCLK = 1;
                ADC_cal();
                EDIS;




   // To powerup the ADC the ADCENCLK bit should be set first to enable
   // clocks, followed by powering up the bandgap, reference circuitry, and ADC core.
   // Before the first conversion is performed a 5ms delay must be observed
        // after power up to give all analog circuits time to power up and settle

   // Please note that for the delay function below to operate correctly the
```

```
        // CPU_RATE define statement in the DSP2833x_Examples.h file must
        // contain the correct CPU clock period in nanoseconds.

   AdcRegs.ADCTRL3.all = 0x00E0;  // Power up bandgap/reference/ADC circuits
   DELAY_US(ADC_usDELAY);         // Delay before converting ADC channels
}



//---------------------------------------------------------------------------
// InitPieVectTable:
//---------------------------------------------------------------------------
// This function initializes the PIE vector table to a known state.
// This function must be executed after boot time.
//

void InitPieVectTable(void)
{
        int16   i;
        Uint32 *Source = (void *) &PieVectTableInit;
        Uint32 *Dest = (void *) &PieVectTable;

        EALLOW;
        for(i=0; i < 128; i++)
                *Dest++ = *Source++;
        EDIS;

        // Enable the PIE Vector Table
        PieCtrlRegs.PIECTRL.bit.ENPIE = 1;

}



//---------------------------------------------------------------------------
// Example: InitFlash:
//---------------------------------------------------------------------------
// This function initializes the Flash Control registers

//                 CAUTION
// This function MUST be executed out of RAM. Executing it
// out of OTP/Flash will yield unpredictable results

void InitFlash(void)
{
  EALLOW;
  //Enable Flash Pipeline mode to improve performance
  //of code executed from Flash.
  FlashRegs.FOPT.bit.ENPIPE = 1;

  //                CAUTION
  //Minimum waitstates required for the flash operating
  //at a given CPU rate must be characterized by TI.
  //Refer to the datasheet for the latest information.
```

```
#if CPU_FRQ_150MHZ
  //Set the Paged Waitstate for the Flash
  FlashRegs.FBANKWAIT.bit.PAGEWAIT = 5;

  //Set the Random Waitstate for the Flash
  FlashRegs.FBANKWAIT.bit.RANDWAIT = 5;

  //Set the Waitstate for the OTP
  FlashRegs.FOTPWAIT.bit.OTPWAIT = 8;
#endif

#if CPU_FRQ_100MHZ
  //Set the Paged Waitstate for the Flash
  FlashRegs.FBANKWAIT.bit.PAGEWAIT = 3;

  //Set the Random Waitstate for the Flash
  FlashRegs.FBANKWAIT.bit.RANDWAIT = 3;

  //Set the Waitstate for the OTP
  FlashRegs.FOTPWAIT.bit.OTPWAIT = 5;
#endif
  //              CAUTION
  //ONLY THE DEFAULT VALUE FOR THESE 2 REGISTERS SHOULD BE USED
  FlashRegs.FSTDBYWAIT.bit.STDBYWAIT = 0x01FF;
  FlashRegs.FACTIVEWAIT.bit.ACTIVEWAIT = 0x01FF;
  EDIS;

  //Force a pipeline flush to ensure that the write to
  //the last register configured occurs before returning.

  asm(" RPT #7 || NOP");
}
```

# Appendix B: Analysis of Senior Project Design

## 1. Summary of Functional Requirements

The design and construction of a high voltage pulse measurement system provides a safe, accurate, and low cost means to measure high voltage pulses in harsh electromagnetic environments.

REQUIREMENTS

1. Measure high voltages, both positive and negative
2. High system bandwidth for high frequency signals
3. Able to operate under harsh electromagnetic environments
4. Provide isolation between the high voltage system and the measurement system
5. Multiple probes for simultaneous node measurements
6. Full system powered by single low voltage source
7. High resolution for high voltages
8. “Hardware programming” for adjustable resolution
9. Adjustable sampling rate
10. Onboard memory
11. Sufficiently large memory
12. Minimize cost

## 2. Primary Constraints

The use of optocoupler technology to provide isolation makes it difficult to measure positive and negative signals. The HCNR200 optocoupler only allows current in one direction, giving two options to measure bipolar signals. The measurement system

can use two optocouplers, where one measures positive signals and the other measures negative signals. Or the measurement system can use only one optocoupler to measure both positive and negative signals, requiring the addition of a full-bridge rectifier.

Initially, the measurement system used the two optocoupler approach. However, matching the optocouplers poses another problem. Optocouplers' CTR vary from one optocoupler to another. Therefore, the magnitude of the output voltage differs for a positive and negative signal of equal magnitudes. The implemented measurement system using two optocouplers verified this mismatch, seen in Figure 3.14.

A single optocoupler, with the addition of a full-bridge rectifier, measurement system eliminates the optocoupler mismatch problem. The full bridge rectifier outputs the absolute value of the signal. One optocoupler can now isolate the full signal rather than just the positive portion or just the negative portion of the signal. However, the negative portion of a signal now appears positive at the output. A simple inversion (multiplication by -1) on the digital end during processing corrects this.

The transition from using two optocouplers to using only one optocoupler in the final design significantly delayed the development process of the measurement system. I needed to order an additional part, reconstruct the analog front-end, test the improved analog front-end, and then test the full design. This delayed the completion of the project by four weeks.

## 3. Economic

The requirements state the measurement system should cost less than $100 per channel. A single channel measurement system had a projected cost of $95.60 but

actually cost $118.82+tax, shown in Table 3. However, each additional channel would only cost $19.82. A two channel system costs $138.64, reducing the per channel cost to $69.32, now meeting the requirement.

| PART | QUANTITY | UNIT COST ($) (ORIGINAL) | UNIT COST ($) (ACTUAL) |
|---|---|---|---|
| 7.5kΩ Front End Resistors MP925-7.50K-F-ND | 2 | 5.00 | 4.45 |
| Full Bridge Rectifier ZXSBMR16PT8 | 1 | N/A | 1.73 |
| Optocoupler HCNR200 | 1 | 5.00 | 4.27 |
| Operational Amplifier LT6221 | 1 | 5.00 | 3.72 |
| 11 kΩ Feedback Resistor | 2 | 0.10 | 0.09 |
| 8.2pF Feedback Capacitor | 2 | 0.40 | 0.51 |
| Analog-to-Digital Converter TMS320F28335 | 1 | 75.00 | 99.00 |
| Memory TMS320F28335 | 1 | | |
| | TOTAL COST | $95.60 | $118.82+tax |

Table 3: Original and Actual Cost of the Measurement System. The table displays all of the parts used to construct the system, the quantity of each part used, and the original and actual cost. Originally, the entire measurement system cost $95.60, but the final product actually cost $118.82.

The labor cost to solder and connect all of the parts together may increase the cost by about $10 per unit. A two channel or greater system still maintains the low cost specification of under $100 per channel.

Table 4 shows the costs of the pulse generator circuit used to test the final design of the measurement system. There were no projected costs because this was used for testing purposes only, but the pulse generator added a development cost of $5.28.

| PART | QUANTITY | UNIT COST |
|---|---|---|
| PMOS<br>FQB1P50TMCT-ND | 1 | $1.00 |
| NMOS<br>FQU1N60CTUFS-ND | 1 | $0.65 |
| 100kΩ Resistor | 1 | $0.09 |
| 4700pF Capacitor<br>399-7725-ND | 2 | $1.77 |
| | TOTAL COST | $5.28 |

Table 4: Pulse Generator Circuit Cost. The circuit costs a total of $5.28. The circuit creates high voltage pulses needed to test and characterized the measurement system.

At the beginning of this thesis, the plan set a completion date for the end of Spring Quarter as shown in Figure A.1. The thesis took longer than expected due inaccurate results of the original design. The measurement system went through a redesign process causing a delay in the completion of the thesis, shown in Figure A.2. The additional tasks in the development of the system includes characterizing the added full-bridge recitifer, testing the improved front-end, constructing the improved final design, and testing the final design.

| FALL QUARTER | Week1 | Week2 | Week3 | Week4 | Week5 | Week6 | Week7 | Week8 | Week9 | Week10 |
|---|---|---|---|---|---|---|---|---|---|---|
| Research Pulse Forming Networks | | | | | | | | | | |
| Research Optocoupler Technology | | | | | | | | | | |
| Research Transimpedance Amplifiers | | | | | | | | | | |
| Design and Simulations | | | | | | | | | | |
| Order Design Parts | | | | | | | | | | |

| WINTER QURATER | Week1 | Week2 | Week3 | Week4 | Week5 | Week6 | Week7 | Week8 | Week9 | Week10 |
|---|---|---|---|---|---|---|---|---|---|---|
| Construct Optocoupler Test Circuit | | | | | | | | | | |
| Characterize Optocouplers | | | | | | | | | | |
| Constuct Front End | | | | | | | | | | |
| Test Front End | | | | | | | | | | |
| Construct TIA Test Circuit | | | | | | | | | | |
| Charaterize TIA | | | | | | | | | | |
| Construct Full Design | | | | | | | | | | |
| Test Full Design | | | | | | | | | | |
| Characterize Microcontroller | | | | | | | | | | |
| Research Pulse Generating Circuits | | | | | | | | | | |

| SPRING QUARTER | Week1 | Week2 | Week3 | Week4 | Week5 | Week6 | Week7 | Week8 | Week9 | Week10 |
|---|---|---|---|---|---|---|---|---|---|---|
| Design Pulse Generating Circuit | | | | | | | | | | |
| Constucting Pulse Generating Circuit | | | | | | | | | | |
| Characterize Pulse Generating Circuit | | | | | | | | | | |
| Low Voltage Testing | | | | | | | | | | |
| High Voltage Testing | | | | | | | | | | |
| Thesis Write Up | | | | | | | | | | |
| Thesis Defense | | | | | | | | | | |

Figure A.1: Original Development Time Gant Chart. The plan sets the completion of the thesis in three quarters.

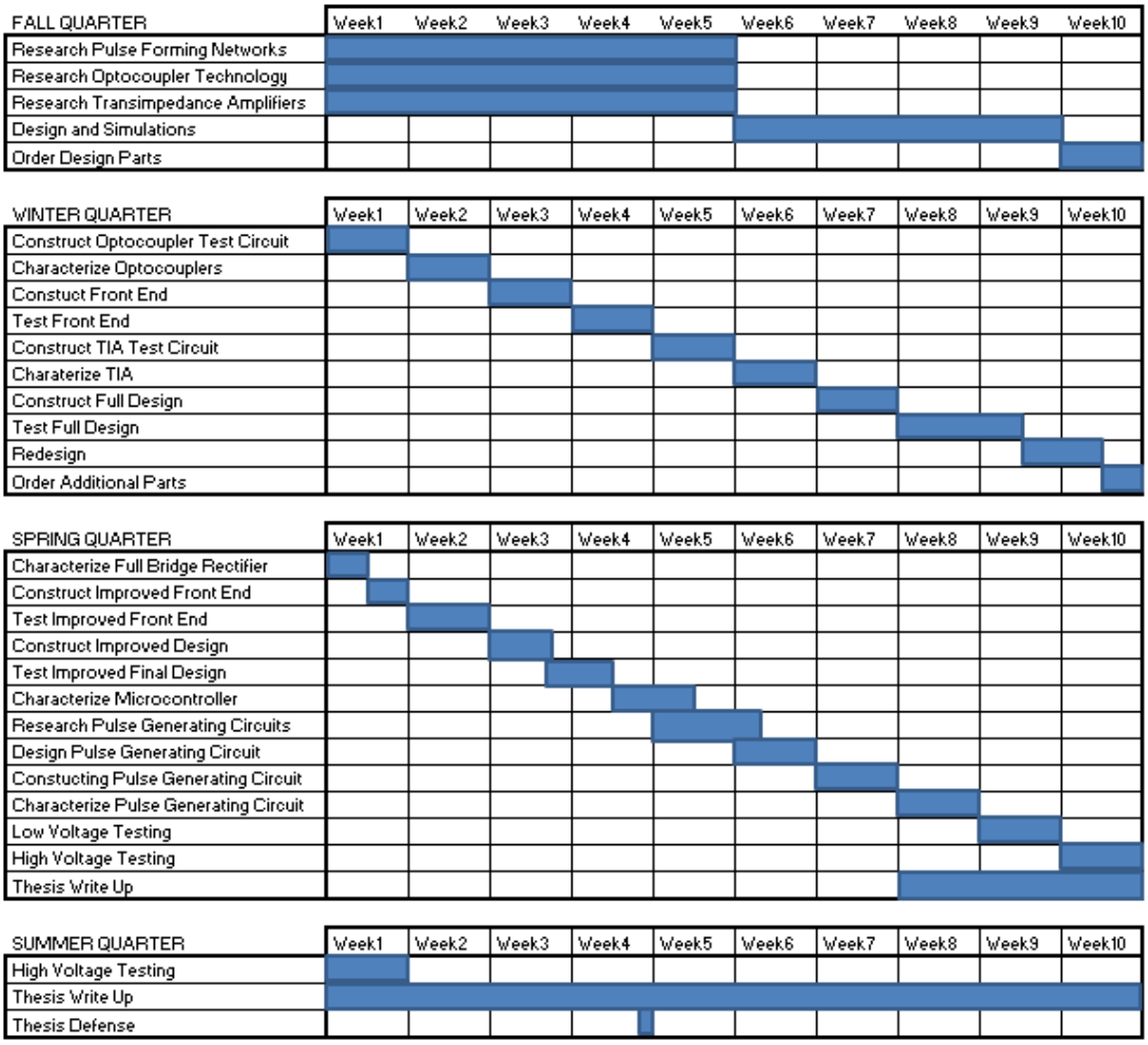


Figure A. 2: Actual Development Gant Chart. The thesis did not finish until four weeks past the expected completion time. The thesis went through a redesign process and additional tasks needed completing.

The completion of the this thesis required not only extra weeks, but a significant amount of additional work hours per week. The redesign process took an additional five weeks, starting in week 9 of Winter Quarter. The completion of the thesis did not occur until four weeks after the original expected competion date.

In hindsight, I would have started work on my thesis earlier to allow a more flexible schedule. The original plan of completing this thesis in three quarters proved a little too ambitious. A more flexible plan would have allowed me to better adjust for delays during the project, such as the redesign process.

## 4. Manufacturing

Table 4 shows the cost of manufacturing 1 unit, 100 units, and 1000 units of a single measurement system. The more units manufactured at a time will reduce the unit cost the system. Current commercial equipment that can measure high voltage pulses cost thousands of dollars. Therefore, this measurement system can be sold for $200, as it still provides a much cheaper means of measuring high voltage pulses.

| PART | COST TYPE (FIXED/ VARIABLE) | QUANTITY | UNIT COST ($) (1 Unit) | UNIT COST ($) (100 Unit) | UNIT COST ($) (1000 Unit) |
|---|---|---|---|---|---|
| 7.5kΩ Front End Resistors MP925-7.50K-F-ND | VARIABLE | 2 | 4.45 | 2.99 | 2.56 |
| Full Bridge Rectifier ZXSBMR16PT8 | VARIABLE | 1 | 1.73 | 1.21 | 0.94 |
| Optocoupler HCNR200 | VARIABLE | 1 | 4.27 | 2.56 | 1.89 |
| Operational Amplifier LT6221 | VARIABLE | 1 | 3.72 | 2.13 | 2.13 |
| 11 kΩ Feedback Resistor | VARIABLE | 2 | 0.09 | 0.03 | 0.01 |
| 8.2pF Feedback Capacitor | VARIABLE | 2 | 0.51 | 0.24 | 0.15 |
| ADC TMS320F28335 | FIXED | 1 | 99.00 | 99.00 | 99.00 |
| Memory TMS320F28335 | FIXED | 1 | | | |
| | | TOTAL COST | $118.82 | $111.42 | $109.40 |
| | | PROFIT IF SYSTEM SOLD AT $200 | $81.18 | $88.58 | $90.96 |

Table 4: Measurement System Costs and Profits. The table shows the cost of each component if a company produces 1 unit, 100 units, and 1000 units. The more units manufactured at a time, the less each component costs and thus increases profit. For systems of more than one channel, only the variable cost parts' quantities increase and add to the total cost, up to 6 six channels.

Pulsed power does not have a large market but applications include rail guns, radar, and food processing. If a company manufactured and sold 100 units they would profit $8858, a 44% sales margin.

Optimizing the microcontroller interface can significantly reduce the cost of the measurement system. The kit used with the microcontroller allows interface with many other capabilities of the microcontroller such as the PWM, McBSP, and eCAN modules. Customizing the interface to only make use of only the ADC and memory will reduce cost and thus increase profit.

## 5. Environmental

The manufacturing of this measurement system has a minimal impact on the environment. The design uses four ICs (rectifier, optocoupler, dual amplifier, and microcontroller), six resistors, and three capacitors. The four components consume only a few grams of resources in the silicon for the ICs, carbon for the resistors, and ceramic for the capacitors. In addition, the system operates off a low power supply to minimize energy consumption. Tests for the optocouplers show reliability over 10,000 hours of continuous operation, ensuring a very long system lifespan. This reduces the waste from systems no longer operating correctly. Therefore, the measurement system has a minimal environmental cost.

## 6. Manufacturability

The design of the board setup for the TMS320F28335 microcontroller does not have high space efficiency. The docking station has a size of 6” x 3” and the control card has a size of 3.5” x 2”. The control board mounts perpendicularly onto the docking station in Figure A.3. The excessive physical space it requires results in a mechanical and packaging design constraint. A parallel implementation of the control board and docking station would utilize space more efficiently. Furthermore, a more customized interface with the microcontroller, such as a single board, would make manufacturing easier.

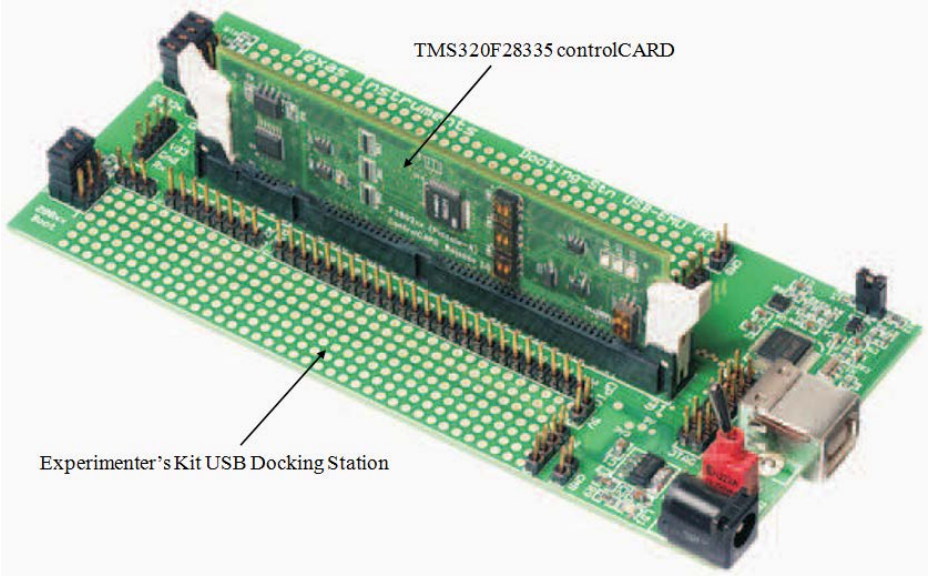


Figure A.3: TMS320F28335 controlCARD and Experimenter's Kit USB Docking Station Configuration. The controlCARD provides the appropriate circuitry needed to interface with each pin of the microcontroller. The docking station provides power, USB interface, and physical interface to the microcontroller. The controlCARD perpendicularly inserts into the center, black dock.

## 7. Sustainability

The measurement system requires very little maintenance and resources. To maintain the system, the user only needs to recalibrate the system about every 500 hours of use. The design of the measurement system only requires a 3.0V power supply. The low voltage power supply minimizes the amount of power needed for operation of the system while maintaining performance. A design for a lower voltage system would result in worse measurement accuracy because this will decrease the full scale range of the ADC. On the other hand, an "improved" system may use a 5.0V power supply to increase accuracy, however would require more power for operation.

## 8. Ethical

The first rule in the IEEE code states engineers should “accept responsibility in making decisions consistent with the safety, health, and welfare of the public, and to disclose promptly factors that might endanger the public or the environment.” The measurement system employs isolation to prevent over voltage damage from the high voltage system to the low voltage measurement system. However, the more important reason for isolation is to protect the user operating the measurement system from high voltages. High voltages can cause serious injury and even death to people. The safety of people remains the highest priority when developing this system.

The IEEE code also states engineers should “be honest and realistic in stating claims or estimates based on available data.” Proper characterization of the measurement system needs execution to provide users with the accurate results. In addition, users need to use the system to measure and accurately report the data they have found on their projects. As of now, the measurement system uses an easily manipulated program in Excel and results can be altered. Users need to use the system to report honest results of their projects when claiming performance and reliability parameters.

## 9. Health and Safety

When dealing with high voltage systems, safety becomes the major concern. As stated in the previous section, the measurement system provides isolation to protect the user from the measured high voltage system.

## 10. Social and Political

The parties involved in the design and manufacturing of this measurement system include:

- Project Designer: Angelo Ballungay (self)
- California Polytechnic State University, San Luis Obispo
- Cal Poly Power Pulse Club
- Pulse power industries
    - Rail guns
    - Radar
    - Medical (defibrillator and ultrasound)
    - Food processing (used to kill certain types of bacteria)
- Companies who sell current pulse measuring equipment (Agilent, Tektronix, etc.)

Not only can Cal Poly Power Pulse Club now measure and characterize their pulsed power systems, but other clubs and individuals experimenting with pulsed power can too. With a more specific application measurement system available, lower budget projects will use this system rather than the expensive measurement equipment current companies sell. More people are able to work on pulsed power projects and contribute to the advancement of the industry.

A low cost measurement system provides people with a way to measure high voltage pulses without spending thousands of dollars on expensive equipment. This is especially important in early stages of product development. Generally, people fund their own ideas or may find investors to give a small initial monetary contribution to get a

project started. However, until proof of concept has been achieved, an investor will not contribute large amounts of money towards a project. Therefore, minimizing the development cost of a design is crucial in the beginning phases of a project.

## 11. Development

Throughout this thesis I learned about high voltage pulse circuits, optocouplers, and a more in depth understanding on the development process of a product. Learning the different designs of PFNs and pulse generators broadened my knowledge of how to use utilize components. PFNs mainly use inductors and capacitors to store energy and then release this energy to create a high voltage pulse. Pulse generators make more use of transistors and diodes, but also sometimes use capacitors and inductors also, to create pulse trains. In class, we learn more building block circuits. Researching and understanding these circuits applied these building blocks and showed how to use these components to invent and innovate.

Optocouplers use an input current to drive an LED which emits photons detected by a photodetector. The photodetector then outputs a current linearly related to the current flowing through the LED. Optocouplers provide isolation between high voltage systems and low voltage systems to protect the low voltage system from overvoltage damage. I learned the different performance parameters that should be taken into account when choosing an optocoupler along with its various applications. I also learned about diode matching, which should be avoided in designing products.

I learned a lot throughout the development of this thesis. From wasted time waiting for ordered parts to troubleshooting techniques of the subsystems, I've learned

how to better manage time and how to break down and analyze situations. Product development should start as soon as possible. The time schedule can then use "stretch" goals to allow more time for different stages of the development cycle. Developers can get ahead of milestone dates and compensate for delays when and if they occur.

Troubleshooting techniques mainly include the ability to break down situations into their smallest parts and developing a method to test each part of the problem. Creating I-V and I-I curves and DC and AC testing assisted in diagnosing the optocoupler mismatch problem. Simulations and derivations of the TIA found the feedback capacitor value that will stabilize the TIA. And analyzing the LED voltage response helped identify system delays due to parasitic capacitances. I believe I have encountered many issues that apply to circuits that I will encounter throughout my career and has developed me as an electrical engineer.

## References


[1] FitzPatrick, Gerald J., and Edward F. Kelley. "Comparative High Voltage Impulse Measurement." *Journal of Research of the national Institute of Standards and Technology* 101.5 (1996): 639-58. Web

[2] Akemoto, M., S. Gold, A. Krasnykh, and R. Koontz. *Design of a PFN for the NLC Klystron Pulse Modulator*. Proceeding of 1998 First Asian Particle Accelerator Conference, Tsukuba, Japan

[3] Maniglia, Jeff, Jordan Smiroldo, Alex Westfall, and Guy Zohar. "Design, Fabrication, and Testing of an Electromagnetic Rail Gun for the Repeated Testing and Simulation of Orbital Debris Impacts." Thesis. California Polytechnics State University, San Luis Obispo, 2010. Print.

[4] Keithley Instruments Inc., "Model 2657A: High Power System SourceMeter Instrument Specifications", May 2012

[5] Agilent Technologies, “InfiniiVision 2000 X-Series Oscilloscopes Data Sheet”, March 2013

[6] Agilent Technologies, “Agilent U1610A/U1620A Handheld Digital Oscilloscope Datasheet”, February 2013

[7] Choy, Benedict, and Ching Chu. Complementary High Voltage Switched Current Source Integrated Circuit. Supertex, Inc., assignee. Patent 07956653. 2 June 2011. Print.

[8] Takayuki Sekiya, Nissin, and Takeshi Sakuma, Nagoya. High-Voltage Pulse Generating Circuit. NGK Insulators, LTD., assignee. Patent 7649284. 19 January 2010. Print

[9] Lucas, Rohan. High Voltage Engineering. University of Moratuwa, Sri Lanka, 2001. Available: http://www.dee.hcmut.edu.vn/vn/bomon/bmhethong/tailieu/tienganh/High%20Voltage%20Engineering.pdf

[10] Electus Distribution, “Optocouplers: When & How To Use Them”, 2001. Available: www.jaycar.com.au/images_uploaded/optocoup.pdf

[11] Fairchild Semiconductor, “Optocoupler Solutions”, 2010. Available: https://www.fairchildsemi.com/products/optoelectronics/high-performance-optocouplers/

[12] Vishay Semiconductors, “Optocouplers and Solid-State Relays: Application Examples”, November 2011

[13] Avago Technologies, “Optocoupler: Designer’s Guide”, June 2006. Available: http://www.avagotech.com/docs/5989-0802EN

[14] PerkinElmer, “Phototransistor and IRED Selection Guide”, pgs. 80-151

[15] Boylestad, Robert L., and Louis Nashelsky. "Chapter 4: DC Biasing-BJTs." *Electronic Devices and Circuit Theory*. 11th ed. Upper Saddle River: Pearson Education, 2012. 143-210. Print.

[16] Karki, James, “Fully-Differential Amplifiers”, Texas Instruments, 2002. Available: http://www.ti.com/general/docs/lit/getliterature.tsp?baseLiteratureNumber=sloa054&track=no

[17] Bhat, Akshay. "Stabilize Your Transimpedance Amplifier." - *Application Note*. Maxim Integrated, 3 Feb. 2012. Web. 24 June 2013. <http://www.maximintegrated.com/app-notes/index.mvp/id/5129>.

[18] Franco, Sergio. *Design with Operational Amplifiers and Analog Integrated Circuits*. 3rd ed. New York: McGraw-Hill Companies, 2001. Print.

[19] Jaeger, Richard C., and Travis N. Blalock. *Microelectroics Circuit Design*. 4th ed. New York: McGraw-Hill, 2011. Print.