FABRICATION AND CHARACTERIZATION OF A
PALLADIUM/ POROUS SILICON LAYER

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ABSTRACT

Fabrication and Characterization of a Palladium/ Porous Silicon Layer

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A scientific paper can be considered a journey into the logic and mind of the scientist who performed the experiment. This paper, a little unconventional, is written as a reflection of how the author organizes and thinks through his topic. In the telling of it this way, he hopes the journey is as compelling for the reader as it was for him.

When porous silicon is plated with a catalytic metal, the two materials can act together as a single entity whose electrical properties are sensitive to its environment – the sensing component of an electrochemical gas sensor. Etching pores into silicon is an electrochemical process; and which type of doped silicon used is one of its key parameters. For nearly all reported porous silicon gas sensors, the silicon has been of the p-doped variety – because p-doped porous etching is better understood and the layers that result from it are more predictable – despite n-doped silicon having potentially significant benefits in ease of fabrication and being more conducive to plating by a catalyst. This experiment is an attempt at creating a palladium plated n-doped porous silicon layer, and an examination into what differentiates this fabrication process and the layers that result from the traditional p-doped type.

The porous layers to be plated are to be the same and would ideally have properties that are a close approximation to what a functional gas sensor would require. This experiment defined a process that fabricated this “ideal” layer out of N-type, <100>, double polished silicon wafers with a resistance of 20 Ω cm. The wafers were subjected to the anodic etching method with an HF/ethanol mixture as the electrolyte; and only two (of among many) fabrication parameters were varied: HF concentration of the electrolyte and total etching time. We find that a concentration of 12% HF (by volume) and an etching time of 6 hours result in layers most appropriate to carry into plating. The anodization current density is 15 mA cm⁻². Deposition of the catalyst, palladium, is done using the electroless method by immersing the porous layer in a .001M PdCl₂ aqueous bath.

Characterization of this Pd/Porous Silicon layer was done by measuring resistivity by four point probe and imaging through Scanning Electron Microscopy. It was found that layers of a

maximum average of $63 \pm 6\%$ porosity were created using our fabrication method. There is evidence of palladium deposition, but it is spotty and irregular and is of no improvement despite the n-doping wafer makeup. Resistivity in well-plated regions was measured to be 7-10 Ωcm , while resistivity in regions not well-plated was measured to be 70-140 $\Omega\text{ cm}$. This is comparable to previous literature values, indicating n-silicon porous silicon can be fabricated and still have potential as a catalytic layer, should metal deposition methods improve.

Keywords: Porous Silicon, Electroless Plating, Anodic Etching.

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Chapter 1: Introduction

At its most general, a porous material refers to a bulk substance penetrated by an orderly series of holes (pores). Although the holes can be of any size, the majority of research in this field centers upon pores with diameters in the micro/nano meter range – for a material with pores on this scale can be bestowed with properties that are of great benefit in a variety of applications. There is, for instance, an increase in interior void space. Void space is the product of two factors, and both have their particular uses. The first, pore size, controls the pockets of emptiness within the material, a crucial attribute when creating vibration dampeners, lightweight structures, or thermal insulators. The second, pore shape, controls the pathways through the material's interior; useful in chemical separators, filters or membrane materials. The pores can also be viewed as small, limiting chambers within which any number of chemical reactions can occur, a benefit to those who need these tiny voids to template for nanowires, synthesize nanoparticles, or are interested in the forming of any other small structures. And then there is surface area, which is increased from the hollowing out of the interior. Surface area amount is crucial for applications of surface chemistry, chromatography, catalysis, and sensing [1].

The key to porous materials' appeal is that these gains – in voids, in templates, in surface area – can be had while simultaneously reducing the amount of material used and saving on the volume of space taken. That is, *porosity is the most efficient use of material*. And the more common the material is, often the greater the desire to benefit from that efficiency. Thus the reason for the large amount of attention of late into making silicon porous: silicon is the most commonly used semiconducting material in the world.

1.1 Porous Silicon

Porous silicon is now extensively studied by scientists who want to improve upon the microelectronics industry by making even lighter, smaller devices. This potential, and the subsequent interest in it, is only a recent occurrence. The material itself was first discovered in 1956 by Uhlir and Turner at Bell Laboratories, who found that electropolishing silicon in hydrogen fluoride (HF) under slight anodization conditions lead to a faint brown tinge on the surface of the semiconducting material. Initially, the two believed the color was a thin film of fluoro-silicon (SiF_2)

surface growth that was a byproduct of the polishing process [2]. But eventually it was found that the color was a product of interference from light reflecting off an increasingly non-uniform silicon surface; no fluoride was present. Uhler had discovered that when anodically etching under lower current thresholds, the silicon was not removed evenly across the surface, as is done during polishing, but instead removed selectively to form a series of pits or holes; this is termed porous silicon [2].

A schematic of a common etching cell is shown in Figure 1 [3]. The cell consists of two parts both commonly made of teflon, which is immune to acidic attack. The top piece contains a hole in the middle into which the etching acid and cathode electrode will go. The base plate is solid, onto which is placed the anode electrode and, above it, the silicon sample. The top and base plates are then attached together, with the aluminum plate, silicon and o-ring sandwiched between them (the o-ring between the top plate and the silicon to prevent leakage). Once a seal is confirmed, the etching electrolyte is poured into the hole and the cathode is placed in this electrolyte so that it hovers above without touching the silicon. Both electrodes are then attached to a regulated power source and, with a closed circuit having now been created, a current is induced. So long as the current stays below a critical threshold (further explanation to be provided), the sample will become porous instead of polished.

Figure 1 Cross sectional view of a conventional single tank cell [3]

The relative simplicity of the etching cell leads to one of porous silicon's great advantages: it is fairly easy and cheap to make. Interestingly however, the discovery was deemed useless and left

to languish until the 1990's, when microfabrication technology began to find potential uses for a material that had previously been relegated as a minor curiosity.

1.2 Electrochemical Sensors

One of these uses involves using the porous silicon as a chemical sensor. As a material, silicon is often optimal for sensing purposes: it has a stable crystalline structure, has durability under extreme temperatures, is relatively inert to indirect chemical processes and yet has a high surface activity for chemical reactions [4]. It is also a great candidate for porosity, with a potential internal surface area found to be between 200-800 $\frac{m^2}{cm^3}$, a well known and predictable electrical and electrochemical behavior, and ubiquitous presence in the industry – making it both an inexpensive and yet familiar material to work with [4].

Because of these characteristics, porous silicon can use changes in any number of properties as a sensing signal, including work function, refractive index, dielectric constant, photoluminescence (PL) intensity, resistivity or capacitance [5]. These changes are brought on by the surface interaction between the analyte – be it a biological, gas, metallic or solution – and the silicon surface.

This thesis builds on the large number of studies by other scientists who have used porous silicon as an electrochemical gas sensor [6,7,8], which works on very simple principles. Porous silicon acts as the active layer that contains a specific resistance. When exposed, the gas adsorbs onto the surface and changes the distribution of charges within the silicon surface, producing a change in the resistivity of the overall layer. Since porous materials have a larger surface area, there is theoretically more adsorption, thus amplifying the signal. Measuring these changes can be easily done by constructing a device of the type shown in Figure 2. Two metal contacts are placed onto the porous silicon. A current is induced across porous silicon and changes in conductivity across the layer in the presence of gas can be measured [5]. This method has shown to be able to detect a diverse collection of species: H_2O , NO , NO_2 , Cl_2 , Br_2 , alcohols and hydrocarbons [5]. In fact, almost any polar molecule has an ability to induce a change in surface state; this is what has made silicon so attractive to sensor makers.

Figure 2 A typical porous silicon gas sensor [5].

For the species which silicon alone cannot sense, the underlying properties of the porous silicon (electrical conductivity, surface area) may still be desirable enough to use in some other fashion. A common workaround is instead to use porous silicon as a substrate material. Another material becomes the actual sensing layer that will be coated on top, and the still fully functional silicon substrate underneath continues as the current-through layer that responds to the changes happening in the layer above it. The two materials complement each other as a single active sensing component in a device. The studies that have explored creating this dual system have often used a surface layer of noble metals – the noble metals: palladium, platinum or ruthenium, being well known for their catalytic activity – and the resulting devices have utilized this catalytic activity to broaden porous silicon’s capabilities; sensing anything from hydrogen gas (H_2) to various toxic gases at room temperature to even humidity in the air [6]. Adding the catalyst doesn’t change the sensor design; this remains similar to what was seen in Figure 2.

1.3 Motivations and Goals of Project

The goal of this project is to describe a fabrication setup capable of creating a sensing layer that is of this dual catalyst/porous silicon combination and to characterize the samples that come out of this setup; an actual catalysis using the layer is not performed. In the process, the experiment attempts an easier fabrication method than what is usually required when making layers of this type, and will analyze these layer’s properties as a comparison to the normal expected performance. Describing what differentiates this process from the norm requires an involved discussion into the science behind porous silicon. The material may have a relatively simplistic manufacturing process but the factors that result from its creation are a multifaceted and much pored over field of study.

Chapter 2: Basics of Porous Silicon

In recent years, there has arisen in materials science a category known as *architected materials*. Whereas most materials – that is, those that are non-architected – are traditionally described by its structure-processing-properties “triangle”; architected materials are described by its structure-*architecture*-processing-properties “diamond” (Figure 3). That extra factor, architecture, refers to the forming of traditional materials into a cohesive geometrical structure at the micro/nano scale, a level above the individual placement of atoms in a lattice [9]. Building and analyzing these structures has only been made possible through modern microfabrication techniques, and they have enabled materials to be arranged into spectacular new forms that enable new functions and properties; essentially categorizing itself as a material of a different type despite being built from familiar elements. Thus the need to expand beyond the traditional triangle and into a diamond type description, the old three point discussion was insufficient to encompass these new configurations.

Figure 3 The three points that make up the traditional (a) "Materials Science Triangle" become a four corner (b) "Diamond" when architecture is added as an extra factor.

Porous silicon is the embodiment of an architected material. To effectively explain any of its characteristics necessitates discussions into semiconductor science, nano-morphology, chemical etching, and residual effects. Hence the metaphor of the diamond, the material is best relayed by organizing each topic into one of the four corners. We will start at the bottom, with structure. This will not cover atomic structure (which is one of the properties that remain beneficially intact) but electronic structure, since it is this concept that will most affect the final property (conductivity) being examined.

2.1 The First Corner: Electronic Structure

Fabricating porous silicon is an electrochemical reaction, as is using it as an electrochemical sensor. A basic explanation of the electronic properties of silicon will be necessary now, in the hopes that this knowledge will aid understanding later.

Electronics of Silicon

Electric conduction through a material is explained graphically by band diagrams, and one each for a metal and a semiconductor are shown in Fig. 4. Conduction is carried out by mobile charge carriers (electrons and holes) contained within one of two electric bands: the

Figure 4 Band structure of a metal and semiconductor. E_C is the conduction band, E_F is the Fermi level and E_V is the valence band [10].

valence band, which is lower in energy and contains filled energy states that render the charges there immobile, and the conduction band, which is higher in energy and predominately contains empty energy states that facilitate charge mobility. Conduction occurs when electrons go from a static state in the valence band to a free moving state in the conduction band. Unlike in a metal – where the valence and conduction bands overlap and thus charge mobility between them is unhindered – semiconductor bands are separated by a band gap. Electrons must be energetically promoted across this gap for conduction to occur (Fig. 4) [11].

To increase conductivity, silicon is often doped with atoms to increase the amount of free charge carriers. There are two types of doping. P-type doping infuses the silicon lattice with the Group III atoms of the periodic table; increasing the number of holes that settle near the top of the valence band and allowing easier conduction across the gap. N-type doping infuses the Group V atoms, increasing the number of excess electrons which settle near the bottom of the conduction band and also allowing easier conduction across the gap [11].

Within this band structure lies the Fermi level (Fig. 4). When not excited, electrons will preferentially rest at the lower energy states of a material's atoms, building up a congregation of electrons known as the "Fermi Sea" [12]. The top of this sea is called the Fermi level, and it is described as the highest energy state where an atom's probability of being filled is 50%. It is a rough approximation whereby all energy states of atoms below the level are filled with electrons while energy states of atoms above the level is predominantly the absence of electrons (or holes). In metals, the Fermi level is nearly always located in the overlap region between the valence and conduction band [11].

In undoped semiconductors, the valence and conduction bands are separated by a band gap, and the Fermi level is located in its middle (Fig 4). In doping the material, an addition of extra charges to one band in particular will move the Fermi level. Figure 5 depicts how; injecting more electrons (n-type) raises the level toward the conduction band, and injecting more holes (p-type) deflects it downward toward to the valence. In addition to doping, the Fermi level is sensitive to temperature (increased heat raises the energy of the Fermi sea), applied potential, and surface contact to a material with a different electronic makeup. Like a real sea, the level of the Fermi sea continually rises and falls according to external factors [10, 11]. Charge mobility within and between materials is dependent on these changes, and they are a crucial concept in the study of junction physics.

Figure 5 Fermi level changes by (a) upward shift for n-doping and (b) downward shift for p-doping [10].

Junction Physics of Silicon

The Fermi level is a metallurgical concept adapted for semiconductor use (hence its awkward location in the middle of a restricted region), and was done so to allow for consistency when describing what occurs when a metal touches a semiconductor [11]. An energy band diagram for such a situation is displayed in Fig 6. In addition to the elements introduced previously, the diagram shows the work function (Φ_m for the metal and Φ_s for the semiconductor), jointly defined as the energy needed to free an electron from a particular solid or the energy difference between the vacuum level and the Fermi level. In metals, this amounts to the same thing, but in semiconductors it is simply another useful notation – there are no electrons at the Fermi level [11]. After contact, the system must come to an equilibrium state by matching

Figure 6 Band diagrams for an n-semiconductor and metal (a) before equilibrium.

Electrons drop to lower state in neighboring metal to match work functions and, (b) after equilibrium, the band bending in the semiconductor [11].

work functions (an alternative way of saying the Fermi Levels must be equal). Electrons that are in an energetically higher state (in the material with the higher Fermi level), will tunnel across the interface and fill the lower energy states (in the material with the lower Fermi level). The act of changing the concentration of electrons moves the Fermi level, and it continues until the Fermi level in both materials is equal [10, 11].

After electron rearrangement, an electric field is created due to changes in electrostatic potential on either side of the interface. One side is predominantly holes, a result of empty

orbitals left behind when the electrons tunnel across. The other side is mostly negative ions, the result of electrons filling previously empty valence levels. The resulting electric field is in the direction of positive to negative regions. In metals, the presence of this field is dampened by the abundant availability of mobile charge carriers, so that no change in its band structure is seen. In semiconductors, however, the bands must bend to reflect these changes. The direction of the bend is dependent on the field created by the contact, a positive field bends the band upwards and a negative field bends the band down (Fig. 7).

Figure 7 Charge makeup and subsequent band bending of the Depletion Region in (a) n-silicon and (b) p-silicon [10].

The magnitude of the band shift is strongest at the interface (the area of greatest electron loss/gain) – this is the maximum energy difference from the Fermi level at equilibrium and is known as the Schottky barrier, ϕ_B . The effect of the metal diminishes with distance, and thus the bands going away from the interface are shown curving gradually back to its intrinsic state. The distance the band bends into the semiconductor (essentially how deep into the material the electric field reaches) is denoted as width, W , and is analogously known as the space charge region (because the region has a build-up of one type of charge) or the depletion zone (because the zone is depleted of one type of charge). The voltage drop across the space charge region is known as the built-in potential. This is a property intrinsic to all junctions, and its particular value is dependent on the work function of the two materials that are meeting [10, 11].

Schottky vs. Ohmic Contact

Under equilibrium, there are thus two things preventing current across the junction: the depletion zone, which hinders the movement of charge carriers, and the band bending, which

requires charge carriers to surmount an energy barrier. Overcoming these requires biasing each side of the junction and doing so can either increase or decrease these barriers; how so depends on the whether the junction is in forward or reverse bias.

Figure 8 N-semiconductor under (a) Forward bias. Notice that the conduction band shifts upward, thereby lowering the potential barrier. And (b) under reverse bias the conduction band shifts downward, thereby raising the potential barrier[11].

Consider Fig. 8, which is an extension of Fig. 6 after it has been placed under bias. Under forward bias, the n-semiconductor is connected to the negative terminal. The space charge region here is positive (band bent up); applying a negative bias will shrink the charge region due to recombination of charges, causing W to narrow. As W narrows, the bias will also cause the bottom of the conduction band to shift up, thereby decreasing the energy barrier an electron must overcome to move into the metal. With the effect of both obstacles drastically minimized, thermal emission is the final push that gives an electron enough energy to hop over the interface [11]. Conduction across this barrier thus depends on both the applied bias and the temperature of the solid, and current across a metal-semiconductor junction in forward bias can be calculated by the equation:

$$I = I_o \left[\exp\left(\frac{eV}{kT}\right) - 1 \right] \quad \text{Equation 1}$$

$$\text{Where } I_o = C \exp\left(-\frac{e\Phi_B}{kT}\right) \quad \text{Equation 2}$$

With the electron charge being e , the Schottky Barrier as Φ_B , C as some constant, k as the Boltzmann constant, T as temperature and V as the applied bias.

Under reverse bias, the n-semiconductor is connected to the positive terminal. The space charge region increases due to repelling of charges (positive bias on positive field), causing W to widen. The bands in the semiconductor shift downwards, thus increasing that energy barrier. The barrier change on the semiconductor side is immaterial, however, because it is the metal that connects to the negative terminal, and it is electrons on the metal side that need to be induced to move into the semiconductor. This involves biasing it enough to overcome the Schottky Barrier, Φ_B , on the metal side, but since the bands of the metal do not rise or fall like the semiconductor's, this is extremely difficult (Fig. 8) [11]. Conduction is essentially unobtainable in reverse bias.

Figure 9 Characteristic look of a Schottky diode. Current flow can only occur in one direction [13].

A junction that allows current more easily in one direction than the other is said to be rectifying, and will display a current-voltage (I - V) curve shown in Fig. 9. It can be seen that at reverse bias, indicated by negative voltage, there is very little current across the junction. There is current at positive bias, but the relationship is not linear but logarithmic. This is the effect of overcoming both the built-in potential and energy barrier in order to induce current. A rectifying curve is known as a Schottky Diode or Schottky Contact [11].

If the right materials are chosen, current is not limited by forward or reverse bias, which is to say it does not matter which side of the junction connects to what polarity of the terminal. This occurs when the Fermi level of the metal is sufficiently above the bottom of the semiconductor's conduction band (alternatively, the work function of metal is less than work function of

semiconductor). Electrons will flow from the material of higher Fermi level to lower, accumulating electrons on the semiconductor interface and bending the band downward. It can be seen that the bending does not hinder electron motility, since the conduction band of the semiconductor

Figure 10 Band structure of an ohmic connection before and after contact. The Fermi level of the metal is always above the bottom of the conduction band [11].

was initially lower than the metal even before contact [11]. At any configuration of bias, there is a clear pathway for electrons to pass between conduction bands of both materials (Fig 10). A junction with no barrier limit on either side of the interface is limited only by the intrinsic resistance in the materials, and conduction through the junction is given by the normal $V=IR$ relationship. This is an Ohmic contact, and its I-V curve is linear in comparison to the Schottky (Fig. 11).

Figure 11 A comparison of the i-V curve of a Ohmic and Schottky contact. The ohmic contact is linear because there is not barrier in the interface [13].

2.2 The Second Corner: Architecture

While the Materials Properties section focused on the electrical properties of silicon, one thing about the material itself bears stating – when working with it, there isn't just one type of bulk silicon. Variations in the types of silicon factor heavily when working with the material: it can be monocrystalline or polycrystalline, the crystallographic planes can be orientated in various directions, it can be doped in one of two types and at different amounts, it comes in different purities, can be roughed or polished at surface...etc.

Thus, there isn't one type of porous silicon either. Regard Figures 12 and 13, which is just a small sample of the many pore morphologies that have been created. Figure 12 are artistic representations, Figure 13 are scanning electron microscope images [1].

Figure 12 Artistic representation of pore types [1].

The fabrication of porous silicon has been described already as an inexpensive and simple process, yet extensive use of it by separate scientists has yielded widely varying results; the pores often come out looking very different. In fact, other than sharing a very general definition of an ordered series of voids and walls, pores can come in many different features and configurations that don't make it seem like they are at all related. The orderliness, however, is the key, as this is what is meant by the term architecture. Porous silicon must have an identifiable repeatable unit through its entirety, such that it gives the illusion that it was "designed" to have this integrity of structure. There is the sense the material was "architected" from the beginning.

Figure 13 SEM images of pores (labeled according to Figure 11) [12,13].

Here are some of the repeated aspects in the pictures that are readily describable: there are pores with smooth walls (Fig 12.1a) and pores with jagged, craggy edges (Fig 12.1b). Some pores drop vertically down in the material (Fig 12.2a), whilst others sink in diagonally (Fig 12.1c). Pores can be branched or branchless beneath the surface (Fig 12.1d and Fig 12.2a respectively). There are many different types of pores [14, 15]. As with any object with such wide variation, a taxonomic system is developed to classify and organize the results. For porous silicon, it was the IUPAC which developed such a system, but the material is so new – and the understanding of it still so much in its infancy – that this classification system comes off as crude and fairly basic. They're working on it.

Classification of Geometry and Morphology for Porous Silicon

A surface is ultimately determined to be porous if it is found to contain regions of pores. A pore is an etched pit in which its depth (d) exceeds its width (w). Once obtained, porous silicon can be described in terms of its porosity, thickness, pore diameter, pore density and microstructure [16].

Porosity – Porosity is porous silicon's most important property. It is defined as the ratio of volume empty space to total volume and can be calculated gravimetrically using the following equation:

$$P = \left(\frac{m_1 - m_2}{m_1 - m_3} \right) \times 100 \quad \text{Equation 3}$$

Where P is the percent porosity, m_1 is the initial mass of the wafer, m_2 is the mass after anodized etching and m_3 is the mass of the silicon after dissolution of the porous layer. Dissolution is performed by immersing the wafer into a 1.0 M aqueous solution of sodium hydroxide (KOH) [5]. A porosity of under 30% is considered low, 30-70% is considered medium, and above 70% is considered high [3].

Thickness – Thickness refers to the depth of the pores into the silicon. Mathematically, it can be calculated using the following formula [3, 16]:

$$W = \left(\frac{m_1 - m_3}{S \times d} \right) \quad \text{Equation 4}$$

Where W is thickness, m_1 and m_3 are the same as defined above, S is etched area and d is the density of the bulk silicon. The thickness can also be measured with imaging.

Pore Diameter – Pore diameter refers to the nominal distance between pore walls, and is grouped by the International Union of Pure and Applied Chemistry into three specific defined categories [3].

- If $2 \text{ nm} \geq$ then micropores
- If between 2-50 nm then mesopores
- If $> 50 \text{ nm}$ then macropores.

Pore Density – This describes the amount of pores within a given amount of space. It is somewhat related to porosity and pore diameter, in that each of those two numbers will effect this one, but the main information is the ability of the fabrication can create “initial removal sites;” the first surface dissolutions that grow into eventual full-fledged pores. A high pore density indicates that a large number of initial sites are present, which often leads to greater porosity [16].

Microstructure – Microstructure is a very unspecific category that essentially refers to any description of the pore surface that is not covered by the previous four terms; essentially any aspect that cannot be defined numerically. These may include questions of open-ended versus closed-ended pores, pores with smooth walls or pores with rough walls, branched or unbranched pores, and pore shape. Often the best way to convey microstructure is to use descriptive language or to show figures, like the drawing and description in Figure 14 [16].

1 Types of pores (a,b) blind, dead-end or 'saccate', (c) interconnected or branched, (d) totally isolated or 'closed', (e) 'through' pores.

FIGURE 2 Pore shapes (a) cylindrical, (b) ink-bottle, (c) funnel, (d) cuboid or slit, (e) triangular or pyramidal.

Figure 14 Description of pore morphology in (1) it is description of interconnectedness of pores while in (2) it is the shape of pores [3].

2.3 The Third Corner: Processing

As has been stated, the reason for the various morphologies is a combination of etching conditions and the chosen bulk, and the connector between the two is how the material actually forms, which is best described by examining the etching mechanism.

The Porous Silicon Etching Mechanism

Since its discovery, the exact method by which silicon became porous was a mystery that, over the years, has lead to as many proposed formation mechanisms as there are types of pores. This is not surprising. As each successively different pore type was discovered, each scientist who discovered it would posit his own explanation for how it came about; and the amount of mechanisms – some contradictory, some complementary to each other – grew in number. Today, a consensus theory is credited primarily to two scientists. Zhang et. al, who in the 1980's established that the reaction mechanism was electrochemical in nature, with current density and electrolyte concentration the two primary parameters. And Lehmann and Foll, who in the early 1990's argued that the dissolution of silicon happened geometrically based on doping and crystallographic properties of the semiconducting substrate itself. Together, the two theories consolidated the gap between how the etching solution, electrical activity, and solid material interacted with each other. When the influence of light on the process (a commonly observed phenomenon) was sufficiently able to be folded into this explanation, it was this mechanism that seemed most valid and became the one widely accepted [1].

Lehmann and Foll treat silicon etching by Hydrofluoric Acid (HF) as if it were a material undergoing corrosion. A graphical depiction a version of this reaction and its intermediate steps is presented in Fig. 15. The corrosion is driven by the presence of holes. Normally, silicon atoms on the surface are hydrogen or oxide terminated. If a hole reaches the surface, there is a nucleophilic attack on the silicon-hydrogen bond by the fluorine ion (Box 1). Once attached, fluorine creates a strong negative dipole moment toward itself, leaving the dipole's positive moment susceptible to another nucleophilic attack by the same species and using up another hole in the process (Box 2). If another fluorine bonds, H_2 is released from the silicon and an electron is released from the fluorine, the reaction thus creates a conducting current (Box 3). The two attached fluorines are extremely electronegative, pulling at the electron density of the remaining silicon-silicon bonds and making them susceptible to another fluoride attack (Box 4). Eventually the silicon atom is removed from the lattice altogether and forms a stable SiF_6^{2-} compound in solution. The newly exposed surface silicon ends' are protonated in the process [17].

Figure 15 Dissolution mechanism of silicon in hydrofluoric acid (HF) that leads to formation of pores. Two holes are used up in Boxes 1 and 2 [17].

Crystalline silicon is inert to HF under no electrical activity, yet the mechanism depends on holes reaching the surface. Thus the process can be thought of as similar to conduction across a junction – there is a need to get a certain charge carrier toward an interface, which in this case is the meeting of the silicon and the electrolyte [18]. This interface is treated like a

Schottky diode: the Fermi level of the electrolyte is always assumed to be in-between the valence and conduction band of the semiconductor, and an accompanying band bend and depletion region forms.

Figure 16 P-silicon under (a) no bias. Band bends downward. (b) Forward Bias, holes at interface lead to corrosion [18].

The etching process is called anodic dissolution because the silicon must always be the anode side of the reaction (attached to the positive terminal), so that the majority charge carrier will always be holes (otherwise, nothing reaches the surface to start dissolution). If the silicon is actually p-doped, this is not a problem, as the diode will be in forward bias. The lattice already contains an excess of holes that can be moved as soon as an electric potential induces it to do so (Fig. 16).

Figure 17 N-silicon in an electrolyte. (a) Illumination is needed to generate holes (b) Holes are then moved to start corrosion reaction [18].

However, if the silicon is n-doped, this is not as easy. As an anode, n-silicon would be under reverse bias. To generate holes, electrons would have to be excited from the valence

band to the conduction. This is done through illumination, which photovoltaically induces electrons to jump the band gap, leaving behind an excess of holes in the solid material [18]. Thus, shining a light generates the holes needed and the applied electric field contributes a force needed to push it across the junction diode, shown schematically in Fig. 17.

The I-V curves for both diode are shown in Figures 18. Notice that there are two curves, one for light and one for dark conditions, due to the photosensitive nature of the silicon.

Figure 18 i-V curves for n and p doped silicon in a diluted HF solution. The J_{ps} peak indicates the start of the electropolishing region and everything below said peak, shaded in gray, leads to a pore etching [19].

For dark conditions in p-silicon and light conditions in n-silicon, a series of small peaks occurs at very low positive potential. The first peak is known as the electropolishing current peak (J_{ps}). At potentials below this peak, the overall corrosion mechanism is expressed by the chemical equation [8]:

This was the reaction depicted in Fig. 15; the entire process uses two holes per removed silicon atom. Porous silicon is only formed in this initial exponential rise region up until the J_{ps} , or numerically $0 < i < J_{ps}$ [19]. These regions, with the pore formation region shaded, are labeled on Figure 18.

The second peak, seen at higher potential, indicates the beginning point of the electropolishing region. Because of the greater strength of the electric field, the density of holes that reach the surface in the potentials after the second peak is greatly increased. The corrosion reaction has a greater availability of holes for nucleophilic attack, and the corrosion chemical equation then becomes:

This reaction uses *four* holes to proceed – as opposed to the two holes in the equation stated earlier – and leads to a more complete and equal dissolution; in regions past this peak, the silicon is electropolished. This was the result Uhler and Turner had been expecting before they accidentally stumbled onto the porosity phenomenon, and underscores that anodically etching at low currents leads to porosity because it limits the amount of holes available for dissolution. As an aside, the regions between J_{ps} and the start of electropolishing is known as the transition region, and is characterized by a formation of an oxide that is needed for the electropolishing process [18].

There are two caveats. First, the values displayed in Figure 18 are not quantitatively absolute. The value of J_{ps} is dependent on the HF concentration and the doping amount, parameters that necessarily shift the values of i - V curves. Second, the curve is created with the assumption that the area being etched is constant. The controlling parameter here is *current density* as opposed to absolute current. Thus it may be more accurate to say that porous silicon will not form across a defined area unless the current density across the region is kept below J_{ps} , that area's particular threshold value [1].

Up until this point, the mechanism is fairly straightforward, describing how the electrochemical etching proceeds, but not explaining how pore configurations form. Once a bias

is applied, pores form because the etch rate vertically outpaces the etch rate horizontally, and the reasons why this occurs are difficult to resolve. The architecture of any layer may be a result of any combination of the following reasons: (1) The high radius of curvature at the tip of the pore generates an enhanced electric field that attracts valence holes preferentially here over the vertical walls (Fig. 19) [14, 18].

Figure 19 Hole movement is in the direction of the electric field. The majority of holes are attracted to a strong electric field at the pore tips. In (a) some holes penetrate into walls but in (b), the Space Charge Region in the walls prevents this [14].

(2) Eventually as the walls narrow, the depletion zone of adjacent pores will meet each other, resulting in vertical posts insulated from current flow (Figure 20). Silicon will continue to etch off at the base of the voids between the posts, but the posts themselves are stable, and become the walls of the porous material [1, 14].

Figure 20 Initial stages of pore formation and the depletion zones around each. As etching continues the depletion zones in adjacent pores begin to overlap [14].

(3) Since current is kept at a minimum, the depletion zone never disappears during the charge transfer process. The region changes with bias and is dependent on the geometry of the cell. The depletion zone is wider along flat areas (the walls), which insulates against charge transport and thus silicon dissolution. The depletion zone, however, is narrow enough at the curved

Figure 21 Diagram of the depletion zone (grey) during anodization of n silicon. The bottom of the pore has the narrowest depletion zone and the vertical walls the thickest [1].

regions of the pore tip for the electric field to overcome, and charge transport continues here (Fig. 21) [1, 14]. (4) As the width of the silicon posts shrink, quantum confinement widens the band gap of the material, leading to insufficient hole transfer (this is true of nanometer range posts) [3, 18]. (5) Fluorine may not be able to reach particular regions (especially true if the HF concentration is low and the pits are deep). These areas are not etched, and there may be formations in the pore layer that are attributed to this effect [18].

Silicon Etching Parameters

With an understanding of the etching mechanism, there is a sense that certain parameters exert control over specific parts of the morphology. While it is not the case that it can be predicted exactly what types of pores will be obtained during a particular etch, scientists have observed trends that have resulted from controlling various aspects during etching. A summarization between the parameters of an etch (with the exception of solvent type) and porosity is shown in Table 1 [19].

HF Concentration – If all other variables are constant, HF concentration controls the porosity and pore width: the higher the HF concentration, the smaller the pore width and the lower the porosity. HF concentration also controls the critical current density, J_{ps} , because HF determines the

amount of F⁻ ions in solution. If a low amount of HF is initially present, a higher current density is needed to facilitate etching. Low amounts of F⁻ present also leads to more defined pores (remember etching preferentially occurs at pore tips) [19].

Table 1 A generalization of etching parameters to pore characteristics [19].

	Porosity	Etch Rate	Critical Current (Jps)
<i>An Increase in...</i>			
HF Concentration	<i>decreases</i>	<i>decreases</i>	<i>Increases</i>
Current Density	<i>increases</i>	<i>increases</i>	-
Anodization Time	<i>increases</i>	<i>almost constant</i>	-
Temperature	-	-	<i>Increases</i>
Wafer Doping (p-type)	<i>decreases</i>	<i>increases</i>	<i>Increases</i>
Wafer Doping (n-type)	<i>increases</i>	<i>increases</i>	-

Solvent type – This is the solvent used to dilute the HF. Porous silicon is hydrophobic but organophilic, etching with HF and DI water as the solvent leads to the solution unable to penetrate into the pores due to high surface tension of water, this leads to poor pore propagation. Aqueous HF etching results inhomogeneous layers, high surface roughness and non-uniformity [9]. HF in ethanol has a much lower surface tension and penetrates into the pores easily, leading to high homogeneity. Most etching experiments must take the solvent choice seriously [19].

Current Density – So long as current density is kept below Jps, the surface will not electropolish. Within this range, it is thought current density controls the pore density and the etch rate, presumably by controlling the amount of holes that reach the surface [19].

Anodization Time – Etch time controls thickness and a longer etch time leads to a thicker layer, as silicon removal in anodic HF solution follows a linear relationship with respect to time. A longer etch time also increases porosity, as more new pores will start to be etched the longer they are exposed to HF [19].

Wafer Doping and Silicon Orientation – Wafer doping controls the types of pores that result. P-doped silicon, in which holes are in excess, will have greater areas of silicon removal. The

porosity of p-doped silicon tends to be high and the pores that result are often highly randomized, interconnected and “sponge-like” (Fig 22), which reflect the abundance of removal sites.

Figure 22 The sponge-like disorderliness of p-type porous silicon [3].

By contrast, n-doped silicon’s scarcity of holes tends to lead to layers that are highly ordered. In addition to the effects of light stated before, etching tends to follow the characteristics typical of silicon during electroless etching: with removal relying heavily on crystal orientation of the material. Silicon typically has an etch rate much higher along the $\langle 100 \rangle$ plane than in any other direction, because of the strained Si-H bonds there. This is a contributing factor in pores propagating in directions that aren’t straight down, (such as diagonally, shown in Fig. 23). Removal of n-silicon removal is much more selective and avoids the mass randomness of the pore networks seen in p-silicon [1,3].

Figure 23 Alignment of pores in different crystallographic n-silicon [14].

2.4 The Fourth Corner: Material Properties Redux

Through three sections, **2.1 Material properties**, **2.2 Processing**, **2.3 Architecture**, three of the four corners of porous silicon's diamond (Figure 3) are accounted for. Everything builds toward a function; the focus here is on the electrical one. This newly minted porous silicon is now treated as its own thin film layer, with a resistivity different from that of its crystalline counterpart. It is a change in this resistance that gives the layer its sensing ability. Despite the familiarity of the substrate material, however, electron transport through the porous silicon is complicated by a variety of factors, essentially to the point where mathematically predicted values of resistance, conductivity, capacitance, etc... are extremely difficult to calculate and rely on a series of assumptions that are different for nearly every study. Thus, the predictions have virtually no physical meaning, since the exact behavior of electrons at the quantum level through a layer of porous silicon is still unknown [3]. Nevertheless, recent papers have made large inroads into understanding the electron transport phenomena and have become crucial to understanding its potential as a sensor.

One way of modeling begins by looking at the most simplistic porous layer – straight walls, unbranched channels – from a two-dimensional standpoint. A schematic can be drawn similar to the one shown in Figure 24 [2]. When a voltage is applied laterally, the current will flow through bulk and pore layer in parallel, with the resistance of the porous layer higher than the resistance of the bulk. The reason for this is explained by modeling two adjacent silicon posts as parallel plate capacitors, with the space between them the dielectric. Current traversing through

Figure 24 Theoretical electrical diagram for conduction through a porous layer [20].

the pore layer has to overcome two barriers – the capacitance when hopping from post to post and the natural resistance of the silicon material inside the rods – on its journey from source to drain.

But there are many unknown factors which complicate this model and lead to uncertainty [3, 20].

- Porosity affects resistivity heavily. For low porosity, the amount of crystalline material is still abundant enough that conductivity is seen as behaving nearly identical to the bulk. For high porosity, the small dimensions of the remaining material (i.e. really thin posts) lead to quantum confinement and depletion of charge carriers. Quantum confinement constricts charge movement and now larger voltages are required to overcome this constriction, if it can be overcome at all. A lack of charge carriers, which may have been used up during anodic etching, may also make the layer almost entirely non-conductive [3]. Because of this unknown or outright lack of electrical activity, electrochemical porous silicon sensors are rarely designed for the nanoporosity range [20]. Instead, nanoporous silicon becomes extremely effective as an optical sensor, since the quantum confinement leads to large amounts of photoluminescence after application of light. The area has become a popular research focus for porous silicon [1].
- The non-uniformity of pores may have an effect. It is unknown how a layer that is rigidly ordered, where the pore spacing and posts are highly similar throughout, or non-ordered, where these dimensions are more random, affects the resistor-capacitor model.
- The connection and transport between the pore layer and the bulk. Since porous silicon is treated as its own thin film, the transport of charge through it into the substrate must also be taken into account, despite being the same material. Further study is needed to decipher how this happens.
- A space charge region building at all exposed surface areas, meaning it runs the length of the vertical pore walls, pore tips and all accompanying branches [3, 20]. The width of this region is dependent on the makeup of the ambient in and around the pores and heavily affects its capacitance-resistance values, becoming another barrier to overcome. It is this property that is exploited by electrochemical sensing: change the environment

around the layer, wait for the ample depletion regions to change accordingly, and measure the electrical difference.

- It is also unknown how charge carriers, once it enters the porous region, chooses which crystalline post to “jump” to next. There has been some speculation that the transport pathway is not straight toward the current drain, but can twist and snake its way through the layer (Fig. 25 [3]) depending on which pathway has the greatest attractive force and least capacitive gap. This may be related to the size of pore walls, the spacing in-between or other unknown factors.

Figure 25 Diagram showing the random “hopping” pathway of a charge carrier through a porous region. Each circle representing a “post” of silicon within a porous region. It can twist every which way while still heading in direction of an electric field [3].

- In quantum confinement, a post with a small enough width may have the depletion zone permeate entirely through the pore wall [3]. In such cases, lack of charge carriers makes the post entirely electrically resistant.
- Temperature. Thermionic emission, in which charge transport is moved thermally rather than electrically, has an unknown effect on the material [3].
- If the porous layer is to be treated as its own thin film, then it has an interface which contains a depletion region between itself and the crystalline material underneath, even if they are both made of silicon [3,8]. The existence of this layer has actually been heavily studied and soundly proved [3], although the nature of this depletion region is always difficult to predict in any way. From a basic science point of view, a region of sufficient width and a Schottky Barrier of accompanying height forms just like any other, and the individual values of these parameters and the direction of the band bending depends, as always, on the doping, charge depletion and depletion regions within individual walls in

the silicon that has become porous. Thus, while it was stated that the porous layer and the crystalline material form a parallel circuit, there is Schottky-like barrier for current going from one to another.

Combined, these reasons complicate modeling electrical activity of a synthesized layer, something that bears out in reported experiments. Canham cites that, for what is deemed low-porous silicon (usually in the meso to macro porous range), the general trend is resistance increasing with increasing porosity, because a greater volume of dielectric material requires more voltage to facilitate charge transfer. But in highly porous silicon (those within the nano range), resistivity can be orders of magnitude higher (up to $10^7 \Omega$) than its low porous counterparts [3]. This may seem counterintuitive, since larger surface area and smaller gaps seemingly decreases capacitance according to the resistor-capacitor model, but it can be explained by the aforementioned quantum confinement effect [3]. There are a small number of studies which use mathematics and computer simulation to preemptively model the porous silicon layer and the electrical sensitivity of this “chip” [20]. But they are exercises in theory. In building a sensor, even measuring baseline resistivity is difficult (as will be explained later).

Chapter 3: Addition of Catalyst

For this experiment, creating porous silicon serves as the support substrate, and is only one part of the dual system. The other part is the catalyst, which will cover the newly increased surface area and is meant to be the actual sensing species. Its plating will be described here.

One of the advantages of making silicon porous is that its high surface activity and electric conduction makes depositing this catalyst easier than comparably other materials. From an electrical perspective, deposition is the opposite of etching. Removing material required anodically biasing the silicon, but adding material requires treating silicon as the cathodic terminal [21]. Most catalytic layers are placed using a wet electrochemical process.

Electrochemistry at the Interface

Again, the interface between the semiconductor and the metal containing solution must come into equilibrium by a matching of Fermi levels and a bending of bands (Fig. 26). Another Schottky-like barrier is formed, preventing charge transfer. Deposition occurs by overcoming this barrier and transferring charge carriers (either holes or electrons) into an acceptor state of the solution (the redox potential of a metal/electrolyte solution) [21]. Since the silicon is now the cathode, there are two possible transfer possibilities: it will either accept holes into its valence band or transfer electrons from its conduction band; either will result in the capturing of a metal ion [22].

Figure 26 Band diagram illustrating mechanism of deposition of metal onto silicon (a) transfer of electrons from conduction band to acceptor state (the distribution curve). (b) Injection of holes into the valence band from acceptor state [21].

In n-silicon, there are enough free charge carriers in the conduction band that at forward bias, the barrier can be overcome and electrons will move across the gap; this is electroplating. For p-silicon, there can be no forward bias, since that would make the silicon anodic. Deposition is a cathodic process and thus a reversal of conditions, with the p-silicon (as opposed to the n-silicon seen in anodic etching) needing to be illuminated to photovoltaically induce electrons to jump the band gap and initiate charge transfer (Fig. 27).

Figure 27 Energy Diagrams for metal deposition in (a) n-silicon under forward bias.

Potential barrier is reduced and electrons transfer over to metal. (b) in p-silicon, there is no forward bias but illumination will generate electrons which will jump to conduction band for transfer [21].

Electroless Deposition Mechanism

For catalysts, the popular method is electroless deposition, which is the dipping of exposed silicon into an electrolyte containing metal ions (the immersion plating technique). Here it is not necessary to forcibly bias the wafer, as was done during etching. Noble metals are one of a small group that can be electrolessly deposited because the solution's acceptor level directly overlaps with the valence band of the semiconductor without any external bias. Electroless deposition has one other benefit: doping does not matter. If the redox potential was already within the valence band of the semiconductor, then band bending will not affect the transfer of valence holes, and the solution proceeds as seen in Fig. 26b.

The mechanism proceeds in a redox reaction similar in chemistry to an oxidation step. As is commonly known, silicon will undergo an oxidation process when in the presence of hydroxyl or oxygen molecules; the reaction is normally shown as follows [23].

If metal particles are present in an aqueous solution (as there will be in electroless plating) then it too can undergo a similar reaction; instead of the proton being reduced however, it will be a metal ion. Like such:

Where: [M] = Noble Metal

Obviously, there is a competing reaction between whether it is the metal or hydride that is getting reduced. Regardless, whichever species is reduced donates two holes into the silicon (see: Reactions 5 and Reactions 7), after which there are three possible outcomes, all of which are displayed in Fig 28. In (a), the holes are absorbed by the lattice and travel to another site, where it contributes to a silicon oxidation process (Reaction 3). Formation of oxidation hinders metal deposition, so most electroless plating solutions contain a bit of HF to etch off the newly formed oxide. In Fig 28(b), the holes migrate elsewhere and are transferred to an electron donor in solution. In (c), the holes are used up by the metal itself to reduce an agent in solution (due to their catalytic ability). In aqueous solutions, this agent is water and leads to the formation of H₂ gas (Reaction 5) [22].

The implications of the three pathways are that electroless plating is hard to predict and control, since it happens spontaneously. To complicate matters, the metal can be deposited in one of two locations. In the first, metal ions are able to be reduced on the surface of bare silicon, but the reaction rate for this step is slow. In the second, the metal ions are also able to be reduced on newly deposited metal, and this step is much faster. Shown visually, the mechanism in Fig. 28c is energetically more likely than Fig. 28a.

Figure 28 Artistic diagram of movement of various ions while electrolessly plating palladium [5]. In (a) holes contribute to removal silicon from the surface. In (b), holes aid in the oxidation of the silicon surface by capturing the hydroxyl electron donor. In (c), holes may be catalytically reduced by metal, leading to the formation of H_2 gas [22].

This leads to the metal that initially deposits onto the silicon being known as the “nucleation site.” Other deposits are then more likely to be reduced here and attach to this metal particle, rather than start a new nucleation on bare silicon elsewhere. As more metal builds up, this preferential depositing results in “islands” of catalyst growth. Layers plated electrolessly often have this 3D island character as opposed to an even coating [21, 22].

Thus, a quality deposited layer is one in which there is a large number of nicely spread nucleation sites – thereby most resembling an even coated thin film. Manipulating the parameters of an electroless etch to maximize these sites, however, is difficult. There is no way, as was done for the etching process, of relating specific parameters to eventual deposition results. The plating process only has four real variables: the amount of metal in solution, the pH, the amount of illumination, and whether there is an oxide present on the surface of the silicon. The metal and pH control the redox potential of the solution, and the more it bends toward the valence level of the silicon, the greater likelihood for charge transfer. The lighting only matters for p-silicon, as it is necessary to generate electrons in the conduction band. The oxide inhibits plating. Most experiments will manipulate these four variables recklessly in an attempt to get the best quality layer from them.

Chapter 4: Project Overview

4.1 Previous Work

All studies that have tried to create a catalyst/porous silicon layer have thus confronted a series of decisions similar to the ones shown on the flow chart in Figure 29. While all reported studies have used their own values for each of the parameters, one parameter remains remarkably constant in every sensor fabrication experiment in literature: the decision to always etch pores out of p-type silicon [6,7,8].

The reasons for this are clear after studying the etching mechanism: p-type etching is more dependable and leads, due to the nature of the layers that come out, to more exposed surface area. The results from such layers can be directly attributed to the forward bias of the interface, wherein current density and HF concentration are parameters that can be carefully controlled during the fabrication process. By contrast, n-type layers are under reverse bias and require illumination in order to be etched, a simple addition whose effects on the rest of the fabrication parameters is unknown [5]. With illumination, there may no longer be a clear relationship between current density and porosity, for example; nor is there a clear trend between the strength of the electrolyte and pore width. There is also a general lessening in surface area amount, meaning n-silicon gives up control and productive functionality. Seemingly, the addition of light casts a shadow on the rest of the experiment.

But there are disadvantages to p-type etching too. For one, the fabrication process involves more steps. Anodic etching requires the current to pass through the whole of the silicon wafer, entering through one interface and passing out through another. The interface we have been focused on, the interface between electrolyte and silicon surface being etched, is the front-side. Current leaves the wafer through this interface. Current enters the wafer through the interface between metal electrode and silicon surface, this is the backside. The direction of the Schottky on the back-side is always opposite the direction of the front-side (Figure 30). Since in p-doped silicon the front-side is in forward bias, the back-side is in reverse and to overcome it an ohmic contact must be made onto this interface. This back-side ohmic contact is critical and is usually achieved through a metal evaporation or physical sputtering process; adding an extra,

Figure 29 Flow chart summarizing the parameters that have to be decided upon when making a catalytic porous layer.

Figure 30 The circuit equivalents of etching for n and p type silicon. For both doped silicons, the diodes on the front and back side point in opposite directions. N-silicon requires illumination to overcome the metal-electrolyte reverse bias. P-silicon requires a backside ohmic contact to overcome the metal-semiconductor reverse bias [18].

potentially expensive, processing step before etching can even begin [6,7,8].

Another disadvantage, the higher porosity often results in more fragile, unstable layers. The sponge-like characteristics of p-type pores give thinner walls arranged in more random, less stable configurations. This has an effect on conduction through the layer. It also has two effects on the plating. The first effect, plating on thinner walls is more difficult. P-silicon is already energetically less favorable to have metal deposit than its N-counterpart, as light must be supplied to generate the necessary ions (**Chapter 3**). Less material leads to less light absorption and fewer nucleation sites, a perpetual problem in many reported studies. The other frequently reported problem: p-type layers often collapse when the catalyst deposits, due to the thin porous walls not able to bear the new metal [8, 24].

Another disadvantage, there is a low margin of error during p-type etching. Because the layers are so sensitive to the parameters, a desired layer could be ruined by even just the slightest shift of the accepted ranges. If the contact resistance is just a tad too high, or the electrolyte strength is a mite too low, or the etch time is allowed to go slightly too long, or the applied bias wavers even slightly, it could wreak large scale damage to the layer and ruin its ability to function.

4.2 Scope of Project

N-type etching could, hypothetically, avoid most of these problems. Since the back-side is in forward bias, it could get by without the back-side ohmic contact, provided a high enough

bias is supplied. Normally, a high voltage is to be avoided but a back-side Schottky has the advantage of being “self-limiting;” its high resistance prevents current from driving past the Jps point in instances where too much voltage is supplied. This simplifies the experiment: there is no longer a need to micromanage the voltage, and there is a larger range of usable voltages, because the setup and material itself provides a failsafe against current going overboard.

There are also structural advantages to an n-silicon layer. The walls tend to be more stable and thicker (this is the reason for the lesser surface area: the interior void space is decreased by having thicker walls), which could result in a greater number of nucleation sites (already helped by a material already more favorable to plating) and stronger walls to bear the additional metal. The resulting layers are not fragile instruments; they are allowed to dry in ambient and handled robustly without fear of instability.

Of course, going this route sacrifices significant control of the layer for ease of fabrication, which is an unacceptable trade if the layer could only perform within a specific set of resistivity values. But this has not been the case. The literature reports wide variations in layer resistivity, ranging from 10 Ω to 10 M Ω , without any hindrance in sensitivity. While there are some layers that have a higher sensitivity factor, no layer that has survived the fabrication process has been unable to sense due to its resistivity value; a failure to sense is usually attributed to another factor (such as poor catalyst plating) [6,7,8].

Thus, the lack of experiments using an n-silicon sensor is a bit of a mystery, as there may not be a discernible difference in ultimate performance. This experiment is an attempt at the alternative, an effort at fabricating an n-silicon porous layer plated with palladium as a catalyst. With this minor material change, the pre-etching process may be able to forego the need to sputter a back-side contact, the etching itself is eased from constantly worrying about voltage overload, the post-etching process could skip multiple steps (such as vacuum drying) that are performed to avoid damaging delicate layers and the layer itself has a potential for increased plating. With all this to be had without affecting any of the required sensor properties, n-silicon shows much promise.

Chapter 5: Experimental

The experiment consisted of three parts. The first was finding a way to make n-doped porous silicon layers worthy of becoming sensors. The second part consisted of making many copies of a worthy layer from the first part and plating them with palladium. In the third part, the plated layers from the second part were characterized according to their appearance and resistivity properties. Since all layers were made under identical specifications, these characterizations demonstrate the repeatability of the fabrication specifications, and serve to determine their suitability for sensor function.

5.1 Part I: Fabrication

The silicon wafers used were N-type, <100>, double polished with a resistance of 20 Ω cm. A self-made teflon cell that etches a 2 cm² circular area on the wafer was used. The wafers were cut into pieces sufficient to contain this area by the scribe and cut method. After a piece was cut, it was cleaned for etching by an ethanol rinse, then placed into the etch cell with aluminum foil as the backside contact. The aluminum foil covers the entire back side of the wafer. Together, sample and aluminum foil were sandwiched into the cell (Figure 31). The wafers were used as received; nothing was done to the either front or back-side.

Figure 31 Experiment setup: power source connected two sides of the etching cell.

Platinum wire is cathode, aluminum foil is anode (labeled).

Since n-silicon anodic etching is little tried, this experiment had to use knowledge about the etching mechanism and p-silicon parameter values from literature as guides for what to vary and what values to vary them by. For example, the mechanism explained how a Schottky on the back-side mitigates our ability to control current density through applied bias. Controllable parameters then become HF concentration, anodization time and light. The light used was the ambient in the lab room coupled with the light from the fume hood (front-side illumination), and was constant. Thus, the only remaining parameters to vary are HF concentration and anodization time. Previous literature used HF concentrations of 7%, 15% and 25% weight by volume in ethanol, which we followed. The HF is Alfa Aesar 99.99% metals basis at 49.5% grade. The ethanol is a Sigma Aldrich anhydrous mix consisting of 85.8% ethanol, 13.3% methanol and 0.9% MIBK. Anodization time was chosen to be 2, 4, 6 hours, respectively, based on early tests that established appreciable differences in the layer between these three times. The two parameters were varied with respect to each other, resulting in nine possible variations. A summary of the makeup and number of samples for each type of etch (all of them front-side illumination) etches are displayed in Table 2.

Table 2 The parameters for each of the 24 samples etched.

	Etch Solutions (% by volume)			
Anodization Time		7%	12%	25%
	2hrs	2	2	2
	4hrs	2	3	2
	6hrs	2	7	2

After the sample and aluminum foil has been sandwiched in, the chosen etching solution was poured into the electrolyte chamber and the electrodes connected to a power source. This results in a closed circuit loop being formed. The applied voltage must induce charge transfer across two key interfaces (Figure 30), both on either side of the silicon. One is the front side, the interface between the silicon and the electrolyte and that faces the light; charge travel across here results in etching into silicon. The other is the backside, the interface between the silicon and the aluminum foil in darkness; charge travel across here facilitates charge travel across the

silicon-electrolyte. At 20 Ωcm , the N-silicon chosen was a relatively low doped and high resistant; coupled with the presence of a Schottky rather than an Ohmic contact point on the back-side and this junction will let nothing but the smallest of currents through, even if the voltage supplied is very high.

Our fabrication setup is counting on this, but how high the voltage must be to get even this minimum of current had to be found by trial and error. The voltage was controlled and monitored by an Elenco XP-752A DC power source. As voltage was continually increased, the current was concurrently monitored by a Cen-tech P35017 digital multimeter hooked in series to the entire circuit. At some point, the current rises above the baseline and pores begin to form. For our setup, an applied bias of 6.8V was needed to push a total current of 30 mA across the cell. Over a 2 cm^2 area that is a current density of 15 mA cm^{-2} , consistent with reported results from other fabrication experiments.

Figure 32 Silicon as it is etching, notice the dulling of color on the sample piece (at bottom of the hole), which indicates reaction is working.

Initially, the experiment etched this way – testing different durations at different HF concentrations – because it was unknown if this fabrication process or any of the values in Table 2 would produce a usable layer. When it was verified that they in fact *all* produce one, it became necessary to find which layer was the most sensor-appropriate of the bunch. Since the plated layers were to be compared against each other, the porous layer underneath all had to be the same. Only one of the nine permutations would become the fabrication “template.” The biggest consideration by far was given to the layer with the maximum surface area – this is the property of greatest interest in porous sensing. No equipment capable of measuring surface area was available to us, however, so the assumption was made that greater porosity coincides with greater surface area. Finding porosity is a characterization process described below. The second consideration was stability of the layer, if the layer did not hold up well to being carried around or collapsed after plating then it was of no use. Stability was observed through imaging, also a process described below. The third consideration was ease and safety of fabrication. The argument for n-silicon layers is that it is relatively easier to make than their p-silicon counterparts, thus any steps that complicate that end goal is defeatist. How we arrived at the particular choice that we did will be discussed in the results, but the 12% HF/6 hr etch “square” was deemed to have produced layers with the best combined traits. This was duly recorded in Table 2, where it can be seen that that particular combination was made more than any other.

5.2 Part II: Plating

Five copies of the chosen layer were made and plated. Plating was performed instantaneously after completion of etching and without removing the piece from the etching device. This prevents a contamination of any dust or foreign elements on the surface and does not allow time for an oxide layer to grow. After anodization, the wires were unhooked from their connections to the cell. Most of the HF solution inside the cell was siphoned out using a pipette, leaving only a small amount (just enough to coat the top of the newly etched layer) of some HF present for etching off the oxide that develops during electroless plating. The plating solution was poured into the electrolyte chamber and left for 20 minutes. The plating solution used for this experiment was 1×10^{-3} M PdCl_2 and 0.04M HCl in DI water.

5.3 Characterization: Thickness and Porosity

The layers were characterized according to the IUPAC categories mentioned earlier. The porosity and thickness of the layers was determined by using the destructive testing method and the calculations Equations 3 and 4. It involves immersing the freshly etched, non-plated porous silicon in a strong aqueous base solution, which dissolves the porous silicon at a much faster rate than the crystalline silicon. A 1M aqueous KOH solution was made with 10-20% by volume ethanol added to ease surface tension. The freshly etched, non-plated, porous silicon was first dried under an N₂ stream after etching, weighed, and then placed into the dissolving solution. A vigorous bubbling appears during dissolution and the wafer was agitated to facilitate the process (Fig 33). Dissolution was allowed to go on until the bubbling stops or was noticeably weaker. Sample was then taken out, rinsed in ethanol, dried under N₂ stream and weighed.

Figure 33 Sample immersed in KOH for thickness and porosity characterization. Notice the bubbles emanating from the porous surface, an indication of the dissolution of the pores.

5.4 Characterization: Morphology

Obtaining images of the created layer requires a higher magnification than what optical microscopes can achieve and so was done using Scanning Electron Microscopy (SEM), which has an imaging range into the nanometers level. The SEM operates by rastering a high energy electron beam across the surface of a sample. Over each spot that the beam touches, the

Figure 34 Schematic of a SEM [25].

electrons interact only with atoms in the first few nanometers of the samples' surface, producing a signal that can be detected and interpreted into a topography of that surface (Fig. 34) [25].

The type of signal being detected is important, as there are several different species emitted when the electron beam hits an atom, and each species gives a particular type of information. For this experiment, the species detected was the secondary electrons – electrons knocked out of its atomic orbit by an incoming electron colliding with it at a high energy. Secondary electron detection is the primary method of imaging using an SEM because they are so readily emitted, provided the sample is conductive enough to prevent charge build-up at the surface due to the beam. Silicon is more than adequate a conductor for SEM analysis – even when porous – thus making this method the most suitable to inspect surface features. The pore diameter, pore density and morphology, both before and after plating, were determined using SEM.

5.5 Characterization: Electrical Resistivity

From a sensor standpoint, resistivity is treated as a characterization property – it is important to know, because the changes in this resistivity are the basis for the layer's sensing ability. But whether that resistivity value is actually the layer's "true resistivity" is unimportant. Ultimate sensing ability does not depend on resistivity being within any particular numerical range

nor does it matter whether the value is a truly the material's intrinsic resistivity; so long as a measurement method can find a number that can represent a base condition, and that same measurement method can detect differences from that base condition, the layer can function as sensor.

This is just as well, because complications of current travel through a layer (expounded upon in Ch 2.4) make it tough for any measurement method to declaratively state that their finding is the "true resistivity," there are always provisos to any value obtained. For this experiment, the electrical resistivity is measured using the 4-point probe method, chosen because of its close approximation to the lateral configuration of a typical sensor setup [Fig.35].

Figure 35 Recall a typical gas sensor configuration from Figure 2, the current source and drain are provided by metal contacts placed laterally across the porous layer [5].

Previous studies back calculated the resistivity by performing a voltage sweep across the two contact points placed laterally across the layer. Current enters via the source contact point, crosses that Schottky barrier into the porous silicon, continues on through the porous layer, and potentially crosses into the bulk by traversing the depletion region at the interface, before negotiating another Schottky barrier at the drain contact [3]. The i-V curves of these measurements resulted in, predictably, Schottky behavior and a single resistance number for the catalyst/porous system was obtained only by extrapolating from the curve and subtracting all the multiple barriers in the current pathway, a process that involved considerable mathematical guesswork.

The four point probe is arguably the best method by which to measure resistivity in the thin film system alone. It circumvents measuring the contact barrier between the electrodes and the porous layer, negating one of the problems from previous measurements. And its operation consists of limiting current to a low value in a lateral configuration (in other words, current flows

preferentially near the surface) – coupled with a thick porous layer and the natural barrier at the interface of the porous layer and bulk, and it is assumed that the other problem (current flowing across the bulk rather than the pore layer) is somewhat minimized. The mathematics from interfering barriers is not taken into account; the probe gives a simple reading across only one layer.

A four point probe consists of a row of four well-defined tips that are mechanically lowered onto the sample. A current is passed through the outer two tips, and the voltage drop is measured between the two inner tips. By separating the two measurements, the impedances of the contact points and wiring is eliminated (Fig. 36).

Figure 36 Schematic of a four point probe [18].

If the spacing between the probe tips is significantly larger than the thickness of the film *and* significantly smaller than the width of the thin film's cross sectional area, then the sheet resistance, R_s , can be given by the formula

$$R_s = 4.532 \frac{V}{I} \quad \text{Equation 5}$$

Where, V is the voltage measured and I is the applied current. The resistivity, ρ , is given by the formula, where t is the thickness of the film.

$$\rho = R_s t \quad \text{Equation 6}$$

For this experiment, a 4-point probe with 50 mils spacing between 5 mils probe tips was used to measure a thin film porous layer approximately 30 microns thick and with an area of 2 cm^2 . The applied current to the outer tips varied from between 6, 8, and 10 mA, as it is necessary to lower

this number for highly resistive samples. Ten measurements are taken in multiple locations within the circular 2 cm^2 porous area.

Figure 37 The four-point probe placed onto the 2 cm^2 circular porous area.

Chapter 6: Results and Discussion

The chapter on porous silicon used the concept of a diamond to explain the intricacy of the material; each corner representing one of four concepts (structure-architecture-processing-property). Now that the material has been put to some use, the four concepts are explained again, to see what has changed. The background chapter explained the basic science (solid state physics) first, in order to build to an explanation of an ultimate property (layer conductivity). But a results and discussion section goes in reverse; it is concerned first with data about the property in question (this is the result) and from it attempt to extrapolate the basic science (this is the discussion). So we will start at the top.

6.1 The Fourth Corner: Electronic Properties of Fabricated Layer

Of the 29 pieces of silicon subjected to this porosity treatment, five were sacrificed in the testing of the etching chamber and experimental setup, so 24 were available as actual results (their exact distribution shown in Table 2). Of these 24, 17 are used to characterize the porous layer at parameters other than the maximum; seven were actually etched at the magic combination (12% HF for 6 hours). Of these seven, the normal two pieces were used for electrical and physical characterization (which, recall, destroys the layer), and five overall were plated. Of these five...two worked, or showed signs of palladium plating.

First, layer conductivity is an indication of plating or non-plating. The resistivity measurements by four-point probe of the samples are shown in Fig. 38. The data is a scatterplot grouped by sample, with each dot representing one measurement on some location in the porous area. The control is provided by "Naked Porous Silicon," this is the resistivity of a layer that is not exposed to the plating solution at all, although it is etched at the same 6 hour, 12% HF/EtOH solution. Any samples with resistivity ratings that drastically deviate from the control is suspect to having metal additions on them. The data reveal a huge discrepancy (Figure 38). All measurements fall within one of two small ranges: an upper region of approximately 90-130 Ωcm that coincides with the resistivity of bare porous silicon, and a lower region of approximately 7-20 Ωcm , of which only Sample 1 and Sample 3 have points.

Figure 38 Scatterplot by category of measurements made by four-point probe. Each dot represents a measurement on some location. All samples etched at 6 hours, 12% HF/EtOH.

There is almost nothing in between, Sample 5 was considered, but later analysis showed it as only a bare layer with a slightly lower resistance than other bare samples. Thus, the explanation for the distribution in resistances is that there are essentially two, and only two, regions within our sample. There are the regions that plated well. And the regions that plated well plated uniformly well, to the point where the resistances of these areas all hover around the 7 Ω cm range (about half of the original wafer value) across two different samples. And then there are the bare patches, regions that did not plate, and the bare patches are uniformly bare, because their resistances match those of a porous layer that was not exposed to palladium at all.

Electronic measurements bear out the existence of an etched area able to carry charge across it, and two regions within that area of differing conductivity, with the only possible difference between them being that one must contain palladium and one cannot.

6.2 The Second Corner: Architecture

Electronic measurements give evidence of one region containing palladium and one region that does not. Confirming this conclusion – and explaining the disparate behavior between the two regions – requires studying another corner, architecture, which is revealed using visual imaging.

Visual imaging confirms two things. The first is that an actual porous layer is formed. Figure 39 shows what the surface of an n-doped silicon looks like after a four hour etch at 12% HF. At this low magnification, it is easy to see the surface is penetrated by an orderly series of holes or, by definition, porous silicon. At higher magnification, the IUPAC terms that classify architecture are able to be picked out and labeled, as they are in Figure 40.

The defining characteristic of our layer is its unique *microstructure*. It is unmistakable, either in the low magnification (Figure 39) or high magnification (Figure 40) images: the pores all pattern themselves into a “cross” or “plus” sign. These crosses are not of uniform dimension, some of the arms stretch out farther than others, and from a high vantage point there is a Mayan block quality about them: they look like the carved blocks that form the walls of that ancient civilization. Because of their size variation, it is difficult to define a *pore density* for our layer, and

Figure 39 Image of the surface of a 12%, 4 hour etch at low magnification.

Figure 40 Pore surface at higher magnification and with key features labeled.

we do not do so. Choosing a *pore diameter* is tricky, as the pores are not circular. Inspecting the layer at higher magnification, however, reveals that the crosses show scalloping: the walls of the crosses are not vertical but have a significant semi-circular, wavy pattern. The pattern is matched with its opposite wall across the void, meaning both were likely formed together. The directionality of the scalloping suggests a mechanism. An initial pit is etched into the surface, and from this pit, the pore grows by having spherical chunks broken off it, starting at the center and radiating outward. These chunks appear to radiate only in an orthogonal direction, parallel and perpendicular to the surface and each other. The larger the cross, the older its original pit, as its transept and nave have had longer etch time to lengthen. The scalloping is a vestige of a spherical chunk that detached itself, and their diameter appears to be around 1 μm . We take this to be our *pore diameter*. Layer *thickness* we identify by imaging a cross-section of the layer, as shown in Figure 41. These images confirm more of the scalloping seen in Figure 40, but now in vertical cut-away. In this view, it can be seen that pore thickness is as variable as pore density.

As a ballpark figure, the most prominent pores delve approximately 25-30 μm into the silicon, and this we identify as a typical *layer thickness* for a 12% HF, four hour etch.

Figure 41 Two images of 12% HF, four hour etch in vertical cutaway.

The second thing visual (SEM) evidence confirms: that palladium can be plated onto the surface. Fig. 42 shows what a successfully plated cluster of this noble metal appears like. This is one of the samples tested under four point probe (results in Fig. 38). Here, the same architecture is now coated over by a metal layer; in some areas so thick it covers the opening of the pores themselves. Higher magnification shows these palladium crystals attached to the n-silicon. It appears most palladium crystals are too big to penetrate into the pores (Fig. 42b).

The palladium seems to amass to itself, flocking together like alike-feathered birds. This phenomenon has been observed by other experiments (and written about in Chapter 3) and the penchant for palladium to clump together explains the disparity between the well-plated, less resistant regions and the more resistant, bare patches revealed by four-point probe. Hence our porous layer, despite using n-doped silicon that is energetically more favorable toward metal deposition (it is a forward bias reaction, Ch. 3) and having thicker walls and wider pores than porous p-silicon can achieve, is unable to seed enough nucleation sites to get an even palladium coating across its surface. It is unable to avoid the 3D island effect that is commonplace with immersion plating. It is unable to consistently get palladium to electrolessly deposit at all – only

Figure 42 Two images of a palladium plating (a) low magnification and (b) higher magnification.

two of five samples showed any detectable palladium – and the reasons why are unknown and a potential topic for further study.

The architecture affects the ability of this layer to carry current. Pure porous silicon shows a high resistivity (for our layer, about 90-120 Ωcm) and the difficulties that an electron traveling through it must encounter were elucidated already in **Ch. 2.4**. With the addition of palladium, the electron now has two potential materials it can traverse across, with an accompanying metal-semiconductor barriers when crossing between materials (Figure 43) [26].

Figure 43 (a) Current path through a Pd-Si layer (b) and its circuit equivalents [26].

Electrical current follows the path of least resistance. Palladium, with a material electronic resistance of $1.08 \times 10^{-9} \Omega \text{ cm}$, is that path. The current will take every opportunity to bypass traveling through silicon when it can travel through palladium, even if it means passing through multiple Schottky barriers along the way. In cases like Figure 42(a), where the palladium have stacked high enough to cover over large swaths of pore openings, the current may have a pathway to bypass the silicon entirely.

It is this easier conduction pathway that the four-point probe is able to pick up on and the reason for the lowered resistance in certain locations. It is unknown what this lowered resistance says about the quality or amount of the palladium layer itself; the 7-10 Ωcm range is very consistent, even if the locations where those readings occur are random. It can also be said that

there is no single 3D island of palladium large enough to span the entire 5 mil spacing between the four-point probe's probe tips; if there were, the resistance would be that of just palladium. The current must cross at least some porous silicon. The palladium layer is hard to place definitive conclusions on – sometimes it plates and sometimes it doesn't, and it plates in some places and not others, and when it does there is at least some evidence that its signature islands are somewhat limited in size – but if it is present, it gives a noticeable electrical and visual signal that it is there.

An argument for using n-silicon is that the thicker walls would be less susceptible to cracking or crumbling in either its natural state (when capillary pressure could stress it to do so) or when plated (when additional weight overcoming its natural strength causes the same). With no need for delicate handling during the fabrication process, visual evidence shows the whole of the etched region, once a previously planar surface, now densely pockmarked with identifiable, repeatable pore units. Successfully plated samples show this vast porous surface broken by islands of palladium that, clumped together, are the reason for the difference in electrical activity found during electronic measurements. The images are remarkably homogeneous; no layers show any jagged edges, partially collapsed walls or scattered silicon debris that would indicate cracking or crumbling. The layers show no instability.

6.3 The Third Corner: Processing

Everything about our layer so far – the way it performs electronically, the way it looks architecturally – indicates a potential to carry out sensing functions. Seemingly there is something about our fabrication process that is of merit. That process was the result of our choosing a value for two particular parameters: HF concentration and etch time; a decision that came after extensive testing showed what varying the two actually did to our layer.

Deciding on a single etch time depended on establishing a relationship between the time of etch, the porosity of the layer, and the pore depth of the layer. **Chapter 2.3** had established how all three were related. **Chapter 5.2** detailed the destructive testing method needed to find porosity and pore depth. The results of these tests are shown in Figure 44, which plots

Figure 44 Scatterplots of (a) Calculated porosity and (b) Calculated pore depth with respect to etching time and grouped by HF concentration.

calculated porosity and calculated layer depth against its respective etch time (and grouped according to HF concentration). Figure 44(a) shows porosity is indeed controlled by etching time. Specifically, porosity rises with etch time, with the average maximum porosity after a six hour etch calculated to be $63 \pm 6\%$. Figure 44(b) shows pore depth is an extension of porosity and has a similar relationship; like porosity, the general pore depth increases in proportion to etch time. The pore depth calculation can actually be verified by comparing a calculated result with a cross-sectional SEM image from the previous section (Fig. 41). Those images show a four hour etch in

which the most prominent pores have a depth at around 25 μm , while the calculation of a four hour etch comes out with pore depths at around a 15-25 μm range (Calculated Average: $19.3 \pm 3.0 \mu\text{m}$). For pore depth, the data and calculated values are close enough to match, thereby validating Figure 44(b). There however is not a similar way to validate the porosity calculations the way we did with pore depth, but nevertheless we accept the validity of our numbers and take the 63% porosity as our maximum. Since the greater the porosity the better the sensor, all palladium plated layers were thus specified to be from six hour etches.

As for HF concentration, in **Chapter 2** we wrote, "*If all other variables are constant, HF concentration controls the porosity and pore width.*" If this were true, however, Figure 44 would show a clear delineation between the HF concentration groupings within each column. That Figure 44 does not show this, instead having the data points so jumbled together that it is difficult to differentiate between any groupings, points to a lack of a trend or connection. HF concentration has no effect on ultimate porosity; nor does imaging of any layer etched past two hours show that changing HF concentration has any effect on pore width.

Instead, imaging of layers before two hours show an entirely other effect: HF concentration affects the speed of pore initiation. Figure 45 shows the surface of the silicon after 30 minutes of etching under the three differing etching solutions. Fig. 45A is not even an SEM image, but taken with an optical microscope, Fig. 45B and C are taken under SEM. In 30 minutes, the 7% solution did little more than mildly roughen up the surface, in no specific configuration, with no presence at all of pores. The roughened surface is on a scale large enough to be discerned by an optical microscope. In the same anodization time, the 12% solution did much the same, but now the roughening is on a scale smaller than the 7%, and is faintly perceived by SEM, but only at very high magnification (indicating the surface is still very planar); still no sign of pores. But for the 25% concentration, at the end a thirty minute etch, the SEM is able to pick up the presence of holes on the surface (at a magnification lower than the 12% images because the pits are now bigger); no uniform sizes and it is unknown what their depth is. Because all the surfaces develop into the cross-like appearance eventually, the holes seen here must be the initial pits. Evidently, in higher HF concentration this initiation just

happens faster. Even without magnification imaging, this could be seen with the naked eye. Surfaces etched with greater HF concentrations darkened noticeably quicker.

Figure 45 Etching surface after 30 minutes of (a) 7% HF in ethanol, (b) 12% HF in ethanol and (c) 25% HF in ethanol.

But despite starting quicker, the layers don't tend to show much difference in any other feature. For example, while it is true that samples etched in 25% HF start forming pores earlier, there is no correlation between that concentration and a finished layer's pore width, pore depth or pore density. It seems at some point deep into anodization, the etching rate gradually evens out. Because of this, we chose to use 12% HF for all samples to be palladium plated. This concentration is a more economical use of HF (using less for much the same result), and more timely in indicating whether a particular sample is etching at all (the lowest 7% HF solution takes

too long to start initiating. For a multi-hour etch it's better to know earlier if the surface is darkening – signifying pores – as to not waste time).

6.4 The First Corner: Material Electronic Properties

The two processing parameters are not the only thing affecting the final porous layer. The etching process is an electrochemical reaction driven by the conductivity of the silicon. It is this innate material property – the most fundamental of the four corners – upon which the entire experiment depends.

The current through the entire circuit is measured at 30 mA. Since the load was supplied by a DC power source, this gives the impression that the current was also DC in nature. Monitoring, however, reveals this as not accurate: current across the cell is not constant, but

Figure 46 A log of current across cell taken every second.

actually fluctuates. Figure 46 is a graph of absolute current with respect to time recorded during a 300 second time period. The 30 mA value is not constant but turns out to be a maximum; in some instances there is no current through, in some instances 10 mA and 20 mA. We assume the accuracy of the multimeter's readings. That is, this is not noise but an indication of a pulsating nature to our anodization current. Our closed-loop circuit involves a triple interplay between the backside contact (in forward bias for n-silicon), the front-side interface (in reverse bias for n-silicon) and the illumination on the front (photochemically active). The data reveals a

telling behavior (to be explained later) about the complexity of such a setup. Such an assumption is made with the knowledge that the data is limited by a crude measurement method. The sampling rate is at 1 Hz (once per second) and the measurement is limited to 10 mA increments, the quantization limit of our digital multimeter. Electrical data, of course, is normally measured with techniques and on a scale much more refined than this, but we were limited to the means at our disposal, and we believe this method suffices for what we are trying to show. The accuracy is there, even if the absolute precision is not.

With every new porous layer, each scientist would posit his own mechanism for how it came about based on an accumulation of all data and observations from the four corners of the diamond. Since we have just finished such an accumulation, it would be remiss to not contribute one of our own.

For that we refer back to Lehmann who, recall from **Chapter 2.3**, is a key figure in the modern understanding of porous etching mechanics. Lehmann put great emphasis on the electrical behavior during the anodization process, his work meticulously mapped out how electropolishing current peak (Jps), concentration of p-dopants in the silicon, HF concentration in electrolyte, applied bias and current density changed in relation to each other. Lehmann found he could not do this for low doped, illuminated n-silicon (which is our material) – for these samples the bias and current density became decoupled [5]. Whatever was inducing current in these situations was not following normal junction behavior.

Instead, Lehmann suggests current in these experiments is most likely due to avalanche breakdown, the phenomenon wherein the bias in a reverse biased junction is so high that free roaming electrons gain sufficient kinetic energy to knock into electrons of other atoms, exciting them from the valence to the conduction band and creating a new electron-hole pair in the process. The newly created ions are themselves affected by the electric field and are accelerated toward an electrode (holes toward the cathode, electrons toward the anode). Generated charges cross over from side to side of the interface, caroming into other electrons on the way and knocking them into the same excited state. This starts a chain reaction, leading to the

“avalanche” effect stated in the name (Fig. 47) [11]. As collisions multiply rapidly, the increased internal energy induces the material to heat up uncontrollably and cause both materials irreparable harm. Normally, this means avalanche breakdown is to be avoided. But etching silicon consumes charges (Reaction 1 and Figure 14). Here both sides of the interface, electrolyte and semiconductor, are protected from the avalanche effect by the corrosion reaction that happens where silicon, fluorine, holes and electrons meet [5].

Figure 47 Representation of the behavior of electrons during avalanche breakdown [11].

With this mechanism, much of our data is explainable. In the beginning, an electrolyte of a particular concentration HF in ethanol and silicon with a particular concentration of n-dopant is placed in contact with each other. The n-silicon is positively biased, an anode, and the electrolyte is negatively biased, a cathode and this means the junction itself is under reverse bias. Biasing the electrolyte forms F^- ions and illumination on n-silicon generates holes. But there is another generator of charged ions. At 6.8V, the voltage is so high as to induce avalanche breakdown and cause a small current, at any value between 0-30 mA, to flow across the cell. Many of the charges generated by either method are consumed in a corrosion reaction at the electrolyte-silicon surface; silicon is etched off in this instance. This constant gain and loss of charges is the reason for the fluctuating electrical current documented in Fig. 46. The n-silicon is the limiting factor in all of this, as holes are a minority carrier for this material. Their scarcity – in addition to the corrosion reaction – limits avalanching, keeping current at a minimum and preventing runaway thermal breakdown no matter how high the voltage gets [5]. Thus, while bias may indeed induce current, the material itself decouples any relationship it may have had with it.

The n-silicon is also responsible for the decoupling the relationship between HF concentration from porosity and pore width, leaving it to control only the speed of pore initiation. Again, holes are the minority carrier in n-silicon. But at the start of anodization, before pores have begun to form, there is a double supply of holes generated by two separate methods, illumination and high bias. Here concentration of HF matters, because the amount of holes may exceed the amount of F⁻ ions to deal with them. Fluoride is the limiting factor. As the pores grow deeper into the material, the light is not able to penetrate as far, and the holes generated from illumination cease. Here concentration of HF is irrelevant, because the F⁻ ions exceed the amount of holes available to react with them. Presence of holes becomes the limiting factor. And this is consistent with our observation: despite higher concentrated HF electrolytes showing faster pore initiation, the ultimate porosity and pore depth of our layers turned out to be the same. After the initial burst, the etch rate between all electrolytes even out. Over long, multiple hour etches, the differences from that initial burst become negligible.

Even the hallmarks of our architecture – porous layers' tens of microns thick and pores in the appearance of a plus sign – are revealed to be just another result dictated by the material chosen. The observation is that the pores radiate from a central point in directions parallel and perpendicular from each other (**Chapter 6.2**), with vertical pores being longer and wider than the horizontal ones. The verticality is not a surprise. For a <100> wafer, the <100> direction will etch at a faster rate due to (1) the planar density being lower here than in the <111> direction – with a lower density, fewer atomic bonds need to be broken and the atoms on this plane etch off comparatively quicker – and; (2) steric placement wherein the <100> direction has greater exposure to etchant and thus greater dissolution compared to the <110> direction [5, 18]. Normally, these two factors would lead to a porous layer with steep vertical walls, modest porosity and not much else, but the electrical activity during our etching process produces significant differences.

That electrical activity is avalanche breakdown current and it is – for reasons beyond the scope of this project – known to be maximum along the <100> plane [5]. This current movement causes holes to concentrate along any exposed <100> face; so while initially there is only silicon

dissolution in the vertical direction, the walls of the pits become newly formed interfaces that also have a buildup of holes, and they soon too become susceptible to fluoride attack. Branch pores are the result of this. There can be many branches stemming from a single parent pore, they grow horizontally while the pore tip of the “root” continues vertically, and their growth is stopped by encountering the depletion region of a neighboring pore [5]. Thus the anisotropic dissolution rate, already faster in the $\langle 100 \rangle$ plane because of the diamond cubic lattice, is only accentuated by the electrical behavior; and together the layer’s porosity increases and its morphology changes due to both factors. This morphology, a branching along the $\langle 100 \rangle$ plane, is the distinguishing characteristic of our etching process; it is a form of branching Lehmann called “spiking” [5]. We had called it “Mayan Block-like” in **Chapter 6.2**, and had deduced a similar mechanism for it using images alone. By taking into consideration the material used and the electrical data collected, the mechanism is expanded into a more detailed explanation.

Through this mechanism, we can see that many of the parameters that vex p-silicon etchers have little bearing on us. Testing different HF concentrations show there is no need to be concerned over HF concentration. Tracking current shows no need to obsess over the Jps point, nor obsess over keeping current density under it. There is no hovering over the voltage dials, fretting over the slightest change. There is no backside sputtering, trying to create the perfect ohmic contact point. N-silicon, through its innate electronic properties, forms pores mainly of its own volition, and this greatly simplifies the work that goes into making it. And that, if you can recall, is the purpose of this experiment. Here is our statement, restated from **Chapter 1**:

“The goal of this project is to describe a fabrication setup capable of creating a sensing layer that is of this dual catalyst/porous silicon combination... the experiment attempts an easier fabrication method than what is usually required when making layers of this type.”

Chapter 7: Conclusions

Figure 48 The intertwined nature of the materials diamond. Every corner affects every other corner.

The idea to use porous silicon as a gas sensor is so nascent, so in its infancy, that the number of designs – and descriptions of how to make these designs – are very small in number. Basing a design on n-doped silicon, as this experiment does, had not even been attempted before. It was our intent to examine whether the creation of this layer was even possible.

To do this, we followed the approach of experiments past, even if they were tailored for p-doped silicon etching, because they based themselves on a core philosophy of materials science. Materials science uses the triangle concept as more than just a way to organize a description of a material; it can also be a guide to thinking through an experiment. How, for example, changing one corner of the triangle in turn affects all the others (Figure 48). For an architected material such as porous silicon, early research has kept this simplicity as its guiding principle: if the processing and only the processing corner is being changed, then the observable effects on the corners of architecture and property are all attributable to how the processing was done. The underlying material, silicon (representing the atomic structure corner), is unchanged and unaffected, and this simplifies any cause and effect questions that may arise from the results.

We dutifully followed along with this line of thinking, attempting to obtain a sensing layer by methodically testing different processing parameters and picking a resulting layer that came out best. The ideal layer turned out to average $63 \pm 6\%$ porosity with $1 \mu\text{m}$ width between pore walls and pores that are cross-shaped in visual appearance. Palladium onto our layer is achievable and plated regions show a layer resistance of $7\text{-}10 \Omega \text{ cm}$ – well within the range other experiments have established as acceptable for sensor function. The presence of these regions show it is possible to design a palladium/porous silicon hybrid layer with n-doped silicon as its base.

But we only proved it possible. There are issues that prevent our layer from being truly usable and improving upon them will be a key area of future work. The first issue is the quality of the palladium plating. The layer we arrived at was too unpredictable: plating randomly, in random amounts and in random formations. To apply the logic of the materials triangle: if the properties are too unpredictable, then the processing must be too unpredictable, and a better way of processing must be found. This could mean a technique different from the wet electroless method we used, but it could also mean a more involved look into electroless plating itself. All our plating was done using only a single solution; we were simply trying to prove deposition in this way is possible. But a more methodical approach, using the principles of the mechanism behind electroless plating (described in **Chapter 3**), could be the basis for a more in-depth examination into how the quality of a plated layer changes depending on the compositional makeup of the plating solution. It is a question that warrants future study.

The second issue is the loss of control: fabricating n-doped porous silicon requires a willingness to allow the properties of pore width, pore depth and microstructure to be dictated more by the silicon's innate electronic properties rather than the processing parameters (per mechanism explained in **Chapter 6**). Ceding processing control over the particulars of a porous layer, for a technology based on porous layers, is an understandably hard sell and the reason n-doped silicon is often discarded as a viable alternative. But the loss of control is not really a loss at all; those properties are simply ruled by another corner on the diamond – the materials structure corner. This is a corner researchers actually have control over, as they pick the material

that is being etched. Thus regaining control is a matter of upending of the current guiding principle – that porous silicon is controlled by processing alone – and a simultaneous replacing of it with another expanded version: what would occur should *two corners* on that architected materials diamond be changed, and what eventual properties will be attributable to which of the two corners?

The connection between the material substrate and its anodic etching processing has always been known, we mentioned it in **Chapter 2.3**, but had previously been willingly neglected in the interests of simplicity. That is, the idea to use porous silicon as a gas sensor is so nascent, so in its infancy, that research into designing it hasn't even progressed to the point where both processing and materials selection are taken into account. Should future work attempt this, perhaps the amount of ways to make a porous silicon sensor – and the amount of things it can sense – will grow to become a list full of silicon in all its p and n doped varieties.

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