CONSTRUCTING AND OPTIMIZING A SINGLE WAFER SOLAR CELL ARRAY
IN THE MICROFABRICATION LAB AT CALIFORNIA POLYTECHNIC
STATE UNIVERSITY AT SAN LUIS OBISPO

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ABSTRACT

Constructing and Optimizing a Single Wafer Solar Cell Array in the Microfabrication

Lab at California Polytechnic State University at San Luis Obispo

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Solar cells are more and more becoming a significant source of energy in the world today. They are used to power entire buildings as well as small devices and everything in between, and are utilized all around the world. Smaller solar devices, such as hearing aid battery chargers, cost a lot of money relative to the monetary wealth in third-world countries. For this purpose, a less expensive, more efficient solar cell array should be developed.

This study contains research that details all aspects of how solar cells work. It also details three years' worth of studies at California Polytechnic State University (Cal Poly) that attempt to fabricate a solar cell array on a single wafer.

Two tests were carried out that will help determine the optimal attributes of the solar cells. The first compared a solar cell made on a 10 μm thick silicon on insulator (SOI) wafer to solar cells made with the exact same masks on a 500 μm thick wafer. The thicker solar cell had 2.5 times the maximum power as the SOI solar cell. Aspects of the solar cell that would need to be improved are: increase thickness to between 70-100 μm from the SOI thickness, texture the front surface, add a passivation layer on the front surface, decrease the contact resistance for the metal electrodes, and add in a rear reflector. The next test was all about analyzing the metal contacts and interconnects.

Ten gold-silver filled epoxy-gold bonds were constructed and measured ten times each, giving a grand mean between 10 and 11 Ω . Another short test was run with a commercial solar cell to characterize the change in power based on the series resistance. It was discovered that the both the epoxy and the gold add too much to the resistance. To fix this, a silver solder-like paste and a thicker contact metal should be used. There is also a derivation that details the design of a top contact layer that optimizes the finger spacing and finger width based on other solar cell factors. With the materials available at Cal Poly, a solar cell array can be fabricated on a single wafer. When accounting for the materials and processes available to the scientific community as a whole, a very effective and efficient solar cell can be fabricated.

Keywords: Solar Cell, Semiconductor, Band Gap, PN Junction

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1 INTRODUCTION

1.1 Motivation

One of the biggest concerns in the next few years is the growing difficulty of finding sources of energy. Natural deposits such as petroleum are running out and can't be recreated (Roberts, 2008). Another is growing fear of pollution, especially carbon dioxide being released into air from traditional fuels (Roach, 2007). There are numerous proposed solutions for finding new sources of energy and finding ways to reduce the amount of pollution people put into the environment. One solution that can greatly benefit both issues is solar technology. Using only light from the sun, a solar panel can provide electricity with no emissions aside from what it took to create it (Kasap, 2006).

Solar science is a field that has been growing for years. It is currently branching out and being utilized in new applications that have not been feasible until now. Examples include organic solar cells that could be painted onto nearly any surface (Nobel Media, 2000), large band gap inorganic material solar cells (Wu, 2011), materials with tunable band gaps (Wu, 2011), and multi-junction solar cells (King, 2007). Research is being done to make devices such as electric cars or airplanes able to run on only solar power (Ghose, 2013). By far the most common solar cells in use by number are made of silicon, either single- or polycrystalline, which are currently used on rooftops of private and industrial buildings, as well as for smaller devices such as rechargeable lanterns and cell phone chargers (Locke, 2008).

This study focuses on characterizing a fabrication process for a silicon solar cell that would be useful for recharging small power batteries. The example that will be used in this study is rechargeable batteries for hearing aids. While there is not likely a significant market for such a device in America, since batteries can be recharged by plugging them into a wall, third-world countries and places without electricity would greatly benefit from using the sun to ensure that they can continue to hear. It would likely be a small device that could attach to a hat or outside of a pocket and would recharge the battery during the day, every day.

Devices such as the one described in the previous paragraph do, however, already exist (World Health Organization, 2013). Such a device would be easily affordable for a first-world country, but expensive for impoverished countries. Unfortunately, these impoverished countries need the technology more than anywhere else in the world. This study focuses primarily on determining a more efficient way of fabricating the actual solar cell component in the device, with the intent of reducing the total price and making solar technology more accessible to communities around the world that need it most.

1.1.1 Benefits to Third-World Countries

According to the World Health Organization (WHO), approximately 200-400 million people living in developing countries are hearing impaired, with half of that amount again in developed countries. Unfortunately, neither the hearing aids themselves nor the batteries that power them are cheap. The least expensive hearing aids commercially available are as low as \$165, though some cost as much as \$3,000. Furthermore, replacing batteries for them costs around \$20 or more a month. This cost

does not decrease over time and will never stop being necessary. In America, recurring costs minimally deter people from using hearing aids. However, in third-world countries, the hearing impaired are rarely able to cope with a recurring cost of any amount.

Regardless of location, hearing disability is a big problem for children who need to be able to hear in order to attend school. Without the ability to hear, they are denied the opportunity to be educated and their ability to get a job later in life is severely impaired. Likewise, adults with hearing problems who are not able to afford to get batteries as needed are often not able to hold down a job, which creates a feedback loop with their inability to buy hearing aid batteries. Clearly, a cheaper alternative is needed.

One way that this problem is being combated is through the utilization of solar energy to recharge hearing aid batteries. While not many of these devices exist, the Solar Ear, developed by Howard Weinstein, recharges hearing aid batteries that can be discharged and recharged daily for a period of 2-3 years (World Health Organization, 2013). Over that two to three period, batteries alone would cost upwards of \$300 in replacement, which a solar charging device would completely nullify. Conversely, the batteries sold by the Solar Ear company cost only one dollar.

The flip side to the non-existent continued cost is the up-front cost of buying a device that recharges the hearing aid batteries as well as the hearing aid itself. The Solar Ear company, through buying parts at cost, is able to produce a hearing aid that is available for \$40. This price includes the solar charger as well. Part of the reason that Solar Ear is able to make these hearing aids available for so cheap is that they are a non-profit, non-government organization that is concerned with meeting the medical needs of people who cannot afford their own care (World Health Organization, 2013). While

there likely are ways to reduce the price of the hearing aid itself, this study only focuses on the physical solar recharging device. Even though forty-one dollars is quite low for a hearing aid and battery, the fabrication of a cheaper recharging unit means that more units can be provided to more people for the same amount of money.

1.1.2 Characterization of Cal Poly's Solar Cell Production Capabilities

One purpose of this thesis is to define the different aspects of solar cell fabrication that will result in the most efficient possible cell. Ideally, the research presented here will benefit the fabrication of the microfabrication lab at Cal Poly in the future. This study refers to many factors that affect how well solar cells work. In order to finely control some of these factors, some very sophisticated equipment is needed that is not available at Cal Poly. Thus, two purposes of this thesis are based on the one previously mentioned. Specifically, this study will 1) seek to find the ideal aspects of a solar cell that is physically possible to create and 2) discover the closest to ideal that is possible with the resources in the Cal Poly clean room.

1.2 Background Science

Photovoltaic cells, commonly known as solar cells, are devices made of a semiconductor that produces electricity by converting energy from sunlight. Due to the presence of a distinct junction, they have the ability to conduct current in one direction through an external circuit. Solar cells, at present, typically reach around 20% efficiency, and as such are considered a viable source of energy for larger power applications such as providing electricity to a house or industrial building. They have recently become popular, and are gaining popularity, in smaller applications such as recharging flashlights

or mobile devices (Locke, 2008). This study will focus more on the latter application, since a solar array constructed from one wafer would not be beneficial for high power applications. High power applications, such as a solar powered airplane or housing units, require a large amount of area to absorb more light and produce more current. In that case, a whole wafer is made into a single solar cell instead of an array.

This study utilizes silicon as the photosensitive material. Silicon is the most commonly used semiconducting solid today, and has probably been studied the most as well (Locke, 2008). For this reason, it is a good material for testing a proof of concept device, such as a silicon on insulator (SOI) solar cell array.

1.2.1 Silicon Doping

Silicon has a diamond cubic crystal structure. Each atom in the lattice is attached to four other atoms at equivalent angles (109.5°). As a single crystal and in its natural state (called its intrinsic state), silicon acts as a fairly typical semiconductor. In order to make it act as a solar cell, it must be doped. This means that different regions of the material have a higher concentration of atoms that can contribute charge carriers. (Kasap, 2006)

For the cell to promote current flow in the correct direction, there must be a region consisting of mostly positive charge carriers (called p-type) in contact with a region consisting of mostly negative charge carriers (called n-type). The p-type region has substitution impurity atoms of an element that has less than four valence electrons (typically three). The atoms with three valence electrons replace silicon in the lattice and only bond to three surrounding silicon atoms, leaving a hole where the last bond should

be. These holes can be replaced by an electron from an adjacent bond, resulting in a new hole and giving the material the ability to carry a charge. N-type silicon works by replacing silicon atoms with atoms of an element containing more than four valence electrons (typically five). Since there are enough valence electrons, the dopant atom bonds to the four surrounding silicon atoms, but has a leftover electron. This electron, like the holes in p-type material, has the ability to move through the lattice. With no added energy, however, neither the spare electrons nor holes have the ability to move freely around the lattice, since their lowest energy state balances out through recombination. The surface where p-type silicon and n-type silicon are in contact is called the pn junction. At the pn junction, the excess electrons from the n-type silicon fill in some of the excess holes in the p-type silicon. This charge imbalance creates an electric field (space charge), which keeps the two types of silicon distinct from each other. (Kasap, 2006)

1.2.2 Photovoltaic Cells

In photovoltaic cells, or solar cells, outside energy comes from sunlight. The photons coming from the sun have some energy, which is described as a distribution. A photon of sufficient energy can be absorbed by the silicon lattice, thereby creating electron-hole pairs. This is accomplished by increasing the energy of an electron such that it leaves the orbit of the atom it was bound to and is free to move within the silicon lattice and conduct current. If this electron-hole pair is created within or close to the pn junction, the electron or hole can be pulled to opposite sides of the silicon according to the space charge at the pn junction. The excess charge carriers are then able to flow out

of the solar cell through some connected circuitry and do work. After travelling through the attached circuitry, they finally end up on the opposite side of the pn junction that they were initially pulled to and recombine with the opposite charge in order to complete the circuit. (Bowden, 2008)

There are two equations that describe the amount of current created by the solar cell. First, the equation for the total current through a solar cell is given in Equation 1 (Tan, 1995).

Equation 1: Current through solar cell

$$I = I_0 \left[e^{(qV/nkT)} - 1 \right] - I_L$$

Where I_0 is the reverse saturation current, I_L is the photocurrent, q is the charge of the charge carrier (in this case, the charge of an electron), T is the absolute temperature in Kelvin, k is the Boltzmann constant, η is the ideality factor (between 1 and 2), and V is the voltage that the solar cell is exhibiting (Bowden, 2008). There are a few special cases regarding this equation. First, when the solar cell is in the dark, there is no total current, which means that the photocurrent is equal to the rest of the equation. This graph looks like the graph of a typical diode, shown in Figure 1. (Kasap, 2006; Bowden, 2008)

Figure 1: Typical graph of an ideal diode I vs. V curve. (Bowden, 2008)

With increasing light intensity, the curve moves below the axis, giving a curve that exhibits some short circuit current, which is equal to the photocurrent. Figure 2: Solar cell with no illumination (left), some illumination (middle), and high illumination (right). shows three cases of the I vs. V curve in a solar cell with different amounts of light.

Figure 2: Solar cell with no illumination (left), some illumination (middle), and high illumination (right). (Bowden, 2008)

Typically, the graphs of illuminated solar cells have an inverted axis so that the area completely captured by the curve and the axes is in the first quadrant. This convention exists because the solar cell is generating current, while a normal diode conducts current. (Kasap, 2006; Bowden, 2008)

The other equation that determines the current and voltage characteristics of a solar cell relates to the load present on the cell. Because the current and voltage through the solar cell are the same for the load, it can be modeled by $I=V/R$. If the current out of the solar cell is assumed to be negative, the equation would be $I=-V/R$. Since the voltage is the same on the load as on the solar cell, these two equations must be set equal to each other. Figure 3 shows the graph of the two equations on the same plot. The point where they intersect shows the current and voltage that the solar cell outputs.

Figure 3: V-I Characteristics of a PV Cell. The curved line is the inverted diode characteristic line from Figure 2. The top line represents the maximum power that can be generated by the solar cell. The lower line is a generic load line based on a resistance R_L , with a slope of $1/R_L$. (Das, 2012)

1.2.3 Band Gaps

The amount of energy that a photon needs to impart in the silicon lattice is called the band gap. In intrinsic (pure and undoped) silicon, this is the amount of energy between the top of the valence band and the bottom of the conduction band. These bands describe what energy levels electrons are allowed to have. The valence band is the amount of energy that electrons have in the valence band, and the conduction band is the amount of energy that electrons have while conducting electricity. Typical semiconductors have a band gap that is greater than zero and less than 4 eV. Silicon has a band gap of 1.11 eV. Figure 4 shows a diagram of the band structure of semiconductors.

Figure 4: Energy diagram of the band structure of semiconductors. The shaded boxes represent filled electron energy states, the empty box represents unfilled energy states, and E_g is the band gap. (Tan, 1995)

1.2.4 Fermi Level and Work Function

One important feature of the band gap that has many consequences is the Fermi energy. The Fermi energy level is defined as the energy level that has a 50% chance of being filled. In metals, this is simply equal to the border between the conduction and valence band. Semiconductors, however, typically have a Fermi level within the band gap, even though electrons cannot have energies within the band gap. This is analogous to the average value of a roll from a six-sided dice being 3.5, even though the die can never land on 3.5. For semiconductors, it is a value that gives a good hint at what the

relative electron donor and acceptor concentrations are. When a semiconductor is n-type doped (having extra electrons in the lattice), the Fermi level is closer to the conduction band, as seen in Figure 5.

Figure 5: Fermi level for different types of doping in semiconductors. The left side of the picture shows p-type doping, and the right side shows n-type doping. (Schlenker, 2011)

Closely related to the Fermi level is the work function. The formal definition of the work function is the difference in energy between a free electron in a vacuum and an electron at the Fermi energy level (Kasap, 2006). In a diagram, it is shown as the distance from the Fermi energy level to the top of the conduction band. As the location of the Fermi level changes based on the doping level, so the work function changes with it. It is also good to note that the work function is a property of a surface of a material, not a bulk material itself, because it is usually measured at and has an effect only at the surface where two materials interact. It still varies greatly depending on material. Work

function affects the solar cells anywhere where two different materials interact, specifically silicon and metal contacts. Larger differences in work function result in an increased resistance between the two materials, and larger resistance means more power lost.

1.2.5 Indirect versus Direct Band Gap

Another aspect of semiconductors that affects this study is direct versus indirect band gaps. As with most models, the previously described method of electrons moving back and forth between the valence and conduction bands is incomplete. To move to a different band, the electrons not only have to experience a change in energy (from a photon), but must also conserve momentum by matching their velocity (which is affected by a phonon) to their destination. Figure 6 shows a diagram of the difference between a direct and indirect band gap (Kasap, 2006). A phonon is the movement of the crystal lattice in a periodic or wave-like fashion, similar to sound waves in air. The important value in a phonon is its k-vector, or wave number, which is the vector that describes the movement of the wave within the lattice. If the k-vector is the same for free electrons or holes as it is for the lattice, the material exhibits a direct band gap. This is true of many blended semiconductor materials, such as GaAs or GaN. Any significant difference in k-vector indicates an indirect band gap. Many single-element semiconductors, such as silicon or germanium, exhibit indirect band gaps. When an electron and hole either couple or decouple in a direct band gap material, the change in energy is sufficient for the pair to emit or absorb (respectively) a photon. For indirect band gap materials, not only must the electron hole pair be present with a photon of equal energy as the band gap, a

phonon with at least equal minimum energy as the difference in k-values must simultaneously exist. Higher energy photons impart more energy to the electron and lower the amount of momentum change that the phonon needs to impart. This phenomenon makes indirect band gap materials much less effective as solar cells, especially when they are relatively thin (Kasap, 2006; Wikipedia-Band Gaps).

Figure 6: Energy diagrams for direct (left) and indirect (right) band gap materials. The red curve represents the valence band and the green curve represents the conduction band. The vertical arrows represent energy from photons, while the horizontal arrow on the indirect band gap graph represents momentum imparted by a phonon (11). (Wikipedia-Band Gaps)

Because phonons are controlled by thermal energy, the effectiveness of indirect band gap materials in absorbing light is better at higher temperatures. This is because, at cooler temperatures, phonons are less frequent and have a lower magnitude. Conversely, semiconductors have a higher resistivity at higher temperatures. What this means for solar cells is that indirect band gap materials need to be thicker in order to absorb lower energy photons, such as in the infrared region. This thickness required to absorb light is called optical thickness (Bonneau, 2006; Bowden, 2008; Kayes, 2008).

1.2.6 Optical Thickness

In order for a silicon solar cell (silicon has an indirect band gap) to reliably absorb the full solar spectrum, it must be approximately 100 μm thick. The SOI solar cells used at Cal Poly are only 10 μm thick. One of the tests that carried out in this study addresses this issue directly in order to characterize the performance of a thin versus thick silicon solar cell.

In order to show this concept mathematically, we must look at the equation for light absorption, which is expressed in Equation 2.

Equation 2: Light absorption

$$A = \ln \frac{I_0}{I} = \alpha l$$

where alpha is called the absorption coefficient, l is the path length in a material, I_0 is incident light intensity, and I is transmitted light intensity (Tan, 1995). The absorption coefficient is the inverse of the penetration depth for a given wavelength of light in a given material. (Bowden, 2008; Tan, 1995) Figure 7 shows a graph of the absorption coefficient for different materials at common wavelengths of light. A high absorption coefficient means that more light is absorbed near the surface of the material. This is true for direct band gap materials. Conversely, indirect band gap materials have a low absorption coefficient, meaning that high energy photons are absorbed relatively early, but the whole solar spectrum is not absorbed until much deeper.

Figure 7: Absorption Coefficient vs. Wavelength for various semiconductor materials. Of the listed materials, only Si, Ge, and aSi are indirect band gaps. Even though CdS is a direct band gap material, it has a large band gap, explaining the drop-off in α . (Bowden, 2008)

In any solar cell, it is important for the thickness of the solar cell to be thicker than the optical thickness. For a cell that is thinner than the optical thickness, some wavelengths of light will not be absorbed before exiting through the rear of the solar cell. Due to silicon's absorption properties, it has a relatively high optical thickness. Direct band gap materials, such as gallium arsenide (GaAs), have a low optical thickness, approximately 5 μm . Figure 8 is a graph of the absorption depth versus the wavelength of light. (Tan, 1995)

Figure 8: Absorption vs. wavelength of light for silicon. It shows that any significant amount of light requires much more than 10 μm of material. (Bowden, 2008)

This graph brings up an ambiguity with the definition of optical thickness. Specifically, how much light of the solar spectrum needs to be absorbed within the optical thickness? It can't be all incident light because silicon is infrared transparent. A typical definition is that the optical thickness is the thickness required to absorb 90% of incident light above the band gap. Using this definition, silicon has an optical thickness of approximately 125 μm (Kayes, 2008). The reason silicon is used in this study is because direct band gap materials are much more expensive and cannot be processed in the labs at Cal Poly.

1.2.7 Reducing Optical Thickness

Though the standard optical thickness is constant per material, there are ways of artificially changing it. The two main strategies being used by industry are to apply reflective coatings to the back of thin solar cells and to apply surface texturing to the front.

Silicon solar cells that are less than 125 μm thick are not thick enough to absorb 90% of available solar energy from the sun because some of the light will travel through it. Once the photons have exited the back of the cell, they are effectively lost. By placing a reflective coating on the back of the solar cell, any photons that reach the back of the cell will reflect back and have twice as much material to absorb into. This effectively halves the optical length of the material since there is twice as much absorption for each unit depth of solar cell. Figure 9 is a schematic of how the rear reflector adds to the optical transmission length.

Figure 9: Example of a solar cell with no rear reflective layer (left) and with a rear reflective layer (right). Note that light travels through the silicon for twice as long with a rear reflective coating present. (Bowden, 2008)

Another strategy to reduce optical thickness of a material is to use surface texturing. Surface texturing relies on the properties of refraction as well as reflection to maximize the amount of light absorbed by the solar cell. When light is incident on any surface, some of it reflects and some of it refracts. On a textured surface, the reflected light will often be incident on another surface, allowing even more light to enter the cell. As an added bonus, the refracted light from the textured surface travels in the solar cell at an angle, meaning that it is not as deep in the cell while still travelling the distance of the optical thickness before decoupling an electron-hole pair. Figure 10 shows a few schematics of how light reflects and refracts on textured surfaces, and Figure 11 shows a scanning electron microscope (SEM) image of a textured surface of a solar cell.

Figure 10: Schematic showing how reflection and refraction assist in an increase of light into the solar cell (left) and how light travels far in a solar cell with both front and back texturing (right). (Bowden, 2008)

Figure 11: Scanning electron microscope image of pyramidal surface texturing on a solar cell. The base of the large pyramids is approximately 10 μm . (Bowden, 2008)

1.2.8 Recombination Losses

There are numerous aspects of solar cells that can cause inefficiencies, the most important of which is efficiency loss due to recombination. Recombination loss refers to the combining and subsequent annihilation of an electron and a hole. This can happen on the surface, which includes at the contacts, or within the bulk in a solar cell.

Recombination is undesirable because the charge carriers that would otherwise produce a current are no longer available and the energy that it took to decouple them was wasted.

1.2.8.1 Bulk Recombination

The most important aspect of decoupled electrons and holes with regards to bulk recombination is the diffusion length. The diffusion length measures how far a charge

carrier can move before recombination. Any minority charge carriers that are generated further from the pn junction than the diffusion length do not contribute to the current or voltage characteristics of the solar device. More heavily doped semiconductors have a lower diffusion length due to a greater excess of the majority charge carriers, which results in an increased likelihood that a minority charge carrier will recombine. There are however reasons to dope certain regions more heavily than others which will be discussed later. This form of recombination is called bulk recombination. In order to minimize recombination, it is desirable to maximize the diffusion length. Both the bulk recombination and charge carrier diffusion length affect the open circuit voltage, as shown in Figure 12.

Figure 12: Open circuit voltage and diffusion length vs. doping level. There is an ideal doping level required to maximize V_{oc} , which occurs at the same doping level that diffusion length drops off. (Bowden, 2008)

1.2.8.2 Surface Recombination

Recombination does not only happen within the bulk material. It is much more likely for electrons and holes to recombine at sites such as the surface of an unpassivated material, a grain boundary (if the semiconducting material is polycrystalline), or the electrical contacts. Figure 13 shows the effect of recombination losses on the quantum efficiency, which relates to the current, versus wavelength in solar cells.

Figure 13: Quantum efficiency vs. wavelength is affected by recombination losses. (Bowden, 2008)

The region of a typical solar cell that is responsible for the most surface recombination is the top surface. Due to the fact that semiconductors absorb high-energy photons quickly, a large number of charge carriers are generated near the surface of a solar cell. Minority charge carriers that are produced close to the junction are more likely to diffuse to the junction, which increases efficiency, but the surface of a semiconductor has dangling bonds that would be bonded to other silicon atoms if there were more silicon instead of a surface. This region of dangling bonds is quite conductive and

facilitates the recombination of the photogenerated electrons and holes. A common and effective solution to this problem is to bond a non-conducting material to the dangling bonds, thereby minimizing a large amount of surface recombination. Often times this material is a thermally grown silicon oxide.

Another area that is subject to recombination but cannot be so easily passivated is the area under the top and bottom metal contacts. The dichotomy is that they need to be in electrical contact with the silicon, but they allow for surface recombination. In order to prevent minority charge carriers from coming in contact with the contacts, a small region that is only in direct contact with the contacts can be doped. While this does shorten the diffusion length, there are no minority charge carriers being generated directly under the contacts, so the resulting effect on diffusivity is unimportant. On the other side of the cell, the heavy doping near the rear contact slightly acts as a pn junction in that it creates an electric field called the Back Surface Field (BSF). This electric field works to keep electrons from diffusing below the heavily doped region, ensuring that they stay away from the rear contact. If there are no electrons near the rear contact, then there is negligible surface recombination there. Figure 14 shows a cross section of a solar cell with the passivation layer on top and heavily doped regions at the contacts. (Bowden, 2008)

Figure 14: Cross section of a solar cell showing the passivation layer and doping regions that are designed to minimize surface recombination. (Bowden, 2008)

1.2.9 Internal Resistance

Another important aspect of solar cells is the presence of both series and shunt resistance, which are always present in the cell. Series resistance (R_s) is the amount of resistance between the contacts and the solar cell. Ideally, R_s is zero, indicating that there is nothing impeding the current flow in from the solar cell. If R_s increases, the ideal curve in the I vs. V plot straightens out and becomes linear between the open circuit voltage and the short circuit current. If it continues to increase after that, the short circuit current decreases until there is no signal, but this requires a high resistance in order to occur, as shown in Figure 15. (Bowden, 2008; Kasap, 2006)

Figure 15: Effect of series resistance on the current and voltage characteristics of a 1 cm^2 solar cell. The figure shows the curve with zero series resistance (top), with 10Ω series resistance (middle), and with 20Ω series resistance (bottom). (Bowden, 2008)

Shunt resistance (R_{Sh}) is a phenomenon that occurs which provides an alternate path for the photo-generated current. A high R_{Sh} prevents surface recombination. Thus,

opposite from R_s , it is desirable for R_{sh} to be as high as possible. As described in the recombination section, adding a passivation layer prevents surface recombination by drastically reducing the conductivity (or increasing the resistance) along the surface. If R_{sh} becomes low enough, it decreases the open circuit voltage and simultaneously straightens the graph out, quickly decreasing the fill factor, shown in Figure 16.

(Bowden, 2008; Kasap, 2006)

Figure 16: Effect of shunt resistance on the current and voltage characteristics of a 1 cm^2 solar cell. The figure shows the curve with $10^4 \Omega$ of shunt resistance (top), a shunt resistance of 35.5Ω (middle), and shunt resistance of 14.1Ω (bottom). (Bowden, 2008)

1.2.10 Contact Design

Series resistance is often the more detrimental of the two types of internal resistances. It is based very heavily on the design of the top contact. In order to understand the effect that it has on the efficiency of the solar cell, it is more accurate to calculate the power loss in different regions of the solar cell. The three most prevalent losses to efficiency in solar cells are shadowing losses, emitter resistive losses, and finger resistive losses. These losses will be described here but will be looked at in detail in section 3.4.3.

Shadowing losses are caused by the top metal contacts blocking light from entering the solar cell. Any area in which light is blocked cannot generate electrons. The fractional area covered by the top contacts is the fractional power loss based on shadowing.

Emitter loss is the encountered resistance to flow that the electrons face on the surface of the solar cell as they are going towards the contacts. It is assumed that electrons travel toward the closest finger perpendicular to the length of the finger.

Finger loss is the resistive loss based on the resistance encountered by the electrons in the finger as they travel toward the busbar. Thinner fingers means more area exposed to sunlight, but higher resistance. It has an identical definition to the busbar loss, though is calculated differently. Since the busbar is typically the length of the solar cell, it is reasonable to ignore its effect.

1.2.11 Additive Properties of Solar Cells

Solar panels that provide any significant power have sections of solar cells that are wired in series and in parallel. Solar cell arrays made of individual solar cells wired in series display a total voltage that is equal to the sum of the voltages of the individual cells and a current equal to the lowest current of any of the cells. The opposite is true of wiring solar cells in parallel; the currents add and the total voltage is equal to the lowest voltage. In order to achieve a high current and voltage, industrial solar panels consist of arrays of solar cells wired in parallel, where each array consists of cells connected in series. For the purposes of this study and previous studies that this one is based on, only the individual arrays of solar cells in series are being considered.

Another important factor that must be considered in solar cell arrays is the built in resistances. Since series resistance (R_S) is in series with the current, it is additive when multiple solar cells are placed in series. This total R_S , when determining the current and voltage properties of a series of solar cells, is applied to each cell in order to find its properties. Once those properties are found, the voltages in the series add, and the current that the array outputs is equal to the cell with the lowest current. Following the pattern, if the solar cells are placed in parallel, each R_S affects only its own distinct solar cell. This effect works primarily to make all of the parallel solar cells equal to the same voltage, in accordance with Kirchhoff's voltage law. (Wikipedia-Kirchoff's circuit laws) Whether in series or in parallel, shunt resistance (R_{Sh}) only affects the individual solar cell and does not add to or mitigate the effects of the R_{Sh} from other cells.

1.2.12 Solar Cell Science Applied to this Study

In the following discussion sections contained in this study, portions of this background science section are referred to. Many of the factors and variables that affect how solar cells work can be adjusted in each of the tests in this study. All of these factors will be addressed in the final discussion of this study when determining the feasibility of producing a solar cell array from a single silicon wafer and if that is possible in the microfabrication lab at Cal Poly San Luis Obispo.

1.3 Current Technology

In order to try to improve a certain technology, it is necessary to understand how it currently works. A typical solar device that is produced currently follows a standard series of steps. First, a silicon wafer, usually p-type, is doped with an n-type layer. Sets of metal contacts that conduct current from the cell are also deposited at this point. (Bremmer, 2009) Since the whole n-type region is connected to the same p-type region, the wafer with multiple sets of contacts does not act as multiple solar cells. This means that the silicon wafer must be broken so that all the n-type regions are distinct and coupled with p-type regions. Next, a conductive tape or foil must be applied to both the n- and p-type portions of the modules so that they can be connected together. (Solarbuzz) Before they are connected though, they must be mounted in their final configuration on the device. Then the individual modules are connected together using the conductive tape or a reflow soldering technique. After all cells are connected in series, they are encased to protect the circuitry and the production is complete. (Bremmer, 2009; Solarbuzz)

This process is not complicated and is used to produce many solar devices yearly as shown in Figure 17. (Roney, 2010) There may still be a better way to produce these devices with fewer steps. This study addresses is the possibility of making a working solar cell array, just as described above, but without having to break the wafer into separate modules, connect the modules with conductive tape, or carry out a soldering process. What if the solar cell array never had to leave the clean room until it was ready for packaging? Such a process would likely save time and money, if it can be successfully designed.

Figure 17: Yearly solar cell production measured in megawatts. (Roney, 2010)

It is prudent to note that this study is being researched primarily with manually run machines, as opposed to the almost complete automation that is standard in industrial clean rooms. (Campbell, 2008) Such a set up is great for tweaking parameters, but not for achieving ideal reproducibility. Therefore, it is good to view this study as a

characterization of the production capabilities of the microfabrication lab at Cal Poly as well as a research project that answers how all the parts of a silicon solar cell work and the best way to optimize it in future studies.

1.4 Previous Projects

There have been, to date, three projects attempting to solve the problem presented in the introduction and case study sections. All three of these projects were based off the production of single solar cells for a class at Cal Poly. The key difference between those studies and this comes down to scope. The previous projects have focused on trying to replicate the results without ensuring that the parts all work. This study is the opposite; parts of the project are tested and much more extensive research is conducted with the goal of laying the groundwork for future experiments, hopefully giving them a better chance at success.

1.4.1 Microfabrication Lab

Every winter quarter at Cal Poly, there is a lab in the materials engineering department, hereafter referred to as MatE 435, in which students fabricate semiconductor devices. One of these devices is a solar cell. The class gives the students opportunity to not only learn how semiconductor devices are made, but gives them the hands-on experience of actually making one. Since the focus of the lab is not the device itself, but rather the processing therein, the solar cell is designed to work but is not optimized.

Figure 18 shows the two masks used in the MatE 435 solar cell. The wafer is a single-crystal p-type wafer, just as is typical in industry. One of the biggest differences from commercial solar cells is the junction. As discussed in the “Background Science”

section, a typical pn junction in a solar cell is made by doping one whole side of a p-type wafer, which creates a flat junction. This design utilizes an n-type doped well on the top of the wafer that accounts for approximately half of the area, as well as an uneven junction. The two doping types are composed of “fingers” that alternate n- and p-type. Between a quarter and a third of the thickness of each finger is covered with gold contact.

Figure 18: Microfabrication Lab solar cell mask for doping layer (left) and metal layer (right).

The parameters of this design vary from ideal circumstances in a number of ways. First, the width of the contacts blocks a lot of light from shining into the solar cell. Though increased size of the contacts does decrease the resistance, the large amount of light blocked results in net higher efficiency losses. In addition, the regions in which the top of the solar cell is p-type is less efficient than if it was n-type. The charge carriers in p-type silicon are holes, which are far less mobile than electrons. During the time a hole

diffuses up to the surface of the solar cell while staying in the p-type region, it will experience more resistance than an electron that moved through the junction and to the surface.

1.4.2 Senior Project 2010

In 2010, the solar cell array project at California Polytechnic University at San Luis Obispo (Cal Poly) was first attempted (Lenhof, 2010). The researchers designed a few test wafers to determine the parameters of the final design. They decided on a design that incorporated 1,247 separate silicon solar cell modules connected in series. Each module was made of the epitaxial layer of silicon on top of a silicon-on-insulator (SOI) wafer. The 180 μm distances between the modules was filled in with a B_2O_3 layer in order to insulate any leakage current. Finally, aluminum interconnects were used to connect all 1,247 modules in series. Figure 19 shows a schematic of the design.

Figure 19: Overall schematic of all 1,247 modules in series (left) and schematic of a single cell (right) (Lenhof, 2010)

Since all modules are connected in series, any one of them failing would effectively result in an open circuit, and therefore render the entire array ineffective. The design also incorporates small features, which drastically increases the probability of errors in production. Most of the possible errors in production, with this many small features, would result in a disconnected module, and therefore an open circuit. Those that wouldn't result in an open circuit could result in short circuits, effectively nullifying the given module and not contributing any current or voltage to the response. This is less

of a critical problem because the module would still work, but it would be less efficient due to inactive modules. Finally, aluminum has the tendency to react with silicon, which forms an electrically conductive intermetallic that reacts far down into the silicon and can bridge the gap between n and p type, effectively short-circuiting the cell. This phenomenon is called aluminum spiking, and likely caused multiple modules to be short-circuited. Some combination of these imperfections occurred, as the array produced a maximum of 8.47 mV, which is nearly negligible compared to the theoretical 624.5 V for 1,247 silicon solar cells in series, or even the .5 V for one silicon solar cell. One method of preventing aluminum spiking is to deposit aluminum that has 1.5-2% silicon in it. This way, the aluminum already has some dissolved silicon and will be less likely to react. Another fix is to use a different metal that won't cause spiking, like gold. Gold also has the added benefit of being more conductive and less reactive to the environment.

1.4.3 Senior Project 2011

In 2011, another group attempted to make a solar cell array (Blattner, 2011). They began by making only two modules on an SOI wafer in order to prove that a 10 μm thick solar cell would work. They found that one of the cells did not output any power and the other displayed non-ideal behavior. Accepting these results, they then designed a wafer with twelve silicon modules connected in series. They again used aluminum as the contact metal, but instead of relying on them to coat up and down the sides of the modules, they filled in the gaps with SU-8, a photo-hardening polymer. This way, there would be a flat, seamless transition from silicon to polymer to silicon for the aluminum to deposit to. Their design is shown in Figure 20.

Figure 20: Schematic of the 2011 solar cell array project (Blattner, 2011)

Just like the previous year, the array did not perform ideally, but this was much better. Two of the four wafers worked somewhat as intended. The big problem the researchers had this year was connectivity. The SU-8 was not level, smooth, nor as thick as the epitaxial layer, resulting in ledges at the silicon-polymer boundary, as well as within the polymer region. This prevented the interconnects from being continuous, resulting in an open circuit. The two best wafers had no and one discontinuities, while the other two had all discontinuities. The individual modules did, however, work as intended, as shown by the voltage. The best wafer had 5.5 V out of a theoretical 6 V, and the second best had 4.3 V. This means that each properly working module exhibits a voltage near .5 V, which is ideal for silicon cells.

The current, however, was not as close to the ideal value as the voltage. As previously mentioned, the interconnects were again made out of aluminum, which likely caused aluminum spiking, which severely reduces the efficiency of the affected modules. Also, the closest interconnect to the location where the electron-hole pairs originate is not close to each other, thereby reducing the current further. Interdigitated “fingers” in both the doped region as well as the contacts allow more electrons and holes to get into the circuit. This design clearly worked better than the 2010 version, but the researchers recommended that future projects use a metal other than aluminum and that the connectivity issue be addressed.

1.4.4 Senior Project 2012

Finally, the 2012 group tested two different strategies (Gade, 2012; Savage, 2013). One design revolved around doping wells within wells in the silicon wafer, hoping that these regions would act as distinct solar cells. This design was called the multi-well design. The other was essentially the same as the previous year but with a different strategy of interconnects. Specifically, the traces would be on a glass wafer that would be attached on top of the solar modules. This design was called the silicon islands design. Figure 21 shows pictures of the two 2012 solar cell array designs.

Figure 21: Multi-well design (left) and silicon island design (right) (Gade, 2012)

The multi-well design did not need to utilize an SOI wafer, since an extra depletion region was the tool for keeping the separate cells apart. Since this design had no direct predecessor at Cal Poly, a test wafer was used to determine the ideal spacing between cells. It was found that the further apart the cells were, the better they worked. Using this knowledge, a design incorporating only two cells was designed and fabricated. A cross-section schematic is shown in Figure 22.

Figure 22: Multi-well solar cell array cross-section (Gade, 2012)

The results for this design were less than promising. While the two cells did function as distinct cells, they had a combined voltage of .6 V, as opposed to the theoretical 1.0 V. More cells could be put on the wafer, but that would mean that all the

cells would be closer together, which was shown in the test to degrade the performance of all of the cells.

The silicon islands design worked on the same principles as both the 2010 and 2011 version. In order to avoid the two biggest problems with the 2011 design (aluminum spiking and rough fill-in of the area between the islands), a new type of interconnection was devised. The traces, made of gold, would be patterned on a transparent glass wafer. Titanium was used as an adhesion layer to ensure that the gold layer did not delaminate. It was then attached to each island with an application of electrically conductive epoxy. A cross-section of the design is shown in Figure 23.

Figure 23: Cross section of the silicon island design (Gade, 2012)

Unfortunately, though each island did not have anything wrong with it, the connection between the conductive epoxy and the silicon and a $40\text{ M}\Omega$ resistance, which is more than enough to shut down any signal that the modules would have achieved.

2 TESTING A SOI SOLAR CELL

2.1 Introduction

The first problem that this study addresses is the effect of silicon's indirect band gap on the effectiveness of a 10 μ m thick solar cell. As described in section 1.2.5, a silicon solar cell, given its indirect band gap, needs to be around 125 μ m thick in order to absorb the full solar spectrum. A thinner cell will be less likely to or unable to absorb any light in the infrared region. To attempt to quantify this, a SOI wafer was used to make a single solar cell. Since the Materials Engineering 435-Microfabrication Lab has constructed the exact same cells on 500 μ m thick wafers, the data from those was compared to the data from the SOI single module cell. To ensure equal surface area for photons to be absorbed, no part of the solar cell was etched out in the manner that it has been during the 2010-2012 tests. The open circuit voltage is an inherent property of the material and should be close to .5 V in both cases. Less photon absorption would most likely be reflected on a lower short circuit voltage, also resulting in less total power with any given load on the cell. The thickness of the cells should not, however, affect the depth of the doped wells, which means that variance should only come from the difference in thickness of the cells. Figure 18 in Section 1.4.1 shows the masks used to create the doping layer as well as interconnects for the microfabrication lab. In interest of comparison, the same masks were used for the thin solar cell in this test.

2.2 Method

The goal of this test is to quantify the difference between two nearly identical solar cells that have a crucial difference; one has a thickness significantly less than the

optical length and one has a thickness significantly more than the optical length. To do this, the results for this test are compared to other solar cells that utilize exactly the same masks, but are made out of 500 μm thick silicon wafers. Comparing the thick and the thin solar cells should give a good picture of how exactly the thickness affects the solar cell performance. Additionally, solutions to the factors that cause a solar cell to be less efficient will be discussed.

2.2.1 Fabrication

The solar cell starts out as a SOI wafer with a 500 μm thick silicon handle with an oxide layer on it. On top of the oxide layer is a 10 μm epitaxially grown layer of single crystal n-type silicon. P-type silicon produces more efficient solar cells since the minority charge carriers (electrons) are more mobile, but the difference is small and n-type SOI wafers are more readily available at Cal Poly.

First, a 5000 $\text{\AA}$ thick thermally grown oxide layer was grown on the SOI wafer. This was accomplished in a wet oxygen environment at 1050°C for 1.5 hours. A layer of Shipley positive Photoresist was then spun onto the oxide layer using a Bree Cee 200X Spin Coater. The planarization step of the spinning process took place at 4000 RPM for 20 seconds and resulted in a 1.0-1.2 μm thick layer. Afterwards, it was soft baked at 90°C for one minute. Afterward, the Photoresist was exposed and developed. A Canon PLA501FA aligner was used for the light exposure and a CD-26 microposit developer was used. The developer is 2.5% tetramethyl ammonium hydroxide (TMAH) and took approximately two minutes to develop the Photoresist. After the development, the wafer was hard baked at 150°C for one minute. In order to use the oxide layer as a diffusion

mask, the wafer was submerged in a HF solution for approximately 6 minutes in order to etch through the exposed oxide layer through the openings in the Photoresist. After the diffusion mask is finished, the Photoresist was stripped off the wafer using a Shipley 1156 microposit remover at 50°C for 15 minutes.

A solutionized dopant was spun onto the wafer in order to dope the p-type regions of the solar cell. The main component in the dopant is dissolved boron. The dopant was driven via diffusion into the solar cell at 1050°C for 1.5 hours to a depth of about 2 μm . After the dopant was driven in, the wafer was once again submerged in a HF solution that removed everything on top of the silicon.

Using a Denton Desk V Sputtering System, a .2 μm thick gold layer was deposited on the wafer. In order to pattern the traces that will be made from this deposited gold, a layer of positive Photoresist was spun onto the gold layer. The planarization step of the spinning process took place at 4000 RPM for 20 seconds and resulted in a 1.0-1.2 μm thick layer. Afterwards, it was soft baked at 90°C for one minute. The Photoresist was exposed and developed. A Canon PLA501FA aligner was used for the light exposure and a CD-26 microposit developer was used. The developer is 2.5% TMAH and took approximately two minutes to develop the Photoresist. After the development, the wafer was hard baked at 150°C for one minute.

The traces were etched out from the gold layer using a gold etchant at room temperature. It only took a few seconds for the etchant to etch through the gold. After the traces were finished, the Photoresist was stripped off the wafer using an 1156 Microposit remover at 50°C for 15 minutes. Leads were then attached to the pads on positive and negative sides of the solar cell with Ted Pella CD-26 silver filled epoxy so

that the test system can be readily attached to the solar cell. The epoxy was cured at 80°C for an hour. Figure 24 shows the cross section of the final SOI solar cell.

Figure 24: Cross section of final SOI solar cell. The red area is n-type silicon, the green area is p-type silicon, the gray area is silicon dioxide, and the yellow area is gold.

2.2.2 Testing

The finished solar cell, made with an SOI wafer, was tested under a tungsten halogen light source. Though not a perfect replication of the solar spectrum, it effectively demonstrates the differences between solar cells. An Amprobe Solar-500 Solar Analyzer was used to test the voltage versus current characteristics of the cell. Figure 25 shows a picture of the finished SOI solar cell.

Figure 25: Completed SOI solar cell with attached positive and negative leads (red and green, respectively). A part of one of the gold fingers broke off in the etching process.

2.3 Results

Figure 26 shows the resulting I-V curve for the SOI solar cell test. It shows that the maximum (open circuit) voltage is .427 volts, the maximum (short circuit) current is 5.4 mA, and the maximum power is .594 mW.

Figure 26: Voltage versus Current characteristics of the SOI solar cell. The blue line on the graph is the voltage versus current function, while the red line is the power versus current function.

2.4 Discussion

The theoretical voltage of a single silicon solar cell is .5 volts, so the achieved value of .427 V displays an error of only 14.6%. Commercial solar cells exhibit short circuit currents between 28 mA/cm² and 35 mA/cm². Solar cells on a 10 cm diameter wafer have a surface area of about 78.5 cm², so it could theoretically put out much higher than the achieved current of 5.4 mA. This is likely due, in part, to the fact that few wavelengths of light are likely absorbed by the first 10 μm of silicon, as well as the fact that only electrons generated within a micron of the junction are collected.

Table I shows the data collected for the SOI solar cell alongside the average of 5 thicker 500 μm solar cells.

Table I: SOI versus 500 μm thick (regular) solar cells. The regular data is an average of five different solar cells.

Solar Cell	Open Circuit Voltage	Short Circuit Current
SOI	4.27 V	5.4 mA
Regular	4.33 V	13.5 mA

Compared to the thicker version, we start to get a picture of the differences between thick and thin solar cells. The short circuit voltage values are about the same for both types of cells, which is not surprising due to the fact that voltage is an intrinsic property of silicon. The current, however, ranged from about the same in both to about 2.5 times more in the thick cells (around 13.5 mA). Assuming that the higher current cells have fewer defects, they show that a thicker solar cell will perform better. Even with their marginally better performance, however, the thicker solar cells still display far below the market low for commercial solar cells. The reason that the SOI solar cell produced more than 10% of the current likely comes from the difference in the photon energy distribution between the sun and the light source. Since the light source used was different from the sun, the optical length discussed in the background science section does not apply.

There are a few reasons why both the SOI solar cell and the thicker solar cells fabricated at Cal Poly are significantly less efficient than they could be. These include the fact that the SOI cell is not thick enough to absorb the full solar spectrum, the surface is highly polished, there is no passivation layer on the top of the cell, there is no rear reflector, the contacts take up too much space on the top of the wafer, and the contacts

are not in the right form to promote high efficiency. With the exception of the thickness of the silicon, all of these issues have the same effect for thicker solar cells.

First of all, the thickness of the solar cell made on a SOI wafer does not have the ability to absorb the full solar spectrum. According to Figure 8, a silicon solar cell needs approximately 125 μm of depth to absorb 90% of the solar spectrum above its band gap (Kayes, 2008). This required thickness can be reduced in a number of different ways, including adding a rear reflector and texturing the front and back surfaces. The reflector in back, as shown in Figure 9, doubles the effective depth of the solar cell. In a thick cell (anything thicker than half the optical depth), the rear reflector is significantly less effective because some of the extra effective depth will not contribute to generated charge carriers. Rear reflectors, however, are only useful if it is within the diffusion length of the junction. A textured surface of the solar cell, as shown in Figure 10, also helps reduce the required thickness since light can travel at a diagonal through the material and be absorbed closer to the junction (Bowden, 2008).

Related to the optical thickness in a solar cell is the diffusion length. Though this solar cell utilized n-type silicon instead of the more efficient p-type silicon, the dopant concentration in the wafer was around 10^{16} cm^{-3} , which gives a diffusion length of just over 100 μm (Savage, 2013). This diffusion length is very close to the optical length and is much more than the thickness of the solar cell in this test, so there should be no significant power loss or inefficiency due to the diffusion length.

Another issue is the bare, unchanged surface of the solar cell. By texturing the surface as described in both Figure 10 and this section, light will be able to reflect off of the solar cell in multiple locations, meaning that more light can be absorbed due to

refraction (Bowden, 2008). In addition, a textured surface of the solar cell helps reduce the required thickness since light can travel at a diagonal through the material and be absorbed closer to the junction (Bowden, 2008). The other change that should be implemented on the surface is that there should be an oxide or other passivation layer grown on it. Such a surface helps to drastically reduce the surface recombination, as described in section 1.2.8.2 (Bowden, 2008).

Finally, the area covered by the metal contacts is nearly a third of the area on the fingers. This automatically reduces the theoretical efficiency to 67%. Additionally, larger fingers further away from each other means that the electrons have to travel along the surface for a further distance, which results in a higher chance of recombination. Although the fingers will have more resistance, the overall more efficient configuration consists of a central busbar with very thin fingers spaced closer together. This allows electrons to move much shorter distances in order to be collected by the contacts. The busbar-finger configuration will be discussed in greater detail in the next chapter.

3 INTERCONNECT TESTING

3.1 Introduction

The next aspect of the solar cell array that this study addresses is the interconnects between the solar cell modules. Due to the lack of a chemical mechanical polisher (CMP) or other means of achieving near-atomically flat material with no height difference between silicon islands and filler material, this study will focus on the method of interconnection used in the 2012 Cal Poly senior project, in which the gold traces were attached to a glass wafer. Specifically, this study will test the best method of connecting the modules with a glass wafer that has gold traces on it. The primary failure in the 2012 study was the conductive, silver-filled epoxy was bonded directly to bare silicon, which resulted in a resistance of around 40 M Ω (Gade, 2012). In order to test if the connection method is acceptable for using in a solar cell array, the resistance of a gold-epoxy-gold bond is tested.

3.2 Method

The goal of this test is to quantify the resistance of a gold-conductive epoxy-gold bond and determine if it is sufficiently low and will leave the solar cell power unhindered. In addition, the shape and dimensions of the ideal traces will be discussed.

First, a glass wafer patterned with gold traces, identical to the one used in 2012, is fabricated. Next, a silicon wafer is coated in gold. Note that this wafer is not doped or patterned at all, since this experiment is only intended to test the bond resistance, not any actual solar cells. The gold-coated silicon wafer is then broken into pieces that could be connected across the breaks in the traces with the conductive epoxy. Finally, the

resistance across each gold-epoxy-gold connection is measured, since there are portions of exposed gold traces on either side of the broken silicon piece. In order to eliminate any fluke data and to take into account the variance of the connections, multiple measurements were taken from each connection. Multiple measurements help us to more accurately conclude the actual resistance of the bonds.

With the given pattern of the gold traces, there are ten available positions for gold-coated silicon pieces to be attached. Though we could attempt to figure out the resistance value of the individual bond, it is unnecessary due to the fact that series resistances stack when solar cells are connected in series. In order to acquire the most statistically significant data, each connection was measured ten times. The data is then analyzed in JMP statistical software by SAS Institute, Inc. as a one-way ANOVA where the factor is connection number and the response is resistance. Analysis is also done to ensure that the bond is the only influence on resistance.

3.2.1 Fabrication

The interconnect resistance test starts with a glass wafer. Using a CRC-150 Sputtering System, a .5 μm thick titanium layer was deposited on the wafer. Using a Denton Desk V Sputtering System, a .2 μm thick gold layer was deposited on top of the titanium layer.

A layer of positive Photoresist was spun onto the gold layer with a Bree Cee 200X Spin Coater. The planarization step of the spinning process took place at 4000 RPM for 20 seconds and resulted in a 1.0-1.2 μm thick layer. Afterwards, it was soft baked at 90°C for one minute. The Photoresist was exposed and developed. A Canon

PLA501FA Aligner was used for the light exposure and a CD-26 Microposit developer was used. The developer is 2.5% TMAH and took approximately two minutes to develop the Photoresist. After the development, the wafer was hard baked at 150°C for one minute.

The traces were etched out using a gold etchant at room temperature. It only took a few seconds for the etchant to etch through the gold. The wafer was then submerged into a titanium etchant solution at room temperature for approximately one minute. After the traces were finished, the Photoresist was stripped off the wafer using an 1156 microposit remover at 50°C for 15 minutes.

For the gold on silicon pieces that connect the traces together, we started with a n-type silicon wafer. Using a Denton Desk V Sputtering System, a .2 μm thick gold layer was deposited on top of the titanium layer.

Using a scribing tool, scratches were carved into the wafer making small rectangles. The wafer was then broken along the line of the scratches resulting in small silicon pieces that can be used to connect the interconnects on the traces wafer.

Using Ted Pella H22 Epo-Tek silver filled conductive epoxy, the silicon pieces were connected to the traces so that everything is in series. The epoxy was cured at 80°C for one hour. Figure 27 shows the final cross section of the interconnect test wafer.

Figure 27: Cross section of the final interconnect test wafer. The red area is n-type silicon, the yellow area is gold, the blue area is silver filled epoxy, the black area is titanium, and the gray area is glass.

3.2.2 *Testing*

Before attaching the silicon pieces to the glass wafer, the resistance was measured on the traces on the glass wafer. This was done in order to compare how much resistance came from the epoxy versus the gold film. The values came out to about 4 ohms for each quarter inch, and even less than that on the gold-coated silicon wafer. To attach the two components together, a small dot of silver-filled conductive epoxy was attached to the end of each of the “fingers” of traces. Figure 28 shows the epoxy after it is applied to the traces as well as the pieces of silicon that will be attached to the traces.

Figure 28: Epoxy dots applied to traces (left) and pieces of gold-coated silicon (right).

After the ten pieces of gold-coated silicon were placed on the traces, the whole thing was placed into an oven at 70°C for an hour to cure the epoxy. Figure 29 shows a view of the traces from through the glass wafer with attached silicon pieces.

Figure 29: Test 2 assembly. The gold-coated silicon pieces are attached with a conductive epoxy to the gold traces. The resistance is measured across each piece of silicon via the gold traces.

The resistance was measured across each piece of silicon by applying the two probes of an ohmmeter on the gold traces on each side of the connections. Figure 30 shows the top view of the test 2 assembly with each connection numbered, as well as green dots showing where the measurements were taken from.

Figure 30: Top view of test 2 assembly. Each silicon piece was numbered and a green dot was applied next to the traces in order to make sure that the measurements were taken from the same place each time.

3.3 Results

3.3.1 Statistical Analysis

The resistance across each silicon piece was measured ten times. The raw data is shown in Appendix C. Analysis of variance (ANOVA) analysis was run on the resistance data with respect to the connection number. Figure 31 shows the scatter plot and ANOVA test output generated in JMP statistical software. With an automated process, this test would be unimportant, since there would be very little source of variance. At Cal Poly, there is no automated process for depositing and curing silver-filled epoxy, so it is good to know what the approximate variance is when using this process.

Figure 31: Graph of collected data (top) and ANOVA (bottom) showing that the different connections can not be assumed to have similar means based on any reasonable level of confidence.

The ANOVA tests whether or not all of the means of each connection is equal to each other. Specifically, the null hypothesis is that all of the connections have the same average resistance, while the alternative hypothesis is that at least one mean is different from the other. A p-value lower than the significance level indicates that we reject the null hypothesis and conclude that there is reasonable evidence to suggest that at least one of the means is not equal to the others. A typical confidence level is 95%, corresponding

to a significance level of .05. Since the p-value, which is labeled “Prob > F” on the readout, is so low, we can with any reasonable level of confidence say that at least one of the means is different from the others. In order to determine which can be said to be statistically similar with a given level of confidence, a Tukey pair-wise comparison test was run. This test compares each pair of factor levels, in this case connection numbers, and determines if they are statistically similar with a specified level of confidence, which we will assume to be 95%. Figure 32 shows the Tukey test.

Connecting Letters Report		
Level		Mean
C2	A	12.380000
C9	A B	11.120000
C8	B	10.960000
C10	B	10.920000
C3	B C	10.350000
C7	B C	10.040000
C1	B C	9.990000
C5	B C	9.870000
C4	C D	9.450000
C6	D	8.550000

Levels not connected by same letter are significantly different.

Figure 32: Tukey pair-wise comparison for the resistance data. Each pair that shares a similar letter has statistically similar means based on a 95% confidence level.

The physical meaning of the confidence level is that 95% of the time, samples taken from the different factor levels that share a letter on the Tukey test will have statistically similar means. The Tukey test supports the ANOVA analysis in that not all of the connections have similar means. Most of the pairs have statistically similar means between 11.12 and 9.87 Ω . Specifically, all but connection two (which has a higher

resistance), and connections four and six (which have lower resistances, though they are similar to each other) are similar.

In order to determine if these resistances are unacceptably high, a short test was run in which a commercial solar cell was connected in series to a variable resistor and run through a voltage sweep. The comparison of the max power point should give a good idea of how much built in resistance is or is not acceptable. Table II shows the resistance value, short circuit current, open circuit voltage, and maximum power.

Table II: Solar cell properties based on the series resistance.

Resistance (Ω)	Short Circuit Current (mA)	Open Circuit Voltage (V)	Maximum Power (mW)
0	57.7	6.788	256.1
23	48.9	6.103	155.8
65	46.6	6.027	115.6
144	37.8	5.988	59.36
278	19.5	6.020	29.13

3.4 Discussion

3.4.1 Series Resistance Effect on Maximum Power

From Table II, the open circuit voltage of the solar cell with no resistance gives us a good idea of how many individual, distinct modules compose it. The theoretical voltage of a single silicon pn junction is .5 V (Kasap, 2006). Assuming the solar cells are close to ideal, there are fourteen or fifteen modules. Though the maximum power does not scale linearly, a resistance of 35 Ω (2.5 Ω for 14 cells) should give somewhere

between 135-140 mW, which is barely half of the power with no connected resistance (256.1 mW). Assuming we used the lowest measured resistance value for Test 2, the total resistance of 14 cells would be around $25\ \Omega$, which corresponds to a maximum power in the tested solar cell of around 155 mW, which is still low. Based on these results, it would be ideal to get the resistance to around one or less ohm per cell.

3.4.2 Reducing Series Resistance

Due to the reduction of power from relatively low resistances, it is clear that all parameters of solar cells must be adjusted in such a way as to minimize the series resistance and ensure the maximum possible power.

3.4.2.1 Thicker Traces and Trace Material

There are a few ways to decrease the resistance of the contacts. Perhaps the simplest fix is to change their geometry. Though the length and width help determine the spacing and number of fingers due to the area of solar cell that will be covered, the thickness can be pretty freely changed. The only impact with increasing contact thickness is that it takes longer to deposit the metal and costs a little bit more, since more metal is present. In terms of benefit, the percentage increase in thickness is the same percentage decrease in resistance (Bowden, 2008). Gold, due to its rarity and resistance to corrosion, is very expensive, so only a minimal amount can be afforded. Aluminum is significantly cheaper and has a comparable conductivity to gold ($2.6\ \mu\Omega\cdot\text{cm}$ for aluminum versus $2.1\ \mu\Omega\cdot\text{cm}$ for gold (Wikipedia)). It is much less costly to deposit more aluminum onto a solar cell, meaning that changing material and increasing thickness of the contacts is a viable option for decreasing the resistance in the cell and increasing

performance. The added benefit of using aluminum is that it is much less expensive than most other metals used in solar cells. The downside is the aluminum spiking talked about in the previous projects section. One way to reduce the effects of aluminum spiking is to use an alloy consisting of 98.5% aluminum and 1.5% silicon (Savage, 2013; Lindholm, 1982). This means that the aluminum contacts already have silicon and therefore don't as readily diffuse into the silicon. The drawback to using an aluminum-silicon alloy is that the contact resistance is significantly increased. Figure 33 shows a graph of the resistance versus the contact area for the pure aluminum and the aluminum-silicon alloy.

Figure 33: Interfacial contact resistance vs. contact window area for aluminum (dotted line) and a 98.5% aluminum 1.5% silicon alloy (solid line). (Lindholm, 1982)

Regardless of material, metal resistance can be reduced through a process called sintering. Sintering encourages the coalescence of grains in the metal, resulting in larger

grains and less resistance. The only downside to sintering is that it encourages aluminum spiking.

Another option for contact material is a silver paste. This material is often used in solar cells in industry, and thus is proven to work. Silver-tin paste, which is a colloid of micro- and nanoparticles in a flux material that is melted and solidified, has a resistivity of about $7.7 \mu\Omega\cdot\text{cm}$, which is almost four times that of gold and slightly over three times that of silver (Seiward, 2011). Unlike gold and aluminum, however, it is easy to make very thick, thereby reducing the resistance in the contact elements. The process for applying the silver paste is to begin by laying a metal stencil over the solar cell. Then a squeegee applies a thick layer of silver paste to the stencil, which is then lifted off, leaving the correct pattern on the solar cell. Once the stencil is removed, the solar cell is put in an oven, which melts the solder and allows it to solidify when cooled (Lin, 2011).

Another benefit of silver paste is that it is easy to attach to a network of traces that connect to other solar cells. One of the problems with the conductive epoxy is that there was a distinct junction with the metal trace, which usually displays a higher resistance. If both the top contact and the traces on a separate wafer were made of silver paste and were connected together with silver solder, there would be no boundary between the different sections, which would reduce resistance.

3.4.2.2 Heavy Doping Under Contacts

Another feature that will reduce the contact resistance between the metal contacts and the silicon is a heavily doped layer right under the contacts. Ideally, we want there to be no resistance to electron flow at the contact point of the metal to the silicon. Such a

low resistance setup is called an Ohmic contact, while a contact that allows current through based on its voltage is called a Schottky diode. In order to achieve an Ohmic contact, the metal and underlying doped silicon must have a similar work function. N-type silicon has a Fermi level that is closer to the conduction band than the valence band, and p-type silicon has a Fermi level closer to the valence band. Heavier doping moves the Fermi level to greater extremes than normal. To increase the Fermi level, thereby decreasing the work function, a heavily doped n-type layer is needed. Typical metals, such as aluminum (~ 4.3 eV) and silver (~ 4.5 eV), have smaller work functions than silicon (~ 4.7 eV) (Bowden, 2008; Kasap, 2006; Warwick, 2011). In order for the electrons to cross unimpeded from one medium to the other, the work functions should approximately match before coming into contact, which means that the work function of the silicon should be reduced an amount based on the contact material. Figure 34 shows an energy diagram of an Ohmic contact.

Figure 34: Ohmic contact between a metal (left) and semiconductor (right). The semiconductor band structure is bent down at the metal contact due to the abundance of electrons present in the metal structure. Note that electrons cannot occupy the area between E_C and E_V , so the closer E_F is to E_C , the more freely electrons can move between mediums. (Warwick, 2011)

The only drawback to heavy doping is that the diffusion length is decreased in heavily doped regions. On the plus side, heavy doping for the region in contact with metal aids in preventing surface recombination. The area right under the contact is not subject to bulk electron transport, meaning that there is no detriment to the heavier doping. For this reason, only the area in contact with metal should be heavily doped. Unfortunately, the measurement of small resistances and accurately measuring the contact resistance is difficult and cannot be done in the materials engineering labs at Cal Poly. This means that all resistance measurements in this section may not be very accurate, which may account for some of the variance in Figure 31.

3.4.3 *Balancing Contact Area and Power Loss*

The whole point of testing the traces is to improve the efficiency of the solar cell by decreasing the power lost to the various resistance elements. Minimized resistance means that less power is lost to the resistive elements. Any power lost in resistive elements is equal to Equation 3. Note the following list of equations indirectly comes from a number of sources. Variations on these equations was given in the different sources and the intermediary equations were re-derived from information and definitions present in all of them (Bowden, 2008; Bonneau, 2006; Serreze, 1978). The final equations are consistent with literature.

Equation 3: Incremental power loss in a resistive element

$$dP = I^2 dR$$

This equation also shows that less power is lost if current is less, but more current means more power total. The drawback is that the easiest way to decrease the resistance is to make the contacts bigger, which covers more of the solar cell. Any area covered by the contacts cannot generate minority charge carriers, which means that the percent coverage is the percent loss due to shadowing. Clearly, there must be some balance between the amount of coverage and the resistance to flow encountered by the electrons. Note that since the bus bar in a typical solar device takes up the entire length of the cell, we will ignore any effect of the bus bar. This means that the area of the solar cell, A_{cell} , is the total area minus the area of the bus bar. Equation 4 shows the specific formula.

Equation 4: Percent area fraction of fingers

$$\%A_f = \frac{L_f w_f N_f}{L_f (S + w_f) N_f} = \frac{w_f}{S + w_f}$$

Where L_f is the length of the finger, w_f is the width of the finger, N_f is the number of fingers, and S is the spacing between the fingers (Bowden, 2008).

3.4.3.1 Surface Power Loss

The first resistive element that it makes sense to talk about is the resistance on the top of the solar cell. When an electron is generated in the p-type region, it diffuses toward the junction, through the n-type layer, and makes it to the surface. The movement of the electron is assumed to be perpendicular to the surface of the solar cell. Once at the surface, it encounters the sheet resistance of the material along the surface, which causes some power loss. The current term in the power loss equation is defined in Equation 5.

Equation 5: Current term for power loss for sheet resistance

$$I = J L_f y$$

Where J is the current density and y is the distance to the finger from halfway between fingers. The incremental resistance term, dR , is shown in Equation 6.

Equation 6: Incremental resistance term for power loss for sheet resistance

$$dR = \frac{\rho_s}{b} dy$$

Where ρ_s is the sheet resistivity in Ω/square . It is important to note that this is only for the area from halfway in between the fingers to a finger, which means that each finger correlates to twice this amount of resistance and twice this amount of current. First we take the integral of $I^2 dR$ from zero to $S/2$ (where S is the spacing between

fingers), then multiply the result by 2, since the integral only represents the area on one side of the finger. After all this we get the total power loss due to resistance along the surface, which is shown in Equation 7.

Equation 7: Resistive power loss due to sheet resistance

$$P_{Surface} = \frac{N_f J^2 L_f \rho_s S^3}{12}$$

In order to get the percent loss from the surface, the above power loss on the surface is divided by the total power theoretically generated by the solar cell. This total power is defined in Equation 8.

Equation 8: Total theoretical power generated by a solar cell

$$P_T = J S L_f N_f V_{MP}$$

Where V_{MP} is the voltage at maximum power. Finally, to find the percent power loss due to the surface resistance of a solar cell, we divide $P_{Surface}$ by P_T . This division results in the percent resistive power loss due to the sheet resistance is shown in Equation 9.

Equation 9: Percent resistive power loss due to sheet resistance

$$P_{\%Surface} = \frac{\rho_s S^2 J}{12 V_{MP}}$$

3.4.3.2 Finger Resistance

Since the fingers on a solar cell are also resistive elements, they have a power loss of $dP = I^2 dR$. Each finger has a current running through a finger is equal to the current

produced by the semiconductor on each side of it extending halfway to the next finger.

This current is shown in Equation 10.

Equation 10: Current term for resistive power loss for finger resistance

$$I = JxS$$

Where x is the distance along the finger. The incremental resistance of the finger is a simple calculation of the resistance based on the resistivity of the metal and its physical dimensions, shown in Equation 11.

Equation 11: Incremental resistance term for resistive power loss for finger resistance

$$dR = \frac{\rho_m dx}{w_f t_m}$$

Where ρ_m is the resistivity of the metal used in the contacts, dx is the incremental distance along the finger, and t_m is the thickness of the metal. Taking the integral of $I^2 dR$ from zero to L (the length of the finger) and multiplying by the total number of fingers gives us Equation 12.

Equation 12: Resistive power loss due to finger resistance

$$P_{finger} = \frac{N_f L_f^3 J^2 S^2 \rho_m}{3 w_f t_m}$$

Dividing this value by P_T gives us Equation 13.

Equation 13: Percent resistive power loss due to finger resistance

$$P_{\%finger} = \frac{L_f^2 J S \rho_m}{3 w_f t_m V_{MP}}$$

3.4.3.3 Finger Optimization

The percent power losses can all be added up to find the total power loss based on the geometry of the top contact layer, specifically the fingers. From adding up these three equations, we get Equation 14.

Equation 14: Total percent resistive power loss based on finger area, sheet resistance, and finger resistance

$$\%P_{loss} = \left(\frac{w_f}{S + w_f} \right) + \left(\frac{J\rho_s S^2}{12V_{MP}} \right) + \left(\frac{SJL^2\rho_m}{3w_ft_mV_{MP}} \right)$$

Table III shows some standard values for these variables (Bowden, 2008; Hannebauer, 2011; Seiward, 2011).

Table III: Approximate values for Equation 14.

Factor	Value
Current Density (J)	.035 A/cm ²
Sheet Resistivity (ρ_s)	20 Ω
Metal Resistivity (ρ_m)	2.6•10 ⁻⁶ $\Omega\cdot\text{cm}$
Max Power Voltage (V _{MP})	.23 V
Metal Thickness (t _m)	1.0 μm
Finger Length (L)	1 cm

V_{MP} will be assumed to .23 V, since that is the value according to Figure 26: Voltage versus Current characteristics of the SOI solar cell. The blue line on the graph is the voltage versus current function, while the red line is the power versus current

function.. Since aluminum is available at Cal Poly, the table shows the resistivity of aluminum and assumes a relatively thick metal layer at 1.0 μm . Finally, the length of the finger typically goes all the way out to the edge. Unlike V_{MP} , J at max power was found in literature to typically be .035 A/cm² (University of Illinois). Since small islands will be created, the finger length will be assumed to be 1 cm. In a solar cell array made on a single wafer, this number will be on the scale of .5 cm. Finally, finger width will be held constant, but will be analyzed at different values. The power loss and ideal finger spacing will be calculated for width equals .1, .05, .01, .005, and .001 cm.

This equation was analyzed in Microsoft Excel such that all variables except finger spacing were held constant. The percent power loss trend based on finger spacing was determined by finding the minimum point of the graph produced by the equation. The ideal spacing corresponds to the minimum power point of the graph. Table IV shows the spacing values used along with the minimum power loss and corresponding spacing, and Figure 35 shows the graph produced with these values.

Table IV: Minimum power loss values and corresponding finger spacing based on width of finger.

Wf	S	P
0.1	0.5	0.236666667
0.05	0.45	0.162241546
0.01	0.25	0.084140787
0.005	0.2	0.076532091
0.001	0.15	0.08618393

Figure 35: Fractional Power Loss vs. Finger Spacing based on five different values of finger width. The graph contains the trend that reducing finger width and spacing decreases power loss in the solar cell.

The trend shown in this analysis is that minimizing finger width while also keeping a very fine control of the finger spacing also minimizes power loss. The minimum power loss is achieved at a finger width of 50 μm , with a corresponding finger spacing of 1 mm. A finer surface analysis can give a more exact number, but the importance of Figure 35 is that there is a minimum power loss. Additionally, if the fingers are so small as to be broken in subsequent steps, severe power losses will be incurred. The labs' capabilities should always be incorporated and the closest width to 50 μm should be used.

One final note on this analysis is that it does not incorporate the resistance within the wafer or the busbar, as well as the differences in generated power with surface texturing, surface passivation, or varying thicknesses. Equation 14 is only intended to aid in the design of the finger width, spacing, and material concerns.

4 DISCUSSION AND CONCLUSIONS

4.1 Summary of Results

4.1.1 *Thin Solar Cell Test*

A solar cell made with a 10 μm thick silicon has a fairly low power output, around .594 mW. Compared to solar cells made with a 500 μm thick silicon wafer, they had less than half of the maximum power output. There are things that can be done to the process to improve the efficiency. These include texturing the top of the wafer, adding a passivation layer, and reducing the width of the traces. To improve the efficiency even further, the wafer could not be an SOI wafer. This would allow the addition of a rear reflector, a flat pn junction, and the ability to have a busbar-finger top contact.

4.1.2 *Connection Test*

The main conclusion from the connection test showed that the traces should not be connected together using a silver-filled epoxy. Using a commercial solar cell and a potentiometer, the power versus resistance was tested. It was found that it takes a small amount of resistance to drastically reduce the efficiency of a solar cell. In order to combat mitigate this power loss, two major factors were considered: contact material and contact shape.

Based on research, instead of gold contacts with a silver-filled epoxy, an industry standard silver paste similar to lead-free solder should be used. As for the contact dimensions, the equations for power loss in the fingers were derived and the ideal finger

and spacing relationship was derived, and is based on current density, contact resistivity, sheet resistivity, length of the fingers, thickness of the contacts, and max-power voltage.

4.2 Future Work

There are two possibilities for future work: the best possible solar cell array that can be made with current technology and the best solar cell that can be made at the lab at Cal Poly.

4.2.1 Factors for Consideration

One of the aspects of the solar cells made at Cal Poly that is least ideal is the material of the solar cell itself. The only bulk material that we have the ability to process at Cal Poly is silicon, which has an indirect band gap. For reasons described in section 1.2.5, indirect band gap materials need to be much thicker to absorb the full solar spectrum of light, and even then it is less efficient. Ideally, the solar cell would be made of a direct band gap material like GaAs. GaAs, as mentioned before, requires only about 5 μm thickness to absorb the entire solar spectrum. In addition, it has an electron minority carrier diffusion of 2 μm even in a very heavily doped diode. This value can be as high as 20 μm in a lightly doped GaAs diode, meaning that GaAs is a good choice of material to make thin and efficient.

The other material to look at is the contact material. Ideally, the best material will have a low contact resistance, low bulk resistivity, and low connection resistance. Some of these materials have been discussed in section 3.4.2.1, so a summary will be given here.

Gold has a very low resistivity, but it is expensive to deposit which means that gold layers are typically thin. It does, however, have a very low contact resistance at small currents, so connection between cells is not a problem. Aluminum is more feasible to coat a wafer in due to its low cost, but has the potential to cause aluminum spiking, which short-circuits the solar cell rendering it useless. Using an aluminum-silicon alloy as the contact metal can mitigate this, but it has a downside of having a higher contact resistance. Lastly, there's silver paste that can be squeegeed on very thick in order to reduce resistivity. It also is very easy to use the paste to connect multiple modules together, whether or not the actual contacts are made with the silver paste. (Bowden, 2008; Lin, 2011; Lindholm, 1982; Savage, 2013; Seiward, 2011)

Finally, the form of the solar cell array is dependent on the available technology. The lab at Cal Poly does not have a machine that can polish a wafer to near atomic flatness, which means that an island design with the area in between etched out and filled in (such as was tried in 2010 and 2011) will not work. With different facilities available, different solar cell arrays can be made.

4.2.2 Limitless Facilities

With unlimited facilities and resources, the ideal solar cell array that can be made will look vastly different than anything that can be made at Cal Poly. The materials used, connection methods, and processing all consist of aspects that are not possible in our lab. One major difference with an ideal solar cell array is that it will take the form of the 2010 or 2011 Cal Poly senior project in that it will not have a glass top. The glass top, though clear, is a place that is prone to reflecting light, meaning that less would get to the solar

cell itself. Likely, the best single wafer solar cell array will have islands of semiconductor on an insulating substrate, with a material filling in the area between islands and interconnects deposited across the filler.

GaAs, like silicon, is typically grown via Czochralski growth (CZ) in which a single crystal ingot is drawn out of a liquid GaAs melt. It is then cut with a diamond saw and polished to an atomically flat surface. The GaAs wafer is cut just thin enough that it can be handled and bonded to a stronger substrate, such as sapphire. First though, the GaAs would have to be doped so that it can work as a solar cell. Also, the sapphire surface would be coated in a silver paste, which will serve as the back contact. The paste will be cured, bonding the GaAs to the sapphire. A photoresist mask will cover the top of the GaAs wafer so that some of it can be etched away, likely by reactive ion etching (RIE), all the way down to the silver paste. The tops of the GaAs wafers would then be covered with gold, as thick as can be afforded, and patterned to the ideal grid measurements. Once the traces are on, the surface would be textured via RIE and passivated via chemical vapor deposition (CVD) to decrease reflection and surface recombination, respectively (Lee, 2004). Finally, something would need to connect the top of one solar cell to the bottom of the next one. This would likely be a piece of conductive tape, or more silver paste with a piece of insulator that prevents the short-circuit of the n- and p-type semiconductor.

4.2.3 *Capabilities at Cal Poly*

The process in the previous paragraph contains materials and steps that are not workable at Cal Poly. The following paragraphs outline a process that will result in the best solar cell that can be made in the microfabrication lab at Cal Poly.

There is a significant trade-off when deciding what form of silicon should be used. A standard 500 μm thick wafer is thick enough to absorb the full solar spectrum of light, but it is difficult to bond to a substrate that will hold the array together and difficult to etch through without any negative consequences. On the other hand, an SOI wafer is easier to work with and will hold together easier, but it is too thin to absorb the full solar spectrum, even with some heavy surface texturing. The best option is to buy or grind down a thick p-type wafer to a thickness of around 70-100 μm . That wafer can then be doped with an n-type layer on top before anything else. The next step will be to connect the back of the silicon wafer to a glass wafer using a silver paste, just like in the ideal array. Depending on the adhesion of the silver paste to the glass wafer, a layer of titanium may need to be deposited so that nothing detaches in the following steps. Once the paste is cured, a mask would be placed on top of the wafer and it would be etched into islands using either RIE or with a tetramethyl ammonium hydroxide (TMAH) etchant to separate the silicon into islands, ideally without damaging the cured silver paste layer.

In order to finish the electrical separation of the silicon islands, the silver paste (and titanium layer, if applicable) would need to be etched away so that some area is still exposed. A thick layer of aluminum, likely with 1.5% silicon in the metal, will then be deposited and patterned into the ideal grid that minimizes the resistive power loss. In order to reduce reflective losses and decrease the optical length, the assembly thus far

would be etched in the RIE for 30-60 seconds, which will rough-up the surface. Finally, some conductive tape would be used to connect the solar cells together in series and some more silver paste would be used to attach wires to both sides of the array.

The only one of these steps that is not readily available at Cal Poly is the ability to grind a silicon wafer down to 70-100 μm . It is still a valid step for two reasons: 1) because the solar cell array is simply not feasible without a thinner wafer, and 2) there is a chemical-mechanical polishing (CMP) company in San Luis Obispo that is willing to aid in school projects.

4.3 Conclusion

Based on the properties of solar cells, specifically what affects their ability to absorb light and convert it into electricity as well as where power is lost in the system, two processes were proposed that will result in a functioning solar cell array using only clean room fabrication processes. One uses processes and materials that will result in a very advanced solar cell array, while the other utilizes only processes and materials available at Cal Poly. The latter process, which is the main focus of this study, consists of proven steps that have not been utilized before at Cal Poly. In theory, it results with a solar cell array that is all on one wafer and has a voltage equal to half of the number of silicon modules. Each silicon solar cell would have a diffusion length that is greater than the optical length and is approximately as thick as the optical length. The form of the metal contacts should result in a minimum power loss and the shape of the pn junction should produce a standard current versus voltage curve. As long as wafers can be ground

down to the correct thickness, this process is entirely feasible to accomplish in the microfabrication lab at Cal Poly.

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APPENDIX A: SOI SOLAR CELL PROCESSING

The following color key distinguishes material for both Appendix A and B:

N-Type
P-Type
SiO ₂
Photoresist
Gold
Titanium
Silver-Filled Epoxy

Full description of the processing for the SOI solar cell test, with graphical representations of the device step by step.

The solar cell starts out as a SOI wafer with a 490 μm thick silicon handle with an oxide layer on it. On top of the oxide layer is a 10 μm epitaxially grown layer of single crystal n-type silicon.

First, a 5000 Å thick thermally grown oxide layer was grown on the SOI wafer. This was accomplished in a wet oxygen environment at 1050°C for 1.5 hours.

A layer of positive Photoresist was spun onto the oxide layer using a Bree Cee 200X Spin Coater. The planarization step of the spinning process took place at 4000 RPM for 20 seconds and resulted in a 1.0-1.2 µm thick layer. Afterwards, it was soft baked at 90°C for one minute.

The Photoresist was exposed and developed. A Canon PLA501FA Aligner was used for the light exposure and a CD-26 Microposit developer was used. The developer is 2.5% TMAH and took approximately two minutes to develop the Photoresist. After the development, the wafer was hard baked at 150°C for one minute.

In order to use the oxide layer as a diffusion mask, the wafer was submerged in a HF solution for approximately 6 minutes in order to etch through the exposed oxide layer through the Photoresist.

After the diffusion mask is finished, the Photoresist was stripped off the wafer using an 1156 microposit remover at 50°C for 15 minutes.

A solutionized dopant was spun onto the wafer in order to dope the p-type regions of the solar cell. The main component in the dopant is dissolved boron.

The dopant was driven into the solar cell at 1050°C for 1.5 hours to a depth of about 2 μm .

After the dopant was driven in, the wafer was once again submerged in a HF solution

Using a Denton Desk V Sputtering System, a .2 μm thick gold layer was deposited on the wafer.

A layer of positive Photoresist was spun onto the gold layer. The planarization step of the spinning process took place at 4000 RPM for 20 seconds and resulted in a 1.0-1.2 μm thick layer. Afterwards, it was soft baked at 90°C for one minute.

The Photoresist was exposed and developed. A [aligner] was used for the light exposure and a CD-26 Microposit developer was used. The developer is 2.5% TMAH and took approximately two minutes to develop the Photoresist. After the development, the wafer was hard baked at 150°C for one minute.

The traces were etched out using a gold etchant at room temperature. It only took a few seconds for the etchant to etch through the gold.

After the traces were finished, the Photoresist was stripped off the wafer using an 1156 microposit remover at 50°C for 15 minutes.

APPENDIX B: INTERCONNECT TEST PROCESSING

Full description of the processing for the interconnection test, with graphical representations of the device step by step:

Test 2 starts with a glass wafer.

Using a CRC-150 Sputtering System, a 1 μm thick titanium layer was deposited on the wafer.

Using a Denton Desk V Sputtering System, a .2 μm thick gold layer was deposited on top of the titanium layer.

A layer of positive Photoresist was spun onto the gold layer with a Bree Cee 200X Spin Coater. The planarization step of the spinning process took place at 4000

RPM for 20 seconds and resulted in a 1.0-1.2 μm thick layer. Afterwards, it was soft baked at 90°C for one minute.

The Photoresist was exposed and developed. A Canon PLA501FA Aligner was used for the light exposure and a CD-26 Microposit developer was used. The developer is 2.5% TMAH and took approximately two minutes to develop the Photoresist. After the development, the wafer was hard baked at 150°C for one minute.

The traces were etched out using a gold etchant at room temperature. It only took a few seconds for the etchant to etch through the gold.

The wafer was then submerged into a titanium etchant solution at room temperature for approximately one minute.

After the traces were finished, the Photoresist was stripped off the wafer using an 1156 microposit remover at 50°C for 15 minutes.

For the gold on silicon pieces that connect the traces together, we started with a n-type silicon wafer.

Using a Denton Desk V Sputtering System, a .2 μm thick gold layer was deposited on top of the titanium layer.

Using a scribing tool, scratches were carved into the wafer making small rectangles. The wafer was then broken along the line of the scratches resulting in small silicon pieces that can be used to connect the interconnects on the traces wafer.

Using Ted Pella H22 Epo-Tek silver filled conductive epoxy, the silicon pieces were connected to the traces so that everything is in series. The epoxy was cured at 80°C for one hour.

APPENDIX C: INTERCONNECT TEST RAW DATA

The following table is the raw data from the ten interconnects in 3 INTERCONNECT TESTING, each tested ten times.

Test Number	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
1	9.2	11.1	10.3	9.1	9.6	8.3	8.7	9.8	10.7	9.9
2	9.3	11.7	10.3	9.2	9.4	8.0	8.8	10.6	10.4	9.5
3	10.3	12.0	10.4	9.3	9.5	10.6	9.0	10.8	10.2	10.5
4	10.0	12.0	9.9	9.6	9.4	8.9	9.1	11.2	10.6	11.7
5	9.4	12.1	10.3	9.1	10.2	8.2	10.1	10.4	11.1	10.2
6	10.6	13.6	10.3	9.8	9.7	8.2	9.6	11.6	12.1	10.1
7	10.0	12.4	10.5	9.9	10.1	8.2	13.7	10.4	10.2	12.6
8	10.9	14.2	10.8	9.3	10.4	8.0	9.9	11.4	13.2	11.2
9	9.4	11.4	9.9	9.1	9.1	7.6	10.4	12.9	12.1	11.6
10	10.8	13.3	10.8	10.1	11.3	9.5	11.1	10.5	10.6	11.9