A FLYBACK INVERTER TOPOLOGY WITHOUT ELECTROLYTIC INPUT
CAPACITORS AS ENERGY STORAGE ELEMENT

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ABSTRACT

A Flyback Inverter Topology without Electrolytic Input Capacitors as Energy Storage Element

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In today's PV inverters, the high input capacitance, necessary for the energy storage during the slow 60Hz cycle is provided by bulky electrolytic capacitors. Liquid electrolyte stored in the capacitor is quickly evaporated due to above rating temperatures, leading to a rise in ESR (equivalent series resistance). The resulting elevated heat dissipation reduces efficiency and accelerates degradation, possibly leading to eventual failure of the inverter. The challenge is to replace these electrolytic capacitors with a different energy storage element. This thesis proposes a new inverter using a Flyback transformer to eliminate the use of electrolytic capacitors as energy storage. A 35W inverter prototype was designed and built to demonstrate the operation of the proposed inverter. Results show that the inverter is able to provide a square-wave AC output, without large electrolytic input capacitance, while meeting several design specifications.

Keywords: 2-Switch Inverter, DC-to-AC, Electrolytic Capacitor-Less, Flyback, Solar, Photo Voltaic

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CHAPTER 1

Introduction

Renewable sources of energy have seen a tremendous rise across the globe in the recent years. Sources such as wind, water and solar are becoming more popular and more affordable. The International Energy Agency estimates that in 2009 13.1% of the primary energy supply and nearly one fifth of the total global electricity generation was delivered by renewables [1]. Global investments are soaring as well as \$257B were spent on renewable energy in 2011, a 17% increase from the previous year according to the Collaborating Centre for Climate and Sustainable Energy Finance [2].

Although over the past two decades the use of renewable energy has been steadily increasing, just recently has photo voltaic (PV) emerged to become a recognized member of this movement. In the year 2000, PV appeared for the first time on the statistics of renewable sources that generate electricity and replaced about 100 tons of oil that year. In 2011 this number grew to 21.6k tons as estimated by the Department of Energy and Climate Change [3]. Recent advancements in technology, causing the price of solar modules to fall by almost 50%, resulted in rapid expansions in select countries [2] as seen in Figure 1-1.

Figure 1-1: Annual Generation of Electricity through PV [3]

The most basic commercial PV system consists of solar panels, which are connected to a maximum power point tracker (MPPT), batteries and an inverter to be able to supply home appliances. There are three different types of commercial PV systems: the stand-alone system, the grid-tie with battery backup system and the grid-tie system [4]. The stand-alone system uses a battery bank for storage and an inverter to supply home appliances. The grid-tie with battery backup system is the same as the stand-alone system, while also having the ability of feeding excess electricity to the utility grid. The grid-tie system without battery backup is the most logical choice for areas with reliable grid power, but does not provide backup power during a power outage. The three options are shown side by side in Figure 1-2.

**Figure 1-2: 3 Types of Commercial PV Systems. (a) Stand-Alone (b) Grid-Tie with Battery Backup
(c) Grid-Tie [4]**

Another recent trend is the rising popularity of residential grid connected PV systems. Not having to rely on utility companies to supply your home with power is an advantage to some. However, receiving payment from distributors for excess electricity, while avoiding the installation and maintenance cost of battery banks appeared attractive to more consumers, especially when living in suitable areas, such as California. In 1998, the first renewables and self-generation programs emerged, marking the beginning of the self-supplying era. In 2007, the new solar homes partnership and California solar initiative started, further energizing the movement [5]. The results are shown in Figure 1-3.

Figure 1-3: Grid-Connected PV Installed Capacity in California [5]

As the PV industry experiences such rapid growth, all aspects of the product are being taken into consideration. For the commercial user the most important statistic is the return on investment, therefore price and efficiency will naturally be the dominant approach any profit oriented manufacturer will take. Any part, from the individual cells, to the panels, to the MPPT to the inverter will be the focus. As it turns out, shading can be detrimental to the output of the PV system, therefore “probing” each individual cell, instead of entire rows may become the standard. This, however, puts increased pressure on the inverter from multiple perspectives such as size, price, efficiency and life-time. In

turns, this poses further technical challenges to inverter manufacturers to produce inverter technology that will improve the overall performance of grid-tie PV systems.

CHAPTER 2

Background

In this chapter background information on the objective of the proposed design is provided. Initially inverters are examined, more specifically what they are and why they are useful. A close look will be taken at currently available topologies, including their specifications, strengths and downsides. One particular drawback to be considered will be the input capacitor and the predicament its significance implies.

2.1 What is an inverter?

An inverter is a device that converts a DC voltage to an AC waveform. It is basically an inverse rectifier and hence received its name. Using transformers and switches, both the amplitude and the frequency of the output signal can be adjusted to meet the specifications. Shown in Figure 2-1 is the block diagram of a modern 2-stage inverter, connected to the output of a solar panel and feeding the inverted current into the grid [6]. On the far left is the solar module, outputting a constant DC voltage and a DC current based on the illumination of the sun. It is followed by a capacitor and the switching side of an isolated converter, such as a Flyback or a push-pull converter. Next is the output stage of the converter, which in many cases and as shown here, is succeeded

by a rectifier. The converter allows for adjustment of the amplitude. Finally, the actual inverter portion, an arrangement of synchronized switches, modulating the signal to the desired output frequency, feeds the alternating current into the grid.

Figure 2-1: Modern 2-Stage Inverter [6]

2.1.1 How does a Grid-Tie Inverter Work?

When taking a closer look at the final block in the previous diagram, a configuration similar to the one shown in Figure 2-2 may be found [7]. The switches Q6 through Q9 are IGBTs, operating in PWM mode, are in parallel with freewheeling diodes to offer current paths when necessary. During modulation, they will be in one of three modes: either Q6 and Q9 are active and a positive potential is applied across C4 or Q7 and Q8 are active and a negative potential is applied across C4 or all switches are off. The inductor L3 and the capacitor C4 act as a low pass filter, reducing harmonics [7].

Figure 2-2: General Output Stage of an Inverter [7]

2.1.2 Pulse Width Modulation

GTIs (Grid-Tie Inverters) have strict requirements on their output. The voltage waveform amplitude and frequency need to be in sync with the grid. If the voltage output of the inverter exceeds that of the grid, the inverter is put under stress. On the other hand, an output voltage that is too low may result in the inverter sinking current. Usually the voltage across C4 is slightly higher than the grid voltage and L_{grid} compensates for the difference [7]. The algorithm of the IGBT driver, including the feedback from the grid is rather intricate, but a simplified visualization is shown in Figure 2-3.

Figure 2-3: Visualization of the Gate Driver Voltage Pulses to achieve a Sinusoidal Output [7]

2.2 Currently Available Topologies

In most households that use solar panels, an inverter will already be required whether or not a grid connection exists since most home appliances operate using off-grid AC energy. Having the inverter grid-tied and being able to sell excess electricity to utility companies with little additional effort and cost is hence attractive to all. But whether to select grid-tie and off-grid is not the only choice that needs to be made. Additionally, when buying equipment for a PV project, one has the option between a centralized inverter and micro inverters.

Figure 2-4: A Centralized Inverter (left) and a Micro Inverter from EnPhase [13]

2.2.1 Centralized Inverter

Centralized inverters are popular for large and for household PV installations alike. They have been available for much longer than micro inverters and have proven themselves through quality with efficiencies of up to 95% and through cost effectiveness, as they are generally less expensive. However, there are several disadvantages associated with centralized inverters. One drawback is that if the inverter fails, the entire system will fail and the solar array will be offline until the inverter is replaced. Another weakness is shading. If panels are just partly shaded, the total output may be reduced by 25% or 50% or possibly even 100% [8]. Figure 2-2a and Figure 2-2b show various shading scenarios and the corresponding power output when using a single centralized inverter [9] [10].

Examples of partial-cell shading that reduce PV module power by $\frac{1}{2}$

Figure 2-5a: Partial-Cell Shading [9]

Example of full-cell shading that can reduce PV module power to zero

Example of full-cell shading that can reduce PV module power by $\frac{1}{2}$

Figure 2-5b: Full-Cell Shading [10]

2.2.2 Micro Inverters

Micro inverters can make up for these drawbacks. If one panel is shaded, its output will still decline, however, the rest of the array will not be affected. Micro inverters also operate at the 95% efficiency range and by converting the electricity from DC to AC at the panel level, they have small individual output voltages, rather than one hazardous one. Over their lifetime, it is estimated that solar arrays using micro inverters will harvest 5% to 20% more than installations with centralized inverters. For these reasons, micro inverters are becoming increasingly popular for smaller residential projects, even though the initial cost is higher. However, large, commercial and utility arrays, installed over a wide area to prevent shading, will continue using centralized inverters [13].

2.3 Comparison of Inverter Specifications

Table 2-1 provides a numerical comparison of centralized and micro grid-tie inverters from a large database [11]. Centralized inverters seem to be specifically chosen for each project. They come in a wide variety of power ratings, anywhere from a few kW for smaller household projects to almost 100kW for large scale utility and commercial arrays. While it is convenient to only buy and install one inverter, the specificity implies that an expansion would require either the replacement of the old inverter or the purchase of an additional unit, thus complicating measurements and readouts. The micro inverters on the other hand appear universal and vary very little in rating and price range

throughout. An expansion of an existing array would be easier and EnPhase even advocates the Do-It-Yourself approach [12]. Figure 2-5 shows a centralized inverter (left) and a micro inverter [13].

Table 2-1: Side by Side Comparison of Centralized and Micro Inverter Characteristics [11]

	Centralized Inverters	Micro Inverters
V_{in} (V_{DC})	125 - 600	45 - 62
P_{out} (kW)	.7 - 95	.2 - .25
η (%)	92.4 - 96.5	95.5 - 96
Weight (lb.)	35 - 1,748	3.5 - 4
Price (\$)	990 - 40,235	140 - 180

2.4 Disadvantages of Inverters

Solar is the futuristic way to power anything from individual households to entire business complexes. It is clean, sustainable, renewable energy. What is the reason that even in suitable areas not more people are interested in the idea of powering their appliances, devices, cars and machines independently from utilities? Of course it does take some time planning and it's understandable that some may not be as environmentally motivated as others. However, the main constrain most people seem to have is due to the spreadsheet that shows how this purchase might or might not turn out to be a beneficial decision over the next 25 years. The sooner the initial expense can turn into a profitable investment, the greater the number of investors. The inverter is an essential part in this calculation. Besides the initial price, maintenance and replacement cost due to malfunctions also need to be considered.

2.4.1 Failure of the Inverter

Breakdown of the inverter in any system would be detrimental. In a micro setup, the connected panel would be isolated and would not contribute to the output of the entity. Since the setup continues to operate normally, the sudden decay in energy output may even go unnoticed. In a centralized structure, the entire system would collapse and the total output would become zero. A reliable inverter is hence not only desirable, but in fact a necessity. One of the most common reasons for the failure of the inverter is the breaking of the input capacitors. Traditionally, large input capacitance is needed at the input to sustain the massive energy requirement during the cycles. These capacitors are electrolytic and seem to frequently break as they dry out due to the enormous energy storage as well as the ambient heat [14]. An overhaul appears overdue for old-fashioned inverters such as the one shown in Figure 2-6.

Figure 2-6: Inverter with Large Input Capacitance through an Array of Electrolytic Capacitors [15]

2.5 Attempts to Replace the Electrolytic Input Stage

The conflict of cost vs. reliability regarding the input stage of inverters is not just a recent issue. Many attempts have been made to replace the electrolytic capacitor array, while staying cost efficient and without overly complicating the design. One of these attempts was published in 2007, titled “A Single-Phase Grid-Connected Inverter with a Power Decoupling Function”. The article describes a Push-Pull/Flyback topology that uses a power decoupling circuit to store and provide power when appropriate. The full schematic is shown in Figure 2-7 [25].

Figure 2-7: Push-Pull and Flyback Combination with Power Decoupling Circuitry [25]

This topology uses a mobile method of storing energy, which requires much smaller component values, compared to other circuits. This not only condenses the design, but also allows the use of slightly more expensive, yet more reliable parts. Both capacitors C_{DC} and C_X are film capacitors of value $44\mu\text{F}$ and $50\mu\text{F}$, respectively. On the other hand, the control circuitry of the five switches on the primary side seems difficult to implement, especially when faced with the additional complication of synchronizing the output waveform to the grid.

2.6 Main purpose of Thesis

The proposed design will try to match the existing characteristics of currently available inverter topologies while revising the input stage to avoid relying heavily on the large electrolytic capacitors and additionally retaining a simple control algorithm. The conflict is to replace an element that is as essential to the inverter as the inverter is to a PV system itself. It provides storage for the largely varying output power requirements for the slow, 60Hz cycles, sinking and sourcing current naturally, without further external stimulus. Additional building guidelines include a simple, economical design with as few components as possible and an efficiency of 85% or more. A low component count will likely be synonymous to a price competitive end product and an 85% efficiency design, although at the lower end of today's standard, is acceptable for a low power prototype with non-finalized components.

CHAPTER 3

Design and Simulation

This chapter entails a detailed derivation of all aspects considered and chosen for the proposed inverter. Beginning with setting the design specifications and arguing for the DC-DC topology, each corresponding component value will be calculated. The process of design is thoroughly described and supported with simulations. Throughout, three Linear Technology ICs are introduced and discussed.

3.1 Design Specifications

Listed in Table 3-1 are the design specifications for the proposed inverter. Since this implementation is a prototype, values compared to actual applications are scaled down. The inverter will convert a $50V_{DC}$ input into a square wave with V_{Peak} of 50V at .5A. The goal is a design with an efficiency of 85% or more.

Table 3-1: Design Specifications for the Proposed Inverter

V_{Innom}	40 VDC
V_{Inmax}	50 VDC
V_{Out}	50 VDC
P_{Out}	25 W
I_{Outmax}	0.5 A
V_F	1.3 VDC
f_{sw}	115 kHz
η	85+ %
Output	Square Wave

3.2 Selecting a Topology

The primary purpose in designing this custom inverter topology is to avoid the use of a large, electrolytic input capacitor. This capacitor is in general needed to supply the load with enough energy to last the low frequency output, i.e. the 60Hz grid connection. This storage element cannot be ignored regardless the topology and will need to be replaced with an element or a combination of equally purposeful components. Additionally, to be practical, the topology needs to be as simple, as efficient and as cost effective as existing modules.

After research and thorough consideration the Flyback topology was chosen. The advantage of the Flyback topology is primarily the transformer, which not only offers isolation, but also serves as a storage element with sufficient storage capacity to replace

the electrolytic capacitor, if designed adequately. Further, it is a simple yet elegant topology, requiring few components and hence providing a low loss environment.

One of the drawbacks of the Flyback converter is its large output ripple. Usually to compensate for this flaw, large output capacitance is needed. However, an actual grid-tie inverter will control the output voltage through PWM modulation, hence only a small, high frequency output capacitor will be required.

3.3 The Flyback Converter

3.3.1 Structure

The basic Flyback converter is made up of two isolated sides. The primary side consists of, the input stage, the primary winding of the transformer as well as the regulating switch. The input voltage can be DC or AC. The secondary side consists of the secondary winding of the transformer, which is the isolated connection to the primary side, a diode and a capacitor across the load. A simple schematic of a Flyback converter is shown in Figure 3-1.

Figure 3-1: Basic Schematic of a Flyback Converter

The Flyback converter is comparable to a buck-boost converter with the inductor split, forming a transformer.

3.3.2 Principle of Operation

In steady state, the Flyback converter operates in one of two states:

During the on-state, the switch is closed and current flows from the input through the primary winding and through the switch to ground. Due to the inductance of the primary winding, current ramps up linearly, starting at zero. However, no current flows through the secondary winding, since the voltage induced is negative, reverse biasing the diode. Therefore the energy is stored in the magnetic field of the transformer. For this cycle, the output capacitor will supply the load with energy.

Figure 3-2: A Flyback Converter during the On-State

During the off-state, the switch is opened and no current flows through the primary side. Instead, the secondary winding acts as a continuation of the primary winding, discharging the energy stored linearly into the load and the output capacitor.

Figure 3-3: A Flyback Converter during the Off-State

Therefore, in the ideal case of the Flyback converter, the input and output voltage are related as follows.

During the on-state:

$$D: V_{TP} = V_{in} \quad (3-1)$$

Where:

V_{TP} = Voltage across the Primary Winding of the Transformer

D = Duty Cycle

During the off-state:

$$D': V_{TP} = -V_{out} \times N_{PS} \quad (3-2)$$

Where:

N_{PS} = *Primary to Secondary Turns Ratio of the Transformer*

Volt Second Balance states that the average voltage across an inductor is zero.

Therefore, by adding the previous two equations and setting it equal to zero, the transfer function is derived:

$$\frac{V_{out}}{V_{in}} = \frac{D}{1-D} \times \frac{1}{N_{PS}} \quad (3-3)$$

Note: This is the transfer equation of the simplified model of the transformer, assuming CCM or BCM.

3.4 The LT3748

To take a closer look at the actual implementation, first the LT3748 needs to be introduced. The LT3748 is a switching regulator controller, designed by Linear Technology for the Flyback topology. It has a wide input voltage range of 5V to 100V and is usually used to deliver load power of several tens of watts. It normally operates in boundary conduction mode, so the switch on the primary side will turn on once the current on the secondary side reaches zero. Figure 3-4 shows a typical application of the LT3748, Figure 3-5 shows the block diagram of its internal circuitry [16].

3.5 Transformer Turns Ratio

Designing any converter topology is an iterative process. Many times changing a fundamental characteristic of the design may lead to benefits and drawbacks at the same time. For this design, maximizing efficiency is the objective. Since the main contributors to loss are the diode and the switch, it seems only logical to first vary a parameter that will affect both parts.

The turns ratio of the transformer is directly related to the voltage across as well as the current through the switch and the diode.

The voltage across the NMOS while it is turned off is:

$$V_{DS(MAX)} \geq V_{in(MAX)} + V_{out} \times N_{PS} \quad (3-4)$$

The reverse voltage across the diode is can be derived using mesh analysis on the secondary loop:

$$-\frac{V_{in(MAX)}}{N_{PS}} = V_{out} - V_{RRM} \quad (3-5)$$

Therefore:

$$V_{RRM} = \frac{V_{in(MAX)}}{N_{PS}} + V_{out} \quad (3-6)$$

Where:

V_{RRM} = Reverse Repetitive Maximum Voltage across the Diode

Note: To compensate for slight variations of the input voltage, the maximum value seems more appropriate than the nominal value for these calculations.

Once a turns ratio has been chosen that results in a reasonable drain-to-source voltage for the switch as well as an acceptable reverse bias voltage for the diode, preliminary components are chosen. A basic rule of design is that components with higher ratings have in general other, less favorable, characteristics. For example, a diode that allows a larger reverse voltage, may have an increased forward drop and similarly a MOSFET with a larger V_{DS} rating will likely have a higher R_{DSon} .

3.6 Duty Cycle

After a suitable diode has been found, meeting the V_{RRM} requirement, its forward voltage drop needs to be researched in the datasheet and considered in the following calculations of the duty cycle. Rearranging the transfer function of the basic Flyback model and including the forward voltage drop of the diode, allow for the duty cycle to be more accurately defined as:

$$D = \frac{(V_{out} + V_F) \times N_{PS}}{V_{in} + (V_{out} + V_F) \times N_{PS}} \quad (3-7)$$

Where: $V_F = \text{Forward Voltage Drop of the Diode}$

Once the duty cycle is known, the peak current of the primary winding as well as the RMS current through the diode are calculated. This is important to ensure that the diode and MOSFET chosen meet the current requirements.

The minimum efficiency requirement is assumed to calculate the primary peak current:

$$I_{peak} = \frac{2}{.85} \times \frac{I_{out}}{N_{PS} \times (1-D)} \quad (3-8)$$

Finally the average current through the diode is calculated:

$$I_{D(RMS)} = I_{peak} \times N_{PS} \times \sqrt{\frac{1-D}{3}} \quad (3-9)$$

For the proposed design, Table 3-2 was created to easily overview the options and consequences resulting from the selection of a different winding turns ratio. For these calculations the values from Table 3-1 were utilized.

Table 3-2: Preliminary Results when Choosing the Transformer Turns Ratio

N_{PS}	V_{DSmax} (V)	V_{RDiode} (V)	D_{VinMax}	D_{VinNom}	I_{Peak} (A)	I_{Diode} (A-RMS)
0.5	75	150	0.34	0.39	3.86	0.87
0.75	87.5	116.67	0.43	0.49	3.08	0.95
1	100	100	0.51	0.56	2.69	1.03
1.25	112.5	90	0.56	0.62	2.45	1.10
1.5	125	83.33	0.61	0.66	2.29	1.16

Note: To calculate the peak and RMS current the duty cycle at nominal V_{in} was used.

For the design a primary-to-secondary turns ratio of 1 would be most advantageous. It would allow for an acceptable spread of the power requirements across the components, while decreasing the difficulty of designing a custom transformer.

3.7 Sense Resistor/Switching Frequency

The LT3748 regulates the switching frequency using the current sense resistor connected between the source of the NMOS and ground. During the on-state, the current rises linearly and so will the voltage V_{sense} . Once the threshold of 100mV is reached, an internal SR Latch will reset resulting in a voltage drop to zero at the gate pin, turning the MOSFET off. Hence, by decreasing the value of R_{sense} , the switching frequency can be decreased, as it will take longer for V_{sense} to reach the threshold. This allows for greater power transfer, however, at the cost of a larger output ripple.

For the optimal design, the maximum value of R_{sense} should be chosen to meet the output voltage requirement at the maximum load, to ensure sufficient energy storage time at peak conditions, while minimizing the ripple.

The value of the sense resistor is simply calculated using the peak current of the primary winding:

$$R_{sense} = \frac{100mV}{I_{peak}} = \frac{100mV}{2.69A} = 37 \text{ m}\Omega \quad (3-10)$$

3.8 Primary Inductance of the Transformer

Accurately specifying the primary inductance is one of the most critical tasks when designing a Flyback using the LT3748. The effects of varying the primary inductance of the transformer are much comparable to those of varying R_{sense} values. Lower primary inductance results in higher switching frequency or reduced output ripple,

yet less power transfer since the RMS current through the winding is lower, meaning less energy stored.

The maximum plausible primary inductance is established when considering the minimum switching frequency.

$$L_{Pri (MAX)} = \frac{V_{in} \times (V_{out} + V_F) \times N_{PS}}{f_{sw(min)} \times I_{peak} \times ((V_{out} + V_F) \times N_{PS} + V_{in})} = 55.8 \mu H \quad (3-11)$$

For the minimum possible primary inductance, internal limitations of the LT3748 need to be considered. The sampling circuit has a minimum settle time of 400ns and the minimum sense voltage is 15mV.

$$L_{Pri (min)} = (V_{out} + V_F) \times R_{sense} \times N_{PS} \times \frac{400ns}{15mV} = 51 \mu H \quad (3-12)$$

An additional constraint of the internal circuitry is a 250ns minimum on time of the gate. This restriction is mostly prevalent in designs using low duty cycles yet should not be neglected.

$$L_{Pri (min)} = V_{in} \times R_{sense} \times \frac{250ns}{15mV} = 31 \mu H \quad (3-13)$$

For this design, the objective is to maximize the efficiency at a fixed output power, hence a low inductance value should be selected.

There are in fact several manufacturers that besides supplying a wide range of typical transformers also allow for custom requests. Since this design is somewhat unique, I decided to build my own transformer as documented in more detail in Chapter 4.

3.9 Primary MOSFET

The absolute minimum ratings for the switch have been established when the turns ratio was decided. While keeping the designers dilemma in mind, it is also important to allow for slight discrepancies between calculation and actual implementation. For example, voltage spikes caused by leakage inductance in the transformer may put additional stress on components, especially the MOSFET.

Since the objective is to create a high efficiency environment, a NMOS with low R_{DSon} is preferred. Therefore the IRFB4115GPBF was chosen. It is a single N-channel power MOSFET by International Rectifier, rated at 150V from drain-to-source with a large drain current limit of 104A. The typical R_{DSon} for this device is measured typically at 9.3m Ω and a maximum of 11m Ω .

3.10 Flyback Diode

Similarly to the MOSFET, a diode is selected. For the diode it is important to keep the forward voltage low. The transformer, the switch and the diode are the three critical components of the design. The switch and the diode will be the highest power consuming elements, while the transformer decides how the dissipation is distributed.

For the diode, the RS3G-E3/57T was selected. The V_{RRM} rating for this component is 400V with an average forward current of 3A, exceeding either requirement sufficiently. The forward voltage drop is 1.3V at 2.5A and 25°C. To decrease the impact

of the V_F the turns ratio was chosen in order to decrease the RMS current through the diode and hence lower its power consumption.

3.11 Feedback Resistor Ratio for Desired Output Voltage

As shown previously, the output voltage is controlled using the turns ratio as well as the duty cycle. Once in steady state, the output voltage is controlled using an external feedback resistor network, R_{FB} and R_{REF} , on the primary side as follows:

During the off-state, the voltage at the drain of the NMOS equals:

$$V_{Drain} = (V_{out} + V_{Diode} + I_{sec} \times R_{sec}) \times N_{PS} \quad (3-14)$$

Where: $V_{Diode} = \text{Forward Drop of the Diode}$

$I_{sec} = \text{Current through the Secondary Winding of the Transformer}$

$R_{sec} = \text{Total Resistance of the Secondary Circuit}$

As shown in the block diagram, this voltage is converted into a current by R_{FB} and Q2, which then flows through R_{REF} to ground. When the secondary current reaches 0, this voltage is sampled, fed into an error amplifier with the bandgap voltage as reference. Finally, the result of the error amplifier either adds or subtracts from the current limit until the voltage of R_{REF} is nearly equal to the bandgap reference.

The relationship can be expressed as:

$$V_{Drain} = V_{BG} \times \frac{R_{FB}}{R_{Ref}} \quad (3-15)$$

Where: $V_{BG} = \text{Internal Bandgap Reference Voltage} \equiv 1.223V$

Substituting into the previous equation, and solving for V_{out} :

$$V_{out} = V_{BG} \times \frac{R_{FB}}{R_{Ref}} \times \frac{1}{N_{PS}} - V_{Diode} - I_{sec} \times R_{sec} \quad (3-16)$$

In boundary mode, the output impedance can be assumed to be nearly zero, yet especially for small output voltages, the diode drop should be taken into consideration.

The LT3748 manual suggests keeping R_{REF} at or close to 6.04k, so for an output voltage of 50V, a turns ratio of 1 and neglecting impedance in the secondary loop, R_{FB} is calculated to be:

$$R_{FB} = (V_{out} + V_{Diode}) \times \frac{R_{Ref} \times N_{PS}}{V_{BG}} = (50V + 1.3V) \times \frac{6.04k \times 1}{1.223V} = 253k\Omega \quad (3-17)$$

For R_{FB} a standard 1%, .25W, 249k Ω resistor was selected.

3.12 EN/UVLO

The EN/UVLO pin, short for enable under voltage lockout, is designed to turn the LT3748 on once a set minimum input voltage threshold has been reached. The input voltage is split using a simple resistive voltage divider network and compared to the internal band gap voltage of 1.223V.

$$V_{min} = \frac{R_{top} + R_{bot}}{R_{bot}} \times V_{BG} = \frac{412k\Omega + 15.4k\Omega}{15.4k\Omega} \times 1.223V = 34V \quad (3-18)$$

Where: V_{min} = *Minimum allowable Input Voltage*

R_{top} = *Resistor connected between the Input and EN/UVLO*

Pin

R_{bot} = *Resistor connected between EN/UVLO Pin and Ground*

For my design I chose $R_{TOP} = 412k\Omega$, 1%, .125W and $R_{BOT} = 15.4k\Omega$, 1%, .125W resulting in a minimum input voltage of close to 34V. The main reason behind setting this limit was to prevent the prototype to draw high currents at low input voltages.

3.13 TC Pin Resistor

The TC pin (temperature compensation pin) allows for temperature compensation by producing a current related to thermal change. This current is proportional to $V_{TC} = 0.55V$ divided by an external resistor and is added to the R_{REF} resistor. A correctly valued resistor allows for more accurate measurement of the output voltage by compensating for the negative temperature coefficient of the diode.

The preferred way of determining the value of this resistor is by testing V_{out} over a wide temperature range, and then using the thermal coefficient in this formula:

$$R_{TC} = \frac{R_{FB}}{N_{PS}} \times \frac{\partial V_{TC}}{\partial T} \times \frac{1}{\frac{\Delta V_{out}}{\Delta Temp}}$$

(3-19)

Where: $\frac{\partial V_{TC}}{\partial T} \equiv 1.85mV/^{\circ}C$

$$\frac{\Delta V_{out}}{\Delta Temp} = \text{Measure Temperature Coefficient}$$

For the design the change in the output voltage while varying the temperature was not able to be measured, therefore a default value $R_{TC} = 56.2k$ was chosen.

3.14 VC Pin

The VC pin (voltage compensation pin) compensates the internal error amplifier and helps eliminate noise. Typically it is connected to a capacitor and resistor. Suggested values were $R = 10k\Omega$ and $C = 4700pF$.

3.15 INTVcc Pin Capacitor

The INTVcc pin is connected to ground through a capacitor and supplies current to the gate pin if required. For the design a $4.7\mu F$ capacitor was selected as suggested in the LT3748 manual.

3.16 SS Pin Capacitor

The SS pin (Soft-Start pin) allows delaying the startup of the chip. The pin is connected to a capacitor that is connected to ground and will charge up linearly through a $5\mu A$ until it reaches about $.65V$. I decided on a $1.3ms$ delay. The only reason for this value was to compensate for the startup of additional circuitry in the simulation. To calculate a capacitance for a specific time delay:

$$C_{ss} = i_c \times \frac{dt}{dV} = 5\mu A \times \frac{1.3ms}{.65} = 10nF \quad (3-20)$$

Where: $i_c \equiv 5\mu A$

$dt = \text{Desired Delay}$

$dV \approx .65V$

The schematic and output of the LT Spice simulation using the values previously calculated are shown in Figure 3-6 and Figure 3-7 respectively:

output voltage. By properly designing the output stage, oscillation as seen in this simulation may be avoided. This process is described later on as it pertains specifically to meet the requirements of an inverter, rather than a DC-DC converter.

This concludes the calculations for a DC-DC Flyback converter design with $V_{in} = 40V$, $V_{out} = 50V$ and $P_{out} = 25W$. Turning the design into a DC-AC converter, or more specifically a 60Hz square wave inverter is described next.

3.17 Converting the DC-DC Flyback into an Inverter

3.17.1 Multiple Outputs

The main reason to build a square wave inverter, rather than an inverter that outputs a sinusoid was that a square wave output will put the most stress on the components. A successful prototype may almost guarantee a successful sinusoidal application even at higher power. Designing for a low frequency output at 60Hz, strengthened this idea.

The first step to creating an inverter was to design the Flyback outputting both a positive as well as negative voltage. For a resistive load this meant changing the direction of the current or simply the perspective of the currents direction by repositioning the ground. Figure 3-8 shows the standard secondary side of a Flyback converter, while Figure 3-9 shows an inverted or negative Flyback output stage.

Figure 3-8: Flyback Converter Output Stage

Figure 3-9: Flyback Converter Inverted Output Stage

Both output stages were then incorporated into a single Flyback design, shown in Figure 3-10. The output voltage waveforms are shown in Figure 3-11.

Figure 3-10: Schematic of Flyback Converter with Positive and Negative Output

Figure 3-11: Positive and Negative Output Voltage Waveforms of the Flyback Converter

The output waveforms of the positive and of the inverted, but otherwise identical negative output stages converge symmetrically: equal output power, equal absolute voltage magnitudes, mirrored, yet identical settling waveform. This is the required basis for the inverter.

3.17.2 Combining the Two Output Stages

The second step was to merge both output stages. To be able to see their combined output, one side had to be interrupted, while the other was active. Therefore two N-Channel MOSFETs were added, one to each loop, driven by synchronized, yet inverted square waves. Shown in Figure 3-12 is the schematic of a 250Hz square wave inverter using the LT3748, while merely adding one additional winding to the

transformer, one diode and two N-channel MOSFETs. Figure 3-13 shows the output waveform.

Figure 3-12: Schematic of LT3748 as Flyback Square Wave Inverter

Figure 3-13: Output Voltage Waveform of Flyback Square Wave Inverter from Figure 3-12

Figure 3-13 shows the output waveform of a successfully implemented Flyback square wave inverter. There is still slight overshoot during the transition, which, as previously mentioned, can be improved by designing a proper output stage.

To simplify the design, the NMOS of the negative output loop was replaced with a PMOS. This allowed the entire design to be driven with a single square wave pulse since now the voltage referenced source of each FET was tied together. Previously this was not possible, since the body diodes of each FET needed to oppose the direction of the actual diodes in each loop.

Figure 3-14: Driving the Flyback Inverter using a Single Square Wave Pulse

Attempts to implement the design, by replacing the voltage source with real life high side FET drivers failed at first. No driver existed that allowed the reference voltage of the source to fall below ground. However, the introduction of the PMOS now allowed

for rearrangement of the circuit, with both sources grounded and hence a single square wave as the driver at the desired frequency.

3.18 The LTC6991

The LTC6991 is a low frequency, programmable oscillator. It can be set to output a square wave at a frequency range from 29.1 μ Hz up to 977Hz, which corresponds to a period range from 1.024ms up to 9.54 hours. The acceptable input voltage range for this IC is only 2.25V to 5.5V.

Using the LTC6991 to create a 60Hz output waveform is simple when following the instructions that Linear Technology provides in their datasheet.

The first step is to decide whether the reset pin should be active high or active low. An active high RST pin implies that while the voltage at the reset pin is close or equal to the voltage at V_{in} , all oscillation at the output is stopped. While the RST pin stays low or grounded, the output continues as programmed.

The second step is to choose frequency resistor divider values, depending on the desired output frequency. For the design a 60Hz output waveform was chosen, which corresponds to a period of approximately 16.66ms. Using this information and the decision made in the first step, the resistor values are given in Table 3-3 [17], and is also provided in the datasheet.

Table 3-3: DIVCODE Programming for LTC6991 [17]

DIVCODE	POL	N _{DIV}	RECOMMENDED t _{OUT}	R1 (kΩ)	R2 (kΩ)
0	0	1	1.024ms to 16.384ms	Open	Short
1	0	8	8.192ms to 131ms	976	102
2	0	64	65.5ms to 1.05sec	976	182
3	0	512	524ms to 8.39sec	1000	280
4	0	4,096	4.19sec to 67.1sec	1000	392
5	0	32,768	33.6sec to 537sec	1000	523
6	0	262,144	268sec to 4,295sec	1000	681
7	0	2,097,152	2,147sec to 34,360sec	1000	887
8	1	2,097,152	2,147sec to 34,360sec	887	1000
9	1	262,144	268sec to 4,295sec	681	1000
10	1	32,768	33.6sec to 537sec	523	1000
11	1	4,096	4.19sec to 67.1sec	392	1000
12	1	512	524ms to 8.39sec	280	1000
13	1	64	65.5ms to 1.05sec	182	976
14	1	8	8.192ms to 131ms	102	976
15	1	1	1.024ms to 16.384ms	Short	Open

Figure 3-15: Resistor Network Corresponding to Table 3-3 [17]

For an active low design and a switching period of 16.66ms, R1 and R2 are 102kΩ and 976kΩ respectively.

Lastly, a resistor at the SET pin is required to create an accurate oscillation at the desired frequency. The value of this resistor is determined as shown below:

$$R_{SET} = \frac{50k}{1.024ms} \times \frac{t_{out}}{N_{DIV}} = 101.7k\Omega \quad (3-21)$$

Where: $t_{out} = \text{Desired Output Period}$

$N_{DIV} = \text{Divider Value given in Table 3 – 3}$

A R_{SET} value of $101,721\Omega$ is calculated. $102k\Omega$ is a standard 1% resistor value, resulting in a -1.28% worst case frequency shift, as shown below:

$$\% \text{ Error} = \frac{101,721 - (102,000 \times 1.01)}{101,721} \times 100\% = -1.28\% \quad (3-22)$$

This value is acceptable, since the main goal is to build a prototype that produces a low frequency output signal.

A low frequency oscillator has been designed, laying the foundation for the switch drivers. However, the output waveform of the LTC6991 swings only from ground to the voltage at the input pin, which is at maximum 5.5V. A simple solution to create a switch driver capable waveform is to feed the output signal through an OP-Amp.

3.19 The LT1007

The LT1007 is a basic, low noise OP-Amp. For the operation as a switch driver, the non-inverting input terminal was connected to the same input as the LTC6991 through a voltage divider network that cuts the input voltage in half. The maximum slew rate of the LT1007 is $2.6V/\mu s$. The maximum output current is 30mA. The NMOS of the

secondary side has a C_{GS} of 5165pF, while the PMOS has a C_{GS} of 2121pF. The maximum rate of change is determined below:

For the N-Channel MOSFET:

$$i = C \frac{dV}{dt} \Rightarrow \frac{dV}{dt} = \frac{i}{C} = \frac{30mA}{5165pF} = 5.81V/\mu s$$

Since the P-Channel MOSFET has an even smaller C_{GS} , the maximum rate of change is solely set by the LT1007 and determined to be 2.6V/ μ s.

3.20 The Secondary MOSFETs' Driver

The output of the LTC6991 was connected to the inverting input of the LT1007. This way the output of the OP-Amp swings from rail to rail when the LTC6991 oscillates. The setup and output waveform are shown in Figure 3-14 and Figure 3-15:

Figure 3-16: Driver Circuitry for Inverter Stage

Figure 3-17: Output of Driver Circuitry shown in Figure 3-14

The output waveform of the driver circuitry proves to have sharp edges and fast transitions at precise 60Hz switching. The startup is about 1.25ms which is the reason the soft start of the LT3748 was chosen to delay the turn on by 1.3ms. However, since the Flyback driver and driver circuitry will be driven independently, this startup time is insignificant.

3.21 Finalized Design

The schematic of the complete design is shown in Figure 3-16, as well as the simulated output, shown in Figure 3-17:

Figure 3-18: Full Schematic of Final Design

Figure 3-19: Output Waveform of Finalized Design shown in Figure 3-20

The final output waveform, meeting the specifications mentioned earlier. Once the startup of the Flyback converter is completed, the voltage settles. The transitions are fast and the edges are sharp creating a 60Hz output square wave with 50V_{Peak} and 100V_{Peak-Peak}.

This concludes chapter 3 and the design portion of the project. Chapter 4 describes the process of building the inverter, including detailed description of the components used, how they were arranged using the PCB and general considerations to improve regulation and avoid noise.

CHAPTER 4

Hardware Implementation

This chapter discusses the details of the physical implementation of the proposed design. These include the designing and building of the transformer as well as the process of laying out the PCB using Eagle CAD software. Although LT Spice requires the essential components for the simulation to run correctly, due to its ideality it does not consider the importance of the location of the parts or additional capacitors necessary for the physical model to work properly.

4.1 Transformer Design

The only component of the entire design that is to be custom built is the transformer. As mentioned previously, many characteristics of the project will be affected by its attributes. Accuracy of the turns ratio is important to set the output voltage correctly and the primary inductance will affect the switching frequency as well as the output voltage ripple. An additional property that needs consideration is the leakage inductance. Leakage inductance will cause voltage spikes and ripple at the drain of the primary FET, which in turn will result in having to choose a switch with increased ratings and likely higher loss compared to the simulation.

4.2 Transformer Specifications

In Chapter 3, many of the design requirements, such as the inductance and turns ratio were calculated and decided on and are listed in Table 4-1. Using these parameters, the main objective is to find a suitable core.

Table 4-1: Previously Determined Characteristics necessary for Transformer Design

L (μH)	I_{Peak} (A)	D	N_{PS}
51	2.69	0.56	1

A difficulty, particular to this design, is the additional secondary winding, increasing the required volume of the windings by at least one third. To compensate for this uncommon necessity when laying out the Flyback transformer, the original PCB was designed for a PQ 26/25 core [18]. For the first actual implementation attempt the PQ 20/20 [19] core was chosen, a much smaller core with an area product of about 40% compared to the PQ 26/25. Table 4-2 shows parameters necessary for winding turns and air gap calculation.

Table 4-2: Useful Parameters of the PQ 20/20 [19]

V_e (mm³)	l_e (mm)	A_e (mm²)	A_{min} (mm²)	d_{min(core)} (mm)	d_{max(core)} (mm)	B (T)
2850	4537	6.26E-01	59.1	9	17.35	<0.32

where: V_e = Effective Volume

l_e = Effective Length

$A_e =$ Effective Area

$A_{min} =$ Minimum Area

$d_{min(core)} =$ Inside Diameter of the PQ 20/20

$d_{max(core)} =$ Outer Diameter of the PQ 20/20

$B =$ (Maximum) Magnetic Flux Density associated with this Core

4.3 Transformer Calculations

Once these basic parameters have been researched and established the turns required to achieve the required inductance can be calculated. In equation (4-1) the inductance L is in μH and the effective area is in cm.

4.3.1 Required Turns

$$N = \frac{L \text{ (in } \mu H) \times I_{Peak}}{B \times A_e} \times 10^{-2} = \frac{51 \times 2.69}{.32 \times .626} \times 10^{-2} = 6.85 \text{ turns (4-1)}$$

Since 6.85 turns is physically not possible, it is necessary to round up and hence 7 turns is chosen. This in turn will require for the magnetic flux density to be recalculated. Equation (4-2) shows the calculation of the adjusted magnetic flux density, through the ratio of the calculated turns to the actual turns value that was chosen.

Adjusted magnetic flux density

$$B_{adjusted} = \frac{t_{calculated}}{t_{actual}} \times B = \frac{6.85}{7} \times .32 = .313 \text{ T} \quad (4-2)$$

This is an acceptable value since it is still less than the specified peak flux density B_{Max} of .32 T.

4.3.2 Air Gap

Lastly, for reference, the air gap length is calculated. (4-3) shows the necessary quadratic equation. Parameters are adjusted to be in cm when required.

$$\begin{aligned} l_g &= \mu_o \times N^2 \times \frac{A_e}{L} \left[1 + \frac{l_g}{d_{core(min)}} \right]^2 \times 10^4 \\ &= 4\pi \times 10^{-7} \times 7^2 \times \frac{.626}{51} \times \left[1 + \frac{l_g}{.9} \right]^2 \times 10^4 = 7.68 \times 10^{-3} \text{ cm} \end{aligned} \quad (4-3)$$

The physical implementation of this air gap is described later on.

4.4 Wire Sizing

Before building the transformer, a wire gauge has to be chosen. Many variables need to be considered when choosing the wire for the windings. The diameter of the core

is an issue in this project, hence the diameter of the wire will be important. The diameter of the wire, which is inversely correlated to the gauge, is also proportional to the amount of current that can flow through it without heating up and dissipating too much energy. In this project, the peak current is anticipated to be 2.69A as mentioned in Table 4-1. The RMS current and average current are calculated in (4-4) and (4-5) respectively.

$$I_{RMS} = I_{Peak} \times \sqrt{\frac{D}{3}} = 2.69 \times \sqrt{\frac{.56}{3}} = 1.16A \quad (4-4)$$

$$I_{Avg} = \frac{1}{2} \times I_{Peak} \times D = \frac{1}{2} \times 2.69 \times .56 = .75A \quad (4-5)$$

Additionally, the diameter of the wire is inversely proportional to the frequency at which 100% skin depth is achieved. Skin effect is an important consideration since the estimated switching frequency is 100 kHz. Table 4-3 shows an excerpt from the American Wire Gauge Table, with a range plausible wire sizes for the project.

Table 4-3: Excerpt from American Wire Gauge Table

Gauge	diameter (in)	diameter (mm)	$\Omega/1000\text{ft}$	Max Current Exposed (A)	Max Current Bundled (A)	Max Freq. for 100% Skin Depth
20	0.032	0.8128	10.15	11	1.5	27 kHz
21	0.0285	0.7239	12.8	9	1.2	33 kHz
22	0.0254	0.64516	16.14	7	0.92	42 kHz
23	0.0226	0.57404	20.36	4.7	0.729	53 kHz
24	0.0201	0.51054	25.67	3.5	0.577	68 kHz
25	0.0179	0.45466	32.37	2.7	0.457	85 kHz
26	0.0159	0.40386	40.81	2.2	0.361	107 kHz
27	0.0142	0.36068	51.47	1.7	0.288	130 kHz
28	0.0126	0.32004	64.9	1.4	0.226	170 kHz
29	0.0113	0.28702	81.83	1.2	0.182	210 kHz
30	0.01	0.254	103.2	0.86	0.142	270 kHz

It was assumed that the current ratings were in RMS, although it was not specified. Given Table 4-3 there is not gauge to meet the specifications of the project. While gauges 26 through 30 meet the frequency requirement, while only gauge 20 and 21 would meet the current limitations.

4.5 Multi-Filiar

The solution to this problem is simple, multiple paralleled wires per winding, i.e. bifiliar or trifiliar. This method offers additional advantages particularly useful for this project. For one, current will split equally across each strain, given they are the same length, allowing the use of thinner wires for larger currents. Another is low leakage inductance [21], a desired property for most transformers, but particularly useful in Flyback topologies, further explained in the following section about Snubbers. Finally, the decreased diameter, if the paralleled wires are set side by side instead of bundled,

which is desired since the space from the center of the core to the outer radius is limited, as shown in (4-6).

Available Distance from Inner to Outer Boundary of the Coil Former in PQ20/20

$$d = \frac{d_{\max(\text{core})} - d_{\min(\text{core})}}{2} = \frac{17.35 - 9}{2} = 4.175 \text{ mm} \quad (4-6)$$

Since isolation using multiple layers of Kapton tape are required between each winding as well as at the outer layer and overlapping of wires at the end of the winding will combine to take about .8mm each, the maximum diameter of the wire should therefore be <.6mm.

4.6 Choosing a Gauge

Considering again the switching frequency, current limit and maximum space available, the optimal choice would be trifilar windings of gauge 26. However, trifilar windings offer a challenge in their construction, therefore bifilar windings of wire gauge 24 were selected.

4.7 Building the Transformer

Now that the physical characteristics of the transformer have been calculated, building of the transformer can begin. Figure 4-1 shows the necessary materials needed to build this particular transformer. Every item, from left to right, is listed below. The piece of paper, a thin layer of a napkin for the air gap, is not shown.

Figure 4-4: Parts needed to build the Transformer

Parts List

- 14 Pin PQ 20/20 Coil Former (Transformer Skeleton or Bobbin)
- 2 Halves of the PQ 20/20 Iron Core
- Clamp
- 24 Gauge Wire
- Kapton Tape

The transformer consists of three equal windings, one primary and two secondaries. For maximum coupling from the primary to each secondary, the inner most winding should be one secondary, followed by the primary, followed by the other secondary. Figure 4-2 shows two intermediate pictures of the inner most secondary winding and the primary winding. Each winding is isolated by three layers of Kapton

tape. Additionally, Kapton tape was used at the upper half of the coil former to decrease the surface area and force the windings to overlap each other.

Figure 4-5: Inner Most Secondary Winding (left) and Primary Winding

After all windings and Kapton tape have been completed, the iron core was added, surrounding the six layers. To hold it in place, the clamp was applied. An advantage of using the clamp, rather than keeping the core tight using tape is that the inductance can be measured and, if necessary an air gap can be added, without much complication. Once all modifications have been completed and the inductance has been adjusted to a preferred value, Kapton tape is recommended for additional security. Figure 4-3 shows the completed transformer.

Figure 4-6: Completed Transformer from the Primary Side (left) and the Secondary Side

4.8 Characterizing the Transformer

The final step in the design process of the transformer is to measure the individual inductance of each winding and the leakage inductance. The Multi-Frequency LCR Meter was used to complete this task with the frequency set to 100 kHz to match the application frequency. The individual inductance can be approximately determined by simply measuring across each winding, as shown in Figure 4-4.

Figure 4-7: Measuring Winding Inductance using the Multi-Frequency LCR Meter

This method, however, will include the leakage inductances in each measurement as shown in Figure 4-5 [20]. To find the exact winding inductances, the leakage inductances need to be determined and subtracted. Since the leakage inductance is usually very small compared to the winding inductances, it is negligible. However, at least for the primary winding, it is a crucial characteristic that needs to be determined. Its consequences are further discussed in the Snubber portion, following this section.

Figure 4-8: Measured Inductance when Probing across a Winding [20]

Finding leakage inductance is slightly more complicated and requires shorting all other windings besides the one being measured across. By doing so, the voltage drop across the shorted winding is zero and hence the voltage drop across any coupled winding will be zero. Since leakage inductance does not couple, it solely remains. This concept is shown in Figure 4-6 [20].

Figure 4-9: Measured Leakage Inductance when Shorting any Secondary Winding [20]

4.9 Transformer Characteristics

The inductances of the transformer are shown in Table 4-4. The turns ratio from primary to secondaries is approximately .985, since the secondary windings' inductance

is about equal. This is not only acceptable, but also advantageous since the diode drop and other non-idealities may cause the output voltage to drop below the simulated value. A turns ratio slightly below will hence elevate the output voltage slightly [21]. Also note that the value of leakage inductance is given in nano Henries and is only about .4% compared to any of the other windings.

Table 4-4: Measured Inductances of Transformer

L_P (μH)	L_{S1} (μH)	L_{S2} (μH)	L_{LP} (nH)
51.17	52.94	52.99	194.6

4.10 Snubber/Voltage Clamp

The effects of the previously mentioned leakage inductance will be discussed in this section. Most of the energy is transferred from the primary to secondary winding through the magnetic field of the coupled inductors. However, the leakage inductor cannot transfer its stored energy since it is not coupled and instead will cause a high voltage spike at the drain of the MOSFET. This occurs because the leakage inductor tries to continue the current, when the switch opens and interrupts the path. It acts as if it was a constant current source, supplying any voltage needed to keep the current continuous. Even when faced with an impossible obstacle such as an open. Similarly, a voltage source will output a large current, when shorted.

For comparison, Figure 4-7 and Figure 4-8 show a drain voltage response without and with leakage inductance respectively.

Figure 4-10: Drain Voltage Response of a Primary Flyback MOSFET without Leakage Inductance

Figure 4-11: Drain Voltage Response of a Primary Flyback MOSFET without Leakage Inductance

Although the calculations for Snubber design looked promising originally, in practice they turned out unsuccessful. Hence they were not included in the report. Instead, a voltage clamp was developed experimentally. The results are described and explained in Chapter 5.

4.11 Powering the Prototype

One additional aspect that needs to be taken into consideration for the layout of the board is powering the ICs. The driver of the Flyback stage itself, the LT3748, is located on the primary side and will be powered by the input itself. Its large input voltage range is ideal for the application. On the other hand, the LTC6991 and LT1007 are positioned on the secondary side. Since the topology is isolated, it is not possible to power these two ICs using a power supply connected to the same ground as the input. Instead batteries will be used. Three AAAs of 1.5V each will power the LTC6991, while the rails of the LT1007 are established with two 9V alkaline batteries. All terminals, including output (voltage and ground) will be connected to pin and socket connectors to allow for easy access.

4.12 Additional Capacitors not included in the simulation

Before the actual layout process can begin one final issue needs to be discussed. The placement of additional capacitors that weren't necessary in the simulation. They are meant to protect the components from momentary voltage spikes, decrease noise and increase the overall stability of the circuit. Table 4-5 contains the added capacitors. The

electrolytic capacitor at the input is not used for low frequency storage, but rather high frequency voltage smoothing.

Table 4-5: Additional Capacitors, including Location, Value, Justification and Type

Location	Value	Reason	Type
Input Voltage Terminal	10 μ F	DC Smoothing	Electrolytic
Input Voltage Terminal	2.2 μ F	DC Smoothing/Backup	Ceramic
Input of LT3748	1 μ F	Decrease Noise/Stability	Ceramic
Input of LTC6991	1 μ F	Decrease Noise/Stability	Ceramic
Sense Pin of LT3748	47pF	Suppress Noise Peaks	Ceramic

4.13 PCB Layout

Once the complete schematic has been established and all components have been decided on, the next crucial stage follows, the PCB layout. For the PCB layout process, the software CadSoft EAGLE was chosen [22]. EAGLE (Easily Applicable Graphical Layout Editor) allows the user to add a schematic of the circuit and convert it to an easily modifiable PCB layout editor. Additional features include the ability to create custom components and auto routing of traces to find the closest common nodes. The software is very intuitive and promotes a self-learning environment. For the proposed design two layers and a board size are required, which is supported in the freeware version of EAGLE.

4.14 Design Components

After becoming familiar with the interface, the first step to board design is to add the components that are not found in the EAGLE library. Although the library is

extensive, it is not only difficult to locate each part, but it is also important to verify that they are up to date, by comparing them to a current data sheet. Since this is a tedious process, it is recommended, especially for complex components, to add a verified reference personally. This is a quick and simple step that guarantees accuracy especially after a few iterations.

To begin, the datasheet is researched, which contains not only the electrical specifications, but also the physical outlines. For example, Figure 4-9 shows the package of the IRF6218, a P-channel MOSFET, used in the design [23]. The IRF6218 comes in a TO-220AB through hole package.

Figure 4-12: Package Outline of IRF6218 P-Channel MOSFET [23]

The most relevant information obtained from this data sheet are the dimensions of the outline of the component, as well as the size of the holes that are required. Being

generous with the outline is important to ensure that parts do not overlap and so that there is adequate space to allow soldering and de-soldering if necessary. Also, it is recommended to increase the size of the holes as given in the datasheet by about 50%, which makes it easier to fit and, more importantly, remove the part. Table 4-6 shows the significant data obtained from the datasheet and compares it to the actual values chosen for the implementation [23].

Table 4-6: Dimension Comparison between Datasheet and Actual PCB Imprint [23]

	Datasheet	Layout
Width (mm)	4.69	4.99
Length (mm)	10.54	11.01
Diameter (mm)	.69-.93	1.1

Figure 4-10 shows the simple layout design, which will be imprinted on the PCB. The dimensions (mm) have been added for reference.

Figure 4-13: Package of Through Hole TO-220AB Component

Figure 4-11 shows the corresponding design for the schematic editor. Its shape and size are not significant, but it requires an equal amount of pins, designated by the green circles.

Figure 4-14: Schematic of Through Hole TO-220AB Component

In the final step of the creation of a new component, the pins of the schematic design will be routed to the terminals of the layout component. This process is shown in Figure 4-12.

Figure 4-15: Connecting Pins and Pads from Package and Schematic

The process for a surface mount component is very similar. Instead of vias, surface pads are used. Larger surface pads will notably simplify soldering. Particularly for ICs with close pins it is advantageous to lengthen the pads. Overall, the best advice

during component design is generosity. A complete list of all custom created components, for the proposed design, can be found in APPENDIX A.

4.15 Board Schematic

With all components available, the schematic for the board using EAGLE can be created. This is a simple step, since it just requires copying the LT Spice schematic, with one slight difference: since the proposed design utilizes an isolated topology, the grounds on the primary and secondary sides need to be distinguished. Figure 4-13 shows the schematic of the proposed design in EAGLE. During the hardware implementation some parts were replaced compared to the original design and the complete and updated list of components can be found in APPENDIX B.

Figure 4-16: EAGLE Schematic of Proposed Design

4.16 PCB Layout

The printed circuit board is the foundation of the project. It represents all thoughts and understanding developed throughout research, discussion, simulation and implementation. Attention to details a must. For this project, one of the main objectives was to construct a clean, organized PCB that allows for easy assembly and troubleshooting, even by a third party. Labeling each component consistently throughout, in LT Spice, EAGLE schematic and even imprinted on the PCB was the first step. Staying orderly is easy for a rather small design, such as the proposed, but still good practice for more complex projects. Other specific aspects to consider were keeping the edges of traces dull, by avoiding 90° angles and widening traces when possible to reduce any resistances. Space between the components and the edges of the board allow for safe and secure handling, while easily accessible input and output pins make it easy to set the circuit up. Finally, avoid bridging, for a sleek finish.

Examining the proposed design when taking a step back, two isolated sides, connected and accessible only through the transformer, are found. Each side has a power stage and a signal stage. This is manifested through the PCB, using the board itself as a barrier. The top is used for the power stage, while the bottom holds all control circuitry. Each stage has its own ground plane, two on the primary side, two on the secondary side, only connected through the input or output ground terminal, respectively. Figure 4-14 shows a snapshot of the board (colors are inverted). The white rectangle designates the location of the transformer. The solid red lines signify the power traces and pads, while the blue colored lines represent the signal paths. The dashed lined shapes are the outlines

of the ground planes. The added GND In and GND OUT (white circles) symbolize the ground external terminals.

Figure 4-17: Modified Capture of the PCB focusing on the Ground Planes and Separation of Power and Signal

A closer look at the bottom side of the board reveals another design strategy: keeping components directly connected to ICs as close to the chips as possible. This helps eliminate noise issues and is important for the IC to respond swiftly and accurately. For example, detecting the event of the secondary transformer current dropping to zero through a resistor feedback network at the rate of 100kHz requires precise timing. Long trace distances may interfere or delay the reading. In case of the proposed design, there

are two exceptions to this rule: the INTV_{cc} capacitor and the sense resistor. Both need to be connected to the power ground plane and hence are somewhat distant to the LT3748. Figure 4-15 shows the bottom side of the PCB (as if one is looking through the board). The white circles mark the previously mentioned exceptions. Both are linked to the power ground through multiple vias.

Figure 4-18: Signal Layer/Bottom Side of the PCB Layout (Looking through the Board)

The power side of the board defines the size of the PCB. Contrary to the signal layer, larger spacing is advantageous to prevent components from heating each other up. Additionally, trace widths are wider. Figure 4-16 shows the completed top layer of the board.

Figure 4-19: Power Layer/Top Side of the PCB Layout

4.17 The Printed Circuit Board

This completes the design process of the PCB. Using EAGLE the Gerber files were created. For the printing job Advanced Circuits was chosen. Table 4-7 contains the necessary fabrication parameters [24].

Table 4-7: Fabrication Parameters

Parameter	Value
Number of Layers	2
Board Width (mm)	95.98
Board Length (mm)	64.36
Board Thickness (mm)	1.57
Copper Thickness (mm)	0.035
Solder Sides	Both
Silkscreen Sides	Both
Number of SMD pads	76
Minimum Trace Width (mm)	0.305
Minimum SMD Pitch (mm)	0.203
Minimum Hole Size (mm)	0.5

The top side of the finalized PCB is shown in Figure 4-17.

Figure 4-20: Top Side of Finalized PCB

The bottom side of the finalized PCB is shown in Figure 4-18.

Figure 4-21: Bottom Side of Finalized PCB

CHAPTER 5

Hardware Testing and Experimental Results

This chapter summarizes the hardware test results of the proposed solar inverter prototype. Screen captures of different probing points are displayed, compared to simulation and calculations and evaluated. Additionally pictures of the finalized board and the setup are included.

5.1 Testing Individual Stages

5.1.1 Secondary Gate Driver

Mistakes happen and misconceptions are too frequently made. The likelihood of building the full design and having it work properly the first attempt are miniscule. Hence, the approach taken when assembling the proposed design was to progress slowly and carefully, to verify individual connections and to test in stages. Figure 5-1 shows the output of the secondary MOSFETs' gate driver. It agrees with the simulation, outputting a 60Hz and 50% duty cycle square wave.

Figure 5-22: Gate Driver for Secondary MOSFETs

Further inspecting the gate driver voltage by itself, the rise time is found to be approximately $7\mu\text{s}$. The simulation suggested $6.12\mu\text{s}$. The rise of the square wave is shown in Figure 5-2.

Figure 5-23: Rise Time of Gate Driver for Secondary MOSFETs

5.1.2 Positive and Negative Output Waveform of the Flyback

More intermediate measurements were the individual voltage outputs of the Flyback. The positive output is shown in Figure 5-3 and the negative output is shown in Figure 5-4. As anticipated, both outputs have a magnitude of approximately 50V. The voltage ripple appears slightly larger on the negative output, however, this should not have an effect on the final waveform.

Figure 5-24: Positive Output when Tested Individually

Figure 5-25: Negative Output when Tested Individually

5.2 Completed Board

Figure 5-5 shows the top side of the completed board. A heat sink was necessary for the primary MOSFET due to the leakage spikes at the drain of the component. A solution to this problem is discussed later on, as a custom Snubber is experimentally determined; however, the heat sink was left in place for safety. One component that has been modified from the original design is the inductor at the output. Although the current rating of .8A of the original choice seemed acceptable, it was heating up. The new inductor is rated at 1.4A.

Figure 5-26: Top Side of the Completed Board

Figure 5-6 shows the bottom side of the completed board. No changes have been made from the original layout. The ends of the MOSFETs have not been clipped for measurement purposes.

Figure 5-27: Bottom Side of the Completed Board

5.3 Testing

Figure 5-7 shows the basic testing setup. The input is connected to a DC voltage supply, the output is connected to a resistive load of 70Ω . The batteries, necessary for the secondary MOSFET driver to run, have been attached. A scope meter is used for probing and is hooked up to the drain of the primary FET.

Figure 5-28: Testing Setup

5.4 The Effects of Leakage Inductance

As mentioned earlier, it was necessary to attach a large heat sink to the primary MOSFET since large leakage spikes were causing it to overheat. The primary FET is rated for 150V and, as shown in Figure 5-8, it experienced repetitive voltage spikes of 170V+.

Figure 5-29: Unclamped Primary FET Drain Voltage

To avoid the problem, not only a basic resistor-capacitor-diode Snubber was added, an additional 90V Zener diode was required. The resistor, $6.04\text{k}\Omega$, the capacitors, total of $2.22\mu\text{F}$ and the Zener diode are in parallel. Figure 5-9 shows the drain voltage of the primary FET as a result of this configuration. Ideally, the diode used in the Snubber should have a faster recovery time to contain the oscillation.

Figure 5-30: Clamped Primary FET Drain Voltage with RCD + Zener Snubber

5.5 Switching Frequency and Duty Cycle

Figure 5-10 shows the gate driver of the primary FET. The switching frequency is approximately 106 kHz. This is slower than the simulation and originally anticipated range of 115 kHz to 120 kHz. A consequence of this discrepancy will likely be slightly larger output voltage ripple. The duty cycle was measured to be .53, just below the calculated value of .56.

Figure 5-31: Frequency of Primary FET (Gate)

5.6 Evaluation of Secondary Gate Driver

Figure 5-11 shows the gate driver voltage of the secondary MOSFETs during operation. The voltage ripple is much larger compared to Figure 5-1 when the circuit was not active, which is acceptable. However, after the high-to-low transition there appears to be a reoccurring period during which the ripple remains small (black circle). This might indicate that the P-Channel MOSFET may not turn on immediately. Since PMOS usually have a lower turn on time than NMOS, it may be possible that the PMOS is defective or that the operational amplifier lacks the strength to turn the FET on instantaneously. The problem persisted, even after the P-Channel FET was replaced and according to the data sheets, the gate charge requirement is much lower for the PMOS than for the NMOS.

Figure 5-32: Gate of Secondary FETs during operation

5.7 Final Output

Figure 5-12 shows the final output voltage waveform of the completed circuit. The maximum peak is about 50V and the absolute minimum is about -50V as anticipated. The ripple is less than 5V. Although the transition appears to be relatively quick, the response seems over damped. Decreasing the output capacitance may allow for sharper edges, yet it would also coincide with larger ripple. Figure 5-13 puts emphasis on the output frequency of 60Hz. One notable issue, when running the circuit, is a relatively loud scratching noise, coming from the transformer. It is not unlikely that this can be attributed to the previously mentioned problem of the secondary gate driver.

Figure 5-33: V_{PP} , V_{PMax} and V_{PMin} of Final Output Voltage

Figure 5-34: Frequency of Final Output Voltage

CHAPTER 6

Conclusion and Future Work

6.1 Conclusion of Results

The hardware indicates that the main issue that needs to be resolved is the driver of the secondary MOSFETs. A problem arises if the transformer is discharging its energy and the gate driver inverts its output voltage. In this situation, if all three switches, the primary and the two secondaries are off, then the only path for the current to flow is through the Snubber. For a few nano seconds this is acceptable, however, the delay indicated by Figure 5-11 is not. For that reason the transformer responds with loud rustling noises.

However, overall the results look promising. Although the final output response is over damped, Figure 5-12 proves that the Flyback circuit is capable of fast transitions. A sinusoidal output voltage would not need such rapid transitions as the square wave of the proto type board and is therefore entirely possible. The transformer allows for energy storage at the switching frequency and replaces the large electrolytic input capacitance necessary in traditional inverter design. The current board size is relatively small and may slightly increase to accommodate for components with larger ratings, such as the transformer and the power diodes on the secondary side. However, the board appears cost

effective, given its low component count, including only two FETs necessary for inversion, compared to the traditional four-switch inverter.

6.2 Improvements of Proposed Design

As mentioned previously, the secondary MOSFETs' driver circuitry requires revising. One possibility would be to replace the operational amplifier with a power OpAmp. A power OpAmp will output larger currents and allow for quicker turn-on and turn-off times of the FETs. Another solution could be to add an additional discharge path to allow storage in case all switches are off simultaneously.

On the primary side, the Snubber may need an overhaul, to avoid the use of a heat sink. On the other hand, a FET with increased voltage rating, yet small parasitic capacitance is also a plausible solution. An improvement from the perspective of the layout of the PCB would be to keep components that heat up even further apart.

6.3 Future Work

The design has definite potential to be converted to a higher power application. As mentioned in Chapter 2, a standard micro inverter outputs between .2 and .25 kW as shown in Table 2-1, which is about 6 to 7 times that of the prototype. The input voltage is between 40 V_{DC} and 60 V_{DC}, similar to the current input voltage. The MOSFETs may need to be replaced with IGBTs, but the other components just need a slight upgrade in ratings.

Also, instead of having a square wave, a sinusoidal output would be more realistic to a real life implementation. An additional benefit of choosing a sinusoidal output would be slower transition speed and no sharp edges. Therefore larger output capacitors and inductors could be added to decrease the ripple.

Lastly replacing the Flyback driver may be in order. A boundary conduction mode driver is very useful for a static DC-DC design, however, to be more flexible a CCM and DCM driver should be considered. If PWM switching is chosen to modulate the output to a sinusoid, then the primary and secondary side switches need to be in sync. Whether energy is still stored in the core or the current through the secondary winding has reached zero, the primary side should be able to adjust to the energy needs and demanded by the output.

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Appendices

- A. EAGLE Library – Custom Created Components
- B. Final Component List
- C. SPICE Netlist

APPENDIX A

EAGLE Library – Custom Created Components

Snubber Diode

Figure A-35: Snubber Diode, Schematic (left) and Package

Input Capacitor (Electrolytic, 10uF)

Figure A-2: Input Capacitor, Schematic (left) and Package

Output Capacitor (Film, 1uF)

Figure A-3: Output Capacitor, Schematic (left) and Package

Inductor (1mH)

Figure A-4: Inductor at Output, Schematic (left) and Package

N-Channel MOSFET (TO-220AB Package)

Figure A-5: N-Channel MOSFET, Schematic (left) and Package

P-Channel MOSFET (TO-220AB Package)

Figure A-6: P-Channel MOSFET, Schematic (left) and Package

PQ26/25 Transformer

Figure A-7: PQ26/25 Transformer, Schematic (left) and Package

Power Diode

Figure A-8: Power Diode, Schematic (left) and Package

LT1007

Figure A-9: LT1007, Schematic (left) and Package

LT3748

Figure A-10: LT3748, Schematic (left) and Package

LTC6991

Figure A-11: LTC6991, Schematic (left) and Package

APPENDIX B

Final Component List

Table B-1: List of Components

Ref.	Mfg.	Type	Description
C1	Vishay	SMD, 0805	Capacitor, 4.7nF
C2	Vishay	Electrolytic	Capacitor, 4.7μF, 10V
C3	Vishay	SMD, 0805	Capacitor, 10nF
C4	KEMET	Film	Capacitor, 1μF, 100V
C5	Vishay	SMD, 0805	Capacitor, 1μF
C6	AVX	SMD, 1210	Capacitor, 2.2μF, 100V
C7	Vishay	SMD, 0805	Capacitor, 47pF
C8	Vishay	SMD, 0805	Capacitor, 10nF
C9/Cin	EPCOS	Electrolytic	Capacitor, 10μF
C10	TDK	SMD, 0805	Capacitor, 1μF
C11	AVX	SMD, 1210	Capacitor, 100nF
D1	Vishay	400V, 3A, 150ns	Power Diode
D2	Vishay	400V, 3A, 150ns	Power Diode
D3	ROHM Semi	200V, .8A, 25ns	Switching Diode
D4	OnSemi	91V, 3W	Zener Diode
Lout	Bourns Inc.	Toroidal	Inductor, 1mH, 1.3A
M3/PMOS	International Rectifier	IRF6218PbF	MOSFET
M4/NMOS	International Rectifier	IRFB4115PbF	MOSFET
Q1/NMOS	International Rectifier	IRFB4115PbF	MOSFET
R1	Xicon	SMD, 0805, 1%	Resistor, 56.2K
R2	Vishay	SMD, 1206, 1%	Resistor, 249K
R3	Xicon	SMD, 1210, 1%	Resistor, 6.04K
R4	Xicon	SMD, 0805, 1%	Resistor, 10K
R5	Xicon	SMD, 0805, 1%	Resistor, 412K
R6	Xicon	SMD, 0805, 1%	Resistor, 15.4K
R7	Susumu	SMD, 1206, 1%	Resistor, 33m
R8	Xicon	SMD, 0805, 1%	Resistor, 102K
R9	Xicon	SMD, 0805, 1%	Resistor, 976K
R10	Xicon	SMD, 0805, 1%	Resistor, 102K
R11	Xicon	SMD, 0805, 1%	Resistor, 1M
R12	Xicon	SMD, 0805, 1%	Resistor, 1M
R13	--	Power Resistor	Resistor, 67
R14	Panasonic	SMD, 1210, 1%	Resistor, 6.04k
T1	None (Custom)	52u-53u-53u	Transformer
U1	Linear Technology	LT3748	Integrated Circuit
U2	Linear Technology	LTC6991	Integrated Circuit
U3	Linear Technology	LT1007A	Integrated Circuit

APPENDIX C

SPICE Netlist

```
Final.asc
R1 N011 0 56.2K
V1 IN 0 40
C1 N015 N014 4700p
C2 0 N023 4.7μ V=10 Irms=0 Rser=0.003 Lser=0 mfg="TDK"
pn="C3216X5R1A475M" type="X5R"
R2 N005 N009 249K
R3 0 N012 6.04K
L1 N004 N005 52μ Rpar=5K
L2 N022 N019 53μ Rpar=5K
R4 N014 0 10K
C3 0 N020 .01μ
R5 IN N008 412K
R6 N008 0 15.4K
XU1 0 MP_01 MP_02 N016 IN N023 N008 MP_03 MP_04 N020 N021 N015 N009
N012 N011 LT3748
MSQ1 N005 N016 N021 N021 Si4488DY
R7 N021 0 33m
L3 N006 N001 53μ Rpar=5K
D1 N001 N002 MURS320
D2 N002 N022 30BQ060
C4 N002 0 1μ V=100 Irms=4.58 Rser=0.025 Lser=0 mfg="KEMET"
pn="C2225C105K1RAC" type="X7R"
L4 N002 Out 1m IpK=1.5 Rser=1.3 Rpar=45000 Cpar=220f mfg="Gowanda"
pn="894AT1004V"
M3 N006 Driver 0 0 IRF9640
M4 N019 Driver 0 0 BSC22DN20NS3
R8 N007 N018 102K
R9 N018 0 976k
R10 N017 0 102k
V2 N007 0 4.5
XU2 N007 0 N017 N018 N007 N010 LTC6991
R11 N013 0 1meg
R12 N013 N007 1meg
XU3 N013 N010 V+ V- Driver LT1007
V3 V+ 0 9
V4 V- 0 -9
C6 IN 0 2.2μ V=100 Irms=115m Rser=0.68 Lser=0 mfg="Nichicon"
pn="UPR2A220MPH" type="Al electrolytic"
R13 Out 0 67
C5 N007 0 1μ
C7 N021 0 47p
C8 Out 0 10n
C9 IN 0 10μ
C10 IN 0 1μ
L5 IN N004 200n
```

```
C11 IN N003 100n
R14 IN N003 50k
D3 N005 N003 D
D4 IN N003 1N5375B
.model D D
.lib E:\Programs\LTSpice\lib\cmp\standard.dio
.model NMOS NMOS
.model PMOS PMOS
.lib E:\Programs\LTSpice\lib\cmp\standard.mos
K1 L1 L2 L3 1.
.tran 20m startup
.lib LT3748.sub
.lib LTC.lib
.lib LTC6991.sub
.backanno

.end
```