**RF Reliability Comparison between DC Stressed and
Non-DC-Stressed GaN-on-Si HEMTs in a 1GHz Class F
Power Amplifier**

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By

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Committee Membership

TITLE: RF Reliability Comparison between DC Stressed and
Non-DC-Stressed GaN-on-Si HEMTs in a 1GHz Class F Power
Amplifier

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ABSTRACT

RF Reliability Comparison between DC Stressed and Non-DC-Stressed GaN-on-Si HEMTs in a 1GHz Class F Power Amplifier

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Gallium Nitride (GaN) is a wide band gap semiconductor with an energy gap of 3.4eV. The large energy gap of this III-V semiconductor gives it the ability to withstand high electric fields, high operating temperatures, and allows for high power density. These properties of GaN maintain their advantage at high frequencies and are ideal for use in power amplifiers.

This thesis discusses the reliability of a GaN high electron mobility transistor (HEMT) used in a class F power amplifier configuration. GaN HEMTs have only been commercially available since 2006 and as a result their long term reliability is still under investigation. The mechanisms that cause device failures and reduced performance are not fully understood and current work continues to produce new theories as to why they occur and how they affect device performance. The mechanisms that cause changes in device performance have been heavily explored in DC studies. These are useful in understanding the mechanisms that may lead to a change in device performance. However, there is less literature investigating how these mechanisms affect the radio frequency (RF) performance of devices.

Using the information gathered from literature about DC studies this thesis launches an investigation to observe the RF behavior of GaN HEMT amplifiers that have been subjected to DC stressing. The DC stressing consists of applying a large negative voltage to the gate terminal while connecting the drain and source terminals to ground. The applied voltage is large enough to cause permanent damage to the device. To perform the investigation four GaN class F power amplifiers are subjected to DC stressing while another four GaN class F power amplifiers receive no DC stressing. The performance of the two groups of amplifiers is compared and evaluated.

The eight power amplifiers are constructed to output 4 watts of power. The output power and DC bias are continuously monitored for each test. After a DC stress test, consisting of -70V applied between the gate and drain/source terminals, four observations are noted. One, the drain current, and two, the output powers are initially reduced and recover after roughly a 3 hour period of time. Three, when operated for periods of time greatly exceeding the recovery period there are no differences seen in behavior between stressed and non-stressed amplifiers. These three observations happened in all the test runs. Four, a permanent gate leakage current is observed in all stressed amplifiers.

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Chapter 1 Introduction

Gallium Nitride (GaN) is a wide band gap semiconductor with an energy gap of 3.4eV. The large energy gap of this III-V semiconductor gives it the ability to withstand high electric fields, high operating temperatures, and allows for high power density. These properties of GaN maintain their advantage even at high frequencies. The high field, temperature, and power density capabilities of GaN are useful in power amplifier applications [1].

This thesis first discusses the power amplifier application through the use of a GaN high electron mobility transistor (HEMT) and describes in detail its operation. HEMT topology transistors are able to perform better at higher frequencies than ordinary transistors due to increased electron velocity. The applications of HEMT devices include use in RADAR, base station transmitters, and high performance space electronics [1].

The next topic discussed is the reliability of GaN in a HEMT device. GaN HEMT devices have only been commercially available since 2006 and as a result their long term reliability is still under investigation [2]. The mechanisms that cause device failures and reduced performance are not fully understood. Current work continues to understand the mechanisms and produce theories as to why they occur. Three major theories are discussed and an attempt to link the observed device behavior to these theories is made. These theories include hot electrons, Inverse piezoelectric effect, and process dependent defects.

The mechanisms that cause changes in device performance have been heavily explored in DC studies that stress devices with high electric fields and/or large drain currents. The DC studies are useful in understanding the mechanisms that may lead to a change in device performance. However, there is less literature that investigates how

these mechanisms affect the radio frequency (RF) performance of devices. This thesis utilizes the information gathered from DC studies and launches an investigation into the RF performance of GaN HEMTs that have been subjected to stressing in the form of high DC electric fields. These DC electric fields are created by applying a large negative voltage, -70V, to the gate terminal while both the drain and source terminals are connected to ground.

Chapter 2 GaN Background

2.1 GaN Applications

Gallium Nitride is a wide band gap III-V semiconductor that is attractive for use in power electronics, laser diode (LD), and LED applications [1]. These applications take advantage of GaN by using it in place of conventional semiconductor materials such as gallium arsenide (GaAs). One example is the use of GaN in high electron mobility transistors or HEMTs. GaN HEMTs have found use in wireless infrastructures and high power electronics due their high efficiency, high frequency operation and high operating voltages [1].

2.2 GaN Properties

2.2.1 Band Gap

Band gap is a material property that defines the energy required for an electron in the valence band to move into the conduction band and represents the difference in energy between the two. Between these two bands is an area known as the forbidden zone, where electrons cannot exist. GaN falls into the wide band gap (WBG) category of semiconductors with an energy gap of 3.4eV [3]. Table 2.1 shows a comparison of material characteristics for GaN, silicon (Si), and GaAs.

Property	Si	GaAs	GaN
Bandgap (eV)	1.12	1.43	3.45
Dielectric Constant	11.9	13.1	9
Electric breakdown field (KV/cm)	300	400	2000
Electron Mobility ($\text{cm}^2/\text{V}\cdot\text{s}$)	1500	8500	1250
Hole Mobility ($\text{cm}^2/\text{V}\cdot\text{s}$)	600	400	850
Thermal Conductivity ($\text{W}/\text{cm}\cdot\text{K}$)	1.5	0.46	1.3
Saturated Electron Drift Velocity ($\times 10^7 \text{ cm/s}$)	1	1	2.2

Table 2.1: Material Characteristics of Si, GaAs, and GaN [3].

2.2.2 Temperature Characteristics

WBG semiconductors have the ability to maintain their electrical characteristics at high ambient temperatures as a result of large energy gaps. The thermal energy of an electron increases with increasing ambient temperature. There exists a critical temperature above which electrons have enough energy to move from the valence band to the conduction band resulting in uncontrolled conduction. For GaN the critical temperature is in excess of 700 C, whereas GaAs has a critical temperature of 300 C [1]. This ability allows for GaN devices to operate in harsher temperature conditions than conventional GaAs devices.

2.2.3 Electric Field Characteristics

WBG semiconductors have a large electric breakdown field, due to their large energy gaps. This high breakdown field is translated directly to higher electric breakdown fields in GaN devices. Due to the higher electric breakdown fields, high

doping levels within the material can be obtained and thinner device layers for the same breakdown voltage levels can be achieved. Therefore GaN power devices are thinner than conventional GaAs devices [3].

2.2.4 Frequency Characteristics

The ability of a semiconductor device to operate at high frequencies is directly proportional to the drift velocity of particles, electrons in this case, within the material. Drift velocity is defined as the product of electron mobility and electric field applied to the material. Therefore the higher the electron mobility of a material, the higher the maximum operating frequency it can achieve. WBG materials have higher electron mobility than regular band gap materials, resulting in better performance at higher frequencies [3].

2.3 GAN HEMTs

2.3.1 Basic HEMT

A high electron mobility transistor or HEMT is a field effect transistor that incorporates the use of a heterostructure. The classification of the transistor as a HEMT device is due to the utilization of the superior transport capabilities provided to electrons that reside in a potential well [5]. Figure 2.1 represents a simplified structure for a GaN HEMT device.

Figure 2.1: Basic GaN HEMT structure [1].

From Figure 2.1 it can be seen that a layer of aluminum gallium nitride (AlGaN) is placed on top of a layer of GaN creating the heterostructure. The AlGaN layer has a larger energy gap than the GaN layer causing a sharp dip in the conduction band at the interface [4]. The band diagram for the GaN HEMT device is shown in Figure 2.2.

Figure 2.2: Band diagram of GaN HEMT [21].

The sharp dip in the conduction band creates a large electron density in a narrow region known as a potential well. This potential well occurs in the horizontal drain to source direction of the device. The large concentration of electrons can be modeled as a two dimensional structure due to the small thickness of the potential well with respect to

the length and width of the channel. This concentration of electrons is referred to as the two dimensional electron gas (2DEG) and is quantified by sheet carrier density [5].

In a conventional HEMT the wider band gap material is comprised of a lightly doped substrate that provides donor electrons for the formation of the 2DEG. In contrast, a GaN HEMT does not require the wider band gap substrate to be doped. The 2DEG forms regardless of material doping and the sheet carrier density is not proportional to the amount of doping [5].

2.3.2 GaN HEMT

At the AlGaIn/GaN heterostructure of the GaN HEMT a large built in piezoelectric polarization exists that yields a 2DEG sheet carrier density in excess of 10^{13} cm^{-2} . The built in piezoelectric polarization alters the band structure in the AlGaIn layer and electron distribution of the AlGaIn/GaN heterostructure. This alteration causes a large number of electrons to transfer from surface states to the 2DEG, creating the high density sheet charge. The built in piezoelectric polarization also causes the crystalline structure of the AlGaIn to be distorted creating large amounts of tensile strain in the material [5].

The properties of the AlGaIn heterostructure make the GaN HEMT ideal for use in high frequency, high power applications. The heterostructure, with its high sheet carrier density and high electron mobility, produces a large max drain current at high operating frequencies. Figure 2.3 illustrates the relationship between the properties of GaN and the device properties of a GaN HEMT.

Figure 2.3: Properties of GaN and device properties of GaN HEMTs [4].

In order to rate the performance of devices made of different materials there are two important figures of merit. The first is Johnson's figure of merit, which describes a device's ability to operate at both a high power and high frequency. This is determined by the product of electric field breakdown and electron saturation velocity (maximum drift velocity) [6]. The second is Baliga's figure of merit, which describes the resistive losses of a device [7]. Table 2.2 shows a comparison of GaN with conventional semiconductor materials. The figures of merit are presented as a ratio with devices that are made with silicon (Si).

Material	$\frac{JFOM}{JFOM(Si)}$	$\frac{BFOM}{BFOM(Si)}$
Si	1	1
GaAs	1.8	14.8
GaN	215.1	186.7

Table 2.2: Comparison of Johnson and Baliga figures of merit for semiconductor materials [4].

2.4 Nitronex NPTB00004 GaN HEMT

This thesis will utilize the Nitronex NPTB00004 Gallium Nitride 28V, 5W RF Power Transistor. Nitronex's first generation GaN HEMT platform was qualified and released for commercial production in October 2006 [2]. Since this release date Nitronex has developed a family of GaN devices with power capabilities reaching two hundred watts and operating frequencies up to 6GHz.

Nitronex uses a Si substrate for their devices due to its low crystal defect density and wafer-wafer consistency that has been achieved through decades of manufacturing optimization. Si substrates also offer the high quality surface needed to perform Nitronex's epitaxy process known as SIGANTIC for the growth of crack free GaN [2].

In the growth process a thin initial layer of aluminum nitride (AlN) is deposited on the Si substrate to accommodate the strain produced from the differences in crystal properties of Si and GaN, referred to as the transition layer [2]. Figure 2.4 is a schematic of the Nitronex epitaxially grown GaN HEMT material structure.

GaN Cap	Cap Layer (15 Å)
AlGaN Barrier	Barrier of Composition - x (26% Al) and Thickness - d (180 Å)
GaN Channel & Buffer	2DEG $n_s = 8.5 \times 10^{12} / \text{cm}^2 \pm 2.9\%$ $\mu_n = 1,500 \text{ cm}^2 / \text{V-s} \pm 2.5\%$ Semi-insulating GaN Buffer Layer (0.8 μm)
Transition layer	Stress Mitigating Transition Layer
Silicon	High Resistivity Silicon Substrate (10,000 $\Omega\text{-cm}$)

Figure 2.4: Nitronex GaN HEMT material structure [2].

Figure 2.5 is a cross section photograph of a fully fabricated Nitronex GaN HEMT on Si device. It can be seen that Nitronex uses a source connected field plate in construction. This helps to alter the distribution of the electric field within the AlGaN layer, reducing the peak value. This reduction in peak electric field causes an increase in the breakdown voltage of the device and means a more negative voltage can be applied to the gate terminal before any damage occurs within the device [27].

Figure 2.5: Photograph of fully fabricated Nitronex GaN HEMT [2].

The NPTB00004 consists of a single 2mm die attached to a thin copper flange with a silver epoxy. The gate and drain terminals are connected by bond wire to the terminals of the PSOP package. The package is sealed with an overmolded plastic coating that encases the die and bond wires [8]. Figure 2.6 is a picture of the final surface mount device.

Figure 2.6: Nitronex NPTB00004 surface mount GaN HEMT.

Chapter 3 GaN HEMT Class F Power Amplifier

In order to investigate the RF performance of the Nitronex GaN HEMT it is implemented in a class F power amplifier. The class F topology allows for the design of an efficient power amplifier and represents a commercial application. In this thesis the amplifier needs to adhere to non-exacting design requirements that are chosen to be of quality but attainable in one or two iterations as this is only the first step in the experiment design process.

3.1 Class F Operation

A class F amplifier is a switching class amplifier and relies on a harmonic tuning network configuration to be connected to the device. The switching class is referred to as such because the behavior of the voltage and current at the output of the device resembles that of a switch. When the switch is open the voltage is at its maximum with no current, when closed the current is at its maximum with no voltage. The DC bias of a class F amplifier is not restricted to a specific point and can be adjusted for a desired performance goal. A higher bias point allows for more output power from the device while a lower bias point allows for a higher efficiency from the device. Due to the switching behavior harmonics are generated at the output of the HEMT device. These harmonics are desired and controlled to improve amplifier efficiency [22].

Class F amplifiers, theoretically, can achieve an efficiency of 100% with the device consuming no power and providing zero harmonic content to the load. This can only be achieved if a harmonic tuning network is designed with the ability to control an infinite number of harmonics, making it impossible to physically realize [9]. The control of an infinite number of harmonics allows for the voltage and current waveforms at the

drain of the device to have zero overlapping area, resulting in no power being consumed by the device. The ideal operation of a class F amplifier has a perfect square wave for the drain voltage and a half rectified sine wave for the drain current with the two being 180° out of phase [10]. Figure 3.1 shows the ideal drain voltage (blue) and current (green) waveforms of a class F amplifier.

Figure 3.1: Ideal drain voltage (blue) and drain current (green) for a class F amplifier.

A periodic function can be represented by the summation of an infinite number of sinusoidal functions, referred to as a Fourier series. Therefore the waveforms seen in Figure XX can be described using Equation 1.

$$\text{Waveform}(t) = A_0 + A_1 \cos(\omega_0 t + \theta_1) + A_2 \cos(2\omega_0 t + \theta_2) + A_3 \cos(3\omega_0 t + \theta_3) + \dots \quad (1)$$

In order to obtain the square wave needed for 100% efficiency the Fourier series for the drain voltage must contain only odd harmonics, resulting in Equation 2 where k represents the harmonic order [13].

$$\text{Square}(t) = \frac{4}{\pi} \sum_{k=1}^{\infty} \frac{\sin(2\pi(2k-1)\omega_0 t)}{2k-1} \quad (2)$$

In order to obtain the half rectified sine wave needed for 100% efficiency the Fourier series for the drain current must contain only even harmonics, resulting in Equation 3 where k represents the harmonic order [13].

$$\text{HRS}(t) = \frac{1}{\pi} + \frac{1}{2} \cdot \sin(t) - \frac{2}{\pi} \sum_{k=2,4,6}^{\infty} \left(\frac{\cos(kt)}{k^2 - 1} \right) \quad (3)$$

The control of less than an infinite number of harmonics reduces the overall efficiency of the class F operation. This is due to the deviation in the voltage and current waveforms from the ideal case, allowing for overlap and therefore device power consumption. The maximum achievable efficiencies for incrementally increased control of the output harmonics from the first through the fifth are shown in Table 3.1.

Output Harmonic Control	Maximum Efficiency (%)	Increase in %
1	50	n/a
2	70.7	20.7
3	81.65	10.95
4	86.56	4.91
5	90.45	3.89

Table 3.1: Maximum achievable efficiency and increase in efficiency for incrementally increased output harmonic control [12].

As the number of controlled harmonics increases the improvement in efficiency becomes smaller, yielding diminishing returns. This is partially due to the parasitic drain source capacitance, C_{ds} , built into the device. The higher frequency harmonics leak through C_{ds} and therefore contribute less to amplifier performance when controlled [12]. A balance between the complexity of the harmonic tuning network and the desired

efficiency must be achieved. It is common practice in class F design to control only up to the third harmonic.

3.2 Design and Simulation

The first steps in designing the amplifier are to pick an operating frequency and a DC bias point. Next load/source pull measurements are used to determine the input/output impedances that need to be presented to the device to obtain maximum power transfer. The frequency is chosen to be 1 GHz due to the availability of RF signal generators and the quiescent current is chosen to be fifty milliamps with a drain voltage of 28 V. The Nitronex NPTB00004 data sheet provides the input and output impedances required at the quiescent drain voltage and current over the operating frequency range of the device shown in Table 3.2 and on a Smith Chart in Figure 3.2. The input impedance is represented by Z_S and the output impedance is represented by Z_L .

Frequency	$Z_S (\Omega)$	$Z_L (\Omega)$	$I_{DQ} (mA)$	Optimized Tuning Condition
900	$9.2 + j23.8$	$52.6 + j22.8$	50	CW Power and Efficiency
1800	$5.2 + j0.5$	$24.5 + j18.3$	50	CW Power and Efficiency
2140	$5.0 - j2.6$	$17.1 + j15.0$	50	CW Power and Efficiency
2500	$5.4 - j10.5$	$14.7 + j10.0$	50	CW Power and Efficiency
3500	$5.0 - j21.0$	$11.2 + j4.7$	50	CW Power and Efficiency

Table 3.2: Input and output impedances for maximum power transfer for Nitronex NPTB00004 [23].

Figure 3.2: Smith chart representation of input and output impedances for maximum power transfer for Nitronex NPTB00004 [23].

The input port of the device is presented the proper impedance through the use of an input matching network. The network must transform fifty ohms an input impedance of $6.5+j7\Omega$ for maximum power transfer. A series-shunt topology network is used and is referred to as such because the first element in the matching network is a series transmission line connected to the device input with the second element being an open circuited stub. Figure 3.3 shows the topology of the series-shunt network.

Figure 3.3: Series-Shunt matching network topology.

In order to minimize the size of the matching network both microstrip line lengths are kept less than a half wavelength at the fundamental frequency. A transmission line that is a half wavelength provides a 360° phase shift meaning it has no effect on impedance. Therefore any line exceeding this length can be reduced by a half wavelength and produce the same result, demonstrated in Figure 3.4 where Z_1 and Z_2 are the same in both cases.

Figure 3.4: Demonstration that a $\frac{1}{2}$ wavelength increase in line length does not affect the operation of the tuning section for impedance transformation.

The design process uses a smith chart to determine the required lengths for the transmission lines in the matching network. Figure 3.5 below is the smith chart used for

the input matching network and Figure 3.6 is the corresponding network response. The process begins by normalizing the desired device input impedance based on a 50Ω system, point A. The series transmission line moves the impedance along a constant radius VSWR circle to point B where the real impedance is a normalized 1Ω , translating to a de-normalized impedance of 50Ω . The remaining normalized imaginary impedance is eliminated by the open circuited stub line which has an equal and opposite value causing a cancellation and movement to point C [25]. The line lengths are determined by the distance moved between points on the smith chart and are in terms of wavelength. The result is a network that has 50Ω amplifier input impedance and a $6.5+j7\Omega$ impedance at the input of the device.

Figure 3.5: Smith chart used in the design process for the input matching network showing movement from point A (device input), to point C (amplifier input).

Figure 3.6: Network response of the input matching network with S_{11} in blue and S_{21} in red.

To control the harmonics this thesis will use a third harmonic peaking topology applied only to the output of the device. Studies show that controlling the harmonics at the input of the device helps improve efficiency, but this is beyond the scope of this thesis [13]. Third harmonic peaking refers to a Class F amplifier that only controls the third harmonic, reducing the complexity while maintaining desirable efficiency. As stated in chapter 3.1 it is necessary to remove all even harmonics for the voltage waveform and all odd harmonics for the current waveform at the drain terminal of the device. This is achieved by presenting an open circuit to the drain terminal of the device for the third harmonic while presenting a short circuit for the second harmonic.

Figure 3.7 below is a lumped element example demonstrating third order peaking topology. Tank 1 is a parallel resonant LC circuit with a resonant frequency at the third harmonic presenting an open circuit to the drain terminal of the device at $3f_0$ and a short circuit at all other frequencies. Tank 2 is another resonant circuit that resonates at the fundamental frequency, creating an open circuit, and allowing f_0 to reach the load. It

provides a short to ground for all other frequencies and provides the presentation of a short circuit to the drain terminal of the device for the second harmonic.

Figure 3.7: Lumped element schematic for 3rd order peaking output harmonic tuning network.

The lumped element harmonic tuning network is used to demonstrate the principles behind the operation of the harmonic tuning network but does not perform well at higher frequencies. It is difficult to realize capacitors and inductors that behave as such when operated at the RF frequencies utilized in this thesis and therefore a distributed network is used instead. For a distributed network the necessary impedances are provided through the use of open, short, and series microstrip transmission lines of varying lengths. Table 3.3 shows the relationships between electrical length and harmonic number used in the design of the tuning network.

Harmonic	Electrical Length		
1	$\lambda/8$	$\lambda/12$	$\lambda/4$
2	$\lambda/4$	$\lambda/6$	$\lambda/2$
3	$3\lambda/8$	$\lambda/4$	$3\lambda/4$

Table 3.3: Relationship between harmonic number and electrical length, used for quick reference in designing distributed networks.

Figure 3.8 below is a simplified schematic of the distributed harmonic tuning network. Transmission line 1 (T_1) is RF short circuited to ground through the capacitor at all harmonic frequencies. At the fundamental frequency, first harmonic, T_1 is a quarter wavelength and therefore provides a 180° phase shift transforming the short circuit to an open circuit at node A. At the second harmonic T_1 is a half wavelength and therefore remains a short circuit at node A. At the third harmonic T_1 is three quarters of a wavelength and therefore transforms the short circuit to an open circuit at node A. T_1 provides the necessary presentation of a second harmonic short circuit to the drain terminal of the device while not affecting harmonics one and three. T_3 is an open circuit stub that is a quarter wavelength at the third harmonic transforming node B to a short circuit. Nodes A and B are connected by T_2 which is a quarter wavelength at the third harmonic transforming node A to an open circuit. The combination of T_2 and T_3 provide the necessary presentation of a third harmonic open circuit to the drain terminal of the device.

Figure 3.8: Schematic of distributed 3rd order peaking output harmonic tuning network.

The performance of the tuning network is measured by simulating the S_{11} parameter at the drain terminal shown in Figure 3.9 below. On the smith chart the second harmonic, marker 1, is low impedance while the third harmonic, marker 2 is high impedance meeting the design requirements. The two harmonics are not perfectly open and short due to the parasitic effects that occur from the interaction of different microstrip sections. The 90° bend between the connections of $T_{1,3}$ with T_2 create additional tuning parameters that alter the network behavior. Also the characteristics of the lines will change with frequency, reducing their ability to behave as designed at the higher order harmonics.

Figure 3.9: Smith chart for S_{11} presented at the drain terminal from the output harmonic tuning network. The response shows low impedance for the second harmonic and high impedance for the third harmonic as expected.

The device output impedance at the fundamental frequency is transformed by the tuning network and therefore the load pull data in the Nitronex data sheet can no longer be used. The impedance at node B must be matched to 50Ω through the use of an additional output matching network. The output matching network must also present the

necessary impedance to node B for maximum power transfer to occur. This network can be designed by performing a load pull analysis with the harmonic tuning network in place at the device output and matching to the resultant impedance. A second design option is the use of the optimization feature in Agilent's Advanced Design System (ADS). This thesis uses the optimization method for obtaining the necessary network parameters.

Before the optimization tool is utilized the topology of the matching network must be laid out. A series-shunt stub topology is used to match the output of the tuning network to 50Ω . The same process used for the input matching network on pages 17-18 is applied here.

The final considerations in the amplifier design are the DC bias networks. These will provide DC voltage to both the gate and drain of the GaN HEMT device. The goal is to provide this DC voltage without interfering with the RF operation of the amplifier. The DC power supply cannot simply be attached to the input and output matching networks without being first RF isolated. This amplifier design incorporates the drain voltage supply into the harmonic tuning network through the use of the RF short circuited tuning stub, T_1 in Figure 3.8. The DC power supply simply needs a conduction path to the device and is not affected by the length of the tuning stub. The RF signal is affected by the length of the tuning stub and therefore this must be taken into account. Node A in Figure 3.8 is transformed to an open circuit by T_1 from the DC connection point at the fundamental frequency; therefore the RF signal is isolated from the DC supply.

The gate voltage supply uses an RF choke to isolate the RF signal from the DC supply. According to the Nitronex data sheet a 200Ω resistor should be placed in series before the RF choke to dampen any oscillation in the amplifier circuit. Two capacitors are placed in parallel across the terminals of the DC power supply in both the gate and

drain bias networks. These provide an RF path to ground for any non-DC signal that reaches the supply terminal preventing interaction with the DC power supplies. Multiple capacitors are used to prevent resonance with any parasitic inductance present in other parts of the circuit.

Figure 3.10 is an electrical schematic of both the DC bias networks incorporated with the input and output networks of the amplifier.

Figure 3.10: Schematic of DC bias networks for both gate and drain terminals.

The final design is shown in Figure 3.11 with the input, output, tuning, and DC bias networks all connected and attached to the Nitronex device. The input and output matching networks are further adjusted at this point using the optimization tool in ADS to improve amplifier performance. Capacitors C_2 and C_3 are added to the input and output of the amplifier circuit to provide AC coupling to connected components, thereby preventing any DC interaction.

Figure 3.11: Final ADS schematic of class F power amplifier with current probes and voltage markers in place to calculate amplifier figures of merit.

The simulation uses a technique referred to as harmonic balance that uses multiple input harmonics and a Fourier transform to determine the time domain response steady state response of the amplifier. The Nitronex application note states that the power input to the device should not exceed 20dBm and therefore the simulation is an input power sweep from 0dBm to 20dBm [14]. The results are shown in Table 3.4 and Figure 3.12.

Input Power (dBm)	Output Power (W)	DC Power (W)	Gain (dB)	Drain Efficiency (%)	PAE (%)
0	0.133	1.760	21.233	7.545	7.511
1	0.168	1.836	21.261	9.166	9.124
2	0.213	1.927	21.290	11.067	11.018
3	0.270	2.036	21.318	13.275	13.216
4	0.342	2.165	21.344	15.810	15.740
5	0.433	2.317	21.364	18.686	18.604
6	0.546	2.494	21.375	21.906	21.810
7	0.687	2.699	21.371	25.464	25.352
8	0.861	2.933	21.348	29.342	29.212
9	1.071	3.196	21.298	33.508	33.360
10	1.324	3.489	21.216	37.927	37.756
11	1.622	3.808	21.096	42.549	42.353
12	1.966	4.151	20.931	47.310	47.087
13	2.355	4.512	20.713	52.104	51.849
14	2.779	4.887	20.429	56.730	56.438
15	3.213	5.264	20.054	60.819	60.488
16	3.560	5.598	19.490	63.247	62.879
17	3.817	5.878	18.775	64.314	63.909
18	3.936	5.776	17.898	67.332	66.801
19	3.993	5.581	16.957	70.631	69.893
20	4.037	5.450	16.001	73.065	72.059

Table 3.4: ADS simulated performance of class F amplifier for the following figures of merit: output power, DC power, gain, drain efficiency, and power added efficiency (PAE).

Figure 3.12: ADS simulated performance of class F amplifier. The top graph shows output power, the middle graph shows gain and the bottom graph shows power added efficiency (PAE).

3.3 Construction

Once the simulation meets the required performance specifications the next step is to create a layout file for the printed circuit board (PCB) construction. The layout file,

pictured in Figure 3.13 is created in Cadsoft Eagle and has extra metal pads added for ground plane and DC connections. There are vias, green circles, placed throughout the ground plane pad to ensure a constant potential across the entire surface. Additional input and output lengths of microstrip lines are added after the AC coupling capacitors to allow for the placement of end launch SMA connectors. The pad for the GaN HEMT is inside the yellow circle and is specially designed for heat sinking purposes.

Figure 3.13: Cadsoft Eagle layout of class F amplifier for PCB fabrication. The extra metal pads are used for mounting lumped components and the metal ground plane is electrically connected to the back ground plane through copper plated vias. The input, harmonic tuning, and output networks are shown in their final implementation. The yellow circle highlights where the Nitronex device is mounted to the PCB.

In the Nitronex thermal applications note a study is performed demonstrating several methods for heat sinking. This design utilizes a via farm directly under the source pad of the NPTB0004 device to conduct heat through the substrate and into the heat sink bolted to the bottom of the PCB [15]. The heat sink is a piece of aluminum that is attached by four bolts to the PCB board. Figure 3.14 shows a zoomed in picture of the pad for mounting the GaN HEMT.

Figure 3.14: Zoomed in picture of via farm mounting pad for Nitronex GaN HEMT. This zoomed in portion is taken from inside the yellow circle of figure 3.13.

The layout file is sent to a commercial PCB manufacturer and an unpopulated PCB board is the result. Next the amplifier construction is finalized through the placement of the lumped components and SMA end launch connectors onto the PCB. A picture of the completely constructed amplifier is shown in Figure 3.15.

Figure 3.15: Picture of fully constructed class F power amplifier with all lumped components and end launch connectors in place. Refer to figure 3.13 for detailed description of layout.

3.4 Performance

The constructed amplifier is characterized by performing an input power sweep similar to the one used in simulation. The output power and DC power are also measured in order to calculate gain, and PAE. The Nitronex application note 11 states that the input power to the device should not exceed 20dBm and therefore to match the simulation the input power sweep goes from 0dBm to 20dBm.

The ADS simulation model requires that a quiescent current of 50mA is used and therefore the constructed amplifier must also use this value. A voltage of -2V is applied to the gate before any power is applied to the drain. Next 28V is applied to the drain and the gate voltage is increased until the proper quiescent current is achieved. At this point RF power is applied to the amplifier and a sweep is performed [16]. The results of the input power sweep are shown in Figure 3.16 below.

Figure 3.16: Comparison of simulated ADS (green) and measured (blue) amplifier performance data. The top graph shows power output, the middle shows gain, and the bottom shows power added efficiency (PAE).

The expected results from the simulation for an input power of 20dBm are a 72% PAE with a gain of 16dB and output power of 36dBm. The results of the experiment match closely with a 60.68% PAE, 16.7dB gain and an output power of 36.7dBm. The output power and PAE curves have similar shapes to those from ADS while the gain continuously drops with an increasing input power. The second and third harmonic output powers for the power amplifier are 36dB and 60dB less than the fundamental tone, respectively, indicating proper operation of the output tuning network. All higher order harmonics share these levels of attenuation further indicating proper operation of the output tuning network.

These results indicate a design that is functioning as designed and provide justification that the use of this class F power amplifier is suitable for the RF performance study that is this work.

Chapter 4 DC Studies of GaN HEMTs

The implementation of a device for commercialization requires that the device be reliable and stable under continuous operation. The first step taken in testing the reliability of a device is to power on the device and observe how it operates throughout its lifetime. This is accomplished and sped up through accelerated DC lifetime tests where the GaN HEMTs are provided with DC bias and subjected to stress under various conditions. There are four major stress conditions that include: higher power, on, off, and $V_{ds}=0$ states. These stress conditions can produce high electric fields between the gate and drain/source terminals, either symmetrical or asymmetrical, and different magnitudes of device drain current. The purpose of the tests are to better understand the behavior and determine the mechanisms behind device breakdown and failure.

4.1 On State DC Stress Test

The on state test produces electric fields between the gate-source and gate-drain terminals that are not equal in magnitude, asymmetric, as a result of different voltages applied to each terminal. The on state implies there is significant drain current present in the device. The test is accelerated by increasing the baseplate temperature causing the junction temperature within the device to increase. The test applies a 40V drain bias and a starting drain current of 250mA/mm to a device with a gate width of 400 μ m for 1000 hours with junction temperatures up to 320° C. Throughout the test at every hour the stress is removed from the device to allow for the gate and max drain currents to be measured. The device is said to have failed if the maximum drain current drops more than 10% from its original value [17].

The devices used in this test are Triquint GaN HEMTs that are epitaxially grown on silicon carbide (SiC). Standard III-V commercial production processing is used to

fabricate the devices that are being tested. This is important because it provides a realistic fabrication of the devices, rather than that of a small laboratory controlled process. To ensure that the devices are grown without any defects in the crystalline structure a transmission electron microscope (TEM) is used to view the heterostructure shown in Figure 4.1 below. The flat interfaces between layers confirm defect free devices [17].

Figure 4.1: Cross sectional TEM image of defect free GaN HEMT heterostructure used in the DC stress experiment [17].

Figure 4.2 shows the results of the test through a plot of both quiescent drain current and max drain current versus time with current values represented as percentage of starting value [17].

Figure 4.2: Evolution of drain current (I_{DQ}) during 40V drain bias and maximum drain current (I_{Dmax}) [17].

The degraded devices are observed through a TEM to reveal any physical damage associated with the electrical degradation. The result is that after stress the device always contains a pit/crack shaped defect on the gate edge nearest the drain in the top AlGaIn layer. Figure 4.3 displays the pit/crack defect and should be compared to Figure 4.1 for reference [17].

Figure 4.3: TEM images of defects formed in the drain side of the gate after DC stress test for devices a and b [17].

The physical defects formed in the devices at the drain side of the gate strongly correlate to drain current reduction and indicate mechanical stress. The degradation of devices fabricated through identical processes show significant sample to sample variation, even on the same wafer [17].

4.2 $V_{ds}=0$ DC Stress Test

The $V_{ds}=0$ test refers to the voltage difference between the drain and source terminals during the test. In this case they are shorted together and connected to ground causing the electric fields between the gate-source and gate-drain terminals to be equal or symmetric. This test does not simulate real world operation of the device but rather provides insight into how electric fields developed in the device affect DC characteristics. The biggest advantage for using this test is that it isolates the effects of drain current and electric field. While in the $V_{ds}=0$ state there is no drain current in the device, due to no potential difference between the drain and source terminals, meaning any phenomena that occurs are strictly caused by electric field effects.

This test uses prototype industrial devices from different wafers and runs fabricated by three different manufacturers. A large negative voltage is applied to the gate terminal while the drain and source are shorted together causing high vertical fields through the barrier layer but small fields within the channel. The test is performed at room temperature in the dark with device characteristics being measured throughout the test. The following characteristics are measured in 1-2 minute intervals throughout: threshold voltage (V_T), max drain current (I_{Dmax}), source resistance (R_s), drain resistance (R_D), and gate leakage current (I_{Goff}) while the I-V characteristics are measured at the beginning and end of each test. The gate voltage is stepped more and more negative

starting at -10V and continuing to -50V with a 1V step every minute. Figure 4.4 shows the results of this stepped stress test [18].

Figure 4.4: Change in device characteristics before and after DC step stress experiment in the $V_{ds}=0$ state. (A) output characteristics, (B) transfer characteristics, (C) gate leakage current characteristics, (D) sub-threshold characteristics [18].

The I-V curves for a typical GaN HEMT after the $V_{ds}=0$ test are shown in graph A of the figure and show a reduction in drain current post stress. Graph B shows the transfer characteristics of the device and indicate a positive shift in V_T . Graph C shows an increase in off-state drain current which is due to the increased gate leakage current shown in Graph D that occurs when the device is in reverse bias [18].

The stress voltage and gate current versus time are graphed in Figure 4.5 A while device parameters versus stress voltage are graphed in Figure 4.5 B. There appears to be a critical voltage at which sudden device degradation occurs, most

prominently seen in the stress gate current ($I_{Gstress}$) of graph A. The degradation of the device is symmetric at both the source and drain side of the gate terminal as expected and shown by the identical increase in both the source and drain resistance (R_s , R_d) [18].

Figure 4.5: (A) Stress voltage and stress gate current in $V_{ds}=0$ state. (B) Change in I_{dmax} , R_d , R_s , and I_{loff} in $V_{ds}=0$ state [18].

4.3 Off State DC Stress Test

The off state test refers to the device and implies that no drain current is flowing through the channel. In order to prevent drain current a large negative voltage is applied to the gate terminal, pinching off the channel. The voltage applied to the drain terminal is then increased in steps over time. This test does not simulate real world operation of the

device but rather provides insight into how electric fields developed in the device affect DC characteristics. The biggest advantage for using this test is that it isolates the effects of drain current and electric field. Any degradation seen in this test is attributed solely to electric field effects.

This test uses prototype industrial devices from different wafers and runs fabricated by three different manufacturers. To ensure the channel is completely pinched off, -5V is applied to the gate terminal while the source terminal is connected to ground. The drain voltage is stepped from 5V to 45V in 1V increments. Figure 4.6 shows the results of the stress test [18].

Figure 4.6: Change in I_{dmax} , R_d , R_s , and I_{goff} in an OFF-state, the two components of I_{goff} are plotted [18].

This test supports a critical voltage value between the gate and drain that causes a sudden change in device parameters. The observed critical voltage value is greater than that observed in the $V_{ds}=0$ case of section 4.2. From the figure it can be seen that the drain resistance (R_D) begins to increase beyond the critical voltage value while the

source resistance (R_s) does not. This result is consistent with the behavior of the gate current versus stress voltage. In the figure above the gate leakage current I_{Goff} is plotted along with its two components, gate to drain current (I_{GD}) and gate to source current (I_{GS}). I_{GD} increases beyond a critical voltage value while I_{GS} , found by the difference between I_{Goff} and I_{GD} causing it to be noisy, remains constant. This indicates degradation that occurs only on the drain side of the device with the source side remaining almost intact [18].

4.4 High Power DC Stress Test

The high power stress condition is very similar to the on state condition with the only difference being that the drain current of the device is increased for subsequent devices being stressed. The voltage applied to the gate terminal is increased with each subsequent run causing more current to flow in the channel of the device for the same drain voltage. The drain voltage is increased in 1V steps. With drain current being present in the device there is little electric field between the gate and other two terminals. This isolates the cause of any degradation effects to drain current and not electric field [18]. Figure 4.7 shows the results of the step stress experiment in the high power state.

Figure 4.7: Change in I_{Goff} in the high-power state for different values of drain current [18].

As the drain current for each stress test is increased the critical voltage value also increases meaning that a higher drain current actually mitigates the degradation due to large V_{GD} . This indicates the drain current by itself is not an accelerating factor for device degradation [18].

4.5 Mechanisms for Failure

The results found in performing the DC stress tests are used to theorize as to the mechanisms that cause device failures. With an understanding of how the devices fail or degrade it is possible to alter the fabrication process to create devices more resistant to these mechanisms. The results from the DC stress tests are analyzed by first determining if the results match with previously understood mechanisms for failure from older generation devices.

4.5.1 Hot Electrons

The first theory postulated for causing device failures is the presence of hot electrons. Hot electrons are referred to as such because in modeling them, their

effective temperature is set to a high value resulting in high amounts of kinetic energy. With these high amounts of kinetic energy the electrons have the ability to overcome potential barriers within the device and “leak” out of the channel reducing device performance through the reduction of sheet carrier density [19].

This phenomenon is readily understood and studied in GaAs HEMT devices creating a common model that defines device behavior with hot electrons. This model is not followed well by GaN HEMT devices, weakening the hypothesis that hot electrons are the cause of their degradation [20].

4.5.2 Inverse Piezoelectric Effect

The second theory proposed for device degradation is that of mechanical strain induced by inverse piezoelectric effects. GaN and AlGaN are strongly piezoelectric materials and large stresses are induced inside these materials in response to high voltages. During operation of the GaN HEMT devices large electric fields are formed under the gate edges across the GaN/AlGaN barrier resulting in a large amount of mechanical strain in a small section of the AlGaN barrier [18]. Figure 4.8 depicts this phenomenon.

Figure 4.8: Depiction of the mechanical strain in the AlGaN barrier as a result of high electric fields induced from high voltages being applied to the device.

The issue of mechanical strain is exacerbated by the fact that GaN and AlGaIn are severely lattice mismatched materials. Section 2.3.2 describes the polarization properties created by the heterojunction that result in the storage of large amounts of elastic energy in the form of tensile strain while at rest. When not at rest, with voltage applied, the elastic energy is increased in the high field regions on top of the already present energy [18].

When the elastic energy exceeds a critical value, defects are formed in the crystalline structure. These defects are electrically active and change the device characteristics significantly. The active defects are referred to as traps and when charged result in the reduction of sheet carrier concentration in the channel of the device due to large time constants that eliminate the electrons from participating in high frequency operation. The defects formed in the crystalline structure are permanent and therefore reduced performances of devices are permanent. This model is followed fairly well by GaN HEMT devices, supporting the hypothesis that electrically active defects are formed and are the cause of degradation [20].

4.5.3 Process Dependent Defects

Process Dependent defect is an umbrella term that incorporates anything causing improper or un-anticipated device operation before any sort of stimulus is applied. The growth of GaN on Si is difficult due to the lattice mismatch between the two materials. This mismatch can cause dislocations within the GaN buffer layer and these dislocations can propagate all the way through to the AlGaIn barrier layer. Dislocations are thought to be the major process dependent defects in the manufacturing of GaN HEMTs. These dislocations produce electron traps, reducing the performance of the device. The specific process dependent defects are more difficult to study and

understand because they cannot be isolated and studied individually [12]. The defects will appear as uncharacteristic device behavior during initial operation. Figure 4.9 displays the dislocations that can occur during the growth of lattice mismatched crystalline materials.

Figure 4.9: Illustration showing the presence of a dislocation formed from the growth of two lattice mismatched crystalline materials on top of one another. The dark blue circles represent a material with small lattice spacing while the light blue circles represent a material with large lattice spacing [28].

Chapter 5 RF Reliability Study of GaN HEMTs

An experiment test plan must be created before the reliability study can be conducted. This test plan details the experimental steps of the project and provides an outline of all necessary information and goals. The first step in the test plan process is to determine the goal of the project. Once the goal has been determined the next step is to design an experiment to achieve said goal. Step three is the design of the test set up and the final step is the analysis of the data generated and drawing conclusions.

5.1 Project Goals

Chapter 4 presents previous work that has been performed detailing the behavior of GaN HEMTs. This work has been focused in the area of DC stressing of devices and less work has been performed investigating how the device under test (DUT) performs in a high frequency application. The project goal is to implement class F GaN HEMT power amplifiers and investigate how DC stressing affects amplifier performance. The performance is evaluated by comparison of, a) non-stressed, and, b) DC stressed, amplifiers that are operated under the same conditions.

5.2 Experimental Test Set Up

The experiment that is used to explore the RF behavior of a DC stressed device relies on the integration of various items including lab equipment, software, and specifically constructed RF components. Eight class F power amplifiers are operated simultaneously and performance data is collected continuously for each. Figure 5.1 is a block diagram of the entire test set up that is implemented.

5.2.1 RF Signal Generation and Initial Amplification

An RF signal generator is used to create a 1 GHz continuous wave signal (CWS) that is input into each class F power amplifier. The CWS is amplified at the output of the signal generator; Figure 5.2 is a picture of the signal generator with subsequent amplifier used in the experiment set up.

Figure 5.2: Picture of RF signal generator with initial amplifier and DC power supplies.

5.2.2 Test Fixture

The following components are all designed, constructed, and purchased for this thesis: power splitter, preamp with voltage detector (VD), class F power amplifier, five watt 20dB attenuator, and output VD. The components are mounted to a large plate of aluminum and connected through the use of semi-rigid coaxial cable. The complete set

up is referred to as the test fixture and two are used in this thesis. The process of mounting all the test fixture components to a plate of aluminum creates a mechanically stable system. The mechanical stability prevents fatigue of both component and subcomponent connections during equipment manipulation.

5.2.2.1 Power Splitter

The initially amplified CWS is split into four different paths by a power splitter that is constructed on copper plated substrate. The construction uses a commercially purchased Mini-Circuits BP4C1+ 4 way-0° 50Ω Power Splitter/Combiner. Figure 5.3 displays the properties and shows an electrical schematic of the power splitter. Figure 5.4 is a picture of the power splitter on the test fixture.

Freq. (MHz)	Total Loss ¹ (dB)				Amp. Unbal. (dB)
	S-1	S-2	S-3	S-4	
750.00	6.79	6.98	6.96	6.98	0.19
800.00	6.63	6.79	6.77	6.79	0.16
820.00	6.60	6.74	6.72	6.75	0.15
840.00	6.57	6.71	6.69	6.72	0.14
860.00	6.57	6.69	6.67	6.70	0.14
900.00	6.57	6.68	6.65	6.69	0.12
920.00	6.59	6.68	6.65	6.70	0.11
940.00	6.61	6.69	6.66	6.71	0.10
960.00	6.63	6.70	6.68	6.72	0.09
980.00	6.66	6.72	6.69	6.74	0.08
1000.00	6.69	6.74	6.71	6.76	0.07
1050.00	6.78	6.80	6.76	6.83	0.06
1100.00	6.87	6.86	6.83	6.90	0.07
1150.00	6.97	6.93	6.89	6.97	0.08
1200.00	7.06	7.00	6.96	7.05	0.11

Figure 5.3: Table of electrical properties (top) and schematic (bottom) for mini-circuits BP4C1+ 4-way power splitter.

Figure 5.4: Picture of fully constructed power splitter mounted on test fixture.

5.2.2.2 Preamp with Voltage Detector

Each CWS output from the power splitter is amplified using a preamp constructed on copper plated substrate with a VD to measure the preamp output power. The preamp uses a commercially purchased Mini Circuits PHA-1+ 50Ω Monolithic Amplifier. Figure 5.5 shows the amplifier specifications important for the design in this experiment.

Parameter	Condition (GHz)	Vd=5.0V ⁽¹⁾		
		Min.	Typ.	Max.
Frequency Range		0.05		6
Gain	0.05	15.4	17.2	19.4
	0.8	14.1	15.7	17.3
	2.0		13.5	
	3.0		11.8	
	4.0	9.6	10.7	12.3
	6.0		9.7	
Input Return Loss	0.05		11.7	
	0.8	13.0	17.0	
	2.0		11.3	
	3.0		10.2	
	4.0		10.2	
	6.0		8.6	
Output Return Loss	0.05		14.5	
	0.8	13.0	20.8	
	2.0		17.1	
	3.0		15.3	
	4.0		13.8	
	6.0		11.0	
Reverse Isolation	2.0		19.9	
Output Power @1 dB compression	0.05	20.0	22.2	
	0.8	20.0	22.6	
	2.0	20.0	22.4	

Figure 5.5: Mini-Circuits PHA-1+ RF amplifier specifications used for the preamp design process.

The PHA-1+ is solely an amplifier and therefore the DC bias network is constructed externally to the package. Figure 5.6 represents the electrical schematic of the application circuit used to utilize the amplifier.

Figure 5.6: Application circuit for mini-circuits PHA-1+ amplifier.

In order to measure the output power of the preamp a VD circuit is constructed and placed in parallel to the RF out port. The VD uses a low capacitance shottky diode, capacitor, and resistor to rectify the CWS to a DC voltage. This DC voltage is proportional to the CWS power and is used to track changes in the preamp output power versus time. Figure 5.7 is the electrical schematic of the VD circuit.

Figure 5.7: Electrical schematic of voltage detector circuit used to track changes in power levels.

The concept of AC and DC coupling is an important factor when using a VD circuit. When two components are DC coupled there is a transfer of both DC and AC voltage between the two. Two components that are AC coupled only allow the transfer of AC voltages while blocking the transfer of DC voltages. AC coupling is achieved by placing a capacitor in series between two components. The RF out pin of the PHA-1+ is AC coupled to the RF out port of the preamp, seen in Figure 5.6, by the capacitor placed between the two. Subsequently the RF output port of the preamp is AC coupled to the input port of the class F amplifier, preventing any DC current to flow between the two. The VD circuit is connected between the two AC coupled components shown in Figure 5.8.

Figure 5.8: Voltage detector placement between two AC coupled components preventing a path for DC conduction.

In order to rectify the CWS to a DC voltage there needs to be a path for DC current to flow into the VD. This path is achieved by placing a resistor to ground at the RF out port of the preamp. The complete schematic and final implementation of the preamp with VD is seen in Figure 5.9.

Figure 5.9: Complete electrical schematic (top), and picture (bottom), of fully constructed preamp #5 with voltage detector.

5.2.2.3 Class F Power Amplifier

The design, construction, and characterization of the class F power amplifier are performed in Chapter 3 of this document. Each output CWS from the preamp components are used to drive the class F power amplifiers. The output of each power amplifier is terminated with a five watt, 20dB high power attenuator. The attenuators are commercially purchased Mini-Circuits Precision Fixed Attenuators.

5.2.2.4 Output Voltage Detector

The final component is another VD that measures changes in the output power generated by the class F power amplifier. The schematic is the same used in section 5.2.2.2 Figure 5.7. The RF out port of the class F amplifier is connected to the output VD through an attenuator, providing the necessary DC path for VD operation shown in Figure 5.10. Figures 5.11 and 5.12 show the constructed VD and the completely constructed test fixture, respectively.

Figure 5.10: Output voltage detector placement with attenuator creating path for the necessary DC current.

Figure 5.11: Fully constructed output voltage detector #4 with attenuator. Reference figure 5.7 for electrical schematic of the output voltage detector.

Figure 5.12: Fully constructed test fixture. Starting from the left and moving right: power splitter, pre amp and VD, DUT (class F amplifier), and output voltage detector all connected through semi-rigid coax.

5.2.3 Measurement Set Up

Each Class F power amplifier requires two separate DC voltage sources, drain and gate. Each VD output requires a DC voltmeter to record the rectified CWS. VD circuits measure changes in both the input and output power to each class F amplifier. Each preamp component needs a five volt DC power source. The five volt preamp sources are implemented by connecting the four DC bias networks on each test fixture to a single source. This results in the need of thirty four external connections to power and monitor the two test fixtures.

The five volt preamp sources and gate voltages do not need to be monitored and therefore simple DC power supplies are used. The sixteen VD and eight drain connections need to be remotely monitored. Sixteen Agilent U3606A Sourcemeters are used to accomplish this with each consisting of a voltage supply and multimeter. Having two instruments in the same casing gives the sourcemeter the ability to perform two separate functions simultaneously. The sourcemeters are connected and controlled remotely by a PC with LabVIEW through the use of a GPIB interface.

The LabView controlled instruments are used to record the power amplifier performance data as well as changes in the power level at which they are being driven. Data points are recorded at predefined increments of time.

5.2.4 Test Set Up Summary

In summary, there are eight class F power amplifiers operating simultaneously. The CWS power input into each is measured by a VD connected to a sourcemeter. The DC drain power of each is measured by a sourcemeter. The output power of each is measured by a VD connected to a sourcemeter. The preamp and gate voltages are

supplied by unmonitored DC power supplies. Figure 5.13 shows pictures of the complete experimental test set up.

(a) Side view picture of complete experimental test set up.

(b) Front view picture of complete experimental test set up.

(c) Back view picture of complete experimental test set up.

Figure 5.13: (a) Side, (b) front and (c) back view pictures of the entire experiment test set up.

5.3 Experimental Test set up characterization

In order to utilize the test set up properly, a full characterization must be performed on each test fixture. The characterization is a calibration procedure and allows for the identification of the operating point for each test fixture. The operating point is essential because each class F amplifier under test must be operated under the same conditions.

The first step is to ensure that each preamp has the ability to drive each power amplifier with the required 20dBm of power and also that this power level is reached by all the preamps at the same input power level for each test fixture. This is important as there is no way to adjust the power input into each individual preamp or power amp. The outputs of each power splitter are connected directly to the preamps and therefore will provide the same input power to each of the test fixture preamps. Figure 5.14 shows the output power response curve for each preamp grouped by test fixture. The preamps of

test fixture 2 show almost identical power responses while those of test fixture 1 have under a 2 dB difference in their responses.

Figure 5.14: Preamp output power vs. RF signal generator power response curves grouped by test fixture.

The second step involves the generation of calibration curves for the VDs that are built into the preamp components and those connected to the power amp outputs. These calibration curves are used to convert the output DC voltage to a relative CWS power level in dBm. The curves are generated by inputting a known power level into the component while and recording the corresponding DC voltage value. Table 5.1 displays the data for the generation of the output voltage detector calibration curves.

Input Power (dBm)	Voltage Reading (V)							
	1	2	3	4	5	6	7	8
-3	0.152	0.035	0.028	0.051	0.033	0.006	0.017	0.041
-2	0.189	0.050	0.041	0.071	0.047	0.010	0.026	0.058
-1	0.230	0.069	0.058	0.096	0.066	0.015	0.038	0.080
0	0.280	0.093	0.079	0.126	0.089	0.024	0.054	0.105
1	0.336	0.121	0.104	0.161	0.116	0.035	0.074	0.136
2	0.399	0.154	0.134	0.202	0.149	0.050	0.098	0.171
3	0.470	0.192	0.168	0.248	0.186	0.069	0.126	0.212
4	0.553	0.237	0.210	0.303	0.231	0.093	0.160	0.261
5	0.644	0.287	0.256	0.363	0.281	0.120	0.199	0.315
6	0.749	0.346	0.311	0.433	0.339	0.153	0.244	0.377
7	0.867	0.412	0.373	0.512	0.405	0.192	0.296	0.449
8	0.998	0.487	0.443	0.601	0.480	0.236	0.355	0.529
9	1.145	0.570	0.522	0.699	0.564	0.286	0.421	0.619
10	1.309	0.664	0.611	0.810	0.658	0.343	0.496	0.720
11	1.492	0.769	0.711	0.933	0.763	0.408	0.580	0.834
12	1.696	0.887	0.823	1.072	0.882	0.481	0.673	0.961
13	1.932	1.024	0.953	1.231	1.020	0.566	0.786	1.110
14	2.195	1.177	1.098	1.410	1.173	0.663	0.910	1.275
15	2.490	1.349	1.260	1.608	1.345	0.771	1.050	1.461
16	2.816	1.540	1.438	1.827	1.535	0.891	1.205	1.667
17	3.180	1.754	1.635	2.068	1.747	1.025	1.381	1.898

Table 5.1: Calibration data for the output voltage detectors. An input power sweep is performed and the corresponding DC voltage reading is measured.

A high order polynomial is used to create an equation to describe the curves from a sample of data points. The DC voltage readings are fed into their respective equations and the resultant is a relative power level in dBm. Figure 5.15 shows a plot of the fitted polynomial for output voltage detector 1 and Table 5.2 shows the sample data compared with the fitted curve interpolation. From the table it can be seen that as the input power level to the VD increases the curve becomes more accurate to the sampled data. Output VDs 1-8 are calibrated for an input power level of 17dBm. This is due to the fact that the max output power of any of the class F power amplifiers does not exceed 17dBm after the 20dB of attenuation.

Figure 5.15: Plot of fitted polynomial over measured data points for output voltage detector 1 sensitivity curve.

DC Voltage (V)	Actual Input Power (dBm)	Interpolated Input Power (dBm)	Difference (dB)
0.1520	-3.0	-2.9974	-0.0026
0.1890	-2.0	-1.9947	-0.0053
0.2300	-1.0	-1.0228	0.0228
0.2800	0.0	0.0089	-0.0089
0.3360	1.0	1.0134	-0.0134
0.3990	2.0	2.0028	-0.0028
0.4700	3.0	2.9863	0.0137
0.5530	4.0	4.0039	-0.0039
0.6440	5.0	4.9930	0.0070
0.7490	6.0	6.0039	-0.0039
0.8670	7.0	7.0081	-0.0081
0.9980	8.0	7.9979	0.0021
1.1450	9.0	8.9941	0.0059
1.3090	10.0	9.9989	0.0011
1.4920	11.0	11.0067	-0.0067
1.6960	12.0	11.9972	0.0028
1.9320	13.0	12.9988	0.0012
2.1950	14.0	14.0014	-0.0014
2.4900	15.0	14.9995	0.0005
2.8160	16.0	16.0001	-0.0001
3.1800	17.0	17.0000	0.0000

Table 5.2: Measured output voltage detector response compared to sensitivity curve interpolated response.

The purpose of the experiment requires the knowledge of any change in power over the course of operation. Therefore the VDs are used to measure relative power difference between each measured data point in time. The final result gives the ability to detect any changes in power level at both the input and output of the class F amplifier. This gives the ability to see if any change in power amplifier operation can be traced back to the input power or how it affects the output power.

The next step is to ensure that each class F amplifier constructed meets the performance criteria set forth by the original prototype. Chapter 3.4 describes the process used to characterize the prototype power amplifier and it is used once again to characterize each test fixture power amplifier. Figure 5.16 displays three important figures of merit for each power amplifier with the performance results of all eight plotted on each graph. From the data it is seen that each amplifier performs almost identically and matches the prototype as expected.

Figure 5.16: Output power (top), PAE (middle), and gain (bottom) response curves of all eight class F power amplifiers operated in the experiment. The tight grouping of the curves for each amplifier shows that each constructed amplifier operates almost identically.

The final step in the test fixture characterization process is determining the operating point for each test fixture to ensure that all of the power amplifiers under test operate at the same output power condition. This is done by using a SA to measure the output power of each class F amplifier with both test fixtures powered on. Table 5.3 shows the output power of each power amplifier with specified RF signal generator power. The power amplifiers all produce nearly the same output powers ensuring that each is operating similarly.

RF signal Gen. Power	Test Fixture 1 Output Power (dBm)				Test Fixture 2 Output Power (dBm)			
	PA 1	PA 2	PA 3	PA 4	PA 5	PA 6	PA 7	PA 8
-13 dBm	34.43	34.73	34.42	34.48	34.66	34.17	34.36	34.39

Table 5.3: Output power of each class F amplifier at -13dBm RF signal generator power. This is the operating point used in the experiment.

An important thing to note at this point is although the output power of each amplifier is the same, the input and DC powers may be slightly different for each. This is because each preamp driving the power amps was built by hand and therefore has slightly different characteristics at the output terminals. The VD circuit placed in parallel to the RF output port alters its impedance and therefore alters the impedance driving the power amplifiers as seen by preamp 1 in Figure 5.17.

Figure 5.17: Smith chart showing preamp 1 driving impedance for power amplifier 1. Marker 2 is the driving impedance seen by the power amplifier; note no longer a perfect 50Ω.

The driving source is no longer a perfect 50Ω, as used in the amplifier characterization process. The major effect is that the performance of each power amplifier is varied slightly, due to the inconsistency between each individual preamp, resulting in a change of DC power delivered to each. The maximum difference in DC power delivered is less than a quarter watt. The maximum output power for each class F power amplifier is also reduced.

5.4 Testing Procedure

To begin the experiment a baseline test of all 8 power amplifiers is performed over a one day period. After the baseline test four of the eight power amplifiers are selected at random, two from each test fixture, for DC stressing. These four power amplifiers are stressed in the $V_{ds}=0$ state described in chapter 4.2. The gate leakage current is measured during stressing and the transfer curves are measured both pre and

post stress. The stressed power amplifiers are then placed back on the test fixture with the non-stressed devices and operated for a period of time. During this time the input power, output power, and drain current of each power amplifier is monitored. Once the operating period is over, the four power amplifiers chosen for stressing are subjected to this process again. The experiment consists of repeating this process four times and observing the operation of all 8 power amplifiers while noting differences between stressed and non-stressed performance.

5.4.1 Baseline RF Performance

The first test performed provides baseline performance data for each amplifier. This test occurs before any of the GaN HEMT devices undergo DC stressing. The purpose is to perform device burn-in and provide a starting point for performance comparison. Although the Nitronex application note 007 describes the process used at the factory to perform device burn-in it is still important to note whether any further burn-in effects occur in the power amplifier set up [24]. Baseline performance data is compared to post stressing data and shows the affect DC stressing has on amplifier performance. This information also allows for the detection of any factory flaws in the devices. If a baseline test is not performed there is no guarantee that any change in performance is solely due to DC stressing.

The test begins by setting up the quiescent point for each individual amplifier described in section 3.4. Each amplifier must have a quiescent drain current of 50mA before RF power is applied and the test can begin. The test collects performance data every minute and is conducted over a span of 24 hours. A spectrum analyzer (SA) is used as a power meter and for visualizing the frequency content of each amplifier output. Figure 5.18 shows the SA data captured for power amplifier 1 initially during the

baseline test. Two 20dB attenuators are placed between the power amp output and the SA input and therefore all readings are reduced by 40dB. The -5.57dBm power reading at 1GHz means the power amplifier is outputting 34.43dBm. This matches the data from the test fixture 1 characterizations. All four amplifiers on the test fixture undergo this same process and ensure that the set-up is operating correctly. Figure 5.19 shows the SA data captured for power amplifier 5 initially during the baseline test and matches the data from test fixture 2 characterizations showing the set-up is operating correctly.

Figure 5.18: Power amplifier 1 output power spectrum during baseline test showing proper operation.

Figure 5.19: Power amplifier 5 output power spectrum during baseline test showing proper operation.

Figures 5.20 and 5.21 on pages 73-74 are plots of the data collected throughout the baseline test. The first observation to note is the spiking that occurs three times in every measurement at of the drain current at nearly the same point in time. This phenomenon occurs at the beginning of the test and is boxed in with two vertical black dotted lines to show when it occurs later in the test. These spikes are the result of using the SA to perform power measurements. The SA requires a manual connection to each output VD and therefore the measurement occurs over a large time span. For this reason a window of time is used to highlight when the spikes occur. Another important property about the manual nature of the SA connection is that it affects the output VD operation. The VD's used in this test fixture are described in section 5.2.2.2 and 5.2.2.5. An inherent property of these devices is their sensitivity to the environment and physical interaction. Each VD is extremely sensitive to any sort of movement and manipulation ranging from adjusting external connections to slight movement on the test fixture itself. This creates a problem when using the SA to collect data. After each connection and removal of the SA to the output VD the power readings and drain currents change. This

is the reason that before and after the spikes in each measurement the nominal value of the measurements change. In some cases the alteration in the measured value is large while in other cases it is negligible. This phenomenon means that the SA measurements are removed from all subsequent testing.

Test fixture 1, shown in Figure 5.20, displays stable amplifier performance outside of the SA measurement windows. The input powers are largely unchanged with most changes in power less than one tenth of a decibel. The output powers show less change than the input powers. Power amplifier drain currents are also stable outside the SA measurement windows.

Test fixture 2, shown in Figure 5.21, shows both stable and unstable operation. The input powers for amplifiers 6-8 change very little. The output powers are similar with only a few spikes in the change of power. Power amplifier drain currents are stable with little change outside the SA measurement windows.

The input power for amplifier 5 is constantly changing with spikes exceeding half a decibel, while the output power shows more stability with changes in power less than one tenth of a decibel. The drain current is not stable and is noisy with large changes occurring even outside the SA measurement windows. No cause is determined for this behavior and it is noted for future use of amplifier 5.

The data from both test fixtures indicates that a slight further burn-in from the factory process might have occurred in some devices, as the drain currents are slightly smaller at the end of the test than at the beginning.

Figure 5.20: Test fixture 1 baseline test plots. The top graph is the change in input power and is located at point D in the test set up block diagram of figure 5.1. The middle graph is the drain current and is located at point E in the test set up block diagram. The bottom graph is the change in output power and is located at point F in the test set up block diagram. The manual connections made by the SA measurements occur inside the dotted vertical lines and cause large changes in plotted values.

Figure 5.21: Test fixture 2 baseline test. The top graph is the change in input power and is located at point D in the test set up block diagram of figure 5.1. The middle graph is the drain current and is located at point E in the test set up block diagram. The bottom graph is the change in output power and is located at point F in the test set up block diagram. The manual connections made by the SA measurements occur inside the dotted vertical lines and cause large changes in plotted values.

5.4.2 DC Stressing of Class F Power Amplifiers

To achieve the goal of this thesis, explained in chapter 5.1, four power amplifiers must be subjected to DC stressing. Each of these four amplifiers is stressed in the $V_{ds}=0$ configuration described in chapter 4.2 with -70V applied to the gate and zero ramp up time. The first device stressed is used to create a baseline for stressing the remaining three devices. This method is used for each of the four subsequent DC stress tests performed on the set of devices. During the stress test of the first device the gate leakage current is measured and used as the indicator for level of stress that needs to be applied to each device. Therefore each subsequently stressed device is operated in the stress condition until the gate leakage current matches that of the first device. The gate leakage current is measured using a multimeter that is interfaced with LabView on a PC next to the set up. In order to provide a relative indication of how each device has degraded from DC stressing, the transfer curve for each will be measured both before and immediately after stressing has occurred. To generate the transfer curve, the gate voltage is swept while maintaining a constant drain voltage, and the drain current is plotted versus the gate voltage.

This measurement is performed using the HP4155 Parameter Analyzer. The transfer curve provides an indication of any shift in threshold voltage for the device. With the required 28V for the drain bias the parameter analyzer can supply a maximum drain current of 50mA. The greater the shift in threshold voltage, the more the device has been degraded. Figure 5.22 is a picture of the DC stress test set up. For the experiment, devices 1, 2, 6, and 8 are subjected to DC stressing.

Figure 5.22: Picture of the DC stress test set up.

Stress test 1: The first device is stressed reaching a gate leakage current of 1.8mA providing the baseline for the remaining devices.

Stress test 2: The first device is stressed to a gate leakage current of 4.2mA.

Stress test 3: The first device is stressed to a gate leakage current of 5.8mA.

Stress test 4: The first device is stressed to a gate leakage current of 7mA.

Stress test 5: Only performed on power amplifier 6, with a gate leakage current of 20mA.

The following Figures, 5.23-5.26, display the gate leakage current versus time and transfer curves for each stressed device. All the stress test data for each device are displayed on a set of two graphs.

Figure 5.23: Device 1 DC stress data showing (a) gate leakage current and (b) transfer curves.

Figure 5.24: Device 2 DC stress data showing (a) gate leakage current and (b) transfer curves. Type 1 Category

Figure 5.25: Device 6 DC stress data showing (a) gate leakage current and (b) transfer curves

Figure 5.26: Device 8 DC stress data showing (a) gate leakage current and (b) transfer curves.

In devices 1, 2, and 8 it can be seen that the gate leakage current has a spike at the beginning of each stress test, following the initial stress test. This transient then dies out and the gate leakage current drops to roughly the last value achieved in the previous stress test before beginning to rise over time. Device 6 does not share the spike at the beginning of the test but the gate leakage current does begin at roughly the value achieved in the previous stress test.

The gate leakage current rises at a different rate for each device with the following values: Device 1: 1.61mA/hour, Device 2: 2.94mA/hour, Device 6: 134mA/hour, Device 8: 1.37mA/hour. Devices 1, 2, and 8 have gate leakage rise time rates on the same order while device 6 is 100 times larger.

After stress test 3 it was decided to stress the devices to their maximum gate leakage current before complete device failure occurs. This value was determined from previous work performed on Nitronex Gan HEMTs [26]. The initial value chosen was 10mA for each device. For stress test 4, device 2 was chosen to be stressed first. The gate leakage current reached 8mA when a complete device failure occurred. Due to this fact, devices 1 and 6 were only stressed to 7mA. Other previous work had found that for a device with a fast gate leakage current rise time, like that of device 6, the maximum value before device failure is much higher. Therefore device 6 was stressed to a gate leakage current of 20mA during a fifth DC stress test.

The threshold voltage shifts more positive with each subsequent device stressing supporting the idea that gate leakage current is a good measure for level of stress applied to a device. The pre-stress transfer curves, represented by solid lines, show recovery after each stressing then amplifier operation. This recovery is in the form of a threshold voltage shift back in the negative direction. The recovery is not perfect as can

be seen by the differences in the groups of pre-stress transfer curves for each device. The transfer curves for the devices that have been stressed and then recovered have a smaller slope than the initial unstressed transfer curves. This same behavior is seen in the post-stress transfer curves but it is less pronounced. Device 6 has the smallest variance in the pre and post stress groups of transfer curves with much tighter grouping than the three other devices.

These results bring about the conclusion that there are two types of devices present in this experiment. Type 1 has gate leakage current with a slow rise time and small maximum value before device failure. Type 2 has a gate leakage current with a fast rise time and large maximum value before device failure. In conjunction to this thesis, work was performed that also shows the presence of two types of devices with over forty devices tested.

5.4.3 RF Performance of DC Stressed Devices

5.4.3.1 Post Stress Test 1

Figures 5.27 and 5.28 display the performance results of all eight amplifiers versus time after DC stress test 1 has been performed. The first stress test produces a gate leakage current of 1.8mA. The amplifiers are then operated in the high power amplifier state for a period of 7 days.

Test fixture 1 PA input powers show no significant changes with the maximum power level being less than a quarter of a decibel throughout the test. The power amplifiers on test fixture 1 also show small changes in output power versus time with the exception of amplifier 1. The VD at the output of amplifier 1 shows a very noisy output power reading at various points throughout the test with large spikes. These spikes do

not appear to be related to or affect the other two amplifier measurements. Test fixture 2 shows small changes in input powers and output powers for all amplifiers versus time with the exception of a few points.

The stressed amplifier drain currents are initially diminished with a recovery period. For power amplifiers 1, 2, 8 the diminished drain currents and recovery periods are greater than those of power amplifier 6. The recovery period is observed to be on the order of 3 hours after device turn on. After the recovery period the drain currents stabilize and remain stable throughout the remainder of the test. The non-stressed amplifiers also have a slightly diminished initial drain current but it is much less than the stressed amplifiers and fully recovers within tens of minutes after being turned on. When the time exceeds the recovery period for the stressed amplifiers it is impossible to differentiate between stressed and non-stressed amplifier performance.

The drain current of amplifier 8 demonstrates behavior that is not consistent with that of the other amplifiers on test fixture 2. There are sustained changes on the order of 5mA at multiple points in time with recovery to previous values. This behavior appears to have minimal effect on the output power of the amplifier.

Figure 5.27: Test fixture 1, stress 1 data. The top graph is the change in input power and is located at point D in the test set up block diagram of figure 5.1. The middle graph is the drain current and is located at point E in the test set up block diagram. The bottom graph is the change in output power and is located at point F in the test set up block diagram. Noisy output power readings are seen for PA1

Figure 5.28: Test fixture 2, stress 1 data. The top graph is the change in input power and is located at point D in the test set up block diagram of figure 5.1. The middle graph is the drain current and is located at point E in the test set up block diagram. The bottom graph is the change in output power and is located at point F in the test set up block diagram. The drain current for PA8 does not share the smooth behavior of the other PAs on the test fixture.

5.4.3.2 Post Stress Test 2

Figures 5.29 and 5.30 display the performance results of all eight amplifiers versus time after DC stress test 2 has been performed. The second stress test results in an increase in gate leakage current to 4.2mA. The power amplifiers are then operated for a period of 4 days.

For both test fixtures 1 and 2 the input PA powers show very little change with the exception of input 3, which has slightly larger variations. The output powers for each amplifier are extremely constant with changes rarely exceeding five one hundredths of a decibel on both test fixtures. Early and late in the test, input 3 has multiple power level changes that exceed those of the other inputs on test fixture 1.

The diminished drain currents are once again observed in the stressed amplifiers along with the recovery period on the order of 3 hours. Again amplifiers 1, 2, 8 have a more diminished initial drain current than amplifier 6 and therefore a larger recovery period. In this test the non-stressed amplifiers on test fixture 1 show very small initially diminished drain currents and almost no initially diminished drain currents on test fixture 2. The stressed drain currents also stabilize after the recovery period and present no differences in operation when compared to the non-stressed amplifiers.

The drain current of amplifier 3, a non-stressed device, has erratic behavior with large sustained changes in drain current on the order of 10mA. These large changes happen near the times when the input power also has its largest changes. The output power does not seem to be affected by these changes in drain current.

Figure 5.29: Test fixture 1, stress 2 data. The top graph is the change in input power and is located at point D in the test set up block diagram of figure 5.1. The middle graph is the drain current and is located at point E in the test set up block diagram. The bottom graph is the change in output power and is located at point F in the test set up block diagram. PA 3 has very erratic drain current that has changes on the order of 10mA.

Figure 5.30: Test fixture 2, stress 2 data. The top graph is the change in input power and is located at point D in the test set up block diagram of figure 5.1. The middle graph is the drain current and is located at point E in the test set up block diagram. The bottom graph is the change in output power and is located at point F in the test set up block diagram. After a recovery period for the drain currents no abnormal behavior is observed.

5.4.3.3 Post Stress Test 3

Figures 5.31 and 5.32 display the performance results of all eight amplifiers versus time after DC stress test 3 has been performed. The third stress test results in a gate leakage current of 5.8mA. The power amplifiers are then operated for a period of 3 days. While setting up the test fixtures to run the experiment a connection for the gate voltage of amplifier 8 came loose resulting in the complete destruction of the GaN HEMT making the amplifier non-operational. Therefore no operating data exists beyond this point for amplifier 8.

For test fixture 1 the PA input powers are extremely stable while for test fixture 2 they are slightly less stable. Near the beginning and end of the test all three remaining PA input powers on test fixture 2 show variance, but they share almost all points in time when these variances occur. The output powers for each amplifier changes very little for both test fixtures. Test fixture 2 shows a very slightly less stable output power but almost all changes in power are less than one tenth of a decibel.

Amplifiers 1, 2 have a more diminished initial drain current than amplifier 6 and therefore a larger recovery period. The drain currents also stabilize after the recovery period and present no differences in operation when compared to the non-stressed amplifiers. The non-stressed amplifiers all show almost no initially diminished drain current. During this test there are no anomalies in the behavior of the drain current for any of the power amplifiers.

Figure 5.31: Test fixture 1, stress 3 data. The top graph is the change in input power and is located at point D in the test set up block diagram of figure 5.1. The middle graph is the drain current and is located at point E in the test set up block diagram. The bottom graph is the change in output power and is located at point F in the test set up block diagram. After a recovery period for the drain currents no abnormal behavior is observed.

Figure 5.32: Test fixture 2, stress 3 data. The top graph is the change in input power and is located at point D in the test set up block diagram of figure 5.1. The middle graph is the drain current and is located at point E in the test set up block diagram. The bottom graph is the change in output power and is located at point F in the test set up block diagram. After a recovery period for the drain currents no abnormal behavior is observed with the exception of small variances in input power near the end of the test run.

5.4.3.4 Post Stress Test 4

Figure 5.33 and 5.34 display the performance results of all eight amplifiers versus time after DC stress test 4 has been performed. The fourth stress results in a gate leakage current of 7mA. The power amplifiers are then operated for a period of 17 days. This final stress test only contains two stressed amplifiers, 1 and 6. During the DC stressing of amplifier 2 a complete failure of the device occurred. The channel of the HEMT no longer has the ability to be pinched off and therefore any significant bias voltage on the drain would cause the device to destroy itself. The results are discussed in section 5.4.2 and can be seen in figure 5.24.

For both test fixtures 1 and 2 the input PA powers are very stable with changes consistently less than one tenth of a decibel. Test fixture 2 shows more stability at the beginning of the test than at the end. Test fixture 1 shows very stable output power for each amplifier while test fixture 2 shows initially stable output powers.

On test fixture 1 it can be seen that a sudden jump in input power for amplifier 1 occurs just before the midpoint of the test and at the same time a drop in drain current and increase in output power occurs. Later in time there is a sudden drop in input power to amplifier 1 and at the same time the drain current increases to nearly the value it was at before the initial drop.

On test fixture 2 it can be seen that about a third of the way through the test the drain currents of amplifiers 5 and 7 drop to 50mA while amplifier 6 drops to zero. At this point the RF power is turned off to test fixture 2 and amplifier 6 is disconnected to undergo a fifth DC stressing. The purpose of this is explained in section 5.4.2 page 79. After being reconnected amplifier 6's drain current shows a recovery period.

The stressed device drain currents behave the same as before with an initial diminished value that goes through recovery and then behave the same as non-stressed device drain currents. The non-stressed do not show a large initially diminished drain current on either test fixture.

5.4.3.5 Drain Current Comparison

Table 5.4 below shows the difference between initial and final device drain current values for each stress test run. The stressed devices show a significantly larger change in drain current throughout the test run. Device 6 shows the smallest change in drain current for a stressed device, leading to more evidence of two types of devices present in this experiment.

Device	Test Run 1 Delta Drain Current (mA)	Test Run 2 Delta Drain Current (mA)	Test Run 3 Delta Drain Current (mA)	Test Run 4 Delta Drain Current (mA)
1	14.8	18.3	19.3	14.7
2	15.2	20.8	15.4	n/a
3	2.1	-2.2	1.7	0.4
4	2.8	1.7	1.7	0.5
5	0.1	0.2	0	-1.4
6	3.8	4.5	3.2	3.6
7	-0.4	3.7	0.6	1.3
8	19.1	18.6	n/a	n/a

Table 5.4: Changes in drain current from the initial values to the final values for each experimental test run. The stressed amplifiers (1, 2, 6, 8) show significantly greater change throughout the test than non-stressed amplifiers (3, 4, 5, 7).

Figure 5.33: Test fixture 1, stress 4 data. The top graph is the change in input power and is located at point D in the test set up block diagram of figure 5.1. The middle graph is the drain current and is located at point E in the test set up block diagram. The bottom graph is the change in output power and is located at point F in the test set up block diagram. PA 1 drain current has 2 abrupt changes that occur at the same time as small spikes in the change in input power.

Figure 5.34: Test fixture 2, stress 4 data. The top graph is the change in input power and is located at point D in the test set up block diagram of figure 5.1. The middle graph is the drain current and is located at point E in the test set up block diagram. The bottom graph is the change in output power and is located at point F in the test set up block diagram. There is a large spike seen in the graphs near the first third of the test that is caused from the RF power being turned off to the test fixture to allow for further stressing of PA 6.

5.4.3.6 Output Power Comparison

Figure 5.35 displays the relative output power for each power amplifier operated on test fixture 1 and Figure 5.36 displays the relative output power for each amplifier operated on test fixture 2. The data is presented to provide a comparison between changes in performance for both stressed and non-stressed devices. As mentioned in the beginning of section 5.4.1 a comparison needs to be made between the baseline data and post stress data. The graphs present this comparison along with comparison of device performance for each subsequent stress test.

The relative output power for the baseline test in general shows a more erratic behavior than post-stress tests. This is attributed to the mechanical operation of the SA measurement described in section 5.4.1 but may also support that further device burn-in occurs throughout the baseline test.

For all the stressed amplifiers the relative output power is initially diminished and recovers with time for each post-stress operation. This matches the behavior of the drain currents and is expected. The non-stressed amplifiers do not share this consistent increase in power vs. time for each test run as expected once again by the behavior of the device drain currents. Only in test runs when the drain current for non-stressed amplifiers is initially diminished is the output power also initially diminished.

The data also shows constant changes in relative output power for each amplifier from test to test. This eliminates any erratic behavior seen from test to test to be solely attributed to DC stressing effects and indicates that other factors are present.

The long term performance results show no difference between stressed and non-stressed amplifiers. Cases exist for both categories of amplifiers, stressed and non-stressed, that show both erratic and stable performance, preventing this behavior to be solely attributed to DC stressing.

Figure 5.35: Test fixture 1 power amplifier relative output power for each test run. These measurements all occur at point F in the test set up block diagram of figure 5.1. After an initial recovery period there are no major observable differences between stressed and non-stressed amplifiers and changes in relative power from test to test occur in all amplifiers.

Figure 5.36: Test fixture 2 power amplifier relative output power for each test run. These measurements all occur at point F in the test set up block diagram of figure 5.1. After an initial recovery period there are no major observable differences between stressed and non-stressed amplifiers and changes in relative power from test to test occur in all amplifiers.

Chapter 6 Conclusions and Future Work

6.1 Conclusions

This thesis performs work that monitors the behavior of Nitronex NPTB00004 GaN HEMTs operated in a class F power amplifier configuration. The main goal for this document is to observe how power amplifiers that are subjected to DC stressing in the $V_{ds}=0$ state perform in comparison to non-stressed power amplifiers when both are operated under the same conditions. This investigation provides an expansion, or next step, to the DC studies outlined in chapter 4.

Analysis of the performance data for each amplifier shows that there are differences in the drain current and output power behaviors during the initial time of operation for the amplifier performance test runs. These differences in behavior are observed as a transient reduction in initial drain current, and relative output power. The initial reduction in drain current is predicted by all the DC studies referenced and discussed in chapter 4. However the drain currents for the stressed power amplifiers are transient and do recover with time.

Point 1

Once the transient in device drain current, pictured below in Figure 6.1, has disappeared there is no distinguishable difference in performance between the stressed and non-stressed power amplifiers.

Figure 6.1: Reduction in initial drain current during amplifier operation after device stressing.

Point 2

Further analysis is performed to determine if the observed behavior during the RF operation of the devices can be attributed to any previously studied degradation mechanisms in the literature from chapter 4. The initially diminished drain currents observed fit nicely with the inverse piezoelectric mechanism that is thought to be the driving mechanism for failure during $V_{ds}=0$ DC stressing.

Point 3

The traps that are generated during the $V_{ds}=0$ stressing have an associated energy requirement in order for electrons to be released. When the device is operated as a power amplifier for a long period of time there is a significant amount of heat generated within the device. This heat provides energy to the trapped electrons releasing them and therefore allowing for a recovery in device drain current. This recovery was observed to have a time constant on the order of 3 hours for stressed devices.

Point 4

The gate leakage current is another parameter that supports the results of the DC $V_{ds}=0$ stress test. It is the only measured parameter that maintains its degraded state regardless of how the device is handled. Even after being operated as a power amplifier the gate leakage current does not show recovery further indicating the presence of traps in the form of electrically active defects. The transfer curves for each device show recovery after being stressed when operated as a power amplifier.

Points 1-4 substantiate the hypothesis that DC stressing in the $V_{ds}=0$ state does in fact produce electrically active defects in the device that alter its performance, but that these defects can be overcome when enough energy is supplied to the device. These defects once again mostly agree with the inverse piezoelectric failure mechanism.

The small initial reductions in drain current and output power sometimes seen in non-stressed devices can be attributed to process dependent defects. These defects may be dislocations that act as traps formed during the growth of the HEMTs. Through the same process of heating and adding energy mentioned for the stressed devices electrons in traps of non-stressed devices can overcome potential barriers and escape.

In conclusion this thesis demonstrated that devices exposed to DC stress conditions are permanently degraded, but when operated as RF power amplifiers show recovery and given enough time, behave similarly to non-stressed devices.

6.2 Future Work

The longest period of time studied in this work is 17 days. With the gained understanding of device behavior during DC stressing the next logical step would be to determine if stressed devices suffer long term performance problems. This can be achieved by operating the devices for longer periods of time, from months to a year, and monitoring similar performance criteria set forth in this document. The additional study of how junction temperature affects device performance would be useful.

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