CASCADED HIGH VOLTAGE CONVERTER WITH VARIABLE CONTROL FOR PULSED ELECTRIC FIELD APPLICATIONS

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ABSTRACT

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Living a sustainable lifestyle while facing increasing population and decreasing natural resources has become one of humanity's largest challenges. Locating fossil fuels is becoming more difficult while the demand for them to power our societies is ever increasing. Instead of finding more efficient methods of extracting fossil fuels, developing technologies that create renewable substitutes for fossil fuels is now the strategy. Algae biofuel matches fossil fuel performance while also meeting the criteria for renewable energy. The focus now shifts to finding methods for commercially producing algae biofuel. Therefore, the objective of this thesis is to develop a system that provides the flexibility in finding the optimum operating conditions for lysing algae. Lysing is the process of disrupting the cell membrane in order to isolate the cellular components necessary to produce biofuel. The proposed system consists of cascaded power converters that provide a pulse output voltage in order to create a pulsed electric field (PEF) to lyse algae. The proposed system is unique from any known PEF systems because it provides the ability to independently adjust peak voltage, pulse width and frequency of the output voltage. This in turn provides great flexibility in determining optimum pulse voltage at various operating conditions for lysing algae. The system was tested on its ability to control the required variables while maintaining independence from the other variables. The new network was also designed and tested on how well it regulated the specific output waveform under the effects of different load currents as well as variations in the input voltage.

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Chapter 1 Introduction

Sustainability is the capacity to endure or maintain. Since the early 1980s, there has been an increased effort for human sustainability on Planet Earth which led to the United Nations defining sustainability as “sustainable development that meets the need of the present without compromising the ability of future generations to meet their own needs” [1]. Although a simple concept, it has proven to be one of the largest challenges facing society today as well as future generations to come.

In 2005, the World Summit reiterated the need to aggressively tackle the issue of sustainability. They reaffirmed their “commitment to achieve the goal of sustainable development by...committing [themselves] to undertaking concrete actions and measures at all levels and to enhancing international cooperation”. They will “promote the integration of the three components of sustainable development- economic development, social development, and environmental protection- as interdependent and mutually reinforcing pillars” of leading a sustainable lifestyle [2].

A system to measure humanity’s Ecological Footprint was developed in order to track the progress of these new efforts. This system is a standardized measurement of Humanity’s demand on the Earth’s ecosystem and the planet’s ability to regenerate the natural capital humans consume [3]. The unit of measurement is global Hectares, the area of land required to feed, exploit materials, produce energy, and rid waste as a result of activity. In 2007, two years after the UN declared to aggressively address sustainability, the human population’s total Ecological Footprint measured at 1.5 Earths [4]. This means that humanity was using ecological resources 1.5 times faster than the Earth’s ability to renew them. Humans are living well beyond the carrying capacity of Earth creating an unsustainable lifestyle.

Individual countries of the United Nations were tested against two variables, Ecological Footprint per capita and Standard of Living. As shown in Figure 1.1, only one country is living a sustainable lifestyle while also meeting standards of human development. The United States claimed the second largest footprint at 9.5 Hectares, 4 ½ times the threshold for sustainability, while only having a Human Development Index only 1.6 units above the threshold.

Figure 1.1: Ecological Footprint of Humanity measured against Standard of Living [5].

The biggest challenge to sustainability is the dangerous “combination of population increase in developing worlds and the unsustainable consumption levels in developed worlds” [6]. The United Nations measures the current population at a fraction over 7 billion and is expected to grow exponentially. As shown in Figure 1.2, the population projects to exceed 9 billion by 2050. Therefore,

not only is there a need to reduce the Ecological Footprint of the current population, growth in population means the threshold for sustainability is further reduced on a per capita basis.

Figure 1.2: World Population and projected growth [7].

An increase in population means an increase on the stress humanity places on the Ecosystem. Only healthy ecosystems can provide the resources necessary to sustain a decent standard of living therefore the longer humanity remains unsustainable, the more difficult it becomes to be sustainable. The only logical solution is aggressive management of human consumption of natural resources. The Environment Department of the World Bank, spearheaded by economist Herman Daly, created three basic guidelines for sustaining ecosystems [8].

1. Renewable resources should provide sustainable yield.
2. For non-renewable resources there should be equivalent development of renewable substitutes.
3. Waste generation should not exceed assimilate capacity of environment.

The largest consumption of resources comes from the Energy sector. Since the Industrial Revolution, countries have relied heavily on Fossil Fuels to power growth. This growth leads to breakthroughs in technology, politics, and economics, particularly in Western Civilizations. Maintaining this growth and lifestyle further increases the dependency of Fossil Fuels. In addition, developing countries trying to achieve this high standard of living require intense high consumption of energy to power their growth. However, because Fossil Fuels require millions of years to form, they are non-renewable resources and reserves are being consumed much faster than the rate of production. Figure 1.3 shows the enormous dependency of Fossil Fuels that contribute to 88% of the World's energy sources. This level of consumption cannot be sustained and there is yet to be an equivalent substitute.

Figure 1.3: Breakdown of Energy resource consumption as of 2010 [9].

According to the Theory of Peak Oil, at the current rate of consumption each Fossil Fuel has the following years of production: Coal 148 years, Oil 43 years, and Natural Gases 61 years [10]. The theory also suggests that oil production will decline more rapidly because the resource will no longer be economically feasible or physically possible to produce. Instead of trying to find more efficient ways of harvesting fossil fuels, there should be an effort in commercialization of renewable energy, developing less carbon consuming technology and transportation, and helping individuals lead carbon neutral lifestyles. This solution came with the development of Biofuels which use biological carbon fixation to derive energy. Carbon Fixation is the process where photosynthetic organisms turn inorganic carbon (CO_2) into organic compounds, usually in the form of carbohydrates. These carbohydrates can then be extracted and processed to form fuel.

Transportation is currently the largest application for Biofuels. Transportation fuels require clean burning fuels in order to keep the engine clean, efficient (less heat dissipation), and to minimize pollution. The first generations of Biofuels came in the form of sugars, starches, and vegetables. These compounds are fermented, distilled, dehydrated, and evaporated in order to create fuels for vehicles. The resulting products were Bioethanol, Biodiesel, Green Diesel, and Vegetable Oil which are considered viable substitutes to Fossil Fuels. In 2010, biofuels constituted 2.8% of the world fuels for road transport [11]. Over 28 billion gallons of biofuels were produced with the United States and Brazil producing 90%.

Although Biofuel provide a substitute for Fossil Fuels, they are not a viable replacement in terms of human sustainability. The production and use of biofuel actually causes various social, economic, environmental, and technical issues. The biggest issue with Biofuels is the fuel vs. food debate. Biofuels are made from sources that contribute greatly to fueling the human body. In order for mass production of biofuels, an increase of production of sugars, vegetables, and starches would be necessary. These resources would then be reserved for production of biofuels instead of nutritional support for the body.

On the global scale, there is not an abundance of natural food to justify using those resources to create fuel for transportation. Doing so would increase poverty, decreasing standard of living, and still not contribute to sustainable development. In fact, more land would be needed to produce these compounds further increasing the human ecological footprint and making humans less self-sustaining. According to the Center for Agricultural and Rural Development, the new demands for these agricultural goods have led to a 30% increase in food prices in related foods [12]. In addition, producing biofuel on a commercial level would require deforestation and cause soil erosion and a loss of biodiversity. Last of all, the process for creating biofuels is not an efficient method. The net energy gain in Biofuels, energy put into manufacturing fuel compared to the energy created when fuel is burned, is significantly lower than Fossil Fuels. Biofuels have a net energy gain in the neighborhood of 0.45 depending on the type of process and the type of biofuel. This is almost half of the net energy gain of gasoline which measures around 0.81. To summarize, even though first generation biofuels are a valid energy source substitute for fossil fuels, they create more obstacles when trying to become a sustainable society.

Algae became the answer to debatable land based biofuels. Algae would not diminish food resources because it is not part of the human food chain. It can be harvested on currently unprofitable lands as well as waste water from other industries. The process to produce algae is also low cost when compared to other biofuels and does not negatively affect the ecosystem. In addition, algae consume a significantly larger amount of CO₂ than the amount released when burning algae biofuel. Having large amounts of algae population will reduce the concentration of CO₂ in the atmosphere canceling greenhouse effects. Algae are composed of high concentration of lipids (fats) which result in high yields of biofuel. The high fat composition also results in algae fuel burning cleaner and more efficiently than petroleum. In conclusion, algae can be produced easily and cost effectively in a robust environment, do not put further stress on other resources, match the performance of fossil fuels, and meet the requirements for human sustainability.

Chapter 2 Background

2.1 Converting Algae into Biofuel

In 2007, Continental Airlines became the first US commercial flight fueled by a sustainable biofuel blend [13]. The Boeing 737 aircraft flew from Houston to Chicago powered by algae biofuel blended with conventional jet kerosene. Results concluded that the blend produced better flight mileage due to the biofuel burning cleaner and at lower temperatures; which also resulted in a 4% increase in energy density. Airline companies and militaries around the world, seeing no modification to the jet engine is necessary, started investing in commercially produced algae biofuel [14].

Harvesting algae is well documented and capable of being produced at commercial levels. However, algae lysing, the process of disrupting the cell membrane to isolate lipids, is a brand new technology still being developed. The current mechanical and chemical methods are energy intensive, expensive, and present safety and health issues [15].

Figure 2.1: The simplified process for creating algae biofuel [16].

The three new extraction methods expected to replace the unsatisfactory technology are enzymatic hydrolysis, amphiphilic solvents, and pulsed electric field (PEF) technology [16]. Of the three, the pulsed electric field technology looks the most promising for extracting algae oil on a commercial level. The current leader in this extraction method is Massachusetts based Diversified Technologies, Inc. They estimate PEF technology would be a low energy process of lysing that would only cost \$0.10/gallon. This is a significantly cost-reduced process compared to conventional methods which cost \$1.75/gallon to lyse algae. This low cost, low energy, and safe process leads many biofuel experts to believe pulse electric field technology is the key to the commercialization of algae biofuel.

2.2 Pulse Electric Field Technology

The first techniques for producing high voltage pulsed electric fields for lysing were adopted from food pasteurization systems. They consist of Resistor-Capacitor (RC) and Resistor-Inductor-Capacitor (RLC) circuits to create a pulsed electric field [17]. Figure 2.2 shows the most common circuits and the PEF waveforms. A large DC voltage is necessary to charge the capacitor(s) that eventually create the high voltage PEF to lyse algae. This was accomplished by stepping up an AC signal, usually 120 Vrms, using a high turns-ratio power transformer followed by a rectifying stage. However, the simplicity of these circuits inhibits the user's ability to control them.

Figure 2.2: Basic RC (a) and RLC (b, c) circuits used to create pulsed electric fields for algae lysing [17].

The peak output voltage is set to the HVDC applied to the circuit. Manipulating this peak output voltage requires creating a new circuit, such as a voltage doubler, or changing the turns- ratio of the input stage. As shown in Figure 2.3, the main components are located on the high voltage side and must be rated accordingly. This requires large and expensive components that can withstand the high peak output voltage. In addition, maximum circuit efficiency is 42% [18]. Power dissipated in the charging resistors, DCR's of the Inductors, and ESR's of the capacitors leads to large losses and increased input power. The biggest drawback from the circuits is the lack of user control when operating the circuit. The pulse width is a function of the component values or the circuit. Changing the pulse width requires changing component values. The frequency is adjustable using the switch, most likely a MOSFET with very high breakdown voltage, but can only repeat once the reactive elements have been fully charged. These simple circuits lack the ability to make adjustments to variable parameters of the load. If the load in the treatment chamber has known values for what the voltage, current, and frequency should be the circuits of Figure 2.2 will suffice. However, this is not the case for algae lysing.

Figure 2.3: A closer look at the common square wave generator and the produced output voltage [18].

When controllable output voltage became required, power electronics was incorporated into algae lysing. The addition of new power electronic techniques give the user control and the ability to convert electrical power in order to effectively and efficiently lyse algae. Using power electronic topologies give the user the ability to produce a regulated and precise output voltage, switching frequency, pulse width, as well as make each one adjustable if needed. Because of this fact, the newest techniques for pulsed electric field technology incorporate power electronics. Algae lysing, and related applications such as food pasteurization and cell treatment, use power electronics for optimum solutions to specific applications. In addition, power electronics offers greater circuit efficiency, making commercialization capable and economically feasible. Although cost effectiveness is beneficial, the importance of power electronics is that building low efficiency converters with large output power is impractical [19]. Given a fixed output power, greater efficiencies correspond to a decrease in required input power and system power losses. Power losses are dissipated through the circuit, usually as heat, which must be removed. The process of removing heat is usually difficult and expensive. Failure to remove heat often means sacrificing system reliability [20]. These problems are magnified when dealing with high output power. As mentioned before, previous PEF techniques often exhibit $\eta \leq 42\%$. If 100 W is required to lyse algae, the circuit requires 238 W. This corresponds to 138 W dissipating within the system causing elements in the circuit to overheat or breakdown. Power electronic topologies are capable of greater efficiencies yielding more reliable and practical systems.

The five most common power electronic topologies that will create a PEF are Flyback, Forward, Push-Pull, Half-Bridge, and Full Bridge [21]. Flyback and Forward are usually for low power applications (5-150 W), the Push-Pull is usually for medium power (300 W), and the bridges are used for high power applications (>500W) [22]. These topologies can operate using a rectified AC power source as input voltage. In addition, these topologies are isolated which is important for system protection and safety because they are connected to the grid. The reason they are isolated is because each topology

contains a transformer which is also capable of stepping up or down voltages. The user is then able to produce a voltage much larger or smaller than the input voltage which is key for high intensity pulsed electric fields.

In 2006, the circuit in Figure 2.4 was proposed in [23] for Food Processing applications. The circuit is based off the Flyback topology but uses programmable logic to drive the MOSFET instead of using a feedback system. No output capacitor network was connected creating a square wave output voltage. Duty cycle and frequency are controlled using the gate driver. The voltage, however, is not variable and set using the turns-ratio of his transformer. Altering the output voltage would require using a Variac to control the input voltage amplitude. The circuit was designed for food processing and only required low magnitude output voltages; therefore, a step down transformer was used.

Figure 2.4: Flyback based topology producing controllable PEF for food processing applications [23].

The output voltage is shown in Figure 2.5. The peak output voltage is only 1 V and the period is 10 μ s. In this application, the electric field strength was accomplished using small spacing between the parallel plates. Although this is sufficient for testing, it is more practical to produce high voltage in order to create large electric fields. The output voltage also peaks then decays exponentially. For food pasteurization applications, this decay in the output voltage is acceptable because the intent is to destroy bacteria, which is accomplished with the peak output voltage. This type of ingenuity shows how power electronics must play a large role in PEF technology advancements.

Figure 2.5: Output voltage of Flyback altered circuit in figure 2.4 (100mV/div, 500uS/div).

Since algae lysing is relatively new, there are still many unknowns on optimum methods to lyse algae for biofuel. The main objective is to break the algae cell membrane in order to release the unharmed lipids. It is a controlled shock treatment where, unlike food pasteurization, so that the required cellular components are unharmed. The fact that there are so many unknowns about algae lysing is part of the reason the thesis proposal came to be. In order to accomplish a controlled pulsed

electric field, all parameters must be adjustable. This is accomplished using different power electronic topologies or a combination of them to eliminate the unknown variables of algae lysing.

In this thesis, a new method for producing a Pulsed Electric Field capable of lysing algae is proposed. The new converter offers the ability to alter the voltage magnitude, period, and duty cycle of the pulsed electric field. Each parameter can be changed individually and without altering the circuit. In addition, each parameter will have a large range for which to change. The new converter will be a robust solution capable of producing a large variety of pulsed electric fields.

Chapter 3 Design Requirements

3.1 Thesis Overview

The purpose of this thesis is to develop a robust power converter that provides a pulse output voltage with adjustable peak voltage and pulse width. The adjustment of the peak voltage and the pulse width can be done independently from each other. This will therefore provide the flexibility to find the optimum operating conditions under which algae lysing occurs. For algae lysing, the three main variables which will be investigated are voltage amplitude, frequency, and pulse width.

Figure 3.1 gives a high level block diagram of the functionality of the proposed thesis. The system will use 120Vrms AC voltage waveform. This allows the user to connect the system to a wall outlet and operate the system anywhere a grid connection is available. The output voltage is a square wave having the amplitude A , the period T , and the pulse width of the $D \cdot T$, D is duty cycle. The three variables will be adjustable using control signals the user inputs to the system. The adjustments should be easy to make and not require system modification.

Figure 3.1: Overall block diagram of proposed circuit showing inputs and outputs.

As with any system it is key to establish goals, rules, and regulations. The most challenging aspect of this project is setting design parameters because algae lysing is a new technology; therefore there is no set range of conditions that best lyse algae. Once again, the objective is to create a system to find the unknown variables to lyse algae, not necessarily create the optimum solution for lysing algae. In addition, the system must be robust to different loads due to testing on different algae strains. Therefore, the best approach is to set realistic ranges of each variable and design accordingly. Table 3.1 summarizes the system objectives. An output voltage range of 10V-80V will allow the user to adjust the electric field strength across the load. Adjustable voltage define what electric field strength lysing occurs without damaging the required cellular components. The target frequency range of the output square wave is from 60Hz to 100 kHz which corresponds to periods of 17ms down to 10 μ s. This adjustable parameter will determine how often the output voltage must be applied to the load to rupture the cell membrane. The duty cycle will be adjustable from 20% up to 80% in order to discover what duration of the period the voltage should be applied to the algae. Most importantly, the user will be able to adjust each variable individually while keeping the others constant in order to find the optimum conditions lysing occurs for different strands of algae.

Table 3-1: Target performance specifications and range of operation of proposed thesis.

Thesis Objectives					
	Output Voltage	Output Power	Frequency	Period	Duty Cycle
Minimum	10 V	-	60 Hz	10 μ s	20%
Nominal	40 V	-	-	-	50%
Maximum	80 V	20 W	100 kHz	17 ms	80%

Vout	Full Load Current
10 V	2A
40 V	500 mA
80 V	250 mA

Since high voltages are used and the system is connected to the grid, the system must be isolated. Just in case the system is shorted on the output, the isolation will prevent very large amounts of current to be sunk. The system will be designed for a maximum output power of 20 W in order to set limits on the output current at different output voltages. The full load current ratings at different output voltages are also summarized in Table 3.1.

3.2 Circuit Solution

In order to give a robust solution to the thesis objectives a series of cascaded systems was designed to yield accurate controllability for the user. By cascading different power electronic topologies, each with a specific function, the system will be able to meet the design requirements. A detailed block diagram is shown in Figure 3.2. The system contains a rectifier circuit, to ensure the system does not deal with negative voltage from the input power. A switching DC-DC converter will be a critical component of the design. The regulator establishes and maintains a constant DC voltage throughout the system regardless of the load. In addition, the regulator is the component that will allow the user to adjust the output voltage. Another critical component in the system is the two switch network. The network will allow the user to determine the frequency and duty cycle of the output square wave. The following sections explain the desired objectives of each stage within the system.

Figure 3.2: Block diagram of proposed thesis to achieve thesis objectives.

3.2.1 Input Stage Rectifier

The system is powered by an AC power source so the first stage rectifies the AC signal to produce a DC voltage. Although not a complicated component of the system, the rectifier is critical to the system because the DC-DC converter operates on a DC power supply. Therefore, the only requirement of the input stage is that it rectifies the input voltage. A full wave rectifier as shown in Figure 3.3 is recommended as it produces a higher average voltage to the converter input. A higher average voltage will result in reduced input voltage ripple into the switching converter. Since the power from the grid is regulated to 120 Vrms $\pm$ 5%, the rectifier should operate with a maximum of 126 Vrms (178.2 Vpk) input voltage [24]. Another important design consideration is the current capability the rectifier can withstand. There is not a significant amount of input current to the system since voltage is being stepped down however it is important that the diodes be rated for the forward current. The last parameter to consider is the voltage drop across the diodes when they conduct. The less power dissipated through the rectifier the higher the efficiency.

Figure 3.3: Full wave rectifier circuit showing expected output voltage and ripple.

The rectifier should convert the 120 Vrms AC signal shown in Figure 3.3 and rectify the signal to the voltage labeled DC out. The peak voltage should be 170 V. The output voltage has large ripples, 170V to be exact; however adding large high voltage capacitors will reduce the ripple to hold a clean DC voltage. Table 3.2 gives a summary of the specifications of the rectifier. Once again, the minimum and maximum voltages depend on the signal from the grid. Since the wall outlet voltage is regulated to 120Vrms +/- 5%, the rectifier should be able to operate under these conditions. The important voltage is the peak inverse voltage which is 178V. This is the voltage the diodes must block without breaking down. The frequency of the input signal is 60 Hz; therefore there is no need for the diodes to have high switching capabilities.

Table 3-2: Design requirements for input rectifier.

Rectifier Objectives					
	Input Voltage	Output Voltage	Peak Reverse Voltage	Output Power	Frequency
Minimum	114 Vrms AC	161 V rectified	-	-	-
Nominal	120 Vrms AC	170 V rectified	-	-	60 Hz
Maximum	126 Vrms AC	178 V rectified	178 V	20 W	-

3.2.2 Switching Regulator

A Flyback converter will be selected for the switching regulator due to the low part count while providing the isolation necessary for high voltage applications. The Flyback will be responsible for maintaining a constant DC voltage rail within the system. The Flyback plays a significant part in the system stability and will be regulated accordingly. Figure 3.4 shows a simplified circuit for the Flyback topology. It is an isolated topology and capable of a wide range of output voltages which is an objective of the design.

Figure 3.4: Traditional Flyback topology with common components.

Table 3.2 lists the design requirements of the Flyback converter. As mentioned in the previous section, the input voltage is a rectified 120 Vrms AC signal. However, the design must operate with an input voltage range of 161 Vpk-178 Vpk to account for the $\pm 5\%$ change in the input voltage. In addition, the converter must have a line regulation less than 5%; the converter must maintain the output voltage within 5% of the nominal value given this change in the input voltage (refer to equation 3.1). The load regulation must also be less than 5%, the output voltage must be maintained within 5% despite the load current changing from 10% to 90% (refer to equation 3.2). The peak to peak output ripple should not exceed 5% of the output voltage. In order to achieve the system goal of having an output voltage range of 10-80 V, the Flyback converter must have an output voltage range of 10 V to

80 V. The ideal output power of the converter is 20 W which will eventually be supplied to the load.

Realistically, the actual design will account for power losses in the following stages to still supply 20 W to the load. The last design requirement is that the converter, regardless of output voltage, should have efficiency greater than or equal to 75% at full load.

Table 3-3: Flyback range of operation and performance goals.

Flyback Objectives						
	Input Voltage	Output Voltage	Output Power	Load Regulation	Line Regulation	Vout Ripple
Minimum	161 Vpk	10 V	-	-	-	-
Nominal	170 Vpk	40 V	-	-	-	-
Maximum	178 Vpk	80 V	20W	5%	5%	5%

Vout	Full Load Current	η @ Full Load
10 V	2.0 A	75%
40 V	300 mA	75%
80 V	250 mA	75%

$$\%Line\ Regulation = \frac{V_{out(high-input)} - V_{out(low-input)}}{V_{out(nominal)}} \times 100\% \quad (3-1)$$

$$\%Load\ Regulation = \frac{V_{out(minimum\ load)} - V_{out(full\ load)}}{V_{out(nominal)}} \times 100\% \quad (3-2)$$

3.2.3 Two Switch Network

A Two Switch Network is implemented into the system in order to take a DC voltage and convert the signal into a periodic square wave. Figure 3.5 shows the schematic of a classic Half Bridge converter from which the idea was derived from. Whereas a half bridge is designed to drive inductive loads, the two switch network, Figure 3.6, is designed to produce a square wave for resistive loads. The DC voltage, V_{cc} , is applied to the rail and represents the peak value possible on the output waveform. The

output voltage of the two switch network is shown in Figure 3.7. The voltage amplitude A would equal V_{cc} of Figure 3.6. The periodic waveform of Figure 3.7 is generated by the control signals that drive the MOSFETS Q1 and Q2. The control signals create a current path resulting in a potential difference across the load. A driver IC is needed in order to send control signals that turn on the MOSFETS and turns them on quickly. The drivers have high current drive to charge the gate capacitance of the MOSFET quickly. The driver also ensures V_{cc} does not have a direct path to ground. The output waveform has a variable period and duty cycle by applying the correct control signals to the MOSFETS.

Figure 3.5: Simplified Half Bridge used in motor driving applications.

Figure 3.6: Two switch network circuit.

Figure 3.7: Output voltage of two switch network with variable duty cycle and constant period.

Figure 3.8: Output voltage of two switch network showing variable period and fixed duty cycle.

The two switch network will be responsible for establishing the period and duty cycle of output voltage. The user will have accurate control of these two variables by having the correct control signals. Table 3.3 details the design objectives of the two switch network. It should be able to operate from the output voltage of the Flyback converter. As stated in Table 3.2, the output voltage of the Flyback converter ranges from 10-80V therefore the two switch network should operate with an input voltage range from 10-80V. Through proper control signals driving the MOSFETs, the two switch network should create a square waveform. The two switch network should also be capable of adjusting each parameter individually. Figure 3.8 shows the output voltage with variable period while maintaining amplitude and duty cycle constant. The output voltage frequency range is 60 Hz to 100 kHz. In addition, the pulse width is adjustable which will determine the duty cycle of the output voltage. This is shown in Figure 3.7 where only the duty cycle is changing from waveform to waveform. Last of all, the two switch network should be capable of sinking the same current the Flyback outputs. The maximum sink current occurs when the rail voltage is 10 V and the two switch network should be able to pass 2A to the load.

Table 3-4: Summary of design specifications for the two switch network.

Two Switch Network Objectives

	Input voltage	output voltage	output power	Frequency	Duty Cycle
Minimum	10 V	10 V _{pk} sq. wave	-	60 Hz	20%
Nominal	40 V	40 V _{pk} sq. wave	-	-	50%
Maximum	80 V	80 V _{pk} sq. wave	20 W	100 kHz	80%

Vout	Full Load Current
10 V	2.0 A
40 V	500 mA
80V	250 mA

Chapter 4 Design and Simulation Results

In this chapter, the proposed system design to meet the design requirements documented in Chapter 3 is described in detail. Each stage in Figure 3.2 is analyzed using schematic diagrams, component calculations and selections, and simulations showing performance relative to design requirements. The last step is to integrate and analyze overall system performance.

4.1 Input Rectifier Design

Figure 4.1: Schematic for Full Wave Rectifier used for Input stage of system.

The Full Wave Rectifier implemented in Figure 4.1 is the basic circuitry needed for rectification from AC input to a DC output voltage. It consists of four diodes connected as configured in Figure 4.1. The input and output voltage relationship of this schematic is shown in Figure 4.2. The positive cycle of the sinusoidal input voltage V_{ac} passes through D1 and D4 and returns to the source. The negative voltage of the sinusoidal input is rectified by passing through D2 and D3 and returns to the source. Therefore the rectified voltage has a peak voltage of two diode forward voltage drops less than the input peak voltage. When selecting the components for a full wave rectifier, three important characteristics to examine are the diode's rated V_{RRM} , average forward current, and the forward voltage

drop. To determine what rated breakdown voltage should be, the peak input voltage must be known. As mentioned in section 3.2.1, when connected to the grid, the maximum peak input voltage is 178 Vpk. Therefore the rated V_{RRM} should be at least 178 V. Using simulation results, the maximum input current from the AC supply is 300 mA of average current; therefore the average current rating must be greater than this value. There is no specific forward voltage drop the diode must have, however the less voltage consumed by the diodes, the more voltage that is applied to the rest of the system. In order to meet these requirements, four MURS320 diodes will be used for the rectifier. The MURS320 diode has a maximum repetitive reverse voltage (V_{RRM}) of 200 V, an average forward current rating of 3A, and a forward voltage drop of 0.6 V [25]. The 200V is more than the required 178 Vpk, even leaving a 22V safety margin. The rated average forward current is ten times the required amount, more than enough for this application. The forward voltage drop is 0.6 V in normal operating conditions, when the junction temperature is less than 175 °C, meaning the input of the DC converter is 1.2 V less than the peak input voltage.

Figure 4.2: Input signal (A) compared to rectified signal (B).

With the basic diode rectifier, the output voltage will not be a flat DC voltage but rather follows the shape of the sinusoidal wave as shown in Figure 4.2B. This further requires adding a large output capacitor to minimize the ripple. The required capacitance value is determined by max allowable peak

to peak ripple acceptable for the next converter stage. The following illustrates capacitance value calculation:

INPUTS: Vac=120Vrms single phase, Output power of rectifier= 20 W

CONSTRAINTS: Output ripple less than 5%

ASSUMPTIONS: PF = 1, $\eta_{\text{rectifier}} = 95\%$

$$V_{pk} = 120 V_{rms} * \sqrt{2} = 170 V$$

$$V_{ripple} = 170V * 0.05 = 8.5V$$

$$P_{in} = \frac{P_{out}}{\eta} = \frac{20 W}{0.95} = 21.05 W$$

$$\Delta t = \frac{1}{2 * 60 Hz} = 8.3 ms$$

$$I_{rms} = \frac{P_{in}}{V_{rms} * PF} = \frac{21.05}{120} = 175mA \quad \text{where } I_{rms} = i_c$$

$$C = i_c * \frac{\Delta t}{\Delta V_c} = 175mA * \frac{8.3ms}{8.5 V} = 171\mu F = C$$

The calculated capacitance is the minimum value required for a 5% output voltage ripple of 8.5V, which is a reasonable amount of ripple on the converter input. Figure 4.3B shows the output voltage with the calculated minimum capacitance of 171 μF . The results verify that this minimum capacitance will meet the output ripple requirement. Now that the minimum capacitance is known, two other factors that determine capacitor selection are rated breakdown voltage and equivalent series resistance (ESR). The maximum peak voltage is the same voltage the diodes were rated for, 178Vpk. The ESR of a capacitor causes the rectifier to be less efficient and also causes added spikes in the output voltage. Therefore selecting capacitors with a low ESR will make the rectifier more efficient and not cause added peak to peak ripple due to spikes. For a safety margin, the minimum capacitance was more than doubled (two 220 μF electrolytic capacitors in parallel) yielding an effective capacitance of 440 μF . Another 220 μF capacitor was connected in parallel to further reduce the effective ESR. Each capacitor

has a breakdown of 250 V. Since the maximum peak output voltage is 178 V, there is a safety margin of 72V. The total capacitance of the input filter is now 660 μ F. The added capacitance will lead to a smaller ripple in the output voltage and have the ability to source more current should the circuit demand it.

Figure 4.3: Full wave rectifier with capacitor and no load (A), and with capacitor and resistive load (B).

Figure 4.4 shows how changing the input voltage affects the rectified output voltage. The peak to peak output voltage ripple remains the same because the load current does not change. The peak to peak output voltage ripple is measured to be 8.5 V.

Figure 4.4: Rectifier circuit output measured with different AC input voltages.

4.2 Flyback Design

Figure 4.5: Flyback schematic used for controlling output voltage amplitude.

The next stage is a DC-DC converter responsible for providing a DC output voltage with varying magnitude. The Flyback topology was selected for the DC-DC converter as the second stage of the proposed system. The Flyback is an isolated topology because of the transformer's ability to electrically isolate the output from the input, which is critical because the system is connected to the grid. The Flyback is capable of producing large ranges of output power and more importantly, high output voltages at low power [26]. An important characteristic of the Flyback for this application is that the IC is not in the power path. The MOSFET gate drive voltage does not require amplification for operation. This in turn simplifies the design when compared to those topologies that require high side drive.

The Flyback design to implement in the overall system is shown in Figure 4.5. The LT3748 Flyback controller was selected as the IC for the converter. The LT3748 is a top of the line controller with few restrictions which gives the designer a large degree of freedom. The chip has high power capabilities, implements pulse frequency modulation to ensure boundary mode conduction mode, and

regulates output voltage from the primary side leading to fast transient responses [27]. These qualities will be key for the thesis system performance. The square wave generated on the output of the system is essentially a repetitive load transient for the converter. The converter will always remain in boundary conduction mode leading to higher efficiencies at the low output current levels the system outputs [27].

The LT3748 Flyback controller has a maximum input voltage of 100 V. Since the output of the full wave rectifier is 170 V DC, additional steps are necessary to protect the IC from the high input voltage. Figure 4.5 shows that a third transformer winding, also called an auxiliary winding, is necessary for the IC to regulate in offline applications, see Figure 4.5. This auxiliary winding is connected to a 50V reference and the feedback resistor. Because the output voltage is reflected to the auxiliary winding, the winding is used to relay the feedback voltage to the IC. The 50V is used to bias the IC. Only a couple milliamps are drawn from the voltage reference and it does not contribute significant power. The auxiliary winding, L1 in the schematic, should have the same number of turns as the secondary side of the transformer in order to relay the correct output voltage.

The maximum output power of the Flyback is limited by the external components of the IC. The three biggest limitations are voltage, current, and thermal based. The biggest voltage limitation comes from the MOSFET and the output diode reverse-bias rating while the current limitation comes from the transformer [27]. Since the maximum output power of the system is 20 W, maximum output current and voltage can be calculated.

The proper transformer must be selected in order for the Flyback current requirements to be met. Maximum output current of the Flyback is 2A and occurs when the output voltage is 10V.

Therefore the transformer must be able to transfer 2A to the secondary side without saturating the core. When selecting the transformer, the RMS and saturation current ratings of the secondary side must be 2A at the minimum. Because the IC operates in Critical Conduction Mode, the inductance of

each winding does not contribute to the performance of the Flyback. The inductance of the transformer windings usually determines the current mode of the converter. However, regardless of the current slope set by the inductance, the controller forces Boundary Conduction Mode.

The output voltage of the system can determine the turns-ratio requirement. The duty cycle of a Flyback is given by the following equation [28]:

$$D = \frac{(V_{out} + V_{Fdiode}) * N}{V_{in} + (V_{out} + V_{Fdiode}) * N} \quad (4-1)$$

where N is the turns ratio N_p/N_s . Since the minimum output voltage requirement is 10 V, equation 4-1 is used to determine the approximate duty cycle of the Flyback to achieve the output voltage. Assuming a voltage diode drop of 1 V (large drop), input voltage of 170 V, and a 1:1 turns ratio ($N=1$), the nominal duty cycle is approximately 6.1%. By increasing the turns-ratio, the duty cycle will increase. If the turns-ratio is set at $N=3$, the duty cycle is calculated to be 16.3% leading to a more realistic duty cycle for the controller. Using a step down transformer will allow low output voltages without over stressing the controller. Stepping down the voltage is not a requirement but a design feature to improve system operation.

When selecting a transformer the following requirements must be met. The saturation and RMS current ratings must be above 2A. The transformer must also have an auxiliary winding. A preferred turns-ratio of 3:1 must also be considered. For these reasons, the Midcom 31369R transformer was selected. The transformer was altered in order to meet the requirements and improve functionality. The transformer contains twelve pins and six different windings creating a 1:1:1:1:1:1 transformer. Each winding has a base inductance of 14.4 μ H, a RMS current rating of 1.6 A, DCR of 60 m Ω , and 500 V isolation between each winding [30]. In addition, each winding has a rated saturation current of 4.25 A; if more than 4.25 A of DC current is applied, the inductance will decrease approximately 15%. As

mentioned before, the output is regulated on the primary side of the transformer; hence a tightly regulated turns-ratio is important. The Midcom transformer has a regulated turns-ratio of $\pm 1\%$ [30]. In order to meet the Flyback requirements, the Midcom transformer was configured as shown in Figure 4.6. Pins 12 and 2, 11 and 3 were connected in series while pins 5 and 6, 8 and 7 were connected to form parallel winding. The configuration creates a 3:1 winding while still having an auxiliary winding to connect to the V_{in} of the IC.

Figure 4.6: Configuration of Midcom transformer implemented in Flyback.

The reason for connecting the transformer as shown in Figure 4.6 is to output low voltages, improve converter efficiency, and increase output current capabilities. Table 4.1 summarizes the characteristics of the transformer created for the Flyback and shows it meets the design requirements.

The primary side sees an increase in DCR and inductance with a decrease in saturation current. However, because the primary voltage is stepped down to the secondary side, the secondary current is three times the current of the primary winding; this results in a reduced need for high current capabilities of the primary side and less current being dissipated through the DCR. Connecting two winding in parallel on the secondary doubles the output current capabilities while dividing the effective DCR in half leading to increased efficiencies of the converter. The saturation current is also unaffected which is important to performance. In a Flyback, the core of the transformer is used for energy storage. If the core is saturated, the energy injected to the core is not transferred to the secondary and instead dissipated as heat [28]. The rated RMS current of the secondary side is now 3.2 A which is 1.2 A larger than the system requirement of 2 A, giving a large safety margin.

Table 4-1: Calculated characteristics of Flyback Transformer.

	Primary Side	Secondary Side
DCR	180 mΩ	30 mΩ
Inductance	129.6 μH	14.4 μH
I_{rms}	1.6 A	3.2 A
I_{sat}	1.42 A	4.25 A

For Series Windings
$$L = L_{base} * W_s^2 \quad (H) \quad (4-2)$$

$$I_{rms} = I_{rms\ base} \quad (A) \quad (4-3)$$

$$I_{sat} = \frac{I_{sat\ base}}{W_s} \quad (A) \quad (4-4)$$

For Parallel Windings
$$L = L_{base} \quad (H) \quad (4-5)$$

$$I_{rms} = I_{rms\ base} * W_p \quad (A) \quad (4-6)$$

$$I_{sat} = I_{sat\ base} \quad (A) \quad (4-7)$$

*W_s is the number of Windings connected in series, W_p is the number of winding connected in parallel

In order to meet the maximum 80 V output requirement of the system, the peak voltage of the MOSFET and the output diode must be rated accordingly. The theoretical maximum V_{DS} is given in Eq. 4-8 while the maximum output diode reverse voltage is given in Eq. 4-9.

$$V_{DS\ max} = V_{IN\ max} + (V_{OUT\ max} * N) \quad (4-8)$$

$$V_R = V_{OUT\ max} + \left(\frac{V_{IN\ max}}{N}\right) \quad (4-9)$$

Under the conditions of 80 V_{out}, 178 V_{in}, and N=3, the rated V_{DS} should be 418 V while the output diode reverse voltage should be rated for 140 V. However, these calculated values should be doubled to account for leakage inductance spikes on the drain of the MOSFET and the anode of the output diode [28]. Increasing the rated V_{DS} of a MOSFET usually increases R_{DSon} and increasing the rated breakdown voltage of a diode increases the forward voltage drop, which results in lower efficiencies. The proposed thesis implements a MURS320 output diode rated at 400 V and an Infineon SPA11N60C3 NMOSFET rated at 650 V_{DS}.

The main disadvantage of the LT3748 is the minimum load requirement. Output regulation depends on data gathered when the MOSFET turns off and the secondary winding conducts current [28]. For this to occur, a minimum load is required. When no load is applied, the output voltage steadily increases because of the lack of feedback so it is important to have a load. The minimum load is 2% of the maximum load current. The maximum load current is set by R_{sense} or R_3 of Figure 4.5. The full current of the system is 2 A therefore R_3 was set to 20 mΩ. The minimum load required to regulate effectively becomes 40 mA.

The output capacitors are critical to the ripple of the output voltage. Once again, the capacitance value required is determined by how much peak to peak ripple is acceptable on the output. The following illustrates how the minimum capacitance value is calculated [26]:

Given: $V_{out} = 10V$, $V_{in} = 170$, $N=3$, Full Load Current= 2A

Requirements: $\Delta V\% = 5\%$ (maximum possible ripple voltage to find $C_{out\ min}$)

Assumptions: $f_{sw} = 42kHz$ (from datasheet, slowest f_{sw} gives worst case scenario)

$$\frac{\Delta V}{V_o} = \frac{D}{RCf}$$

$$C_{min} = \frac{D}{R_{min} \times f_{min} \times \frac{\Delta V}{V_o}}$$

Using Equation 4-1, $D = 0.163$

$R_{min} = V_o / I_{fullload} = 5\Omega$, $\Delta V/V = 0.05$

$$C_{min} = \frac{0.163}{5 \times 42kHz \times 0.05} = 16\mu F$$

The minimum required capacitance to ensure less than 5% ripple is 16 μF . The maximum output voltage of the system is 80 V which means the minimum rated capacitor voltage must be above 80V.

The Flyback uses six 10 μF X7R capacitors in parallel. The effective capacitance is almost 4 times the required minimum. Each capacitor is rated at 100 V giving a 20V safety margin. The reason for using 6 capacitors in parallel is that the effective ESR is greatly reduced. This further reduces output ripple and improves converter efficiency.

Now that the Flyback is designed to regulate a DC output voltage, the feedback resistor determines what output voltage will be regulated. The equation given in [28] takes into account forward diode drops and the output capacitor's ESR to give an exact resistor value. However, given that the feedback resistor is a potentiometer, a good approximation of the output voltage is given by:

$$V_{out} = V_{BG} \times \frac{R_{FB}}{R_{REF}} \times \frac{1}{N_{PS}} \quad (\text{Eq. 4-10})$$

Where $V_{BG} = 1.223V$ and $R_{REF} = 6.04k\Omega$. Solving Eq. 4-10 for R_{FB} gives:

$$R_{FB} = \frac{V_{out}}{V_{BG}} \times N_{PS} \times R_{REF} \quad (\text{Eq. 4-11})$$

Since the auxiliary winding is connected to the feedback resistor, the turns-ratio of Figure 4-10 and 4-11 is one. Using equation 4-11, the feedback resistance was calculated for common output voltages. The results are located in Table 4-2. A key feature of the proposed thesis is the controllability of the output voltage magnitude. According to Figure 4.5, in order to easily change the output voltage, a potentiometer is connected to the Rfb pin as the feedback resistor. Table 4.2 summarizes what the potentiometer must be set to in order to achieve specific voltages and the full load at each voltage. In order to ensure the feedback resistor is never zero, a 40k resistor is placed in series with the potentiometer. The maximum output voltage requires 370 k Ω . A standard 500 k Ω potentiometer is used and it is the responsibility of the user not to exceed 370 k Ω . Exceeding beyond that amount could damage circuit components.

Table 4-2: Desired output voltage look up table with associated maximum load.

Rfb (Ω)	Vout	10% load (A)	90% load (A)	Full Load (A)	Full Load (Ω)
48.2 k	10	0.2	1.8	2	5
96.0 k	20	0.1	0.9	1	20
188k	40	0.05	0.45	0.5	80
280.1k	60	0.033	0.3	0.33	182
370 k	80	0.025	0.225	0.25	320

4.3 Flyback Simulation Results

Now that the design of the Flyback is complete, simulation results report how well the converter performs under multiple scenarios. The main responsibility of the converter is to regulate an adjustable DC output voltage. Simulations must be performed on how well the converter produces a desired output voltage and how well the voltage regulates the voltage at different loads and different input

voltages. To make the simulations as realistic as possible, real component models were used for the output diode and NMOS. The transformer was modeled according to Table 4.1.

Figure 4.7 shows two basic yet important aspects of the Flyback converter. Figure 4.7A shows that by simply changing the feedback resistor, the output voltage is set to a certain voltage. The feedback resistance for a certain voltage is also easy to calculate by following the datasheet. The steady rise time when powering the device is due to the soft start capacitor in order to limit the inrush current. Figure 4.7B shows the switch node corresponding to the output voltages of Figure 4.7A. The higher the voltage the higher the switch node leading to a higher rated V_{DS} MOSFET. No leakage inductance spikes are present in the waveforms because they cannot be modeled but the magnitude is exactly as calculated by Eq. 4-8. Figure 4.7B demonstrates the IC operates in PFM because the controller changes the gate signal frequency to regulate the output.

A

B

Figure 4.7: Simulated output voltage (A) and switch node voltage (B) at different feedback resistances.

The next simulations tested for load and line regulations. Figure 4.8 are the simulation results when R_{fb} is set to 96 kΩ. Figure 4.8A shows the output voltage when the nominal 120 Vrms is applied at the input along with minimum and maximum input voltage. Using Equation 3-1, the line regulation can be calculated. Line regulation simulations were done under full load conditions. Figure 4.8B shows the output voltages when different load currents, 25%-100% full load in increments of 25%, are applied to the system. As the output current increases, the converter does a better job of regulating the output voltage. Load regulation is calculated applying Equation 3-2 to the data found in Figure 4.8B.

Figure 4.8: Simulated output voltage at three input voltages (A) at four load currents (B) with $R_{fb}=96k$.

The same procedure was applied using a feedback resistance of $188k\Omega$. Figure 4.9A shows Line Regulation. It also shows that the output voltage ripple is smaller than in Figure 4.8A due to less AC current being dissipated through real component models. Figure 4.9B once again shows load regulation. The more output current drawn from the converter the lower the output voltage is.

Figure 4.9: Simulated output voltage at three input voltages (A) at four load currents (B) with $R_{fb}=188k$.

The line regulation continues to improve as the output voltage increases. The output voltages in Figure 4.10A do not deviate as much as in Figure 4.8A or Figure 4.9A. Figure 4.10B shows that at extremely light loads, the converter cannot regulate to the desired output. Even though the minimum load requirement is met, the converter does not receive the required feedback from the Flyback pulse [29]. The lack of current signal fed back causes the controller to regulate at a voltage slightly

higher than the theoretical output voltage. Once the load current is increased, the Flyback pulse is increased and the converter regulates closer to the theoretical value. Figure 4.10B exemplifies this concept when the output current increases from 84 mA to 168 mA; the output voltage decreases from 61.9 V to 60.7 V.

Figure 4.10: Output voltage at different input voltages (A) and different load currents (B) with R_{fb} set to 280k.

Figure 4.11: Comparing simulated load (A) and line (B) regulation at different output voltages.

Efficiency simulations were calculated at 20V, 40V, and 60V at their respective full loads. Output ripple was also calculated. A graphical depiction of the data is shown in Figure 4.11A and 4.11B. For these simulations, an estimate of each capacitor's ESR was included in the circuit model. As shown in Figure 4.12, the output capacitor's ESR causes a spike in the output voltage ripple. When the MOSFET is turned off, the energy stored in the transformer is dissipated to the load, some of which is dissipated

through the ESR of the capacitor causing the spike. Once the MOSFET is turned back on, the transformer begins to store energy, leaving the output current to be supplied by the output capacitors. When capacitors discharge, the output voltage decreases as shown in Figure 4.12. The larger the load current the larger the spike when the MOSFET is off and the larger the drop when the MOSFET is on.

Figure 4.12: Voltage ripple spike due to capacitor ESR.

Table 4-3: Summary of important Flyback characteristics at different output voltages.

Nominal Vout	Load Regulation (%)	Line Regulation (%)	η (%)	ΔV_{out}
20 V	0.6	0.1	81.3	60 mV
40 V	0.65	0.03	89	38 mV
60 V	2.17	0.04	86	35 mV

Figure 4.13: Comparing efficiency (A) and output ripple (B) at different Flyback output voltages.

A summary of all the simulation test and calculations is shown in Table 4-3. Figure 4.13 shows graphical depiction of efficiency and ripple at different output voltages. As expected, the voltage ripple for 20 V at full load is the largest due to the increased current being released into the ESR of the output capacitors. Load regulation was calculated from 25% load to full load and shows that the converter has difficulties regulating at light loads, which occurs when the output voltage is set to 60 V. Table 4-4 is an example summary of the efficiency report by LTSpice showing the losses for 40 V output of the converter simulated at a full load of 500 mA. For all three efficiency simulations, the greatest power losses were dissipated by the MOSFET followed by the output diode. For the most efficient converter, these components must be high efficiency parts while still meeting the requirements of Equation 4-8 and 4-9.

Table 4-4: Efficiency report showing I_{pk} , I_{rms} , and power dissipation for each component.

Efficiency: 89.0%			
Input: 22.8W @ 170V			
Output: 20.3W @ 40.5V			
Ref.	I_{rms}	I_{peak}	Dissipation
C1	106mA	1483mA	0mW
C2	0mA	0mA	0mW
C3	0mA	0mA	0mW
C4	93mA	1093mA	0mW
C5	803mA	2074mA	10mW
D1	968mA	2864mA	450mW
L1	0mA	0mA	0mW
L2	968mA	2864mA	28mW
L3	382mA	1003mA	26mW
M2	382mA	1003mA	1219mW
R1	0mA	0mA	3mW
R2	0mA	0mA	185μW
R3	377mA	1561mA	3mW
R4	0mA	0mA	8mW
R5	0mA	0mA	130μW
R6	0mA	0mA	3μW
R7	0mA	0mA	0μW
U1	153mA	1527mA	757mW

4.4 The Two Switch Network

Figure 4.14: Schematic diagram for two switch network.

The two switch network is the last stage of the proposed system. It is responsible for creating output voltage pulses at variable pulse width and frequencies. Figure 4.14 shows the schematic of the two switch network. For simulation purposes, the LT1160 Half-Bridge Driver is used to control and drive the N-Channel power MOSFETS. The two switch network requires a 12V power supply, V1, and two control signals, V2 and V3 which drive the top and bottom gate respectively. When the voltage to the INtop pin is driven above 2V the Tgate pin is driven high, turning on the top gate NMOS M1 [32]. When the voltage to INbot pin is driven above 2V the Bgate pin is driven high, turning on the bottom gate NMOS M2. The LT1160, as well as most half bridge drivers, has internal circuitry that prevents both INtop and INbot to be logic high simultaneously [32]. If both control signals are logic high, the driver doesn't turn on either gate and no current path exists. The driver also has regulated dead time between switching cycles for added protection. An excel spreadsheet was created in order to calculate

each parameter to achieve a specific output voltage frequency and pulse width. Table 4-5 shows the control signals in order to have an output square wave of 60 Hz at 50% duty cycle. The 50% duty cycle corresponds to a pulse width of 8.33 ms.

Table 4-5: Two switch network driver control signals for desired frequency and duty cycle.

Duty Cycle (%)	50
freq (Hz)	60

TG (V2)		BG (V3)	
V1 (V)	0	V1 (V)	0
V2 (V)	8	V2 (V)	8
TD (sec)	0.000000	TD (sec)	0.008333
TR (sec)	1.67E-05	TR (sec)	1.67E-05
TF (sec)	1.67E-05	TF (sec)	1.67E-05
PW (sec)	0.008333	PW (sec)	0.008333
PER (sec)	0.016667	PER (sec)	0.016667

When the top MOSFET (M1) is on, the bottom MOSFET (M2) must be off and the only current path from the Drain of M1 is through the load. The voltage connected to the Drain of the top MOSFET is also the peak voltage of the output square wave. This voltage is referenced as Voutfly in Figure 4.14. The two switch network output voltage is shown in Figure 4.15 when control signals of Table 4-5 are applied. Figure 4.15 also shows when different values are used for Voutfly. Regardless of the voltage applied to Voutfly, the two switch network outputs a square wave with period and pulse width specified by the control voltages.

Figure 4.15: Two switch network square wave output voltage.

In order to turn on the top MOSFET, a bootstrap capacitor (C1) holds the Boost pin 12V above the voltage of the Tsource pin. The driver uses the input voltage as the potential difference between the boost pin and the Tsource pin. Figure 4.16 shows this concept. The bootstrap capacitor allows the top MOSFET to be turned on and is rated accordingly. Since the max input voltage to the IC is 20V, a 25V 1 μF capacitor was used for C1 giving a 5V safety margin. A diode, D1, is necessary to prevent the bootstrap voltage from being applied anywhere besides the Boost pin. Because the maximum output boost voltage is 92V, which occurs when the output is 80V, a diode should have be rated above this voltage. A MBR51100 diode was used for this purpose. It has a breakdown voltage of 100V which is 8V higher than the maximum boost voltage of 92V. Both MOSFETs experience a maximum V_{DS} of 80V which is our maximum output voltage. To add a significant safety margin, 200V MOSFETS were used. For best performance and efficiencies, the MOSFETS should have low R_{DSon} values. The selected MOSFETS have a maximum R_{DSon} value of 20 m Ω .

Figure 4.16: Turning on the top MOSFET requires a bootstrap capacitor holding V_{boost} at $V_{source} + V_{in}$.

4.4 Two Switch Network Simulation Results

The following section investigates how the network performs in different operating conditions. Figure 4.15 shows that the network is able to output the peak minimum and maximum requirements of the system. However, the main responsibility of the two switch network is to be able to easily adjust the period and pulse width of the output voltage. In addition, each parameter should be able to be changed individually and the variables should be independent of each other; meaning each changing one variable should not affect the other variables. How well the pulse wave is maintained at different load currents is also important to investigate.

Figure 4.17 shows how well pulse waves of different pulse widths are generated. To test this parameter, voltage was maintained at 40V and frequency was fixed at 5 kHz. The system requires a minimum of 20% duty cycle and a maximum of 80%. Therefore the simulations have duty cycles (D) of 20%, 50%, and 80%. A load resistor that draws 10% full load was also connected to show the effects of loading. Figure 4.17A shows the output voltage with D=20%. The corresponding pulse width is 40μs which is exactly 20% of 200μs. 200μs is the period of a 5 kHz signal thus showing the system responds correctly to the control signals. The same is true for Figure 4.17B and 4.15C. There are also no visible effects of loading when testing the three duty cycle values.

Figure 4.17: Effects of changing duty cycle on the output voltage of the two switch network.

The next parameter to simulate is how well the network achieves the desired frequency. For these simulations, the voltage, 40V, and the duty cycle, 50%, were held constant while changing the frequency from 60 Hz (f_{min}) to 100 kHz (f_{max}). A frequency in the middle of this large range, 5 kHz, was also simulated for comparison. Once again, a load current of 10% full load was applied to see the effects of loading. The results of the simulations are summarized in Figure 4.18. In order to see the different frequencies, each window was zoomed in to include three pulse trains. Each frequency was regulated producing the desired signal. The small delay occurs in Figure 4.18A at the beginning of the waveform.

This delay is probably due to the rise time and the high set frequency of 100 kHz. Besides this small delay, each frequency is accurate. The load current seems to have no effect on the integrity of the signal.

Figure 4.18: Frequency effects on the two switch network output voltage.

The two switch network must also be able to maintain each parameter regardless of the load current being supplied to the load. At 40V, the maximum load current is 500 mA. Figure 4.19 shows the effects of different load currents on the integrity of the output voltage. The two switch network was set to output a 5 kHz, 100µs, 40V output pulsed voltage. It was then simulated from 10%-90% full load to see if any of the parameters were significantly altered. Figure 4.19 seems to only contain one signal meaning all three are overlapping. This means frequency and pulse width are unaffected with a change of load current.

Figure 4.19: Pulse width and frequency measured against different load currents.

The peak voltage, however, was affected. More output current corresponds to a larger voltage drop across R_{DSon} of the top MOSFET. Figure 4.20 shows the voltage drop leading to a lower peak voltage of the output waveform. As mentioned before, by multiplying the load current by 20 mΩ, the R_{DSon} , the voltage drop in the simulation results is accounted for. The maximum voltage drop is only 8 mV which is insignificant compared to the nominal output voltage. Load testing was simulated for different duty cycles as shown in Figure 4.20B and 4.20C. The change in duty cycle had no effect on the voltage drop across R_{DSon} of the top MOSFET.

Figure 4.20: Effects of load current on the peak voltage of output waveform.

Overall, the simulations show that both pulse width and frequency are independently adjustable in the two switch network. Changing one parameter does not affect the other variables. In addition, each necessary output voltage was accomplished without damaging the network. Simulation results show the two switch network is able to meet all system requirements.

4.5 Overall System Implementation and Simulations

Figure 4.21: Schematic diagram of the overall system.

Implementing the overall system is done by simply connecting the cascaded stages together. The rectified AC voltage is connected to the primary side of the transformer in the Flyback converter. The output node of the Flyback converter is connected to the Drain of the top MOSFET. The grounds of the primary side of the transformer should not be connected to the grounds of the secondary side of the transformer or the grounds of the two switch network. This creates the electrical isolation from the input voltage. However, for simulation purposes it is acceptable to have a common ground. System simulations with non-ideal components give pretty accurate results and should always be referenced before advancing to real testing.

Due to extensive simulations in the previous sections, the system simulations were designed for overall checking system performance. The first simulation is the system's response to each variable set at maximum values. The duty cycle is set to 80%, the frequency is set to 100 kHz, and the voltage is set to 60V. The voltage was set to 60V instead of 80V in order to compare to other simulations in the previous section. The system is simulated for different load currents in order to see the effect of loading

on the system. The load current is initially 20% of full load and increased in increments of 20% until reaching 80% full load. It should be noted that the listed currents are I_{pk} delivered to the resistive load. Since the output voltage is a pulse wave, the current through the load will result in a pulse wave.

Figure 4.22 shows the output voltage upon startup. The soft start capacitor causes the output voltage of the Flyback to increase steadily which affects the output voltage magnitude as well. The output voltage magnitude increases to about 65V before regulating back down to 60V. The reason the graphs are a solid color is because the frequency is 100 kHz. Figure 4.22 is meant to show the soft start as well as the overall regulation. An increase in load current corresponds to smaller settling times.

Figure 4.22: Overall scope of output voltage showing rise time and settling time.

The first variable to investigate is the peak output voltage set by the Flyback converter. Figure 4.23 shows the Flyback voltage once steady state is reached. They are very similar to the results of Figure 4.10B with one important difference. Besides the ESR spike that increases as load current increases, there is also a voltage dip in the Flyback output voltage. It becomes apparent when Figure 4.23 is compared to Figure 4.24B. The large dip is the transient response of the Flyback from an increase in load current when the output voltage is high. The extra current needed to supply the load is drawn from the Flyback output capacitors causing a dip in the Flyback output voltage. Figure 4.23 also

reiterates the fact that the Flyback controller does not regulate to the proper voltage. Instead of regulating to 60.6V, the controller regulates to 61.47V. In the overall picture this is not a huge difference but it does show the importance of load regulation. In addition, user can always adjust R_{fb} to fine tune to the correct output voltage.

Figure 4.23: Close up look of the Flyback output voltage at different load currents.

Figure 4.24 shows a closer look at the output voltage. Figure 4.24A shows that the frequency of the output waveform is not affected by the load current. The control signals to the two switch network should produce a 100 kHz pulsed signal and simulation results confirmed the frequency. Figure 4.24B verifies once again the decrease in peak magnitude in reference to the output of the Flyback. The drop in voltage is due to the R_{DSon} of the top gate MOSFET. The ESR spike is also visible on the rail voltage when the output pulse is high. The duty cycle seems to measure a little bit larger for low loads in Figure 4.24B. However, this only is visible at the peak voltage and all waveforms reach zero voltage at the same time. The pulse width is unaffected by a change in load current because the output voltage pulse reaches in the correct time.

Figure 4.24: Effects of load current on output voltage magnitude and pulse width, $f = 100$ kHz.

The next simulation was under the system's minimum requirements. The duty cycle was set to 20%, the frequency was 60 Hz, and the voltage magnitude was 20V. Once again, even though the minimum voltage is 10V, better comparisons can be made to previous simulations if the voltage magnitude is 20V. The simulation shows the effect of different load current on each variable. The load current begins at 20% of full load and is increased in increments of 20% until reaching 80%.

Figure 4.25 shows the output voltage at startup. The frequency is only 60 Hz, making the output pulse visible. There is also a large spike in the output voltage at roughly 16 ms before regulating back down to the desired 20V output. The reason why is clear in the Flyback output voltage.

Figure 4.25: Effects of load current on output voltage waveform upon startup.

The waveform of the output of the Flyback converter shows why the output voltage contains a large peak. Because the frequency and duty cycle are set to the minimum, the Flyback experiences no load for an extended period of time. As explained in section 4.2, there is a minimum load requirement. If the minimum load requirement is not met, the feedback system cannot sample the output voltage resulting in the output voltage to continuously increase. Even though the 2% full load minimum load requirement is reached, the low frequency causes a large period of not loading the Flyback. The solution to the problem is connecting a load resistor across the output terminal of the Flyback in order to always meet the minimum load requirement.

Figure 4.26: Effects of different load current on Flyback output voltage.

Figure 4.27 shows the output voltage in closer detail. Once a load is applied, the Flyback begins regulating the voltage. The Flyback has a faster transient response as the load current increases. The output voltage is regulated in three of the four cases. At 20% load, the voltage is never regulated all the way back to 20V. This leads to an unstable system. Once the load current goes back to zero, the Flyback output voltage will continue to increase as shown in Figure 4.26. The voltage at 20% load never goes back to 20V meaning each period the net voltage increases. Adding the load resistor will prevent this from happening.

Figure 4.27: Effects of load current on output voltage pulse width, frequency, and magnitude.

Minimum and maximum conditions of each variable in the system have been simulated. Figure 4.28A shows results of the system producing a 20V, 5 kHz, 50% duty cycle pulse train. The Flyback voltage is superimposed to show the rise in voltage still occurs when no load current is drawn from the Flyback. Figure 4.28B shows that the rise in unregulated voltage only reaches 20.8V being regulated. This leads to 600mV ripple in the output voltage but the system is stable and operating correctly. The small rise in voltage is a factor of output frequency and pulse width. If the output pulse frequency or duty cycle is decreased, the output pulse voltage spike will increase.

Figure 4.28: Output pulse train (A) and regulation occurring when pulse is applied (B).

Overall, the simulation results show that the system produces a design able to achieve variable frequency, pulse width, and voltage magnitude. However, the system does not change each variable independently which is an issue. Changing frequency or pulse width has a direct effect on the peak voltage. Changing one parameter should not change another. In most cases the changes are miniscule however some cases lead to the voltage continuously rising. In order for the minimum Flyback controller current requirement to be met, a load resistor will be connected across the Flyback output voltage.

Chapter 5 Hardware Results

Before connecting and testing the overall system, the Flyback converter and the Two Switch Network were tested individually. The input rectifier was included in the Flyback testing. Testing and characterizing each section individually allows complete control over the tests and the ability to test specific parameters in set conditions. After each section passes the requirements, the cascaded system is connected and tests were performed to characterize the overall system.

5.1 Flyback Converter Test Setup

Figure 5.1: Block diagram for testing the Flyback converter.

Figure 5.1 shows how the Flyback converter was connected in order to test the circuit. Table 5-1 shows the equipment used for the test. The variac controls the input voltage magnitude in order to measure line regulation. The power meter gives an accurate measure of the ac input current and input power. As mentioned in section 4.2, the converter needs a 50V reference voltage in order to operate. For testing this was provided by a power supply. The electronic load easily controls the output current sourced by the converter while accurately reading the output power. However, since current is being

drawn to the electronic load, there is a significant voltage drop through the wire connectors. A separate multi-meter was connected across the output to accurately measure the voltage. An oscilloscope was used in order to capture time varying signals such as output voltage ripple and switch node voltage.

Table 5-1: Equipment used for testing Flyback converter.

Purpose	Equipment	Manufacture	Model
Controlling Vac Magnitude	Variac	Cal Poly	
Measuring Input Power	Power Meter	GSK	
50 V reference	Power Supply	GW	GPR-6060D
Measuring I _{out} , P _{out}	Electronic Load	B&K Precision	8540
Accurate V _{out} measurement	Multimeter	Agilent Technologies	U341A
Ripple Voltage, Switch Mode voltage	Oscilloscope	GW	Instek GDS-2204

Since dealing with high voltages, especially the AC outlet voltage, the proper safety measures should be taken. Before connecting the circuit, the Variac and the DC power supply were turned down to zero volts. After the proper connections were made, the electronic load was turned on and set to the required load. This ensures the converter will regulate once powered on. The 50V supply voltage was turned on and the Variac voltage was slowly increased to 120V. The proper measurements were then recorded. When powering off the Flyback converter, the Variac voltage was decreased until reaching zero. The power supply voltage was then turned off. The electronic load was left on throughout this process and finally turned off once everything else was off.

5.2 Flyback Converter Test Results

The Flyback is responsible for regulating a specified rail voltage which dictates the peak output voltage. Therefore, the Flyback was tested on if the required range of output voltages can be achieved and how well these voltages are regulated at different load currents. Another important test is the line regulation which measures how well the output voltage is regulated when changing the input voltage.

Table 5-2 once again shows what the feedback resistor, R4 in Figure 4.5, should be set at in order to set the output voltage. Another added benefit of the potentiometer is that output voltage can be set accurately by tuning the potentiometer, negating tolerances of a regular feedback resistor. Table 5-2 also shows load currents at which the converter was tested. Load regulation was tested according to Eq. 3-2, using 10% load and minimum load and 90% load as full load as specified in the table. It should be noted that the minimum load for 60 V and 80 V is less than the 40 mA current the regulator requires to regulate. As a result, the controller will regulate to a slightly higher voltage.

Table 5-2: Output voltage lookup table with associated full load currents.

Rfb (Ω)	Vout	10% load (A)	90% load (A)	Full Load (A)	Full Load (Ω)
48.2 k	10	0.2	1.8	2	5
96.0 k	20	0.1	0.9	1	20
188k	40	0.05	0.45	0.5	80
280.1k	60	0.033	0.3	0.33	182
370 k	80	0.025	0.225	0.25	320

All the voltages were checked from 10-80V while drawing 150 mA from the electronic loads. The converter was able to produce each voltage by simply adjusting the potentiometer. In order to check regulation, the output voltage was set to 20 V and loaded from 100 mA to 1 A in increments of 100 mA. The results are listed in Table 5-3. It is seen that that the output voltage slightly decreases as the output current increases. This is typical in switching regulators and is usually caused by a combination of switching losses and copper losses. Increased current corresponds to a larger voltage drop across component's series resistance such as the DCR of the transformer [35]. That is why component selection is very important to efficiency and load regulation. Efficiency was also calculated using Eq. 5-1:

$$\eta(\%) = \frac{P_{out}}{P_{in}} \times 100\% \quad (5-1)$$

Table 5-3: Efficiency data of the offline Flyback with feedback resistor set to 96 kΩ.

R _{fb} = 96 K				
I _{load} (A)	V _{out} (V)	P _{out} (W)	P _{in} (W)	η (%)
0.1	20.1	2.01	2.71	74
0.2	20.04	4.01	5.35	75
0.3	19.97	5.99	7.78	77
0.4	19.86	7.94	9.81	81
0.5	19.86	9.93	11.94	83
0.6	19.86	11.92	14.12	84
0.7	19.86	13.90	16.34	85
0.8	19.86	15.89	18.6	85
0.9	19.85	17.87	20.84	86
1	19.76	19.76	22.98	86

Input power was measured with the AC Power meter and output power was calculated by multiplying the output DC Voltage and the load current. Efficiency of the offline Flyback at different load currents is compared in Figure 5.2. As the load current increases, the offline Flyback regulates the output voltage more efficiently. At full load the offline Flyback has an efficiency of 86%. The efficiency at full load surpassed our goal of 80% which is excellent for the offline Flyback topology. Load regulation was calculated using Eq. 3-2.

$$Load\ Reg\ (\%) = \frac{20.1V - 19.85V}{20V} \times 100\% = 1.25\%$$

The load regulation of the converter also meets the requirement of 5%. This means the small change in voltage when different loads are applied is acceptable to the overall performance of the system.

Figure 5.2: Efficiency curve of Offline Flyback with feedback resistor set to 96 k Ω .

Figure 5.3: Output voltage ripple and switch node voltage of Flyback.

Figure 5.3 shows four very important voltages of the Flyback. Figure 5.3A shows the output ripple of the converter and 50% of full load. The actual ripple is very small due to the large output capacitance and low output current. However, there are large spikes that account for an output voltage ripple of 37.6 mV. At full load, the voltage ripple increases to 312 mV. The output voltage ripple should be less than 5% of the output voltage. Using Equation 5-2, the $\% \Delta V_{out}$ is calculated to be 1.56% meeting the requirement for output ripple.

$$\% \Delta V_{out} = \frac{V_{pk-ripple}}{V_{out}} \times 100\% \quad (5-2)$$

Figure 5.3B shows the reason for the large spikes. The yellow trace is the switch node, which is the drain of the MOSFET and the blue trace is the output voltage ripple. One large spike occurs when the MOSFET is turned on, causing the drain to be grounded, and another spike occurs when the MOSFET is turned off, increasing the gate voltage to $V_{in} + N \cdot V_{out}$, as in Eq. 4-8 [22]. When the MOSFET is turned on, the energy in the core is transferred to the load causing the spike [34]. When the MOSFET is turned off, the core is charging and the capacitors provide the output current. Because capacitors do not instantaneously change voltage, a large current is sourced to the load. This current surge causes the spike seen when the MOSFET is turned off. These spikes do not show in the simulations due to the transformer having perfect coupling.

Another important concept not shown in simulations is shown in Figure 5.3C. The figure shows the leakage inductance spike of the switch node voltage. This spike is why a large safety margin is necessary when selecting the MOSFET. The MOSFET must be able to withstand the spike that occurs when the switch is turned off. At 20V out and 170V_{in}, using Eq. 4-8, the theoretical voltage is:

$$20 \cdot 3 + 170 = 230V$$

Figure 5.3C shows a peak voltage of 260V before stabilizing back down to the theoretical 230 V.

Table 5-4 gives the data measurements for testing done at 40V out. One data point that stands out is the output voltage at 50 mA load current. There is one volt difference in the output voltage when an extra 50mA is applied to the load. Even though the minimum output current of 40 mA is met, the controller is regulating to a voltage slightly above the nominal. This also holds true for the simulation results (reference Figure 4.9B). However, in the simulations the voltage drop is not as large. Even at 100mA load current, the output voltage is 500mV above the nominal. The converter regulates to the nominal output voltage around 150mA load current. The load regulation was calculated using Eq. 3-2 resulting in 2.7%. The Load regulation still meets requirements, which means the change in output voltage is acceptable.

Table 5-4: Efficiency data of Offline Flyback with feedback resistor set to 186 k Ω .

R_{fb} =186k Ω				
I_{load} (A)	V_{out} (V)	P_{out} (W)	P_{in} (W)	η (%)
0.05	41.5	2.08	3.18	65
0.10	40.47	4.05	5.61	72
0.15	39.94	5.99	8.07	74
0.20	39.93	7.99	10.64	75
0.25	39.93	9.98	12.99	77
0.30	39.9	11.97	15.26	78
0.35	39.91	13.97	17.53	80
0.40	39.91	15.96	19.68	81
0.45	39.88	17.95	21.60	83
0.50	39.88	19.94	23.68	84

Figure 5.4 shows that the efficiency of the offline converter improves as the load current is increased. The converter has a relatively low efficiency of 65% at 10% load current, however the efficiency improves all the way to 84% at full load. The efficiency requirement is met when the converter is regulating 40V out. The efficiency curve also seems linear when compared to Figure 5.2. This is due to the small changes in load current from data point to data point. The output voltage ripple was measured as 143mV. Equation 5-2 calculates a $\% \Delta V_{out}$ of 0.36% which is below the requirement of the Flyback.

Figure 5.4: Efficiency curve of Offline Flyback with feedback resistor set to 186 kΩ.

The same issue that occurred at 40V occurs at 60V. Full load for high voltages is reduced due to the maximum output power of 20W. When the full load is only 330mA, 10% of full load does not meet the minimum load requirement. 33mA is only 7mA below the minimum load current so the converter will regulate, but it will regulate to a slightly higher voltage. The data in Table 5-5 show that the converter regulated to 64 V, 4V above the nominal. Since the load steps are also small, the converter does not fully regulate until 40% load current, 132 mA. The same is seen from the simulation results

(refer Figure 4.10B). The calculated load regulation using Eq. 3-2 gives 6.05% which does not meet the requirement of 5%. The output voltage ripple was measured at 85mV and the calculated $\% \Delta V_{out}$ is 0.14%.

Table 5-5: Efficiency data of Offline Flyback for feedback resistor set to 280 k Ω .

Rfb = 280.1k				
Iload (A)	Vout (V)	Pout (W)	Pin (W)	η (%)
0.033	64	2.11	3.28	64
0.067	62.45	4.18	6.05	69
0.1	61.21	6.12	8.50	72
0.132	60.45	7.98	10.89	73
0.165	60.42	9.97	13.54	74
0.2	60.41	12.08	16.10	75
0.231	60.38	13.95	18.50	75
0.264	60.38	15.94	20.73	77
0.297	60.37	17.93	22.97	78
0.33	60.37	19.92	25.43	78

The efficiency curve shown in Figure 5.5 is also linear due to a small step in load current. If tested at higher currents, the efficiency is expected to continue to increase. However, the 78% efficiency at full load meets the 75% goal of the Flyback converter. Looking at Figure 5.6, it is clear that the efficiencies decline at higher output voltage levels due to the low load currents.

Figure 5.5: Efficiency curve of Offline Flyback with feedback resistor set to 280 kΩ.

Figure 5.6: Comparing efficiency curves of Offline Flyback at different output voltages.

Line efficiency was then measured by seeing how the output voltage of the converter reacted to a change in the input voltage. The measurements were made while full load was applied to the converter. Table 5-6 shows the results of the test at the specified voltage.

Table 5-6: Summary of line regulation data for different output data.

	$R_{fb} = 96 \text{ k}\Omega$	$R_{fb} = 186 \text{ k}\Omega$	$R_{fb} = 280 \text{ k}\Omega$
$V_{in} (V_{rms})$	$V_{out} (V)$	$V_{out} (V)$	$V_{out} (V)$
114	19.82	39.87	60.34
120	19.85	39.88	60.37
126	19.85	39.89	60.38

Figure 5.7 graphs the results and shows the converter regulates the converter output to within 40mV regardless of the line voltage. The change in output voltage is unnoticeable when compared to the output voltage. Equation 3-1 was used to calculate the line regulation of each output voltage and the results are listed in Table 5-7.

Figure 5.7: Line regulation at different output voltages.

Table 5-7: Summary of test results for offline converter at different feedback resistor values.

R_{fb}	Load Reg (%)	Line Reg(%)	Full Load η (%)	ΔV_{out} at full load
96 k Ω	1.25	0.15	86	312 mV
186 k Ω	2.7	0.05	84	143 mV
280 k Ω	6.05	0.07	78	85 mV

Table 5.7 summarizes the test results of the Flyback and Figure 5.8 shows them measured against the simulation data. As expected the simulations produced better regulation for each parameter. However, the hardware also performed well. The line regulation meets the requirement of 5% regulation. The maximum line regulation of the converter is 0.15% which occurs when the output voltage is 20V. The efficiencies at full load meet the 75% requirement for each output voltage. The output voltage ripple is also well within the 5% tolerance for each output voltage. The hardware tests conclude that the Flyback converter is able to produce the full range of output voltages in the design requirements. Furthermore, the converter will regulate the output voltage throughout the full range of possible input voltages. The converter is able to regulate the output voltage within the load regulation requirements when the minimum current is above 40mA. However, at 60V the load regulation was measured slightly above the maximum value of 5%. Note that adding a resistor across the load before system testing will ensure the minimum load current condition is met per chip requirements. The constant load current will increase the load regulation of the system.

Figure 5.8: Comparing Hardware and Simulation results for measured characteristics of Flyback.

5.3 Two Switch Network Test Setup

Figure 5.9: Block diagram for testing the two switch network.

Figure 5.9 shows how the Two Switch Network was connected in order to test the circuit.

Testing this stage is not as involved as testing the Flyback converter. Table 5-8 lists the equipment used to test the circuit. The 12V IC power supply was applied to turn on the gate driver. The high voltage DC power supply was set at to 0V and applied to the drain of the top MOSFET (Reference Voutfly of Figure 4.13). The load resistor was not connected in order to verify the circuit works under no load conditions. Before connecting the control signal, it was connected to the oscilloscope to verify the signal. Once verified, the control signal was applied to the network. A 10:1 scope probe was connected across the output terminal in order to accurately measure the output voltage waveform. The DC rail voltage was then increased to the test voltage. The proper variable load resistance was connected to the system for testing.

Table 5-8: Equipment used for testing the Two Switch Network.

Purpose	Equipment	Manufacture	Model
Simulate Flyback output voltage	Power Supply (80V)	GW	GPR-6060D
Gate Driver power supply	Power Supply	Agilent	E3640A
Control signals	Pulse Generator	BK Precision	4033
Simulate algae load	Power Potentiometer (20 W)	Cal Poly	
Measure output Voltage waveform	Oscilloscope	GW	Instek GDS-2204

5.4 Two Switch Network Test Results

The two switch network was tested to see how well it produces the desired pulse waveforms for a given input voltage. The network was tested on how well it produces a variable frequency pulse waveform as well as how well it adjusts the pulse width of a given frequency. The network was also tested on how well it maintains these variables under different loading conditions and voltages. The full

load currents are the same as in the previous sections. For testing the two switch network, percentages of full load are in reference to peak current, current delivered to load when output voltage is high.

The gate driver used for the hardware design was International Rectifier's IR2111 Half Bridge Gate Driver. The IC has the same parameters and functionality as the LT1160. The difference between the IC's is that the IR2111 only has one control input signal. The input control signal drives the top MOSFET. Internal circuitry of the IR2111 inverts the control signal and applies it to the bottom gate [35]. Dead time is also added to the control signal ensuring the two gates are never on at the same time, just as in the LT1160.

The first parameter tested was the network's ability produce a given pulse width at a set frequency and input voltage. Figure 5.10 shows the test results when the rail voltage was 20V, the frequency was set to 5kHz, and a 100Ω resistor was used for loading. Channel 1 (yellow trace) indicates the output voltage while channel 2 (green trace) is the control signal. The control signal was then adjusted to produce pulse widths of 20%, 50%, and 80% of the period (200us). According to the system specifications these are the 20% and 80% are the minimum and maximum duty cycles required. Figure 5.10 shows the results for each duty cycle. The oscilloscope was set to measure the resulting frequency, peak voltage, and duty cycle of the output voltage. The results show that each duty cycle was able to be produced within 0.02% of the nominal. The same procedure was repeated while changing the rail voltage to 40V and 60V. Regardless of the change in input voltage, the network was able to accurately produce the full range of pulse widths.

Figure 5.10: The two switch network regulation of frequency with 10% load current applied.

The next step was to test the network's ability to maintain the pulse width under different loading conditions. The frequency remained constant at 5 kHz and the input voltage was set to 20V. Each duty cycle was tested under the different load conditions and the pulse width was measured at each one. The load current was set by adjusting the power resistor. Table 5-9 summarized the measured pulse width under each condition. The biggest pulse width change occurs when the duty cycle is set at 80%. The pulse width changes 7us from 10% load to 90% load. Figure 5.10 is a graphical depiction of the data.

Table 5-9: Pulse width measurements when different load currents applied.

PULSE WIDTH		% Full Load (1A)		
		10%	50%	90%
	20	40.2 μ s	40 μ s	39.9 μ s
D (%)	50	100.1 μ s	99.9 μ s	99.6 μ s
	80	163 μ s	159.9 μ s	156 μ s

Inputs
f = 5 kHz
T = 200 μ s
V _{out} = 20V

Figure 5.11: Two Switch Network's regulation of Pulse Width at different load currents.

The two switch network was then tested to see how well it produces a pulse at a specified frequency. More specifically, tests were done at the minimum (60Hz) and maximum (100kHz) frequencies required by the system. 5 kHz was also tested to represent a frequency in between. The power resistor was adjusted to apply loading to the network. The results are shown in Figure 5.11 for an input voltage of 22V. The system was able to produce each frequency fairly accurately. Once again the output voltage is channel one and the control signal is channel two. The most interesting waveform is

the high frequency waveform of Figure 5.12. Peaking occurs at the beginning of each pulse and the duty cycle is significantly less than the nominal 50%. This delay is due to the built in dead time which only affects the output waveform at high frequencies [35].

Figure 5.12: Comparing output frequency to control signal while 10% load current applied.

Efficiency tests were also performed on the two switch network. For the first test, called maximum case, each testing variable was set to testing the maximum. Voltage was set to 60V, frequency was 100 kHz, and duty cycle was 80%. The minimum case was the exact opposite; Vout was

set to 20V, frequency to 60 Hz, and duty cycle was set to 20%. Efficiency tests were done on each case as well as a median case where output voltage was 40V, frequency was 5 kHz, and duty cycle was 50%.

Tables 5-10, 5-11, and 5-12 show the data for each case. The efficiency of the network was nearly perfect. Output power of the network was calculated by Equation 5-3 because of the pulse wave output.

$$P_{out} = \frac{(V_{pk} * \sqrt{D})^2}{R} [W] \quad (5-3)$$

The efficiency curves were then compared in Figure 5.12.

Table 5-10: Two Switch Network efficiency data and specified conditions for Maximum case.

V=60V	D=80%	f= 100 kHz	I_{full load}	0.33		
I_{load} (%)	R_{load} (Ω)	V_{pk out} (V)	P_{out} (W)	V_{in} (V)	P_{in} (W)	η (%)
20	912	59.97	3.15	60	3.16	99.90
40	457	59.97	6.30	60	6.30	99.90
60	303	59.96	9.48	60	9.49	99.87
80	225	59.96	12.77	60	12.79	99.87

Table 5-11: Two Switch Network efficiency data and specified conditions for Minimum case.

V=20V	D=20%	f= 60 Hz	I_{full load}	1.00		
I_{load} (%)	R_{load} (Ω)	V_{pk out} (V)	P_{out} (W)	V_{in} (V)	P_{in} (W)	η (%)
20	100	19.96	0.80	20	0.8	99.60
40	50	19.96	1.59	20	1.6	99.55
60	33	19.96	2.39	20	2.4	99.55
80	25	19.94	3.18	20	3.2	99.40

Table 5-12: Two Switch Network efficiency data and specified conditions for Median case.

V=40V	D=50%	f= 5 kHz	I_{full load}	0.50		
I_{load} (%)	R_{load} (Ω)	V_{pk out} (V)	P_{out} (W)	V_{in} (V)	P_{in} (W)	η (%)
20	403	39.98	1.98	40	1.98	99.90
40	202	39.98	3.95	40	3.96	99.90
60	133	39.98	5.99	40	6.00	99.90
80	100	39.97	7.99	40	8.00	99.85

When comparing the efficiency curves of Figure 5.13, the efficiency of the two switch network decreases when the average load current is increased. The main component contributing to the power loss is the R_{DSon} of the top gate MOSFET. As the current to the load is increased the power dissipated in the MOSFET increases. Having a MOSFET with low R_{DSon} is therefore important to achieving high efficiencies.

Figure 5.13: Efficiency curves of the Two Switch Network under specified conditions.

Overall, the two switch network meets all requirements. All frequency ranges were achieved as well as having variable pulse width for each frequency. In addition, each variable was easily changed by setting the correct input control signal. The biggest difficulties came at high frequency testing. Some peaking occurred on the output voltage and the pulse width was slightly smaller than expected.

5.5 Overall System Performance Results

Figure 5.14: Block diagram for testing the entire system.

After the Flyback controller and the two switch network passed the required tests, they were connected together by connecting the output of the Flyback to the Drain of the top MOSFET and the isolated ground output of the Flyback to the ground of the two switch network. In order to ensure the minimum load requirement of the Flyback is always met, a 5k Ω potentiometer was connected across the output voltage of the Flyback. By adjusting this potentiometer, 40 mA will be drawn from the Flyback causing better regulation of the rail voltage.

Figure 5.14 shows how the system was set up for testing. The same equipment was used as in the previous sections. There was no longer a need for the electronic load, the multi-meter, or the high voltage power supply. The Flyback was the first components to be powered up following the same steps as in section 5.2. The Flyback output voltage was then adjusted to the desired voltage before the turning on the 12V power supply. After checking the control signal, the Flyback was applied to the two switch network which created a pulsed output voltage. Figure 5.15 shows two of the output voltage waveforms under minimum and maximum voltage and frequency conditions. Some peaking occurred

on the output at high frequencies but it only resulted in a 4V increase. Overall each variable was able to produce the required values and the system was able to produce a pulsed output voltage.

Figure 5.15: Output waveforms under Maximum (A) and Minimum (B) case conditions.

The next step was to measure overall system efficiency. The maximum case and minimum case were once again tested. The results are listed in Table 5-13 and Table 5-14. Efficiency curves of each case were then put into graphs and compared in Figure 5.17.

Table 5-13: Overall system test data when applying maximum test conditions.

V=60V	D=80%	f= 100 kHz	I _{full load}	330 mA	
I _{load} (%)	R _{load} (Ω)	V _{pk out} (V)	P _{out} (W)	P _{in} (W)	η (%)
20	912.00	60	3.16	6.447	49
40	457.00	60	6.30	11.053	57
60	303.40	60	9.49	15.31	62
80	225.23	60	12.79	19.98	64

Table 5-14: Overall system test data when applying minimum test conditions.

V=20V	D=20%	f= 60 Hz	I _{full load}	1.000	
I _{load} (%)	R _{load} (Ω)	V _{pk out} (V)	P _{out} (W)	P _{in} (W)	η (%)
20	100.00	20	0.80	1.72	47
40	50.00	20	1.60	2.857	56
60	33.33	20	2.40	3.67	65
80	25.00	20	3.20	4.55	70

Figure 5.17 shows the efficiency curves of the two cases compared. They seem to both be fairly close to each other with both increasing as the load current increases. Compared to the efficiencies of the individual system, the efficiencies are much lower than the expected value. The biggest factor contributing to reduced efficiencies is the resistor placed across the output voltage. The system sacrifices efficiency in order to regulate the peak voltage, which is key for creating an accurate pulsed output voltage. In addition, the really low system efficiencies occur at low current. Referring to Table 5 13, the input power at 20% load is only 6.45 W. Since the load resistor is set to sink 40mA, the resistor across the output of the Flyback is consuming 2.4 W. This leads to low efficiency ratings because the input power is only 6.45 W. However, looking at the ideal application of the system, algae lysing can potentially be accomplished with only 6.45 W input power.

Figure 5.16: Efficiency curve of system under Minimum and Maximum conditions.

The testing concludes that the system as a whole meets all requirements. The system is able to produce a controllable pulsed output voltage. The system is also able to create a pulse output voltage, where the voltage amplitude and frequency can easily and independently be adjusted. For a given frequency, the pulse width of the signal may also be varied. An important characteristic of the system is that each variable does not affect the set parameters of the other variable. Finally, the system maintains the integrity of the output voltage regardless of the load which is important for pulsed electric field applications.

Chapter 6 Conclusions

The objective of this thesis was to develop a system that provides the flexibility in finding the optimum operating conditions for lysing algae. The system consists of power converters that should provide a pulse output voltage in order to create a pulsed electric field (PEF) to lyse algae. The proposed system is unique from any known PEF systems because it provides the ability to independently adjust peak voltage, pulse width and frequency of the output voltage. This in turn provides great flexibility in determining optimum pulse voltage at various operating conditions for lysing algae.

Due to the fact that algae lysing is a new technology, the ability of each variable to accomplish a large range is necessary. Therein lies the most difficult aspect of the project, the design has no set values to base a design on. However, to demonstrate that the proposed system provides a solution for algae lysing, certain design parameters were set. When matched against these design goals, the proposed system was able to meet most of the requirements. The only parameter that could have improved was the load regulation at low load currents. Overall, simulation and hardware results demonstrate that the proposed new system can indeed produce pulse output voltages with adjustable voltage, pulse width and frequency.

Some of the issues encountered involved selecting components that met the wide range of output conditions. Although the Flyback offers great flexibility, simplicity, as well as isolation, it has some major drawbacks. One common issue with Flyback is that it is prone to leakage spike which may cause voltage across the main MOSFET to well exceed its theoretical value. Hence, enough safety margin between the theoretical maximum switch node voltage and the V_{DS} of the selected MOSFET should be provided so that the MOSFET can withstand the extra leakage inductance spike. One suggestion for future improvement would be to use a different topology that is immune to leakage spike. One good candidate as an example is the Double-Ended Forward converter. Another issue came from the fact that

the chosen Flyback IC has a minimum load requirement which made it difficult to regulate the output voltage when the output impedance was high. It is therefore recommended that for future improvement, a Flyback controller that does not require a minimum load be used for the proposed system. For this project, the problem with minimum load requirement was resolved by placing a resistor to the output of the Flyback to draw the minimum current. The addition of the resistor fixed the regulation problem but decreased the efficiency of the overall system. Another suggestion for future improvement would be to make the entire system operate from a single AC Input voltage rather than using multiple power supplies. For the current system, two additional external power supplies were used to power the driver IC and to provide the 50V reference voltage for the Flyback controller. Creating controller circuits to provide these power requirements from the 120 Vac input voltage would make the system less complicated and easier to use. Another idea for improvement is to implement a microprocessor for the control signal which may further enable users to interface the proposed system with a computer.

Overall, the project was a great learning experience. Designing a cascaded system and a system solution to a real world problem made the design very challenging. Designing the system required attention to details and the wide range of operation required not overlooking any design parameters. The system successfully demonstrates that the proposed topology works and is able to adjust each variable individually and independently.

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