SDC6: High-Efficiency Power Amplifier (HEPA)

by

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Abstract

The project includes design and fabrication of a high efficiency power amplifier for a student design competition held at International Microwave Symposium (IMS) 2023. Efficient power amplifiers are critical for base station communication requiring efficient use of available power. The final design optimizes power added efficiency (PAE) and linearity. The amplifier will operate at 2.45 GHz. Competitive PAE above 50%, and C/I above 30 dB is achieved by leveraging a Doherty class amplifier using accurate discrete CGH4006P transistor models to simulate an efficient and linear design. Unique design features include optimal transistor bias point selection and power split ratios between the auxiliary and main amplifiers. Equipment required for the project includes access to ADS software for design, a drill press, a tap and die set, and soldering equipment to manufacture the amplifier. Additionally, access to a vector network analyzer, spectrum analyzer, RF power meter, and frequency synthesizer is critical for the testing of the project. Materials required include GaN HEMTs, Rogers laminate blanks, and passive surface mount components.

Project Overview

IMS was held from June 11 - 16, 2023 at the San Diego Convention Center. It is a yearly in-person conference dedicated to RF, microwave and mm systems and applications. There are opportunities for teams of students from various undergraduate and graduate programs to compete in a student design competition (SDC). SDC6 is the formal name of the competition where students are challenged to design a high efficiency power amplifier (HEPA).

Competition Description and Rules for SDC6 2023

The nineteenth High Efficiency Power Amplifier (HEPA) Student Design Competition (SDC) will take place at the 2023 IEEEMTT-S International Microwave Symposium (IMS) in San Diego, California, on Tuesday, June 13, 2023. This competition is open to all students, both undergraduate and graduate, registered at a recognized educational establishment. This year’s contest will focus on PAs having both high efficiency and linearity over a relatively broad frequency band. The competitors are required to design, construct, and measure a highly efficient, linear PA at a frequency of their choice between 1 GHz and 10 GHz. To qualify for the linearity test, the PA must produce an output power of at least 4 watts, but no more than 40 watts, when excited by a single carrier at the frequency of the test. All linearity testing will be conducted using two equal amplitude carriers spaced 20 MHz apart. To qualify for the linearity measurement, with 0 dBm per tone input, carrier-to-intermodulation ratio (C/I) must be greater than 30 dB*. The winner will be the PA that demonstrates the highest power added efficiency (PAE) when producing a two-tone carrier-to-intermodulation ratio (C/I) of 30 dB* weighted for the frequency of operation [2].
**Definitions:**

**Output power:** The RF power delivered by the amplifier to the load. Target output power for the design is at least 4 W (36dBm).

**Signal gain:** Ratio of output to input power of the amplifier. This design shall achieve a gain between 12 dB and 22 dB.

**Linearity:** Measure of amplifier’s ability to linearly scale an input signal without introducing harmonics, intermodular distortion, and other nonlinear effects.

**Power Added Efficiency (PAE):** Figure of merit to quantify efficiency of conversion of DC power to RF signal amplification.

\[ PAE = \frac{P_{RF_{out}} - P_{RF_{IN}}}{P_{DC}} \times 100\% \]

Our Design is aiming for a PAE of over 65%.

**P1dB:** Output power at which the gain decreases 1 dB from its small signal value. The system operates at the edge of saturation to increase efficiency. Therefore, P1dB values for this system are in the range of 37 dBm to 41 dBm.

**Single Tone Test:** A single carrier tone is applied to the RF input port to measure PAE and P1dB.

**Two Tone Test:** Two equal amplitude carriers spaced closely together (20 MHz) centered around the device's center frequency is applied to the RF input port to test device linearity. Typically, the 3\(^{rd}\) order intermodulation product magnitude is the figure of merit for linearity measurements.

**Carrier to Intermodulation Ratio (C/I):** Figure of merit for amplifier linearity. C/I is the ratio between carrier and 3\(^{rd}\) order intermodulation product magnitude during the two-tone test. Our design is aiming for a C/I of over 30 dB up until the maximum input power of 24 dBm.

\[ (C/I)_{dB} = 10 \log_{10} \left( \frac{P_{out}}{P_{IMD,3r}} \right) = (P_{out})_{dBm} - (P_{IMD,3rd})_{dBm} \]
**Customer Requirements and Engineering Specifications.**

Engineering specifications are derived from customer requirements. Customer requirements are the rules of the IMS student design competition. Major risks associated with this project include meeting the targets for linearity (E6) and PAE (E7) while maintaining amplifier input power (E5) and output power (E4) within the test range.

**Table 1 - Customer Requirements**

<table>
<thead>
<tr>
<th>ID</th>
<th>Customer Requirement</th>
<th>Engineering Specs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>RF Ports</td>
<td>E1</td>
<td>The PA mechanical design should allow for internal inspection of all relevant components and circuit elements. The RF ports should be SMA female connectors. Bias connections should be banana plugs.</td>
</tr>
<tr>
<td>C2</td>
<td>Bias connections</td>
<td>E2</td>
<td>The PA should require a maximum of two DC power supplies for biasing</td>
</tr>
<tr>
<td>C3</td>
<td>Frequency Range</td>
<td>E3</td>
<td>The PA must operate at a frequency in the range of 1 GHz to 10 GHz and have an output power level when excited by a single carrier of at least 4 W, but no more than 40 W at the test frequency.</td>
</tr>
<tr>
<td>C4</td>
<td>Output Power</td>
<td>E4</td>
<td>PA output power should reach a minimum of 36 dBm</td>
</tr>
<tr>
<td>C5</td>
<td>Input Power</td>
<td>E5</td>
<td>All PAs should require less than 24 dBm of input power to reach the minimum 36 dBm output power when excited with a single carrier.</td>
</tr>
<tr>
<td>C6</td>
<td>Testing</td>
<td>E6</td>
<td>All linearity measurements are performed under CW two-tone operation with two equal amplitude carriers spaced 20 MHz apart at room ambient conditions into a 50Ω load.</td>
</tr>
<tr>
<td>C7</td>
<td>Criteria for judging</td>
<td>E7</td>
<td>The amplifier’s PAE measured during official testing at the lowest power level for which the C/I ratio* equals 30 dB is used for the figure of merit scoring. If the C/I ratio is better than 30 dB over the entire testing range, the measurement at 21 dBm input power per tone is used. The figure of merit for scoring is $\text{PAE} \times (f_{\text{GHz}})^{0.25}$.</td>
</tr>
</tbody>
</table>
Table 2 - Engineering Specifications

<table>
<thead>
<tr>
<th>Engineering Spec</th>
<th>Description</th>
<th>Target [units]</th>
<th>Risk</th>
</tr>
</thead>
<tbody>
<tr>
<td>E1</td>
<td>RF Layout shall use SMA Female connectors</td>
<td>N/A</td>
<td>none</td>
</tr>
<tr>
<td>E2</td>
<td>External DC bias provided through banana plugs</td>
<td>N/A</td>
<td>none</td>
</tr>
<tr>
<td>E3</td>
<td>Frequency Range</td>
<td>1-10 GHz</td>
<td>low</td>
</tr>
<tr>
<td>E4</td>
<td>Output Power Range</td>
<td>36-46 dBm</td>
<td>medium</td>
</tr>
<tr>
<td>E5</td>
<td>Max Input Power</td>
<td>24 dBm</td>
<td>low</td>
</tr>
<tr>
<td>E6</td>
<td>Linearity (C/I ratio)</td>
<td>&gt; 30 dB</td>
<td>high</td>
</tr>
<tr>
<td>E7</td>
<td>PAE</td>
<td>65%</td>
<td>high</td>
</tr>
<tr>
<td>E8</td>
<td>Gain</td>
<td>&gt; 12 dB</td>
<td>low</td>
</tr>
</tbody>
</table>
Previous Winners

The amplifier is designed to compete in the 19th HEPA competition held at IMS 2023 in San Diego CA. Previous winning designs, including transistor technology, amplifier class, operating frequency, PAE, and FoM are listed below in Tables 3 and 4. Almost all winning groups have used Gallium Nitride high electron mobility transistors. Recent winners have used the Doherty architecture. Other classes with high success rates include F, inverse F, and J type structures. A large portion of recent contest winners have operated at 3.5 GHz while no amplifier operating over 5.35 GHz has succeeded in winning the competition.

Table 3 - IMS High Efficiency PA Winners 2006-2014, from [10]

<table>
<thead>
<tr>
<th>Year</th>
<th>Device</th>
<th>Class</th>
<th>Freq (GHz)</th>
<th>PAE (%)</th>
<th>FoM</th>
</tr>
</thead>
<tbody>
<tr>
<td>2018</td>
<td>GaN HEMT</td>
<td>Doherty</td>
<td>5.350</td>
<td>49.5</td>
<td>75.2</td>
</tr>
<tr>
<td>2013</td>
<td>GaN HEMT</td>
<td>Doherty</td>
<td>3.5</td>
<td>62.5</td>
<td>85.5</td>
</tr>
<tr>
<td>2012</td>
<td>GaN HEMT</td>
<td>Doherty</td>
<td>3.5</td>
<td>59.0</td>
<td>80.7</td>
</tr>
<tr>
<td>2011</td>
<td>GaN HEMT</td>
<td>F</td>
<td>3.5</td>
<td>80.1</td>
<td>109.2</td>
</tr>
<tr>
<td>2010</td>
<td>GaN HEMT</td>
<td>J</td>
<td>3.5</td>
<td>74.7</td>
<td>102.1</td>
</tr>
<tr>
<td>2009</td>
<td>GaN HEMT</td>
<td>F¹</td>
<td>3.3</td>
<td>71.1</td>
<td>95.6</td>
</tr>
<tr>
<td>2008</td>
<td>GaN HEMT</td>
<td>F¹</td>
<td>3.2</td>
<td>71.9</td>
<td>96.1</td>
</tr>
<tr>
<td>2007</td>
<td>GaN HEMT</td>
<td>F</td>
<td>1.2</td>
<td>82.9</td>
<td>87.0</td>
</tr>
<tr>
<td>2006</td>
<td>Si LDMOS</td>
<td>F¹</td>
<td>1.0</td>
<td>75.9</td>
<td>75.9</td>
</tr>
</tbody>
</table>

Table 4 - Recent IMS High Efficiency PA Winners

<table>
<thead>
<tr>
<th>Year</th>
<th>Device</th>
<th>Class</th>
<th>Freq (GHz)</th>
<th>PAE (%)</th>
<th>FoM</th>
</tr>
</thead>
<tbody>
<tr>
<td>2020 [12]</td>
<td>GaN</td>
<td>Doherty</td>
<td>3.475</td>
<td>64.2</td>
<td>87.6 (sim)</td>
</tr>
</tbody>
</table>
Transistor Technology and Selection

Factors that influence transistor technology selection include cost, power, and frequency limitations. *Figure 1* shows optimum transistor technologies for specific power and frequency ranges. Our project requires 4W - 40W of output power in the 1 GHz to 10 GHz range. GaN HEMT devices are favorable for applications operating at both high power (3 - 300 W) and high frequency (2 - 60 GHz). Typically, a Si substrate will be less expensive than SiC at the cost of a decrease in efficiency at output powers above 100 W [4]. Due to cost, operating frequency, and power handling capability GaN HEMT on a Si substrate was selected. Other considerations include ADS model availability.

![Figure 1 - A process technology comparison of microwave frequency range power electronics [8]](image-url)
Figure 2 – PAE, Gain, and Output Power vs. Input Power of GaN HEMT [9]

### Table 5 - GaN on SiC HEMTs

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CGH40006P</td>
<td>6</td>
<td>65%</td>
<td>&gt;11</td>
<td>0 - 6.0</td>
</tr>
<tr>
<td>CMPA0530002S</td>
<td>2</td>
<td>52%</td>
<td>18</td>
<td>0.5 – 3.0</td>
</tr>
<tr>
<td>CG2H40010P</td>
<td>10</td>
<td>65%</td>
<td>&gt;16</td>
<td>0 – 6.0</td>
</tr>
<tr>
<td>TGF2933</td>
<td>7</td>
<td>57%</td>
<td>15</td>
<td>0 - 25.0</td>
</tr>
<tr>
<td>T2G6000528-Q3</td>
<td>10</td>
<td>53%</td>
<td>17</td>
<td>0 - 6.0</td>
</tr>
</tbody>
</table>

The 10 W transistors have insufficient gain to operate at peak efficiency given that the maximum input power is 21 dBm. The 2 W option is also not viable due to the low drain efficiency and low output power. The 6 W transistor, CGH40006P is the best option due to the high drain efficiency, and it nears saturation at 21 dBm input power. Additionally, we have obtained access to the Wolfspeed RF portal which contains large signal ADS models for the CGH40006P transistor. Large signal transistor models such as the ones provided by Wolfspeed are necessary for this project since the transistors are simulated at higher input powers to capture behavior that cannot be predicted by small signal S-parameters. Table 5 shows tradeoffs between transistor choices.
**Amplifier Classes**

An amplifier class is defined by how the transistor is biased, determined by the quiescent point. In Figure 3 the drain current is on the vertical axis, as the drain current moves along the load line it can be seen that the class A amplifier conducts for the entire cycle of the input signal. Class AB and B amplifiers conduct only partially during the positive half cycle of the input, Class C amplifiers only conduct in the positive half cycle of the input. Conducting during a partial cycle increases amplifier efficiency but distorts the signal. The signal can be recovered through filtering.

**Table 6 – Amplifier Class Efficiency**

<table>
<thead>
<tr>
<th>Power Amplifier Class</th>
<th>Class A</th>
<th>Class AB</th>
<th>Class B</th>
<th>Class C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Theoretical Drain Efficiency</td>
<td>50%</td>
<td>78.5%</td>
<td>50-78.5%</td>
<td>100%</td>
</tr>
</tbody>
</table>

![Figure 3 – Amplifier Classes](image-url)
**Doherty Architecture**

For a typical single transistor Class AB amplifier, peak efficiency happens at a single input power. Such a device is at a disadvantage because it is unable to operate at peak efficiency at multiple output powers. The Doherty Power Amplifier was originally designed for AM tube transmitters. The Doherty PA maintains high efficiency when backed off from peak efficiency and minimizes distortion across all input powers. In the low power region of a Doherty PA Figure 4, Main is ON and operates inefficiently and linearly (Class A only); Aux is OFF. In the Doherty region, Main is operating at high efficiency. Aux is also ON and delivers power to the load preventing Main from saturating. Beyond the Doherty region, both amplifiers saturate significantly until peak efficiency is achieved.

![Figure 4 – Theoretical Drain Efficiency Behavior [3]](image-url)

Figure 4 – Theoretical Drain Efficiency Behavior [3]
Load Modulation in a Doherty Amplifier

In a Doherty Power Amplifier (DPA) the auxiliary amplifier modulates the load seen by the main amplifier forcing it to operate at maximum efficiency for a range of power levels (Doherty region). As the main amplifier saturates, the auxiliary turns on. This effectively increases the impedance ($R_{\text{main}}$) seen by the main amplifier. As input power to the main amplifier increases, the load resistance seen at its output increases which keeps the device operating near saturation. To maintain a constant voltage swing across the load ($Z_L$) an Impedance Inverting Network (IIN) – a quarter-wave transformer – is required\(^1\). For constructive recombination of the aux and main signals at the load, the auxiliary amplifier must be $90^\circ$ out of phase with the main amplifier (see Figure 5).

![Figure 5 – Typical DPA configuration][1]

Design

Design Overview

A closed form bias conditions solution was attempted for two identical devices [3]; the relevant equations are in Appendix A. Closed form solutions resulted in -9V gate bias and $Z_L$ values that conflict with datasheet recommendations. However, the analysis showed optimal performance requires unequal input power to each transistor, and insight on how to choose biasing conditions, and load impedance to achieve a Doherty region. The final load impedance was chosen based on datasheet recommendations, biasing was chosen by testing different bias conditions while sweeping input power. A complete ADS system model with ideal components was created based on optimized bias points and optimal load impedances. The input side of the amplifier is an ideal quadrature splitter with a tunable split ratio. The matching networks and output combiner are defined as ideal transmission lines. Ideal DC and AC coupling components were used to bias the model without affecting behavior.

---

\(^1\) See original Doherty Amplifier paper [1]
Impedance Inverting Network (IIN) in a Doherty Amplifier

To maintain high efficiency as input power increases, the DUT must maintain constant maximum voltage swing across the load (V_{DD} to V_{Knee}) as the load current increases. An IIN maintains constant current (I_1 in figure 6) independent of load impedance. This creates a voltage controlled current source (VCCS) defined in (1.2). The ABCD parameters for a microstrip quarter wave transformer is defined in (1.1).

\[
\begin{bmatrix}
V_M \\
I_M
\end{bmatrix} = \begin{bmatrix}
0 & jZ_o \\
jZ_o & 0
\end{bmatrix} \begin{bmatrix}
V_L \\
I_1
\end{bmatrix}
\]  
(1.1)

Solving for \( I_1 \):

\[I_1 = -\frac{jV_M}{Z_o} \]  
(1.2)

The main amplifier load resistance when the auxiliary amplifier is off:

\[R_{main} = \frac{Z_o^2}{Z_{L\_main}} \mid I_A = 0 A \]  
(1.3)

In a Doherty amplifier when the main amplifier enters the saturation region, the IIN output current \( I_1 \) becomes fixed\(^2\). As the auxiliary amplifier turns on, current through the load (Z_L) increases. This causes the value seen by the main amplifier to increase to:

\[Z_{L\_main} = Z_L \left(1 + \frac{I_A}{I_1}\right) \]  
(1.4)

\(^2\) As the DPA passes the break point entering the medium power region, the main amplifier is saturated with its output approaching maximum voltage swing of \(V_{DD} - V_{Knee}\)
This increase causes the main amplifier’s seen resistance \( R_{main} \) to decrease (eq. 1.5).

\[
R_{main} = \frac{Z_0^2}{Z_L(1 + \frac{I_A}{I_I})}
\]  

(1.5)

This allows the designer to maintain Doherty region operation by selecting values of \( Z_0 \) and \( Z_L \) that maintain maximum voltage swing with an increasing output current. Maximum efficiency over a wider input power range can be obtained by maintaining constant voltage swing while increasing load current provided by the auxiliary.

**Load Pull**

Load pull simulations calculate PAE, gain, and transistor linearity vs. load impedance with a constant source impedance. In a load pull simulation, the source impedance is fixed while the load impedance is swept. PAE and gain were calculated for a single tone input. Transistor linearity was assessed for an equal power two-tone input with a 10 MHz offset centered at 2.45 GHz. The 2\(^{nd}\) and 3\(^{rd}\) harmonics were shorted to ground (0.1 Ω) for load pull simulation. In our final design we plan to include 2\(^{nd}\) and 3\(^{rd}\) harmonic shorts in the output matching network for both transistors. The source impedance was set to the datasheet recommended value, \( Z_s = 4.78 + j1.78 \Omega \). This value was later verified using a source pull simulation. Using a single tone load pull simulation, it was verified that a load impedance of \( Z_L = 35.625 + j31.211 \Omega \) provides high PAE and gain for a wide range of input power and gate bias. Table 7 shows some of the cases and results of load pull simulation. C/I, PAE, and output power contours were plotted on a \( Z_L \) Smith chart, see figure 7.

**Table 7 - PAE and Delivered Power**

\( Z_L = 35.625 + j31.211 \Omega \)

<table>
<thead>
<tr>
<th>Case</th>
<th>Vg [V]</th>
<th>Pin [dBm]</th>
<th>PAE [%]</th>
<th>Power Delivered [dBm]</th>
<th>3(^{rd}) IMD [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-3.8</td>
<td>23.35</td>
<td>76.54</td>
<td>38.08</td>
<td>12.5</td>
</tr>
<tr>
<td>2</td>
<td>-3.8</td>
<td>21.35</td>
<td>75.95</td>
<td>37.64</td>
<td>15.8</td>
</tr>
<tr>
<td>3</td>
<td>-3.8</td>
<td>18</td>
<td>61.89</td>
<td>35.28</td>
<td>19.5</td>
</tr>
<tr>
<td>4</td>
<td>-2.8</td>
<td>18</td>
<td>56.4</td>
<td>36.74</td>
<td>16.1</td>
</tr>
<tr>
<td>5</td>
<td>-2.4</td>
<td>18</td>
<td>50.45</td>
<td>36.95</td>
<td>15.5</td>
</tr>
<tr>
<td>6</td>
<td>-2.4</td>
<td>20</td>
<td>56.08</td>
<td>37.86</td>
<td>12.5</td>
</tr>
<tr>
<td>7</td>
<td>-5.0</td>
<td>20</td>
<td>58.84</td>
<td>34.33</td>
<td>13.8</td>
</tr>
<tr>
<td>8</td>
<td>-5.0</td>
<td>21</td>
<td>69.65</td>
<td>35.83</td>
<td>16.1</td>
</tr>
</tbody>
</table>

We confirmed our predictions that the optimal PAE is accompanied by greater distortion. When looking at different biases, no suitable load impedance provided a 3\(^{rd}\) order IMD greater
than 30 dB. Consequently, we chose the load impedance \( Z_L = 35.625 + j31.211 \Omega \) which optimizes PAE while achieving necessary output power\(^3\).

**Figure 7 – Two Tone Load Pull Simulation Results: Vg = -3.8 V, Pin = 23.35 dBm**

### Matching Network Design

Once a load impedance is selected, an appropriate matching network can be designed. The output matching network must match the fundamental frequency to this value while simultaneously shorting 2\(^{nd}\) and 3\(^{rd}\) harmonics. Our chosen output matching network topology can be found in *figure 8*. A \( \lambda/4 \) stub terminated with a DC blocking capacitor to ground is a second harmonic short and a fundamental frequency open. A \( \lambda/12 \) open stub is a 3\(^{rd}\) harmonic short. This stub presents an impedance at the fundamental frequency that must be considered in the matching network design. A matching stub and line are used to match to the desired load impedance \( Z_L = 35.625 + j31.211 \Omega \). The transistor can be DC biased at the end of the \( \lambda/4 \) short without changing the load impedance. *Figure 8* shows the ideal transmission line model in ADS. *Figure 9* shows the ADS Co-Simulation model while *figure 10* shows the matching networks simulated \( \Gamma_L \) at fundamental along with 2\(^{nd}\) and 3\(^{rd}\) harmonic frequencies.

\(^3\) IMS competition requires total output power exceeding 4W (36dBm). In a Doherty Amplifier output power is approximately the sum of the main and auxiliary amplifiers. Therefore, output power of each amplifier (main/aux) must be in the range of 2-4W.
Figure 10 - Output Matching Network EM simulation results
Input Splitter Design

The input to the Aux (Port 2) is 10 dB greater and lagging by 90 degrees relative to the input of Main (Port 3). Therefore, an unequal split quadrature coupler is needed. A 10 dB branchline coupler requires large and impractical line impedances. Lange couplers can also attain a 10 dB power split, but require wire bonding and impractically small trace widths, adding unnecessary manufacturing expenses. A coupled line coupler can provide unequal split ratios, and the required phase shift.

\[
S = \begin{bmatrix}
S_{11} & S_{12} & S_{13} & S_{14} \\
S_{21} & S_{22} & S_{23} & S_{24} \\
S_{31} & S_{32} & S_{33} & S_{34} \\
S_{41} & S_{42} & S_{43} & S_{44}
\end{bmatrix}
\] (1.6)

For a symmetrical 4 port network

\[
S_{11} = S_{22} = S_{33} = S_{44} \quad (1.7)
S_{21} = S_{12} = S_{43} = S_{34} \quad (1.8)
S_{41} = S_{14} = S_{32} = S_{23} \quad (1.9)
S_{31} = S_{13} = S_{42} = S_{24} \quad (1.10)
\]

For 10 dB coupling factor

\[
S = \begin{bmatrix}
0 & \frac{10}{11} \angle -90^\circ & \frac{1}{11} \angle 0^\circ & 0 \\
\frac{10}{11} \angle -90^\circ & 0 & 0 & \frac{1}{11} \angle 0^\circ \\
\frac{1}{11} \angle 0^\circ & 0 & 0 & \frac{10}{11} \angle -90^\circ \\
0 & \frac{1}{11} \angle 0^\circ & \frac{10}{11} \angle -90^\circ & 0
\end{bmatrix}
\] (1.11)

Figure 11 - Coupled Line Coupler
A coupled line coupler has a characteristic impedance of (1.12)

\[(Z_0)^2 = Z_{0e} \times Z_{0o}\]  \hspace{1cm} (1.12)

where \(Z_{0e}\) and \(Z_{0o}\) \(^4\) are calculated in ADS and resulted in the following parameters.

- Trace Thickness: 35 um
- Substrate Height: 0.51 mm
- Trace Width: 15 mil
- Trace Spacing: 6 mil
- Dielectric Constant: 3.48

A 10 dB split requires that the impedance seen by each port is 100\(\Omega\), see figure 12. Matching networks for ports 2 and 3 are low impedance \(\lambda/2\) transmission lines that convert the 100\(\Omega\) impedance seen at the coupler port to the desired source impedance of \(Z_{in}\) determined from load pull simulations. A similar network was used to match port 1.

![Figure 12 - Input Splitter Functional Diagram](see figure 11 for port numbering)

\(^4\) The Even and Odd mode Impedance for coupled microstrip transmission lines is a function of spacing and microstrip parameters [15]. Calculations were done in ADS.
Figure 13 - Input Splitter EM Co-Simulation
Figure 14 - $Z_S$ presented to Aux amplifier, Simulated (blue) vs. Ideal (red)

Figure 15 - $Z_S$ presented to Main amplifier, Simulated (blue) vs. Ideal (red)
For ideal splitter

S21 Ideal = -0.41 dB
S31 Ideal = -10.41 dB

Figure 16 – ADS Forward transmission coefficients showing 10dB Split

Figure 17 – ADS 90° Phase Shift
Complete Simulation

Figure 18 – Complete EM Co-Simulation, Fabricated Model
Table 8 – Simulated $P_{\text{out}}$ (W), PAE vs. $P_{\text{in}}$ (dBm) for Different Bias Conditions

<table>
<thead>
<tr>
<th>Case</th>
<th>$P_{\text{out}}$</th>
<th>PAE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td><img src="image1" alt="Graph 1" /></td>
<td><img src="image2" alt="Graph 2" /></td>
</tr>
<tr>
<td>2</td>
<td><img src="image3" alt="Graph 3" /></td>
<td><img src="image4" alt="Graph 4" /></td>
</tr>
<tr>
<td>3</td>
<td><img src="image5" alt="Graph 5" /></td>
<td><img src="image6" alt="Graph 6" /></td>
</tr>
<tr>
<td>4</td>
<td><img src="image7" alt="Graph 7" /></td>
<td><img src="image8" alt="Graph 8" /></td>
</tr>
<tr>
<td>5</td>
<td><img src="image9" alt="Graph 9" /></td>
<td><img src="image10" alt="Graph 10" /></td>
</tr>
</tbody>
</table>
Table 9 – Simulated $P_{out}$, PAE vs. $P_{in}$ for Different Bias Conditions

<table>
<thead>
<tr>
<th>Case</th>
<th>$V_{DS, Aux}$ (V)</th>
<th>$V_{DS, Main}$ (V)</th>
<th>$V_{GS, Aux}$ (V)</th>
<th>$V_{GS, Main}$ (V)</th>
<th>$P_{out}$ (W) @ $P_m=22$ dBm</th>
<th>PAE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>28</td>
<td>15</td>
<td>-3.3</td>
<td>-3.3</td>
<td>4.000</td>
<td>55.3 %</td>
</tr>
<tr>
<td>2</td>
<td>28</td>
<td>28</td>
<td>-3.3</td>
<td>-3.3</td>
<td>3.945</td>
<td>50 %</td>
</tr>
<tr>
<td>3</td>
<td>28</td>
<td>28</td>
<td>-4.0</td>
<td>-3.3</td>
<td>3.856</td>
<td>55.87 %</td>
</tr>
<tr>
<td>4</td>
<td>28</td>
<td>15</td>
<td>-4.0</td>
<td>-3.3</td>
<td>3.875</td>
<td>62.670 %</td>
</tr>
<tr>
<td>5</td>
<td>28</td>
<td>14</td>
<td>-4.0</td>
<td>-3.6</td>
<td>3.542</td>
<td>64.275 %</td>
</tr>
</tbody>
</table>

The complete simulated model is seen in figure 17. The results of these simulations can be seen in Table 8 and Table 9.

**Fabrication**

After complete EM co-simulations, layout was done in ADS and PCBs were ordered from a PCB manufacturer. Fabrication included soldering components to the PCB, and then using a tap and die with threaded screws to mount the fabricated PCB to a heatsink, see figure 19. The PCB is thermally coupled to the heatsink using thermal paste and held tightly in-place against the heatsink using standard 4-40 machine screws. The transistors were soldered to the board using solder paste and an oven to maintain temperatures below Wolfspeed’s recommended maximum soldering temperature. The passives and banana connectors were soldered by hand.

![Figure 19 - Fabricated Design](image-url)
### Table 10 – Cost/ Bill of Materials

<table>
<thead>
<tr>
<th>Part</th>
<th>Description</th>
<th>Quantity</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>Banana plug connectors</td>
<td>Circuit Board Hardware - PCB Circuit Board Hardware - PCB .125 UNINS. JACK</td>
<td>6</td>
<td>$12.13</td>
</tr>
<tr>
<td>100Ω Terminations</td>
<td>High Frequency/RF Resistors High Frequency/RF Resistors 125 mW 100 Ω 5% Wrap Around</td>
<td>3</td>
<td>$9.72</td>
</tr>
<tr>
<td>100pF Capacitor</td>
<td>Low ESR (0.1 Ω at 1 GHz), and High SRF Silicon RF Capacitors / Thin Film Silicon RF Capacitors / Thin Film 250V 100pF Tol 5%</td>
<td>10</td>
<td>$11.10</td>
</tr>
<tr>
<td>CGH4006P</td>
<td>GaN HEMT JFET Transistor</td>
<td>2</td>
<td>$130.68</td>
</tr>
<tr>
<td>PCB</td>
<td>Rogers 4350B, 5 is the minimum number of boards per order</td>
<td>5</td>
<td>$100.00</td>
</tr>
<tr>
<td>Preamp</td>
<td>PHA 102+ from Mini-Circuits Samples</td>
<td>5</td>
<td>$ -</td>
</tr>
<tr>
<td>Heatsink</td>
<td>Purchased as surplus from RadioShack</td>
<td>1</td>
<td>$4.00</td>
</tr>
<tr>
<td>Thermal Paste</td>
<td>Purchased from Best Buy</td>
<td>1</td>
<td>$14.00</td>
</tr>
<tr>
<td>Broadband RF Choke</td>
<td>4310LC-132KEC, from Coilcraft. Free Sample</td>
<td>4</td>
<td>$ -</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td></td>
<td></td>
<td><strong>$281.63</strong></td>
</tr>
</tbody>
</table>
Testing

Input power vs. PAE was simulated for the design at five different bias conditions in Tables 7 and 8. Single tone PAE testing was done for each case. The bias conditions that provided the best PAE (Case 3 in Table 8) was selected for two-tone testing to measure C/I.

During initial testing, a 1 MHz oscillation was observed as spectral lines spaced 1 MHz apart around the carrier (see Figure 20). To reconcile this issue additional 20 nF ceramic bypass capacitors were added to main and aux drain bias to short provide a better low frequency short than the 100 pF capacitor. The addition of the capacitors eliminated the 1 MHz oscillations that were observable on the spectrum analyzer. Another issue encountered was a 50 kHz oscillation that occurred due to a DC power supply (HP-E360A). The TPS – 4000DC power supplies did not give 50 kHz oscillations when used for biasing the drains.

Figure 20 - 1 MHz Oscillation, Output Spectrum Initial Testing
Table 11 – Test Equipment

<table>
<thead>
<tr>
<th>Equipment</th>
<th>Quantity</th>
<th>Model</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Power Supply</td>
<td>2</td>
<td>TPS – 4000</td>
<td>Drain biasing</td>
</tr>
<tr>
<td>DC Power Supply</td>
<td>3</td>
<td>HP- E360A</td>
<td>Negative gate biasing + Preamp</td>
</tr>
<tr>
<td>Power Head</td>
<td>1</td>
<td>HP - 485A</td>
<td>Power Measurements</td>
</tr>
<tr>
<td>Power Meter</td>
<td>1</td>
<td>HP - 437B</td>
<td>Power Measurements</td>
</tr>
<tr>
<td>Signal Generator 1</td>
<td>1</td>
<td>Agilent - E443B</td>
<td>Signal Generator</td>
</tr>
<tr>
<td>Signal Generator 2</td>
<td>1</td>
<td>HP - 8562A</td>
<td>Signal Generator</td>
</tr>
</tbody>
</table>

Preamp

Preamplification is required to supply 24dBm input power. The preamplifier boards were repurposed from a previous project that used pre-matched amplifiers. The old amplifiers were switched out with higher power versions and were individually tested. Cable losses, uncertainties in signal generator capabilities, and additional preamplification required measurement calibration up to the preamp output. Figure 21 shows the preamp with a PHA-102+ gain block. Figure 22 is the preamplifier calibration block diagram. Figure 23 shows calibration results. The preamp was linear and capable of providing the necessary maximum input power of 24 dBm to the DUT.

![Figure 21 - Preamp Module using PHA-102+](image)

![Figure 22 - Preamp Calibration Diagram](image)
Figure 23 - Preamplifier Characterization

PAE Measurements

PAE measurements were taken under the following bias conditions; $V_{DD\text{ main}} = 15$ V, $V_{DD\text{ aux}} = 28$ V, $V_{GG\text{ main}} = -3.3$ V and, $V_{GG\text{ aux}} = -4$ V. Figure 24 shows the measurement setup for measuring PAE. The simulation results in figure 25 showed a clear Doherty region from 20-30 dBm. However, the measured data in figure 26 has no visible Doherty region. The actual amplifier was drawing less current and was outputting less power (see figure 26) than simulation (figure 25). Further testing on the amplifier could be done to test behavior beyond 25 dBm. However, based on simulations it was not anticipated that measurements would require input powers higher than 25 dBm.

Observing the current drawn by each amplifier suggests that the main and aux see a small fraction of the power coming into the RF input port figure 26. At 25 dBm, the main and auxiliary amplifier draws 19 mA and 135 mA, respectively. In simulation, each amplifier was drawing 100 mA and 175 mA respectively. The main amplifier had a large current draw discrepancy from simulation. Additionally, observing the isolated PAE of the main and comparing to simulation the issue with the design lies primarily with the main amplifier.
Figure 24 – PAE Measurement test setup

Figure 25 – Simulated PAE Test Results

Figure 26 – Measured PAE Test Results
C/I Measurements

Figure 27 shows the test setup used to measure C/I with a two-tone test. Figure 28 shows the results of the C/I test. At low input powers, the device behaved non-linearly with C/I ratios less than 30 dB. As input power increases, C/I reaches the required 30 dB at an input power of 14 dBm per tone. Testing the amplifier at higher input powers with a more powerful preamp, drain currents could be measured as the amplifier is driven toward saturation.

Upon testing it was realized that this topology has poor C/I at low input powers because the main is not turning on fully. Main is biased in Class AB and is seeing 1/20 (figure 16) of the power incident at the input. Further, as the aux turns on, it creates distortion. This behavior was seen in simulation. This can be fixed by adding a power-dependent switch on the aux output. The aux does not provide power until the channel is fully open. Figure 29 shows the amplifier operating linearly with a C/I exceeding 30 dB at an input power of 15 dBm.

Figure 27 – Two Tone test schematic

Figure 28– C/I measurements
Additional Tests

The input splitter was tested to observe the match at port 2 and port 3. This was done by shearing one of the boards up to the gate pad of the transistor and adding SMA connectors and testing each port on a VNA. Figure 30 shows the test setup for these measurements. Figures 31 and 32 show the measured and simulated input splitter S-parameter frequency response.

Figure 30 – Output Spectrum, C/I > 30 dB at P_{in} = 15 dBm

Figure 30 - PCB from Manufacturer (Left), Splitter Test (Right)
Figure 31 - Measured Results of Splitter Test

For ideal splitter
S21 Ideal = -0.41 dB
S31 Ideal = -10.41 dB

Figure 32 - Simulated Results of Splitter Test
Conclusions

The 2 W provided by the amplifier did not meet the minimum output power requirement of 4 W to participate in the IMS competition given the max input power of 21 dBm. There is a loss of gain most likely caused by the input splitter design that was chosen to meet the strict 10 dB split ratio requirement. The input splitter test was inconclusive and further simulations can be done to verify that a redesigned coupled line coupler could work as an input splitter. At higher input powers, although beyond competition rules, the amplifier began to act linearly and had increasing PAE. Testing the amplifier at higher input powers beyond what test equipment allows may show load modulation behavior and a high PAE region.

Banana Plugs

The amplifier was initially manufactured using grabbers instead of banana plugs for DC connections. During testing the negative gate bias for the main amplifier slipped off and caused the drain to draw too much current and destroyed the channel. After this banana plugs were used for sturdy bias connections.

Low Frequency Oscillations

Upon initial testing, 1 MHz oscillations were observed as evenly spaced spectra on the spectrum analyzer. This was because the 100 pF bypass capacitors were insufficient to short lower frequencies. One explanation is that lower frequencies were resonating in the biasing/matching network. Adding a 20 nF bypass capacitor from drain to ground solved the problem.

Post Design Feedback

The splitter was tested as a module and did not simulate or test close to its ideal behavior. $S_{21}$ is over 4.6 dB less than ideal, and $S_{31}$ is 3.5 dB less than ideal. For further improvement on this design. Further EM simulation of the quarter wave splitter could be done. However, there are other solutions that have been considered and are mentioned here for future readers. One possible solution is to redesign with cascaded coupled line couplers [16] which are better suited for asymmetric split ratios. Another solution is to redesign the amplifier so that a 10 dB split is not required. The 10dB power split specification imposed on the design caused the power splitter to be unreliable at best. If a less extreme split ratio was used, an unequal split branchline coupler [17] could be used.
Appendix A. High Efficiency RF and Microwave Solid State Power Amplifiers

The design equations used are based off transistor specifications, Doherty amplifier output power, and output back off (OBO). Generally, OBO is the back off power from the maximum output power where the amplifier is intended to operate. In a Doherty amplifier OBO is the output power region where the Auxiliary amplifier is on and providing enhanced efficiency. Gain linearity factor (GLF) is a figure of merit measuring the linearity of the amplifier in the Doherty region. Our initial design is based on the paper Designing a Doherty Power Amplifier [3] which fixes: GLF = 0 [4]. $x_{\text{break}}$ is a fractional value between $x \{0 \leq x \leq 1\}$ that corresponds to the input drive level when the auxiliary amplifier has a non-zero output current. The value corresponds to the transition of the DPA from the low power region into the Doherty region of operation. $x \{0 \leq x \leq 1\}$ is a parameter that describes output current evolution resulting from different current conduction angle (CCA) which corresponds to different drive levels for $I_{\text{dc}}^{x=0}$ to $I_{\text{Max}}^{x=1}$. This effect is captured in equation A.1 which applies for Main and Aux from High Efficiency RF and Microwave Solid State Power Amplifiers.

$$\cos\left(\frac{\theta_M}{2}\right) = x \cos\left(\frac{\theta_x}{2}\right) \quad (A. 1)$$

$x_{\text{break}}$ approximates the output backoff off by the following.

$$OBO \approx -20 \log_{10}(x_{\text{break}}) \quad (A. 2)$$

Under the constant voltage swing assumption used for the Doherty region, the main amplifier delivers a fraction of the maximum output power at $x_{\text{break}}$ this introduces another design parameter $\alpha$. Maximum current ($I_{\text{Max}}$) of the main amplifier can also be calculated when the desired output power is chosen at $x=1$.

$$\alpha \approx \frac{P_{\text{out_Main_break}}}{P_{\text{out_Main,max}}} = \frac{I_{\text{out_Main_break}}}{I_{\text{out_Main,max}}} \quad (A. 3)$$

$$\alpha \approx \sqrt{OBO} \quad (A. 4)$$

$$I_{\text{Max}} = \frac{P_{\text{out}} \cdot \alpha \cdot 2}{(V_{DD} - V_{Knee})} \quad (A. 5)$$

$\alpha$ fixes the input back off by the following equation.

$$IBO \approx -20 \log_{10}(\alpha) \quad (A. 6)$$

Range of possible OBO values in dB correspond to back off output power from $P_{\text{out_max}}$.

$$OBO = \{-10, -8, -6, -4, -2, 0\}$$

$\zeta$ values that optimize linearity in the Doherty region as a function of OBO from GLF plot$^4$. $0 < \zeta < 0.5$ for class A/B bias.
\( \zeta \) = [0.05, 0.07, 0.08, 0.1, 0.12, 0.14]

\( \theta_{AB} \) can be calculated from \( \zeta \).

\[
\theta_{AB} = 2\pi - \arccos \left( \frac{\zeta}{1 - \zeta} \right)
\]

(A.7)

\( \theta_{AB} = [186.0^\circ, 188.6^\circ, 190.0^\circ, 192.8^\circ, 195.68^\circ, 198.7^\circ] \)

Use \( \theta_{AB} \), the current conduction angle (CCA) to calculate fundamental current contribution from Main when \( x = 1 \).

\[
I_{1,Main}\bigg|_{x=1} = \left( \frac{I_{Max,Main}}{2\pi} \right) \left( \frac{\theta_{AB} - \sin(\theta_{AB})}{1 - \cos \left( \frac{\theta_{AB}}{2} \right)} \right)
\]

(A.8)

\[
I_{1,Main}\bigg|_{x=1} = [0.0819, 0.1037, 0.1309, 0.1656, .2096, 0.2652]
\]

Use \( \alpha \) to calculate the fundamental current contribution from Aux when \( x = 1 \).

\[
I_{1,Aux}\bigg|_{x=1} = \frac{1-\alpha}{\alpha} \left( I_{1,Main}\bigg|_{x=1} \right)
\]

(A.9)

\[
I_{1,Aux}\bigg|_{x=1} = [0.1772, 0.1568, 0.303, 0.0969, 0.0543, 0]
\]

\( x_{break} \) can be calculated by solving equation 15 numerically.

\[
x_{break} [\theta_{Main} - \sin(\theta_{Main})]_{x=x_{break}} = \alpha(\theta_{AB} - \sin(\theta_{AB}))
\]

(A.10)

\[
x_{break} = [0.2708, 0.3412, 0.4466, 0.5794, 0.7591, 1.000]
\]

\( R_L \), is the external load that is seen at \( x = 1 \).

\[
R_L = \frac{V_{DD} - V_{knee}}{I_{1,Main}\bigg|_{x=1} + I_{1,Aux}\bigg|_{x=1}}
\]

(A.11)

\[
R_L = [84.9, 84.5, 84.2, 83.8, 83.4, 83.0]
\]

\( Z_0 \), is the characteristic impedance of the quarter-wave transformer at output of the main amplifier.

\[
Z_0 = \frac{V_{DD} - V_{knee}}{I_{1,Main}\bigg|_{x=1}}
\]

(A.12)

\[
Z_0 = [296.0, 212.2, 168.0, 132.8, 105.0, 83.0]
\]
DC current for Main can be approximated by using $\zeta$

$$\zeta \equiv \frac{I_{DC,Main}}{I_{Max,Main}}$$ (A.13)

$$I_{DC,Main} = [8.1, 14.2, 20.5, 32.3, 48.7, 71.6] \text{ mA}$$

DC current for Aux can be approximated by using the CCA $\theta_C$, to calculate $I_{Max,Aux}$

$$\theta_C = 2 \arccos(x_{\text{break}})$$ (A.14)

$$I_{Max,Aux} = \frac{(I_{1,\text{Aux}}|_{x=1})(2\pi)(1-\cos(\frac{\theta_{AB}}{2}))}{\theta_{AB} \sin(\theta_{AB})}$$ (A.15)

$$I_{DC,Aux} = -I_{Max,Aux} \frac{x_{\text{break}}}{1-x_{\text{break}}}$$ (A.16)

$$I_{DC,Aux} = [-0.28, -0.39, -0.61, -1.02, -2.3] \text{ A}$$

Bias points, power split ratio ‘$\Lambda$’, have been fixed by defining an output power and OBO chosen by the designer.

$$P_{Aux} = \frac{(I_{Max,Aux})^2}{R_L}$$ (A.17)

$$P_{main} = \frac{(Z_0)^2(I_{Max,Aux})^2}{R_L(1+\frac{I_{Max,Aux}}{I_{Max}})}$$ (A.18)

$$\Lambda = \frac{P_{Aux}}{P_{Aux}+P_{Aux}}$$ (A.19)

$$\Lambda = [0.93, 0.91, 0.89, 0.87, 0.85]$$

Table 12 – Design Parameters for Output Power of 37.5dBm at Different Output Backoff Values (OBO)

<table>
<thead>
<tr>
<th>OBO dB</th>
<th>-10</th>
<th>-8</th>
<th>-6</th>
<th>-4</th>
<th>-2</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\zeta$</td>
<td>0.05</td>
<td>0.07</td>
<td>0.08</td>
<td>0.1</td>
<td>0.12</td>
<td>0.14</td>
</tr>
<tr>
<td>$\theta_{AB}^{\circ}$</td>
<td>186.0</td>
<td>188.6</td>
<td>190.0</td>
<td>192.8</td>
<td>195.7</td>
<td>198.7</td>
</tr>
<tr>
<td>$\theta_C^{\circ}$</td>
<td>148.6</td>
<td>140.1</td>
<td>126.9</td>
<td>109.2</td>
<td>81.23</td>
<td>0</td>
</tr>
<tr>
<td>$x_{\text{break}}$</td>
<td>0.27</td>
<td>0.34</td>
<td>0.45</td>
<td>0.58</td>
<td>0.76</td>
<td>1</td>
</tr>
<tr>
<td>$R_L$ $\Omega$</td>
<td>84.9</td>
<td>84.5</td>
<td>84.2</td>
<td>83.8</td>
<td>83.4</td>
<td>83.0</td>
</tr>
<tr>
<td>$Z_0$ $\Omega$</td>
<td>268.5</td>
<td>212.2</td>
<td>168.1</td>
<td>132.8</td>
<td>105.0</td>
<td>83.0</td>
</tr>
<tr>
<td>$I_{DC,Main}$ mA</td>
<td>8.1</td>
<td>14.2</td>
<td>20.5</td>
<td>32.3</td>
<td>48.7</td>
<td>71.6</td>
</tr>
<tr>
<td>$I_{DC,Aux}$ mA</td>
<td>280</td>
<td>390</td>
<td>610</td>
<td>1002</td>
<td>2300</td>
<td>NaN</td>
</tr>
<tr>
<td>$\Lambda$</td>
<td>0.93</td>
<td>0.91</td>
<td>0.89</td>
<td>0.87</td>
<td>0.85</td>
<td>NaN</td>
</tr>
</tbody>
</table>

Relations to derive PAE were found in “Chapter 11: The Doherty Power Amplifier of High Efficiency RF and Microwave Solid State Power Amplifiers” [3] and “Designing a Doherty Power Amplifier” [4]
Since $x$ describes the evolution of the Doherty amplifier conduction across from the low power region ($x \in [0, x_{\text{break}}]$) up until the peak power region ($x = 1$), $x$ should be a function of the input power to the Doherty amplifier. Eq (A.20) describes this relation:

$$P_{\text{in,main}}(x) = \frac{0.5 \cdot (x + V_{\text{in,main,}\text{max}})^2}{R_{\text{in,main}}}$$  \hspace{1cm} (A.20)

**Low Power Region PAE Analysis:**

To analyze the PAE of the DUT all expressions are derived and plotted vs. parameter $x$. The first expression that is derived is RF output power in the low power region.

$$P_{\text{out}}(x) = \frac{x^2}{\alpha} \left[ \left( \frac{\theta_{x,\text{Main}} - \sin(\theta_{x,\text{Main}})}{\theta_{AB} - \sin(\theta_{AB})} \right)^2 \right] \cdot P_{\text{out,Main,Max}} \mid x \in [0, x_{\text{break}}] \hspace{1cm} (A.21)$$

$$\theta_{x,\text{Main}}(x) = 2 \cdot \cos^{-1} \left( \frac{\cos(\theta_{AB})}{x} \right)$$  \hspace{1cm} (A.22)

Next, find the DC power consumed by the DUT as a function of $x$.

$$P_{\text{DC}}(x) = x \cdot \frac{V_{\text{DD}} \cdot I_{\text{M,Main}}}{2\pi} \cdot \frac{2 \sin \left( \frac{\theta_{x,\text{Main}}}{2} \right) - \cos \left( \frac{\theta_{x,\text{Main}}}{2} \right) - \theta_{x,\text{Main}}}{1 - \cos \left( \frac{\theta_{AB}}{2} \right)}$$  \hspace{1cm} (A.23)

With expressions for RF output power and DC power gain of the Doherty amplifier must be found to allow for solving for PAE. In the low power region, the auxiliary amplifier is off. This means all gain of the device comes from the main amplifier.

$$G_{\text{Main}}(x) = G_{\text{Main,\text{break}}} \left[ \theta_{x,\text{Main}} - \sin(\theta_{x,\text{Main}}) \right] \mid x \in [0, x_{\text{break}}]$$  \hspace{1cm} (2.24)

$$\theta_{x,\text{break}} = \theta_{x,\text{Main}}(x_{\text{break}})$$  \hspace{1cm} (A.25)

$$G_{\text{Main,\text{break}}} = G_{\text{AB,Main}} \cdot \frac{\alpha}{x_{\text{break}}^2}$$  \hspace{1cm} (A.26)

Gain of a class AB amplifier can be expressed in terms of class A gain, and conduction angle:

$$G_{\text{AB,Main}} = G_{\text{A}} \left( 1 - \cos \left( \frac{\theta_{AB}}{2} \right) \cdot \left( \frac{\theta_{AB} - \sin(\theta_{AB})}{4\pi} \right) \right)$$  \hspace{1cm} (A.27)

Class A Gain is equivalent to the small signal gain of the transistor ($S_{21}$)

**Doherty Region**

Power out of the main amplifier is dependent on the fundamental (1\textsuperscript{st} order) current component of the main amplifier in the Doherty region ($I_{1,\text{Main}}^+$).

$$P_{\text{out,Main}}(x) = \frac{1}{2} (V_{\text{DD}} - V_r) I_{1,\text{Main}}^+(x) \mid x \in [x_{\text{break}}, 1]$$  \hspace{1cm} (A.28)
DC power is simply the supply voltage multiplied by the DC current component in the Doherty region $I_{o,Main}^+$.

$$P_{DC,Main}(x) = V_D I_{o,Main}^+(x)$$ (A.29)

The DC current component in the Doherty region can be solved for using the following relations:

$$I_{o,Main}^+(x) = I_o(x) - \Delta I_o$$ (A.30)

$$I_o(x) = \begin{cases} \frac{l_{DC}}{2\pi} \frac{I_M \theta_x - \sin(\theta_x)}{\cos\left(\frac{\theta_A}{2}\right)} & \text{if } x < x_{\text{min}} \\ \text{else} & \end{cases}$$ (A.31)

$$x_{\text{min}} = \begin{cases} -\cos\left(\frac{\theta_A}{2}\right) & \text{Main} \\ x_{\text{break}} & \text{Aux} \end{cases}$$ (A.32)

$$\Delta I_o = \frac{x I_{M,Main}}{2\pi} \frac{2 \left(\frac{\theta_s}{2}\right) \cos(\frac{\theta_s}{2}) \theta_s}{1 - \cos(\frac{\theta_A}{2})}$$ (A.33)

Variable $\theta_s$ is defined by the following relation and used to calculate the change in DC current in the Doherty region.

$$\Delta I_1 = I_1(x) - I_{1,Main}^+(x) = \frac{x I_{M,Main}}{2\pi} \frac{\theta_s - \theta_c - \sin(\theta_c)}{1 - \cos(\frac{\theta_A}{2})}$$ (A.34)

$$I_{1,Main}^+ = \alpha \left\{ 1 + \frac{(1-\alpha) \theta_x - \sin(\theta_x) - \sin(\theta_{x,Aux})}{\theta_c - \sin(\theta_c)} \right\} I_{1,Main}(\theta_{AB}) \mid x \in [x_{\text{break}}, 1]$$ (A.35)

$$I_1(x) = \begin{cases} 0 & \text{if } x < x_{\text{min}} \\ \frac{x I_{M,Main}}{2\pi} \frac{\theta_x - \sin(\theta_x)}{1 - \cos(\frac{\theta_A}{2})} & \text{else} \end{cases}$$ (A.36)

Total gain in a Doherty amplifier is a combination of the gain from the main and auxiliary amplifier. Gain for the main and aux amplifier is reduced by the power split ratio ($\Lambda$).

$$G_{doherty} = G_{main} \Lambda_{AB} + G_{aux} \Lambda_c$$ (A.37)

$$G_{main}(x) = \frac{G_{main,AB} \alpha}{x^2} \left[ 1 + \frac{(1-\alpha) \theta_x - \sin(\theta_x) - \sin(\theta_{x,Aux})}{\theta_c - \sin(\theta_c)} \right] \mid x \in [x_{\text{break}}, 1]$$ (A.38)

$$G_{aux}(x) = \frac{G_{aux,CA}}{x} \left[ 1 + \frac{(1-\alpha) \theta_x - \sin(\theta_x) - \sin(\theta_{x,Aux})}{\theta_c - \sin(\theta_c)} \right] \frac{\theta_{x,Aux} \sin(\theta_{x,Aux})}{\theta_c - \sin(\theta_c)}$$ (A.39)

$$G_{Main,AB} = G_A \left( 1 - \cos\left(\frac{\theta_A}{2}\right) \right) \frac{\left(\frac{\theta_{AB} \sin(\theta_c)}{4\pi}\right)}{4\pi}$$ (A.40)

$$G_{Main,C} = G_A \left( 1 - \cos\left(\frac{\theta_c}{2}\right) \right) \frac{\left(\frac{\theta_c \sin(\theta_c)}{4\pi}\right)}{4\pi}$$ (A.41)
References


