Modeling and Analysis of a Four-Switch Buck-Boost Dynamic Capacitor

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Oscar Plasencia
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COMMITTEE MEMBERSHIP

TITLE: Modeling and Analysis of a 4-Switch Buck Boost Dynamic Capacitor

AUTHOR: Oscar Plasencia

DATE SUBMITTED: December 2011

COMMITTEE CHAIR: Dr. Taufik, Professor

COMMITTEE MEMBER: Dr. Ahmad Nafisi, Professor

COMMITTEE MEMBER: Dr. Bill L. Ahlgren, Associate Professor

ABSTRACT

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Oscar Plasencia

Modern electric power utilities are facing a variety of challenges introduced by the increasing complexity of their operation, structure, and consumer loads. One such challenge has been to supply the ever growing demand for reactive power which is essential for grid support. For this reason dynamic VAR technologies are becoming much more important to modern day power systems. A recent dynamic VAR technology known as the Dynamic Capacitor offers full quadrant capacitive VAR control through the combination of AC/AC buck and boost cells. This paper introduces a new topology deemed the “Four-Switch Buck-Boost Dynamic Capacitor” which promises to combine the performance of the AC/AC buck and boost cells into a single power electronic device. This is done in an effort to reduce the required component count and thus reduce the overall device footprint and implementation cost of the Dynamic Capacitor technology. Derivations and analysis will detail the workings of the Four-Switch Buck-Boost Dynamic Capacitor, while simulations in LTSpice and Matlab Simulink will demonstrate the functionality and performance of the proposed topology. The results of this thesis prove the Four-Switch Buck-Boost Dynamic Capacitor to be a feasible shunt reactive compensating device.

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I. INTRODUCTION

Taking a look around in today's world, it is not hard for one to see that electrical energy is by far the most prevalent type of energy being used by the general population. Electrical energy has become popular due to its ease of transportation from one place to another, low environmental pollution, flexibility, high efficiency, and overall low cost in comparison to other forms of energy. According to the U.S. Energy Information Administration the world demand for electricity is increasing at a rate of 2.3% per year with the world electricity generation expected to reach 25.5 trillion kilowatt-hours by 2020 [1]. Electrical energy can be seen in almost every aspect of everyday life ranging from the powering of large industrial factories all the way to the batteries in cell phones. Due to society's heavy dependence on electrical power, the role of electrical utility companies and their ability to generate and transmit electrical power to customers has become of the utmost importance. Furthermore, methods for improving the generation and transmission of electrical power, such as increasing efficiency or improving power quality are highly desirable.

When it comes to power AC power, and more specifically three-phase AC power, has become the standard for large-scale power transmission and distribution across the modern world. Within AC power systems one can find 3 distinct forms of power: *real* power, *reactive* power, and *apparent* power. Apparent power has units of Volt-Amperes (VA) and is the total power that is generated by the system / delivered to a source. Apparent power can be broken down into its real and reactive parts. Real power is referred to as the power dissipated by a load, or in other words the power that allows a load to do work for a given amount of time. Real power

has units of Watts (W) or Joules per second. Reactive power has units of Volt Ampere Reactive (VAR) and is caused by energy storage devices such as inductors or capacitors which store energy and later return it back to the source [2]. Figure 1-1 below depicts what is known as the power triangle which summarizes the relationship between real, reactive, and apparent power. Using the Pythagorean's theorem one can see that the three powers are related by the simple equation $S = \sqrt{P^2 + Q^2}$.

Figure 1-1: Power Triangle

In any discussion on power systems power factor is another important topic. Power Factor is most commonly known as the ratio between real power and apparent power ($\frac{P}{S}$) or, if both the voltage and current are sinusoidal, as the cosine of the impedance phase angle ($\cos \theta$). Power Factor has a unit less value between 0 and 1. If the equivalent load that the system sees is purely resistive then all the power transferred to the load will be real power and will result in unity power factor or in other words, a power factor equal to one [2]. During this case the

system's current and voltage waveform will be identical in shape and phase. On the contrary if the equivalent load is purely reactive (either inductive or capacitive) the power delivered to the load will be purely reactive power and the power factor will be zero. In this case the system's current and voltage waveforms will be out of phase (offset by 90°). For power factor values in between one and zero the equivalent load will be either mostly inductive in which case the system current will lag the system voltage, or it will be mostly capacitive which will cause the system current to lead the system voltage. Modern power systems tend to have a slightly lagging power factor due to the inductive nature of transmission lines and the fact that most loads are inductive (i.e. large induction motors, air conditioners, heaters, etc) [3].

For utilities it is extremely desirable to maintain the system power factor as close to unity as possible. By looking at the power triangle in Figure 1-1 one can see that at a power factor of one the total power delivered to the load (apparent power) is purely real power which as was discussed earlier is the power that allows the load to do work. When the power factor is not at unity a portion of the power delivered to the load is reactive power. Therefore, for a fixed amount of apparent power supplied, as the power factor decreases so does the portion of that power that is real. In large scale utility applications the voltage at the loads is maintained fairly constant and thus the only variable factor in determining the apparent power is the current delivered to the load. For this reason to maintain a fixed amount of real power delivered to a load as the power factor decreases the utility must supply more apparent power which means more current. With higher currents comes higher line losses and in addition since utilities only bill customers for the real power they use (kilowatt hours), it costs utilities money to generate the extra apparent power for the same real power as the power factor decreases. Therefore, utilities

desire to have unity power factor as it is the condition for which they can generate the minimum required apparent power to supply a given amount of real power [3][4].

Since it is highly impractical and nearly impossible to use only resistive loads in order to have unity power factor another method must be used to maintain the power factor as close to unity as possible while leaving existing loads intact. This is where power factor correction comes into play. Traditionally power factor correction is implemented thru what is known as shunt reactive compensation. As previously mentioned large inductive loads generally cause busses throughout the system to have a slightly lagging power factor. In order to raise the power factor at a desired bus closer to unity, a shunt capacitance can be placed at said bus. To illustrate this point one can look at Figures (1-2) – (1-5) below:

Figure 1-2: Uncompensated System (One-Line Diagram)

Figure 1-3: Phasor Diagram for Uncompensated System

Figure 1-4: Compensated System (One-Line Diagram)

Figure 1-5: Phasor Diagram for Compensated System

Figure 1-2 above depicts the one line diagram for a simple uncompensated transmission system with an AC generator supplying a load through a transmission line. From the phasor diagram of said system, shown in Figure 1-3, one can observe that the transmission line current (I_L) and receiving end current (I_R) are identical and are both lagging the receiving end voltage (V_R) by an angle θ (*Note: Here the receiving end voltage is being used as the reference point). Therefore, the receiving bus is operating at a lagging power factor. By connecting a shunt capacitance at the receiving bus, as shown in Figure 1-4, a current (i_c) is injected into the line and the transmission line current is now the summation of the load current and the injected capacitive current. By adjusting the capacitive current to be equal to the magnitude of the load's reactive current demand (i_q), the input current to the bus (which is the same as the transmission line current) is now in phase with the receiving voltage and therefore the power factor at the bus is at unity. The reason for this is that the reactive component of the load current, which is inductive in nature, is now supplied by the reactive current of the capacitor and no longer needs

to be supplied by the source. The source now only needs to supply the real power demands of the load. Therefore the power delivered to the load from the source is now $S = P + j0 = P$. By using simple circuit analysis one can see that $i_c = \frac{V_r}{Z_c} = j\omega C * V_r$, therefore the injected current is directly proportional to the capacitance connected to the bus meaning the injected current can be increased by increasing the shunt capacitance and vice versa. In addition, if we ignore the line resistance the real and reactive power flow in the radial system of figure 1-5 can be modeled by the following two equations (note: X is simply the reactance to the transmission line):

$$P = \frac{|V_s||V_r|}{X} \sin \delta \quad (1-1)$$

$$Q = B_c V_r^2 - \frac{V_r^2 - V_r V_s \cos \delta}{X} \quad (1-2)$$

Where B_c is the reactive admittance of the shunt capacitor or in other words $B_c = \omega C$. Therefore one can see that the addition of shunt capacitors affects the reactive power flow of the system but leaves the real power unchanged.

The benefits of installing shunt capacitors are many. By raising the power factor to unity the transmission line current is reduced is reduced by a factor of $1/\cos\theta$ which signifies that the I^2R losses of the line are reduced by a factor of $(1/\cos\theta)^2$ [3]. By reducing the transmission line current less strain is placed upon the generator, transformers, transmission line, etc. Besides raising the power factor as mentioned above shunt capacitors also raise the bus voltage thus generally improving transmission line voltage regulation [3][4].

II. Background

When discussing present day power systems, the installation of large shunt capacitors is considered the conventional solution for shunt reactive compensation. Shunt capacitors were first employed for compensation purposes in the year 1914, and as previously mentioned are mainly used to reduce line losses, provide voltage support, and correct the power factor at desired locations across the grid [5]. Shunt compensation usually occurs at substations on the distribution level as shown in Figure 2-1. At a given substation anywhere from 1-4 capacitor banks are usually installed, with each bank consisting of 6-10 individual capacitors [6,7]. The number and size of these banks are usually determined by the amount of compensative VAR's needed at a particular location. As the load changes throughout the day capacitor banks are switched in and out of the system through electromechanical switches, known as circuit breakers, in order to maintain the desired power factor [5]. Through this method the injected VAR's are characterized by discrete steps as shown in Figure 2-2.

Figure 2-1: Typical Utility Substation Showing a 4.5 MVAR Capacitor Bank And Adjacent Distribution Loads [6]

Figure 2-2: Discrete Step VAR Injection Behavior Exhibited by the Capacitor Banks [7]

Switched capacitor banks are used by utilities over other solutions due to their inexpensive installation and maintenance costs [8]. However, this technology has many serious downfalls including that its compensation response time is limited by the system frequency

therefore it is sluggish, it is unreliable/requires constant maintenance due to moving parts, and due to discrete switching, large inrush currents and voltage spikes can introduce harmonics into the system during transients thus affecting power quality [5][6][8]. It is common practice that detuning reactors are placed in series with the capacitor banks to prevent the large inrush currents that cause many of these harmonics. It is also common that additional filtering equipment be installed at substations containing capacitor banks. However, the biggest problem with switched or fixed capacitor banks is that their reactive power output is proportional to the square of the voltage across the bank therefore under low voltage conditions when compensation is needed the most, the banks are the least efficient [8].

With the introduction of Flexible AC Transmission Systems (FACTS) into today's existing power systems, utility companies have been able to obtain a surprisingly higher degree of control over the power flow throughout the grid. These power electronic devices have allowed for increased transmission capacities, better power factor correction, higher voltage regulation, decreased harmonics, etc. Furthermore, due to the electronic-based controllers that these FACTS devices implement, they are able to provide rapid response times and can not only frequently vary the output but can do it in a smoothly-adjustable or vernier fashion [9]. For these reasons FACTS devices are becoming viable alternatives to the dominantly mechanical based devices that are often used in power systems, such as the capacitor banks previously mentioned in this chapter. In the area of shunt reactive compensation FACTS devices known as SVC's and STATCOM have been gaining increased attention throughout recent years.

SVC

When it comes to FACTS devices that provide shunt reactive compensation, Static Var Compensators (SVC's) are a well proven technology that promises fast response times and low maintenance requirements [10]. SVC's mainly consist of standard reactive power reactors and capacitors which are controlled via bidirectional thyristor switches to rapidly provide variable reactive power [5]. In essence SVC's act as a variable shunt reactance (either inductive or capacitive) to provide fine control over a wide VAR range. When discussing any sort of SVC configuration one can find that the two main components to be the Thyristor Switched Capacitor (TSC) and the Thyristor Controlled Reactor (TCR).

Figure 2-3: Basic TSC Configuration [5]

The Thyristor Switched Capacitor, or TSC for short, is comprised primarily of a capacitor bank, a bidirectional thyristor switch, and a small current limiting resistor that is used to suppress inrush currents in the case a control malfunction causes wrongful switching [5][9].

The TSC is similar to the previously discussed switched capacitor bank, however it has eliminated the use of moving mechanical parts; and with proper control of the thyristors, it can provide transient-free switching. In order to provide switching, without producing any harmonics, the TSC switching must take place during the zero crossings of the branch current. The switching out process automatically occurs at zero current as long as the thyristor gate signal has been removed prior to the crossing. In order for the switching in process to be transient-free the residual voltage across the capacitor must be equal to the applied AC voltage. There are two cases in which this takes place the first being when the capacitor voltage is equal to the instantaneous AC voltage. If the capacitor voltage happens to be greater than the peak AC voltage applied, the second case occurs when the system AC voltage reaches its peak ($\alpha=0$). If these guidelines are followed then the switching of the TSC will be transient-free

Even with the TSC's improved performance over switched capacitor banks, it still has its disadvantages. The first being that the VAR input is still not continuous but is rather injected in steps. Also in order to implement the TSC each capacitor bank must have its own set of thyristor switches, therefore the construction can be expensive. Lastly, the steady state voltage across the non-conducting thyristor is equal to twice the peak supply voltage so the switches must have high voltage ratings, which again adds to the expense [5].

Figure 2-4: Basic TCR Configuration [5]

The other main component of SVC implementation is known as the Thyristor Controlled Reactor (TCR). As seen in Figure 2-4, the TCR is comprised of a fixed air core reactor and a bidirectional thyristor switch. The thyristors in the switch conduct when a signal is applied to the gate pin and the thyristor is forward biased. They automatically shut off at the next zero crossing of the inductor current. In the case of the TCR the thyristor firing angle (α) can also be adjusted in order to achieve a continuous range of absorbed reactive current/power. The thyristors are fully on (maximum reactive power absorption) at $\alpha=90^\circ$, fully off (no reactive power absorption) at $\alpha=0^\circ$, and partially on at any angle in between [5][9].

The disadvantage of the TCR is that it creates low-frequency odd harmonic currents which in turn cause higher losses [5][9]. These harmonics are suppressed by connecting the TCR in various delta configurations or by installing parallel LCR filters tuned to the dominant 5th and 7th harmonics [9]. The fundamental current component as a function of varying firing angle can be seen in Figure 2-5.

Figure 2-5: Amplitude variation of the fundamental TCR current with delay angle α [9]

In essence the TCR can be described as a variable inductor whose effective admittance is proportional to the inductor current magnitude.

When a Static Var Compensator is implemented at a specific system site it may be composed of a variety of different combinations of TCRs, TSCs, Mechanically Switched Capacitor banks (MSC), and Fixed Capacitor banks (FC) to provide the VAR support required. For example many times a single TCR is placed in parallel with existing fixed capacitor banks at a given substation to form what is called a FC-TCR. However, the most common and most practical SVC configuration is comprised of a TCR in parallel with various TCS branches (TSC-TCR) [5][9][10]. The number of TSC branches is usually determined by practical considerations that include the operating voltage level, maximum VAR output, current rating of the thyristor valves, bus work and installation cost, etc. [9]. As seen in Figure 2-6, this configuration many times includes filters to filter out the low-frequency harmonics created by the TCR, as well as a dedicated transformer such that the compensation equipment is at a medium voltage level thus reducing the ratings that the components must be able to handle [10].

Figure 2-6: Schematic Diagram of SVC [10]

In this configuration the TSCs can provide a step-like VAR output by switching the capacitor banks; however, through simultaneous coordination with the TCR, the SVC will provide a continuous and fully step-less control of reactive power [5]. In order to ensure this seamless control at the extremity conditions, the TCR reactor rating is usually slightly higher than the rating of one TSC branch [9][10]. However, in order to keep harmonics as low as possible the TCR rating should be much smaller than the total rating of the TSC branches combined [5][9]. As seen in Figure 2-7 the SVC is capable of both supplying and absorbing reactive power to and from the system. It is worthy to note that an SVC's rating can be symmetric or asymmetric with respect to inductive or capacitive reactive power. For example it can be designed to supply 200 inductive MVAR and 200 capacitive MVAR, or supply 200 inductive MVAR and 100 capacitive MVAR [10].

Figure 2-7: TSC-TCR VAR demand versus VAR output characteristic [9]

By looking at the big picture it can be seen that the SVC acts as a controllable reactance that can act as either an inductor or capacitor in order to provide a wide range of VAR support. In Figure 2-8 one can see that the limitations of the SVC basically come from the TSC and TCR component ratings. It is obvious that this technology is more advantageous than the shunt capacitor banks previously discussed, not only for the greater range of reactive power that the SVC can supply but also from the fact that it can supply this power much faster.

Figure 2-8: Operating V-I area of the TSC-TCR type VAR generator with two thyristor-switched capacitor banks. [9]

STATCOM

With advances in semiconductor technologies, such as the advent of high power gate turn off thyristor and transistor devices (GTO, IGBT, etc), a new generation of power electronic equipment, such as the STATCOM, show great promise in utility applications [10]. The STATCOM, which has played an important role in the power industry since the 1980's, in simple terms behaves as a Voltage Sourced converter (VSC) [11]. As seen in Figure 2-9 the STATCOM's main components are an energy source (such as a capacitor), a DC-AC converter, and a coupling reactance which in practice is provided by the per phase leakage inductance of the coupling transformer.

Figure 2-9: Basic STATCOM Schematic [9]

When compared to SVC, STATCOM is clearly the superior technology. As shown in Figure 2-10 STATCOM can provide a much wider range of VAR compensation and can do so at much faster speeds, with overall system response times of 10ms or less [11]. Furthermore, unlike SVC, STATCOM can maintain full capacitive output current at low voltage conditions thus making it more efficient at improving system transient stability. STATCOM requires around 50% less installation space than its SVC counterpart, and due to redundancies in its design, STATCOM is also highly reliable [11]. Lastly, STATCOM can control both the amplitude and phase angle of its output voltage, which allows it to exchange both real power and reactive power with the connected power system [5].

Figure 2-10: Comparison of V-I Characteristics for SVC and STATCOM [11]

There are two main topologies used for the DC-AC converter used in STATCOM, multipulse and multilevel. In the multipulse topology (shown in Figure 2-11) 3-phase bridges, such as the ones shown in Figure 2-12, are connected in parallel on the DC side and are magnetically coupled by a zig-zag transformer. The transformer is arranged such that the bridges appear to be connected in series when looking in from the AC side. Furthermore, the transformer windings are usually phase-shifted such that selected harmonics are eliminated [11].

Figure 2-11: Multipulse Converter Diagram [11]

Figure 2-12: Basic 3-Phase Bridges used in STATCOM Topologies [9]

PWM or other wave shaping techniques are used to vary the amplitude of the output voltage waveform as well as providing filtering such that the output more closely resembles a perfect sinusoid [9]. This concept can be seen in Figure 2-13 below. The main disadvantage of this topology is that the zig-zag transformer is bulky, costly, and has to be uniquely designed for each installation [11].

Figure 2-13: PWM used for Amplitude Modulation [5]

The multilevel DC-AC topology, shown in Figure 2-14, is more flexible than its counterpart in the multipulse topology. Furthermore, due to the lack of a transformer it is also smaller in size, less expensive to implement, and introduces less losses [11].

Figure 2-14: Basic Multilevel Topology [11]

In this topology single phase H-bridges are connected in series to form a so called “chain-link” circuit [9][11]. Each bridge produces a square or quasi-square output voltage waveform which can be phase shifted with respect to one another and then combined to produce the total output voltage of the converter (as seen in Figure 2-15). The more H-bridges are connected in series the closer the total output voltage will resemble a perfect sinusoid. As seen in Figure 2-16, with enough bridges the output voltage waveform will be close enough to a perfect sinusoid that it will require little or no extra filtering [9]. With proper control techniques this waveform can be amplitude modulated and phase shifted as desired.

Figure 2-15: Typical output voltage waveform of a three level multilevel converter [11]

Figure 2-16: Voltage quality as a function of number of bridges [5]

Dynamic Capacitor

Unlike SVC or STATCOM technologies which have been around for quite some time, Dynamic Capacitors (otherwise known as Inverter-less STATCOM's) are relatively new VAR compensating devices that offer various advantages over its predecessors. The Dynamic Capacitor (or D-Cap for short) essentially consists of a PWM AC chopper, small LC filter, and a power correction capacitor which work together to essentially create a variable capacitor. The D-Cap can deliver fully controllable capacitive VARs from zero to a maximum design value both under nominal voltage conditions and even during significant system voltage depressions [7] [12] [13].

The PWM AC chopper component of the D-Cap is a technology that has been used in a variety of voltage regulating applications, however, only recently has it been attached to power correction capacitors to provide dynamic shunt VAR compensation. PWM AC choppers are AC/AC converters that use semiconductor switches at high switching frequencies to convert an input sinusoidal voltage into an output sinusoidal voltage of different magnitude. These

converters use very similar topologies to conventional dc/dc voltage regulators such as the buck, boost, and buck-boost converters and even function according to similar transfer functions (but with ac signals as opposed to dc). Usually in order for these topologies to work with AC signals the switching frequency must be kept much higher than the system frequency such that during a given switching period the input and output voltages remain constant (and thus act just like DC) [14] [15].

Figure 2-17: D-Cap Buck Cell [13]

Figure 2-18: Buck Cell Operating Range [13]

Two different topologies have been used to implement Dynamic Capacitors; the buck cell and the boost cell. The buck cell shown in Figure 2-17 consists of a buck PWM AC chopper, an input filter (C_i), and power factor correction capacitor (C). By varying the duty cycle applied to the switches this ac/ac converter can decrease or “buck” the voltage seen across the capacitor from full system voltage (V_s) to zero. This in turn controls the amount of leading reactive

compensating current (proportional to VARs) that is injected back into the system by the capacitor. Thus the converter can also be said to vary the effective capacitance that the system sees (C_{eff}) [7] [12] [13]. Figure 2-18 shows how the buck cell can output low reactive current even at full system voltage. This is important when trying to accurately control the amount of VARs the system needs at a given point in time. The equations describing the behavior of the buck cell can be seen below:

$$V_C = D\hat{V}_s \sin(\omega t) \quad (2-1)$$

$$I_x = \omega D^2 C \hat{V}_s \cos \omega t \quad (2-2)$$

$$C_{eff} = D * C \quad (2-3)$$

Figure 2-19: D-Cap Boost Cell [13]

Figure 2-20: Boost Cell Operating Range [13]

The D-Cap boost Cell shown in Figure 2-19 consists of a boost PWM AC chopper, an input filter (C_i), and power factor correction capacitor (C). By varying the duty cycle applied to its switches the Boost Cell can increase/ “boost” the sinusoidal voltage across the capacitor to a magnitude higher than that of the system input voltage. Once again this varies the amount of capacitive current that the device will inject back into the system thus making the system see an effective capacitance that can be higher than the capacitance of the actual power factor capacitor [7] [12] [13]. By looking at Figure 2-20 one can see that the boost cell is capable of injecting full VAR’s/compensating current even at low system voltages. The range of the boost cell is limited to 1pu current due the current ratings of the semi-conductor components. To limit the boost cell the duty cycle is constrained to a calculated $D_{\max}$ to assure 1pu current [13]. The equations describing the behavior of the boost cell can be seen below:

$$V_C = \frac{\hat{V}_s}{(1 - D)} \sin(\omega t) \quad (2-4)$$

$$I_x = \omega C \hat{V}_s / (1 - D)^2 \cos \omega t \quad (2-5)$$

$$C_{eff} = \frac{C}{1 - D} \quad (2-6)$$

In order for the Dynamic capacitor to provide full quadrant leading VAR control individual buck and boost cells are connected in parallel as shown in Figure 2-21. With this configuration the buck cell can be controlled to provide anywhere from zero to the full amount of VARs the device is designed for under normal line conditions. Furthermore the boost cells can be activated when the amount of VARs required exceed the capability of the buck cell alone such

as when the system voltage drops [12] [13]. The ideal control range of the D-Cap is shown in Figure 2-22.

Figure 2-21: D-Cap formed by the interconnection of buck and boost cells [12]

Figure 2-22: Ideal Control Range for the D-Cap [12]

By combining D-Caps in series as shown in Figure 2-23 it is possible to achieve higher system voltages while still maintaining relatively low individual component ratings. This would allow the D-Cap to be applied at a variety of different voltage levels (distribution, commercial, etc.) [13] [16]. Furthermore, additional papers have discussed controlling the D-cap with the Virtual Quadrature Sources principle such that it can also serve as an active-filter without requiring an inverter stage [7] [17]

Figure 2-23: Series combination of D-Cap cells to achieve higher voltages [13]

As previously mentioned, Dynamic Capacitors offer various advantages when compared to SVC and STATCOM technologies. Firstly due to the high frequency switching of AC Choppers the D-Cap maintains a high input power factor and requires much smaller filtering devices than thyristor based technologies such as SVCs [14] [15]. Also the D-Cap offers microsecond dynamic response time comparable to that of STATCOM and much faster than SVC which has response times of 0.5-1 cycle. This is especially important during transient conditions after a system fault in which rapid response is crucial for whether the voltage will recover or collapse [13]. Furthermore unlike SVCs or MSCs whose VAR output decreases by a factor of the voltage squared, a D-Cap can output full VARs at even low system voltage conditions which is when VARs are needed the most [7] [12] [13]. By not requiring a dc/ac inverter stage the D-Cap is considerably less expensive than a similarly rated STATCOM and through the use of Thin AC converter technologies (TACC) it is possible for Dynamic Capacitors to use existing power factor correction capacitor banks thus further reducing implementation costs. By adding a suitably rated inductor to the D-cap it would be able to provide leading VARs just like SVC and STATCOM [7] [12] [16] [17].

Thesis Outline

This thesis will explore the feasibility of using a Four-Switch Buck-Boost Dynamic Capacitor (D-Cap) topology to provide shunt reactive compensation. The motivation behind exploring this topology is that the proposed Four-Switch Buck-Boost Dynamic Capacitor promises to combine the performance of both the buck and boost D-Cap devices into a single power electronic converter. By doing so, full capacitive VAR control can be achieved using fewer components, thus making the D-Cap an even more affordable technology.

Chapter 1 of this thesis began with a basic introduction of AC power including the concept of power factor and its importance. This first chapter also discussed the idea of shunt reactive compensation and its connection to system power factor and voltage regulation. Chapter 2 provided a brief overview, including the advantages and disadvantages, of existing shunt reactive compensating technologies such as the MSC, SVC, and STATCOM. The chapter concludes with introduction of a newer technology known as the Dynamic Capacitor and how this technology provides superior VAR compensation when compared with SVC while maintaining lower implementation costs than similarly sized STATCOMs.

The remainder of this thesis will be organized as follows: Chapter 3 will discuss design constraints and basic requirements for the 4-Switch Buck-Boost D-Cap, accompanying controls, and simulation test setup. Chapter 4 of this thesis will go into more detail by deriving the transfer functions for this new topology, explaining critical component design calculations, and discussing controller methodology. Chapter 5 will entail design verification via simulations in LTSpice and MATLAB Simulink. Closing analysis, existing problems, and future improvements will all be discussed in Chapter 6 thus concluding this study.

III. Design Constraints

In view of this thesis being more of a proof of concept as opposed to an actual device implementation, many simplifications have been made rather than being scrutinized for performance as may be the case in an actual hardware setup. The largest simplification is the use of ideal components (switches, inductors, capacitors, etc.) to perform the simulations presented later in this thesis. As previously mentioned, the intended purpose of this project is to present an improvement to the existing shunt reactive compensation technology known as the Dynamic Capacitor. This will be done by combining the performance of individual buck and boost D-Cap cells into a single power electronic converter known as the Four-Switch Buck-Boost Dynamic Capacitor. This is all done in an effort to reduce the Dynamic Capacitor's component count and device footprint. The general block diagram for the implementation of the 4-Switch Buck-Boost Dynamic Capacitor is shown in Figure 3-1.

Figure 3-1: General Block Diagram for implementation of 4SWBB D-Cap

4-Switch Buck-Boost Dynamic Capacitor (4SWBB D-Cap)

At the core of the 4-Switch Buck-Boost Dynamic Capacitor is the 4-Switch Buck-Boost converter. While this converter topology is not new, its implementation as an AC/AC converter (or AC chopper) as well as a shunt reactive compensation device are both novel concepts. Although a thorough explanation of the 4-Switch Buck-Boost D-Cap design will be given in Chapter 4, a brief introduction will be given here.

Figure 3-2: Switch Buck-Boost Dynamic Capacitor (with Input Filter Shown)

Looking at Figure 3-2 above one can see that by closing switch SW4, leaving switch SW3 open and modulating switches SW1 and SW2 by D and $(1-D)$ respectively, the 4SWBB D-Cap would essentially behave just like the Buck Cell D-Cap. Conversely by closing switch 1, leaving switch 2 open and modulating switches 3 and 4 by D and $(1-D)$ respectively, the 4SWBB D-Cap would essentially behave just like the Boost Cell D-Cap [18]. Through this logic, by controlling the 4 switches with the appropriate signals the 4SWBB can replace the previous method of implementing a Dynamic Capacitor (parallel combination of buck and boost cells) with a single device.

To prove the 4SWBB D-Cap's shunt reactive compensation capabilities, it is desired to model it after an existing SVC output characteristics. PG&E's 115 kV Potrero Switchyard in San Francisco, CA contains an SVC rated at -100 (inductive)/ +240 (capacitive) MVAR [19]. The design characteristics for the 4SWBB D-Cap as pertaining to this thesis will thus be to provide +240 MVAR at a rated line-to-line voltage of 115 kV. Furthermore, the 4SWBB D-Cap will be designed such that it will be capable of providing full VAR output during a voltage depression (up to 20%) at the connected bus.

Controller

In order for the 4-Switch Buck-Boost Dynamic Capacitor to function as desired, a controller is needed. To provide shunt VAR compensation the controller will monitor the voltage at the bus where the compensation is desired, or in other words, the bus where the D-Cap is connected. This measurement will be compared with a reference voltage set to the nominal bus voltage. The comparison between the two voltages determines the action taken by the controller as discussed below:

$$\underline{V_{bus} < V_{ref} :}$$

When the amount of load (inductive in nature) on the bus is increased the voltage source must supply the reactive current needed by that load. This increased current must travel through a transmission line of fixed impedance thus causing the bus voltage to drop below its nominal value. To correct this, the D-Cap can inject capacitive VARS into the system to counteract/provide the VARS needed by the load thus causing the bus voltage to rise. While the D-Cap is in buck mode the controller will increase the duty cycle to increase VAR output

until the system is compensated or $D_{\text{buck}}=1$, meaning the VAR output in this mode is at its maximum. Once $D_{\text{buck}}=1$ the D-Cap will switch to boost mode and start increasing D_{boost} to provide additional VARs until the system is compensated or the maximum VAR output of the converter has been reached ($D_{\text{boost-max}}$)

$$\underline{V_{\text{bus}} > V_{\text{ref}} :}$$

In this case there is an excess amount of capacitive VARs in the system thus causing the bus voltage to rise above its nominal value. To correct this, the D-Cap must reduce the amount of capacitive VARs that it is injecting. While the D-Cap is in boost mode the controller will decrease the duty cycle until the bus voltage is back to normal or $D_{\text{boost}}=0$. Once $D_{\text{boost}}=0$ the D-Cap will switch to buck mode and start decreasing the duty cycle until the bus voltage is back to normal or $D_{\text{buck}}=0$ at which point the D-Cap is not inputting any VARs.

$$\underline{V_{\text{bus}} = V_{\text{ref}} :}$$

During this case no additional compensation is needed thus the current switching signals are left as is.

Simulation Test Setup

In order to test the 4-Switch Buck-Boost Dynamic Capacitor's abilities as a shunt VAR compensator, it will be connected to a test system as shown in Figure 3-3.

Figure 3-3: General Block Diagram for Experimental Test Setup

As previously mentioned the system voltage will be set to 115 kV_{LL} and the 4SWBB D-Cap will be designed to provide up to +240 MVAR at rated voltage. To test the D-Cap under transient conditions a secondary load will be connected to the initial system load through an ideal switch set to close at a specified time. Different Loads will be used to test the D-Cap in a variety of system conditions. Such load values will be chosen to test three distinct cases which represent three possible modes of D-Cap operation.

- The D-Cap compensates the system in buck mode
- The D-Cap compensates the system in boost mode
- The D-Cap cannot fully compensate the system due to excessive VAR demand

IV. System Design and Component Selection

Transfer Function Derivations

As with any other power electronic devices, the 4SWBB has a set of equations which characterize its basic operation and function. When deriving these equations, one assumption is that the 4-Switch Buck-Boost Converter will operate in Continuous Conduction mode (CCM). Furthermore the switching frequency of this converter will be chosen to be much higher than the system frequency of 60 Hz, thus during any given switching period the input voltage and current will approximately remain constant. For this reason, as will be discussed below, the derivations will be strikingly similar to those of the buck and boost DC/DC counterparts.

Buck Mode

While in buck mode switch SW3 remains open, switch SW4 remains closed, and switch SW1 and SW2 are modulated according to D and $(1-D)$ respectively. The 4SWBB D-Cap then looks like Figure 4-1.

Figure 4-1: 4SWBB D-Cap in Buck Mode

It is worthy to note that since we are dealing with an AC/AC converter the input voltage has the form $v_i(t) = V_i \sin(\omega t)$, however as previously mentioned, f_{sw}

$\gg f_{\text{sys}}$ therefore during any given switching period (T_{sw}) the value for t and thus $v_i(t)$ is relatively constant. During the time interval $kT_{\text{sw}} \rightarrow (k+D)T_{\text{sw}}$ switch SW1 is closed, switch SW2 is open and the D-Cap performs according to the following equations:

$$v_L(t) = v_i(t) - v_o(t) \quad (4-1)$$

$$v_L(t) = L \frac{di_L(t)}{dt} \quad (4-2)$$

$$i_i(t) = i_L(t) = i_o(t) \quad (4-3)$$

$$\Delta i_L = \frac{v_i(t) - v_o(t)}{L} DT \quad (4-4)$$

During the time interval $(k+D)T_{\text{sw}} \rightarrow (k+1)T_{\text{sw}}$ the D-Cap behaves according to the following equations:

$$v_L(t) = -v_o(t) \quad (4-5)$$

$$i_i(t) = 0 \quad (4-6)$$

$$i_o(t) = i_L(t) \quad (4-7)$$

$$\Delta i_L = \frac{-v_o(t)}{L} (1 - D)T \quad (4-8)$$

From equations (4-3), (4-6) and (4-7) we can describe the currents for the Buck mode with the general equations below:

$$i_i(t) = D * i_L(t) \quad (4-9)$$

$$i_o(t) = i_L(t) \quad (4-10)$$

Figure 4-2: Inductor voltage and current waveforms while in buck mode

To derive a steady state transfer function for the buck mode we take a look at the average inductor voltage over an entire switching period. Using equations (4-1) and (4-5) this can be seen to be:

$$v_L(t) = [v_i(t) - v_o(t)]D + [-v_o(t)](1 - D)$$

Reducing the right hand side and plugging in equation (4-2) on the left, this expression becomes:

$$L \frac{di_L(t)}{dt} = Dv_i(t) - v_o(t)$$

Plugging in (4-9) for $i_L(t)$ and through some rearranging of terms we get the equation below:

$$Dv_i(t) = \frac{L}{D} \frac{di_i(t)}{dt} + v_o(t) \quad (4-11)$$

Using equation (4-11) the steady state equivalent circuit for the buck mode 4SWBB D-Cap can be modeled as shown in Figure 4-3.

Figure 4-3: Steady State Equivalent Circuit for the 4SWBB D-Cap in Buck Mode

By applying ohms law to the Steady State Equivalent Circuit of the 4SWBB D-Cap in Buck Mode, the input current is given by:

$$i_i(t) = \frac{Dv_i(t)}{Z_{eq}} \quad (4-12)$$

where the equivalent impedance (Z_{eq}) is defined to be:

$$Z_{eq} = \frac{Z_L}{D} + Z_C = \frac{j\omega L}{D} + \frac{1}{j\omega C}$$

By knowing the impedance of the capacitor and the current flowing through it, the expression for the output voltage in terms of the input voltage is derived:

$$v_o(t) = i_i(t) * Z_C = \frac{Dv_i(t)}{(1 - \frac{\omega^2 LC}{D})} \quad (4-13)$$

Boost Mode

While in buck mode switch SW1 remains closed, switch SW2 remains open, and switch SW3 and SW4 are modulated according to D and (1-D) respectively. The 4SWBB D-Cap then looks like Figure 4-4.

Figure 4-4: 4SWBB D-Cap in Boost Mode

During the time interval $kT_{sw} \rightarrow (k+D)T_{sw}$ switch SW3 is closed, switch SW4 is open and the D-Cap performs according to the following equations:

$$v_L(t) = v_i(t) \quad (4-14)$$

$$v_L(t) = L \frac{di_L(t)}{dt} \quad (4-15)$$

$$i_i(t) = i_L(t) \quad (4-16)$$

$$i_o(t) = 0 \quad (4-17)$$

$$\Delta i_L = \frac{v_i(t)}{L} DT \quad (4-18)$$

During the time interval $(k+D)T_{sw} \rightarrow (k+1)T_{sw}$ switch SW3 is open, switch SW4 is closed and the D-Cap is defined by the following equations:

$$v_L(t) = v_i(t) - v_o(t) \quad (4-19)$$

$$i_i(t) = i_L(t) = i_o(t) \quad (4-20)$$

$$\Delta i_L = \frac{v_i(t) - v_o(t)}{L} (1 - D)T \quad (4-21)$$

From equations (4-16), (4-17) and (4-20) we can describe the currents for the Buck mode with the general equations below:

$$i_i(t) = i_L(t) \quad (4-22)$$

$$i_o(t) = (1 - D) * i_L(t) \quad (4-23)$$

Figure 4-5: Inductor voltage and current waveforms while in boost mode

As in the case of the buck mode, to derive the steady state transfer function for the boost mode we take a look at the average inductor voltage over an entire switching period. Using equations (4-14) and (4-19) this can be seen to be:

$$v_L(t) = [v_i(t)]D + [v_i(t) - v_o(t)](1 - D)$$

Reducing the right hand side and plugging in equation (4-15) on the left, this expression becomes:

$$L \frac{di_L(t)}{dt} = v_i(t) - (1 - D)v_o(t)$$

Plugging in (4-22) for $i_L(t)$ and through some rearranging of terms we get the equation below:

$$\frac{v_i(t)}{1 - D} = \frac{L}{1 - D} \frac{di_i(t)}{dt} + v_o(t) \quad (4-24)$$

Using equation (4-24) the steady state equivalent circuit for the boost mode 4SWBB D-Cap can be modeled as shown in Figure 4-6.

Figure 4-6: Steady State Equivalent Circuit for the 4SWBB D-Cap in Boost Mode

By applying ohms law to the Steady State Equivalent Circuit of the 4SWBB D-Cap in Buck Mode, the input current is given by:

$$i_i(t) = \frac{v_i(t)}{(1-D)Z_{eq}} \quad (4-25)$$

where the equivalent impedance (Z_{eq}) is defined to be:

$$Z_{eq} = \frac{Z_L}{1-D} + Z_C = \frac{j\omega L}{1-D} + \frac{1}{j\omega C}$$

By knowing the impedance of the capacitor and the current flowing through it, the expression for the output voltage in terms of the input voltage is derived:

$$v_o(t) = i_i(t) * Z_C = \frac{v_i(t)}{(1-D)(1 - \frac{\omega^2 LC}{1-D})} \quad (4-26)$$

Looking at the transfer functions for both the buck and boost mode (Equations 4-13 and 4-26 respectively) one can see that they have very similar terms in the denominator.

$$(1 - \frac{\omega^2 LC}{D}) \text{ [buck]} \quad (4-27)$$

$$(1 - \frac{\omega^2 LC}{1-D}) \text{ [boost]} \quad (4-28)$$

These constants are caused by the AC impedance of the inductor and capacitor. Noting that $C = 1/\omega X_C$, $L = X_L/\omega$ and solving the two constants in terms reactance the constants become:

$$(1 - \frac{X_L}{X_C D}) \text{ [buck]} \quad (4-29)$$

$$(1 - \frac{X_L}{X_C (1-D)}) \text{ [boost]} \quad (4-30)$$

By choosing component values such that $X_C \gg X_L$ the right hand term for both the equations above will be very small. Therefore, these constants will be approximately equal to 1 and the transfer functions become:

$$v_o(t) = Dv_i(t) \text{ [buck]} \quad (4-31)$$

$$v_o(t) = \frac{v_i(t)}{(1-D)} \text{ [boost]} \quad (4-32)$$

The transfer functions of the 4SWBB D-Cap, shown equations (4-31) and (4-32), are then identical to the transfer functions of the individual DC/DC buck and DC/DC boost converters respectively [20]. Using equation (4-31) the equation describing the capacitor current for buck mode would then be:

$$i_C(t) = i_L(t) = \frac{v_o(t)}{X_C} = \omega C D v_i(t) \quad (4-33)$$

Using equation (4-9) the resulting input current would be:

$$i_i(t) = D i_C(t) = \omega C D^2 v_i(t) \quad (4-34)$$

The effective shunt capacitance that the 4SWBB D-Cap supplies to the system is defined as the voltage across the physical capacitor divided by the current that the converter injects into the system. While in buck mode, this effective capacitance is calculated as shown below:

$$X_{C_{eff-buck}} = \frac{v_o(t)}{i_i(t)} = \frac{D v_i(t)}{\omega C D^2 v_i(t)} = \frac{1}{\omega C D}$$

$$C_{eff-buck} = \frac{1}{\omega X_{C_{eff-buck}}} = C D \quad (4-35)$$

From equation (4-35) it is clear that by varying the duty cycle, while in buck mode, the 4SWBB D-cap can make the system see a capacitance ranging from 0 to C (full capacitance of

the physical capacitor). This allows the 4SWBB D-Cap to inject low current\VARs at full system voltage if necessary.

Using equation (4-32) the equation describing the capacitor current for boost mode would then be:

$$i_C(t) == \frac{v_o(t)}{X_C} = \frac{\omega C v_i(t)}{(1-D)} \quad (4-36)$$

Using equation (4-23) the resulting input current would be:

$$i_i(t) = \frac{i_C(t)}{(1-D)} = \frac{\omega C v_i(t)}{(1-D)^2} \quad (4-37)$$

The effective shunt capacitance that the 4SWBB D-Cap supplies to the system while in boost mode is calculated as shown below:

$$X_{C_{eff-boost}} = \frac{v_o(t)}{i_i(t)} = \frac{v_i(t)(1-D)^2}{(1-D)\omega C v_i(t)} = \frac{(1-D)}{\omega C}$$

$$C_{eff-boost} = \frac{1}{\omega X_{C_{eff-boost}}} = \frac{C}{(1-D)} \quad (4-38)$$

From equation (4-38) one can see that by varying the duty cycle, while in boost mode, the 4SWBB D-cap can make the system see a capacitance greater than that of the physical capacitor. This allows the 4SWBB D-Cap to provide full VAR output, even at low system voltages.

D_{boost-max} Selection

From the derivations in the section above it is seen that while the converter is in boost mode the voltage output increases towards infinity as the duty cycle approaches a value of 1. However, when the converter reaches a duty cycle of 1, SW3 is always closed while SW4 remains open thus effectively shorting the voltage input (or in a real world case the bus that the

D-Cap is connected to) to ground. This of course is highly undesirable and therefore it is convenient to limit the Duty Cycle of the Boost mode to a specified design value. As mentioned in Chapter 3 for this thesis it is desired for the 4SWBB D-Cap to have the capability of outputting full VARs up to a voltage depression of 20%. Therefore the value of $D_{\text{boost-max}}$ is selected such that during a system voltage drop of 20% the converter can increase the voltage across the capacitor to a value equal to the nominal system input voltage. To do this $D_{\text{boost-max}}$ is chosen to be 0.2 or 20%. To illustrate this point the nominal system voltage for this thesis is 115kV_{LL} (3 ϕ) or 66.4kV_{rms} single phase. A 20% voltage reduction would mean an input voltage of 53.12 kV_{rms}. Using equation (4-32) with $D_{\text{boost}} = D_{\text{boost-max}}$ the voltage across the capacitor would be:

$$v_o(t) = \frac{v_i(t)}{(1-D)} = \frac{53.12 \text{ kV}_{\text{rms}}}{1-0.2} = 66.4 \text{ kV}_{\text{rms}}$$

This corresponds to the nominal system voltage thus the 4SWBB D-Cap will output full VARs.

Capacitor Sizing

When selecting component values for the 4SWBB D-Cap, the size of the power factor correction capacitor is normally the first to be determined. This component is chosen based on the desired VAR rating at the rated system voltage (or $V_i=1\text{pu}$). In other words it is desired for the D-Cap to inject rated VARs when the system sees a capacitance equal to that of the physical power factor correction capacitor ($C_{\text{eff}} = C$ which occurs when $D_{\text{buck}}=1$ and $D_{\text{boost}}=0$). The amount of reactive power that a capacitor generates is given by the equation below:

$$Q_c = V_{\text{rms}}^2 * \omega_{\text{sys}} * C \quad (4-39)$$

By rearranging the equation above we can calculate the capacitance needed for the 4SWBB D-Cap, provided that the amount of VARs needed, system voltage, and system frequency are known.

$$C = \frac{Q}{\omega_{sys} V_{rms}^2} \quad (4-40)$$

As previously mentioned in Chapter 3, for the purpose of this thesis, it is desired to model a single phase 4SWBB D-Cap which will provide +240 MVAR at rated line-to-line voltage of 115kV and system frequency of 60Hz. Using equation (4-40) the capacitance required would be:

$$C = \frac{240 \text{ MVAR}}{2 * \pi * 60\text{Hz} * (115\text{kV}_{L-L} \backslash \sqrt{3})^2} = \mathbf{144\mu F}$$

Note that the line-to-line voltage is divided by a factor of root 3 to obtain the rated single phase RMS voltage.

Switching Frequency Selection

Up until now the only requirement given for the switching frequency of the 4-Switch Buck-Boost Dynamic Capacitor has been that it be much greater than the frequency of the system it is connected to. Earlier in this chapter it is shown how this allows the 4SWBB D-Cap to perform similar to its DC/DC counterparts thus giving the desired functionality for AC signals. There are, however, more considerations that need to be accounted for when selecting the switching frequency.

In order for the 4SWBB D-Cap to function properly as a capacitive shunt reactive compensator it must be seen as a capacitor by the system. For this reason we want the impedance of the system to be almost purely capacitive, or in other terms it is desired for $X_C \gg X_L$. As seen

in the previous section, the size of the capacitor is set at a fixed value which is determined by the desired VAR output. Therefore, the size of the inductor is what must be designed to make this condition true. As will be explained below, the switching frequency is inversely proportional to the size of the inductor needed to maintain CCM, therefore higher switching frequencies are desired. To fulfill these conditions, the switching frequency has been selected to be 20kHz for this thesis.

It is worthy to note that for actual hardware implementations one must take into account that higher switching frequencies result in higher switching losses. However, as previously mentioned, the purpose of this thesis is to prove the concept of the 4SWBB D-Cap through simulations with ideal components. Therefore, switching losses are of no concern at this time.

Inductor Sizing

When sizing the inductor for the 4SWBB C-Cap the main goal is keep the inductor current continuous such that the converter remains in CCM. To do this the critical inductance (smallest inductor value which will maintain CCM condition) must be calculated for the 4SWBB D-Cap in both buck and boost modes.

Buck Mode

The following steps must be taken to calculate the critical inductance during buck mode. Taking Equation (4-8) and rearranging it such that L is on the right hand side:

$$L = \frac{-v_o(t)}{\Delta i_L} (1 - D)T \quad (4-41)$$

A general definition for the inductor current ripple is that it is twice the average inductor current multiplied by the inductor current ripple coefficient (k_i).

$$\Delta i_L = 2 * k_i * i_L(t) \quad (4-42)$$

By inserting Equation (4-42) into Equation (4-41):

$$L = \frac{-v_o(t)}{2 * k_i * i_L(t)} (1 - D)T \quad (4-43)$$

The efficiency of the converter during any given switching frequency is given by:

$$\eta = \frac{v_o(t)i_o(t)}{v_i(t)i_i(t)} \quad (4-44)$$

Assuming $X_C \gg X_L$ the ideal buck transfer function (equation 4-31) can be used.

Combining equations (4-9), (4-31), (4-44) and solving for the inductor current gives the equation below:

$$i_L(t) = \frac{i_o(t)}{\eta} \quad (4-45)$$

By replacing the inductor current in equation (4-43) with equation (4-45):

$$L_c = \frac{1}{2} \left[\frac{v_o(t)(1 - D)\eta}{i_o(t)k_i f_{sw}} \right] \quad (4-46)$$

Since the output voltage is taken across the capacitor and the output current is the current through the capacitor, ohms law states:

$$\frac{1}{\omega_{sys}C} = \frac{v_o(t)}{i_o(t)} \quad (4-47)$$

Plugging equation (4-47) into equation (4-46) the critical inductance for the 4SWBB D-Cap in buck mode is calculated as:

$$L_C = \frac{1}{2} \left[\frac{(1-D)\eta}{\omega_{sys} C k_i f_{sw}} \right] \quad (4-48)$$

Values for the converter switching frequency and capacitor were chosen to be 20kHz and 144μF respectively earlier in this chapter. As this thesis will be dealing with simulations with ideal components it is a reasonable assumption to choose the efficiency to be 100%. It is desired for the converter to remain in CCM for all duty cycles, therefore the critical inductance must be calculated at the worst case scenario. From equation (4-48) it can be seen that a small duty cycle causes the (1-D) term to approach 1 at which point the inductance would be at its highest value. For this thesis the inductor current ripple coefficient has been chosen to be 20%. Using this information the critical inductance for the 4SWBB D-Cap in buck mode is calculated as:

$$L_C = \frac{1}{2} \left[\frac{(1-D)\eta}{\omega_{sys} C k_i f_{sw}} \right] = \frac{1}{2} \left[\frac{1}{2 * \pi * 60 * 144\mu F * 0.20 * 20kHz} \right] = \mathbf{2.3mH}$$

Boost Mode

The following steps must be taken to calculate the critical inductance during boost mode. Taking Equation (4-18) and rearranging it such that L is on the right hand side:

$$L = \frac{v_i(t)}{\Delta i_L} DT \quad (4-49)$$

By inserting Equation (4-42) into Equation (4-49):

$$L = \frac{v_i(t)}{2 * k_i * i_L(t)} DT \quad (4-50)$$

Taking similar steps as previously seen in the buck mode case, by combining equations (4-45) and (4-47) with equation (4-50) above, the critical inductance for the 4SWBB D-Cap in buck mode is calculated as:

$$L_c = \frac{1}{2} \left[\frac{D(1-D)^2 \eta}{\omega_{sys} C k_i f_{sw}} \right] \quad (4-51)$$

Using the same assumptions as in the buck mode case and noting that the worst case scenario for the critical inductance occurs at $D=1/3$, the critical inductance for the 4SWBB D-Cap in boost mode is calculated as:

$$L_c = \frac{1}{2} \left[\frac{D(1-D)^2 \eta}{\omega_{sys} C k_i f_{sw}} \right] = \frac{1}{2} \left[\frac{(\frac{1}{3})(1-\frac{1}{3})^2}{2 * \pi * 60 * 144\mu F * 0.20 * 20kHz} \right] = 340\mu H$$

The 4 Switch Buck-Boost Dynamic Capacitor uses a single inductor for both modes of operation, therefore the larger of the two inductance values must be chosen to assure CCM at all points of operation. The larger inductance value of 2.3mF results from the buck mode equations. For extra precaution a slightly larger inductance value of 2.5mF is chosen for this thesis.

Input Filter Calculations

Due to the high frequency switching of the 4-Switch Buck-Boost Dynamic Capacitor, it is often the case that high frequency harmonics be present at the input side of the converter. It is undesirable for the input of the 4SWBB D-Cap have these input harmonics as they can affect the power quality of the system that the converter is connected to. To eliminate the high frequency harmonics a second-order LC filter is added at the input side of the 4SWBB D-Cap.

Figure 4-7: Basic Low pass filter operation

The basic operation of a low pass filter is shown in Figure (4-7). In simple terms it passes signals with frequencies lower than that of a set cutoff frequency and attenuates signals at frequencies higher than the cutoff frequency. For this thesis the high frequency harmonics to be filtered are located around the switching frequency of the 4SWBB D-Cap which is set at 20kHz. However, it is critical that the fundamental component of the input not be filtered out, therefore the cutoff frequency must not be set too close to 60Hz. With this in mind the cut off frequency is set to one decade below the switching frequency or in other words at 2kHz.

In order for the input filter to not to affect the expected performance of the 4SWBB D-Cap the filter capacitor must be much smaller than the capacitor of the converter. The size of the filter inductor is not as crucial since it is in series with the converter inductor and can only raise the inductance value further above the critical inductance required to keep CCM. Choosing a capacitor size 100 times smaller than the converter capacitor, the inductor value is calculated below:

$$f_c = \frac{1}{2\pi\sqrt{L_i C_i}} \quad (4-52)$$

$$f_c = 2kHz$$

$$C_i \ll C \rightarrow C_i = 1.44\mu F$$

$$L_i = \frac{1}{(2\pi f_c)^2 C_i} = \frac{1}{(2 * \pi * 2kHz)^2 (1.44\mu F)} = 4.4mH$$

Controller Design/Methodology

To function properly as shunt reactive compensator, the 4-Switch Dynamic requires a controller. The controller should take in measurements from the bus that the 4SWBB D-Cap is connected to and then output the appropriate signals to the four switches in order to provide the required amount of VARs. In chapter 3 a general overview of the desired controller functionality was discussed. Describing the design process required to implement said functionality, will be the goal of this section.

Figure 4-8: Block diagram for 4SWBB D-Cap Controller

Figure 4-8 depicts a block diagram for the 4SWBB D-Cap Controller. As one can see the measured bus voltage (V_{in}) is subtracted from a reference voltage (V_{ref}) which is set to the nominal bus voltage. The resulting error signal is passed into a control block which then senses the mode in which the controller is currently in, and then sends the appropriate signals to the

PWM Generators according to the polarity of the error input. The PWM Generators then generate pulses with the desired duty cycles and send the signals to the 4 switches of the D-Cap.

The PWM Generators are implemented using PWM Generator Blocks from the Matlab Simulink Power System Blockset. Each of these blocks incorporates a triangular carrier signal/waveform with amplitude from -1 to 1. The carrier signal is compared with the input signal. One of the PWM Generator's outputs is high when the carrier signal is larger than the input signal and low otherwise. The second output is high when the carrier signal is smaller than the input signal and low otherwise. Therefore, the PWM Generator can be said to output one signal with a duty cycle (D) and the other signal with duty cycle ($1-D$). Looking at Figure 4-8 one PWM Generator provides signals for the buck mode (D_{buck} and $(1-D_{\text{buck}})$ for SW1 and SW2 respectively) while the other provides signals for the boost mode (D_{boost} and $(1-D_{\text{boost}})$ for SW3 and SW4 respectively).

Notice that the duty cycle of the output is varied from 0 to 100% as the input signal is varied from -1 to 1. Furthermore, the frequency of the PWM Generator's outputs is equal to the frequency of the carrier signal. Therefore for this thesis the frequency of the carrier signal is set to 20kHz. This can all be seen in Figure 4-9 below.

Figure 4-9: Waveforms depicting the functionality of a PWM Generator

The D-Cap control Block shown in Figure 4-8 is implemented using Matlab code programed inside a Matlab Function Block. The purpose of this block is to take in the error signal and change the duty cycle of the switches depending on whether the error is positive, negative, or zero.

If the error signal is positive the bus voltage has dropped below its nominal value. Therefore, the system needs more capacitive VARs to counteract the increase in inductive load which has caused the voltage drop. As seen earlier in this section, increasing the duty cycle of the converter increases the effective shunt capacitance that the system senses on the bus, thus it is desired to increase the duty cycle. However, the converter must know what mode it is currently executing, in order to know which duty cycle to increase. If the duty cycle of the boost mode is currently 0% the converter is currently in buck mode and thus the controller increases the signal to the first PWM Generator which in turn increases the buck mode duty cycle. This continues until the error is no longer positive or $D_{\text{buck}} = 100\%$. When $D_{\text{buck}} = 100\%$ the converter

has reached its maximum buck mode VAR output and must start increasing the duty cycle of the boost mode to output more VARs. Again this continues until the error is no longer positive or $D_{\text{boost}} = D_{\text{boost-max}}$ at which point the converter is at its maximum VAR output and can no longer provide further compensation.

If the error signal is negative the bus voltage has risen above its nominal value. Therefore, the system needs less VARs which may be over-compensating the net inductive load and is causing the voltage surge. As seen earlier in this section, decreasing the duty cycle of the converters decreases the effective shunt capacitance that the system senses on the bus, thus it is desired to decrease the duty cycle. Again, the converter must know what mode it is currently executing, in order to know which duty cycle to decrease. If the duty cycle of the buck mode is currently 100% the converter is currently in boost mode and thus the controller decreases the signal to the second PWM Generator which in turn decreases the boost mode duty cycle. This continues until the error is no longer negative or $D_{\text{boost}} = 0\%$. When $D_{\text{boost}} = 0\%$ the converter has reached its minimum boost mode VAR output and must start decreasing the duty cycle of the buck mode to further decrease the converter's VAR output. Again this continues until the error is no longer negative or $D_{\text{buck}} = 0\%$. When $D_{\text{buck}} = 0\%$ the 4SWBB D-Cap is disconnected from the system and the effective shunt capacitance that the system senses is zero.

When the error signal is zero the system is at its nominal voltage value, thus the system is fully compensated. During this condition the controller keeps the duty cycle settings at their current state. Figure 4-10 below provides a flowchart that models the code used to program the D-Cap control block. A copy of the actual code is included in Appendix A.

Figure 4-10: Flow Chart describing the coding sequence for D-Cap Control Block

Note that since Figure 4-10 is a flowchart for the actual code used to program the control block the values depicted correspond to the values sent to the PWM Generators. Therefore, a value of -1 corresponds to a duty cycle of 0% and a value of 1 corresponds to a duty cycle of 100%. Furthermore it is worthy to note that the control block increases/decreases values to the

PWM generators at a set step value each time the code is executed. The code is executed once per time step that the actual Simulink Simulation is run. Therefore the speed at which the controller changes the duty cycle (and thus compensates the system) is a function of the code step size and the simulation discrete sampling time. If the code step size is too large while the sampling time is small the controller constantly overshoots and under shoots the desired duty cycle and therefore the system is not successfully compensated. On the other hand if the code step size is too small while the sampling time is large the controller takes a long time to reach steady state conditions, thus the D-Cap cannot keep up with the required VAR demand and again the system is not compensated. Therefore a balance between the two must be found. After much trial and error, for this thesis the code step size is chosen as 8×10^{-6} and the Simulink Simulation is run at a discrete fundamental sampling time of 1uS

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V. Design Verification and Test Simulations

In chapter 4 a detailed explanation was given regarding the operation and design of a Four-Switch Buck-Boost Dynamic Capacitor. This chapter will take the information provided in the previous chapter in an effort to verify the operation of the 4SWBB D-Cap via simulations in LTSpice and Matlab Simulink.

LTSpice

Before simulating the 4SWBB D-Cap in its entirety, it is desired to first verify the operation of the 4SWBB AC/AC converter. To do so a model was constructed in the SPICE simulation program from Linear Technologies known as LTSpice.

Figure 5-1: LTSpice Model of 4SWBB AC/AC Converter

The 4SWBB AC/AC converter was modeled using the specifications and component values discussed in the previous chapter. These are summarized in Table 5-1 below:

Table 5-1: 4SWBB Model Parameters

Component	Value
Switching Frequency (f_{sw})	20kHz
System Frequency	60Hz
Input Voltage ($v_i(t)$)	115kV _{LL} (3 ϕ) $\rightarrow$ 66.4kV _{rms} (1 ϕ)
Capacitor (C)	144 μ F
Inductor (L)	2.5mH
Input Filter Capacitor (C_i)	1.44 μ F
Input Filter Inductor (L_i)	4.4mH

To test the functionality of the 4SWBB Converter while in buck mode the duty cycle (D_{buck}) is varied from 0% to 100% while leaving SW3 open and SW4 closed (thus $D_{boost} = 0$). From the transfer functions derived in Chapter 4 it is expected that while the converter is in buck mode the output voltage will linearly vary from a minimum value of 0V to a maximum value equal to the input voltage ($v_i(t)$) as the duty cycle is increased from 0% to 100%. This is indeed the observed result seen in Figure 5-2.

Figure 5-2: Output Voltage ($v_o(t)$) as a function of duty cycle (buck mode)

Seeing as the 4SWBB D-Cap is a shunt reactive compensating device, the output voltage is not as relevant information as is the reactive current that the converter is exchanging with the system (which is $i_i(t)$). It is expected that as the output voltage (and thus the voltage across the capacitor) increases, so too should the magnitude of the reactive current at the input of the converter. This is the result that is observed via Figure 5-3.

Figure 5-3: Input Current ($i_i(t)$) as a function of duty cycle (buck mode)

Similarly, to test the functionality of the 4SWBB Converter while in boost mode the duty cycle (D_{boost}) is varied from 0% to 40% while leaving SW1 closed and SW2 open (thus $D_{buck} = 1$). From the transfer functions derived in Chapter 4 it is expected that while the converter is in boost mode the output voltage will increase from a minimum value equal to the input voltage ($v_i(t)$) to a maximum value ideally equal to $(v_i(t)/(1-0.4))$ as the duty cycle is increased from 0% to 40%. This is indeed the observed result seen in Figure 5-4.

Figure 5-4: Output Voltage as a function of duty cycle (boost mode)

As in the buck mode case, once again it is expected that as the output voltage increases, so too should the magnitude of the reactive current at the input of the converter. This is the result that is observed via Figure 5-5. Note that although the duty cycle for boost mode is being limited to 20% , Figures 5-4 and 5-5 show results up to 40% just to prove that the converter continues to increase the voltage and current for duty cycles above $D_{\text{boost}}=20\%$.

Figure 5-5: Input Current ($i_i(t)$) as a function of duty cycle (boost mode)

By measuring the amplitudes of the output voltage waveforms depicted in Figures 5-2 and 5-4, the performance of the 4SWBB AC/AC converter can be compared against the expected values from the ideal buck and boost transfer functions in equations (4-31) and (4-32). The ideal output voltage values are compared with the measured values in Table 5-3. One can see that the measurements are within 15% of the expected values. However, the transfer functions used to calculate the ideal output voltage values were derived without taking into account the input filter. Table 5-4 shows the same measurements; however, these were taken from simulations of the converter without the input filter. As one would expect the margin of error is smaller in this case, with the measurements being within 5% of the expected values. From these tables one can conclude that although the input filter was designed such that it would provide minimal impact on the 4SWBB AC/AC converter, it does cause the performance to deviate slightly from the ideal transfer functions. Note that for the purposes of this thesis D_{boost} is limited to 20%, thus the

only values of interest when looking at boost mode are those at lower duty cycles (these are the ones shown).

Table 5-2: Voltage Measurements for 4SWBB Converter with input filter

Duty Cycle (%)	Ideal Vobuck (V)	Ideal Voboost (V)	Measured Vobuck (V)	Measured Voboost (V)	%error Vobuck	%error Voboost
0	0.00E+00	9.39E+04	1.79E-03	9.96E+04	#DIV/0!	6.092235595
10	9.39E+03	1.04E+05	9.76E+03	1.18E+05	3.951432527	12.80434551
20	1.88E+04	1.17E+05	1.96E+04	1.33E+05	4.164447758	13.69900948
30	2.82E+04	1.34E+05	2.94E+04	1.51E+05	4.412965527	12.33997231
40	3.76E+04	1.56E+05	3.94E+04	1.65E+05	4.936627969	5.186920865
50	4.69E+04	1.88E+05	4.96E+04	-	5.612951326	-
60	5.63E+04	2.35E+05	5.99E+04	-	6.365605141	-
70	6.57E+04	3.13E+05	7.05E+04	-	7.268383975	-
80	7.51E+04	4.69E+05	8.14E+04	-	8.35818511	-
90	8.45E+04	9.39E+05	9.27E+04	-	9.655507035	-
100	9.39E+04	#DIV/0!	9.96E+04	-	6.092235595	-

Table 5-3: Voltage Measurements for 4SWBB Converter w/o input filter

Duty Cycle (%)	Ideal Vobuck (V)	Ideal Voboost (V)	Measured Vobuck (V)	Measured Voboost (V)	%error Vobuck	%error Voboost
0	0.00E+00	9.39E+04	1.79E-03	9.15E+04	#DIV/0!	2.545532006
10	9.39E+03	1.04E+05	9.75E+03	1.05E+05	3.844924912	0.898924273
20	1.88E+04	1.17E+05	1.94E+04	1.17E+05	3.525402066	0.590052189
30	2.82E+04	1.34E+05	2.91E+04	1.29E+05	3.241381759	3.99510065
40	3.76E+04	1.56E+05	3.87E+04	1.39E+05	3.019490894	11.0895729
50	4.69E+04	1.88E+05	4.82E+04	-	2.758547236	-
60	5.63E+04	2.35E+05	5.77E+04	-	2.478077183	-
70	6.57E+04	3.13E+05	6.72E+04	-	2.216879935	-
80	7.51E+04	4.69E+05	7.66E+04	-	1.954414741	-
90	8.45E+04	9.39E+05	8.59E+04	-	1.691104247	-
100	9.39E+04	#DIV/0!	9.15E+04	-	2.534881244	-

As mentioned in chapter 4, in order for the 4SWBB D-Cap to function properly as a shunt capacitive compensator it is imperative that the system see the converter as being mostly a capacitive reactance. Therefore the converter is designed such that $X_C \gg X_L$ (for this design the capacitive reactance is 20 times greater than the inductive reactance). If this is done correctly the current that the compensator exchanges with the system should be capacitive in nature, meaning it should lead the input voltage by 90° . This is the result seen in Figure 5-6. Note that although

the data for Figure 5-6 has been taken while the converter is in buck mode with $D_{\text{buck}} = 0.5$, similar results are seen in both modes and at various duty cycle values.

Figure 5-6: Input Voltage and Input Current ($D_{\text{buck}}=0.5$, $D_{\text{boost}}=0$)

In order to observe the importance of the 4SWBB converter's input filter one must observe the input current for both the case in which there is input filtering and the case for which there is not. Figure 5-7 depicts the input current for a 4SWBB converter that has no input filtering. In this case the signal resembles a “chopped” version of the inductor current. As mentioned before, this type of input current is not desirable as it would introduce high frequency harmonics into the system being compensated, thus degrading the power quality of the AC system.

Figure 5-7: Input Current without Input Filtering ($D_{\text{buck}}=0.5$, $D_{\text{boost}}=0$)

Figure 5-8 shows the input current for a 4SWBB converter with an input filter. As one can see the high frequency harmonics are filtered out and the input current is much closer to resembling an ideal sinusoidal waveform.

Figure 5-8: Input Current with Input Filtering ($D_{\text{buck}}=0.5$, $D_{\text{boost}}=0$)

To observe the relationship between the input current and inductor current of the converter while in buck mode, the two current waveforms can be plotted together as shown in Figure 5-9. One can see that at a duty cycle of 50% ($D_{\text{buck}}=0.5$) the magnitude of the input current is approximately half that of the inductor current. This is expected result according to equation (4-9) which states that the magnitude of the input current is equal to the product of the magnitude of the inductor current and duty cycle.

Figure 5-9: Input Current and Inductor Current ($D_{\text{buck}}=0.5$, $D_{\text{boost}}=0$)

While in boost mode the relationship between input current and inductor current is governed by equation (4-22). According to this equation the inductor current and input current should be equal while the converter is in boost mode. This relationship is shown in Figure 5-10.

Figure 5-10: Input Current and Inductor Current ($D_{\text{buck}}=1$, $D_{\text{boost}}=0.2$)

By looking at the inductor current over a single switching period one can see the characteristic inductor current ripple as shown in Figure 5-11. As there are no discontinuities present in the inductor current, it is verified that the converter is indeed operating in CCM. Comparing it to the driving signal for SW1 one can see that the inductor ripple has a positive slope when SW1 is on and a negative slope when it is off (note the driving signal for SW2 is not shown but it is the opposite of SW1). This is the same behavior as that of a DC/DC buck converter. However, unlike its DC counterpart the 4SWBB AC/AC converter in buck mode can have its output voltage be greater than its input voltage. This occurs during the negative cycle of the voltage waveforms. During this time when SW1 is on the inductor voltage ($v_i(t) - v_o(t)$) is now a negative value and when SW1 is off the inductor voltage ($-v_o(t)$) is now a positive value. Therefore the inductor ripple now has a negative slope when SW1 is on and a positive slope when it is off as seen in Figure 5-12. Figure 5-13 shows the regions on the inductor current waveform that are displayed in Figures 5-11 and 5-12. Also notice that as these waveforms take place at $D_{\text{buck}} = 0.5$, the time it takes for the inductor current ripple to rise equals the time it takes to fall.

Figure 5-11: Inductor Current and SW1 Signal ($D_{\text{buck}}=0.5$, $D_{\text{boost}}=0$, $v_i(t) > v_o(t)$)

Figure 5-12: Inductor Current and SW1 Signal ($D_{\text{buck}}=0.5$, $D_{\text{boost}}=0$, $v_i(t) < v_o(t)$)

Figure 5-13: Inductor current, input voltage and output voltage ($D_{\text{buck}}=0.5$, $D_{\text{boost}}=0$)

Similar to the case of the buck mode, the inductor current over a single switching period while the converter is in boost mode can be seen in Figure 5-14. Once again it is seen that there are no discontinuities present in the inductor current, therefore, it is verified that the converter is indeed operating in CCM. Comparing it to the driving signal for SW3 one can see how the inductor ripple behaves both during the positive and negative cycles of the input and output voltages as shown in Figures 5-14 and 5-15 respectively. . Figure 5-16 shows the regions on the inductor current waveform that are displayed in Figures 5-14 and 5-15.

Figure 5-14: Inductor Current and SW3 Signal ($D_{\text{buck}}=1$, $D_{\text{boost}}=0.2$, $v_i(t) < v_o(t)$)

Figure 5-15: Inductor Current and SW3 Signal ($D_{\text{buck}}=1$, $D_{\text{boost}}=0.2$, $v_i(t) > v_o(t)$)

Figure 5-16: Inductor current, input voltage and output voltage ($D_{\text{buck}}=1$, $D_{\text{boost}}=0.2$)

Simulink

After the operation of the 4SWBB AC/AC converter in LTSpice has been verified, the Four-Switch Buck-Boost Dynamic Capacitor can now be constructed and tested in an AC power system model using Matlab Simulink. Using the same parameters as in the LTSpice model the 4SWBB AC/AC converter was constructed using the Simulink Power System Blockset as shown in Figure 5-17.

Figure 5-17: 4SWBB AC/AC Converter Simulink Model

To provide the needed switching signals for the 4 switches of the 4SWBB AC/AC converter, the controller described in chapter 4 is constructed in Simulink. The 4SWBB AC/AC converter, shown in Figure 5-17, is “masked” into a single block that contains 4 inputs (SW1, SW2, SW3, and V_{in}) and is connected to the controller. To test that the controller and 4SWBB AC/AC converter work as desired, a voltage source (set to the nominal design voltage $66.4kV_{rms}$) is connected to the V_{in} converter input and a Sawtooth waveform is connected to the controller error input. This test set-up is shown in Figure 5-18.

Figure 5-18: D-Cap controller and 4SWBB AC/AC Converter Test Set-up

Figure 5-19 depicts the functionality of the D-Cap control block when it is connected to the Sawtooth error signal. As expected while the error signal is positive the controller increases D_{buck} until it reaches a value of 1 (which produces a duty cycle of 100% by the buck PWM generator). Sensing that D_{buck} has reached its maximum value, and the error is still positive, the controller proceeds to increase D_{boost} . While the error continues to be positive the controller keeps increasing D_{boost} until it reaches $D_{\text{boost-max}} = -0.6$ which, as mentioned in chapter 4, is translated to a duty cycle of 20% by the boost PWM Generator. At approximately 0.062 seconds the error signal becomes negative and the converter begins to decrease the duty cycle beginning in the mode it is currently in, which in this case is boost mode. Once D_{boost} reaches its minimum value of -1 (corresponding to 0% duty cycle) the converter then decreases D_{buck} . In this case the error signal stays negative long enough for D_{buck} to reach its minimum value.

Figure 5-19: Test error input (top), D_{boost} (middle), D_{buck} (bottom)

Figure 5-20 depicts how the 4SWBB AC/AC Converter's output voltage (voltage across power factor correction capacitor) varies in response to the controller signals shown in Figure 5-19. As expected, the amplitude of the output voltage increases as the duty cycle is increased and vice versa. By looking at the section of time when the converter is in boost mode, one can see that the output voltage amplitude increases above the amplitude of the input voltage (93.9kV) to a value approximately equal to 133kv. According to Table 5-2 this is the value expected at duty cycle of 20% while the converter is in boost mode.

Figure 5-20: 4SWBB Converter Output Voltage Response to Sawtooth Error Test

As mentioned earlier in this thesis, the effective capacitance that the 4SWBB D-Cap models increases as the duty cycle is increased. Therefore, as the duty cycle is increased the D-Cap's capacitive VAR output should increase as well. This is seen in Figure 5-21. Note that capacitive VARs are negative in magnitude. Therefore, the more negative the VAR value, the greater the amount of capacitive VARs the D-Cap is outputting. Notice that at approximately 0.05 seconds when $D_{\text{buck}}=1$ (100% buck mode duty cycle) the 4SWBB D-Cap is supplying approximately the nominal design value of 240 MVARs. This is expected seeing that at this condition the power factor correction capacitor is connected directly to the input. One can see that with the added support from the boost mode the D-Cap can output ~420 MVAR at nominal system voltage!

Figure 5-21: 4SWBB D-Cap VAR Output in Response to Sawtooth Error Test

As mentioned in Chapter 4, by setting the value of $D_{\text{boost-max}}$ to 20% the 4SWBB D-Cap should be capable of supplying full VARs (240 MVAR) up to a voltage depression of 20%. To test this condition, the input voltage for the setup in Figure 5-18 is set to 80% of the nominal $66.4\text{kV}_{\text{rms}}$ or in other words to $53.12\text{kV}_{\text{rms}}$. From Figure 5-22 one can see that even though the system voltage is only 80% of its nominal value, the 4SWBB D-Cap is capable of supplying 240MVAR when the converter reaches $D_{\text{boost-max}}=0.2$.

Figure 5-22: 4SWBB D-Cap VAR Output in Response to Sawtooth Error Test and 20% Voltage Depression

After the operations of the D-Cap controller and 4SWBB AC/AC converter have been verified, the final Four-Switch Buck-Boost Dynamic Capacitor is modeled in Simulink as shown in Figure 5-23. As mentioned before, the error input to the controller is formed by subtracting the system input voltage from a set reference voltage. In this model the reference voltage is set to a peak voltage of 93.9kV (which is the single phase peak value of 115kV_{LL}). In order to calculate the amplitude/peak of the system input voltage, a voltage measurement block measures the input voltage and then passes the result to a Discrete Fourier Block which calculates the peak of the sinusoidal waveform.

Figure 5-23: Complete 4SWBB D-Cap Design

To test the true operation of the Four-Switch Dynamic Capacitor a test transmission system is constructed in Simulink. As described in Chapter 3, this test system consists of a voltage source set to the nominal design voltage of $66.4 \text{ kV}_{\text{rms}}$, a transmission line, a receiving end bus, and a load. As the reactive power demand of the load increases so will the voltage drop across the transmission line (modeled as a reactance of 0.002H), thus causing the voltage at the bus to drop below the nominal system voltage. The 4SWBB D-Cap is connected to the receiving end bus as shown in Figure 5-24. The idea is that by connecting the 4SWBB D-Cap near the load, it can supply the reactive power demands of the load. Thus the reactive power that is supplied by the voltage source and the voltage drop across the transmission line should be reduced to approximately zero assuming that the 4SWBB can fully compensate the bus. Three possible modes of compensation that were discussed in chapter 3 will be simulated to demonstrate the operation of the 4SWBB D-Cap.

- The D-Cap compensates the system in buck mode

- The D-Cap compensates the system in boost mode
- The D-Cap cannot fully compensate the system due to excessive VAR demand

Figure 5-24: 4SWBB D-Cap Simulation Test Setup

Compensation in Buck Mode

The first mode of operation of the 4SWBB D-Cap occurs when the device is able to compensate the system while staying in Buck Mode. To ensure that the D-Cap will remain in buck mode, the load is set to draw less reactive power than the rating of the 4SWBB D-Cap. Since the rating of the 4SWBB D-Cap for the purposes of this thesis is designed to be 240 MVAR the load will be set to draw 175 MVAR. In Figure 5-25, one can see that after an initial transient the load draws a constant value of 175 MVARs.

Figure 5-25: Reactive Power Consumption of the Load (Load = 175 MVAR)

The initial transient seen above is due to the fact that the Simulink load component is set to draw 175 MVAR at a nominal voltage of 66.4 kV_{rms}. At first the load causes the voltage on the bus to drop due to the reactive current flowing through the transmission line, therefore the voltage at the bus drops below the nominal voltage and the load does not draw in the full 175 MVAR. As the 4SWBB D-Cap injects capacitive VARs into the system the amount of VARs being supplied from the source, and thus the voltage drop across the transmission line, decreases and the bus voltage returns to its nominal value. Around 0.2 seconds the D-Cap has fully compensated the system, and the load is then drawing its rated 175 MVAR at nominal bus conditions.

Figure 5-26 shows how the initial voltage depression at the bus causes a positive error signal to be sent to the D-Cap controller. The controller sensing this error signal begins to increase the value of D_{buck} and the error signal begins to

decrease. This continues until the error signal reaches the desired value of zero at which point D_{buck} has reached a steady state condition of 0.6 (buck duty cycle of 80%). Since D_{buck} never reaches its maximum value, D_{boost} remains at zero.

Figure 5-26: Error input (top), D_{boost} (middle), D_{buck} (bottom) (Load = 175 MVAR)

Figure 5-27 depicts the reactive power consumption for the Four- Switch Buck-Boost Dynamic Capacitor. As expected the reactive power consumption of the converter begins at a value of zero (as D_{buck} begins at zero), and reaches a maximum value of -175 MVAR at around 0.2 seconds. Since the magnitude of the reactive power consumption is negative this means that the 4SWBB D-Cap is actually supplying reactive VARs into the system/bus. This is what is expected of a shunt capacitive compensator. Furthermore, since the D-Cap supplies 175 MVAR and the load consumes 175 MVAR the system is successfully compensated.

Figure 5-27: Reactive Power Consumption of 4SWBB D-Cap (Load = 175 MVAR)

Figure 5-28 shows the overall system reaction to the 4SWBB D-Cap compensation by depicting the reactive power supply of the source as a function of time. This Figure is basically the summation of Figures 5-25 and 5-27. Since the load begins to consume VARs faster than the 4SWBB D-Cap can initially inject them, the source has to supply this difference in VARs. However, as the D-Cap sources more and more VARs to the load, the VAR output of the source decreases and eventually reaches zero. As previously mentioned, by the source not having to supply the reactive power required by the load there are less losses across the transmission line and better voltage regulation at the bus.

Figure 5-28: Reactive Power Supplied by Source (Load = 175 MVAR)

Figure 5-29 shows how the initial VAR demand of the load causes the voltage on the bus to drop slightly below the desired value of 1pu. As the 4SWBB D-Cap compensates the system the bus voltage returns to its nominal voltage value.

Figure 5-29: Per Unit Bus Voltage (Load = 175 MVAR)

Compensation in Boost Mode

The second mode of operation of the 4SWBB D-Cap occurs when the device is able to compensate the system but must enter boost mode to do so. In Figure 5-21 it was seen that at nominal voltage the D-Cap was supplying ~420MVAR at $D_{\text{boost-max}} = 20\%$. Therefore to ensure that the D-Cap will enter boost mode, but not reach $D_{\text{boost-max}}$, the load is set to draw 390MVAR, which is slightly less than the 420MVAR that can be supplied at $D_{\text{boost-max}}$. As in the previous case, Figure 5-30 shows how after an initial transient the load reactive power remains constant at the value it is set to, which in this case is 390 MVAR.

Figure 5-30: Reactive Power Consumption of the Load (Load = 390 MVAR)

In Figure 5-31 once again one can see that the positive error signal, caused by the reactive demands of the load, force the controller to increase the duty cycles of the 4SWBB D-Cap. In this second case the controller increases D_{buck}

until it reaches its maximum value of 1, yet the error signal continues to be positive. The controller then proceeds to increase D_{boost} until around 0.3 seconds into the simulation at which point the error signal reaches zero and D_{boost} reaches a steady state value of -0.8 (corresponding to a boost duty cycle of 10%).

Figure 5-31: Error input (top), D_{boost} (middle), D_{buck} (bottom) (Load = 390 MVAR)

Figure 5-32 once again shows how the reactive power output of the 4SWBB D-Cap increases as the duty cycle is increased. At around 0.3 seconds it can be seen that the D-Cap reaches steady state and is consuming approximately -390 MVAR, or in other words injecting 390 MVAR into the bus.

Figure 5-32: Reactive Power Consumption 4SWBB D-Cap (Load = 390 MVAR)

As in the previous case, the summation of the Reactive Power Consumption of the load (Figure 5-30) and that of the 4SWBB D-Cap (Figure 5-32) results in the overall reactive power output of the source (Figure 5-33). Once again it is seen that the 4SWBB D-Cap is able to reduce the reactive power output of the source to zero and thus fully compensates the system.

Figure 5-33: Reactive Power Supplied by Source (Load = 390 MVAR)

Compensation not possible

The third and final mode of operation of the 4SWBB D-Cap occurs when reactive power demands of the load exceeds the compensating capabilities of the 4SWBB D-Cap. As mentioned before, in Figure 5-21 it was seen that at nominal voltage the D-Cap was supplying ~ 420 MVAR at $D_{\text{boost-max}} = 20\%$. Therefore to ensure that the D-Cap will not be capable of supplying enough VARs to compensate the load, the load must be set to draw more than 420 MVARs. To ensure that this mode of operation will occur, the load is set to draw 600 MVAR. In Figure 5-34, one can see that after an initial transient the load draws a constant value of 175 MVARs.

Figure 5-34: Reactive Power Consumption of the Load (Load = 600 MVAR)

By observing Figure 5-34, one can see that after an initial transient the load draws a constant value of ~580 MVARs. As previously mentioned the Simulink load component is set to draw a specific amount of VARs (in this case 600MVAR) at a nominal voltage of $66.4 \text{ kV}_{\text{rms}}$. During this third case, however, the load is set to consume more VARs than the 4SWBB D-Cap can produce therefore the system will not be fully compensated and the bus voltage where the load is connected will not be fully restored to the nominal voltage. Therefore, this is why it is seen that the load does not reach 600 MVAR but instead consumes a slightly lower value of 580 MVAR.

Figure 5-35: Error input (top), D_{boost} (middle), D_{buck} (bottom) (Load = 600 MVAR)

Figure 5-35 once again depicts how a positive error signal causes the 4SWBB D-Cap controller to increase the duty cycle starting with buck mode. At an approximate time of 0.275 D_{buck} reaches its maximum value and the converter begins increasing D_{boost} . At approximately 0.32 seconds D_{boost} has reached its maximum value of -0.6 corresponding to a boost mode duty cycle of 20%. It is seen that the error signal is still positive after the 4SWBB D-Cap has reached its maximum VAR output therefore the D-Cap has indeed failed to fully compensate the system.

Figure 5-36: Reactive Power Consumption 4SWBB D-Cap (Load = 600 MVAR)

Figure 5-36 demonstrates the Reactive Power Consumption of the 4SWBB D-Cap as a function of time. It is seen that the shunt compensator has maxed out at slightly higher than the expected 420 MVAR output at $D_{\text{boost-max}}$. This however, is not enough to compensate the 580MVAR demand from the load. Figure 5-37 shows how after the 4SWBB D-Cap has reached its maximum VAR output at around 0.325 seconds the source is still having to supply ~110 MVAR. This shows that the 4SWBB D-Cap has not been able to completely compensate the system as it had in the previous 2 cases.

Figure 5-37: Reactive Power Supplied by Source (Load = 600 MVAR)

Transient Load

Figure 5-38: 4SWBB D-Cap Simulation Test Setup with Transient Load

To test the Four Switch Buck-Boost Dynamic Capacitor under a transient load condition the Simulation Test Setup in Figure 5-38 was constructed. One can see that this is the same setup as in the previous simulations; however, a second load has been connected in parallel with the first, with a switch in between. By extending the simulation time to 1.5 seconds and setting the switch to close at time = 1sec one can observe how the 4SWBB D-Cap responds to a sudden load increase. The initial load is set to draw 175 MVAR at nominal system voltage while the transient is set to draw 215 MVAR. Therefore before the 1 second mark when only the initial load is connected the 4SWBB D-Cap should behave as it did in mode 1. After the 1 second mark the switch will close and the total reactive power demand from the loads will be 390 MVAR thus mimicking the conditions of mode 2.

Figure 5-39: Reactive Power Consumption 4SWBB D-Cap (Initial Load = 175 MVAR, Transient Load = 215 MVAR)

Figure 5-39 depicts how before time = 1 second, the reactive power consumption of the 4SWBB D-Cap is identical to that of case 1. We can see that after the initial transient the converter reaches a steady state output of 175 MVAR. After the transient load is switched in, one can see that the VAR output of the shunt compensator sharply increases and eventually settles out at the expected value of 390 MVAR. The error and duty cycle response for this transient load condition is shown in Figure 3-40. Once again one can see that the response is a combination of the previously discussed simulations for the first 2 modes of operation of the 4SWBB D-Cap.

Figure 5-40: Error input (top), D_{boost} (middle), D_{buck} (bottom) (Initial Load = 175 MVAR, Transient Load = 215 MVAR)

Figure 5-41: Reactive Power Supplied by Source (Initial Load = 175 MVAR, Transient Load = 215 MVAR)

By observing Figure 5-41 one can see that after approximately 0.2 seconds the 4SWBB D-Cap reduces the sources reactive power output to zero thus compensating the system. However, when the transient load is connected there is once again a short period of time that the source must supply reactive power. This spike occurs until the 4SWBB D-Cap once again provides enough VARs to compensate the system at approximately 1.1 seconds into the simulation.

Cost Comparison

One of the major factors that utilities consider when installing FACTS devices is the cost. Therefore if the 4SWBB D-Cap is to be considered a viable option it must compete economically with existing technologies such as SVC and STATCOM. Looking at the STATCOM technology

from chapter 2, one can see that the main components are its AC-DC inverter stage and a large capacitor. As discussed Chapter 2, the STATCOM AC-DC inverter stage is normally made up of multiple H-bridges each of which requires 4 IGBTs to implement [7]. Previous papers have discussed implementing the bidirectional switches needed for Dynamic Capacitors using IGBTs as well. Each bi-directional switch would require 2 IGBTs to implement and since the 4SWBB D-Cap requires 4 of these switches, a total of 8 IGBT's would be needed. Therefore as long as a STATCOM uses more than 2 H-bridges the 4SWBB D-Cap would require less IGBTs to implement. Furthermore, as shown in Figure 2-16 if the STATCOM is to maintain good sinusoidal voltage quality it may require on the order of 16 H-bridges. When it comes to the capacitance required for a set amount of VARs, previous papers have discussed that a STATCOM would require a considerably larger and thus more expensive capacitor [12]. From what is seen above it is clear that the 4SWBB D-Cap should require less capital to implement than a similarly sized STATCOM.

As discussed in Chapter 2, SVC is another technology which 4SWBB D-Cap must be compared to. Firstly from this thesis it is seen that the 4SWBB D-Cap can utilize its boost mode to output more VARs into a system than if its physical capacitor were connected straight to the bus (thus making the system see a higher effective capacitance). Furthermore, it was seen that the 4SWBB D-Cap can provide full VAR output at low system voltages and its VAR output capabilities does not decrease by a factor of the voltage squared as is the case with SVC. Due to the points mentioned above it is clear that the 4SWBB D-Cap requires a smaller capacitor than a suitably sized SVC. When it comes to filtering, SVCs require large harmonic filters due to the fact that thyristor based SVCs produce low frequency harmonics [9]. As was seen in this paper the 4SWBB D-Cap produces high frequency harmonics which require a much smaller input

filter. In the traditional SVC design of a TSC in combination with a TCR, the inductor used by the TCR must have a reactance that is slightly higher than that of the TSC capacitor [9][10]. As was seen in this paper the inductor used by the 4SWBB D-Cap was purposely designed such that its reactance is much smaller than that of the capacitor therefore the inductor used by the 4SWBB D-Cap would be smaller than that of the SVC. However, because thyristors are a technology that is considerably less expensive than IGBTs the switches required to implement the 4SWBB D-Cap would be more expensive than the thyristors needed to implement an SVC.

From the discussion above it would be reasonable to say that the Four-Switch Buck-Boost technology would be less expensive to implement than similarly rated STATCOM. Also, it has been seen that the 4SWBB D-Cap may be slightly more expensive or even on par as far as costs when compared with a similarly sized SVC. The cost to implement a STATCOM has been seen to be \$80-\$100 per kVar while SVC is approximated to cost \$20-\$45 per kVAR [21]. A rough ball-park value for a 4SWBB D-Cap implementation could then be said to be around \$40-\$70 per kVAR.

Figure 5-42: Typical Investment costs for SVC and STATCOM with ball-park investment cost for 4SWBB D-Cap [21]

VI. Conclusion and Recommendations for Future Research

Summary and Conclusion

All in all, the major objective of this thesis was to explore the feasibility of using a Four-Switch Buck-Boost Dynamic Capacitor (D-Cap) topology to provide shunt reactive compensation. Chapter 1, the introduction, discussed the concept of shunt reactive compensation and described the important role it plays in today's power systems. Chapter 2 provided a brief introduction of existing shunt reactive compensation technologies including the relatively new concept of Dynamic Capacitors and the benefits this new technology has to offer. Chapter 3 outlined the major design constraints and objectives of the proposed Four-Switch Buck-Boost Dynamic Capacitor Topology, including the needed controller and simulation test setup. The 4th Chapter of this thesis detailed the theory behind the 4SWBB D-Cap topology, explained the reasoning\equations used when selecting components, and went through the derivations of the converter's transfer functions in both buck and boost mode. Furthermore Chapter 4 specified the design\methodology of the 4SWBB D-Cap controller used in this thesis. Chapter 5 first verified the operation of the Four-Switch Buck-Boost AC/AC converter topology through simulations in LTSpice. It was confirmed that through proper component selection the 4SWBB AC/AC converter behaves much like its DC/DC counterpart and can “buck” or “boost” the AC voltage seen across the capacitor when compared to the input voltage. This in turn allows one to control the reactive current output\VAR output of the 4SWBB D-Cap by changing the duty cycle inputs to the switches. The second half of Chapter 5 concentrated on testing the 4SWBB D-Cap by connecting it to a simulation test setup and performing simulations in the program Matlab

Simulink. From the simulations it was seen that the 4SWBB D-Cap successfully compensates the system by providing the reactive power demand of the load at the bus thus reducing the amount of reactive power supply of the source to approximately zero. This in turn reduces transmission line losses, improves voltage regulation at the compensating bus, and thus will increase overall system stability. It was seen that for VAR demands less than that of the 4SWBB D-Cap design value, the converter remains in buck mode. Furthermore, it was seen that the converter could provide additional VARS by utilizing the boost mode and can supply full compensating VARS during voltage depressions (up to 20% for this design). Through the use of the boost mode, the 4SWBB D-Cap does not suffer from the decrease in VAR output as a function of the voltage squared, which is known to be a major drawback for Mechanically Switched Capacitors and SVC implementations. Lastly it was demonstrated that the 4SWBB D-Cap was able to cope with abrupt transient loads.

In conclusion, this thesis demonstrates that the Four-Switch Buck-Boost Dynamic Capacitor works as expected and is indeed a feasible method of providing shunt reactive compensation. This new topology has proven to be an improvement over the existing method of implementing dynamic capacitors by successfully combining the functionality of the buck and boost D-Cap topologies into a single power electronic device. This in turn allows for a smaller design footprint and lower design costs. The concept of Dynamic Capacitors is still a relatively novel technology but as more research is done on the subject matter it will hopefully one day be a viable alternative to existing SVC and STATCOM devices.

Recommendations for Future Research

Controller

One of the areas of this thesis that can be improved is in the design and implementation of the 4SWBB D-Cap controller. In Chapter 4 it was discussed that the rate at which the duty cycles are changed is currently a function of the code step size and the simulation discrete sampling time. However, this may not be the optimal solution to obtain faster response times. Further research may be done in order to design a controller that will allow the 4SWBB D-Cap to reach the correct steady state duty cycle value in a shorter period of time. Such a controller may be based off of a PI or PID controller design or any other type of controller.

Modification to Provide Lagging Compensation

In Chapter 2 it was seen that SVC and STATCOM devices are capable of supplying both inductive and capacitive VARs into a system. Although this thesis focused primarily on a topology to supply capacitive VARs, further research and design changes may allow the 4SWBB D-Cap to source inductive VARs as well. One method of doing so may be to place a suitably rated reactor in series with the 4SWBB D-Cap. This would require implementation changes to the controller such that the effective capacitance that the 4SWBB D-Cap is producing is changed in relation to the reactance of the reactor, in a sort of balancing game, such that the system would see either an overall inductive reactance or capacitive reactance.

Hardware Construction

A natural extension of this thesis would of course be to build a lab scale prototype. Challenges in this task would include picking suitably rated components that could handle the current and voltage stresses encountered in this power electronic device, building a micro-controller to provide the appropriate switching signals, possibly considering different capacitor types, etc. Choosing suitable semiconductor switches would also be a factor that needs to be accounted for. Previous papers have suggested using wire bonded or Stak Pak IGBT's to implement the required bi-directional AC switches [13].

Scaling the 4SWBB D-Cap to higher voltages

Figure 2-23 back in Chapter 2 demonstrated how through the series connection of D-Cap cells (parallel combination of buck and boost cells) the D-Cap could be scaled to a variety of different voltage levels (distribution, commercial, etc.) without the use of a transformer. A possible extension of this thesis would be to explore the feasibility of reaching the same results though the series connection of 4SWBB D-Cap cells. This would reduce costs by eliminating the need to use a transformer and would reduce the size of individual component ratings.

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Appendix A

```
% Four-Switch Buck-Boost Dynamic Capacitor Controller
% Oscar Plasencia
% Matlab Simulink Simulation

%Function Definition
% Inputs: error ; Outputs: Dbuck, Dboost

function [Dbuck, Dboost] = DCAPcntrl(error)

persistent Dboost_int
persistent Dbuck_int

%Initializing Dboost and Dbuck to
% -1 (zero percent Duty Cycle) during
% first run through code

if isempty (Dboost_int)
    Dboost_int=-1;
end

if isempty (Dbuck_int)
    Dbuck_int=-1;
end

% Limiting Dboost to -0.6 corresponding
% to max boost duty cycle of 20 percent

if Dboost_int>-0.6
    Dboost_int=-0.6;
elseif Dboost_int<-1
    Dboost_int=-1;
end

% Limiting Dbuck to 1 corresponding
% to max buck duty cycle of 100 percent

if Dbuck_int>1
    Dbuck_int=1;
elseif Dbuck_int<-1
    Dbuck_int=-1;
end

Dboost=Dboost_int;
Dbuck=Dbuck_int;

%Positive Error: The Controller begins
%increasing the duty cycle beginning with
%the mode the controller is currently in
```

```

if error > 0
    if Dboost_int==-1                                %Is converter in buck mode?

        if Dbuck_int<1                                %Is Dbuck less than max value?
            Dbuck_int=Dbuck_int+(8e-6);                %increase Dbuck
        else
            Dboost_int=Dboost_int+(8e-6);                %increase Dboost
        end

    else
        %Converter is in boost mode
        if Dboost_int<-0.6                            %Is Dbuck less than max value?
            Dboost_int=Dboost_int+(8e-6);                %Increase Dboost
        end
    end
end

%Negative Error: The Controller begins
%decreasing the duty cycle beginning with
%the mode the controller is currently in

elseif error < 0
    if Dbuck_int==1                                    %Is converter in boost mode?

        if Dboost_int>-1                                %Is Dboost greater than min value?
            Dboost_int=Dboost_int-(8e-6);                %Decrease Dboost
        else
            Dbuck_int=Dbuck_int-(8e-6);                %Decrease Dbuck
        end

    else
        %Converter is in buck mode
        if Dbuck_int>-1                                %Is Dbuck greater than min value?
            Dbuck_int=Dbuck_int-(8e-6);                %Decrease Dbuck
        end
    end
end

end

%No Error: The Controller leaves the
%values of Dbuck and Dboost at their
%current settings

else
    Dboost=Dboost_int;
    Dbuck=Dbuck_int;
end
end

```