Potassium and Sodium Sensing ISFET Device and Array

By:
Liam Hayes

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# Table of Contents

<table>
<thead>
<tr>
<th>Section</th>
<th>Page Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acknowledgments</td>
<td>3</td>
</tr>
<tr>
<td>List of Tables</td>
<td>4</td>
</tr>
<tr>
<td>List of Figures</td>
<td>5</td>
</tr>
<tr>
<td>Abstract</td>
<td>7</td>
</tr>
<tr>
<td>I. Introduction and Background</td>
<td>8</td>
</tr>
<tr>
<td>II. Requirements and Specifications</td>
<td>11</td>
</tr>
<tr>
<td>Device</td>
<td>11</td>
</tr>
<tr>
<td>Array</td>
<td>11</td>
</tr>
<tr>
<td>Fabrication Process</td>
<td>12</td>
</tr>
<tr>
<td>III. Design</td>
<td>12</td>
</tr>
<tr>
<td>Device</td>
<td>12</td>
</tr>
<tr>
<td>Physical Design</td>
<td>13</td>
</tr>
<tr>
<td>Model Description</td>
<td>17</td>
</tr>
<tr>
<td>Array</td>
<td>32</td>
</tr>
<tr>
<td>Fabrication Process</td>
<td>33</td>
</tr>
<tr>
<td>Process Design</td>
<td>33</td>
</tr>
<tr>
<td>Process Conduction/Fabrication Notes</td>
<td>66</td>
</tr>
<tr>
<td>IV. Testing Methodologies</td>
<td>99</td>
</tr>
<tr>
<td>Process Metrology</td>
<td>99</td>
</tr>
<tr>
<td>Device and Array Measurements</td>
<td>100</td>
</tr>
<tr>
<td>V. Testing Results</td>
<td>103</td>
</tr>
<tr>
<td>VI. Conclusion and Recommendations</td>
<td>107</td>
</tr>
<tr>
<td>VII. References</td>
<td>111</td>
</tr>
<tr>
<td>Appendices</td>
<td>116</td>
</tr>
</tbody>
</table>
A. Senior Project Analysis  
B. BOM Analysis  
C. Timeline Analysis  
D. Ethical Analyses  
E. Future Developments  
F. MATLAB Scripts
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List of Tables

Table Name                                                                 Page Number
Table 1: Shows Raw Metrological Data of Wafer Resistivity Used in Wafer Selection 103
Table 2: Raw Data for Oxide Diffusion Mask Thicknesses Note: Wafer #21 Had Accidentally Been Sent to the Next Process and Could Not be in This Data Gathering 104
Table 3: Raw Process Date for Chromium + Silver + Chromium Sputtering 104
Table 4: Raw Process Data for ~30nm Chromium Deposition 105
Table 5: Raw PHPR Process Testing Data 105
Table 6: Raw Sheet Resistance Data From 4-Point Probe Measurements 105
Table 7: Raw PHPR Film Thickness Data Pre and Post Plasma Hardening 106
Table 8: Gate Metallization Chromium Sputter Process Parameters 106
Table 9: Shows Estimated BOM Cost Sheet 119
Table 10: Predictive, Behavioral Device Model MATLAB Script 126
Table 11: Diffusion and Doping Process Time Calculation MATLAB Script 130
### List of Figures

<table>
<thead>
<tr>
<th>Figure Name</th>
<th>Page Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 1: Depicts a Standard Reverse Iontophoresis Process Applied to a Human Skin Surface</td>
<td>9</td>
</tr>
<tr>
<td>Figure 2: Shows Generalized Cross-Sectional View of a Generic ISFET</td>
<td>11</td>
</tr>
<tr>
<td>Figure 3: Shows Modeled I_D Characteristics of Proposed Device in the Subthreshold Regime (Top) and in the Nominal Linear (Orange) and Saturation Regimes (Blue, Bottom)</td>
<td>14</td>
</tr>
<tr>
<td>Figure 4: Shows Fermi-Dirac Distribution Multiplied by the Density of States as Temperature Increases</td>
<td>20</td>
</tr>
<tr>
<td>Figure 5: Shows Electronic Dispersion Relation of Silicon Within the First Brillouin Zone in 3-D k-Space Representation (Right), and the 1-D Projection Factoring in Energy (Left)</td>
<td>21</td>
</tr>
<tr>
<td>Figure 6: Shows Energy Band Shifting Associated with Work Function Calculation</td>
<td>27</td>
</tr>
<tr>
<td>Figure 7: Shows Band Diagram Interpretation of Flat-Band Phenomenon</td>
<td>27</td>
</tr>
<tr>
<td>Figure 8: Cross-Sectional View of Standard Planar MOSFET with Depletion and Effective Junction Depths Depicted</td>
<td>28</td>
</tr>
<tr>
<td>Figure 9: Shows ‘Life-Sized’ View of all Three Photomask Patterns Overlaid in Autocad</td>
<td>53</td>
</tr>
<tr>
<td>Figure 10: Shows Top-Down View of Photomask Pattern of a Single ISFET Device</td>
<td>54</td>
</tr>
<tr>
<td>Figure 11: Shows Example of Nominal ISFET Single Device with Minimum Distance to Body Contact Shown</td>
<td>56</td>
</tr>
<tr>
<td>Figure 12: Shows Example of Nominal ISFET Single Device with Maximum Distance to Body Contact Shown</td>
<td>56</td>
</tr>
<tr>
<td>Figure 13: Shows ISFET Array Containing 2 Series FET Devices Per Parallel Combination</td>
<td>58</td>
</tr>
<tr>
<td>Figure 14: Shows ISFET Array Containing 22 Series FET Devices Per Parallel Combination</td>
<td>59</td>
</tr>
<tr>
<td>Figure 15: Shows Image Proofs of Transparency Photomask Design</td>
<td>60-62</td>
</tr>
<tr>
<td>Figure 16: Shows Zoomed-In View of Single ISFET Device on First Photomask Proof</td>
<td>63</td>
</tr>
<tr>
<td>Figure 17: Shows Zoomed-In View of Single ISFET Device on Second Photomask Proof</td>
<td>63</td>
</tr>
<tr>
<td>Figure 18: Shows Zoomed-In View of ISFET Array on Second Photomask Proof</td>
<td>64</td>
</tr>
<tr>
<td>Figure 19: Shows Zoomed-In View of Single ISFET Device on Third Photomask Proof</td>
<td>65</td>
</tr>
<tr>
<td>Figure 20: Shows Zoomed-In View of ISFET Array on Third Photomask Proof</td>
<td>65</td>
</tr>
<tr>
<td>Figure 21: Shows Full Boat of Wafers Placed in Heated Piranha Solution (a), in BOE (b), and in the Middle of a Drying Stage in the SRD (c)</td>
<td>67</td>
</tr>
<tr>
<td>Figure 22: Resistivity 4-Point Probe Station in Cal Poly Microfabrication Laboratory</td>
<td>67</td>
</tr>
<tr>
<td>Figure 23: Depicts Oxidation Furnace Used (a), Off-Angle View of Wafers Loaded into Quartz Boat (b), and On-Axis View of Wafers Loaded into Quartz Boat (c)</td>
<td>69</td>
</tr>
</tbody>
</table>
Figure 24: Shows Wafers on Quartz Boat Loaded into Furnace at 900°C (a),
Wafers in Quartz Boat Immediately After Being Taken Out of The Furnace (b),
Oxide Thickness Being Measured With the Filmmetrics Profilometer

Figure 25: Primer (Left) and S1813 Photoresist Used (Right) (a), Manual Wafer Centering in Spin-Coater (b), Wafer in the Middle of Spin-Coat Process (c), Soft-Baking Wafer on Hot Plate (d), Wafer on Cold Plate (e), Chromatic Aberration Induced by Photoresist Film (f), First Transparency Mask Mounted on Glass (g), Quintel/Gamm i-line Contact Aligner (h), Post-Lithography Wafer Developing in CD-26 (i)

Figure 26: Shows Photoresist Patterning on Oxide Layer (PR is Green, Oxide is Orange) (a), Wafers Placed in BOE for Oxide Etch (b), Post Oide Etch Pattern (White Now Being Bare Silicon) (c), Wafers Placed in 1165 Remover (d)

Figure 27: AGS Plasma Systems RIE (a), Wafer Placed in Plasma Chamber Before Cleaning (b), 300W O₂ RF Plasma Ignited in RIE Chamber (c)

Figure 28: P507 Diffusant (a), Wafer Centered on Spin-Coater Vacuum Chuck (b), Wafer Undergoing Drive-Off Bake (c), Wafers Placed in Quartz Boat (d), Furnace and Control Panel (e), Furnace Control Panel at Process Temperature (f)

Figure 29: Wafers After Being Removed From Diffusion Furnace (a) (b), n-wells After Diffusion Process (c)

Figure 30: Shows Doped n-wells Underneath Oxide Film

Figure 31: Wafers Immediately After Pulling Them Out Of The Oxidation Furnace (a), Wafers After S1813 Spin-Coat (b), Optical Microscopy View of Aligned and Etched Gate Oxide (c)

Figure 32: Shows Non-Metallized Wafer Loading Onto PVD Chamber Chuck (a), Shows Chromium (Left) and Silver (Right) Targets Loaded Onto Magnetron Guns (b), Shows the Entire PVD System Worked With (c), Shows Wafer Post Metallization (d), Chromium (Orange) and Silver (Dark Brown) Etchants, and Devices in Array Visible Silver Undercutting (e), Shows Wafer Loaded Into Ambios Profilometer, and Testing Result of ~35nm Layer

Figure 33: Single Device Photoresist Patterning for Chromium Etch Step (a), Array Photoresist Patterning for Chromium Etch Step (b), Large Array Patterning After Chromium Etch (c), Small Array Patterning After Chromium Etch Step (d)

Figure 34: Result of Cal Poly’s First Successful Nitride Deposition Process

Figure 35: Shows Profilometry Results for PHPR Process Testing

Figure 36: Shows Wafer With S1813 Resist Spin-Coated in Preparation for Alignment in PHPR Process (a), Post Hard-Baked Wafer (b), Optical Microscopy View of Smaller Array With Gate Regions Patterned for PHPR Process (c), Prepped Wafer in RIE for Plasma Hardening (d), Post Plasma Hardened Wafer Placed in Chuck of PVD Chamber, Awaiting Chromium Sputter (e), Post Etching Wafers With Chromium Flake Still Present (f)

Figure 37: Shows SEM Image of Two Single Devices in an Array
Abstract

The use of Ion-Sensitive Field Effect Transistors (ISFETs) as a means of testing a person’s potassium concentration in real time has broad applications in the consumer space. An avid runner could use such a device to keep track of their hydration and salt levels. A hospital could use it for patients who require around-the-clock remote monitoring, and a variation of ISFETs are currently being used as continuous glucose monitors for diabetes patients. While ISFETs are not a new development in the field of microelectronics, their use as wearable devices has recently become relevant. The goal of this project is primarily to develop a working ISFET with a selectivity bias of potassium and sodium ions with a high level of sensitivity to allow for implementation of the device into a type of “Smart Wristband” someone can wear. In this particular application, the ISFET device will be fed ionic biomolecules via a reverse iontophoresis process, where it can then act as a sensor used to determine the potassium and sodium concentrations of the wearer. A device of this specific nature could be incredibly useful in the medical field as a more convenient means of patient monitoring, specifically for patients with chronic kidney disease or diabetic ketoacidosis [1]. In order to make a device effective enough in this sort of application, the sensitivity of the ISFETs must be very high, and the cost must be low. The following will be a detailed description and analysis of a proposed device design and the associated fabrication methodology used in realizing the proposed design. The following will contain a description and analysis of the designed ISFET device as well as the designed fabrication process and testing methodologies that will be used.
I. Introduction and Background

Both potassium and sodium are critical minerals that allow for bodily functions to take place ranging from the subcellular level, all the way up to the level of organs and their associated systems. For sodium, if someone has too much or too little, their cells will not have the proper osmotic pressures needed to properly hydrate, leading to (in the worst of cases) acute cell death. For potassium, having an out-of-normal concentration level can indicate a vast multitude of issues that may be occurring, from diabetic ketoacidosis, to both chronic and acute kidney disease [1].

While the majority of the human population will never have to think about their sodium or potassium concentrations on a day to day basis, there is a certain subset of people who do. Medical patients with the above listed conditions, kidney transplant donors or recipients, high level athletes, and patients with eating disorders all share in the worry of what may happen if their concentration levels become erratic. At present, if anyone, these high risk patients included, want to get their levels checked, it would require a visit to their doctor, blood tests, and a waiting period. This can be highly troublesome for these at-risk patients, who may need rapid results, or simply do not want to have to spend an entire day just to check up on their health.

A solution to this problem may be near, however, with the advent of wearable medical monitoring devices, largely based on ISFET (Ion Sensitive Field Effect Transistors) technology. When the Dexcom Continuous Glucose Monitoring system broke into the consumer market, it had an immediate effect on diabetes patients, allowing for no more finger pricks, real-time self monitoring, and an ease of use and level of discretion hardly seen in the medical industry. This product, based on ISFET technology, has and will continue to lead the way for similar devices such as the potassium and sodium sensing ISFET being developed for this project.
While the Dexcom CGM Unit is an excellent example of an already realized system that takes advantage of BioFET/ISFET technology, the specific ISFET being designed for this project will differ from both the standard BioFET and currently in-use ISFETs in a few ways. The main electrical difference of these devices is that the natural operating state will be in the subthreshold region of operation, where more conventional device designs utilize the saturation region. This is done in order to match and even exceed prospective current gains and sensitivities usually only observed in designs with more advanced geometries or materials. The second main difference between the specific device being developed for this project and more conventional ISFETs is that it will need to maintain Gate-to-Skin contact throughout its lifetime due to the reverse iontophoresis process being used to drive ions to the sensor (Depicted as the Cathode in Figure 1, below).

Figure 1: Depicts a Standard Reverse Iontophoresis Process Applied to a Human Skin Surface [2]
Most ISFETs used today have a more conventional surrounding setup, wherein an electrolyte solution of a specified type (depends on what is being tested for) will be flowed across the gate contact in order to make a measurement, as is shown in Figure 2. This direct contact necessitated the addition of features to mitigate both potential ESD events from disrupting or even breaking the device, the use of physically strong materials, as well as many other considerations in the overall geometric and electrical design, details of which will be specified in upcoming sections.

*Figure 2: Shows Generalized Cross-Sectional View of a Generic ISFET Use Case [3]*
II. Requirements and Specifications

The following requirements are broken down into three categories, as there are three main design aspects to be considered in the overall project. First, there is the design of a single device, next an array of devices, and lastly, the fabrication processes to be followed. The reasoning behind this is that each category entailed its own design process, thereby necessitating different thought processes when determining the optimal parameters. In general, the determination of the below specifications used a comparative analysis between currently available technology, the ideally desired end results, and the limitations arising from the available testing and fabrication methodologies.

A. Device

1. The device must have as low of a subthreshold swing parameter as is physically realizable given the specified geometry, to allow for as high of a sensitivity as possible, ideally meeting or exceeding the Nernst Limit for BioFET's.
2. Must have a relatively high threshold voltage such that subthreshold operation is able to be maintained throughout nominal operating regimes.
3. Must nominally operate at human body temp (~310K), while being resistant to small thermal fluctuations (no more than a +/-30K variation).
4. Must maintain nominally expected level of ESD and electrical shock safety.
5. Must be compatible with future and previous design plans and objectives.

B. Array

1. Must carry all of the same requirements of the single device.
2. Must nominally maintain total drain currents such that conventional instrumentation techniques can be implemented-no smaller than nano-Ampere regime.
3. May not exceed 10mW of continuous power draw.
4. Must allow for future selectivity layer to be implemented onto devices.
5. Cannot be larger than 1cm x 1cm in surface area.
6. Must be resistant to physical shock and vibrations.

C. Fabrication Process

1. Must utilize conventional CMOS processing techniques with a uniform planar geometry for maximal throughput efficiency.
2. May use no more than 4 photomasks throughout the fabrication process for optimum throughput and manufacturability.
3. No exotic materials can be used, due to deposition limitations.
4. Minimum feature size not to be below 10um due to i-line contact lithography limitations.
5. Must include no more than 50 processing steps to ensure good manufacturability.

III. Design

A. Device

The design of the device overall constitutes two individually designed aspects, namely that of the physical device, and that of a mathematical, predictive behavioral model, which will be of the utmost importance for comparative analysis in the testing phase, as well as being a crucial tool to be used if any iteration on the design is required.
a. **Physical Design**

The ISFET device being developed for this project was designed akin to a nominal rectangular-style geometry, planar MOSFET. As an ISFET is effectively a MOSFET used in a specific application, the main consideration needed in terms of the physical geometry was that the Gate Contact region be left exposed such that ions may reach the contact. The ions will be contacting the Gate via the previously described reverse iontophoresis process, necessitating that Gate-to-Skin contact be made at all times, this left a rather unique situation. The Gate of the FET could not be biased via conventional methods, necessitating some creativity. A potential solution to this was to develop a DGISFET, or Dual-Gated ISFET, as it would allow for any requisite biasing to be performed by the bottom Gate, leaving the top Gate to have the sole purpose of sensing ions. However due to fabrication equipment limitations, this design could not be functionally realized. This was an unfortunate circumstance, as previous exploration into a DG approach yielded excellent results in terms of both device sensitivity and selectivity [4].

It was then recognized that a similar sensitivity level could be realized via the use of the subthreshold region of operation. By having a device operated in the subthreshold region, there would not have to be any explicit Gate biasing at all to achieve accurate sensing, as the thermal interactions alone would provide enough potential to allow for minority carrier conduction through the “channel” of the FET. In theory, the subthreshold region allows for more current gain than all other regions of operation, as well as limits power consumption to a mere fraction of what it otherwise would be in this application. This increase in current-gain brought on by the subthreshold operation can be observed in the plots of Figure 3:
Figure 3: Shows Modelled $I_D$ Characteristics of Proposed Device in the Subthreshold Regime (Top) and in the Nominal Linear (Orange) and Saturation Regimes (Blue, Bottom). Note: Channel Length Modulation Parameter Could Not Been Found Experimentally, giving rise to the relatively large slope of the Saturation Regime Plot.

The only downside with developing this design was that it was a nearly untested mode of operation in the context of ISFET devices, with nearly all real-world ISFET’s utilizing the saturation region of operation. This presented as an interesting tradeoff, in that there were no real, hard results that could be compared against, however with the mentioned positive aspects of this design plan, the tradeoff seemed worthwhile.
To provide further robustness to the design of the subthreshold ISFET, an older technique was implemented as a security blanket, ohmic body biasing. This body biasing would behave as an effective second gate for the FET as a whole, however there are factors associated with it that can only be determined through direct experimentation, such as the biasing levels required. The main impact it would have is to allow for more current to be passed through the conduction channel of the device for a smaller applied true Gate potential, as well as fluctuate the threshold voltage. The level of body biasing that would be required in the finalized design will be determined in the testing phase, as it is largely dependent on the type of instrumentation equipment that would be applied to the eventual system as a whole. However, this gave an opportunity to test an interesting phenomena from a few different aspects, one of which being the overall effectiveness the body effect has in terms of behaving as a true second gate. The other aspect of the phenomena that would undergo testing will be the characterization of the effective spatial range of the body biasing. This will be of the utmost importance since if it is determined that body biasing must be used in the operation of the FET, once the FET’s are placed in an array, it is unclear if the body effect will be felt by all FET’s in the same manner, relative to their distance from the body contact. More information as to this testing approach is given in subsection C.

Another large factor in the macroscopic design of the ISFET is that due to the aforementioned Gate-to-Skin contact, all other regions of the device must be insulated from the user. In order to do this, two methods were initially developed, that of a Parylene coating, and that of a Silicon Nitride coating. While Parylene would yield more favorable electrical properties, in that it has a lower dielectric constant than does Silicon Nitride [5, 6], it would require the use of a Chemical Vapor Deposition (CVD) process as well as the addition of
numerous processing steps in order to account for the etch masking required of the material, both of which the fabrication facility being used was not capable of performing. As this is the case, it was settled that a Stoichiometric Silicon Nitride Reactive Magnetron Physical Vapor Deposition (RMPVD/RPVD) process would be undergone, to provide electrical insulation and physical passivation for the device systems as a whole.

The final macroscopic feature of the design is that of the physical geometries. As mentioned, a relatively general geometry was used in the design in terms of the electrically active aspects. The main parameters of interest are the length and width of the channel region, as these both directly affect the I-V characteristics of the device, through altering the channel resistance. As a high current gain was required of the device as a means of increasing overall sensitivity, the lowest possible channel resistance had to be designed for. As the minimum feature size the available fabrication technology would allow for was 10 micrometers, the channel length was set as such. To improve the effective channel resistance, the cross-sectional area must be increased, and the best way to do this in a controlled fashion is by increasing the channel width drastically with respect to the length. As such, a 100 micrometer channel width was chosen in the design, giving a good tradeoff between a large cross-sectional area, and not making the overall dimensions too large. If the dimensions were too large, then device density when placed in an array would suffer, but if they were too small, desired electrical characteristics could not be realized.

With the above noted considerations made during the design process, it was settled on creating an ISFET device that had the overall geometry of 50 x 100 micrometers (L x W), with the Gate region being 10 x 100 micrometers, and the Source and Drain regions each being 20 x 100 micrometers. The total z-axial stacking of the device (bottom to top, specific to MOS
structure) would naturally be of lightly p-type semiconducting body, with a ~10nm thick Silicon Dioxide dielectric layer, followed by a total ~26nm layer of Titanium and Silver (20nm of Ti and 6nm of Ag). This final metal layer acts as the gate contact, wherein Titanium is used for its exceptional mechanical and adhesion properties, and Silver is used to provide a substrate layer for the selectivity layer to be attached to [7]. Above the Source and Drain contacts, there will be a ~13nm layer of Chromium, then Silver, then Chromium again (7nm of Cr, 20nm of Ag, and 3nm of Cr). The Chromium will aide in the adhesion between the highly conductive Silver metal, the oxide layer below it (oxide layer here is purely for substrate insulation against interconnect currents), and the Silicon Nitride layer above the interconnect metal [7]. Above the metal layers, there will be a ~26nm layer of stoichiometric Silicon Nitride to provide both surface insulation and passivation to protect the device from the user, and isolate the Gate contacts.

\[ b. \ Model\ Description \]

The design of the device largely consisted of the creation of a custom physical model from a quasi-first principles approach. The model utilizes both truly first principles analytical models derived from concepts contained within the realm of solid state physics, as well as models that have been empirically derived. As the mathematics describing the developed device model are described in detail in Table 11 in Appendix F, this section will contain descriptions and reasoning behind the individual constituents of the model and their purpose, with references to the mathematics describing the physical phenomena, and derivations for the first principals analysis that was done (Note: Explicit dimensions of each provided function are given in the MATLAB Script in Table 10 of Appendix F).
While there were many considerations made in the development of this model, the initial point of note is of the thermal phenomena occurring within the Silicon crystal lattice. Since the device will be in constant contact with the wearer’s skin, it will effectively be operating at body-temperature, of which the accepted average is 37°C, or 310K. This alone influences many physical features of the material at hand, and as will be demonstrated, is a main reason for why subthreshold operation was chosen to be implemented. This increase in operating temperature relative to a nominal design temperature of room-temp. (~300K) influences the thermal voltage, intrinsic charge carrier density, intrinsic band-gap, chemical potential, and carrier mobility directly, while influencing nearly all other physical factors indirectly. From the thermal considerations, the complete model will be constructed.

When taking the considerations of the thermal voltage, it is calculated via:

\[ V_t = \frac{k_B T}{e} \]

With \( k_B \) being Boltzmann’s Constant in J/K, \( T \) being the absolute operating temperature, and \( e \) being the characteristic free-space charge of a single electron. This value in and of itself is indicative of the average thermal potential of the electrons in a closed system, given in terms of a voltage [8]. In the context of the ISFET being designed here, it does not intrinsically give any great meaning, but is a valuable tool in conducting the remaining analysis.

Next, there is the intrinsic charge carrier density. It is a crucial value in the context of semiconductor device design as it is used primarily in determining the bulk potential work function of the silicon in reference to the vacuum energy. This is in turn utilized in the calculation of the threshold voltage and the flatband voltage, both of which will be discussed later. The determination of this parameter is much more involved than the thermal voltage in
In general, as the temperature of a semiconducting material is increased, up until a critical value, the number of charge carriers will increase, thereby also increasing the conductivity of the material via the relation:

\[
\sigma = e(n\mu_n + p\mu_p)
\]  

(2)

With \(\sigma\) being the conductivity, \(e\) again being the free-space charge of a single electron, \(n\) and \(p\) being the electron and hole carrier densities, respectively, and \(\mu_n\) and \(\mu_p\) being the electron and hole mobilities, respectively. The explanation for why this occurs arises from energy band theory of solid state physics. More specifically, it is informed by how the theorem of equipartition influences the k-space (a.k.a. Wave-Vector or Reciprocal Space) Fermi-Dirac distribution of the three-dimensional periodic potential model of a crystalline lattice. In simple terms, the Fermi-Dirac distribution is discretely shifted by roughly \(3/2k_BT\), which when taken alongside with the density of states for the given periodic potential, models that allowable electronic states become occupied above the chemical potential of the given material. This shift in the Fermi-Dirac distribution is displayed graphically in the figure below:
Figure 4: Shows Fermi-Dirac Distribution Multiplied by the Density of States as Temperature Increases (Note: Above Image is Using a 2-D Periodic Potential Model, as Denoted by the $k_B T$ Shift as Opposed to $3/2k_B T$, However the Main Point of Equipartition Remains Consistent) [9]

The shifting of this distribution in general indicates the number of electronic charge carriers that have made the jump from the valence band maximum to the conduction band minimum of the bulk Silicon. The explicit description of the derivation is as follows: Once the Fermi-Dirac distribution has been multiplied by the Density of States function, a summation of the resultant values must be made across all occupiable electronic quantum states, given by the Silicon Electron Dispersion Relation found in the figure below:
Figure 5: Shows Electronic Dispersion Relation of Silicon Within the First Brillouin Zone in 3-D \( k \)-Space Representation (Right), and the 1-D Projection Factoring in Energy (Left) [10]

Figure 5a is descriptive of the associated 1-D projection in \( k \)-space of the true dispersion relation found in Figure 5b. The projection was taken along the \(<100>\) family of lattice planes to match the plane of conduction being worked with in the final fabrication of the devices [10]. Given the continuum approximation applied to the discretely defined allowable energy states, one can approximate the above described summation as an integral. Taking this integral, and dividing the entirety of it by the given sample volume yields a number density, which is interpreted as the intrinsic carrier density of a given semiconducting system:

\[
n_i = \frac{1}{V} \int_{-\infty}^{\infty} f(E, T)g(E)dE
\]

(3)

With \( f(E, T) \) being the Fermi-Dirac distribution of form:

\[
f(E, T) = \frac{1}{e^{(E-E_F)/k_BT}+1}
\]

(4)
(With $E_g$ being the intrinsic band gap of the Silicon bulk, and $\mu$ being the thermally adjusted chemical potential of the Silicon substrate) As well as the associated Density of States function being broken down into two separate functions, one that is descriptive of the valence band characteristics, and one describing the conduction band characteristics at their respective maxima and minima regimes:

$$g_{VB}(E) = \frac{V}{2\pi^2} \left( \frac{2m_h^*}{\hbar^2} \right)^{3/2} \left( -E \right)^{1/2}$$

(5)

$$g_{CB}(E) = \frac{V}{2\pi^2} \left( \frac{2m_e^*}{\hbar^2} \right)^{3/2} \left( E - E_g \right)^{1/2}$$

(6)

With $V$ being the volume of the sample, $m_h^*$ and $m_e^*$ [11] being the spatially averaged effective hole and electron masses, and $E_g$ being the intrinsic band gap of the Silicon. Only the regions local to the band edges (specifically VBM and CBM-Valence Band Maximum and Conduction Band Minimum) are factored into the analysis here, as occupied electron states well below the VBM will always maintain their occupied nature, and unoccupied states well above the CBM will always remain unoccupied throughout the lifetime of the material, irrespective of the device being developed (This allows for a parabolic band approximation to be made, a backbone of the theoretical models demonstrated here). Now, if one were to apply each of the respective density of states functions to Equation (3) above, the two resultant numerical expressions would yield an intrinsic electron carrier density, $n$ (using Equation (5)), and intrinsic hole carrier density, $p$ (using Equation (6)). As these functions are both numerical in nature, to make them more readily solvable, a Boltzmann distribution is approximated in place of the Fermi-Dirac distribution. This approximation is valid for situations entailing that:
\[ \frac{1}{2} E_g \gg k_B T \]

Which even at 310K, remains valid. Thus, the Boltzmann distribution can be approximated, transforming the functions from numerical to analytical. Once analytical solutions have been found, the two resultant functions can be combined in accordance with the mass-action law, to form the final analytical function for determining the intrinsic carrier density for a given temperature:

\[
n_i = \sqrt{np} = 2\left(\frac{k_T}{2\hbar^2}\right)^{3/2}\left(m^* m^* \right)^{3/4} e^{-\mu/2k_BT}
\]

(7)

Where \( \mu \) is the thermally adjusted chemical potential of the Silicon material. The resulting value of this function, when all finite values were input (see Appendix F for numerical values), the resultant intrinsic carrier density was \( 1.16 \times 10^{16} \text{ m}^{-3} \) or \( 1.16 \times 10^{10} \text{ cm}^{-3} \), which is within a nominally expected range.

The energy band gap and chemical potential of the bulk silicon also varies depending on temperature. This can be modeled as the VBM being kept constant at zero energy, and the CBM shifting dependant on the electronic thermal interactions. In the case for the ISFET devices being made for this project, the CBM is modelled as shifting slightly downwards in terms of energy, as with the increase in temperature relative to room temperature, electrons in a quantum state at or near the VBM require less energy to make the jump to the CBM. The mathematical dependency for this occurrence is given as [12]:

\[
dE_g = \frac{-2e^2}{16\pi \varepsilon_0 \varepsilon Si} \sqrt{\frac{N_e}{\varepsilon Si}} e^{\frac{\mu}{e k_B T}} \left\{ 1 \right\}
\]

(8)
With repeated constants holding the same value as described before, $\varepsilon_{\text{Si}}$ and $\varepsilon_0$ being the relative permittivity of the bulk Silicon and the free-space permittivity, respectively, and $N_A$ being the acceptor concentration in the bulk material. One can see that a depedance on the background doping of the substrate material is present in the function, however that aspect is minimized in terms of it’s consideration as it was already known that a high concentration of p-type dopants was required, given the nominal subthreshold operation of the devices in their finalized form. By adding the resultant value of Equation (8) to the nominally accepted energy band gap value of 1.12eV, a more accurate CBM value was obtained of 1.1181eV. Then, there is the fact that the chemical potential of the material system will also be altered thermally. This parameter may be interpreted in the context of semiconducting material systems as median energy value between allowable electron and hole states. At 0K, the chemical potential is almost perfectly in the middle of the energy band gap, as is characteristic of semiconducting materials, but as temperature of the system increases, so does the placement of the chemical potential, again in terms of energy. The mathematical relation describing this variation is as follows [11]:

$$\mu = \frac{E_g}{2} + \frac{3}{4}k_BT\log\left(\frac{m^*_h}{m_e}\right)$$

(9)

Where $E_g$ is the 0K energy band gap of the material system. Equation (9) yields an energy value in terms of Joules, however converting to electron-Volts is required for the parameter’s incorporation into other descriptive equations. In doing this, it was found that purely by thermal influence, the chemical potential was increased from a nominal 0.56eV to 0.5645eV. While both the variations in CBM and chemical potential may seem small, when the two factors are taken into account together, large behavourial shift is exhibited relative to the context of an electrically
active solid-state device. These adjusted parameters will be used later in the model description when discussing the associated work functions of the material.

The final parameter considered in the model that is directly affected by thermal variation is that of the electron and hole mobilities. As the majority charge carriers present during subthreshold operation of the device are indeed the holes, the direct calculation of the hole mobility was made via the empirical formula [13]:

$$\mu_h = 54.3 \left( \frac{T}{300} \right)^{-0.57} + \frac{1.38 \times 10^8 T^{-2.33}}{1 + 0.88 \left( \frac{N_a}{2.35 \times 10^{18} \left( \frac{T}{300} \right)^{2.4}} \right)} \left( \frac{T}{300} \right)^{-0.146}$$

(10)

The hole mobility fits into the model in that it directly effects the minimum leakage, or $I_{d0}$ parameter, as well as effecting both the linear and saturation regime descriptive functions, which in turn directly effects the overall relation modelling the I-V characteristics of the devices in the subthreshold, linear, and saturation regions, respectively.

The next group of factors to be considered in the model development, is that of the work functions and their constituent potentials. The first factor involved is that of the adjusted electron affinity in the bulk Silicon substrate (energy difference between the CBM and vacuum potential). As has been demonstrated, the CBM is varied to account for the electronic thermal interactions in the crystalline structure, however due to this variation, both the substrate work function and constituent electron affinity must be varied in turn. To perform this variation, the nominally accepted electron vacuum affinity of Silicon (~4.15eV) was added with the absolute value of the resultant differential CBM given by Equation (8). This obtained a more realistic electron affinity (called qchi in the MATLAB script in Appendix F), which was then used to determine a more accurate substrate work function (called phi_s in the MATLAB script in Appendix F). As a nominal defining aspect of determining work functions associated with
semiconducting materials, the vacuum affinity is subtracted by the Chemical Potential (a.k.a. Fermi Energy in the context of metals). In order to do this, and simultaneously maintain consistency with other aspects of the model, the function [14]:

\[ \phi_S = q\chi + (E_{CBM} - \mu) + \phi_F \]

(11)

\[ \phi_F = V_t \ln\left(\frac{N}{n_i}\right) \]

(12)

With \( \phi_F \) being the bulk potential of the Silicon substrate. This may appear to be different in form to definitional work functions, where simply the difference in energy between the electron vacuum affinity and the chemical potential. The reasoning for this is that since the constituent elements in finding the substrate work function have themselves shifted, so has the perspective of the function. Now, the difference in energy between the CBM and the chemical potential must be added to the already adjusted electron vacuum affinity, in order to determine the net difference in their energies [14]. Performing the calculation in this manner factors in the thermal variation induced by nominally operating the devices at human body temperature, while the inclusion of the bulk potential term, linearly scales the vacuum energy based on the background dopant level in the substrate material, concluding in a much more accurately represented substrate work function (could also be perceived as the band structure shifting downwards in terms of energy). Figure 6, below will aide in giving a more visual insight into the above described phenomena:
With the above work function determined, it was then used to determine the flat-band voltage pertinent to the MOS stack of the device. As the flat-band voltage is in reference to the Gate-to-Body potential required to eliminate the band-bending phenomenon which arises from the Gate metal being in contact with the Gate oxide, leading to slight differences in charge between the metallized and substrate sides of the oxide.
The calculation performed is relatively simple, in that it is merely the subtraction of the contact metal work function (3.6-4.9eV for polycrystalline Titanium, \( \phi_M \) in Equation (13)) from the substrate work function determined via Equation (11) [14]:

\[
V_{FB} = \phi_S - \phi_M
\]

(13)

The next factor considered is the built-in charge due to depletion regions formed in the channel region of the device. There are effectively three different depletion regions formed here, one emanating from the MOS structure, and one from each of the pn-junctions formed by the n-wells diffused into the p-type substrate. In order to find this value, however, the true and effective widths of these depletion regions must be found in accordance with Figure 7, below:

![Cross-Sectional View of Standard Planar MOSFET with Depletion Regions and Effective Junction Depths (Depicted [16])](image)

In terms of the pn-junction depletion regions, the width going into the p-type region (substrate) can be found via the use of the nominal expression for pn-junction depletion widths, originally derived from Poisson’s equation for Electrostatic Potentials (under the Lorenz Gage):

\[
W_p = \sqrt{\frac{2V_{bi}N_D e N_A}{e N_A}} \left( \frac{N_D}{N_D + N_A} \right)
\]
With the built-in potential of the pn-junction being:

\[ V_{biPN} = V_t \ln\left( \frac{N_D}{N_A} \right) \]

As both n-wells involved are theoretically matched in terms of their doping and physical junction depths, the depletion widths found with Equation (14) will yield a nearly identical result for each. With this, the L’ parameter from Figure 7 can be found via taking the nominally designed for channel length of 10\(\mu\)m, and subtracting two times the found depletion width. The effective junction depth can now also be found, via adding the nominally designed for physical junction depth, to the width of the found depletion region. Next, is the depletion region of the MOS system. This is nominally present during subthreshold operation, and will not invert it’s composition until the threshold voltage is applied to the Gate contact (definitional of an inversion layer). This parameter can be found via the function [16]:

\[ W_d = \sqrt{\frac{4\varepsilon \varepsilon_0 \varepsilon Si (\phi_F + V_{BG})}{eN_A}} \]

With the \(V_{BG}\) parameter being representative of the Gate voltage relative to the applied Body voltage (nominally 0V, however can be varied with the physical design of these ISFET’s to adjust threshold voltage via this mechanism). Now, the built-in charge can be calculated via [16]:

\[ Q_{bi} = eN_A W_d \left( \frac{L + L'}{2} \right) \left( \frac{1}{L} \right) \]
Finally, the Gate Oxide Capacitance and Threshold Voltages can be determined via the respective relations [16]:

\[
C_{ox} = \frac{\varepsilon \varepsilon_{0} t_{ox}}{t_{ox}}
\]

(18)

\[
V_{th} = V_{FB} - 2\Phi_{F} - \frac{Q_{bi}}{C_{ox}} (1 - \sqrt{1 + \frac{2W_{d}}{r_{j}} - 1}) \left(\frac{r_{j}}{L}\right)
\]

(19)

With \( r_{j} \) being the effective junction depth found earlier, in accordance with the sketch of Figure 7.

Now that the model has these parameters solved, calculation and plotting of the different I-V relations in the different regions of operation may take place. For the subthreshold region, there are two main functions involved, one being that of the full equilibrium Drain Current, which models the current flowing through the device under complete zero-biasing, and the other being the explicit I-V relation [17]:

\[
I_{D0} = \mu_{h} C_{ox} (n - 1)(V_{t}^{2})e^{-V_{th}/nV_{t}}
\]

(20)

\[
I_{D-sub} = I_{D0} \left(\frac{W}{L}\right) e^{V_{GS}/nV_{t}} (1 - e^{-V_{DS}/V_{t}})
\]

(21)

With \( V_{GS} \) being the relative Gate-to-Source Voltage of the devices, \( V_{DS} \) being the relative Drain-to-Source voltage, and \( n \) being the slope factor of the devices, given by [17]:

\[
n = \frac{C_{ox} + C_{dep}}{C_{ox}}
\]

(22)
\[ C_{dep} = \frac{\varepsilon_{Si}}{W_d} \epsilon_0 \]  

(23)

For the linear operating region, the descriptive function is taken as:

\[ I_{D-lin} = \mu_e C_{ox} \frac{W}{L} \left((V_{GS} - V_t)V_{DS} - 0.5V_{DS}^2\right)(1 + \lambda V_{DS}) \]  

(24)

With \( \lambda \) being the experimentally determined channel length modulation parameter and \( \mu_e \) being the electron mobility, found via [13]:

\[ \mu_e = 88\left(\frac{T}{300}\right)^{-0.57} + \frac{7.4 \times 10^8 T^{-2.33}}{1 + 0.88(1.26 \times 10^{14} \left(\frac{T}{300}\right)^{2.4})} \left(\frac{T}{300}\right)^{-0.146} \]  

(25)

Lastly, there is the Saturation region I-V relation, presented as:

\[ I_{D-sat} = \frac{\mu_e C_{ox}}{2} \frac{W}{L} (V_{GS} - V_t)^2(1 + \lambda V_{DS}) \]  

(26)

The I-V equations were then set up using linear value sweeps of either the Gate-to-Source voltage or the Drain-to-Source voltage to create value matrices, which were then plotted in a piecewise fashion within MATLAB, thus allowing for immediate, direct comparison with any testing results obtained after the devices have been developed. This represents the bulk of the model, however there is one more aspect to it of high importance, that being the Subthreshold Swing parameter.

It is effectively a metric of slope in the linear and subthreshold operating regimes, which is indicative of the sensitivity of the device, and therefore how well it performs its transconducting action. This value is calculated by [18]:
\[ S_{s-th} = \ln(10)V_t n \]

And is of great importance in determining if the devices theoretically meet the desired sensitivity requirements.

**B. Array**

For the array specifically, since it will be made up of the single devices discussed in the previous subsections, there were relatively few additional considerations that needed to be made. The main consideration is that of the array’s electrical configurations, namely if it should be of a parallel or series nature. Ideally, the array would be entirely of a parallel nature, as for each parallel combination yields an effective doubling of measured drain current, and thereby would massively boost the overall sensing capabilities \[19\]. However, the downside of this is the complexity required to implement such a topology was deemed too great from both a fabrication and instrumentation perspective. The reasoning for this is that in a wholly parallel array containing upwards of 100 individual devices, an instrumentation amplifier would need to be attached to each device. As the entire eventual system would need to fit into something the size of a wristwatch, this is wholly unfeasible, as even if LSI or VLSI technologies were utilized to enable the extensive signal amplification, the thermal output from this many amplification units would exceed what is comfortable to the user, as well as rapidly drain the battery power source, necessitating that the user replace their device or recharge it much more frequently than is desired.

A wholly series electrical topology was also out of the question. It would reduce the instrumentation complexity, however, each series combination contained within an array of this type presents an effective halving of the total drain current \[19\]. Since the devices will be
operated in the subthreshold region, the drain currents will already be relatively small (nA-μA regime), and design considerations yielding in any reduction of the drain current would place it well below the noise floor, making any realizable instrumentation impossible.

As such, a combination parallel/series array was settled on, as low complexity instrumentation of a series array persists in this topology, as well as the effective doubling of the drain current that a parallel array provides. The only question remaining was how many series and parallel combinations should be developed? The solution to this was to conduct experimental tests to observe what would provide the best benefit and most accurate sensing. This entailed defining a tradeoff between maximal current throughput and surface area, as the more surface area available for ionic sensing, the more accurate the sensor would be overall. To do this, multiple array topologies were designed and fabricated, with an emphasis on having as many parallel combinations as possible, as the nature of them yields the highest net benefit in terms of maximal current throughput. All arrays were designed to utilize 34 parallel combinations, with as few as 2 series devices per parallel combination, and up to 22 series devices per parallel combination in order to determine the characteristics of this tradeoff, and the best end result.

C. Fabrication Process

a. Process Design

The very first step in the fabrication process is to determine the exact type of Silicon substrate (wafers) that will be used. There were some limitations involved in this decision making process, mainly that the wafers must be either PRIME or TEST grade (ideally PRIME grade to ensure minimal defects in the monocrystall), they must be 100mm in diameter, must be
Single-Side Polished (SSP), and must be 500 micrometers thick, with these last three limitations originating from the process capabilities of the fabrication facility. From this point the only other determinations to be made were that of the dopant type and resistivity of the substrate. As the FET devices were designed to utilize an effective Enhancement-Mode n-MOS type of operation, a p-type substrate was necessitated. The specific dopant type chosen was that of Boron, as there is vastly more literature on the effects of Boron doped Silicon than there is for other p-type dopants. Once this was determined, the resistivity was the only factor remaining. For this determination to be made, consideration of the desired device characteristics had to be factored in. Since the devices were to be nominally operated in the subthreshold regime, nearly all charge carriers involved in the production of a drain current were that of minority hole carriers. Since this is the case, the greater the number of holes in the bulk p-type region, the more efficient could the transconducting action of the devices be performed. As such, it was chosen to use wafers with a resistivity ranging from 1-10$\Omega$-cm. This way, there would not be any degenerate doping effects, and the semiconducting nature of the material could be wholly preserved, but there would be enough holes present to allow for the desired highly efficient transconducting nature. To summate, the wafers/substrates being used in the fabrication of the ISFET devices and arrays was chosen to be that of 100mm diameter, 500um thick, $<100>$ oriented, PRIME grade wafers, Boron-doped to a resistivity of $\sim$1-10$\Omega$-cm, sourced from UniversityWafer.

The next aspect of the fabrication process was the development of a customized overall process flow. As it is a rather lengthy process, the detailed flow will be presented in list form:

1. Clean Wafers in Pirahna Solution for $\sim$10 minutes (mix of highly concentrated Sulfuric Acid and Hydrogen Peroxide, heated to $\sim$70°C), BOE for $\sim$5 minutes (Buffered Oxide
Etch, highly concentrated Hydroflouric Acid and Ammonium Flouride mixed with a Buffering solute at room temperature), and finally with a full run in the SRD (Spin Rinse Dryer).

2. Perform Resistivity Metrology with 4-Point Surface Probe in order to determine the five best wafers to be used in fabrication (the lower the resistivity the better). Five wafers will be used per process run to better ensure successful device and array fabrication, and allow for any process errors or accidental breaking of a wafer.

3. Thermally Grow a Wet Silicon Dioxide (oxide) Mask on Selected Silicon Wafers at ~1100°C for ~2 hours and 15 minutes (see MATLAB script in Table 11 for calculation description).
4. Once wafers are fully cooled, rinse again in Piranha Solution for ~10 minutes and run through the SRD.

5. Spin-Coat Shipley S1813 Positive Tone Photoresist (PR+) onto whole of Wafer Surface using a 4000 RPM spin velocity.

6. Perform a Soft-Bake of the PR+ on a hot plate at ~100°C for ~2 minute.

7. Perform the first Lithography (Litho) Run using Photomask #1 on i-line Contact Aligner to isolate Source and Drain regions for use in localized doping of substrate material.

8. Once Lithography is complete, remove unwanted PR+ with CD-26 Devloper Solution at room temperature for ~3min, 30 seconds.
9. Etch exposed oxide mask with BOE for ~5 minutes at room temperature.

10. Remove Remaining PR+ with Microposit 1165 Solution at ~60°C for ~10 minutes, and perform a cleaning run through the SRD.
11. Spin-Coat Phosphosilicate Diffusant Solution and bake it at \( \sim 150^\circ\text{C} \) to drive-off excess solvent.

12. Perform Thermal Diffusion of the Phosphorous Dopant as a Pre-Deposition step at \( \sim 1000^\circ\text{C} \) for \( \sim 2 \) hours. During this step, most of the Phosphorous dopant will be substitutionally embedded into the Silicon lattice in the specified n-well regions at a depth of \( \sim 6\text{nm} \). These locally n-type wells are the Source and Drain of the FET devices (see MATLAB script in Table 11 for explicit calculations).
13. Once wafers are completely cooled, do another cleaning process containing a dip into ~70°C Piranha Solution for ~10 minutes, a dip into BOE for ~30 minutes at room temperature to remove the oxide masking layer, then perform a run through the SRD.

14. Thermally grow a Dry Silicon Dioxide layer of ~10nm at 900°C for ~30 minutes for use in both interconnect substrate isolation and Gate Dielectric (see MATLAB script in Table 11 for calculation description).
15. Once wafers are fully cooled, dip into a ~70°C Pirhana bath for 10 minutes to eliminate any organic contaminants that may arise in the oxidation process.

16. Spin-Coat a new layer of Shipley S1813 PR+ and soft bake on a hot plate at ~100°C for ~2 minutes.

17. Perform second litho run again using Photomask #1 with i-line Contact Aligner to again isolate the Source and Drain regions such that they can be metallized in following steps.
18. Place wafers in PR+ CD-26 Developer solution for ~3 minutes and 30 seconds to remove any unwanted PR+.

19. Etch the Oxide in BOE for ~6 seconds to remove any unwanted oxide from the Source, Drain and Body contact regions.
20. Remove any remaining PR+ using ~60°C Microposit 1165 solution, and run the wafers through the SRD.

21. Perform a DC Physical Vapor Deposition of Chromium, Silver, then Chromium again in a thickness ratio of roughly 7nm:20nm:3nm. This combination of metallic materials will form the Source, Drain, and Body contacts, as well as the device interconnects for the arrays. The reasoning for this combination of materials is that Chromium provides excellent adhesion to both Silicon Dioxide and Silicon Nitride, with minimal electromigration issues arising upon the devices heating up, whereas Silver provides an excellent electrical conductivity. Having the materials sandwiched in such a way in theory provides a good balance between electrical conductivity and adhesion/structural stability.
22. Spin-Coat another layer of Shipley S1813 PR+, and soft bake again using the same parameters as before.

23. Perform the third litho process, this time using Photomask #2 with i-line Contact Aligner to pattern contact metallization and array interconnects.
24. Again remove unwanted PR+ with CD-26 Developer solution at room temperature for ~3 minutes and 30 seconds.

25. Etch away any unwanted Chromium and Silver by dipping the wafers into room temperature Chromium Etchant for ~5 seconds, room temperature Silver Etchant for ~10 seconds, and again into the Chromium Etchant for ~10 seconds.
26. Strip away remaining PR+ with room temperature Microposit 1165 solution for ~10 minute, and run wafers through the SRD.

27. Perform a Reactive RF Physical Vapor Deposition (RPVD) of Silicon Nitride (nitride) to ~100nm thick using.
28. Spin-Coat another layer of Shipley S1813 PR+ and soft-bake with the same parameters as before.

29. Perform another litho run using Photomask #3 with i-line Contact Aligner to pattern contact pads and gate region for precise Nitride removal.
30. Remove unwanted PR+ with room temperature Developer solution for ~3 minutes.

31. Etch Nitride in Phosphoric Acid bath heated to ~150°C for ~10 minutes.
32. Clean any remaining PR+ with room temperature Microposit 1165 solution for ~10 minute, and run wafers through the SRD.

33. Perform another PVD process, this time using Titanium and Silver with constituent thicknesses of 20nm:6nm. These two materials are used here as Titanium has great adhesion to oxide, as well as relatively good electrical properties. It also avoids migration issues into the Gate Oxide, as well as being thermally and physically robust,
ensuring that the dielectric properties maintain over the lifetime of the device. Silver is coated on top of the Titanium with the sole purpose of providing an optimal substrate for the eventual selectivity layer that will be placed on the devices in future.

34. Perform final Spin-Coating, this time with Ma-n 1420 Negative-tone Photoresist (PR-), and perform a soft-bake with the same parameters as were previously done.
35. Perform final litho run, again using Photomask #3 with i-line Contact Aligner to pattern metallization of contact pads and gate region.
36. Remove any unwanted PR- with room temperature Developer Solution.

37. Etch any unwanted Silver and Titanium with respective etchants and run through the SRD to remove any remaining etchant.
38. Perform final cleaning steps by stripping away the remaining PR- with Microposit 1165 solution, and do a final SRD run.

39. Finally, use Die-Cutter to isolate individual die on the wafer, such that individual arrays and devices can be tested.

This process flow allows for a good balance between manufacturability, process yield, and physical robustness of the constituent devices by utilizing strong materials and the overall relative brevity of the fabrication process. While the processes described above are not novel in their own right, and the individual processing methodologies described above were fairly well characterized before the fabrication of the ISFET devices and arrays, the overall flow is highly customized, with an emphasis placed on manufacturability.

With the overall process flow defined, some constituent processes required their own design aspects, mainly that of the photomask patterns (masks). As can be observed from the above list, only a total of three photomasks ended up being required to complete the fabrication
of the design, even though there are five different lithography processes. This alone was a relatively challenging feat, as in many cases, a new photomask for each of the lithography steps is required. The mask patterns were developed as a set of 2-D Layered Object Groups in Autocad, and once they were completed, the CAD files were sent to CAD Art Services in Oregon for the actually manufacturing of the mask. The patterns were set to be of the transparency type, utilizing 20,000 DPI printing, as this provided a good cost-savings over more expensive Chrome-on-Glass masks. The Autocad layout with all three mask patterns overlaid is shown below in Figure 9, to give a general idea of the scope:

![Autocad layout](image)

Figure 9: Shows ‘Life-Sized’ View of all Three Photomask Patterns Overlaid in Autocad
The individual devices, as mentioned before will have an overall geometry of 50 micrometers by 100 micrometers, with the Gate region alone being 10 x 100 micrometers, and each of the Source and Drain n-wells being 20 x 100 micrometers. Implementation of this in terms of the mask patterns is shown below:

*Figure 10: Shows Top-Down View of Photomask Pattern of a Single ISFET Device*
Where the Blue colored rectangle can be interpreted as the Gate Region, the two Yellow rectangles can be interpreted as the Source and Drain Regions, and the Green colored rectangles represent where metallized interconnects will be present to connect the device to larger contact pads for measurement probing. The reasoning behind the different coloring is that each element was fabricated at different points in the process, utilizing different photomasks—see above process flow list for usage timeline. In order to create the individual features shown in Figure 6, it was necessary to develop three initially separated patterns, representative of each layer shown above. Each of the individual layers corresponded to their associated processing step, namely fabrication of the Source and Drain n-wells and Gate Oxide for the initial, Yellow colored mask, then the second, Green colored mask for the interconnect metallization, and lastly the Blue colored mask for the Gate and Body contact metallizations, all maintaining the feature sizes described in Figure 10. Once each of the individual masks were completed, with a rough alignment between each masks ensured via the creation of alignment markings present on each die, all three pattern layers were overlayed in Autocad, where precise alignment was made. Once this was completed, a final check on the alignment was made across all dies, and the CAD files were sent to CAD Art Services for their production.

One may note that there were many different types of devices and arrays present throughout the different dies shown in Figure 9. Since it was known that there was going to be some experimentation required of the final devices, namely the characterization of the Body Effect in the arrays, and the determination of the best specific size of the array, many different test devices were required to be fabricated at once, necessitating the differing designs within the mask patterns, as can be seen in Figure 9, above. To characterize the body effect, it was decided to fabricate single devices with their body contacts having variant separations relative to the
main active region of the device. This distance was varied in roughly 1 millimeter increments from a nominal 100 micrometers, up to 4.4 millimeters, as this is the maximal distance at which the body effect must be felt in order for all ISFET devices in the arrays to exhibit a uniform biasing. As can be seen in Figure 9, at least three dies worth of wafer space was used to develop the devices with different Body contact spacing, this was done simply to increase the probability of the process yielding a successful device, as even with the best of CMOS fabrication processes, there are always some nonuniformities or irregularities across the wafer. Note that the devices with Body Contact spacing of 100 micrometers will be considered the nominal devices during the testing phase.

Figure 11: Shows Example of Nominal ISFET Single Device with Minimum Distance to Body Contact Shown

Figure 12: Shows Example of Nominal ISFET Single Device with Maximum Distance to Body Contact Shown
As for the determination of the specific array size, multiple different series/parallel configurations were developed across the bulk of the available die space. These are shown in Rows 4-9 in Figure 9, with each row constituting an increase in series combinations in the arrays. As mentioned before, all arrays developed have the same number of parallel combination, due to the more favorable electrical features that parallel FET arrays provide. The reason behind why so many arrays of each size were developed was to ensure that the process outcome would yield at least one fully successful array. The number of series combinations ranged from 2 FET devices in series per parallel combination (shown in Figure 13), up to 22 series FET devices per parallel combination (shown in Figure 14), with an incremental increase of 4 FET devices per parallel combination. This incremental growth will allow for a great deal of characteristic testing to take place, in that there will many data points to consider in the determination of sizing tradeoffs. One feature that was kept uniform across all of the arrays is the spacing for the electrical contact pads. It was required that they remain relatively far away from the active regions of the arrays in order to facilitate electrolyte testing while not shorting the Source, Drain, and Body contacts, of course invalidating any results. This is demonstrated below in Figures 13 and 14, originating from the overlaid photomask patterns developed in Autocad:
Figure 13: Shows ISFET Array Containing 2 Series FET Devices Per Parallel Combination
Figure 14: Shows ISFET Array Containing 22 Series FET Devices Per Parallel Combination

Once the photomask patterns were fully developed, the CAD files were sent to CAD Art Services for them to generate the proofs. Proofs were sent back to us in roughly two weeks'
time, and are displayed below, as the monochromatic aspect aides in the visualization of the z-stack process flow:

(a)
These mask proofs are directly in accordance with the above described design, wherein the mask pattern from Figure 15(a) is used for both generating the Body, Source, and Drain n-wells via the patterning of the diffusion mask, as well as aligning the Gate insulating oxide in
accordance with the previously patterned n-wells (Note: White colored regions are transparent on the physical mask, and in accordance with the nature of positive-tone photoresist used in these steps, represent the regions that will be etched, this is true for all mask images presented used in all lithography steps, aside from the final run of photolithography).

Figure 16: Shows Zoomed-In View of Single ISFET Device on First Photomask Proof

The mask pattern from Figure 15(b) patterns the deposited metal layer, to be used for creating the interconnects between the Source, Drain, and Body contact pads and the physical Sources and Drains, as well as provide interconnects between the devices formed in the various array types developed.

Figure 17: Shows Zoomed-In View of Single ISFET Device on Second Photomask Proof
Finally, the mask pattern of Figure 15(c) depicts the patterning of the etch mask for both the Nitride Etch step, as well as the Gate and Body Metallization steps. Wherein the Nitride Etch uses a Positive-Tone Photoresist (Shipley S1813), and the Gate Metallization step uses a Negative-Tone Photoresist (Micro Resist Technology ma-N 1420). This is important to keep in mind here, as by flipping the tone of the photoresist between the etch steps, as where positive-tone resist is used, the white-colored regions of the photomask will be etched, and with the negative-tone resist, everything except for the white-colored regions will be etched.
Figure 19: Shows Zoomed-In View of Single ISFET Device on Third Photomask Proof

Figure 20: Shows Zoomed-In View of ISFET Array on Third Photomask Proof
Following the receiving of the photomask proof images, they were officially purchased, and once the physical transparency masks were in-hand, the device and array fabrication could commence in accordance with the process flow detailed above.

b. Process Conduction/Fabrication Notes

The fabrication of these devices and arrays ended up not going as smoothly as initially hoped for. There were a multitude of equipment and materials issues that arose throughout the process, leading to the unfortunate circumstance of the devices not being able to be completed within the timeline of the project. As this is the case, this section will focus on processing steps actually taken with photographic support, the respective reasoning behind them, as well as descriptions of what went wrong, and fixes/workarounds implemented in an attempt to have some level of device completion.

Steps 1-16 went as expected, with only minor issues such as a layer of photoresist not properly adhering to the substrate layer, necessitating the removal of the non-exposed resist with acetone, and simply reattempting the spin-coating process. This was largely due to both the HMDS based Primer 80/20 and the Shipley S1813 Positive Tone Photoresist being expired by at least two years, inducing chemical degradation and minimizing their effectiveness. While this was annoying at times, it was an expected potential issue, and did not cause any major processing delays. A brief recap of the processes contained within the first 16 steps will now be shown, with any relevant fabrication notes applied. The initial wafer cleanings in heated Piranha Solution, room temperature BOE, and a run through the SRD all went extremely well, with no inadvertent errors to speak of:
Resistivity metrology also went fairly well, at the point in time where this step was performed, the probe station set up in the lab was utilizing very old equipment, specifically a very old DC PSU and probe:
While these led to a fairly high measurement error (+/- 10%), approximate resistivities were still able to be obtained, such that the most preferable devices were able to be picked out (explicit raw data shown under Testing Results Section, below). As the wafers with the lowest resistivity were the most optimal in terms of the desired electrical characteristics, wafers number 12, 17, 18, 19, and 21 were selected for the full run of processing. The reasoning behind why only five total wafers were selected for the entirety of the processing was that attempting to run all 25 wafers through the desired fabrication would take much too long in a mostly manual facility such as the one being worked in. Since that was known, it was chosen to have at least three whole wafers worth of fully fabricated devices, such that the probability of having a working device at the end of all of the processing would be relatively high. By choosing to start with five wafers, this would also allow for up to two wafers to completely break during the processing, and still be able to net three functional device wafers.

The next step in the processing was to thermally grow a wet oxide layer (called ‘wet oxide’ due to the furnace chamber being flooded with steam during oxidation, as opposed to pure O₂). To do this, the wafers were loaded into a quartz boat with dummy wafers placed at each of the far ends of the boat in order to help diffuse the incoming gasses uniformly throughout the chamber, and with polished sides facing other polished sides, unpolished sides facing other unpolished sides, as is fairly common practice to enable higher uniformity of the oxide during the growing process:
Since the oxide diffusion mask was fairly independent of thickness (as long as it was thicker than \(\sim 10\text{nm}\)), they were loaded into the furnace with another fab user’s wafers, as the process they needed to run would yield an approximate oxide thickness of \(\sim 450\text{nm}\), clearly plenty thick for the application needed of them. The wafers were then loaded into the furnace as it reached 900°C, while flooding the chamber with high purity N\(_2\) gas, such that no oxidation could occur. Once the furnace reached the nominal temperature of 1100°C, the chamber was flooded with wet O\(_2\) (steam), such that the oxidation process could begin. The furnace was then held at that temperature for \(\sim 1\) hour with the wet O\(_2\) flowing. Once the hour had elapsed, N\(_2\) was then flowed into the chamber as it cooled, until it reached a temperature of 800°C, wherein virtually no oxidation would occur, even when exposed to oxygen. The furnace was then allowed to finish cooling to room temperature overnight, and then next day, the wafers were pulled out and the oxide layer thicknesses were measured using the Filmetrics Optical Profilometer found in the Microfab (Raw data from Optical Profilometry given in Testing Results Section).
Next was to perform the first photolithography step, in order to pattern and etch the two n-wells such that they could be doped down the line. This process went exactly according to plan, as there was no alignment needed due to these features being the first to be printed onto the wafers (the truly difficult component to photolithography). The process was fairly simple, as it was merely a matter of Spin-Coating the HMDS based Primer at 3000RPM for 20 seconds, followed by the S1813 Photoresist at 4000RPM for 30 seconds (as per nominal pre-characterized process, yields ~1.4μm resist thickness) after carefully centering the wafers on the vacuum chuck of the spin-coater, performing a soft bake at 100°C for 2 minutes on a hot plate, cooled on a cold
plate, then placing the wafers into the Quintel/Gamm i-line Lithographic Aligner once the transparency mask was mounted to piece of glass via Double Sided Scotch Tape, followed by a 2 minute bath in CD-26 Developer Solution. This yielded excellent results considering the use of transparency masks versus chrome-on-glass photomasks, which provide much sharper, more accurate lithographic printing.
Figure 25: Primer (Left) and S1813 Photoresist Used (Right) (a), Manual Wafer Centering in Spin-Coater (b), Wafer in the Middle of Spin-Coat Process (c), Soft-Baking Wafer on Hot Plate (d), Wafer on Cold Plate (e), Chromatic Abberation Induced by Photoresist Film (f), First Transparency Mask Mounted on Glass (g), Quintel/Gamm i-line Contact Aligner (h), Post-Lithography Wafer Developing in CD-26 (i)
With the patterning of the n-wells developed, the etching of the oxide masking layer could commence. As the oxide was measured to be roughly 450nm in thickness, and the BOE used in the laboratory has an oxide etch rate of ~100nm per minute, an initial 4 minute soak in the BOE was performed (this was to ensure no overetching of the oxide layer). This worked very well for wafer #19, as it had etched perfectly, however the other wafers involved required a bit more time, which is due to slight thickness variations of the oxide layers between the wafers. As such, the other wafers were soaked for another minute, which was found to completely etch away the desired regions. Once satisfactory oxide etching was achieved, the wafers were ran through the SRD, then placed into 60°C Microposit Remover 1165 Solution for 10 minutes in order to remove any persistent S1813 Photoresist present on the wafers.

Figure 26: Shows Photoresist Patterning on Oxide Layer (PR is Green, Oxide is Orange) (a), Wafers Placed in BOE for Oxide Etch (b), Post Oide Etch Pattern (White Now Being Bare Silicon) (c), Wafers Placed in 1165 Remover (d)
At this point, another small problem arose in that the 1165 Remover was not fully striping the wafers of the S1813 resist. This was mainly due to the solution the lab had on-hand being about three years expired, naturally losing it’s potency. The solution to this was to run the wafers through an O₂ RIE (Reactive Ion Etching) process, consisting of a 27mtorr (+/- 3mtorr) Base Pressure, 310mtorr (+/- 5mtorr) Process Pressure, and 300W (+/- 5W) Forward Process Power (at 13.56MHz signal frequency) for roughly two minutes (Note: These Process parameters remained consistent for all O₂ RIE processes performed during project). Doing this process has the benefit of almost guaranteeing that any remaining photresist was removed while leaving any non-organic materials undisturbed, but unfortunately added roughly 25 minutes of time per wafer to the entire process. Since the lab was unable to obtain fresh 1165 Remover during the timeline of the project, this RIE process was necessitated every time photresist needed to be removed. The only exception to this was after any metal layers were deposited, as this RIE process can induce high enough thermal and mechanical stresses in metallic films that they could end up fracturing, which is extremely undesirable.
Once all of the remaining S1813 was removed, the wafers were then spin coated with Filmtronics P507 Phosphosilicate Diffusant using a similar process to the S1813 resist spin-coating, albeit at 5000RPM and with a 115°C bake for three minutes on the hot plate, to drive off any excess solvent. Unfortunately, at this point in the process, wafer #19 broke as it was being dried off with an N₂ gun. There was no obvious cause of the break, other than potentially high mechanical stresses induced by blowing on the wafer with the pressurized N₂. While an unfortunate (and expensive) circumstance, it was somewhat planned for, so it did not cause any delays in the process overall. Once the wafers were coated with the diffusant, they...
were then placed in another quartz boat in the same configuration as before, in order to prepare them to enter the diffusion furnace in the lab. Once the furnace reached 900°C, the wafers were slowly loaded in, to prevent any thermal shock. The furnace then had dry O₂ flowed into it, in order to minimize potential reactivity with the diffusant film, and was ramped to 1000°C. The furnace was left at this temperature for roughly two hours, in accordance with the developed process. At this point, the O₂ gas flow was stopped and the furnace was allowed to cool overnight.

(a)  
(b)  
(c)
The next day, the wafers were taken out of the diffusion furnace, then placed in BOE for roughly one hour. This step may seem excessive given that BOE has an etch rate of 100nm per minute, and the oxide film was only ~450nm, but during the diffusion process, the oxide layer also undergoes some level of doping, and the result of this process is that the BOE has a much more difficult time chemically removing the Oxygen atoms from the film. As this is the case, and BOE will effectively not etch the underlying Silicon at all, the simplest course of action was to leave the wafers in the BOE for as long as possible to ensure all oxide removal. The wafers were then run through the SRD for cleaning, and dipped again in Piranha solution heated to ~70°C for 10 minutes, followed by another BOE dip, this time for one minute, and another SRD run. This prepped the wafer for the next step, being the growth of the Gate oxide material.
Since the Gate oxide grown needed to be so thin in order for the electrical aspects of the device to work properly as designed, a relatively low temperature oxidation process was required. For this run, the prepped wafers were again placed in a quartz boat, and loaded into the oxidation furnace at 900°C, as before. However, this time, the furnace was kept at this temperature throughout the process. After the wafer were slowly loaded into the furnace, dry O₂ was flowed into the chamber, in order to grow a more physically and electrically robust oxide, as a benefit of dry grown oxides is a lower relative permittivity when compared to their wet grown counterparts. The dry O₂ was flowed for roughly 30 minutes in accordance with the Deal-Grove
Model for thermal oxidation of Silicon (explicit calculation provided in MATLAB Script in Table 11 in Appendix F). Once the 50 minutes was over, N\textsubscript{2} was flowed as the furnace slowly cooled, until it reached 800°C. From here, the furnace was again left to fully cool overnight. The next day, the wafers were taken out of the furnace and an attempt was made to measure the film thickness using the optical profilometer used before. Unfortunately however, the Filmetrics unit available in the lab was not able to measure length scales as small as the film theoretically was, so no useful data could be gathered there. There was one other option to use as a quick check to make sure that oxide was indeed present, via performing a another 4-point probe sheet resistance measurement. In this fashion, if the sheet resistance was measured to be any higher than 100Ω, it could be said that at least some oxide was present, as the largest measured sheet resistance measured in the initial wafer characterization phase was ~80Ω. This is especially true as the wafers had been degenerately doped to form the n-wells and ohmic body contacts [20], which would theoretically decrease the overall observed sheet resistance. One added factor to this new test was that the probe station had undergone a minor overhaul between the initial wafer characterization and the Gate oxide test, in that I changed out the old DC PSU and Agilent multimeter for a Kiethley Sourcemeter, as it has the built-in capability for 4-wire sensing. This did not affect the results however, as both setups were comparatively tested using a reference wafer of known sheet resistance, with the Sourcemeter setup being slightly more accurate. Once the test was conducted, it was found that the oxidized wafer had a sheet resistance of ~68kΩ, which was clearly indicative of some oxide being present. While this was far from a perfect film characterization, it was what was available at the time, and was thus taken as proof of a ~10nm oxide layer being present.
Once taken out of the furnace, the wafers were soaked in 70°C Piranha solution for ~10 minutes to ensure no organic particulate had gotten onto the surfaces, followed by an SRD run. Then, the wafers were spin-coated using the nominal process detailed earlier for the S1813 resist to prep for the first proper alignment. Once this was completed, the wafers were put back into the Quintel/Gamm contact aligner with the same photomask as before in order to prepare to properly etch away any oxide present on the Source and Drain regions, as well as the Body contact region. At this point, it was found that an actuator in the aligner, responsible for focusing the microscope built into the system had broke. Without this actuator working, it was near impossible to accurately see the mask and wafer underneath it, which is very necessary when performing manual alignment this fine. Since the company that made the specific actuator had gone out of business over a decade ago, it was not possible to find a suitable replacement, so my
advisor (Professor Hawkins) and I had to fix it ourselves, which delayed the project by roughly a week. Once this issue was resolved, it was noticed that the resist being used was being underexposed after looking at it under an optical microscope. It was realized that the Mercury bulb UV source had started to degrade, and no longer gave the proper dose when paired with the previously used 6.5 second exposure time. As such, the exposure time had to be increased to roughly 9.5 seconds. From here, proper manual alignment could be conducted, and the oxide mask was etched via a 6 second BOE dip followed by a SRD run, after a ~3 minute development period in CD-26 developer. There were some adhesion issues at this stage in the processing as well as some issues with alignment, largely due to me needing to get used to the operation of the aligner, which ended up taking another week to rectify.

(a) (b) (c)

Figure 31: Wafers Immediately After Pulling Them Out of The Oxidation Furnace (a), Wafers After S1813 Spin-Coat (b), Optical Microscopy View of Aligned and Etched Gate Oxide (c)
The next process ran was that of the first metallization layer, consisting of Chromium, Silver, then more Chromium. Since films as thin as the ones desired (~30nm total z-height) had not been attempted before in the microfabrication facility being used, a Kapton Tape test was performed. The test was done by sputtering on the initial Chromium layer for 10 second, followed by the Silver layer for 20 seconds, with a final Chromium sputter for another 10 seconds, all at a Base Pressure of $7 \times 10^{-6}$ torr (+/- 5%), Process Pressure of $2.3 \times 10^{-3}$ torr (+/- 1%), and applied DC Power of 100W (+/- 0.1%). As the sputter system being used does have two magnetron guns in the chamber, this entire process was performed in-situ. Once the chamber was vented, the Kapton strip was pulled up at a 90° angle, and the film thickness was tested using the Ambios Stylus Profilometer available in the laboratory. The film thickness ended up being ~40nm (+/- 5nm), which was slightly too thick for the desired specification. As such, it was settled on using the process of a 10 second initial Chromium sputter, followed by a 20 second Silver sputter, and finishing with a 5 second Chromium sputter. The sputtering itself in this stage went quite well, as did both the resist spin-coating, alignment (now with the second photomask), exposure, and development. However, when it came time to etch away the deposited metals, it was found that the Silver Etchant used (Transene TFS) had much too high of an etch rate for a film of this thickness (20nm per second). The result of which was that for all of the wafers processes, despite best efforts, the top Chromium layer was severely undercut, and the Silver material was nowhere near the physical devices. Due to this, a new plan had to be set in place. While it was not the best in terms of device design, it was settled that attempting a ~30nm purely Chromium layer would be best in terms of rapidity, as at this point, there were only 3 weeks left before the project had to be completed, with much work remaining to be done. So, the initial metal films were completely stripped away using the same etchants (Transene 1020AC
for the Chromium), and a new Chromium layer was sputtered onto the wafers for one minute, at otherwise similar process parameters.
The wafers with the new purely Chromium films on them were then ran through the typical lithographic process, as detailed before with no issues to speak of, and resulted in an excellent looking film and alignment. Once this was done, the Chromium layer was etched using Transene 1020AC etchant, which has an etch rate of roughly 3.2nm per second. As this was one chemical solution that had not yet expired, the etch rate held true. The etchant was diluted in a
2:1 ratio (2 parts etchant to 1 part DI water) in order to halve the etch rate, and increase the probability of a successful etch.

![Images](a)(b)(c)(d)

*Figure 33: Singel Device Photoresist Patterning for Chromium Etch Step (a), Array Photoresist Patterning for Chromium Etch Step (b), Large Array Patterning After Chromium Etch (c), Small Array Patterning After Chromium Etch Step (d)*

The next step in the process would have been to Reactively Sputter (RPVD) Silicon Nitride onto the wafers for use as both a dielectric and passivation layer, however the Nitride Process could not be fully developed in the time required. Before the project had started, the microfabrication facility did not have a Nitride process of any kind, be it RPVD or CVD (Chemical Vapor Deposition), so I needed to develop one. Performing the process via CVD was not feasible due to the lab not having the necessary equipment, however all of the equipment was there for an RPVD process. Technically speaking, this is a more desirable process when depositing Nitride films, as it allows for tighter control over the film stoichiometry, as well as
fewer Hydrogen impurities are made a part of the film. Therefore, it was a matter of repairing the broken RG393 Coaxial Cable, Impedance Matching Network Controller, plum the RF Generator (ENI OEM-12B), and characterizing the process in terms of both deposition rates and film stoichiometry. This aspect of the project was worked on throughout it’s entirety, by both myself, and Professor Hawkins, and while we did end up getting it to work, it was not until the final week of the project that we were able to perform the Cal Poly Microfabrication Facility’s first Nitride deposition. While this was a large success in it’s own right, there was not nearly enough time left for the process characterization to be done, let alone have the process be included in the device fabrication. This was highly unfortunate, as it meant deviation from the original design plan, as well as taking a lot of valuable time.

Figure 34: Result of Cal Poly’s First Successful Nitride Deposition Process
Knowing that a Nitride film could not be included in the actual fabrication, a workaround had to be developed. As time was minimal, and much of the process and photomask designs had already been tailored with the assumption of a Nitride deposition, there were relatively few potential options that could be enacted. The process chosen to be ran was that of PHPR, or Plasma Hardened Photoresist. This was also a new process in terms of the specific fabrication facility, but all of the equipment needed for it was already working. So, after finding some nominal PHPR processes used in other facilities, I tested the process on two dummy wafers by spin-coating them with S1813 photoresist, using the nominal process, this time performing the soft-bake at 115°C for 90 seconds, as well as a hard-bake post development at the same temperature and time. The wafers were then placed in the RIE using the same process pressures as the previously described O₂ process, however this time, at 45W RF Forward Power, and for only 20 seconds. It was found that in doing this, roughly one micron of the resist material was removed from the wafer, and the sheet resistance skyrocketed relative to what it was after the hard-bake (see Testing Results section for raw data), due to the remaining top few nanometers of the photoresist having the constituent Novelac resin cross-linked, and mechanically hardened. This theoretically made it a viable option for moving forward, as it would allow for at least a version of the originally designed devices to be completed and then tested.

Figure 35: Shows Profilometry Results for PHPR Process Testing
From this point, the PHPR process was performed on the device wafers using the third photomask pattern, where they were immediately sent for a final Chromium sputter to act as the Gate metal. Originally, the designed called for a film of Titanium, then Silver to be sputtered onto the wafers here, but as there were merely days left on the project, it was more important to get some testable devices made, and since the work functions of polycrystalline Titanium and Chromium are fairly comparable, this would not have altered the device characteristics in any meaningful way, electrically speaking. The wafers were then sputtered with the Chromium for 6 minutes to ideally achieve a ~250nm film. This layer had to be relatively thick, since the PHPR layer is much thicker than the originally designed for Nitride layer, and PVD processes are typically non-conformal. The final major issue arose in this stage, wherein once the wafers were removed from the PVD chamber, large, flakey pieces of Chromium were present. This was not good at all, as it meant the true thickness of the film could not reliably be known, and it would make spin-coating anything, such as photoresist nearly impossible. The theory for why this occurred is that once the sputtering process was started, bombardment of the Chromium atoms was done with a high enough energy to perform a partial etching of the underlying PHPR layer, wreaking havoc on the rest of the sputtered film. This theory was given some evidence behind it, as an etch process was attempted after a lithography process using ma-N 1420 Negative-Tone Photoresist and ma-D 533/S Developer Solution. The spin-coat followed the exact same process as for the S1813 resist, with a 160°C soft-bake for two minutes, as per the resist datasheet. As it was a negative-tone resist, the exposure time had to be increased to 44 second, again, as per the datasheet, with the development time of two minutes and ten seconds. This did not end up being effective, however, as the flakiness of the Chromium layer caused the resist film to be highly non-uniform, leading to issues in the development phase, as well as made proper alignment
completely impossible on some of the wafers due to alignment markers appearing blown up. There were still two wafers (#12 and #21), however, where proper alignment could be made, and as such, once the lithographic process was done, these two wafers underwent an attempted Chromium etch. Due to the poor development of the resist induced by the flakey Chromium layer, the etch was highly non-uniform, yielding Chromium flake remaining on the wafer, even well after the theoretical etch time was passed. It was noticed at this stage as well, that underneath the Chromium top layer, that bare-looking Silicon was left on the surface in some regions, as opposed to the PHPR that should have been there, indicating its unwanted removal.
This, unfortunately was the final state that the device wafer were left in, as there was no
time to go back and correct any aspect of the wafers, even though the Nitride process had just
become operational. As such, no proper electrical testing of the devices could be made, as the
remaining Chromium layer would effectively short all contacts, making any gathered data wholly
unusable. As brief summation of the alterations made to the device design due to the various
described issues, new cross-sectional sketches were developed and will be presented here, starting from processing step #21:

21) Deposit ~30nm layer of Chromium via PVD:

22) Spin-coat PR+ using nominal process:
23) Perform Alignment and lithography using photomask #2:

![Diagram of alignment and lithography process]

24) Develop PR+ in room temperature CD-26:

![Diagram of development process]
25) Etch Chromium layer with Transene 1020AC at room temperature for ~10 seconds:

26) Strip remaining PR+ with Microposit Remover 1165 at ~60°C for ~10 minutes:
27) Spin-coat PR+ using nominal process:

28) Perform alignment and lithography on new PR+ layer, using photomask #3:
29) Develop in room temperature CD-26 solution and hard-bake PR+ layer:

30) Perform O$_2$ Plasma Hardening of PR+ layer:
31) Deposit the final Chromium layer:

32) Spin-coat Negative-Tone Photoresist (PR-):
33) Align and perform lithography on PR- layer again using photomask #3:

34) Develop PR- in room temperature ma-N 533/S Developer for ~2 minutes:
35) Etch patterned Chromium layer:

![Diagram of Chromium layer etch process]

36) Remove remaining PR-layer:

![Diagram of PR-layer removal process]
IV. Testing Methodologies

A. Process Metrology

There will be a few key measurements that must be made throughout the fabrication process. These measurements will not only increase the likelihood of a successful fabrication run, but also allow for any errors in fabrication to rectified immediately, and aide in any fault analysis if need be. The first type of metrology that will be utilized here is that of a sheet resistance measurement using a four-point probe technique. This is one of the initial steps in the fabrication process as a whole, as it’s purpose is to inform which wafers should be used to have a higher likelihood of obtaining the desired results. In this case, the lower the resistance the better (to a point), which is indicative of more holes present in the lattice structure (holes and not free electrons as the wafers being used were p-type background doped), which is directly related to the magnitude of the drain current relative to any applied biasing, as in the subthreshold region, the minority carriers (in this case holes) conduct the majority of the current. This measurement technique was used a few times throughout the fabrication of the device, mainly to analyze if material coatings remained pure and were present.

The next metrology process that was used is that of stylus profilometry. For this measurement, a highly precise needle is effectively dragged across the surface of the wafer, such that it can measure any changes in surface height. The tool for this in the Cal Poly Microfabrication facility is accurate to ~1nm, thus making this a unique and vastly important tool when working with z-axial heights in the nanometer regime. This measurement tool was used rather extensively, as thickness measurements were made after each permanent coating has been deposited either directly or via test wafers. Another height measurement technique that will
be utilized is that of an optical interferometer, which was used to determine the thickness of thermally grown oxide layers.

The next measurement type that was hopeful to be performed is that of SIMS, or Secondary Ion Mass Spectroscopy. This is done to determine a physical junction depth that is characteristic of the Source and Drain n-wells. This measurement is mainly important for specifying the device model with precision to the real-world, fabricated device such that when comparative analysis is being done, the probability of maintaining a desired relationship between the two will be larger.

Lastly, another measurement process that was done throughout the fabrication process is that of optical microscopy. This was done to qualitatively assure that material layers and overall alignment between layers was kept within good margins of error. While there was no quantitative data pulled from the microscopy, it is of the utmost importance, as the aligner being used in the process is very unsteady relative to the desired precision. In addition to the optical microscopy, scanning electron microscopy was performed at the end of the fabrication process, to again qualitatively assure deposition and alignment accuracies, as well as confirmation of geometric characteristics.

B. Device and Array Measurements

The goal for the device testing after the fabrication process has been completed is to perform a nearly full characterization of the individual devices, a characterization of the Body Effect utility vs. distance, as well as perform array characterization using a basic electrolyte solution to determine the optimal series/parallel topology.
For the individual devices, the initial characterization was to be performed using a curve tracer (a.k.a. Semiconductor Parameter Analyzer). While the curve tracer would not be able to fully characterize the subthreshold operation of the fabricated devices, it is a crucial measurement tool to provide an initial idea of the functionality. This will allow for $I_D$ vs. $V_{DS}$ and $C$ vs. $V_{DS}$ curves to be readily observed. Once the curves have been plotted via the curve tracer, parameters such as subthreshold swing and channel length modulation could be determined, as well as overall qualitative accuracy relative to the behavioral model developed. This tool would also allow for the characterization of Body Effect utility vs. distance from active device via applying a nominal body bias to the differently fabricated devices, and having the curve tracer plot out the characteristic curves for each of the said devices. The resultant curve data can then be normalized by its respective unbiased I-V plot, which would then allow for a true comparative analysis to be made.

Once the initial analysis on the curve tracer is competed for the individual devices, a more conventional testing setup using dual-supply DC PSU and a Kiethley Picoammeter would be used to characterize the subthreshold operation of the devices, as well as their current-noise characteristics. Since this is an FET device operated at relatively low frequencies, $1/f$ or pink noise may cause some disruptions during operation, so it will be imperative that this phenomena be characterized such that mitigation techniques may be implemented. The predictive model would again be useful here, in that it allows for visualization of the subthreshold operation, which would be utilized in the comparative analysis between the modelled and measured $I_D$ vs. $V_{DS}$ and $I_D$ vs. $V_{GS}$ curves. There would also be some AC-regime testing that will be done. This would be carried out by effectively creating a simple common-source amplifier, and characterizing the amplification parameters for very small signals at low frequencies. The
testing setup would remain the same, with the only addition being that of low tolerance resistors. The main goal of this testing would be to characterize the transconducting behavior of the device, a crucial parameter in the context of ISFET operation, in that it allows for an immediate qualitative view of the overall sensitivity of the device.

The final mode of testing for the individual devices would be that of their fault tolerances. The plan for this characterization would be to purposely overload the device in two separate manners using fairly standard equipment of a dual-supply DC PSU, and a Kiethley Sourcemeter, and conventional Keithley Ammeter. First, four very well-matched devices would be selected for this testing to ensure good comparative results (this would be done by selecting four devices whose characteristic $I_D$ curves qualitatively behave in the same manner, most likely spatially close to one another on the wafer). Then, for two of the devices a constant, nominal $V_{DS}$ would be applied, as well as a continually increased $V_{GS}$ voltage. The $V_{GS}$ voltage would be increased up until the breakdown of the MOS structure is observed in order to characterize this failure mode. The next methodology that would be used is to keep the $V_{GS}$ voltage nominally constant while increasing the $V_{DS}$ voltage until failure is observed via either a purely short or purely open measurement reading. Finally, ESD testing would be done using the human-body model in order to determine if the devices are well suited to handling day-to-day ESD events that may occur throughout the device lifetime.

In terms of the array testing, the proposed methodology is that of using a small piece of solidified PDMS (PolyDiMethylSiloxane) with a small microcavity hole punched through it. This piece of PDMS would be cut to match the size of the arrays being tested, without overlapping itself across any electrical contacts, other than the ISFET Gates. With the Source and Drain contacts being connected to a DC PSU through a Kiethley Picoammeter, and the Body
contact being biased via a DC PSU to whatever level deemed necessary from the previous single device testing, a concentrated electrolyte solution would be flowed through the microcavity in the PDMS containing hydrogen ions. The reasoning for using this electrolyte instead of a Potassium or Sodium electrolyte is that the proper selectivity layer allowing for specified Sodium and Potassium sensing will not be completed by the time the ISFET arrays are tested (the selectivity layer being developed is a Master’s Thesis Project of another Student in the BMED Graduate Department). Even though the selectivity layer will not be completed, using a hydrogen ion electrolyte should yield some level of Gate actuation, and if this is found to not be the case, then a more simplistic pH selectivity layer could be readily developed and applied to the arrays to perform the requisite testing. The array itself would also be placed on a hot plate set to 37°C in order to mimic human body temperature. The arrays would then be characterised based on their electrical topologies to observe which topology provides both the best overall drain current capabilities, as well as the best sensitivity to the applied electrolyte solution. Multiple solutions would be used to perform this testing, of different total pH concentration for performing the sensitivity analysis.

V. Testing Results

As mentioned above in the Fabrication Notes section, the devices were not completed sufficiently to enable any electrical testing. The hoped for SIMS metrology also could not be performed, as there was not enough time to have the wafers sent to UCSB to have them perform the measurement. As this is the case, this section will focus on the metrological and process data gathered throughout the fabrication process, starting with the initial resistivity measurements: (Note: Analysis of data will largely not be mentioned here as it is included throughout the report)
<table>
<thead>
<tr>
<th>Wafer Number</th>
<th>Applied Current (mA)</th>
<th>Measured Voltage (mV)</th>
<th>Sheet Resistance (Ohm)</th>
<th>Approximate Resistivity (Ohm-cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10</td>
<td>73</td>
<td>33.069</td>
<td>1.32276</td>
</tr>
<tr>
<td>2</td>
<td>10</td>
<td>85</td>
<td>38.505</td>
<td>1.5402</td>
</tr>
<tr>
<td>3</td>
<td>10</td>
<td>75</td>
<td>33.975</td>
<td>1.359</td>
</tr>
<tr>
<td>4</td>
<td>10</td>
<td>125</td>
<td>56.625</td>
<td>2.265</td>
</tr>
<tr>
<td>5</td>
<td>10</td>
<td>74</td>
<td>33.522</td>
<td>1.34088</td>
</tr>
<tr>
<td>6</td>
<td>10</td>
<td>78</td>
<td>35.334</td>
<td>1.41336</td>
</tr>
<tr>
<td>7</td>
<td>10</td>
<td>70</td>
<td>31.71</td>
<td>1.2684</td>
</tr>
<tr>
<td>8</td>
<td>10</td>
<td>63</td>
<td>28.539</td>
<td>1.14156</td>
</tr>
<tr>
<td>9</td>
<td>10</td>
<td>54</td>
<td>24.462</td>
<td>0.97848</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
<td>106</td>
<td>48.018</td>
<td>1.92072</td>
</tr>
<tr>
<td>11</td>
<td>10</td>
<td>60</td>
<td>27.18</td>
<td>1.0872</td>
</tr>
<tr>
<td>12</td>
<td>10</td>
<td>27</td>
<td>12.231</td>
<td>0.48924</td>
</tr>
<tr>
<td>13</td>
<td>10</td>
<td>70</td>
<td>31.71</td>
<td>1.2684</td>
</tr>
<tr>
<td>14</td>
<td>10</td>
<td>132</td>
<td>59.796</td>
<td>2.39184</td>
</tr>
<tr>
<td>15</td>
<td>10</td>
<td>58</td>
<td>26.274</td>
<td>1.05096</td>
</tr>
<tr>
<td>16</td>
<td>10</td>
<td>69</td>
<td>31.257</td>
<td>1.25028</td>
</tr>
<tr>
<td>17</td>
<td>10</td>
<td>35</td>
<td>15.855</td>
<td>0.6342</td>
</tr>
<tr>
<td>18</td>
<td>10</td>
<td>44</td>
<td>19.932</td>
<td>0.79728</td>
</tr>
<tr>
<td>19</td>
<td>10</td>
<td>40</td>
<td>18.12</td>
<td>0.7248</td>
</tr>
<tr>
<td>20</td>
<td>10</td>
<td>66</td>
<td>29.898</td>
<td>1.19592</td>
</tr>
<tr>
<td>21</td>
<td>10</td>
<td>39</td>
<td>17.667</td>
<td>0.70668</td>
</tr>
<tr>
<td>22</td>
<td>10</td>
<td>65</td>
<td>29.445</td>
<td>1.1778</td>
</tr>
<tr>
<td>23</td>
<td>10</td>
<td>74</td>
<td>33.522</td>
<td>1.34088</td>
</tr>
<tr>
<td>24</td>
<td>10</td>
<td>80</td>
<td>36.24</td>
<td>1.4496</td>
</tr>
<tr>
<td>25</td>
<td>10</td>
<td>169</td>
<td>76.557</td>
<td>3.06228</td>
</tr>
</tbody>
</table>

*Table 1: Shows Raw Metrological Data of Wafer Resistivity Used in Wafer Selection*
The next key metrics of note were that of the diffusion mask thicknesses, tested with the Filmmetrics Optical Profilometer after standard calibration:

<table>
<thead>
<tr>
<th>Wafer Number</th>
<th>Center Measurement (nm)</th>
<th>Bottom Measurement (nm)</th>
<th>Top Measurement (nm)</th>
<th>Right Side Measurement (nm)</th>
<th>Left Side Measurement (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>506.7</td>
<td>513.2</td>
<td>512.2</td>
<td>509.8</td>
<td>511.8</td>
</tr>
<tr>
<td>17</td>
<td>481.3</td>
<td>491.2</td>
<td>503.2</td>
<td>501.8</td>
<td>489.6</td>
</tr>
<tr>
<td>18</td>
<td>456.5</td>
<td>469.4</td>
<td>471.4</td>
<td>463.1</td>
<td>469.4</td>
</tr>
<tr>
<td>19</td>
<td>407.3</td>
<td>423.5</td>
<td>423.5</td>
<td>426.4</td>
<td>401.6</td>
</tr>
</tbody>
</table>

Table 2: Raw Data for Oxide Diffusion Mask Thicknesses Note: Wafer #21 Had Accidentally Been Sent to the Next Process and Could Not be in This Data Gathering

Following this are the PVD process parameters for the Cr + Ag + Cr layer deposited on the wafers:

<table>
<thead>
<tr>
<th>Wafer Number</th>
<th>Base Pressure (x10^-6 torr)</th>
<th>Process Pressure (mtorr)</th>
<th>Chromium Sputter DC Power (W)</th>
<th>Silver Sputtering DC Power (W)</th>
<th>Chromium Sputter Time (1/2) (seconds)</th>
<th>Silver Sputter Time (seconds)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>8</td>
<td>2.5</td>
<td>99</td>
<td>101</td>
<td>10/5</td>
<td>20</td>
</tr>
<tr>
<td>17</td>
<td>8.5</td>
<td>2.5</td>
<td>99</td>
<td>101</td>
<td>11/5</td>
<td>20</td>
</tr>
<tr>
<td>18</td>
<td>8.5</td>
<td>2.5</td>
<td>99</td>
<td>101</td>
<td>10/5</td>
<td>20</td>
</tr>
<tr>
<td>21</td>
<td>4.5</td>
<td>2.5</td>
<td>99</td>
<td>101</td>
<td>10/5</td>
<td>20</td>
</tr>
</tbody>
</table>

Table 3: Raw Process Data for Chromium + Silver + Chromium Sputtering

As mentioned previously, the Cr + Ag + Cr process had to be replaced with a purely Chromium Sputter, of which the raw data is given by:
Table 4: Raw Process Data for ~30nm Chromium Deposition

<table>
<thead>
<tr>
<th>Wafer Number</th>
<th>Base Pressure (x10^-6 torr)</th>
<th>Process Pressure (mtorr)</th>
<th>Ar Flow Rate (sccm)</th>
<th>DC Power Applied (W)</th>
<th>Sputter Time (seconds)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>4.8</td>
<td>2.5</td>
<td>46</td>
<td>100</td>
<td>60</td>
</tr>
<tr>
<td>17</td>
<td>6.3</td>
<td>2.5</td>
<td>46</td>
<td>100</td>
<td>60</td>
</tr>
<tr>
<td>18</td>
<td>4.1</td>
<td>2.5</td>
<td>46</td>
<td>100</td>
<td>60</td>
</tr>
<tr>
<td>21</td>
<td>7</td>
<td>2.5</td>
<td>46</td>
<td>100</td>
<td>60</td>
</tr>
</tbody>
</table>

The next set of raw data points comes from the characterization of the PHPR process, wherein there is both process data, and metrological data in the form of sheet resistance measurements and film thickness:

Table 5: Raw PHPR Process Testing Data

<table>
<thead>
<tr>
<th>Wafer Number</th>
<th>Base Pressure (mtorr)</th>
<th>Process Pressure (mtorr)</th>
<th>Power (Forward/Reverse) (W)</th>
<th>Time (seconds)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>21</td>
<td>307</td>
<td>45/1</td>
<td>20</td>
</tr>
<tr>
<td>4</td>
<td>18</td>
<td>310</td>
<td>45/2</td>
<td>20</td>
</tr>
<tr>
<td>5</td>
<td>21</td>
<td>310</td>
<td>45/3</td>
<td>20</td>
</tr>
</tbody>
</table>

Table 6: Raw Sheet Resistance Data From 4-Point Probe Measurements

<table>
<thead>
<tr>
<th>Wafer Number</th>
<th>Bare Silicon R_s (kΩ)</th>
<th>Hard Bake R_s (MΩ)</th>
<th>PHPR R_s (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>86.1</td>
<td>8.6</td>
<td>842.6</td>
</tr>
<tr>
<td>4</td>
<td>84.3</td>
<td>8.4</td>
<td>792.8</td>
</tr>
<tr>
<td>5</td>
<td>34.0</td>
<td>7.7</td>
<td>747.5</td>
</tr>
<tr>
<td>Wafer Number</td>
<td>Pre-Plasma Hardened Thickness (nm)</td>
<td>Plasma Hardened Thickness (nm)</td>
<td></td>
</tr>
<tr>
<td>--------------</td>
<td>----------------------------------</td>
<td>--------------------------------</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>1400</td>
<td>463</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>1400</td>
<td>574</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>1400</td>
<td>647</td>
<td></td>
</tr>
</tbody>
</table>

*Table 7: Raw PHPR Film Thickness Data Pre and Post Plasma Hardening*

As can be observed from the above PHPR data, the plasma hardening did indeed have a profound effect on both the dielectric properties of the file, as well as the overall thickness, which confirm the findings found in the paper used in defining the process.

The final data to be displayed in this section is that of the final Chromium sputter process parameters:

<table>
<thead>
<tr>
<th>Wafer Number</th>
<th>Base Pressure (x10^-6 torr)</th>
<th>Process Pressure (mtorr)</th>
<th>Ar Flow Rate (sccm)</th>
<th>DC Power Applied (W)</th>
<th>Sputter Time (minutes)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>7.4</td>
<td>2.4</td>
<td>46</td>
<td>99</td>
<td>6</td>
</tr>
<tr>
<td>17</td>
<td>4.7</td>
<td>2.4</td>
<td>46</td>
<td>99</td>
<td>6</td>
</tr>
<tr>
<td>18</td>
<td>-</td>
<td>2.4</td>
<td>46</td>
<td>99</td>
<td>6</td>
</tr>
<tr>
<td>21</td>
<td>9</td>
<td>2.4</td>
<td>46</td>
<td>99</td>
<td>2</td>
</tr>
</tbody>
</table>

*Table 8: Gate Metallization Chromium Sputter Process Parameters*

**VI. Conclusion and Recommendations**

Overall, while the final state of the project may be undesirable relative to the initial goals, the devices and fabrication plans designed met or exceeded nearly all laid out requirements, at least in theory, and according to the BOM analysis found in Appendix B, the project came in
under-budget by roughly $250. The devices (according to the theoretical model) have an excellent subthreshold swing parameter of ~66mV/dec(I), approaching the theoretical minimum of ~59mV/dec(I). When taking the fact that most commonly found MOSFET-type devices yield a subthreshold swing in the mid to high 70’s, 66mV/dec(I) is almost unprecedented given the relatively old processing utilized. The threshold voltage of 0.33V, while not as high as originally hoped for, would theoretically still allow for fully nominal operation in the subthreshold region for a single device, and especially for the arrays, wherein the Gate potentials are distributed throughout the array, causing the individual devices to each have an effective smaller applied bias. As the devices and their model were initially developed with human body temperature as the nominal operating state, this requirement can also be said to have been met, albeit theoretically. With the unfortunate circumstances of the devices not being able to be fully completed, no ESD testing was done, however in terms of user electrical safety, the requirement has been met. This is largely due to the subthreshold nominal operation, wherein all applied potentials are much too small to induce any harm to a user (<100mV, in theory). With the designed aspect of utilizing a Silver Gate contact, the devices are also compatible with future plans, such as the application of the selectivity layer to enable true ISFET behavior. With this being the case, it can be said that all device requirements were indeed met.

In terms of the arrays, since the electrical testing could not be performed, the meeting of requirements #2 and #3 are entirely unknown, however given the theoretical model and the discussed nature of FET arrays, once testing has been completed in the future, there is a very high probability that these requirements will be met. In terms of the remaining array requirements, as mentioned, having the Gate contact fabricated with Silver alone yields compatibility with the future selectivity layer, therefore this requirement can also be said to have
been met. The arrays were indeed designed to take up minimal space on the wafer while still being sizeable enough to have a high device count, but none of the designed arrays came close to exceeding the 1cm x 1cm maximal requirement. As for the physical shock requirement, without explicit testing into this parameter, it will have to remain unknown for now, however in future designs, one could develop the same devices on a thicker substrate material in order to generally improve this robustness. Also, since materials with good adhesion and strong mechanical properties were used in the designs, the arrays should in theory have at least fairly good shock tolerances. All in all for the arrays, while not every requirement was explicitly met, enough of them were met to consider the design as good, especially as a proof of concept.

In terms of the fabrication requirements set forth, all of them were exceeded in the designs. Conventional CMOS processing techniques were indeed utilized throughout the fabrications process, only three photomasks were required, even with a design that required five separate lithographic processes, and none of the masks utilized feature sizes of fewer than ten micrometers. The most exotic material used in the design was Titanium, which is highly conventional in the context of biological sensors, due to its biological inertness. Lastly, the requirement of no more than 50 processing steps was well exceeded, in that the originally designed process only utilized 39 processing steps, and even the alternate design developed when the deposition of the Nitride layer became a non-option only utilized 36 total processing steps.

In terms of recommendations if someone wants to refabricate these devices, I would mainly suggest the use of Chrome-on-Glass photomasks for photomask numbers 1 and 3, as opposed to the used transparency masks. This is due to the much sharper printing on the smaller sized features that can be achieved with the technology, as well as the ease of use it would provide in performing the alignment and lithographic processes.
As a reference, Figure 33 shows two of the fabricated devices, specifically the n-well patterning that was done via a transparency photomask. Relative to the mask design, the printed features appear blown-out and with rounded edges. This led to the channel region being shorter in length than originally designed for. While this in theory makes the electrical characteristics of the devices more favorable, it weakens process control immensely, and the only method of rectification for this issue is to utilize more advances photomasking technology. The use of fresh chemicals such as etchants, photoresists, and their developers would be another recommendation I would make, as it would help to avoid many of the processing disruptions that occurred throughout the process. Finally, now that the Microfabrication Facility at Cal Poly has a Nitride deposition process, I would highly recommend to anyone replicating these devices to utilize that
process as opposed to the PHPR process. Even though theoretically, the PHPR layer has better dielectric properties than the Nitride, it is well worth the tradeoff in terms of manufacturability, and user safety, as Nitride is completely inert biologically, while even the hardened photoresist could still be mildly carcinogenic.

In conclusion, this project was a learning opportunity like no other. The amount of experience gained both in terms of the theoretical work and the practical work was completely unparalleled, and I am immensely grateful to all those involved in allowing me to work on this project. As an added bonus, the trickledown of the work conducted for this project (including the development of the Nitride deposition process) will many student from various departments at Cal Poly to do even greater and more significant work in the future.

**VII. References**


Appendices

A. Senior Project Analysis

Project Title: Potassium and Sodium Sensing ISFET Device and Array

Student’s Name: Liam Hayes

Advisor’s Name: Professor Ben Hawkins

Summary of Functional Requirements:

The Potassium and Sodium Sensing ISFET Device is being designed and manufactured to be implemented into a larger product. This eventual product will be able to sense the users potassium and sodium concentration levels in real time, using the ISFET device arrays as the sensor. The aim of the project is to develop a high quality and robust design for the array and constituent single ISFET devices, as well as to develop and characterize the manufacturing process that will be used to realize them. It will provide the user benefits of real-time monitoring of their bodily ionic levels via a completely harmless and painless process while maintaining a high level of accuracy. This will in turn eliminate the need for the prospective wearer to take expensive, and time consuming tests on a regular basis, increasing their quality of life.

Primary Constraints:

The main constraints are the capabilities of the Fabrication Facility and the resultant geometric limitations of the device. As the Cal Poly Microfab mainly utilizes older equipment, some initial, more advanced designs had to be rejected, as their on-premises manufacturability was impossible. This, combined with the fact that the device needs to be contacting the wearer’s
skin at all times, led to geometric limitations, as the Source and Drain contacts for the device have to be fully insulated from the wearer’s skin, while leaving the gate region fully exposed.

**Economic:**

A. Human Capital: Once the proof of concept has been completed for the product, other engineers will be able to iterate on it, and develop more advanced designs, providing jobs and projects for future engineers.

B. Financial Capital: The eventual product can generate revenue through being sold to both individuals and to hospitals who may want these devices to monitor their patients.

C. Natural Capital: The device itself will be extremely difficult to recycle, and as the lifetime of the Selectivity Layer is roughly two weeks, the product will unfortunately generate a sizeable amount of waste. The manufacturing process, while high scaleable, is also not the most environmentally friendly, as it uses many process gasses and materials that are highly toxic to both the fabricators and the environment.

D. Cost: The product will initially have a large cost associated with it, as it is in the research phase. Once the proof of concept has been verified, and the design is being fabricated in an industry-level facility, the scale of it will drastically decrease the cost to produce. At this point, the hope is that the device will cost no more than $100 per wearable for the end user.

**If Manufactured on Large-Scale Basis:**

ISFET Array/Sensor Only-

Estimated Number of Devices Per Year: 10 Million

Estimated Manufacturing Cost for Each Device: $0.50
Estimated Purchase Price for Each Unit: $5

Estimated Profit per Year: $45 Million

Estimated Cost for User to Operate Device: $0/Cost of Purchase

**Manufacturability:**

At scale, the product will require a fully equipped electronics manufacturing facility, as well as a highly capable CMOS microfabrication facility. Much of the electronics external to the sensing device can be purchased at large scale as consumer products, such as microcontrollers. The ISFET Sensor and watch-style housing will need to be manufactured in-house, to allow for full customization and product control.

**Environmental Impact:**

There are two separate aspects for the environmental impact of the device. The manufacturing impacts are based on the fact that the processes used in micro and nano-scale device fabrication utilize harmful chemicals and gasses that can be carcinogenic, flammable, caustic, highly reactive, corrosive, and highly toxic to both humans and the environment. Recycling and advanced filtering techniques can be used to mitigate these effects, however, there are no truly 100% clean processes as of yet. The device itself will also contribute to environmental waste, as the selectivity layers on the ISFET sensors only last about two weeks before they stop functioning properly. This will lead to the users changing out their devices regularly, causing more non-recyclable waste to be injected into the environment. This can be partly mitigated by careful materials choice for the housing of the product.

**Sustainability:**

To ensure that the device will not negatively impact the environment more than it absolutely has to, choice of materials will be key. Using lead-free solder is one good practice
that may be implemented, using more readily available materials and components may help this cause as well. Choosing either a recyclable plastic or a non-plastic, recyclable material for the housing of the device will also be of the utmost importance in the consideration of sustainability.

**B. BOM Analysis**

The BOM analysis here is done in terms of the actual fabrication that was conducted, and not the ideal process, however, total costs incurred would be roughly the same (+/- $100) if the ideal, theoretical process was conducted one to one.

<table>
<thead>
<tr>
<th>Item</th>
<th>Number of Items Used</th>
<th>Price Per Item ($)</th>
<th>Net Cost ($)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafers</td>
<td>5</td>
<td>14</td>
<td>70</td>
</tr>
<tr>
<td>Positive Photoresist (L)</td>
<td>0.5</td>
<td>500</td>
<td>250</td>
</tr>
<tr>
<td>Negative Photoresist (L)</td>
<td>0.01</td>
<td>500</td>
<td>5</td>
</tr>
<tr>
<td>Photomasks</td>
<td>3</td>
<td>75</td>
<td>225</td>
</tr>
<tr>
<td>Chromium Target</td>
<td>0.001</td>
<td>185</td>
<td>0.185</td>
</tr>
<tr>
<td>Silver Sputter Target</td>
<td>0.00001</td>
<td>290</td>
<td>0.0029</td>
</tr>
<tr>
<td>N2 Gas (Tanks)</td>
<td>3</td>
<td>25</td>
<td>75</td>
</tr>
<tr>
<td>Ar Gas (Tanks)</td>
<td>0.7</td>
<td>76</td>
<td>53.2</td>
</tr>
<tr>
<td>O2 Gas (Tanks)</td>
<td>0.5</td>
<td>189</td>
<td>94.5</td>
</tr>
<tr>
<td>Cr Etchant (Gal)</td>
<td>0.1</td>
<td>150</td>
<td>15</td>
</tr>
<tr>
<td>Silver Etchant (Gal)</td>
<td>0.001</td>
<td>150</td>
<td>0.15</td>
</tr>
<tr>
<td>Microposit 1165 (Gal)</td>
<td>0.5</td>
<td>250</td>
<td>125</td>
</tr>
<tr>
<td>CD-26 Developer (Gal)</td>
<td>0.5</td>
<td>300</td>
<td>150</td>
</tr>
<tr>
<td>Acetone (Gal)</td>
<td>0.5</td>
<td>130</td>
<td>65</td>
</tr>
<tr>
<td>Isopropanol (Gal)</td>
<td>0.1</td>
<td>220</td>
<td>22</td>
</tr>
<tr>
<td>MCC Primer HMDS (L)</td>
<td>0.5</td>
<td>300</td>
<td>150</td>
</tr>
<tr>
<td>ma-D 533/S (L)</td>
<td>0.01</td>
<td>300</td>
<td>3</td>
</tr>
<tr>
<td>General Power Consumption (kWh)</td>
<td>1000</td>
<td>0.45</td>
<td>450</td>
</tr>
<tr>
<td>Total ($)</td>
<td></td>
<td></td>
<td>1753.0379</td>
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</tbody>
</table>

Table 9: Shows Estimated BOM Cost Sheet
C. Timeline Analysis

While the timeline for this project did indeed vary as different issues arose with the fabrication equipment, the prospective timeline to this point presented in a Gantt style chart is as follows:

<table>
<thead>
<tr>
<th>ID</th>
<th>Task Mode</th>
<th>Task Name</th>
<th>Duration</th>
<th>Start</th>
<th>Finish</th>
<th>Predecessors</th>
<th>Successors</th>
<th>Resource Names</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td>Define</td>
<td>22 days</td>
<td>Fri 1/7/22</td>
<td>Mon 2/7/22</td>
<td></td>
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<td>Liam</td>
</tr>
<tr>
<td>2</td>
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<td>Abstract</td>
<td>1 day</td>
<td>Fri 1/7/22</td>
<td>Fri 1/7/22</td>
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<tr>
<td>3</td>
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<tr>
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<td>Liam</td>
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<tr>
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<td>Mon 2/7/22</td>
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<tr>
<td>12</td>
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<td>Liam</td>
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<tr>
<td>13</td>
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<td>Thu 3/10/22</td>
<td>Thu 3/10/22</td>
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<tr>
<td></td>
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<td></td>
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<tr>
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<tr>
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<td></td>
<td>Verify Simulation</td>
<td>7 days</td>
<td>Mon 4/25/22</td>
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Project: EE4605GanttChart/Liam
Date: Tue 6/14/22
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<th>Duration</th>
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<th>Successors</th>
<th>Resource Names</th>
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<tr>
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<tr>
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<td>Fri 6/10/22</td>
<td>Fri 6/10/22</td>
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<td>Liam</td>
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<tr>
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<tr>
<td>26</td>
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<td>Wed 7/30/22</td>
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<td>29</td>
<td>Liam</td>
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<tr>
<td>29</td>
<td></td>
<td>Make Design/Manufacturing Improvements (if Necessary)</td>
<td>2 days</td>
<td>Wed 7/3/22</td>
<td>Thu 7/14/22</td>
<td>28</td>
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<td>Liam</td>
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<tr>
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<td>Fully Characterize Device</td>
<td>1 wk</td>
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<tr>
<td>31</td>
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<td>13.5 days</td>
<td>Thu 7/21/22</td>
<td>Tue 8/9/22</td>
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<td>Liam</td>
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</table>

Project: EE460 Gantt Chart Liam
Date: Tue 6/14/22

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<th>ID</th>
<th>Mode</th>
<th>Task Name</th>
<th>Duration</th>
<th>Start</th>
<th>Finish</th>
<th>Predecessors</th>
<th>Successors</th>
<th>Resource Names</th>
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<td>3 days</td>
<td>Thu 7/21/22</td>
<td>Mon 7/25/22</td>
<td>30</td>
<td>33</td>
<td>Liam</td>
</tr>
<tr>
<td>33</td>
<td></td>
<td>Gather materials for Final Report</td>
<td>1 day</td>
<td>Thu 7/26/22</td>
<td>Tue 7/26/22</td>
<td>32</td>
<td>34</td>
<td>Liam</td>
</tr>
<tr>
<td>34</td>
<td></td>
<td>Write Final Report 1.5 wks</td>
<td></td>
<td>Wed 7/27/22</td>
<td>Fri 8/5/22</td>
<td>33</td>
<td>35</td>
<td>Liam</td>
</tr>
<tr>
<td>35</td>
<td></td>
<td>Present Final Report/Findings</td>
<td>2 days</td>
<td>Fri 8/5/22</td>
<td>Tue 8/9/22</td>
<td>34</td>
<td></td>
<td>Liam</td>
</tr>
</tbody>
</table>

Project: EE460 Gantt Chart Liam
Date: Tue 6/14/22
Using the Gantt Chart, it is predicted that the project will take no longer than until August 9th of 2022, even when factoring in a couple of weeks extra, in case anything may go wrong in the fabrication or testing processes.

The above Gantt Chart and overall timeline were developed prior to the fabrication commencing, and as described above in the Fabrication Notes section, there were many issues that needed to be overcome. The end result of this, as described, was that the devices were not able to be fully completed, let alone tested. As such, the completion of the project, in terms of my involvement was on September 2nd.

**D. Ethical Analyses**

As a whole, the device and product are both highly ethical, in that when they are fully functioning, do nothing aside from help the user. As the likelihood of the user being a kidney transplant patient is relatively high, and the device eliminates any invasiveness that was otherwise required, it can only benefit the user by providing a higher quality of life. It will also put at ease the user’s friends and family, who may normally be constantly worried for the user’s health. The only ethical dilemma associated with the product is the negative environmental impacts that it will cause. Potential mitigation techniques to account for this were discussed in the above two sections. There is effectively no associated harm risk to the user, as all voltage levels will be kept below 5V DC, which is not nearly enough to injure a human.

**E. Future Developments**

While there are many developments that could be made to the project in the context of a more advanced fabrication facility, from what is available within the Cal Poly Microfabrication lab, the main developments to be looked at are the use to degenerately n-type doped polysilicate as a replacement for the Gate contact. This would decrease the work function of the Gate
contact, thereby increasing the flatband voltage, and further, increase the threshold voltage, all of which are extremely desirable in the context of this device. This was not considered in the early design stages, as the facility had no ability to depose polysilicate in any form. This inclusion would also allow for easier fabrication, in that both the Gate contact and dielectric could be etched simultaneously, significantly reducing the number of processing steps needed for device realization.

Another development that will be more difficult to implement, but could still be effective is to utilize multiple lithographic passes when patterning the features around the Gate, such that the channel length decreases to a further degree. This would in turn yield an immediate increase in observed Drain current while keeping all biasing and sensing potentials as they were prior, an obvious general improvement.

Lastly, the one future development that is already being worked on, is the inclusion of a selectivity layer. Once this film has been developed and applied to the devices, the true BioFET nature of them will be enabled, and the devices can be utilized for their intended purpose.

F. MATLAB Scripts

```matlab
%%Liam Hayes
%%Senior Project ISFET Device Design Calculations and Model Result Viewing
format long

%% Physical Constants
e = 1.602e-19;  \text{%Charge Constant}
ep0 = 8.854e-12;  \text{%Free Space Permittivity}
epsi = 11.7;  \text{%Relative Permittivity of Silicon}
epdiOx = 3.7;  \text{%Relative Permittivity of Silicon Dioxide in Highly Ordered Form}
kb = 1.38e-23;  \text{%Boltzmann's Constant in J/K}
Eg = 1.794e-19;  \text{%Intrinsic Silicon Band Gap in J}
Eg_eV = 1.12;  \text{%Intrinsic Silicon Band Gap in eV}
hbar = 1.05456e-34;  \text{%Planck's Constant Divided by 2pi}
me = 0.43*9.109e-31;  \text{%Average Effective mass of Electron in Silicon Lattice}
mh = 0.54*9.109e-31;  \text{%Average Effective Hole mass in Silicon Lattice}
```
T = 310; %Device Operating Temperature (Body Temp.)

%% Device Related Constants
phi_m = 4.33; %Titanium Work Function in eV
tOx = 10e-9; %Proposed Oxide Thickness in m
Na = 7.17e15; %Background Acceptor Concentration in cm^-3
NA = Na*1000000; %Background Acceptor Concentration in m^-3
Nd = 2e18; %Proposed n-well Concentration in cm^-3
ND = Nd*1000000; %Proposed n-well Concentration in m^-3
x_j = 21e-9; %Proposed Junction Depth of n-wells in m
VBG = 0; %Proposed Body to Gate Bias Point (Will be variable)
Vt = (kb*T)/e; %Device Thermal Voltage in V
W = 100e-6; %Designed Channel/Gate Width in m
L = 10e-6; %Constructed Channel/Gate Length in m
lambda = 1; %Channel Length Modulation Parameter

%% Device Parameter Calculations

%Thermally adjusted Chemical Potential in J
mu = ((Eg/2)+(0.75*kb*T*log(mh/me)));

%Thermally adjusted Chemical Potential in eV
Ef = mu/e;

%Intrinsic Carrier Density Using Boltzmann Approximation of Fermi-Dirac Distribution
n_i = 4*((kb*T)/(2*pi*hbar^2))^(3/2)*((me*mh)^(3/4))*exp(-mu/(kb*T));

%Differential Adjustment of Conduction Band in Bulk Silicon due to Background Doping and Thermal Influence in eV
dEg = (((-3*e^2)/(16*pi*epsi*ep0))*sqrt((NA*e^2)/(epsi*ep0*kb*T)))/e;

%Adjusted Conduction Band Energy in eV
E_CB = Eg_eV + dEg;

%Adjusted Electron Affinity due to Conduction Band Variance in eV
qchi = 4.15 - abs(dEg);

%Substrate Work Function in eV
phi_s = qchi + (E_CB - Ef) + phi_F;

%MOS Structure Flatband Voltage in V
V_FB = phi_s - phi_m;

%MOS Structure Built-In Potential in V
V_biMOS = V_FB;

%n-well/substrate Built-In Potential in V
V_biPN = Vt*log(ND*(NA/n_i^2));

%Bulk Potential in V
phi_F = Vt*log(NA/n_i);

%Channel Depletion Region Center Depth in m
Wd = sqrt((2*ep0*epsi*(2*phi_F+VBG))/(e*NA));

%n-well/substrate Depletion Region Depth in m
Wp = sqrt(((V_biPN*2*epsi*ep0)/(e*NA))*(ND/(ND + NA)));

%Adjusted MOS Structure Depletion Region Length in m
Lp = L - (2*Wp);
Effective Depth (n-well Junction Depth + Wp) in m
\[ r_j = x_j + Wp; \]

n-well Depletion Charge Induced by Depletion Region Overlap (Induces Lp) in C
\[ Q_{bi} = \left( e * NA * Wd * ((L + Lp) / 2) / L \right); \]

Oxide Capacitance in F/m^2
\[ C_{Ox} = \left( \varepsilon_{diOx} \varepsilon_0 / tOx \right); \]

Device Threshold Voltage in V
\[ V_{th} = V_{FB} - (2 \phi_F) - \left( \frac{Q_{bi}}{C_{Ox}} \right) \left( 1 - \sqrt{1 + \left( \frac{2 * Wd}{r_j} \right)} \right) \left( \frac{r_j}{L} \right); \]

Temperature and Doping Dependent Hole Mobility, Using Hole Mobility as in Subthreshold, Holes are majority charge carriers in cm^2/Vs
\[ \mu_h = \left( 54.3 \left( \frac{T}{300} \right)^{-0.57} + \left( \frac{T}{-2.33} \right)^{1.36e8} \right) \left( 1 + 0.88 \left( \frac{Na}{2.35e17} \left( \frac{T}{300} \right)^{2.4} \right) \right); \]

Temperature and Doping Dependent Electron Mobility for use in Linear and Saturation Regime I-V Relations
\[ \mu_e = \left( 88 \left( \frac{T}{300} \right)^{-0.57} + \left( \frac{T}{-2.33} \right)^{7.4e8} \right) \left( 1 + 0.88 \left( \frac{Nd}{1.26e17} \left( \frac{T}{300} \right)^{2.4} \right) \right); \]

Depletion Region Capacitance in F/m^2
\[ C_{dep} = \left( \varepsilon_i \varepsilon_0 / Wd \right); \]

Operating Characteristic Calculations

Id vs. Vds Curves

Differential Gate-to-Source Voltages if Device in V-All Regions
\[ V_{gs} = 0.1; \]

Differential Drain-to-Source Voltage Sweeps of Device in V-All Regions
\[ V_{ds} = \text{linspace}(0, 5, 1000000); \]
\[ V_{dsl} = \text{linspace}(0, (V_{gs} - V_{t}), 1000000); \]
\[ V_{dssat} = \text{linspace}((V_{gs} - V_{t}), 15, 1000000); \]

Device Slope Factor-Unitless
\[ n = \left( C_{Ox} + C_{dep} \right) / C_{Ox}; \]

Subthreshold Swing in mV/dec(A)
\[ S_{sth} = (\log(10) * V_{t} * n) * 1000; \]

Full equilibrium Drain Current in A-Subthreshold
\[ I_{D0} = \mu_h \cdot C_{Ox} \cdot (n - 1) \cdot (V_{t} \cdot 2) \cdot \exp(-V_{th} / (n * V_{t})); \]

Drain Current as a function of Vds and Vgs in A-Subthreshold
\[ I_{Ds} = I_{D0} \cdot (W/L) \cdot \exp(V_{gs} / (n * V_{t})) \cdot (1 - \exp(-V_{ds} / V_{t})); \]

Drain Current as a Function of Vde and Vgs in A-Linear
\[ I_{D1} = (0.0001 * \mu_e \cdot C_{Ox}) \cdot (W/L) \cdot ((V_{gs} - V_{t}) \cdot V_{dsl} - 0.5 \cdot V_{dsl} \cdot V_{t}) \cdot (1 + \lambda \cdot V_{dsl}); \]

Drain Current as a Function of Vds and Vgs in A-Saturation
\[ I_{Dsat} = (0.0001 * \mu_e \cdot C_{Ox} / 2) \cdot (W/L) \cdot ((V_{gs} - V_{t}) \cdot V_{dsl} - 0.5 \cdot V_{dsl} \cdot V_{t}) \cdot (1 + \lambda \cdot V_{dsl}); \]

Id vs. Vgs Curves

Differential Drain-to-Source Voltage Static in V-All Regions
\[ V_{ds1} = 0.5; \]

Differential Gate-to-Source Voltage Sweeps in V-All Regions
\[ V_{gs1} = \text{linspace}(0, V_{t}, 1000000); \]
\[ V_{gsl} = \text{linspace}(V_{t}, 5, 1000000); \]
Vgssat = linspace(Vds1, 10, 1000000);
%Drain Current as a function of Vds and Vgs in A-Subthreshold
IDsl = I_D0*(W/L)*exp(Vgs1/(n*Vt))*(1-exp(-Vds1/Vt));
%Drain Current as a Function of Vde and Vgs in A-Linear
IDl1 = (0.0001*mu_e*C_Ox)*(W/L)*((Vgsl-Vt).*Vds1 - 0.5*Vds1^2).*(1 + lambda*Vds1);
%Drain Current as a Function of Vds and Vgs in A-Saturation
IDsat1 = ((0.0001*mu_e*C_Ox)/2)*(W/L)*((Vgssat - Vt).^2).*(1 + lambda*Vds1);

%% Device Operation Plots
tiledlayout(1,2);
nexttile
%Operation plots for Id vs. Vds
if Vgs >= Vth
    plot(Vdssat, IDsat)
    hold on
    plot(Vdsl, IDl)
    hold on
    grid on
    ylabel("Drain Current in Amperes");
xlabel("Vds in Volts");
title("Plot of Id vs. Vds of ISFET Design Showing Linear and Saturation Regions of Operations");
else
    plot(Vds, IDs)
    grid on
    hold on
    ylabel("Drain Current in Amperes");
xlabel("Vds in Volts");
title("Plot of Id vs. Vds of ISFET Design Showing Subthreshold Region of Operation");
end
hold on
nexttile
%Operation Plots for Id vs. Vgs
if Vgs >= Vth
    plot(Vgssat, IDsat1)
    hold on
    plot(Vgsl, IDl1)
    hold on
    grid on
    ylabel("Drain Current in Amperes");
xlabel("Vgs in Volts");
title("Plot of Id vs. Vgs of ISFET Design Showing Linear and Saturation Regions of Operations");
else
    plot(Vgs1, IDs1)
    grid on
Table 10: Predictive, Behavioral Device Model MATLAB Script [21]

%%Liam Hayes
%%ISFET Senior Project Fabrication Process Calculations

format long

%% Physical Constants
q = 1.602e-19; % Free-Space Fundamental Charge in C
T_oxide = 900; % Oxide Growth Oven Temperature in Celcius
T_diff = 1000; % Diffusion Oven Temperature in Celcius-Predep Only
kB = 1.38e-23; % Boltzmann's Constant in J/K
kb = kB/q; % Boltzmann's Constant in eV/K
D0 = 10.5; % Thermally Independent Base Diffusivity of P in Si in cm^2/s
Ea = 3.69; % Activation Energy of P Diffused in Si in eV

%% Device/Fabrication Specific Constants
Xox_dry = 10e-9; % Thickness of Dry Grown Oxide in m
Xox_dry_um = 10e-3; % Thickness of Dry Grown Oxide in um
ssl_p = 9e20; % Solid Solubility Limit of P in Si in cm^-3
C_surf = ssl_p;
N_D = 2e18; % Desired n-Well Dopant Concentration in cm^-3
C_sub = N_D;

%% Gate Oxide Growth Calculations-Deal Grove Model
B = 5e-3; % Parabolic Rate Constant in um^2/hr
BonA = 2e-2; % Linear Rate Constant in um/hr
%Time for Oxide Growth in hr
t_hr = ((Xox_dry_um)^2/B) + (Xox_dry_um/BonA);
t = t_hr*3600; % Time for Oxide Growth in Sec

%% Phosphorous Thermal Diffusion Doping Calculations-Predep
D_p = D0*exp(-Ea/(kb*T_diff)); % Diffusivity of Phosphorous in Si
%Pre-Deposition Process Time in hr
t_pdhhr = 2;
t_pdh = t_pdhhr*3600;
%Pre-Deposition Process Time in sec
Q = (1/sqrt(pi))*C_surf*sqrt(D_p*t_pdh); % Dose Parameter in cm^-2
% Junction Depth Post Pre-Dep in cm
x_jcm = 2*sqrt(D_p*t_pdh)*erfcinv(C_sub/C_surf);
x_j = x_jcm*10^7; % Junction Depth Post Pre-Dep in nm
% Phosphorous Thermal Diffusion Doping Calculations-Drive-In

\[ D_{\text{pdi}} = D_0 \exp\left(-\frac{E_a}{k_B T_{\text{oxide}}}\right) \] %Diffusivity of Phosphorous in Si

\[ t_{\text{di}} = t; \] %Drive-In Process Time in sec

%Drive-In Process Depth in cm

\[ x_{\text{dicm}} = 2 \times \sqrt{D_{\text{pdi}} t_{\text{di}}} \times \sqrt{\log\left(\frac{Q}{C_{\text{sub}} \sqrt{\pi D_{\text{pdi}} t_{\text{di}}}}\right)}; \]

\[ x_{\text{di}} = x_{\text{dicm}} \times 10^7; \] %Drive-In Process Depth in nm

\[ x_{\text{tot}} = x_{\text{di}} + x_j; \] %Total Junction Depth in nm

% Wet Oxide Diffusion Mask Calculations-@T=1100C

\[ D_{0_p} = 5 \times 10^{-14}; \] %Diffusivity of Phosphorous in SiO2 in cm^2/sec

\[ E_a_p = 4.4; \] %Approximate Activation Energy of Phosphorous in SiO2 in eV

%Oxide Mask Thickness in cm

\[ x_{\text{oxcm}} = 2 \times \sqrt{D_{0_p} t_{pd}} \times \text{erfcinv}\left(\frac{C_{\text{sub}}}{C_{\text{surf}}}\right); \]

\[ x_{\text{ox}} = x_{\text{oxcm}} \times 10^7; \] %Oxide Mask Thickness in nm

\[ x_{\text{oxum}} = x_{\text{oxcm}} \times 10^4; \] %Oxide Mask Thickness in um

\[ B_{\text{ox}} = 0.5; \] %Parabolic Rate Constant for Oxide Mask in um^2/hr

\[ B_{\text{onA}_\text{ox}} = 5; \] %Linear Rate Constant for Oxide Mask in um^2/hr

%Time to Grow Wet Oxide Mask in hr

\[ t_{\text{ox}} = \left(\frac{(x_{\text{oxum}}^2)}{B_{\text{ox}}} \right) + \left(\frac{x_{\text{oxum}}}{B_{\text{onA}_\text{ox}}} \right); \]

\textbf{Table 11:} Diffusion and Doping Process Time Calculation MATLAB Script [21,22,23,24]