# Active Contact Lens – Low Power Backscattering Sensor-to-Antenna Integration Circuitry

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# *Abstract*

The Active Contact Lens measures the cornea-scleral radius of the wearer's eye, which correlates to intraocular pressure (IOP), Glaucoma's primary indicator. IOP varies throughout the day, and is drastically different from person to person, so constantly measuring it over a period of a few days can provide individualized tracking of the disease's development and will help doctors develop personalized treatment schedules to treat the disease more precisely.

The Active Contact Lens sensor measures strain, based on the cornea-scleral radius, and reports the results wirelessly, to allow monitoring of an individual's IOP over time. The lens is powered similarly to a passive RFID tag, so the device can operate long-term. The contact lens itself is clear, and biologically safe for the user. This allows the user to wear the device when asked by their doctor with no medical repercussions.

This document proposes part of the sensor-to-antenna integration circuitry. The whole design consists of three stages. The first stage is a Wheatstone bridge which converts the sensor's varying resistance into an analog voltage. The second stage is a biasing circuit which receives the analog voltage, amplifies it, and sets it within the determined input range for the third stage. The third and final stage, which this document focuses on, is a current-starved voltage-controlled ring oscillator (CSVCRO) that translates the voltage to frequency. The oscillator consists of 21 current starved CMOS inverters controlled by a current mirror biasing circuit. The final design has a frequency range of 736Hz to 38.58MHz, and an average power dissipation of 784.7 $\mu W$ at center frequency 23.4MHz. All circuitry was designed and simulated using 180nm CMOS technology.

# *Ch. 1: Introduction*

## 1.1 Background

The Gale Encyclopedia of Medicine defines Glaucoma as "a group of eye diseases characterized by damage to the optic nerve usually due to excessively high Intraocular Pressure (IOP)" [1]. Glaucoma causes very minimal pain, allowing it to remain undetected in humans for years, so doctors often can't treat it until its later stages. This makes the disease the second leading cause for blindness, responsible for about 10% of all cases of blindness worldwide and over 100,000 cases in the United States alone [2]. As Glaucoma develops, the affected person's IOP gradually increases from stunted flow of fluids out of the eye. The increased pressure damages the optic nerve, gradually degrading one's eyesight [3]. **Figure 1** and **Figure 2** show the general eye structure and how increased IOP prevents the flow of fluids out of the eye. Doctors have correlated higher IOP to a larger cornea-scleral radius of the eye [4]. As the pressure increases, the affected eye's condition gradually deteriorates, eventually leading to blindness.

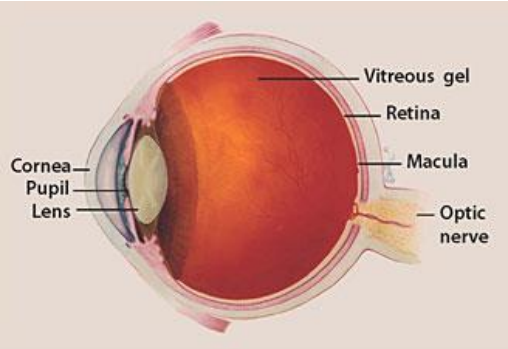



**Figure 1: Eye Structure [5]**

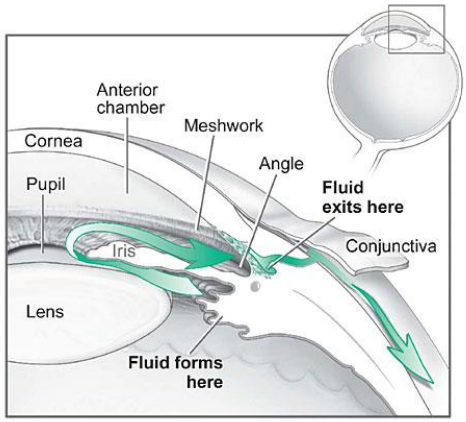



**Figure 2: Effects of Increased IOP on Eye Fluid Movement [5]**

No cure exists for Glaucoma, but doctors can treat the disease in its early stages to slow development [2]. As increased IOP is Glaucoma's main indicator, ophthalmologists measure this quantity in patients, and compare it to typical IOP levels, to check for Glaucoma. Tonometry is the standard method of measuring IOP, but current tonometry tests only measure instantaneous IOP [5]. As every person's IOP fluctuates constantly, these instantaneous measurements do not produce accurate data regarding an individual's average IOP. Many people also naturally have higher IOP than others, just like blood pressure and blood glucose levels vary between people, which makes determining the progression of Glaucoma problematic, as doctors have no standard IOP level that perfectly determines the presence of Glaucoma. Long-term tracking of an individual's IOP produces much more accurate data about the progression of the disease. Only one method in existence – Sensimed's Triggerfish contact lens shown in **Figure 3**– tracks IOP as it varies over time [6].

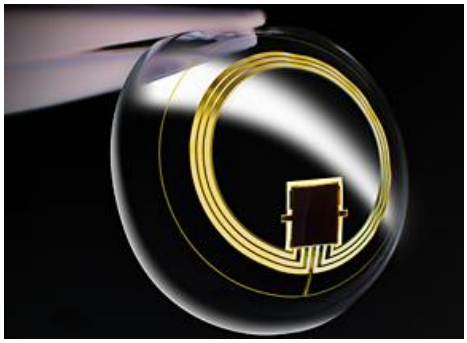


**Figure 3: Sensimed Triggerfish Contact Lens [6]**

## 1.2 Design Purpose

The Active Contact Lens improves on the Triggerfish design, measuring the wearer's cornea-scleral radius. The goal of the Active Contact Lens project is to design a product which the FDA may approve to sell in the US.

The Active Contact Lens sensor measures strain, based on the cornea-scleral radius, and reports the results wirelessly, to allow monitoring of an individual's IOP over time (see **Figure 4**). The lens is powered similarly to a passive RFID tag; it 'sleeps' until the antenna receives a communication signal, and the antenna recharges the local battery with power supplied by the received signal [10]. This allows the device to operate long-term. The contact lens itself is clear, and biologically safe for the user, so the user may wear the device whenever prompted by their doctor with no medical repercussions.

The project integrates a strain gauge, a spiral antenna, and an IC into a wearable contact lens. The strain gauge sensor detects the cornea-scleral radius of the eye, the radius where the cornea and the "white of the eye" meet. The device's internal circuitry encodes via ASK modulation this measured radius in a wireless signal that the antenna backscatters. The backscattered signal can be read by a computer interface such as a smartphone app, and the radius data decoded by the software.

A voltage-controlled oscillator in this system generates the frequency with which to modulate the backscattered signal, encoding the data of the user's eye radius. Oscillators have many design variables and constraints to choose from, including linearity, average power-dissipation, output frequency range, power supply sensitivity, and frequency stability. The Active Contact Lens project prioritizes low power dissipation and small layout size for long-term use of the wireless product. This document proposes an oscillator design for the system.

# *Ch. 2: System Design*

## 2.1 Backscatter Modulation – An Overview

The Active Contact Lens project utilizes a communication method called backscattering for data transmission. Backscattering is a passive communication method currently used with RFID tags. Utilizing an antenna's reflection capabilities, backscattering allows for wireless communication without actually generating and transmitting a signal on the "tag" end of the system. An antenna on the passive end merely receives a signal and reflects it, modulating the reflection. The desire data is encoded in the modulation of the reflected "backscattered" signal.

Because no signal is being produced from the passive end, however, the signal transmission distance significantly decreases. Traditional communication methods utilize both a transmitter and receiver on each end of the signal path, so the signal power received is given by the Friis Model's single path one way transmission equation

$$P_r = \frac{P_t G_t G_r \lambda^2}{(4\pi r)^2}$$

where $P_r$ and $P_t$ are the received and transmitted power, $G_r$ and $G_t$ the receiver and transmit antenna gains, $\lambda$ the signal wavelength, and r the distance between transmit and receive antennae [7].

However, backscatter modulation uses a passive transducer on one end, so the signal is attenuated on both forward and return paths. Because of this, the overall received power with backscatter modulation is

$$P_r = \frac{P_t G_t G_r \lambda^2 \Omega}{(4\pi)^3 r^4}$$

where the new term $\Omega$ is the "radar cross section" (RCS), the portion of incident signal power transmitted back to the source. The $\frac{1}{r^4}$ term dominates the received power equation, limiting the practical distance between the transmitter and tag/backscattering antenna [7].

While it places physical limitations on practical uses of the Active Contact Lens, utilizing this method of communication allows for ultra-low power dissipation in the circuitry.

## 2.2 High Level System Description

The integration circuitry as a whole has one purpose. It detects a change in the user's eye radius and transmits this radius wirelessly to a cell phone via backscattering, using ASK modulation to encode the data in the backscattered signal amplitude.

A block diagram for the general system is shown in **Figure 4**.

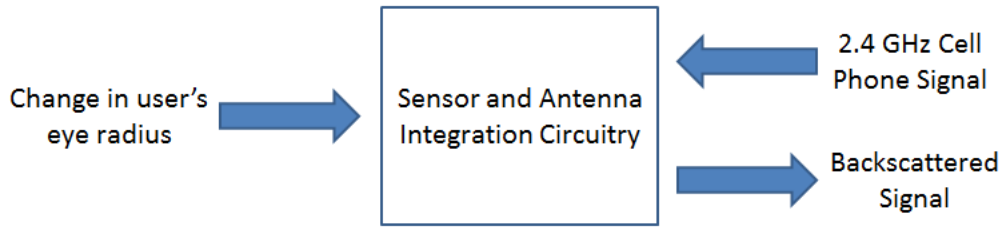



**Figure 4: High Level System Block Diagram**

## 2.3 High Level Circuit Breakdown

The integration circuitry has 3 main components: the sensor, a biasing circuit, and a voltage-controlled oscillator. A piezo-resistive strain gauge produces a variable resistance depending on the radius of the user's eye, which is translated to voltage by an appropriately designed Wheatstone Bridge circuit. The created voltage signal must be amplified to span the input range of the oscillator. These small voltage differences will run through a signal amplifier to a Ring Oscillator.

The VCO controls a switch that pulls the antenna to ground, effectively ASK modulating the backscattered signal. When the oscillator output transitions low, the switch closes, pulling the backscattered signal amplitude down towards 0V. When the oscillator output transitions high the switch opens, maintaining the backscattered signal amplitude.

This more detailed functionality is shown in the Level 1 Block Diagram in **Figure 5**.

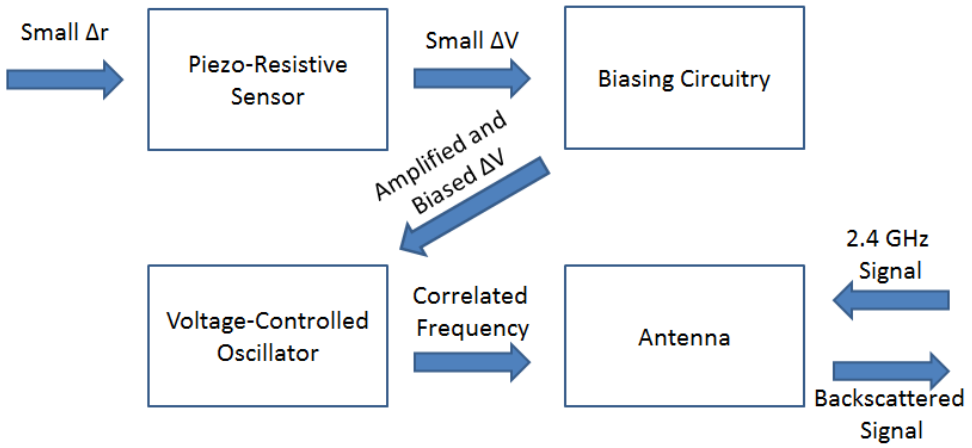



**Figure 5: Integration Circuitry Block Diagram**

## 2.4 Sensor Description

The proposed sensor for this system is a strain gauge, which varies in electrical properties as an external force acts on the material. The material used in this strain gauge is piezo-resistive, which varies electrical resistance. In order to integrate a piezo-resistive material and a VCO, the generated resistance must be converted into an analog voltage via the Wheatstone Bridge circuit shown in **Figure 6**. A typical configuration for the circuit is shown in **Figure 7**. This is most commonly used in with piezo-resistive sensors where $V_{out}$ is dependent on $\Delta R$.

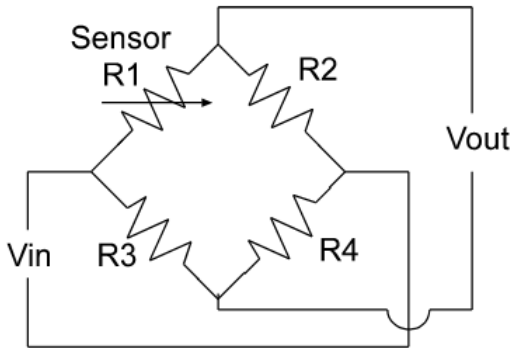



**Figure 6: Wheatstone Bridge Circuit**

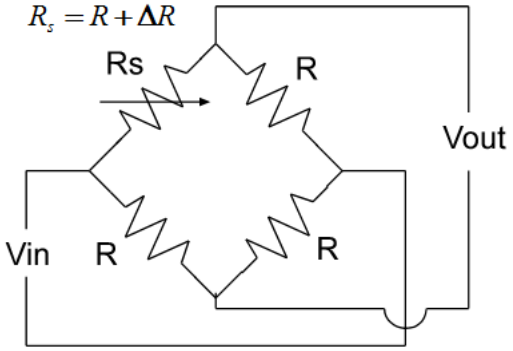



**Figure 7: Typical Wheatstone Bridge Configuration for Piezo-resistive Applications**

For this project application, $V_{in}$ is the reference voltage $V_{ref} = 2.5V$. The output $V_{out}$ can be determined as follows.

$$V_{out} = \left(\frac{R_2}{R_1+R_2} - \frac{R_4}{R_3+R_4}\right)V_{in} = \left(\frac{R}{R+(R+\Delta R)} - \frac{R}{2R}\right)V_{ref}$$

$$V_{out} = \left(\frac{R}{2R+\Delta R} - \frac{1}{2}\right)V_{ref} = \left(\frac{R}{2R+\Delta R} - \frac{R+\frac{\Delta R}{2}}{2\left(R+\frac{\Delta R}{2}\right)}\right)V_{ref}$$

$$V_{out} = \left(\frac{-\frac{\Delta R}{2}}{2R+\Delta R}\right)V_{ref}$$

To estimate values for such a circuit, choose a value for R that will pull a current $I_0 = 1mA$ from $V_{ref}$. Assuming infinite input impedance at $V_{out}$:

$$I_0 = \frac{V_{in}}{R_3+R_4} = \frac{V_{ref}}{2R} \rightarrow R = \frac{V_{ref}}{2I_0} = \frac{2.5}{2*mA}$$

$$R = 1.25k\Omega$$

With this resistance, a strain causing $\Delta R = 1\% * R = 125\Omega$ produces an output voltage of

$$V_{out} = \left(\frac{-\frac{125\Omega}{2}}{2*1.25k\Omega+125\Omega}\right)2.5 = -59.52mV$$

Typical changes in cornea-scleral radius of the eye will not produce changes of 10% in resistance, so $V_{out}$ will be much smaller, on the order of $10^{-6}$. The biasing circuit will amplify this to span 0.2V – 2V, the oscillator's ideal input range, to directly control output frequency with $\Delta R$.

# *Ch. 3: Oscillator Design*

Keeping practicality in mind throughout the design process, it's important to remember that the contact lens is a standalone, wireless device with its own low-voltage power supply. Due to the size constraints of the system, the power supply does not have a large storage capability, which means the circuitry in the IC must, before anything else, be a small and power efficient design. Wider frequency ranges make decoding the eye radius data more accurate, so reasonably large frequency range is another design goal.

Many different VCO designs exist, including LC oscillators (see **Figure 9**), source-coupled oscillators, and phase-shift VCOs which use multiple RC stages. While these circuits certainly function, the oscillator design most suitable for this application is a current-starved ring oscillator using CMOS technology inverter stages (see **Figure 8**). Ring oscillators have larger tuning frequency ranges, and much smaller layout sizes than LC oscillators, and they don't depend on fabricating large capacitors like source-coupled oscillators [8]. The use of CMOS transistors also increases power efficiency, as MOSFETs are not energy-dissipating circuit components.

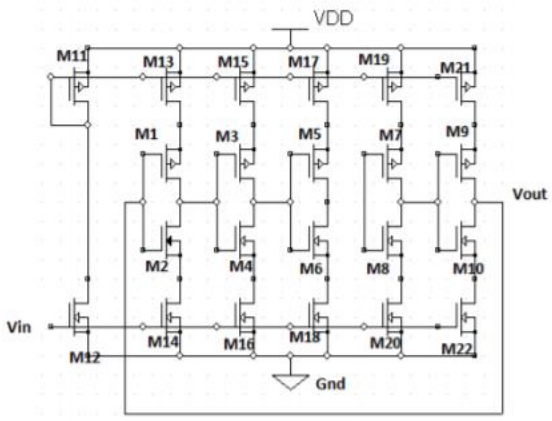



**Figure 8: Current Starved CMOS Ring Oscillator [8]**

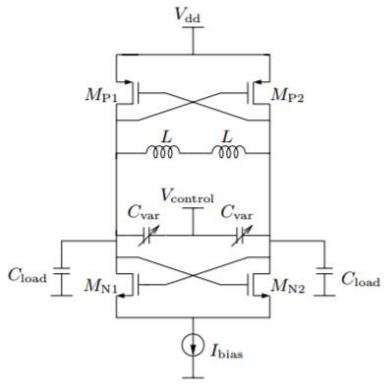



**Figure 9: Complementary LC Oscillator [9]**

This oscillator design assumes a stable voltage reference, as a voltage reference was previously designed for the project [10]. Linearity of the output frequency does not matter because the oscillator can be characterized over an appropriate range of input voltages.

Something else to note is that recent advances in technology allow us to scale down transistor sizes while maintaining, and even increasing, electrical performance. The smaller MOSFET size in recent technology reduces gate delays as well as power consumption. Smaller MOSFET sizes do however introduce short channel effects to the circuit operation. MOSFETs with channel length on the order of $10^{-9}$ have higher leakage currents which increase power losses. They also experience velocity saturation which decreases current drive. One of the more impactful short channel effects on oscillator performance is Drain Induced Barrier Lowering (DIBL), which decreases the gate voltage's control over MOSFET operation. In order to avoid these severe short channel effects, MOSFET channel sizes were decided to be greater than $1\mu m$.

# *Ch. 4: Inverter Stage Design*

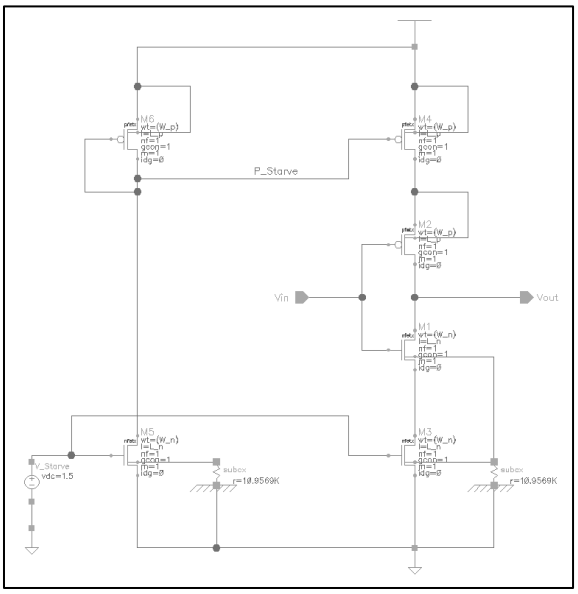



**Figure 10: Current Starved CMOS Inverter**

## 4.1 Balanced CMOS Inverters

According to given characteristics of the manufacturing process used, the process transconductance parameters for NMOS and PMOS devices are related by:

$$k_n' = 4.7 * k_p'$$

This means that for a balanced Inverter,

$$\frac{W_p}{L_p} = 4.7 * \frac{W_n}{L_n}$$

Since the channel length values L are the same for both NMOS and PMOS transistors, we get that

$$W_p = 4.7 * W_n$$
$$L_p = L_n$$

## 4.2 Short Channel Effects

Certain phenomena occur when MOSFET channel lengths decrease to the order of the transistor's depletion layer width, most all of which decrease device performance and should be avoided if possible.

Drain Induced Barrier Lowering (DIBL) causes coupling between the drain and source, making the current $I_d$ more dependent on $V_{DS}$ and less dependent on $V_{GS}$. This makes a FET harder to control with the gate voltage, which inhibit the correlation between input voltage and output frequency of the oscillator.

Larger subthreshold and leakage currents significantly increase power dissipation. In short channel devices, static power dissipation is not negligible. Furthermore, reduced threshold voltage makes transistors more difficult to turn off, which would impact the logic transitions of the oscillator and cause more power dissipation from residual current flow at lower gate voltages.

Velocity saturation also decreases the current drive of a transistor. In the oscillator, this would limit the output frequency range.

## 4.3 Inverter Power Dissipation

Even though this oscillator and the associated circuitry isn't digital, it is designed using CMOS technology, and follows the same theoretical trends as CMOS logic gates. There are three main types of power dissipation in CMOS based logic circuits: static power dissipation from subthreshold leakage currents, dynamic power dissipation from charging and discharging the virtual capacitors, and short circuit power dissipation when both PMOS and NMOS transistors conduct current during logic state transitions. The vast majority of power dissipation, however, can be summed up in the static and dynamic/switching power.

### 4.3.1 STATIC POWER

Ideally, no drain current flows through a MOSFET when the Gate-Source voltage $V_{GS}$ is lesser than the threshold voltage $V_{TH}$. Realistically however, there is some subthreshold current that flows through the device even in its "off" state. For transistors uninhibited from short channel effects, this subthreshold current is almost negligible, but important in final design power analysis for accurate performance description.

### 4.3.2 DYNAMIC SWITCHING POWER

Power is also dissipated when the inverter output switches from 'low' to 'high'. As the transistor gates charge the load capacitance $C_{tot}$ at a frequency $f$, the switching power can be calculated as

$$P_{switching} = C_L * V_{DD}^2 * f * N_{SW} * p_{0-1} = \frac{1}{2} C_L V_{DD}^2 * f * N_{SW}.$$

As the reference $V_{DD}$ is set at 2.5 V, this leaves C and $t_d$ as design parameters for minimizing power loss. Increasing the propagation delay per stage, then, would significantly decrease power consumption. If the input capacitance per stage increases in proportions more than $t_d$, however, a higher oscillation frequency would be more efficient.

## 4.4 Optimizing Inverter Performance

### 4.4.1 OSCILLATOR FREQUENCY

The period of a ring oscillator is given by the equation $T = 2 * N * t_d$ where N is the number of delay stages in the oscillator, and $t_d$ is the average propagation delay time per inverter [2]. The oscillation frequency is then

$f_0 = \frac{1}{T} = \frac{1}{2Nt_d}$. Thus, the oscillation frequency can be set by tuning the propagation delay of each inverter stage, and by changing the number of delay stages.

For the Active Contact Lens project, the system input is strain from eye pressure. Eye pressure changes slowly, over minutes and hours. This negates the need for high frequency signals in the contact lens. The only constraint is that to utilize ASK modulation, the oscillation frequency must be lower than that of the signal received at the antenna, which is 2.4GHz. To decrease dynamic power losses as much as possible, the oscillator frequency was chosen to be 1MHz. Lower frequencies require larger capacitances or more inverter delay stages in the oscillator, both of which increase dynamic power dissipation and required space in the IC.

### 4.4.2 MOSFET SIZING

I chose to use channel length $l = 1\mu m$, large enough to avoid serious performance degradation due to short channel effects, but still small enough to reduce power dissipation. I chose to start with an aspect ratio $\frac{W}{L} = 4$ for the NMOS transistors. A smaller aspect ratio would reduce transistors' current drive, limiting the frequency range of the

oscillator. But using too large channel widths will increase parasitic capacitances and subsequently, the dynamic power dissipation in the oscillator. This aspect ratio gives channel width values of $W_n = 4 * L_n = 4\mu m$ and to balance the PMOS and NMOS transistors, $W_p = 4.7 * W_n = 18.8\mu m$.

## 4.5 Inverter Timing

Time delays occur in CMOS transistors when switching between logic levels due to parasitic capacitances and non-zero resistances of MOSFETs. The total capacitance at one inverter's output can be calculated as $C_{tot} = C_{in} + C_{out}$ where $C_{in}$ and $C_{out}$ are the inverter's input and output capacitance respectively.

Capacitance looking from the input into an inverter consists of the gate capacitances of the inverting transistors M1 and M2. This value depends largely on the oxide capacitance $C_{ox}$ of the manufacturing process used as shown in **4.5.1 Inverter Stage Input Capacitances**.

Capacitance looking from the output into an inverter consists of the drain capacitances of the inverting transistors M1 and M2 as shown in **4.5.2 Estimation of Inverter Output Capacitance and MOSFET Resistance**.

### 4.5.1 INVERTER STAGE INPUT CAPACITANCES

The gate capacitance of a MOSFET depends on the transistor's region of operation. In the saturation region, the gate capacitances are $C_{GS-sat} = \frac{2}{3}C_{GS}$ and $C_{GD-sat} = \frac{2}{3}C_{GD}$ where $C_{GS}$ and $C_{GD}$ are the capacitances in cutoff. Furthermore, due to the miller effect, $C_{GD}$ doubles the expected value when looking into a CMOS inverter.

The total gate capacitances looking from the output of one inverter into next inverter stage, can then be estimated by the instantaneous logic state of the inverters input. In the following calculations, $C_{ox}, C_{GSO},$ and $C_{GDO}$ are manufacturing process' parameters from the MOSFET model file used in Cadence.

#### 4.5.1.1 Logic High Input Capacitance:

$$C_{in} = C_{Gate-sat_{nmos}} + C_{Gate-off_{pmos}}$$

$$= \left(C_{GSov} + \frac{2}{3}C_{GS} + C_{GDov} + \frac{2}{3}(2C_{GD})\right)_{nmos} + (C_{GSov} + C_{GS} + C_{GDov} + 2C_{GD})_{pmos}$$

$$= \left(WC_{GSO} + \frac{2}{3}WLC_{ox} + WC_{GDO} + \frac{4}{3}WLC_{ox}\right)_{nmos} + (WC_{GSO} + WLC_{ox} + WC_{GDO} + 2WLC_{ox})_{pmos}$$

$$= 6.5384(10)^{-14}\ F + 1.65937(10)^{-13} F$$

$$\boldsymbol{C_{in-high} = 2.31321(10)^{-13}\ F}$$

#### 4.5.1.2 Logic Low Input Capacitance:

$$C_{in} = C_{Gate-off_{nmos}} + C_{Gate-sat_{pmos}}$$

$$= (C_{GSov} + C_{GS} + C_{GDov} + (2C_{GD}))_{nmos} + \left(C_{GSov} + \frac{2}{3}C_{GS} + C_{GDov} + \frac{2}{3}(2C_{GD})\right)_{pmos}$$

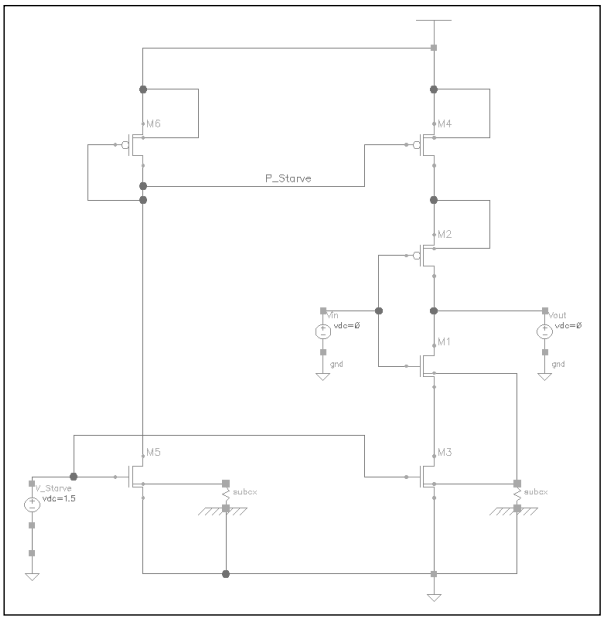
$$= (WC_{GSO} + WLC_{ox} + WC_{GDO} + 2WLC_{ox})_{nmos} + \left(WC_{GSO} + \frac{2}{3}WLC_{ox} + WC_{GDO} + \frac{4}{3}WLC_{ox}\right)_{pmos}$$

$$= 9.6076(10)^{-14} F + 3.07305(10)^{-13} F$$

$$C_{in-low} = 4.03381(10)^{-13}\ F$$

## 4.5.2 ESTIMATION OF INVERTER OUTPUT CAPACITANCE AND MOSFET RESISTANCE

Characterizing an individual MOSFET using its IV curve isn't as useful for this circuit, because $V_{DS}$ and $V_{GS}$ values fluctuate constantly. Simulating an inverter stage and looking at the DC operating point provides a more accurate estimate of parasitic capacitances and on-resistance values. This was simulated using the Cadence simulation profile *Senior_Project\Ring_VCO_Starved_Stage_with_Bias\DC_op*.




Simulating a low-to-high output transition:

Setting both $V_{in}$ and $V_{out}$ to 0 V puts both NMOS transistors in cutoff and forces the PMOS transistors into the active region of operation. This mimics the circuit's behavior at the beginning of $t_{PlH}$ transitions.

Simulating a high-to-low output transition:

Setting both $V_{in}$ and $V_{out}$ to $V_{DD}$ = 2.5 V puts the PMOS transistors in cutoff and forces both NMOS' into active the region of operation. This mimics the circuit's behavior at the beginning of $t_{PHL}$ transitions.

Printing the DC operating point for both PMOS transistors in the low-to-high transition and the NMOS' in the high-to-low transition yields the results displayed in **Table 1**.

**Figure 11: Inverter DC Operating Point Test Circuit**

**Table 1: Inverter Simulated Output Parameters**

| | | $R_{out}$ [Ω] | $C_{dg}$ [$F$] | $C_{ds}$ [$F$] | $C_{db}$ [$F$] |
|---|---|---|---|---|---|
| Logic High Input ($t_{PHL}$) | M2 | ---- | 1.987a | -891.2z | 686.7z |
| | M1 | 58.99k | 8.083f | -9.298f | 1.419f |
| | M3 | 13.09k | ---- | ---- | ---- |
| Logic Low Input ($t_{PLH}$) | M4 | 28.58k | ---- | ---- | ---- |
| | M2 | 69.4k | 32.94f | -40.72f | 8.854f |
| | M1 | ---- | 536.8z | -228.4z | 148.4z |

Values shown as "----" in **Table 1** are insignificant for propagation delay estimation. In measuring $t_{PHL}$, the PMOS transistors M2 and M4 operate in cutoff, and the resistance the inverter's output discharges through relies solely on the NMOS transistors M1 and M3. In measuring $t_{PLH}$ the opposite is true; the NMOS transistors M1 and M3 operate in cutoff, and the output-charging time constant relies solely on the PMOS transistors' resistances. Also, the starving

transistors M3 and M4 don't affect the inverter's output capacitance $C_{out}$ nearly as much as the inverting transistors M1 and M2, and can be ignored.

Note that capacitances shown in **Table 1** are mathematical matrix elements calculated in cadence, and thus can have negative values, even though real capacitances are always positive. For example, $C_{dg}$ is estimated as $\frac{\mathrm{d}Q_d}{\mathrm{d}V_g}$ in the computed matrix and can be negative if leakage charge flows from gate to drain in a simulation.

#### 4.5.2.1 Logic High Output Capacitance:

In the following calculation, $C_{dg}, C_{ds},$ and $C_{db}$ are simulated DC operating point values given in **Table 1**.

$$C_{out} = C_{Drain-nmos} + C_{Drain-pmos} = \left(C_{dg} + C_{ds} + C_{db}\right)_{nmos} + \left(C_{dg} + C_{ds} + C_{db}\right)_{pmos}$$

$$C_{out-high} = 1.88036(10)^{-14}F$$

#### 4.5.2.2 Logic Low Output Capacitance:

In the following calculation, $C_{dg}, C_{ds},$ and $C_{db}$ are simulated DC operating point values given in **Table 1**.

$$C_{out} = C_{Drain-nmos} + C_{Drain-pmos} = \left(C_{dg} + C_{ds} + C_{db}\right)_{nmos} + \left(C_{dg} + C_{ds} + C_{db}\right)_{pmos}$$

$$C_{out-low} = 8.25149(10)^{-14}\ F$$

### 4.5.3 PROPAGATION TIME DELAYS

Propagation delay time is defined as the time it takes the inverter output to reach the "50% point" of a transition. For this oscillator, however, the 50% points don't have any significance. The actual transition time of import with this oscillator is when $V_{out} = V_{SS} + 2V_{TN}$ for $\tau_{phl}$ and $V_{out} = V_{DD} - 2V_{TP}$ for $\tau_{plh}$. These points in the transition activate the NMOS and PMOS transistors in the following inverter stage, causing the next transition to begin.

The propagation time delay per stage can be estimated by an RC time constant where the capacitance C is the combined input and output capacitance of an inverter stage [11] – and the resistance R is the active transistors' on resistance.

Simple RC time delays can be calculated with the following formula.

$$v(t) = V_{final} - \left(V_{final} - V_{initial}\right)e^{-\frac{\Delta t}{\tau}}$$

$$-\frac{\Delta t}{\tau} = \ln\left[\frac{v(t) - V_{final}}{-(V_{final} - V_{initial})}\right]$$

$$\Delta t = -\tau \ln\left[\frac{V_{final} - v(t)}{V_{final} - V_{initial}}\right]$$

There are two different propagation delay times: the high-to-low propagation delay $t_{PHL}$ and the low-to-high propagation delay $t_{PLH}$.

The delay $t_{PHL}$ is calculated using the on resistance of the NMOS transistors below the output node, and it has a $V_{final}$ of $V_{SS}$ and a $V_{initial}$ of $V_{DD}$. The delay $t_{PLH}$ is calculated using the on resistance of the PMOS transistors above the output node, and it has a $V_{final}$ of $V_{DD}$ and a $V_{initial}$ of $V_{SS}$.

$$v_{out}(t_{PLH}) = V_{DD} - 2V_{TP} = 2.5 - 2(0.7) = 1.1V$$

$$v_{out}(t_{PHL}) = V_{SS} + 2V_{TN} = 0 + 2(0.4) = 0.8V$$

Thus, the propagation delay times can be estimated:

$$t_{PLH} = -(R_{Pstarve} + R_{Pinv})(C_{in-Low} + C_{out-low}) \ln\left[\frac{V_{DD} - v_{out}(t_{PLH})}{V_{DD} - 0}\right]$$

$$= -(28.58k\Omega + 69.4\text{k}\Omega)(4.03381(10)^{-13}F + 8.25149(10)^{-14}F) \ln\left[\frac{2.5-1.1}{2.5}\right]$$

$$t_{PLH} = 27.604ns$$

$$t_{PHL} = -(R_{NStarve} + R_{Ninv})\left(C_{in-high} + C_{out-high}\right) \ln\left[\frac{0 - v_{out}(t_{PHL})}{0 - V_{DD}}\right]$$

$$= -(13.09k\Omega + 58.99k\Omega)(2.31321(10)^{-13}F + 1.88036(10)^{-14}F) \ln\left[\frac{-0.8}{-2.5}\right]$$

$$t_{PHL} = 20.5428ns$$

$$\tau_p = \frac{t_{PHL} + t_{PLH}}{2} = 24.0734ns$$

## 4.5.4 NUMBER OF INVERTER STAGES IN OSCILLATOR

Calculating the number of stages N required in the oscillator for a frequency of 1MHz with this average propagation delay time per inverter yields

$$f = \frac{1}{2Nt_d} \rightarrow N = \frac{1}{2ft_d} = \frac{1}{2*1MHz*24.0734ns} = 20.7698 \cong 21 \text{ stages.}$$

## 4.5.5 ESTIMATING OSCILLATOR POWER DISSIPATION

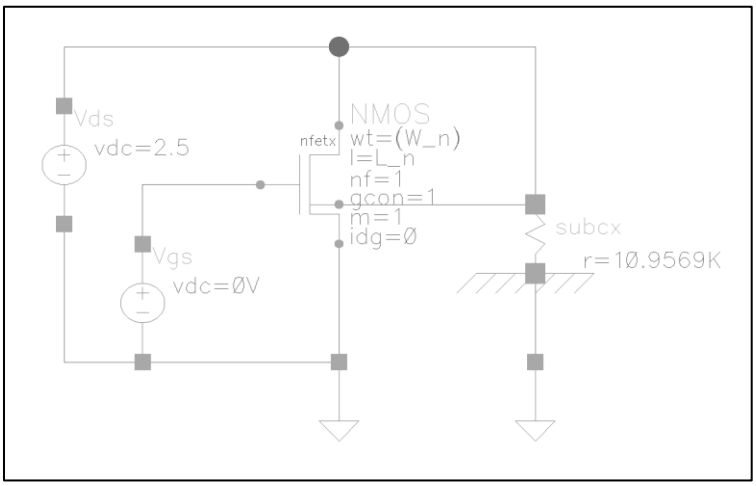



**Figure 12: NMOS Leakage Characterization Circuit**

The static power dissipated by the oscillator was estimated using the characterization circuit shown in **Figure 12**, in the Cadence simulation profile *Senior_Project\Characterize_NMOS\Leakage_Current*. The transistor voltages were set to $V_{DS} = 2.5\ V$ and $V_{GS} = 0\ V$ and the drain current of the NMOS was measured at 935nA. This would provide a leakage dissipation of about $935nA * 2.5V * 21\ inverters * \frac{1}{2} = 24.54\mu W$.

As shown in **4.3.2 Dynamic Switching Power**, dynamic power can be estimated with the equation $P_{sw} = \frac{1}{2} C_L V_{DD}^2 * f * N_{SW}$ . Using an average of the logic-high and logic-low capacitances for $C_L$ and setting $f = 23.4MHz, V_{DD} = 2.5V$, and $N = 21$ stages yields the following result.

$$P_{sw} = \frac{1}{2} * \left[\frac{(C_{in-low} + C_{out-low}) + (C_{in-high} + C_{out-high})}{2}\right] * 2.5^2 * 23.4(10)^6 * 21$$

$$P_{sw} \cong 565.126\mu W$$

The total power dissipation of the circuit is then

$$P_{tot} = P_{leakage} + P_{sw} = 24.54\mu W + 565\mu W = \mathbf{589.669\mu W.}$$

# *Ch. 5: Results*

## 5.1 Final Circuit Design and Simulation

The final design of the oscillator stage is shown in **Figure 13**. The schematic is from the Cadence Virtuoso cell *Senior_Project\Starved_Inverter_Biased*.

Final channel width and length values are

$L_n = L_p = 1\mu m$, $W_p = 18.8\mu m$, and $W_n = 4\mu m$.

**Figure 14** displays the output waveform for the optimum range of $V_{IN}$ (0.6V – 1.6V). Within this range, $f_{osc}$ increases by about 2MHz for every 50mV step in $V_{IN}$.

This simulation used Cadence simulation profile *Senior_Project\Ring_VCO\Increasing_Freq*.

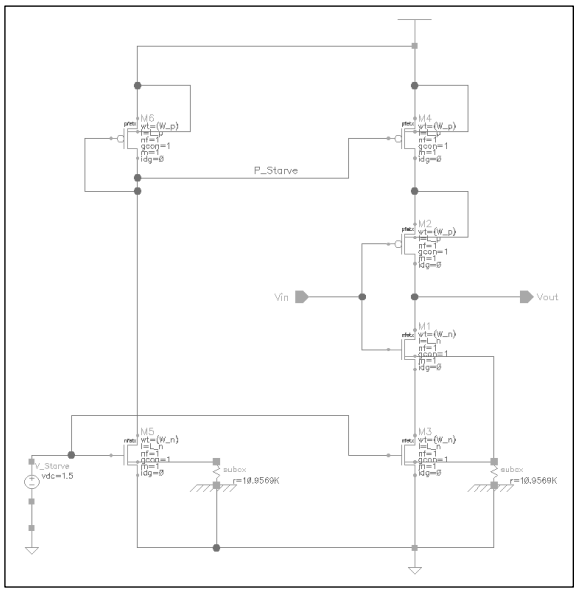



**Figure 13: Final Oscillator Stage Design**

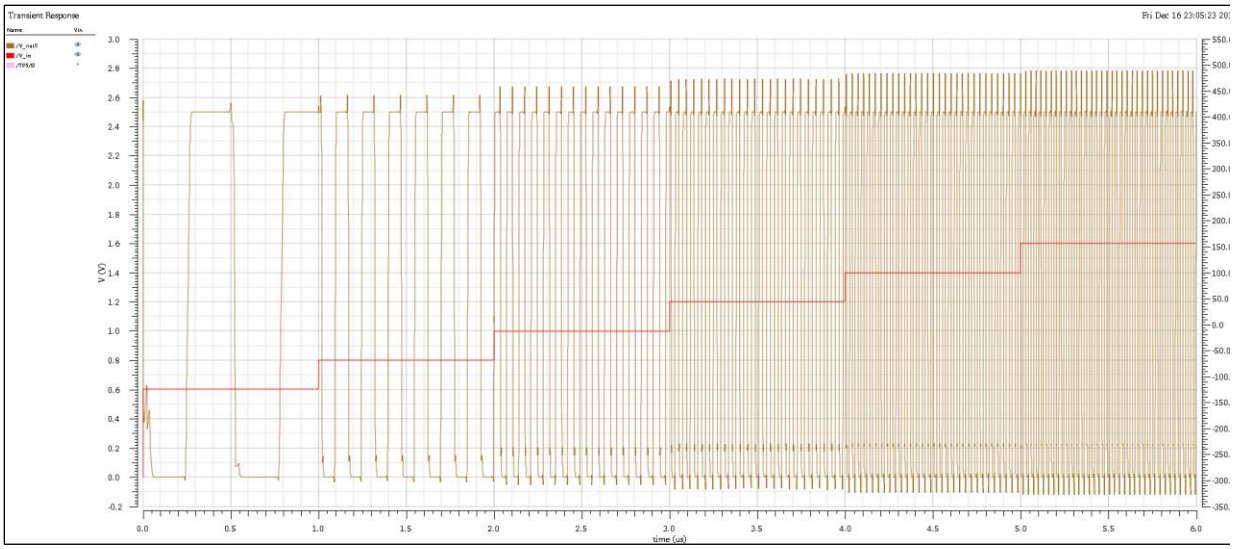



**Figure 14: Output Frequency with Varying $V_{IN}$**

**Figure 14** shows the circuit's response (brown) to a changing input (red) over the optimum input range. The oscillation frequency varies from 1.88 MHz to 34.54 MHz in this simulation. The oscillator has a wider input range than is shown in this simulation, but within this range, the frequency increases almost linearly, as shown in **Table 2**.

The individual inverter's propagation delay was also measured using a Cadence simulation cell titled *Starved_Inverter_Prop_Delays*. **Figure 15** shows the low-to-high propagation delay (red) measured using the cadence simulation profile *Tplh_meas*.

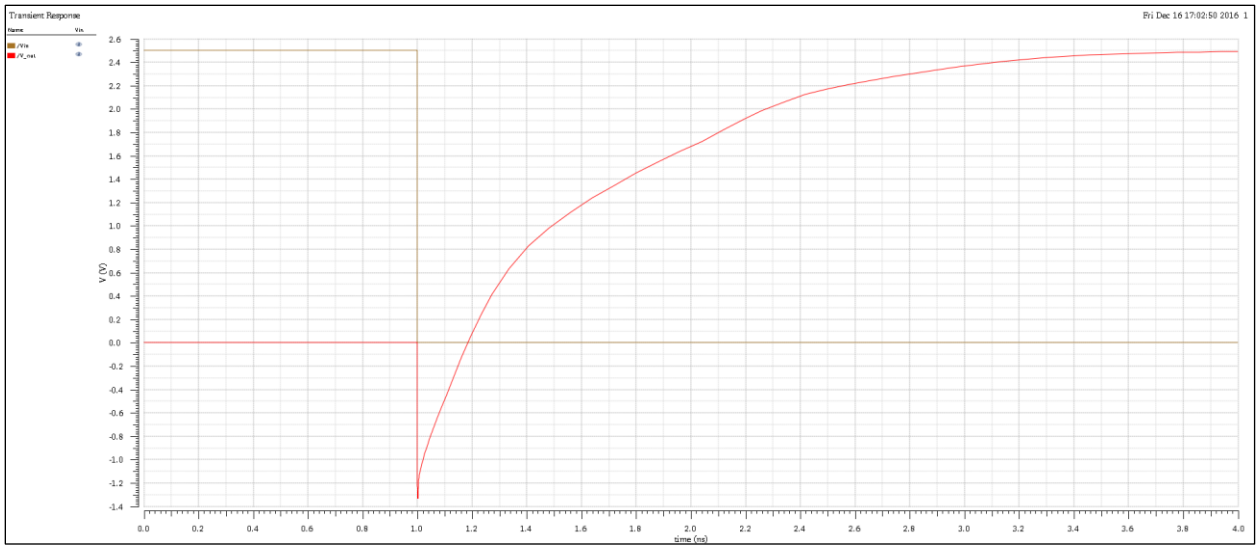



**Figure 15: Inverter Low-to-High Propagation Delay ($t_{PLH}$)**

The output delay shown above in Figure 15 shows a delay time of about 0.6ns, which is much shorter than the predicted in **4.5.3 Propagation Time Delays**.

Figure 16 below shows the high-to-low propagation delay (red), which was measured using the cadence simulation profile *Tphl_meas*. This time delay is about 0.7ns, which is also much shorter than predicted in **4.5.3 Propagation Time Delays**.

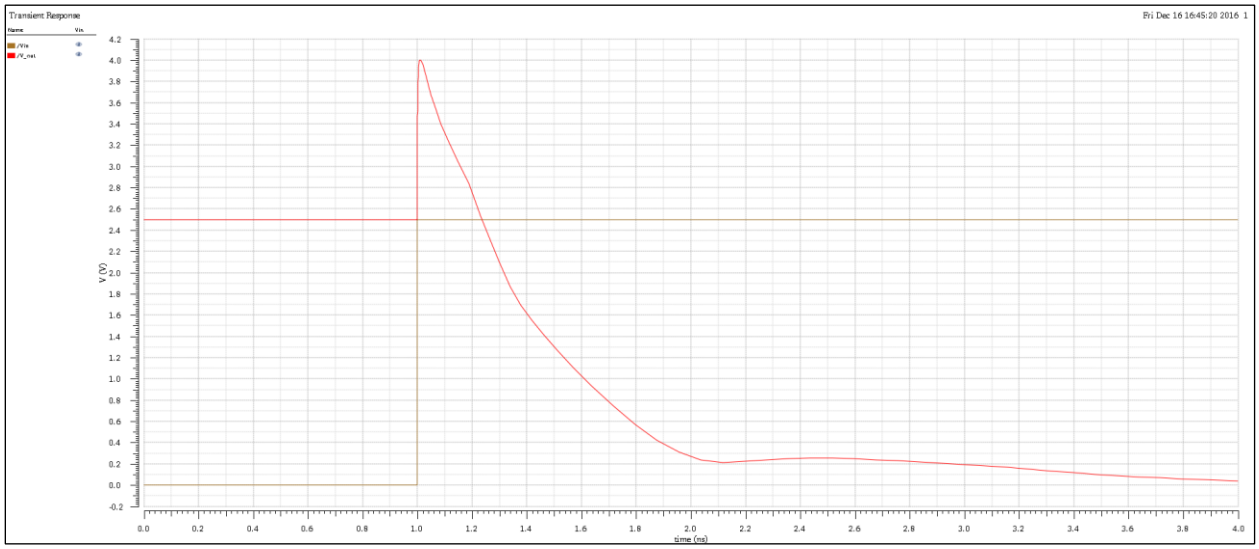



**Figure 16: Inverter High-to-Low Propagation Delay ($t_{PHL}$)**

## 5.2 Output Characterization

Data detailing the oscillator's output characteristics is shown in **Table 2**. The table provides data pairs characterizing Input Voltage to Output Frequency and spans an input range of 0.2V to 2.4V. This data was taken using the Cadence simulation profile *Senior_Project\Ring_VCO\Single_Input_Freq*. In order to get a clean frequency measurement, one simulation was run per data pair.

From the *Ring_VCO* schematic V_out5, the output of the 5$^{th}$ inverter stage, was plotted in a transient simulation. After each simulation in Cadence ADE, the calculator was used to measure the frequency of the V_out5 signal. One simulation was run per value of $V_{IN}$. For each value of $V_{IN}$, the transient simulation stop time was adjusted appropriately to plot several periods of the V_out5 signal for accurate frequency measurements.

**Table 2: Oscillation Frequency vs. Input Voltage**

| $V_{in}$ $[V]$ | $f_{out}$ $[Hz]$ | $V_{in}$ $[V]$ | $f_{out}$ $[Hz]$ | $V_{in}$ $[V]$ | $f_{out}$ $[Hz]$ |
|---|---|---|---|---|---|
| 0.2 | 736.42 | 0.95 | 12.38 E+6 | 1.7 | 36.05 E+6 |
| 0.25 | 3.021 E+3 | 1.0 | 14.37 E+6 | 1.75 | 36.62 E+6 5 |
| 0.3 | 13.24 E+3 | 1.05 | 16.52 E+6 | 1.8 | 37.17 E+6 |
| 0.35 | 46.77 E+3 | 1.1 | 18.62 E+6 | 1.85 | 37.6 E+6 |
| 0.4 | 142.7 E+3 | 1.15 | 20.88 E+6 | 1.9 | 37.99 E+6 |
| 0.45 | 348.6 E+3 | 1.2 | 22.87 E+6 | 1.95 | 38.2914 E+6 |
| 0.5 | 693.3 E+3 | 1.25 | 24.86 E+6 | 2.0 | 38.6271 E+6 |
| 0.55 | 1.199 E+6 | 1.3 | 26.74 E+6 | 2.05 | 38.9016 E+6 |
| 0.6 | 1.88 E+6 | 1.35 | 28.46 E+6 | 2.1 | 39.1569 E+6 |
| 0.65 | 2.845 E+6 | 1.4 | 30.0 E+6 | 2.15 | 39.3374 E+6 |
| 0.7 | 4.114 E+6 | 1.45 | 31.39 E+6 | 2.2 | 39.5809 E+6 |
| 0.75 | 5.425 E+6 | 1.5 | 32.61 E+6 | 2.25 | 39.7373 E+6 |
| 0.8 | 6.856 E+6 | 1.55 | 33.64 E+6 | 2.3 | 39.895 E+6 |
| 0.85 | 8.68 E+6 | 1.6 | 34.54 E+6 | 2.35 | 40.0421 E+6 |
| 0.9 | 10.28 E+6 | 1.65 | 35.34 E+6 | 2.4 | 40.1728 E+6 |

## 5.3 Power Analysis of Final Design

Using the Cadence simulation profile *Senior_Project\Ring_CVO\Energy_per_Stage*, the total current drive was estimated over one period of oscillation for a single inverter stage. A transient simulation was run for the whole oscillator, and the Source current of the starving PMOS (M4) was plotted in **Figure 17**.

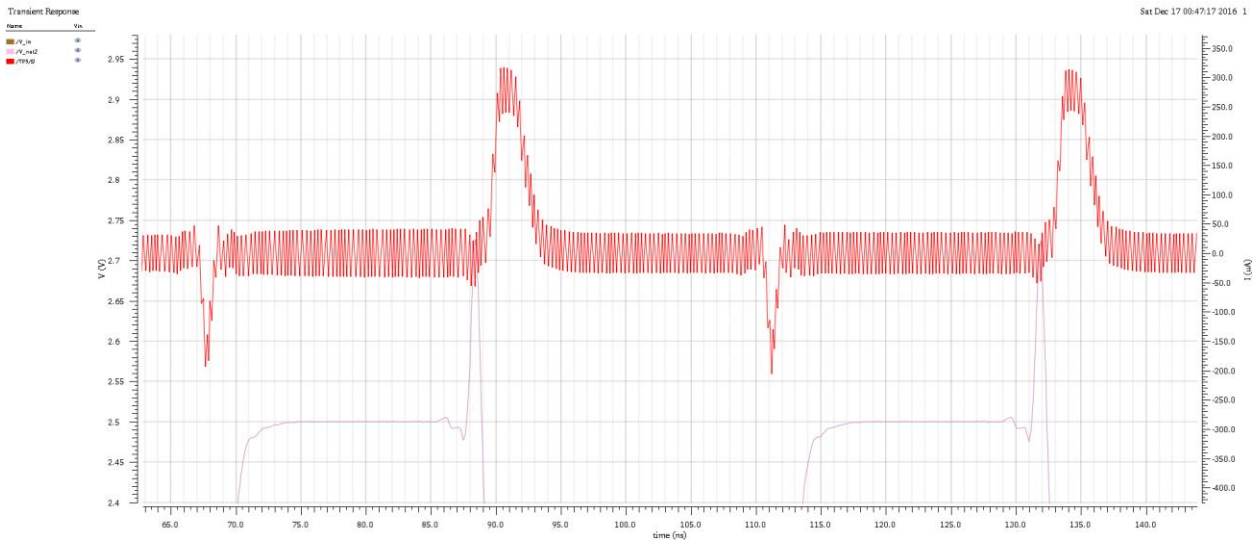



**Figure 17: Energy Calculation Waveform of Current through PMOS from Vdd**

The M4 transistor's current accounts for all power dissipated, as it is the only current supplied directly by the power source for the inverter. Integrated over time, this current may be used to calculate the average power of the circuit. The current waveform was imported to Cadence ADE's calculator and integrated over a period with the following command: **Integ(i("/TP5/S" ?result "tran") 90.07742n 133.5301n)**. The calculation resulted in a value of $642.7(10)^{-15}\ [A * s]$, providing an average power dissipation per inverter stage of

$$P_{avg} = \frac{1}{T}\int P(t)\,dt = \frac{1}{T}\int i(t) * V_{CC}\,dt = \frac{V_{CC}}{T}\int_0^T i(t)dt = \frac{2.5V}{133ns - 90ns} * \int_{90ns}^{133ns} i(\text{"TP5/S"})\,dt$$

$$P_{avg} = \frac{2.5V}{43ns} * 642.7(10)^{-15}\ [A * s] = 37.366\mu W\ .$$

The total power dissipation of the circuit is then

$$P_{tot} = \frac{P_{avg}}{inverter} * N = 37.366\,\frac{\mu W}{inverter} * 21\ inverters = \mathbf{784.692\mu W}.$$

This power is a little larger than the expected power from **4.5.5 Estimating Oscillator Power Dissipation**. The calculated power, however, did not account for short circuit dissipation, which at high frequencies can account for a decent portion of total power losses.

## 5.4 Conclusions

The final oscillator design has an average power dissipation of about $785\mu W$, which is much larger than the $55.3\mu W$ in [11]. The main factors playing into this difference was the size of the fabrication process used and the MOSFETs used in the circuitry; the $55.3\mu W$ design used 45nm CMOS technology while this design used 180nm CMOS technology with transistors sizes in the $1\mu m$ range to avoid short channel effects.

In order to further improve power efficiency, different MOSFETs must be used in the design process. The standard nfetx and pfetx MOSFET model files used in these simulations will incur serious short channel effects if the channel sizes are decreased too much, which will increase leakage currents, and inhibit the oscillator's performance. Double-gated Silicon-on-Insulator (SOI) devices have accurate threshold control, lower parasitic capacitances leading to lower dynamic power, and smaller leakage currents than standard FETs; however, they are much more expensive to fabricate. If such devices were used in the fabrication process, MOSFET sizes could be reduced much more while maintaining low power dissipation and control of output frequency.

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# *Appendix A. Senior Project Analysis*

## Summary of Requirements

This project integrates the device sensor to the antenna that transmits data. The sensor measures the user's intraocular eye pressure with a piezo-electric that produces a voltage difference as a force acts on the piezo-electric material. The sensor integration circuitry takes this voltage and backscatters a signal received from the antenna. This backscattered signal contains the information on the user's eye pressure.

## Primary Constraints

The largest challenge associated with designing this circuitry is maintaining high accuracy with the measurements of the wearer's cornea-scleral radius. Outputting a signal representing the change in eye radius and interpreting that signal within 2% accuracy compared to the actual measurement proves more difficult than just getting the job done. The small size of the project creates the second main constraint. To meet the size constraints, we must micro-fabricate all the device circuitry on the micron level, placing all the electronics on one IC chip. Because of this, we must minimize the physical size of the integration circuitry. Satisfying both the accuracy and size constraints proves difficult.

## Economic Impacts

*Human Capital* –The Active Contact Lens inspires extensive research within the field of detecting Glaucoma. It also provides jobs for doctors and engineers performing research and developing the product, as well as doctors that work with the patients. Ophthalmologists' jobs in particular change with the development of the Active Contact Lens, as they monitor the patients and perform checkups when needed. The device helps catch Glaucoma before in patients, allowing for earlier treatment. This will cause each patient to work more efficiently for a longer period of time.

*Financial Capital* – All the circuitry in the device has to be micro fabricated, which costs an estimated per device. This has been provided in the past by the Cal Poly Biomedical Engineering department, which will hopefully keep funding it in the future.

*Manufactured or Real Capital* – A unanimous company provided a material to be used as the contact lens substrate – the lens itself – that they manufactured specifically for Cal Poly to "do something cool with". The manufacturing process also requires many special tools and fabrication machines. Masks must be built for the micro fabrication, which uses a specific mask-making machine, and there are also other fabrication processes that require very particular, expensive tools to be performed.

*Natural Capital* – This project uses quite a bit of minerals and natural resources that are mined from the Earth. The fabrication process and circuit fabrication, because of the small size of the project, use very specific amounts of elements like silicon and tin, and also have very precise doping specifications for the IC design.

*Project Inputs* – The Active Contact Lens project's research requires a lot of financial input for the fabrication and manufacturing processes in the test phases. It also requires some manufactured input from the requested company, as they are providing the material used for the contact lens itself.
*Project Lifecycle* – The most expensive stage in the project's lifecycle is the "Build" phase. The expenses come mostly from the micro fabrication tools required to manufacture the project components. The "Design" phase of the project really only costs time, which would be the main cost, if the researchers were paid.
*Project Estimated Cost* – this project is expected to cost a total of about $4,500 in research, as shown in the Project Cost Estimate in **Table 3**. The main cost is the micro fabrication of the materials for the contact lens, which will be provided by the Cal Poly Biomedical Engineering department.

# If Manufactured on a Commercial Basis

An estimated 3 million Americans have Glaucoma, but scientists say that only about half of these even know about it [2]. This means the market for Glaucoma patients contains somewhere between 1.5 and 3 million people in the United States alone. The projected sales for the Active Contact Lens show at least 200,000 devices sold per year. The expected manufacturing cost per device is $1,000, and the projected purchase price is $2,000. The user should not have to pay any money to operate the device. The annual profits with these sales prices will be $200 Million, as shown in the equation below.

$$Annual\ Profits = (Purchase\ Price - Manufacturing\ Price) * Annual\ Sales$$
$$P = (\$2000 - \$1000) * 200{,}000 = \$200M$$

# Environmental Impacts

The fabrication process for this device produces waste, with the silicon wafers and substrate material used to form the contact lens. The fabrication process can recycle some of the waste, such as the leftover silicon wafer, for future use. The excess contact lens substrate material must go to a landfill, because once the material cures, it cannot be cured again without changing the material properties. The fabrication process produces approximately 1 oz. of substrate material for every 10 contact lenses.

This project uses some natural minerals associated with building electronics, such as silicon, tin, and tungsten. The small size of each device minimizes the use of these minerals, but the projected sales of 200,000 units per year over several years will wear on the Earth's supply of these conflict minerals. Power plants also supply power for the manufacturing processes. Your typical coal-burning power plant with emissions controls generates 3.5 million tons of $CO_2$, 7,000 tons of $SO_2$, 3,300 tons of $NO_x$, 114 lbs. of lead, 4 lbs. of cadmium, 720 tons of Carbon Monoxide, 225 lbs. of arsenic, and 220 lbs. of hydrocarbons per year, among other toxic substances. Depending on where the manufacturing processes are located, the power plants supporting them emit these toxic substances into either the air or a body of water, whether a river, lake, or an ocean near the power plant.

Through this pollution, the Active Contact Lens product indirectly contributes to the decline of the Earth's ozone layer, mercury pollution in oceanic wildlife, and even the death of thousands of humans per year. This pollution directly impacts other species around the globe. The manufacturing emissions harm aquatic species through mercury pollution, which was a big deal in China and Japan several years ago, causing physical deformities and shorter lifespans in the affected animals, some of which are internationally protected species, such as sea turtles.

## Manufacturability

One of the big challenges of the manufacturing process is the curing process, which involves putting the contact lens circuitry inside the contact lens before the lens itself solidifies. The circuitry has to be completely encased in the substrate, which poses a bit of a challenge with standard manufacturing equipment.

The current solution for this problem involves screen printing micro fabricated circuitry onto one half of the cured substrate, and then curing more of the substrate on top of the circuitry. Because the circuitry printing temperatures are higher than the curing process's baking temperature, doing this doesn't damage the circuitry.

## Sustainability

The design of the Active Contact Lens does not support sustainability of the product. Once the device is manufactured, we cannot change its structure, which poses a challenge for maintaining the device. The only possible maintenance for the device involves improving the design for future models of the product. Every manufactured device that reaches End of Life currently must be thrown away, wasting precious resources.

The sustainability of this product would significantly improve with a circuit separable from the contact lens substrate. A separable circuit and substrate can be recycled individually, reusing the conflict minerals for new electronics. The challenge with this idea is the "how". Since the circuit is embedded in the substrate, we have to create some method of either pulling the circuit out of the lens, or melting the lens substrate off without damaging the circuitry.

Creating a biodegradable substrate would also improve the device's sustainability. However, the nature of the project, researching ways to use a donated material, does not allow us to experiment with different substrate materials.

## Ethical Impacts

According to the utilitarian ethical framework, the Active Contact Lens project may be called "ethically sound". The project provides jobs for mechanical, electrical, and biomedical engineers, as well as expanding the scope of jobs ophthalmologists can perform. Project developers also predict the early detection of Glaucoma in thousands of people annually in the US alone. In the long run, it will help millions of people treat Glaucoma much earlier than they could without it, preventing blindness in thousands of possible victims. The main people group this project may harm is the ophthalmologist community. While also increasing the scope of what their jobs may entail, the Active Contact Lens may also replace them. As the customers become more reliant on the contact lens, they may choose not to consult ophthalmologists, causing them to lose their jobs.

The Active Contact Lens project also follows the IEEE code of ethics. The project researchers base their research topics on studies previously performed, and products already in production, such as Sensimed's Triggerfish. They expand on current knowledge and technology, in accordance with IEEE codes 3, 5, 6, 7, and 10. The product may target certain demographics as its main customers, but anybody may use the Active Contact Lens with their doctor's approval (IEEE codes 2, 8). Researchers for this project also prioritize the customers' safety above all else, according to IEEE code 1.

## Impacts on Health and Safety

The main health concern associated with the Active Contact Lens is the safety of the user's eye. Several factors play into the patient's safety, including the chemical makeup of the contact lens substrate. If the substrate is not bio-friendly, it could cause serious long-term damage to the user's eye.
Another safety concern is the containment of the circuitry inside the contact lens. The lens must completely encase the circuitry, or electric current will flow through the user's eye, possibly damaging the optical nerves.

The positive health impacts the Active Contact Lens have on society far outweigh the negative. This project has the potential to save millions of people from blindness around the world, and to prevent the slow decline of millions of others' eyesight. Not only does this improve the health of those it affects directly, it also indirectly increases the safety of those around them. Glaucoma normally degrades one's eyesight, affecting their day-to-day activities, such as driving vehicles. With the Active Contact Lens, people can treat Glaucoma before it causes serious damage to their optic nerve, allowing them to function normally while going about their day. For activities like driving, which potentially puts the lives of others at risk, the ability to function normally could prevent fatal accidents from occurring

## Social and Political Impacts

One political issue that may come with the mass production of the Active Contact Lens is the pressure that comes with every new drug doctors tell patients about. Some of these drugs are shown, after extensive studies, to actually not do anything for the human body (they are placebos). The Active Contact Lens may inspire debate such as this, with studies arguing cases both for and against the effectiveness of the product.

The Active Contact Lens can impact society in a huge way when people hear about it, saving millions of people from going blind, drastically improving the social aspect of their lives. Those with Glaucoma and others that use the Active Contact Lens are the direct stakeholders in the project, as its development impacts them more than anybody else. This product drastically improves their quality of life, prolonging Glaucoma's development and allowing them to enjoy good eyesight for decades longer than without the contact lens. More of this product's direct stakeholders include me and the other engineers working on the project; we put hundreds of hours of time into developing the project, as well as hundreds of dollars to buy the materials needed in the development process.

The device also indirectly affects competing products, such as Sensimed's Triggerfish. With the Active Contact Lens acquiring CE and FDA approval for sales in both Europe and the US, it takes away possible customers for the Triggerfish. Other systems indirectly affected by this product include the ophthalmologists specializing in diagnosing Glaucoma, as they stand to lose their jobs with the product's development.

The final product will help the patients, improving their quality of life. It may have negative effects on some of the indirect stakeholders, however, as it will steal customers from competing devices, like the Sensimed Triggerfish mentioned above. It also may cause doctors that specialize in Glaucoma to lose their jobs, as the Active Contact Lens can diagnose the patient, relieving them from needing a doctor's expertise.

## Development

I will learn about micro fabrication processes for the development of the Active Contact Lens. I will have to learn how to use various fabrication tools and machinery associated with the manufacturing process. There will be equipment used for two main fabrication processes: developing the contact lens substrate and fabricating the circuitry that the contact lens encases.

I have already learned how to perform a Monte Carlo Analysis for design specifications. This analysis technique is extremely helpful in simulating realistic circuits and accounting for losses that are not normally thought of.

I also performed a literature search in researching Glaucoma, its effects, and the treatments currently in existence. In researching the disease and the total available market for the Active Contact Lens, I found that only one medical device in existence attempts to track the user's IOP long-term: Sensimed's Triggerfish contact lens system, and the Triggerfish does not have FDA approval for marketing and sales within the US, creating a totally open market for the Active Contact Lens in the US. I also found that theoretically, long-term tracking of one's IOP should provide much more accurate data about one's IOP than the instantaneous measurements current tonometry practices provide.

# *Appendix B: Project Planning*

## Cost Estimate

The projected cost for the project as a whole is shown in **Table 3**. The table lays out where the projected expenditures come from, breaking them up into parts and labor cost.

The table also predicts optimistic and pessimistic values for the money spent on each aspect. These values help produce a more realistic cost projection using the PERT method, taking into account possible variations in expenditures.

**Table 3: Project Cost Estimate**

| **Cost Estimate** | | Most Optimistic | Most Likely | Most Pessimistic | Cost / unit | Most Optimistic Cost (a) | Estimated Cost (m) | Most Pessimistic Cost (b) |
|---|---|---|---|---|---|---|---|---|
| Parts | Silicon Substrate Material | N/A | N/A | N/A | N/A | $0.00 | $0.00 | $0.00 |
| | Test VCO Chip | 1 | 1 | 2 | $5 | $5.00 | $5.00 | $10.00 |
| | Set of Discrete Circuit Components for Testing | 1 | 2 | 4 | $5 | $5.00 | $10.00 | $20.00 |
| | Designed IC | 1 | 1 | 2 | $400 | $400.00 | $400.00 | $800.00 |
| Labor | Work Time (hours) | 150 | 178 | 210 | $20.00 | $3,000.00 | $3,560.00 | $4,200.00 |
| Total | | | | | | $3,410.00 | $3,975.00 | $5,030.00 |
| Projected = (a + 4m +b)/6 | | | | | | | | $4,056.67 |