# ENERGY HARVESTING FROM EXERCISE MACHINES: DC-DC BUCK-BOOST CONVERTER (LT3791)

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# Acknowledgements

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# Abstract

Cal Poly's ongoing Energy Harvesting From Exercise Machines (EHFEM) project proposes sustainability and energy saving costs through modifying exercise machines generating DC power, providing a renewable energy resource through physical exercise. The EHFEM project contains multiple sub-projects involving modifying several different exercise machines. Each machine generates DC power and an inverter converts this power to AC. This AC power returns to the grid. This project addresses an issue involving a previously installed DC-DC converter not returning power properly. When generating DC power, the grid demands a specific AC voltage, but the generated power through the previous DC-DC converter and power inverter encountered several problems. One previous converter outputted the desired DC output, but at the cost of low efficiency (<80%) [1]. Another converter had high efficiency, but could not accept a wide input range [2]. This project uses a LT3791 buck-boost DC-DC converter controller, which converts the generated power to a suitable DC voltage with high power efficiency. This project also improves system functionality while not affecting the users' exercise experiences.

# Chapter 1: Introduction

The Energy Harvesting From Exercise Machines (EHFEM) project provides an alternative renewable energy resource by converting physical exercise into electricity. The current trend around the world involves finding a renewable resource which can sustain people's lives and preserve the environment and scarce resources. This proposed renewable energy saves utility costs and gains monetary benefits since the self-generating electricity can pay itself off within a long-term period, specifically after a ten year operation [3]. This renewable energy also reduces and sustains scarce resource consumption since the project harvests energy from physical exercise, an otherwise wasted by-product.

The EHFEM project contains several modified exercise machines generating DC and AC power. Examples include a bicycle, a treadmill, and an elliptical machine. The generator side receives power through physical exercise, and outputs DC voltages between 5V and 45V [2]. This variation occurs because different users exercise at different rates, and also because the elliptical trainer's resistance levels affect the output voltage [4]. This project involves the elliptical machine, which has undergone several revisions through constant improvements and upgrades [1, 2]. Particularly, the elliptical machine, donated by Precor, needs an improved DC-DC converter because the previous converter could not return power to the grid. DC-DC converters provide a stable DC voltage from another DC voltage, where the stable DC voltage undergoes either a step-down or step-up system [5, 6]. This project's DC-DC converter uses a LT3791 IC chip, which works as a LED driver and contains current monitoring. This monitoring utilizes feedback, which controls the converter's switches whenever current exceeds or falls below a determined value. The IC must withstand a bus voltage equivalent to the converter's input voltages. The project's converter can receive nominal input voltages between 5V and 60V

(generated from the generator), while the converter can output nominal voltages between 0V and 60V [7]. Thus, the IC must withstand the generator's input voltages between 5V and 65V, where the 65V signifies the maximum input voltage. This converter attaches to a power inverter, donated by Enphase, which converts DC power to AC power. This inverter accepts a maximum 54V DC, so the converter and inverter must operate compatibly for optimal performance. This project involves the inverter receiving at most 36 ± 2V DC and outputting 240Vrms, an AC voltage compliant to the grid [8].

Fulfilling this project involves satisfying the customers, which include the Cal Poly Recreation Center members, the companies Precor and Enphase, and the Cal Poly students and faculty. Designating the design and project requirements can satisfy the customer needs.

### 1.1 Customer Needs - Design Requirements

Design requirements explain the project's overall main goals while under certain constraints. The design requirements for installing the DC-DC converter include the following:

- Safe for end-users, per the IEEE, PG&E and NEC standards and codes
- Exercise experiences remain the same before and after installing the converter
- No long-term costs to Cal Poly Recreation Center; the machine saves utility costs and pays back the Recreation Center
- The generator portion in the elliptical machine and the converter operate compatibly
- The inverter portion and the converter operate compatibly
- Raises awareness about sustainability and energy saving techniques by using environment-friendly components
- Endures long-term usage with low maintenance required

### 1.2 Customer Needs Project Requirements

Project requirements explain the product's functionality and limits. The project requirements for the DC-DC converter include the following [7, 8]:

- Output voltage undergoes step-down (buck) and step-up (boost) functions
- 5V-60V nominal DC input from the elliptical trainer
- 60V absolute maximum DC input from the elliptical trainer
- 5A absolute maximum input current (DC)
- 8A absolute maximum output current (DC)
- 38V maximum output voltage (DC)
- 200W absolute maximum output power
- Operating temperature junction: –40°C to 125°C

Determining the 200W occurs from that the Enphase inverter can only handle an output current of 830mA and output voltage of 240V. Thus, for high efficiency at 200W, the DC-DC converter must output 36V and about 5A.

These requirements outline the whole project, and Chapter 2 expands on how to implement these requirements into the project effectively.

# Chapter 2: Requirements and Specifications

TABLE I

THE BUCK-BOOST DC-DC CONVERTER REQUIREMENTS AND SPECIFICATIONS

| Marketing Requirements | Engineering Specifications | Justification |
|---|---|---|
| 1, 2, 3, 4, 6 | The converter does not obstruct the machine's other electronics or intrude on the users' exercises. | An ideal, non-intrusive device ensures users' experiences remain the same before and after the converter installation (i.e., the converter should not decrease or increase the machine's resistances). |
| 6, 7 | Long-term benefits outweigh cost implementation; the overall implementation costs should not exceed $360. | Generated power (renewable resource benefit) outweighs the installation time and costs, which estimates around $360 [3]. |
| 3, 6 | The converter does not disrupt or hinder the Enphase Inverter when generating power. | The Enphase Inverter (the elliptical machine has this inverter installed through previous senior projects) enables power conversion, allowing AC power through the grid [8]. This process must remain unaffected, so the converter and Enphase Inverter must operate compatibly. |
| 5, 6 | The converter must produce a voltage at most $36 \pm 2$V. | The machine's previously installed DC-DC converter produced the voltage range between 5V and 60V, while the inverter only accepts a range between 15V and 54V [1]. Also, Yuen's group determined that the inverter performs best with a 36V input [4]. |
| 1, 3, 8 | A previously made input voltage protection device must handle the voltages above 65V, thus ensuring the converter remains operational. | The converter and the machine's other devices could develop problems above 65V (occurs when users apply enough physical effort on the machine, thus generating high voltages) since previous projects have tested below 65V [1]. |
| 1, 6, 8 | The converter and Enphase inverter must never exceed their maximum voltage, current, or power ratings. | The devices must operate between their minimum and maximum ratings, following safety standards and having optimal performances [7, 8]. |
| 1, 6, 8 | The electrical connectors must withstand the maximum voltage, current, and power ratings determined by the converter and inverter. | Since the machine undergoes high voltages, currents, and powers, the electrical connectors and wires should also withstand the maximum ratings to ensure absolute safety for end-users. |
| 5 | Output voltage ripple (OVR) remains < 1% | OVR must remain small so output voltage resembles a DC voltage and not an AC voltage [12]. |
| **Marketing Requirements**<br>1. Users remain safe when riding the elliptical machine (i.e., satisfies PG&E safety requirements, IEEE 1547 specifications, etc. [1]). | | |

2. Users' exercise experiences remain unaffected when using the modified elliptical machine.
3. The converter and machine's other devices operate compatibly.
4. The converter fits the machine's confines, specified through Precor's equipment dimensions [11].
5. The converter converts a voltage range the grid accepts.
6. Low maintenance required.
7. Low overall cost.
8. The machine's devices and the converter must operate within maximum ratings.

The requirements and specifications table format derives from [9], Chapter 3.

Table I describes this project's specifications and requirements, where the most concern involves the users' safety and exercise experiences. Safety concerns include the high voltage levels not affecting the users or their exercise experiences and operating away from any potential hazards (i.e., water bottles, loose cords, etc.). Putting the electronics within the machine's confines should allow these potential hazards deemed avoidable. Another safety concern includes the generator, converter, inverter, and grid operating compatibly, thus avoiding potentially hurting the user. These devices' maximum ratings, high power electrical connectors, and protection circuits help determine the safest design.

Other concerns include low maintenance and low overall costs, since this project should pay itself off when generating electricity to save utility costs. Following Braun's project proposal establishes the overall low costs, where the goal costs fall below $360 [3]. Assuming 10 years of operation, the machine pays itself off after ten years during typical gym usage (12 hours per day, 41 weeks per year). Obtaining low maintenance involves determining the cheapest but most durable and reliable resources available, thus the machine can pay itself off after ten years without replacing the components too frequently.

TABLE II
DELIVERABLE DATES AND DESCRIPTIONS

| Delivery Date | Deliverable Description |
|---|---|
| Feb. 20, 2014 | EE Department-Wide Design Review |
| March 14, 2014 | EE463 Report |
| March 14, 2014 | EE463 Demo Device |
| June 4, 2014 | EE464 Report |
| June 4, 2014 | EE464 Demo Device |
| June 5, 2014 | ABET Senior Project Analysis |
| June 5, 2014 | Senior Project Expo |



Table II describes the project's dates and deliverables throughout the year, though the dates remain tentative. The proposed dates follow California Polytechnic State University's calendar dates. By fulfilling these deliverables, the Cal Poly EE students have fulfilled their Senior Project Design courses and projects.

The Design Review involves presenting design ideas and the design progress to fellow classmates and professors, where we receive comments and suggestions about our designs. The Design Review also gives students practice with speaking with groups of people so that the students have an idea on what to present for the Senior Project Expo.

The Design Review gave me an opportunity to improve on explaining the key features of the DC-DC converter that remained confusing to my fellow classmates. For example, I did not explain thoroughly how the whole LT3791 chip operated and only concentrated on the DC-DC converter components. When I presented an example circuit design of the LT3791, many members of the audience had trouble focusing on the DC-DC converter since other components (snubber circuit, sensor resistors, and other miscellaneous components) appeared along with the converter. Thus, for my Senior Project Expo, I need to focus the audience's attention on the converter without distracting them with the miscellaneous components too much. Chapter 3 can help better understand the main components of the project.

# Chapter 3: System Overview

## 3.1 Introduction

This chapter summarizes the interfaces that connect with the Buck-Boost DC-DC converter. Understanding the overall system can give better insight into developing an efficient and stable converter. For best insight, one must know where the input comes from and where output goes. The voltage input of the converter comes from the self-generating Precor Elliptical Machine that has been modified by previous EE graduates [4]. The converter's DC power output goes through an inverter, provided by Enphase, that converts the DC power to a 240VAC source. The inverter then returns this AC power back to the grid.

## 3.2 Exercise Machine Generator - Precor Elliptical Machine

The input to the converter comes from the self-generating Precor elliptical machine. This machine contains 20 resistance levels, which corresponds with an incline modifier (13° to 40°) [11]. Before previous Cal Poly students modified the elliptical, the machine normally dissipated power through a 10Ω resistor which becomes wasted heat.

After modifying the elliptical, previous students Martin Kou, Zack Weiler, and Ryan Turner have tested the self-generating power to determine what the machine can generate [1, 13]. The results from the previous students' tests measured the average voltage, average current, resistance level, and exercise rates (or strides per minute, SPM). From Kou's results, the elliptical could output a maximum average voltage of 42.84V set at the highest resistance level 20 and at 100 SPM, and could output a maximum average current of 4.09A set at resistance level 16 and at 125 SPM [1]. From Weiler's and Turner's results, the elliptical set at the highest resistance level 20 and at a sprint (230 to 300 SPM) could output a maximum average voltage of 64.591V and a

maximum average current of 6.4591A [13]. Weiler and Turner also showed that the elliptical can output a peak voltage of 150.251V and peak current of 15.025A at resistance level 16 and at a sprint. Since this project focuses on the DC-DC converter and not an input protection system, this project uses the average values as the max values needed for input voltage and current. In any case, previous and current students [14] focus on the input protection system needed for this system to avoid the peak values entering the system and damaging any electrical components. Also, since most exercise users spend their time exercising on the elliptical machines without sprinting or setting the resistance level at 20, the specifications for this project aims for lower average values. Thus, the specifications for this project focuses on a maximum input voltage of 60V and maximum input current of 5A.

### 3.3 Enphase Micro-Inverter M175

The output of the converter goes through the Enphase Micro-Inverter, which converts the DC voltage into an AC voltage. This inverter follows the limits for a Class B digital device under Part 15 of the FCC Rules, follows the installation code of ANSI/NFPA 70 under the National Electrical Code, and complies with the UL1741 and IEEE1547. The inverter contains a maximum peak power tracker (MPPT) to ensure that maximum power exports to the grid. The inverter also has a 5 minute wait time, can tolerate a maximum input voltage of 54V and maximum current of 8A, and can output a nominal AC voltage range between $211V_{rms}$ and $264V_{rms}$, or extended AC output voltage range between $206V_{rms}$ and $269V_{rms}$ [8].

A previous group tested this inverter and determined that the inverter performs optimally with an input voltage of about 36V [4]. Thus, the converter should output about 36V and a max current of 5A to prevent damaging the inverter. Also, a maximum output power of about 200W

or more from the converter should suffice for high power efficiency since the inverter has a maximum output voltage of $269V_{rms}$ and output current of 830mA, or 223.27W.

### 3.4 LT3791 and LT3791-1

The LT3791 chip originally works for driving LEDs and not specifically for functioning as a voltage regulator, though the IC can possibly operate as a voltage regulator with some adjustments. Linear Technology provides another IC alternative specifically for regulating constant voltage; the LT3791-1 contains similar internal components like its counterpart LT3791, but the LT3791-1 regulates constant voltage instead of regulating current. While I use the LT3791, another group, Sheldon Chu and David Yoo, works with the LT3791-1 [14]. The LT3791 contains an OPENLED pin that senses whether an open occurs at the output. The LT3791-1, however, contains a CCM (continuous conduction mode) pin that allows the converter to operate in CCM or DCM (discontinuous conduction mode) and a C/10 pin for charging purposes. Besides these differences, the two ICs have similar internal circuitry. Thus, comparing the two ICs, the LT3791-1 may appear optimal for this project since we require a constant voltage of 36V. However, the DC-DC converter connects with the Enphase inverter, which originally operates for solar panels and contains a MPPT. The MPPT causes the inverter to obtain as much power as possible, which might mean obtaining as much current as possible from the DC-DC converter. If using the LT3791-1, the inverter may try to obtain higher current levels. The LT3791-1 may respond negatively by this endeavor since the IC wants to regulate a constant output voltage. The LT3791, however, can regulate constant current. The LT3791's internal circuitry could possibly operate correctly even with the MPPT. Since the internal circuitry of either ICs cannot not be fully known without breaking into the chips, we separate the

two ICs  into two groups (my project and Sheldon and David's project) in order to find out how each IC responds when operating with the Enphase inverter.

Chapter 4 further discusses on how the LT3791 should operate by discussing its functional decomposition.

# Chapter 4: Functional Decomposition

## 4.1 Introduction

This chapter introduces the functional decomposition design, or the breakdown of the overall design into its several main constituents. In order to understand and design the Buck-Boost DC-DC converter and the LT3791 controller, circuit designers must analyze the main constituents that make up the converter and controller. For this project, there includes the Level 0 design and the Level 1 design. The Level 0 design focuses on the overall project's main inputs and outputs. The Level 1 design focuses on how to accomplish the outputs by manipulating the inputs (i.e. A-D conversion, D-D conversion, etc.). Any additional level designs (Level 2, Level 3, etc.) describe even more details into manipulating the inputs to produce the outputs.

## 4.2 Level 0 Design

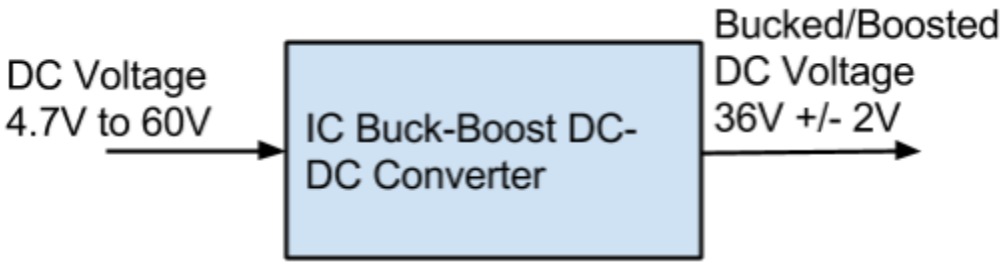


FIGURE 1
LEVEL 0 DC-DC CONVERTER

FUNCTION TABLE III
LEVEL 0 DESIGN DESCRIPTIONS

| | |
|---|---|
| Module | Buck-Boost DC-DC Converter |
| Inputs | DC Voltage: 5V-60V, the minimum and maximum voltage inputs |
| Outputs | Bucked/Boosted DC Voltage: 36 ± 2V |
| Functionality | Step-down or step-up the input DC voltage and obtain a desirable output DC voltage level. |

Figure 1 describes the input DC voltage going through the DC-DC converter and outputting the desired DC voltage. Table III summarizes the Level 0 design. The expected input values and output values correspond with the given specifications. The output contains the bucked or boosted output voltages. The preferred input range reside between 10V to 55V because previous groups found that efficiency remains consistently high for these inputs [1, 2, 13], but a 5V input and 60V input would suffice since exercise users can generate these input voltages when using the Precor's lowest (0) or highest (20) resistance level settings.

### 4.3 Level 1 Design

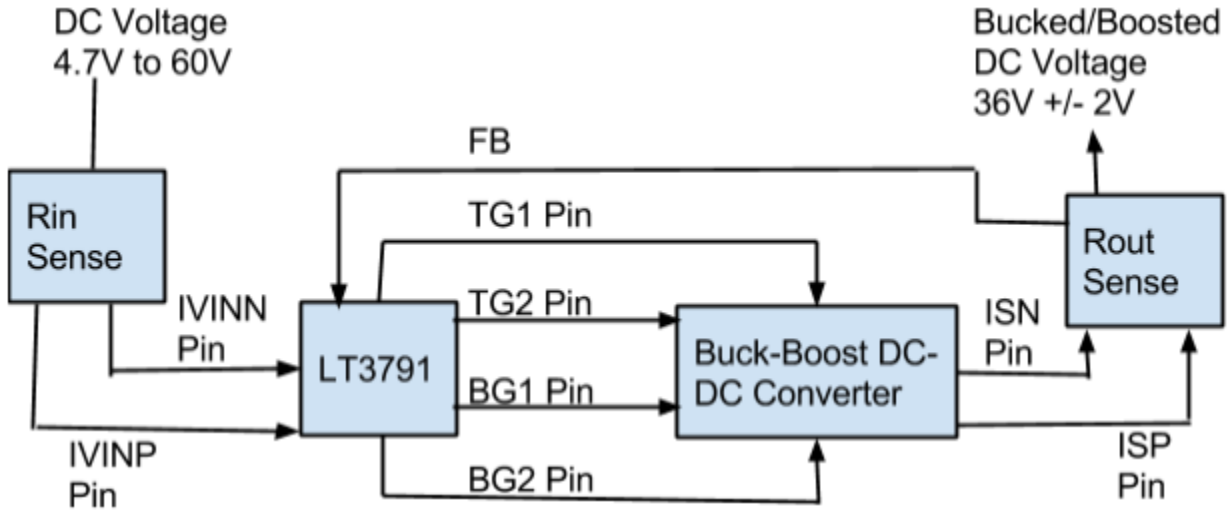


FIGURE 2
LEVEL 1 DC-DC CONVERTER

FUNCTION TABLE IV

LEVEL 1 DESIGN DESCRIPTIONS

| | |
|---|---|
| Module | Buck-Boost DC-DC Converter |
| Inputs | Vin DC Voltage: 5V-60V, the minimum and maximum voltage inputs |
| Interconnects | TG1: 4V-64V, controls whether the power MOSFET, M1, turns on or off<br>TG2: 4V-64V, controls whether the power MOSFET, M3, turns on or off<br>BG1: 0V to 5V, controls whether the power MOSFET, M2, turns on or off<br>BG2: 0V to 5V, controls whether the power MOSFET, M4, turns on or off<br>IVINN: negative input for input current limit and monitor<br>IVINP: positive input for input current limit and monitor<br>ISN: negative input for output current feedback resistor<br>ISP: positive input for output current feedback resistor<br>FB: feedback pin, indicates whether there is an open or short occurring |
| Outputs | Bucked/Boosted DC Voltage: 36V +/- 2V |
| Functionality | The gate voltages (TG1, TG2, BG1, BG2) control the switches (power MOSFETS). The switches determine how the converter behaves (buck, boost, buck-boost) based on whether which switches turn off or on and what order they turn off or on . |

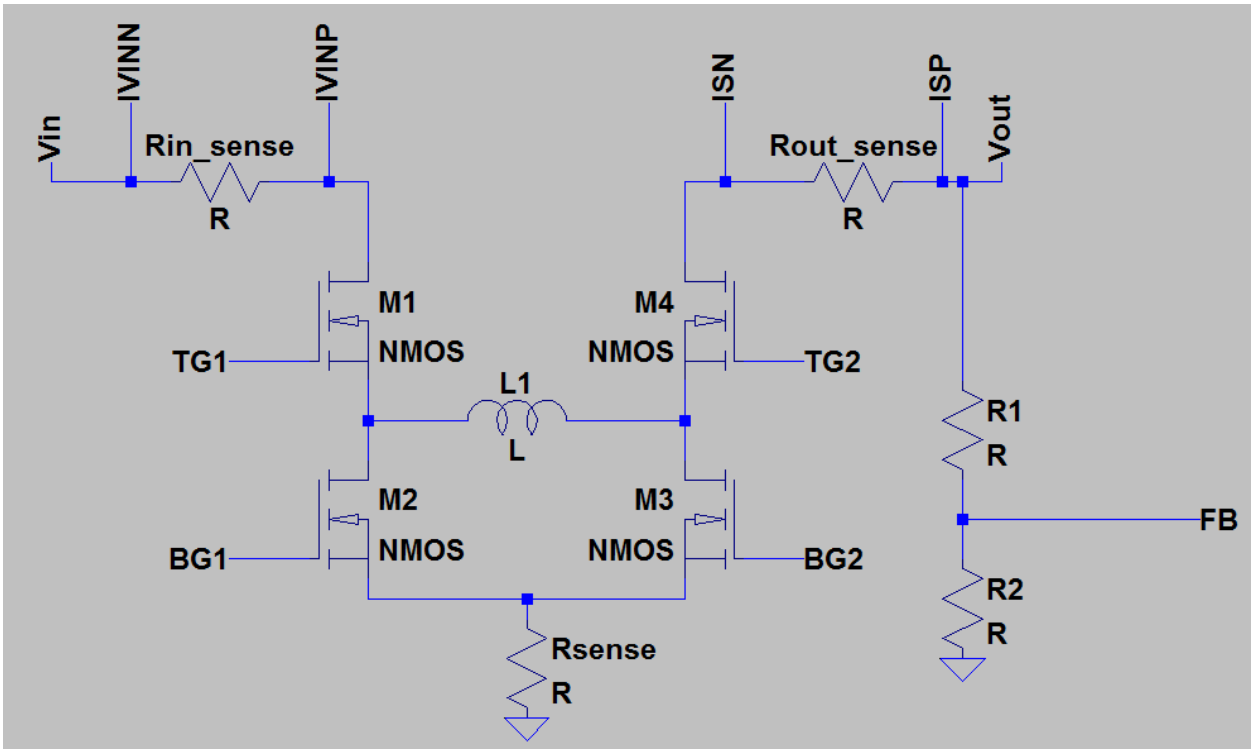


FIGURE 3

DC-DC CONVERTER SCHEMATIC

Figure 2 shows the DC-DC converter's Level 1 design. Table IV further elaborates the Level 1 design, and Figure 3 shows the schematic of the project's DC-DC converter. The gate voltages TG1 (Top Gate 1), TG2 (Top Gate 2), BG1 (Bottom Gate 1), and BG2 (Bottom Gate 2), control the power N-MOSFETS, meaning the gate voltages either turn on or off the N-MOSFETS like switches. Thus, how long the switches turn off or on and what order the switches turn off or on creates either a buck, boost, or buck-boost effect, since the inductor L either absorbs (buck) or releases (boost) energy (Appendix B - DC-DC Converter Design Examples). The LT3791 controller provides the gate voltages for these four gates [7]. Finally, the resistor Rsense determines the maximum output current for buck and boost operation.

The IC chip operates under two operation modes, similar to Yoshida's DC-DC converter patent which explains and expands upon the feedback application utilized through DC-DC converters [15]. This chip may operate in constant current or constant voltage mode. Constant current mode occurs when the voltage between the pins IVINP and IVINN exceeds 50mV. During this mode, the chip regulates constant current and provides this current through the output. Constant voltage mode occurs when the feedback pin FB senses a voltage above 1.2V, which causes the output current level to reduce and regulate the output voltage level.

The ISN and ISP pins, along with the FB pin, can indicate whether the output senses an open circuit. When the voltage between the ISN and ISP pins drops below 10mV and when the FB pin also exceeds 1.15V, the LT3791 tries to stop the TG1 and TG2 MOSFETs from switching and allow the inductor to discharge through the BG1 and BG2 MOSFETs. For a short circuit event, the FB pin must drop below 400mV, during which the LT3791 tries to also discharge the inductor. For further understanding of the whole IC, Chapter 5 discusses each component of the LT3791.

# Chapter 5: System Component Characterization

## 5.1 Introduction

This chapter introduces the characterization of the system components needed to create the Buck-Boost DC-DC converter with the LT3791. The general selections section describes the resistors, capacitors, diodes, and pins for the LT3791. The inductor section discusses the inductor core types, inductance values, and maximum current saturation values. The MOSFET section describes the $R_{DSon}$ values, maximum power dissipations, and maximum $V_{DS}$.

## 5.2 General Selections

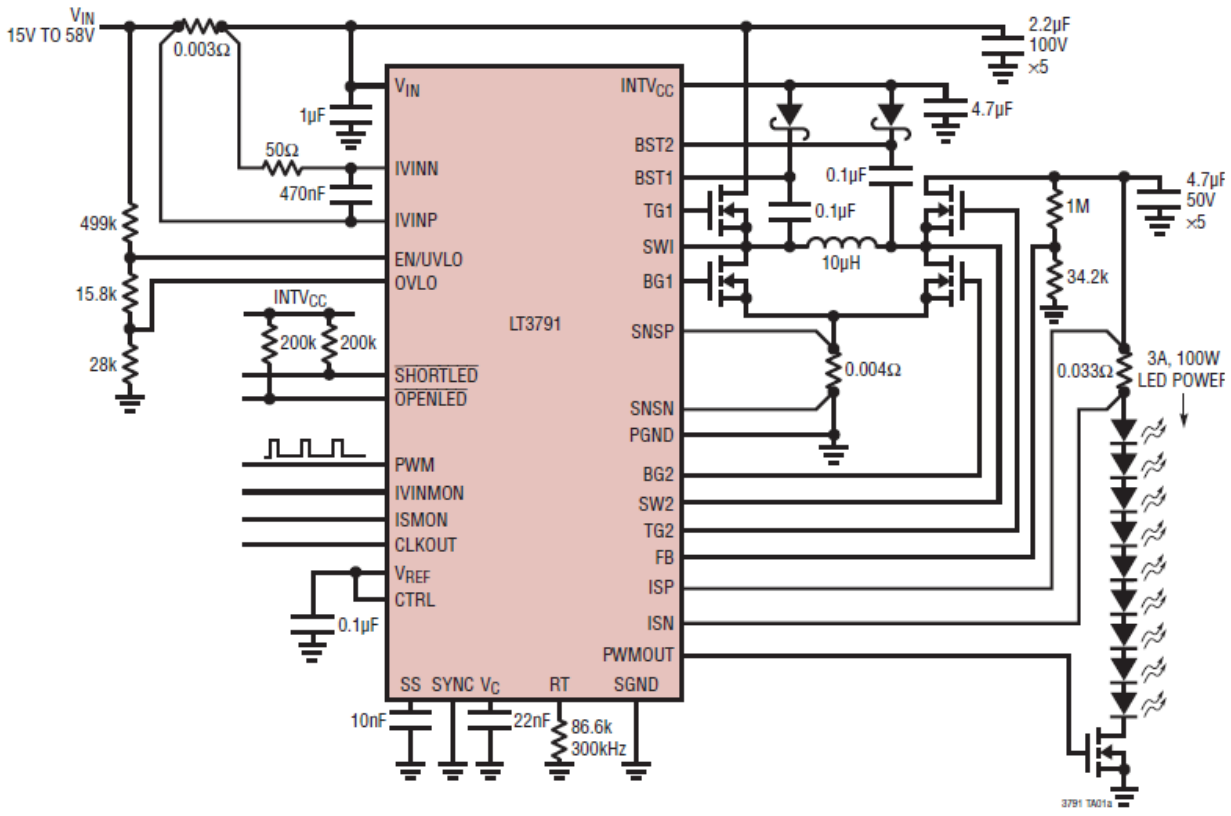


FIGURE 4
EXAMPLE LT3791 DESIGN, FOR A 33.3V AND 3A OUTPUT [7]

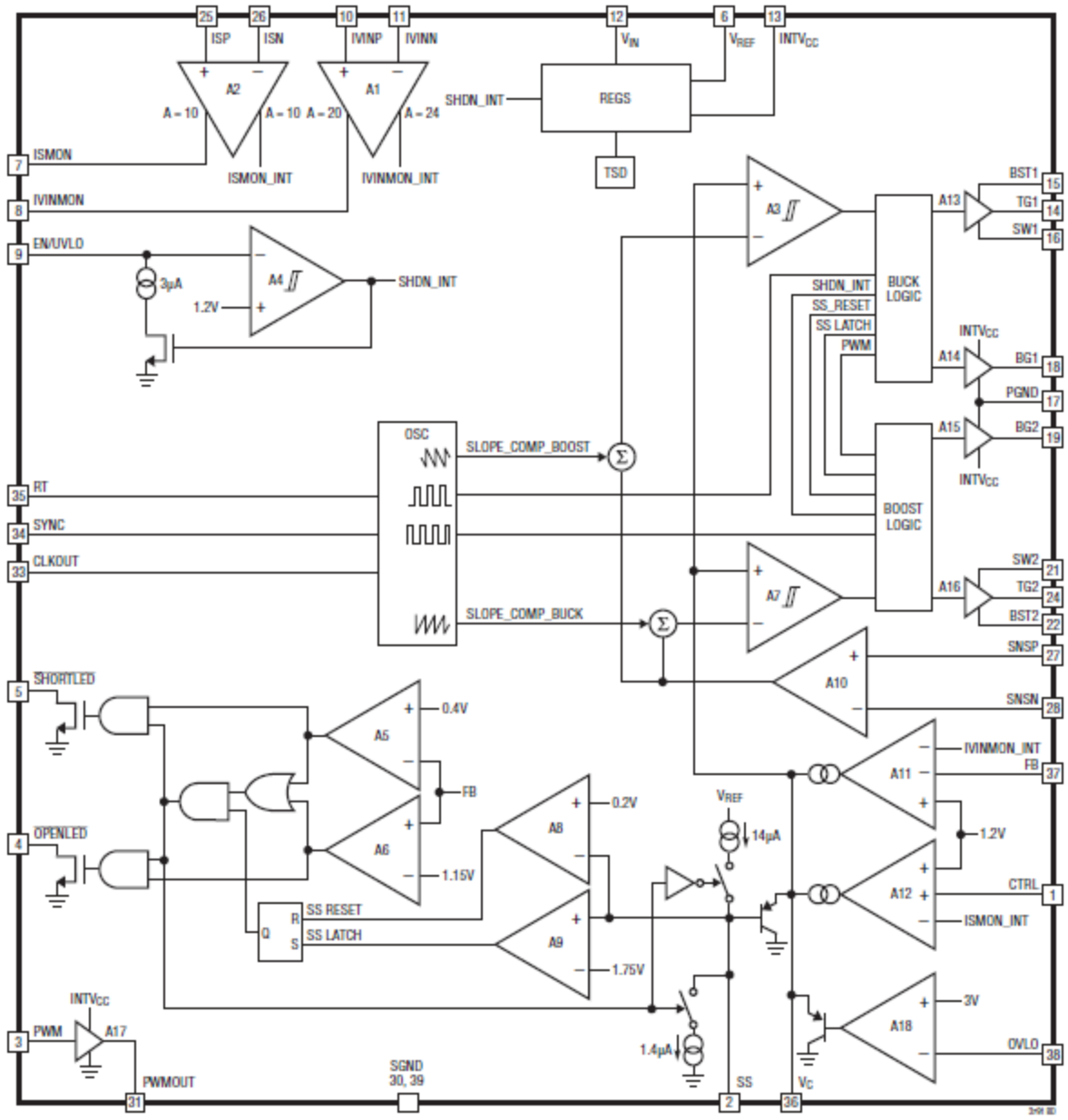


FIGURE 5
INTERNAL SCHEMATIC OF LT3791 [7]

Figure 4 shows an example of how to design the LT3791 and Figure 5 shows the internal components of the IC. Besides the DC-DC converter region, the LT3791 contains several components that need some clarification. The LT3791 contains 38 pins, two of which do not appear in Figure 4 because one of the pins remains a non-connection pin and the other pin

remains a test pin [7]. Also for this project, pins PWM and PWMOUT do not concern us because these pins act as a dimming control operation for LEDs, which this project doesn't focus on. Thus, these pins would either remain open or grounded.

### 5.2.1 Input Connections

To indicate the input voltage range thresholds, users can use the pins EN/UVLO and OVLO. The EN/UVLO pin indicates the lowest operational input voltage and the OVLO pin indicates the highest operational input voltage. To indicate the input voltage limits, users can use voltage dividers to apply the voltage limit in the pins. The LT3791 datasheet includes equations to help determine the input voltage thresholds, and Figure 6 shows the voltage divider example:

$$V_{IN(UVLO^+)} = 1.2\frac{R1+R2}{R2} \quad (1)$$

$$V_{IN(UVLO^-)} = 3uA * R1 + 1.215\frac{R1+R2}{R2} \quad (2)$$

$$V_{IN(OVLO^+)} = 3\frac{R3+R4}{R4} \quad (3)$$

$$V_{IN(UVLO^-)} = 2.925\frac{R3+R4}{R4} \quad (4)$$

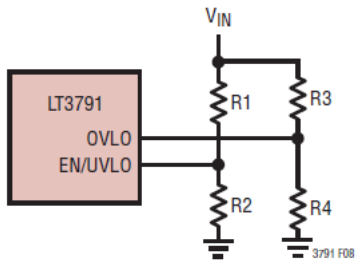


FIGURE 6
VOLTAGE DIVIDER TO SET $V_{IN}$ UVLO AND OVLO THRESHOLDS [7]

The IVINP and IVINN pins, as mentioned before, indicate the input current limit and can put the DC-DC converter into constant current mode. The pins connect to a small sense resistor

value, which can range from 2mΩ and 20mΩ. The input current follows the equation below and Table V shows the corresponding input current values:

$$I_{IN} = \frac{50mV}{R_{IN}} \quad (5)$$

TABLE V
$R_{IN}$ vs. $I_{Limit}$

| $R_{IN}$ (Ω) | $I_{Limit}$ (A) |
|---|---|
| 0.02 | 2.5 |
| 0.015 | 3.3 |
| 0.012 | 4.2 |
| 0.01 | 5 |
| 0.006 | 8.3 |
| 0.005 | 10 |
| 0.004 | 12.5 |
| 0.003 | 16.7 |
| 0.002 | 25 |

For loop stability, a low-pass RC filter must connect between the two pins. Normally, a 50Ω resistor and 470nF capacitor can suffice.

The $V_{IN}$ pin receives the input voltage and supplies power to the LT3791. The $V_{IN}$ pin internally connects to the voltage regulator, where this regulator supplies a reference voltage of 5V to pin $INTV_{CC}$ and 2V to pin $V_{REF}$. Users should bypass the $V_{IN}$ pin with a large enough capacitor $C_{IN}$ to filter the input square wave current during buck operation. The capacitor should ground to the power ground PGND. Users should use a low ESR capacitor to handle the maximum RMS current, where the RMS current equation appears below and obtains a maximum value at $V_{IN} = 2V_{OUT}$:

$$I_{RMS} = \sqrt{(I_{LED})^2 + (\frac{(I_L)^2}{12} D)} \quad (6)$$

### 5.2.2 Output Connections

Since the LT3791 originally operates as a LED driver and this project doesn't involves LEDs, the example LT3791 design from Figure 4 has some modifications. For example, the series of LEDs, the PWMOUT pin, and the MOSFET controlled by the PWMOUT pin do not appear in this project because the PWMOUT pin and MOSFET control dimming operations for the LEDs, which do not apply on this project. Also, the resistor connected between the ISP and ISN pins moves in series with the output voltage instead of residing in parallel with the output. An example of the modifications appear in Figure 7.

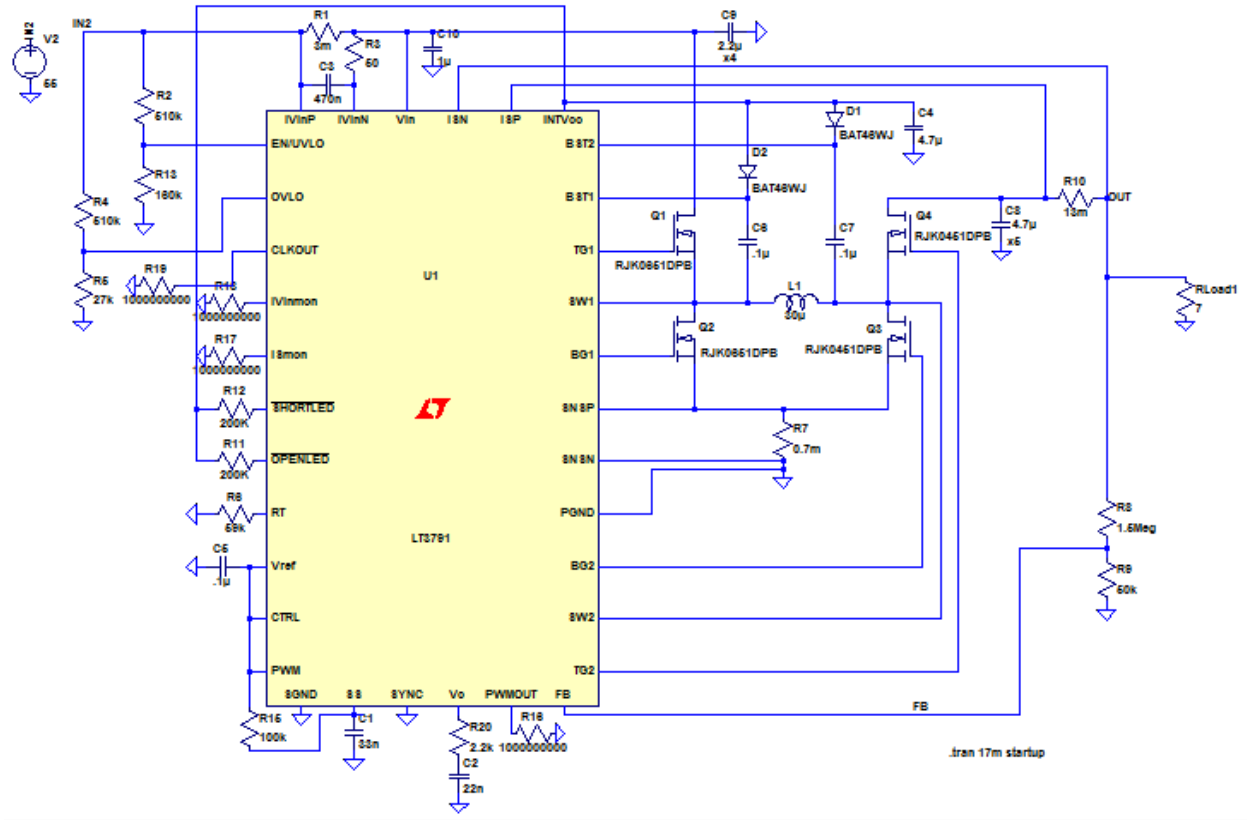


FIGURE 7
LT3791 MODIFICATIONS TO OUTPUT

In Figure 7, the PWMOUT pin connects to large resistor as opposed to another MOSFET for dimming control. The ISP and ISN pins still connect across a resistor to program output current. The ISP and ISN pins determine the output current limit by referencing a 100mV instead of 50mV like the input sense resistor.

The feedback (FB) pin remains the same, and senses whether the overvoltage limit occurs. A voltage divider determines the overvoltage limit by using the following equation:

$$V_{OUT(OVP)} = 1.25 * \frac{R5 + R6}{R6} \quad (7)$$

The rest of the output connections concern with the DC-DC converter, which appear in the next section.

### 5.2.3 DC-DC Converter Connections

Figure 4 shows the DC-DC converter with four MOSFET switches connected with the inductor. As discussed previously in section 4.3, the IC controls the four MOSFETs to create either a Buck, Boost, or Buck-Boost converter. The IC controls the MOSFETs by controlling the gates of the MOSFETs, as shown through the pins TG1, TG2, BG1, and BG2.

Below the four MOSFETs contains the $R_{SENSE}$ resistor, which determines the maximum output current. The pins SNSP and SNSN that connect across the $R_{SENSE}$ resistor set the current trip threshold.

Above the four MOSFETS contains the snubber circuit (the two capacitors and Schottky diodes). The snubber circuit allows the MOSFETs to experience less voltage peaks with the diodes preventing the peaks. Thus, the pins BST1 and BST2 swing from a diode voltage below $INTV_{CC}$ up to a diode voltage below $V_{IN}$ + $INTV_{CC}$. The $INTV_{CC}$ pin outputs 5V, which powers

the driver and control circuits of the IC. For steady DC voltage, we bypass $INTV_{CC}$ with a capacitor with a minimum value of 4.7uF.

The pins SW1 and SW2 control how the top MOSFETs, M1 and M4, since the voltage at the pins can swing from a diode voltage drop below ground up to $V_{IN}$ (SW1) or $V_{OUT}$ (SW2). The IC provides 5V, from the $INTV_{CC}$, to drive the gates of these top MOSFETs charged from the bootstrap capacitors. Whenever the top MOSFETs turn on, SW1 (SW2) rises to the input voltage and BST1 (BST2) rises to the input voltage plus the 5V ($INTV_{CC}$). When the bottom MOSFETs turn on, SW1 and SW2 drops low and the bootstrap capacitors charge from the $INTV_{CC}$ through the bootstrap diodes. These capacitors provide the gate voltage to turn the top MOSFETs on again. The Figure 5 shows the pins entering two op-amps connected to the buck and boost logic blocks, and the op-amps' outputs connect to the TG1 and TG2 pins. Thus, the SW1 and SW2 pins control the switching of the top MOSFETs. Also, the pins BST1 and BST2 connect to the two op-amps, so these four pins determine whether the top MOSFETs either turn off or on.

### 5.2.4 Miscellaneous Connections

The $R_T$ pin programs the switching frequency from 200kHz to 700kHz. A smaller frequency yields better efficiency and less switching losses but requires a larger inductor to handle ripple currents. A higher frequency requires a smaller inductor but yields more switching losses, more gate driving current, and may not allow very low or very high duty cycle operations. Table VI shows resistor values proportional to switching frequency.

TABLE VI
SWITCHING FREQUENCY VS. $R_T$ VALUES

| Switching Frequency (Hz) | $R_T$ (Ω) |
|---|---|
| 200000 | 147000 |
| 300000 | 84500 |
| 400000 | 59000 |
| 500000 | 45300 |
| 600000 | 37500 |
| 700000 | 29400 |

For the following pins discussed further on, we need to refer to another design besides what Figure 4 presents because Figure 4 shows the LT3791 as a LED driver controller instead of a DC-DC controller. Thus, some of the design choices in Figure 4 do not work for a DC-DC controller design (i.e. the $V_C$ pin needs a series resistor to increase the slew rate of the $V_C$ pin to regulate output current during fast transients on the input power supply). The LT3791-1 datasheet presents a DC-DC controller design to base on.

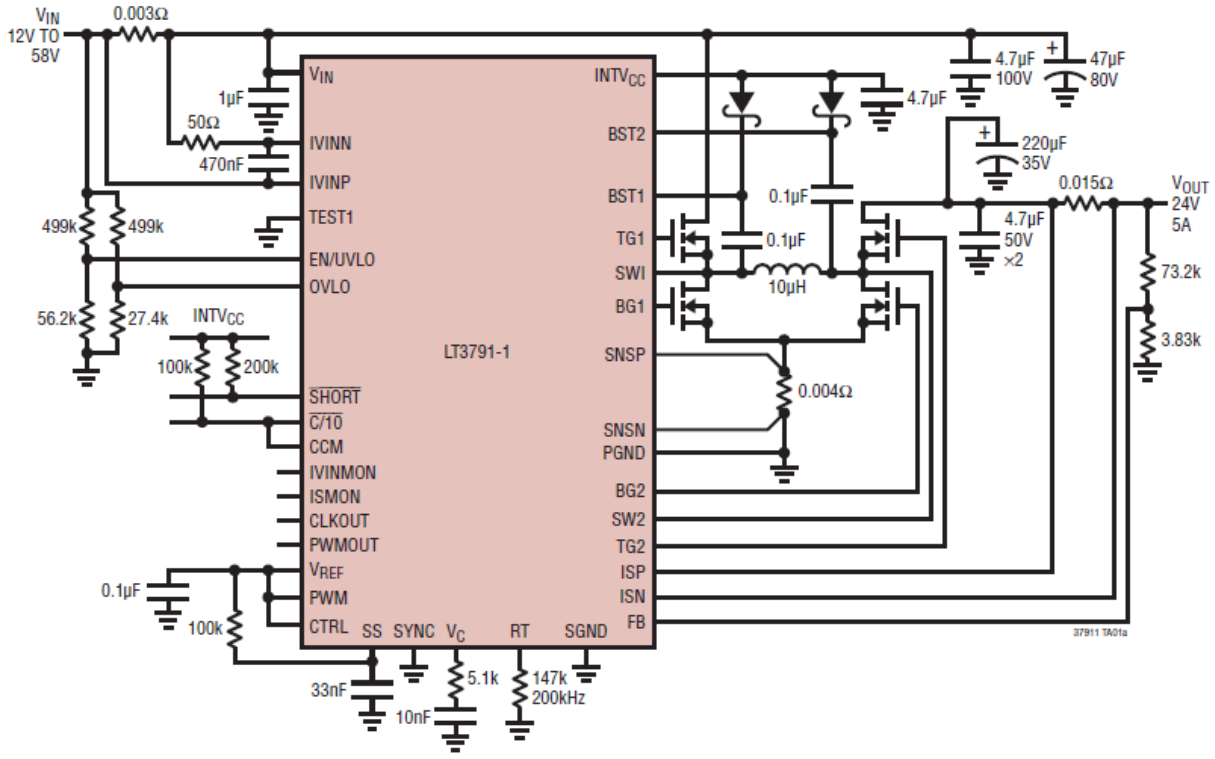


FIGURE 8
LT3791-1 DC-DC CONTROLLER EXAMPLE [16]

Figure 8 shows an example DC-DC controller design from the LT3791-1 datasheet. Again, we use the LT3791 instead of the LT3791-1 because the LT3791 may overcome power problems from the MPPT of the Enphase inverter. But, we need the LT3791-1's design in order to create the DC-DC controller instead of the LED driver controller. Also, Figure 8 shows a few pins not shown in Figure 4, such as the CCM, C/10, and TEST1 pins. Thus, we can ignore these pins in Figure 8 (in fact, pins CCM and C/10 functionally correspond to the OPENLED pin of the LT3791).

The $V_C$ pin compensates the control loop response and stability. For DC-DC controller operation, a series resistor and capacitor must connect to this pin to increase the slew rate.

Without the series resistor, the input power can swing from positive to negative values (or the current would come out or go into the input power source).

The SGND (signal ground) pin, similar to the PGND (power ground) pin, must connect to the ground plane. However, the SGND must connect with all the small-signal components and small-signal compensations at a single point with the PGND. The TEST1 pin must also connect with the SGND pin for proper operation.

The CLKOUT and SYNC pins help synchronize several of the LT3791 ICs together. The CLKOUT pin outputs an in-phase clock frequency provided by the internal oscillator frequency circuit. The SYNC pin synchronizes with the rising edge of the CLKOUT's output frequency. To parallel two ICs together, one of the CLKOUT pins of one IC must connect directly to the SYNC pin of the other IC.

The CTRL pin normally controls the analog dimming by programming the LED output current. For this project's application, however, we do not focus on any analog dimming. Thus, the CTRL pin must connect with a voltage higher than 1.2V in order to get the full-scale 100mV threshold across the sense resistor, which should give the output current. The CTRL pin must also connect with the $V_{REF}$ pin, which typically outputs 2V as reference for the CTRL pin.

The SS (soft-start) pin gradually increases the controller's current limit when turning on the IC. When a LED open or short condition occurs, the SS pin acts as a timer and restarts the IC (turns off the top MOSFETS and turns on the bottom MOSFETS to allow the inductor to discharge to 0). The timer needs a minimum value of 10nF for proper operation. To latch off this timer in the event of a fault, a 500k resistor must reside between the SS and $V_{REF}$ pins.

The OPENLED and SHORTLED pins senses whether an open or short occurs at the output. If either situation occurs, the IC restarts to avoid getting damaged. The OPENLED pin's event

occurs when it senses greater than 1.15V at the FB pin and less than 10mV between the ISP and ISN pins. The SHORTLED pin's event occurs when it senses less than 400mV at the FB pin. Both the OPENLED and SHORTLED pins require external pull-up resistors for proper operation.

### 5.3 Inductor Selections

We must consider several important factors for proper and safe operation when choosing an inductor. These factors include saturation current, inductor size, current rating, and low DC and AC resistances. The following equations help calculate the inductance values needed for certain frequencies:

$$L_{BUCK} > \frac{V_{OUT}\left(V_{IN(MAX)} - V_{OUT}\right) * 100}{f * I_{LED} * \%ripple * V_{IN(MAX)}} \quad (8)$$

$$L_{BOOST} > \frac{V_{IN(MIN)}^2\left(V_{OUT} - V_{IN(MIN)}\right) * 100}{f * I_{LED} * \%ripple * V_{OUT}^2} \quad (9)$$

TABLE VII
VALUES FROM SPECIFICATIONS

| $V_{OUT}$ (+/-2V) | $V_{IN(MIN)}$ (V) | $V_{IN(MAX)}$ (V) | $I_{OUT(MAX)}$ or $I_{LED}$ |
|---|---|---|---|
| 36 | 5 | 55 | 7 |

TABLE VIII
SWITCHING FREQUENCY VS. INDUCTANCE

| Frequency (Hz) | Inductance (uH) |
|---|---|
| Buck (200k) | 29.61 |
| Buck (400k) | 14.81 |
| Buck (600k) | 9.87 |
| Buck (700k) | 8.46 |
| Boost (200k) | 1.4238 |
| Boost (400k) | 0.7119 |
| Boost (600k) | 0.4746 |
| Boost (700k) | 0.4068 |

Table VII shows the values to input into the equations (8) and (9), based on the required specifications. Table VIII shows the differing inductance values based on switching frequency. For clarification, lower frequency correlates to lower switching losses but larger inductor sizes and values. Higher frequency, however, correlates to higher switching losses but smaller inductor sizes and values. Based on Table VII and equations (8) and (9), I chose a 10uH inductance at 600kHz because it's the smallest inductor to find easily (as opposed to 8.46uH or 1.4238uH).

Next, for best performance, chosen inductors must contain high current and saturation ratings to avoid damaging the inductor during boost mode. To determine the maximum ratings, we must determine how much current can possibly run through the inductor. We can consider the maximum current by analyzing the power efficiency of the DC-DC converter. For example, if we expect an output voltage of 36V running through a 10Ω load, we would expect 3.6A and 129.6W at the output. Thus, for an ideal 100% power efficiency, if the elliptical trainer provides 15V as

input voltage (boost mode), then the elliptical trainer must also provide an input of 129.6W or 8.64A.

The  IC can accept an input voltage as low as 5V, but for this project the input voltage limit falls between 10V and 55V. So, assuming a voltage input of 10V, a 10Ω load, and 36V and 3.6A output (129.6W), then an input of about 13A must enter the IC for 100% efficiency. Thus, a chosen inductor must have at least a maximum current and saturation rating over 13A for safe and optimal operation.

For low power consumption, the inductor needs low DC and AC resistances, such as 5mΩ. To meet all of these requirements, I chose the following inductor [17] shown in Table IX.

TABLE IX
INDUCTOR PART: 732-4235-1-ND [17]

| Properties | Test conditions | | Value | Unit | Tol. |
|---|---|---|---|---|---|
| **Inductance** | 100 kHz/ 10 mA | L | 10 | µH | ±20% |
| **Rated inductance** | 100 kHz/ 10 mA/ 21.0 A | $L_R$ | 7.8 | µH | typ. |
| **Rated current** | ΔT = 50 K | $I_R$ | 21.0 | A | max. |
| **Saturation current** | \|ΔL/L\| < 30% | $I_{sat}$ | 26.0 | A | typ. |
| **DC Resistance** | @ 20°C | $R_{DC}$ | 3.40 | mΩ | ±10% |
| **Self resonant frequency** | | $f_{res}$ | 15 | MHz | typ. |

This inductor fulfills the previous requirements specified before: 10uH with 20% tolerance, 21A maximum current rating, 26A maximum saturation rating, and 3.4mΩ DC resistance with 10% tolerance. The current and saturation ratings surpass the 13A limit calculated from before, and the 10uH was easily found compared to 8.46uH and 29.61uH. The low DC resistance allows low power dissipation, and 3.4mΩ appears as one of the lower values found throughout the Digikey inductor products (where most DC resistances go above 10mΩ). So, this inductor appears as ideal as possible for this project.

### 5.4 MOSFET Selections

An ideal power MOSFET has no on-resistances, has no power dissipation, can tolerate infinite $V_{DS}$ and $I_{DS}$, and switch on and off instantaneously. Unfortunately, no such MOSFET exists, so we must consider these limitations when choosing MOSFETs for the DC-DC converter.

For maximum $V_{DS}$ and $I_{DS}$ ratings at specific temperatures, the MOSFETs must withstand the worst case-scenarios. For example, without an input voltage or current protection system, the DC-DC converter could receive at most 150.251V and 15.025A from the elliptical trainer [13]. We must also consider the maximum average voltage of 64.591V and a maximum average current of 6.4591A from the elliptical trainer. Thus, the MOSFETs should withstand the average voltage and current and the maximum values, if possible. However, two groups worked on an input protection system [14] which should bring down the input voltage below 60V. So, the MOSFETs must at least withstand 60V, or have a $V_{DS}$ maximum rating of 60V or more.

For power dissipation considerations, the LT3791 datasheet provides equations to determine the maximum power dissipation through each MOSFET during either buck or boost mode. The following maximum power dissipation equations appear below from the LT3791 datasheet:

$$P_{M1(BOOST)} = \left( \frac{I_{LED} \bullet V_{OUT}}{V_{IN}} \right)^2 \bullet \rho_T \bullet R_{DS(ON)} \tag{10}$$

$$P_{M2(BUCK)} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{LED}^2 \bullet \rho_T \bullet R_{DS(ON)} \tag{11}$$

$$P_{M3(BOOST)} = \frac{(V_{OUT} - V_{IN}) \bullet V_{OUT}}{V_{IN}^2} \bullet I_{LED}^2 \bullet \rho_T \bullet R_{DS(ON)} + k \bullet V_{OUT}^3 \bullet \frac{I_{LED}}{V_{IN}} \bullet C_{ROSS} \bullet f \quad (12)$$

$$P_{M4(BOOST)} = \frac{V_{IN}}{V_{OUT}} \bullet \left( \frac{I_{LED} \bullet V_{OUT}}{V_{IN}} \right)^2 \bullet \rho_T \bullet R_{DS(ON)} \quad (13)$$

The k value in equation $P_{M3}$ accounts for the loss caused by the reverse-recovery current, and equals to 1.7. The $C_{ROSS}$ value comes from the MOSFET manufacturer's specifications. The $\rho_T$ comes from the normalization factor, which can vary depending on temperature as shown in Figure 9.

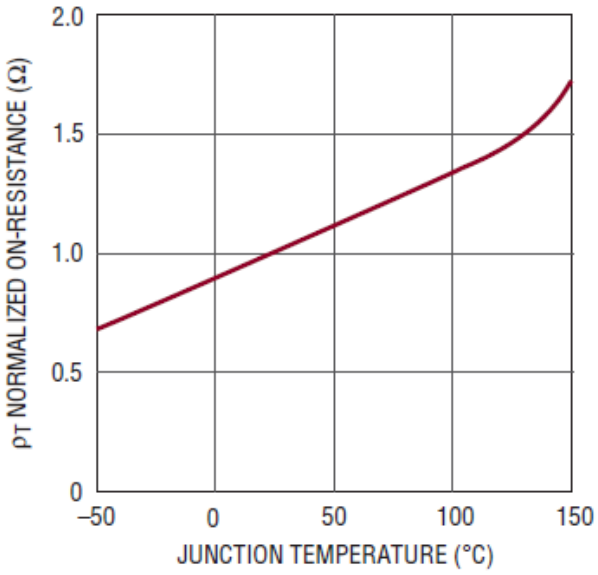


FIGURE 9
THE NORMALIZED $R_{DS(ON)}$ VS. TEMPERATURE [7]

From Figure 9, at 25°C the $R_{DS(on)}$ remains in unity. Table X shows the calculated power values for the four MOSFETs, with $R_{DS(on)}$ left without a specific value, $\rho_T$ left as 1, and $C_{ROSS}$ left without a specific value yet.

TABLE X
MOSFET POWER DISSIPATION INITIAL CALCULATIONS

| | PM1 (Boost, W) | PM2 (Buck, W) | PM3 (Boost, W) | PM4 (Boost, W) |
|---|---|---|---|---|
| Vin = 5V | $2540.16*R_{DS(on)}$ | n/a | $2187.36*R_{DS(on)}$ $+(6.66E10)*C_{ROSS}$ | $352.8*R_{DS(on)}$ |
| Vin = 55V | n/a | $44.5454545*R_{DS(on)}$ | n/a | n/a |

To determine $R_{DS(on)}$ and $C_{ROSS}$ values, one needs to have a datasheet of a MOSFET. For this project, the IXTH180N10T MOSFET has been looked into as a potential candidate [18]. While boasting high $V_{DS}$ and $I_{DS}$ ratings of 180V and 100A, this MOSFET also has typical $R_{DS(on)}$ value of 5.4mΩ and a $C_{ROSS}$ value ranging between 1.5pF to 3pF. So, inputting the typical $R_{DS(on)}$ and 1.5pF to Table X gives the new values as shown in Table XI.

TABLE X
MOSFET POWER DISSIPATION MODIFIED CALCULATIONS

| | PM1 (Boost, W) | PM2 (Buck, W) | PM3 (Boost, W) | PM4 (Boost, W) |
|---|---|---|---|---|
| Vin = 5V | 137.169 | n/a | 118.21734 | 19.0512 |
| Vin = 55V | n/a | 2.40545 | n/a | n/a |

So, a chosen MOSFET must withstand 137.169W, the peak power dissipation coming from the PM1 MOSFET. Fortunately, the IXTH180N10T MOSFET has a 480W power rating at 25°C, so

this MOSFET should be able to handle this peak power given that the MOSFET can operate within a temperature range between a temperature range of -55°C to 175°C.

Since the LT3791 IC can operate within frequencies between 200kHz to 700kHz, the MOSFETs must switch on and off faster than the operating frequencies. The IXTH180N10T MOSFET's switching times appear in Table XI.

TABLE XI
SWITCHING TIMES FOR THE IXTH180N10T MOSFET

| Timing Name | Time (ns) |
|---|---|
| $t_{d(on)}$ | 33 |
| $t_{rise}$ | 54 |
| $t_{d(off)}$ | 42 |
| $t_{fall}$ | 31 |

Based on Table XI, the MOSFET should switch fast enough for the operating frequencies.

The MOSFETs must also tolerate high temperatures when dissipating large power. The IXTH180N10T MOSFET has a thermal resistance junction to case ($R_{thJC}$) value of 0.31°C/W and a thermal resistance case to heatsink ($R_{thCS}$) value of 0.25°C/W. So, as an example, if the MOSFET dissipated 100W, then the temperature on the MOSFET case obtains 31°C plus the room temperature (assuming 25°C), totaling 56°C. Most likely, heatsinks must be included for best performance. With the IXTH180N10T MOSFET having a TO-247 package, the heatsinks must accommodate for these types of packaging. The WA-T247-101E heatsink has been considered due to its small size (1 inch X 0.65 inch) and low thermal resistance of 11°C/W.

### 5.5 Capacitor Selections

Capacitors can help filter or bypass noises and lessen ripple magnitudes. The input capacitors must handle the input current $I_{RMS}$ during buck operation, where the current runs discontinuously. The output capacitors must reduce the output voltage ripple, and create the desired DC (steady-state) voltage. Other miscellaneous capacitors needed for several functions must also be considered.

For the input capacitors, one must first calculate an expected input current. The following equation for $I_{RMS}$ appears as follows from the LT3791 datasheet (also presented as equation (6) seen previously):

$$I_{RMS} = \sqrt{I_{LED}^2 \bullet D + \frac{\Delta I_L^2}{12} \bullet D} \quad (14)$$

The D values represent the duty cycles. Assuming a duty cycle of 37.5%, then the $I_{RMS}$ value becomes 4.3193A. The capacitors must also handle the large $V_{IN}$ coming from the elliptical trainer. Thus, the capacitors must have voltage ratings above 65V and low ESR (effective series resistance) for low power dissipation.

For the output capacitors, the output voltage ripples can change on the capacitor's charging and discharging aspects. The following equations from the LT3791 datasheet determine the voltage ripple for boost and buck operations:

$$\Delta V_{RIPPLE\ (BOOST\_CAP)} = \frac{I_{LED} \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{C_{OUT} \bullet V_{OUT} \bullet f}$$

$$\Delta V_{RIPPLE\ (BUCK\_CAP)} \approx \frac{\Delta I_L}{8 \bullet f \bullet C_{OUT}} \quad (14)$$

Assuming a 600kHz frequency, 36V and 7A output, 5V minimum input, 3A inductor ripple, and 2.2µF, then we have the following answers:

$$\frac{I_{LED} * (V_{OUT} - V_{IN(MIN)})}{C_{OUT} * V_{OUT} * f} = \frac{7A * 31V}{2.2uF * 36V * 600kHz} = 4.5665V_{ripple(boost)}$$

$$\frac{I_L}{C_{OUT} * 8 * f} = \frac{3A}{2.2uF * 8 * 600kHz} = 0.284V_{ripple(buck)}$$

Thus, we need output capacitors valued at 2.2µF that can tolerate these voltage ripples.

For other capacitors needed for miscellaneous functions, one must account for maximum voltage levels seen by these capacitors and the capacitor sizes due to limit PCB layout space. For example, from Figure 8 the capacitor at the SS pin must have a specific value for a slow turn-on startup, where 33nF is the minimum. So, when using a faster switching frequency, a larger capacitor would apply. Most miscellaneous capacitors don't need high voltage ratings, so the most importance feature for these capacitors is size. Table XII shows the capacitor values for these miscellaneous capacitors, as suggested by the LT3791 datasheet.

TABLE XII
CAPACITOR VALUES FOR MISCELLANEOUS CAPACITORS

| Pin Name(s) | Capacitor Values (nF) |
|---|---|
| $V_C$ | 22 |
| SS, $V_{REF}$, CTRL, PWM | 200 |
| SS, $V_{REF}$, CTRL, PWM | 100 |
| $INTV_{CC}$ | 4700 |
| $V_{IN}$ | 1000 |
| IVINN, IVINP | 470 |

**5.6 Resistor Selections**

The IC contains two categories of resistors; the small sense resistors and the "typical" resistors. The IC uses the sense resistors for limiting input current, limiting output current, and determining the value of the output current. The "typical" resistors refer to the voltage divider circuits and other applications (defining frequency, loop compensation, etc.). The sense resistors usually must remain as small as possible for optimal performance, where small means below 1Ω. Due to such small values, the sense resistors must tolerate noisy signals or at least remain as close as possible to the IC on the PCB layout. Since most of these resistors should dissipate power below 1W, one needs resistors with at most 1W power rating.

For limiting the input current, Table V seen previously shows differing current limits for different resistor values. For this project, since the maximum current coming from the elliptical trainer is 5A, the 10mΩ input resistor should suffice for limiting the input current to 5A. For determining the maximum output current limiting resistor, one must consider how much the

Enphase inverter can handle, which in this case is 8A. So, since the IC can regulate the output current through the equation below (where $I_{LED} = I_{OUT}$) [7]:

$$I_{LED} = \frac{100mV}{R_{LED}} \quad (15)$$

Then the sensing resistor $R_{LED}$ can be 13.3mΩ for limiting the output current to 7.5A maximum. Lowering the output current below the inverter's maximum input current ensures that the inverter doesn't operate near its maximum input current, where the 8A current could damage the inverter. For the output current sensing resistor, the following equations can help determine the maximum sense resistor value.

$$I_{OUT(MAX\_BOOST)} = \left( \frac{51mV}{R_{SENSE}} - \frac{\Delta I_L}{2} \right) \bullet \frac{V_{IN(MIN)}}{V_{OUT}} \quad (16)$$

$$I_{OUT(MAX\_BUCK)} = \left( \frac{47.5mV}{R_{SENSE}} + \frac{\Delta I_L}{2} \right) \quad (17)$$

$$R_{SENSE(MAX)} = \frac{2 \bullet 51mV \bullet V_{IN(MIN)}}{2 \bullet I_{LED} \bullet V_{OUT} + \Delta I_{L(BOOST)} \bullet V_{IN(MIN)}} \quad (18)$$

$$R_{SENSE(MAX)} = \frac{2 \bullet 47.5mV}{2 \bullet I_{LED} - \Delta I_{L(BUCK)}} \quad (19)$$

Where $I_{LED} = I_{OUT}$ and equations (16) and (17) become equations (18) and (19). Assuming

$I_{OUT} = I_{LED} = 7A$, $\Delta I_L = 1A$, $V_{IN(MIN)} = 5V$, and $V_{OUT} = 36V$, then we have the following values:

$$I_{OUT(MAX_{BOOST})} = \frac{51mV}{R_{SENSE}} - \frac{\Delta I_L}{2} => R_{SENSE} = 0.001002\Omega = 1.002m\Omega$$

$$I_{OUT(MAX_{BUCK})} = \frac{47.5mV}{R_{SENSE}} + \frac{\Delta I_L}{2} => R_{SENSE} = 7.308m\Omega$$

Since the LT3791 datasheet suggests using a 20% to 30% margin value lower than the calculated $R_{SENSE}$ values, a 0.7mΩ resistor shall be used as the sensing resistor.

For the voltage divider resistors used for several functions, one needs to calculate for these resistors in order to obtain desired voltage references. For example, if one wants an upper voltage limit of 55V, where any higher voltage shuts off the IC, then one needs a voltage divider at the OVLO pin that will reference around 55V. Table XIII shows the calculated resistor values for these voltage dividers for their corresponding functions (pins), and Figure 10 shows an example voltage divider for referencing Table XIII.

TABLE XIII
CALCULATED RESISTOR VALUES FOR VOLTAGE DIVISION

| Pin Name and Resistors: | Top Resistor (kΩ) | Bottom Resistor (kΩ) | Desired Reference Voltage (V) | Actual Reference Voltage (V) |
|---|---|---|---|---|
| Feedback (FB) Resistors | 1500 | 50 | 1.1 | 1.1613 |
| OVLO Resistors | 510 | 27 | 58 | 59.66667 (+)<br>58.175 (-) |
| EN/UVLO Resistors | 510 | 160 | 5 | 6.6178 (+)<br>5.025 (-) |

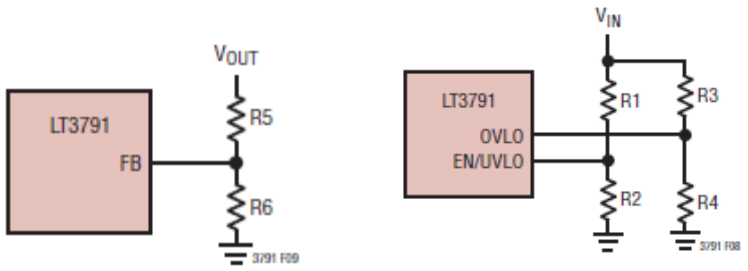


FIGURE 10
EXAMPLES OF VOLTAGE DIVIDERS FOR LT3791 [7]

The values in Table XII were calculated using equations (1-4) and (7).

For the miscellaneous resistors, Table XIV shows the resistor values suggested by the LT3791 datasheet.

TABLE XIV
MISCELLANEOUS RESISTOR VALUES

| Pin Name(s) | Resistor (kΩ) |
|---|---|
| $R_T$ | 37.5 |
| $V_C$ | 2.2 |
| SHORTLED | 200 |
| OPENLED | 200 |
| SS to PWM, CTRL, $V_{REF}$ | 500k |
| IVINN | 0.05 |

**5.7 Diode Selections**

The Schottky diodes have two applications for the IC. The first application concerns with bootstrapping and driving the gates of the top MOSFETs M1 and M4. Referring back to Section 5.2.3, these diodes must withstand a large reverse breakdown voltage coming from the input

voltage, or 60V maximum input. So, Schottky diodes with 65V or larger voltage ratings should suffice for safe operations.

The second application concerns with preventing the body diodes of synchronous switches M2 and M4 from turning on and storing charge during the dead time [7]. The diodes reduce reverse-recovery current between M4's turn-off and M3's turn-on switching. For the diodes to be effective, the inductance between the diodes and the switches must be small, or that the diodes must be placed close to the switches. These diodes must also have a 65V or larger voltage rating due to the input voltage exceeding 60V.

### 5.8 List of Components

With all of these component selections taken, Table XV shows all of the components, their costs, etc. These components mostly come from Digikey or Mouser, due to their wide selections and rapid shipping. The list assumes designing a two parallel IC design, discussed in the next chapter. And with all of these components listed, we can move on to designing the DC-DC converter, where a two parallel IC or three parallel IC design were determined for this project.

TABLE XV
COMPONENTS LIST

| Component Parts | Values | Part Number | Mounting Type | Length | Width | # of Components | Costs per Unit | Total Costs |
|---|---|---|---|---|---|---|---|---|
| Resistors | 1.5MΩ | RHM1.5MKCT-ND | SMD | 2mm | 1.25mm | 2 | $0.10 | $0.20 |
| | 510kΩ | P16051CT-ND | SMD | 2mm | 1.25mm | 4 | $0.50 | $2.00 |
| | 500kΩ | HVCB1206JDL500KCT-ND | SMD | 2mm | 1.25mm | 2 | $3.06 | $6.12 |
| | 200kΩ | A110764CT-ND | SMD | 2mm | 1.25mm | 4 | $0.76 | $3.04 |
| | 160kΩ | 311-160KARCT-ND | SMD | 2mm | 1.25mm | 2 | $0.10 | $0.20 |
| | 50kΩ | PNM0805-50KBCT-ND | SMD | 2.03mm | 1.27mm | 2 | $2.77 | $5.54 |
| | 37.4kΩ | RHM37.4KAHCT-ND | SMD | 2mm | 1.25mm | 2 | $0.17 | $0.34 |
| | 27kΩ | ERJ-P06J273V | SMD | 2mm | 1.2mm | 2 | $1.94 | $3.88 |
| | 2.2kΩ | P2.2KADCT-ND | SMD | 2mm | 1.25mm | 2 | $0.23 | $0.46 |
| | 50Ω | WSCB-50CT-ND | SMD | 6.35mm | 3.81mm | 2 | $1.91 | $3.82 |
| | 13.3mΩ | WSL2512R0130FEA18 | SMD | 6.35mm | 3.18mm | 2 | $1.69 | $3.38 |
| | 10mΩ | P.010AVCT-ND | SMD | 3.2mm | 1.6mm | 2 | $0.90 | $1.80 |
| | 0.7mΩ | ULRB22512R00075FLFSLT | SMD | 6.3mm | 3.2mm | 2 | $4.31 | $8.62 |
| MOSFETs | TO-247 | IXTH180N10T | Through-Hole | 16mm | 5mm | 8 | $4.31 | $17.04 |
| Capacitors | 4.7uF, 50V | 587-2994-1-ND | SMD | 3.2mm | 1.6mm | 10 | $0.50 | $5.00 |
| | 4.7uF, 10V | 587-2258-1-ND | SMD | 3.2mm | 1.6mm | 2 | $0.32 | $0.64 |
| | 2.2uF, 100V | 587-1778-1-ND | SMD | 3.2mm | 2.5mm | 8 | $0.56 | $4.48 |
| | 1uF, 100V | 587-1777-1-ND | SMD | 3.2mm | 1.6mm | 2 | $0.38 | $0.76 |
| | 0.1uF, 100V | 399-1805-1-ND | SMD | 3.2mm | 1.6mm | 4 | $0.24 | $0.96 |
| | 0.1uF, 10V | 399-7999-1-ND | SMD | 2mm | 1.25mm | 2 | $0.12 | $0.24 |
| | 470nF, 10V | 399-9247-1-ND | SMD | 2mm | 1.25mm | 2 | $0.18 | $0.36 |
| | 33nF, 10V | 399-9070-1-ND | SMD | 1.6mm | 0.8mm | 2 | $0.24 | $0.48 |
| | 22nF, 10V | 399-4884-1-ND | SMD | 1mm | 0.5mm | 2 | $0.36 | $0.72 |
| Diodes | 100V | PDS5100-13 | SMD | 6.5mm | 4mm | 4 | $1.63 | $6.52 |
| Inductors | 10uH | 732-4235-1-ND | SMD | 22.5mm | 22mm | 2 | $7.83 | $15.66 |
| Banana Plugs | Black Banana Plugs | 108-0303-001 | Through-Hole | 4.45mm | 4.45mm | 5 | $1.84 | $9.20 |
| | Red Banana | 108-0302-001 | Through-Hole | 4.45mm | 4.45mm | 4 | $1.84 | $7.36 |
| | Black Banana Connector | 108-0903-001 | Through-Hole | 11.125mm | 11.125mm | 5 | $0.70 | $3.50 |
| | Red Banana Connector | 108-0902-001 | Through-Hole | 11.125mm | 11.125mm | 4 | $0.70 | $2.80 |
| Heatsink | TO-247 Heatsink | WA-T247-101E | Through-Hole | 23.4mm | 16mm | 8 | $2.13 | $17.04 |
| PCB | | | | 3.8in. | 2.5in. | 3 | $30 | $90.99 |
| LT3791 | | | | 9.8mm | 6.4mm | 4 | $3.93 | $15.72 |
| Final Costs | | | | | | | | $238.87 |

# Chapter 6: Design Realization

## 6.1 Introduction

In order to accomplish and fulfill the specifications for this project, I suggested two different designs. The first design involves designing the DC-DC converter with two LT3791s in parallel and the second design involves having three LT3791s in parallel. While not intuitive at first glance, both designs can accomplish the specs for this project, though each has its strengths and weaknesses. Again, this project needs more than one IC because the DC-DC converter must output at least 200W, and a single IC can only accomplish only a little above 100W. Also, the project must tolerate an input current of 5A and output current of 8A, and a single IC cannot endure these currents.

When choosing the individual components (resistors, capacitors, MOSFETs, etc.), one needs to consider the size of the PCB layout which the components must solder onto. For this project, I used Express PCB's services, which defines their PCB layouts as a 3.8x2.5 inch board at either $51 (two layered board) or $91 (four-layered board). Thus, this project considers using mostly surface mount devices (SMD), which boasts a smaller size than through-holes components and thus can lower parasitic inductances and capacitances [19, 20]. However, the MOSFETs must remain as through-hole components due to through-hole components having better (lower) junction temperature resistances and higher power dissipation capabilities than SMD counter-parts [19]. Even with these characteristics, through-hole MOSFETs must have heatsinks attached for safe heat dissipation capabilities, or else the PCB can easily overheat and get destroyed from such high voltages (maximum 58V input) and currents (maximum 5A input and 8A output).

### 6.2 Two Parallel ICs

Compared to the three parallel IC design, the two parallel design can fulfill the design requirements by using less components. With less components, less materials are needed to build the circuitry which leads to less precious materials needed. Precious materials needed to build the circuitry include copper, lead, and ceramic materials (which may include zinc, titanium oxide, palladium, aluminum, tantalum, etc. [21, 22]). These materials cannot be replaced or substituted [23], so using as little precious materials as possible ensures a sustainable system until better designs in the future come along.

One drawback to using this design, however, includes considering the current flowing through the inductors. With the two parallel design, more current flows through the two inductors than flowing through three inductors of the three parallel IC design. The inductors chosen for the two parallel design must withstand these large current flows. The inductor chosen for this project (the 10µH SMD) has a maximum current rating of 21A and saturation rating of 26A, and this project should expect a maximum peak current of 9A flowing through the inductor in both the two parallel and three parallel design. So, this inductor should suffice in tolerating the large current flow.

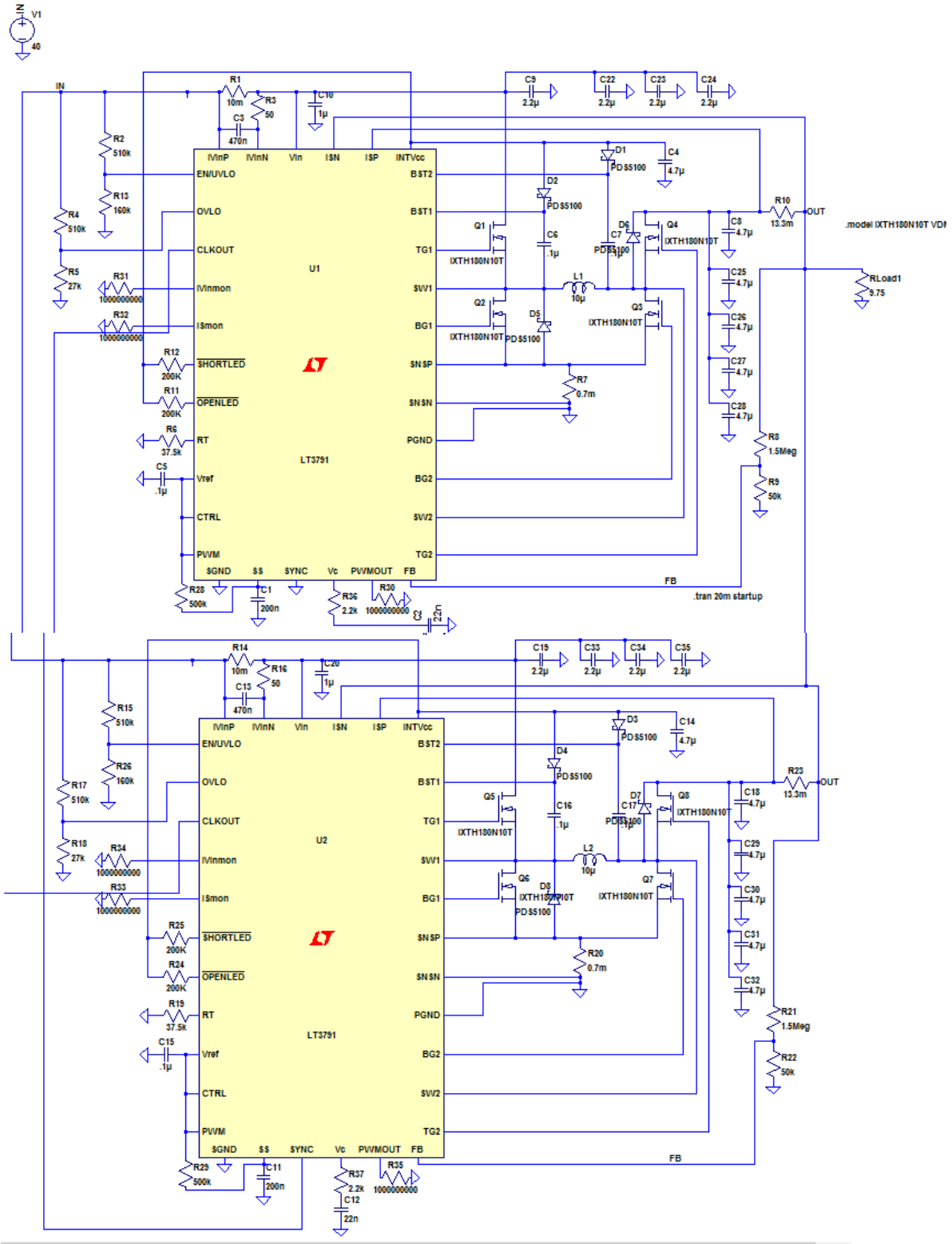


FIGURE 11
TWO PARALLEL IC DESIGN

Figure 11 shows the two parallel design for this project. This design uses the components previous described in chapter 5; this design aims for a 600kHz, 37V output for an input range between 5V to 58V, 10µH inductor, etc. (all described in chapter 5). The load was first tested as a 10Ω load, then a 7Ω load based on Hilario's test runs on what the inverter's input resistance appears as [2], and then with a current load ranging from 0A to 8A. The extra resistors (1GΩ) attached to the PWMOUT, IVINMON, and ISMON pins are for speeding up simulations purposes and are not part of the final PCB layout.

### 6.3 Three Parallel ICs

Compared to the two parallel IC design, the three parallel design can have less power dissipations through each IC, thus ensuring much safer operations. However, creating three PCBs equates to more components and resources used. Thus, the three parallel IC design can be less sustainable than the two parallel IC design because more components must be replaced during maintenance and operations.

The three parallel design matches the two parallel design component-wise, but the three parallel design has one extra IC connected to the second IC through the CLKOUT pin (from the second IC's) to the SYNC (extra IC's) pin. Again, the three parallel design would have less current flowing through each IC compared to the two parallel IC design.

With the designs set, the simulations representation the designs must be taken. I used LTSpice to simulate the two parallel and three parallel designs, as discussed in Chapter 7.

# Chapter 7: LTSpice Simulations

## 7.1 Introduction

After designing the DC-DC Converter around the LT3791, one needs to simulate the design to acquire data about expected power, voltage, current, and efficiency reports. I used LTSpice to simulate the two and three parallel IC designs. For the MOSFET models, I first simulated using a generic MOSFET model that LTSpice has already in its library for faster simulations so as to see and understand how the IC operates. Then I implemented a model MOSFET based on the IXTH180N10T MOSFET. The generic MOSFET was the RJK0651DPB available in the LTSpice MOSFET library. Linear Technology used this generic MOSFET for their LT3791 example on LTSpice available online [24]. This MOSFET has the following characteristics in Table XVI, provided by the datasheet from Renesas [25].

TABLE XVI
RJK0651DPB MOSFET CHARACTERISTICS

| | |
|---|---|
| $V_{DS(on)max}$ (V) | 60 |
| $V_{GSSmax}$ (V) | 20 |
| $R_{DS(on)}$ typical (mΩ) | 11 |
| $I_{Dmax}$ (A) | 25 |
| Channel Temperature Maximum (°C) | 150 |
| Channel Dissipation Maximum (W) | 45 |
| Turn-on delay time (ns) | 8.4 |
| Rise Time (ns) | 4.4 |
| Turn-off delay time (ns) | 42 |
| Fall Time (ns) | 6.8 |
| Channel to Case Thermal Resistance (°C/W) | 2.78 |

While the RJK0651DPB MOSFET can simulate well in LTSpice without any "def-con" or timing out, this MOSFET cannot be used for this project because the $V_{DS(on)max}$ is too low at 60V and the thermal resistance must be lower for optimal heat dissipation. With only 2.78°C/W, this MOSFET can theoretically overheat if it dissipates 55W (or 152.9°C). Thus, a better MOSFET with a higher $V_{DS(on)max}$ and lower thermal resistance must be considered; the IXTH180N10T MOSFET fulfills these requirements and boasts other perks, such as a lower $R_{DS(on)}$ and higher $I_{Dmax}$.

While the generic MOSFET simulations do not accurately reflect the final design since the RJK0651DPB MOSFET cannot be used for this project, the following simulations in the next section (7.2) helps understand how the IC behaves. For example, since the datasheet doesn't

entirely explain what to expect for the maximum inductor current $I_L$, these simulations should help better understand the expected inductor current.

### 7.2 RJK0651DPB MOSFET

The RJK0651DPB MOSFET simulations use the following test cases in Table XVII.

TABLE XVII
TEST CASES FOR RJK0651DPB MOSFET SIMULATIONS

| Test Case # | # ICs | $V_{IN}$ (V) | $I_{OUT}$ Load (A) | Output Resistance Load (Ω) |
|---|---|---|---|---|
| 1 | 2 | 0 to 60 to 0 | n/a | 10 |
| 2 | 3 | 0 to 60 to 0 | n/a | 10 |
| 3 | 2 | 15 | 0 to 8 | n/a |
| 4 | 2 | 55 | 0 to 8 | n/a |

The test cases in Table XVII were chosen to analyze the LT3791's behavior, such as typical power dissipations across the MOSFETs and typical ripple current across the inductor. Each case has different load cases; the first case refers to the simulations using an output resistor load 10Ω for an input voltage ranging from 0V to 60V to 12V (increments and decrements by 12V every 2ms; input would stay at 12V between 1ms to 2ms, then increment during 2ms to 3ms, and stays at 24V between 3ms to 4ms, etc.), and the second case refers to using a current load ranging from 0A to 8A (increments every 2ms) and an input voltage 36V. For reference, in Figure 11, the MOSFETs are arranged in a U-shape; the first MOSFET Q1 is the top left, Q2 is bottom left, Q3 is the bottom right, and Q4 is the top right.

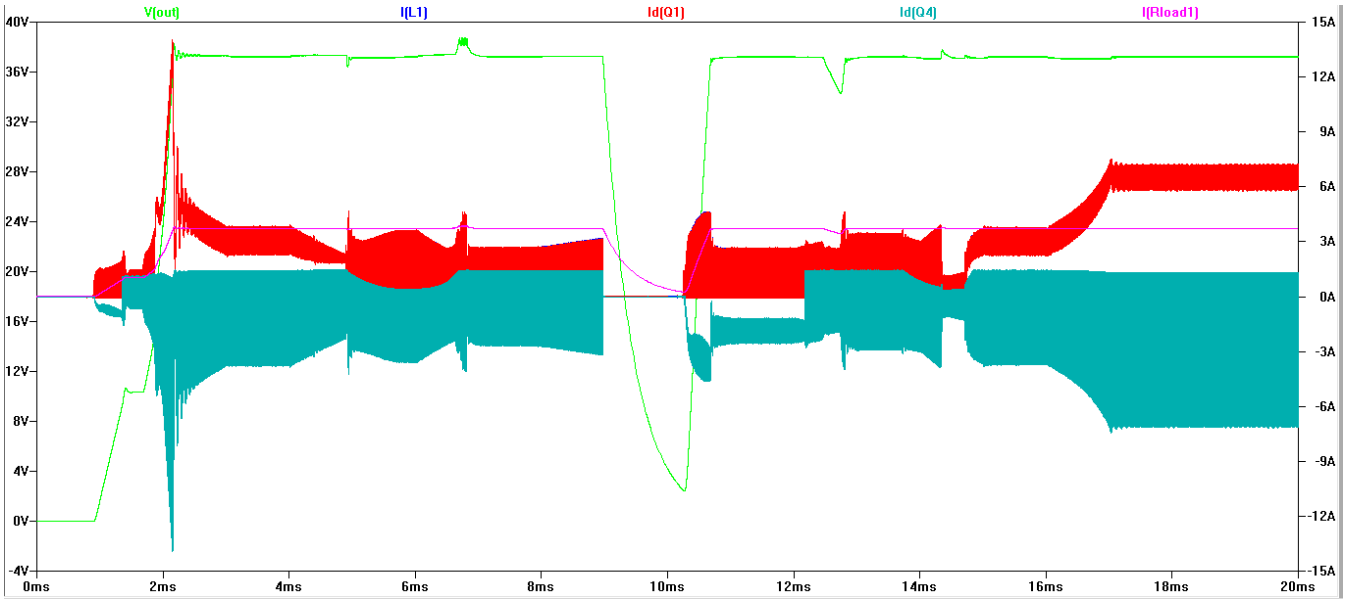


FIGURE 12

SIMULATIONS FOR TEST CASE #1, VARYING INPUT AND 10Ω LOAD, PART 1 {$V_{OUT}$ (GREEN), INDUCTOR CURRENT $I_L$ (BLUE), $I_{D(Q1)}$ (RED), $I_{D(Q4)}$ (TEAL), CURRENT LOAD (PINK)}

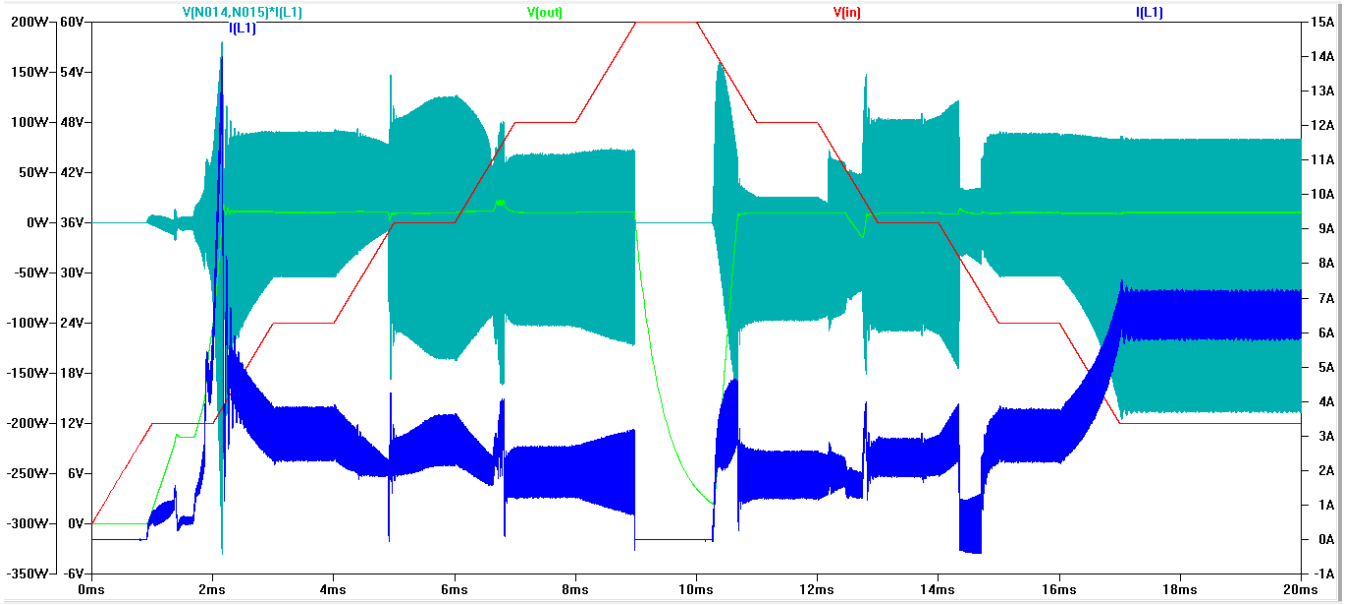


FIGURE 13

SIMULATIONS FOR TEST CASE #1, VARYING INPUT AND 10Ω LOAD, PART 2 {INDUCTOR POWER (TEAL), $V_{OUT}$ (GREEN), $V_{IN}$ (RED), INDUCTOR CURRENT $I_L$ (BLUE)}

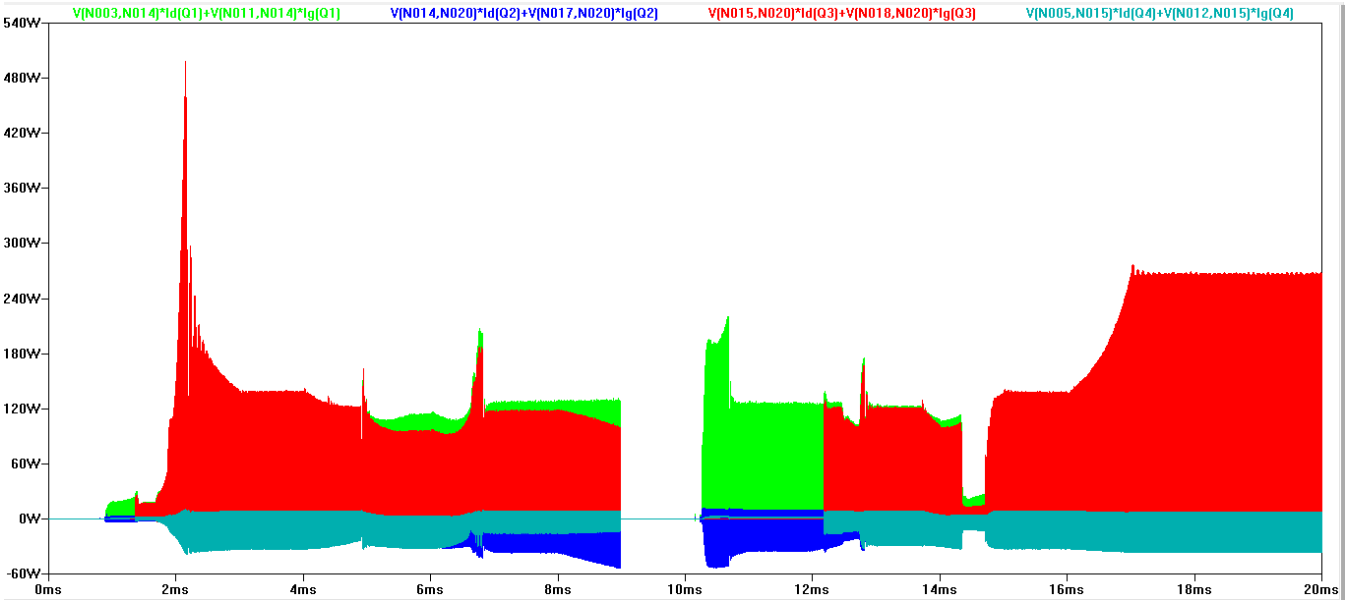


FIGURE 14
SIMULATIONS FOR TEST CASE #1, VARYING INPUT AND 10Ω LOAD, PART 3 {Q1 POWER (GREEN), Q2 POWER (BLUE), Q3 POWER (RED), Q4 POWER (TEAL)}

From Figure 12, the inductor current (blue) and $I_{D(Q1)}$ (red) overlap each other. This test case concentrates on understanding the soft-start function, or whether the soft-start function actually works as expected. From Figures 12 and 13, the current through $I_{D(Q1)}$, $I_L$, and $I_{D(Q4)}$ peaks the highest value of 14.5A around 2ms, where the IC begins to turn on and charges $V_{OUT}$ from 0V to 37V. These current spikes result in high power dissipations across Q1, as shown in Figure 14. The SS (soft-start) should have handled this spike by slowing down the turn-on charge. The simulations may not be implementing the soft-start functions in LTSpice, since the provided LT3791 example simulation from Linear Technology's website [24] also showed similar simulation results where the turn-on charge exceeds some high value than expected.

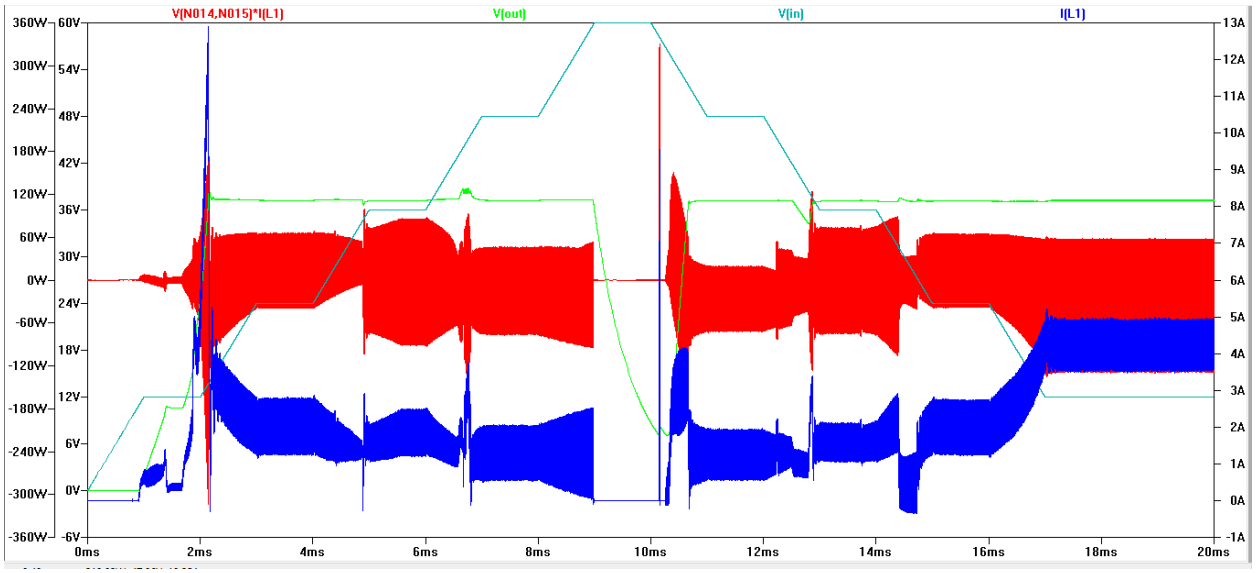


FIGURE 15

SIMULATIONS FOR TEST CASE #2, VARYING INPUT AND 10Ω LOAD, PART 1 {$V_{OUT}$ (GREEN), INDUCTOR CURRENT $I_L$ (BLUE), INDUCTOR POWER DISSIPATION (RED), $V_{IN}$ (TEAL)}

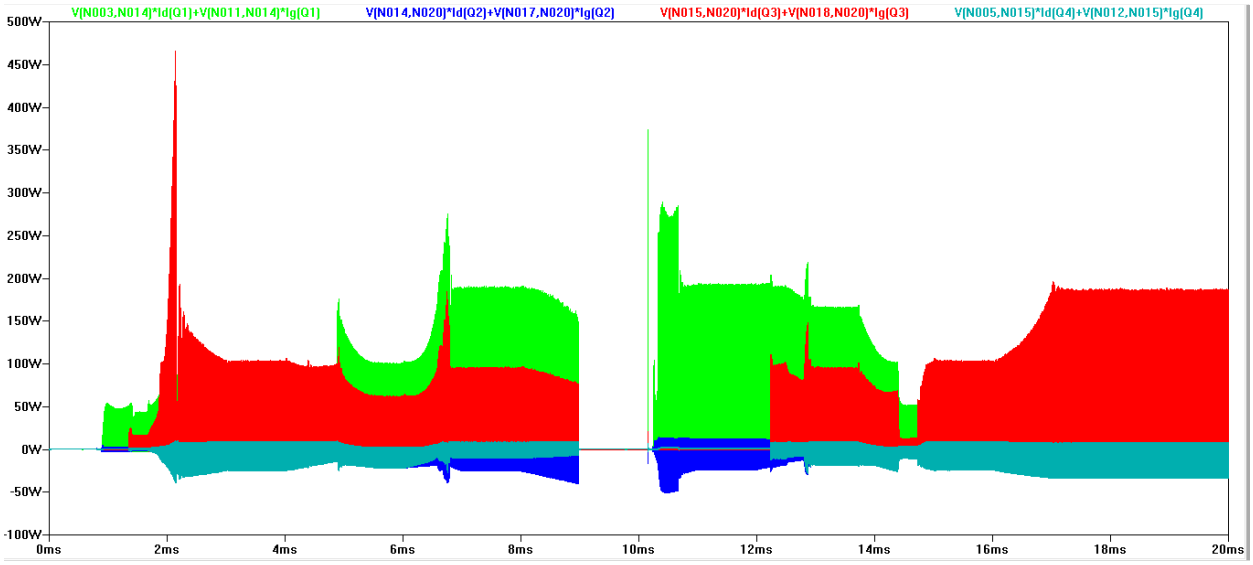


FIGURE 16

SIMULATIONS FOR TEST CASE #2, VARYING INPUT AND 10Ω LOAD, PART 2 {Q1 POWER (GREEN), Q2 POWER (BLUE), Q3 POWER (RED), Q4 POWER (TEAL)}

Test case #2 shows the simulations for three parallel ICs, where the expected current through each IC should be lower than the current through the two parallel ICs. Test cases #1 and #2 have

the exact same test cases, and only different number of ICs used. Comparing Figure 15 with Figure 13, the inductor current lowers from an average 6.5A (two ICs) to 4.25A (three ICs), which that the inductor does experience a lower current average. This lower current also translates to lower power dissipations across the MOSFETs, as shown in Figures 14 and 16.

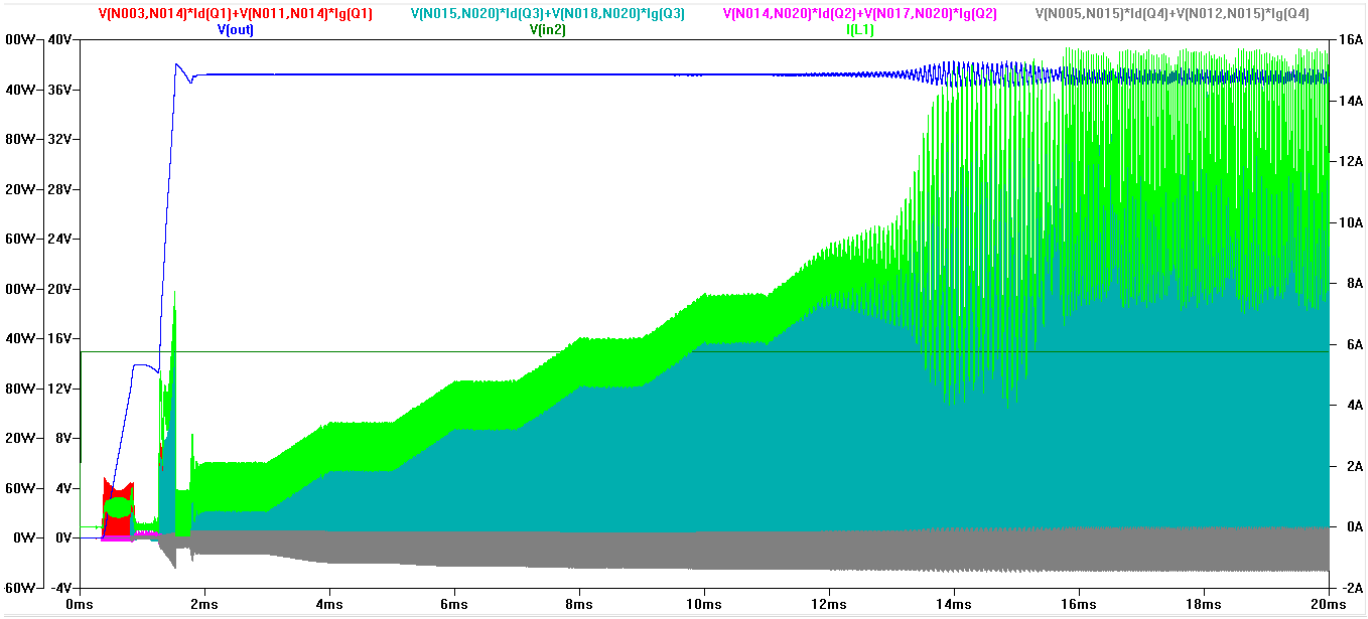


FIGURE 17
SIMULATIONS FOR TEST CASE #3, 15V INPUT AND VARYING CURRENT LOAD {Q1 POWER (RED), Q3 POWER (TEAL), Q2 POWER (PINK), Q4 POWER (GREY), $V_{OUT}$ (BLUE), $V_{IN}$ (DARK GREEN), INDUCTOR CURRENT $I_L$ (GREEN)}

From Figure 17, a current load was used to determine how the IC would react when the output current was controlled, where 8A was the maximum current output that the Enphase inverter could handle. Since this project aims for a maximum 7A output from the DC-DC converter, Figure 17 shows that during a current load of 7A (between 14ms and 15ms), $V_{OUT}$ becomes noisy due to the IC trying to determine whether to turn off or on since the IC limits output current at 7A. Also, since a 15V input was provided (boost mode), MOSFETs Q3 and Q4 would

experience the highest power dissipations, with about 600W peak maximum power dissipation during a 8A current load. Since the Enphase inverter may try to obtain as much current as possible from the DC-DC converter (due to MPPT), then we expect the inverter to try to obtain 7A from the DC-DC converter and thus we must ensure the MOSFETs would tolerate such high power dissipations.

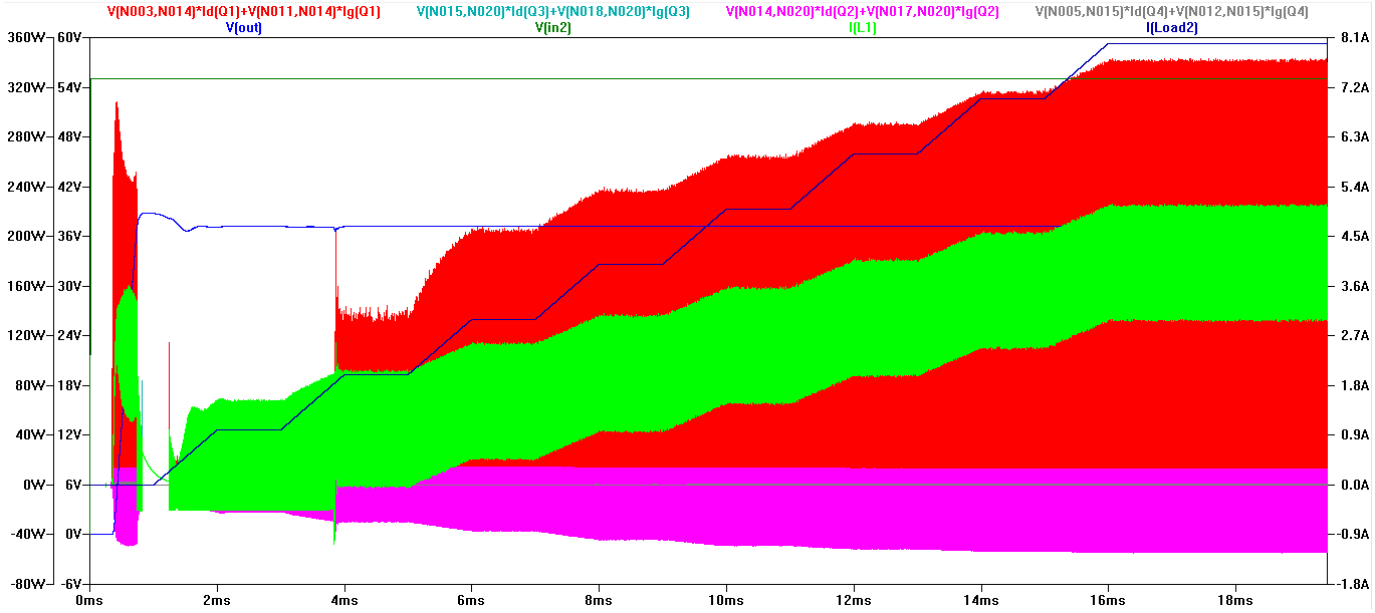


FIGURE 18

SIMULATIONS FOR TEST CASE #4, 55V INPUT AND VARYING CURRENT LOAD {Q1 POWER (RED), Q3 POWER (TEAL), Q2 POWER (PINK), Q4 POWER (GREY), $V_{OUT}$ (BLUE), $V_{IN}$ (DARK GREEN), INDUCTOR CURRENT $I_L$ (GREEN), CURRENT LOAD (DARK BLUE)}

In Figure 18, unlike Figure 17, the output voltage and current remain steady instead of noisy, even while the output current peaks at 8A. This result may stem from that the simulations runs in buck mode, where less input current runs through the IC than during boost mode; to maintain around 90% power efficiency, since the input already has 55V, then the IC needs a smaller input current compared to a higher input current for boost mode. Also, Q1 and Q2 now experience the

highest power dissipation, with Q1 peaking a peak maximum power of 340W during a 8A current load.

### 7.3 IXTH180N10T MOSFET

This section discusses the simulations using the IXTH180N10T MOSFET model, which represents the actual MOSFET used for this project. The IXTH180N10T MOSFET has varying Vto between 2.5V and 4.5V, but 4.5V was too high for the MOSFETs to have since the IC only provides 5V gate drive (0.5V = $V_{GS}$ wasn't enough to turn the MOSFETs on). So, the MOSFET model on LTSpice has Vto=3.5, as shown below:

.model IXTH180N10T_2 VDMOS(RG=3.3 Vto=3.5 Rd=6.3m Rs=0.0m Rb=2.8m Cgdmax=0.3n Cgdmin=0.15n Cgs=5n Cjo=0.8n mfg=IXYS Vds=100 Ron=6.5m Qg=151n M=.84343 N=2.9032 BV=100 IBV=5E-6 Vj=0.95 Kp=100.18)

From the model above, parameters M (body diode grading coefficient) and N (bulk diode emission coefficient) were based on another IXYS model, IXTH88N15. This IXYS model was used because the IXTH180N10T model was not provided by IXYS Corporation, and the IXTH88N15 was the closest model to the IXTH180N10T that was provided by IXYS. The other parameter values, however, remain based on the IXTH180N10T values [18]. The Kp parameter, though, needed to be calculated since the IXYS datasheet doesn't provide a Kp value. The calculations above below, based on the IXTH180N10T datasheet:

$$I_D = \frac{1}{2} K_n' \frac{W}{L} \left(V_{gs} - V_T\right)^2 (1 + \lambda(V_{DS} - V_{DSat})) \quad (20)$$

Known: $I_D$ = 60A, $V_{gs}$ -$V_T$ = 2.5V, and assuming λ = 0 and W = L = 1μm,

then (1/2)(K')*(W/L) = I/(Vgs-Vt)^2 = 60 A/(2.5 V)^2 = 9.6 A/V^2.

But,

$$K = \frac{g}{(V_{GS} - V_T)} \quad (21)$$

$$\text{or } K = \frac{g^2}{2I_{DS}} \quad (22)$$

where g represents the transconductance and equals 110 A/V (from datasheet [18]).

Using equation 22, K = 100.833 A/V^2.

So, K remains a value between 9.6 and 100.833. This wide range occurs because equation 22 doesn't reference $V_{GS}$, and equation 20 doesn't account for the actual λ value (assumed λ = 0). Thus, 100.83 A/V^2 was chosen as the parameter because a larger K value should represent the 100A maximum across the MOSFET. Table XVIII shows the test cases used for this new MOSFET.

TABLE XVIII
TEST CASES FOR IXTH180N10T MOSFET SIMULATIONS

| Test Case # | # ICs | $V_{IN}$ (V) | $I_{OUT}$ Load (A) | Output Resistance Load (Ω) |
|---|---|---|---|---|
| 1 | 2 | 0 to 60 to 0 | n/a | 10 |
| 2 | 2 | 0 to 60 to 0 | n/a | 10 |
| 3 | 2 | 36 | 0 to 8 | n/a |
| 4 | 2 | 55 | 8 to 0 | n/a |
| 5 | 2 | 15 | 8 to 0 | n/a |

From Table XVIII, the number of ICs remain as two (2), since the simulations for three ICs took over 3 hours for each simulation to finish. So, the three IC parallel design was abandoned at this point.

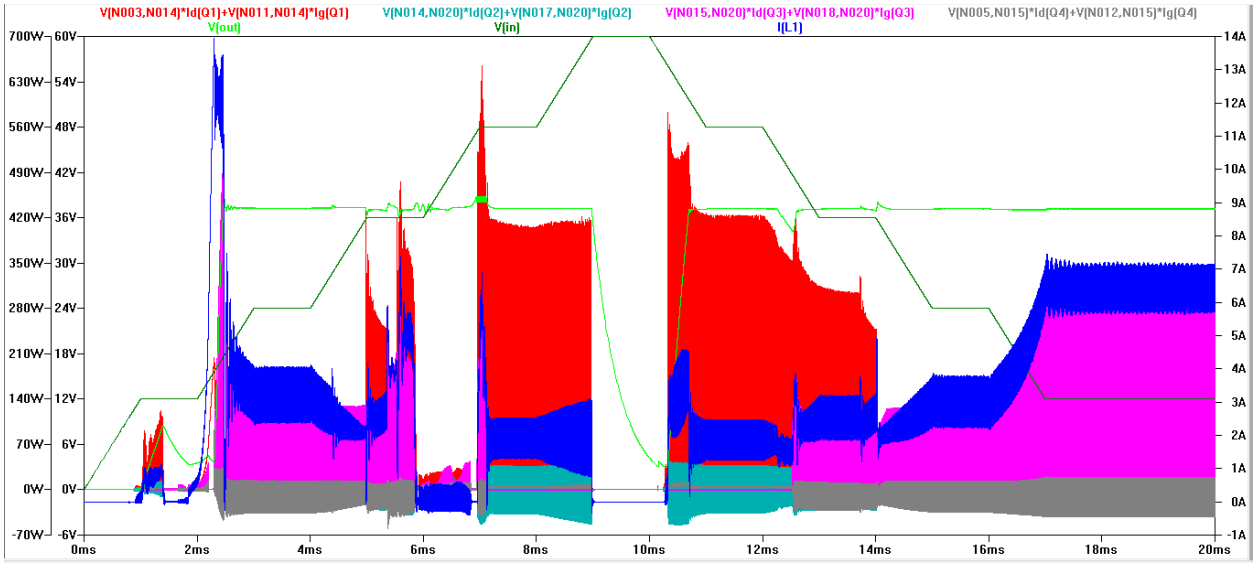


FIGURE 19

SIMULATIONS FOR TEST CASE #1, VARYING INPUT AND 10Ω LOAD, SMALL SS CAPACITOR, {Q1 POWER (RED), Q2 POWER (TEAL), Q3 POWER (PINK), Q4 POWER (GREY), $V_{OUT}$ (GREEN), $V_{IN}$ (DARK GREEN), INDUCTOR CURRENT $I_L$ (BLUE)}

From Figure 19, the IC begins to turn on after 2ms, where the input voltage is at 12V. At this moment, in rush current flows through the IC, which causes a large power dissipation across Q3 (500W). The IC was supposed to handle this in rush current by using the soft-start function to lower the current during start-up. The simulations, however, may not be reading or simulating with a soft-start within its calculations, so this in rush current may not actually occur in our actual project. However, for safety precautions, the in rush current must somehow be lowered in the simulations. Also of note, since the input voltage range in the simulations go as high as 60V and the IC has a OVLO limit at 58V, then the IC should turn off when the input voltage exceeds 58V. This situation does occur in Figure 19, where $V_{OUT}$ drops exponentially and all power dissipation drops below zero.

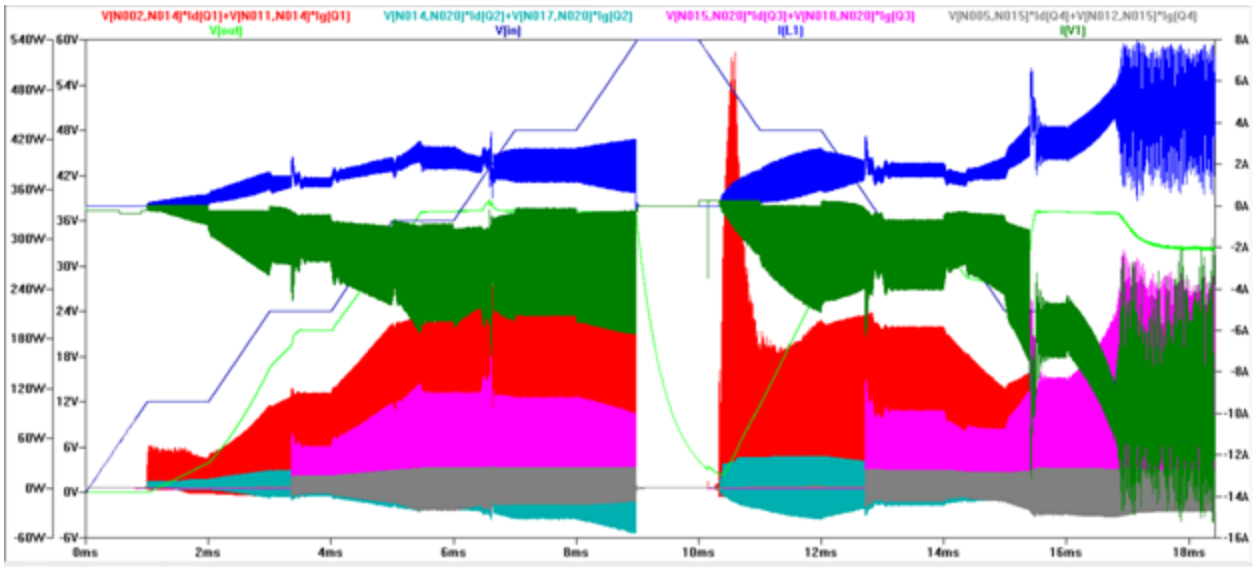


FIGURE 20

SIMULATIONS FOR TEST CASE #2, VARYING INPUT AND 10Ω LOAD, LARGE SS CAPACITOR {Q1 POWER (RED), Q2 POWER (TEAL), Q3 POWER (PINK), Q4 POWER (GREY), $V_{OUT}$ (GREEN), $V_{IN}$ (DARK GREEN), INDUCTOR CURRENT $I_L$ (BLUE)}

Test cases #1 and #2 have the same cases, but have different SS capacitors. Test case #1 has a 33nF capacitor and test case #2 has a 200nF capacitor; a higher valued capacitor should slow down the start-up functions in the IC. From Figure 20, the in rush current has disappeared at around 2ms, unlike what Figure 19 showed. However, the in-rush current after 10ms still outputs a huge current spike from the large input voltage 58V, since the IC starts up again after being off due to too high an input voltage at 60V. So, while the in rush current was eliminated at 2ms, the 10ms in rush current still occurs.

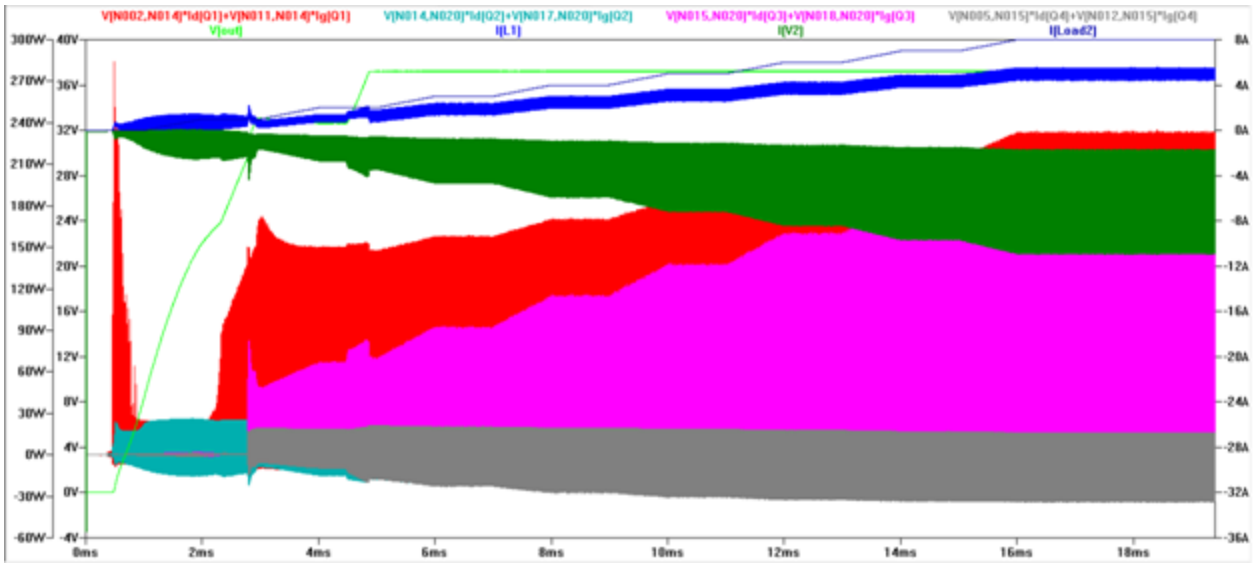


FIGURE 21

SIMULATIONS FOR TEST CASE #3, 36V INPUT AND VARYING CURRENT LOAD {Q1 POWER (RED), Q2 POWER (TEAL), Q3 POWER (PINK), Q4 POWER (GREY), $V_{OUT}$ (GREEN), $I_{IN}$ (DARK GREEN), INDUCTOR CURRENT $I_L$ (BLUE)}

Test case #3 examines how the modified MOSFETs respond to a current load. From Figure 21, the input current steadily rises from 0A to 11A, which was due to the input voltage source assuming an indefinite amount of current provided. Since the elliptical trainer can only provide 5A maximum, the input current in Figure 21 should be ignored. Also, the in rush current appears again at 0.5ms, where Q1 dissipates almost 280W. So, the 200nF capacitor doesn't work for this simulation.

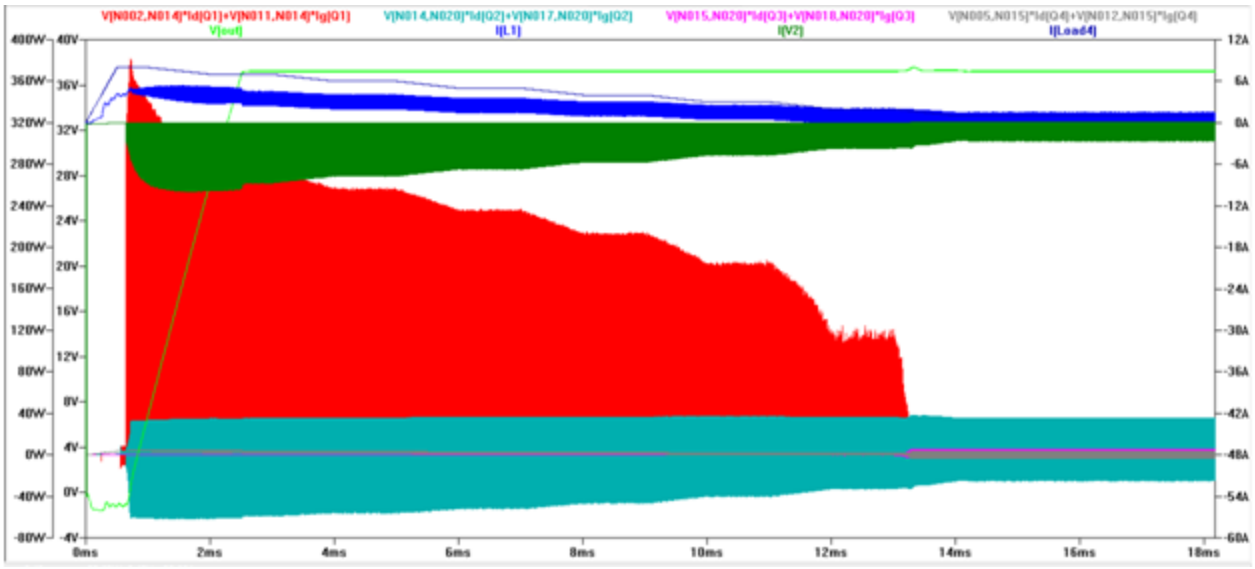


FIGURE 22

SIMULATIONS FOR TEST CASE #4, 55V INPUT AND VARYING CURRENT LOAD {Q1 POWER (RED), Q2 POWER (TEAL), Q3 POWER (PINK), Q4 POWER (GREY), $V_{OUT}$ (GREEN), $I_{IN}$ (DARK GREEN), INDUCTOR CURRENT $I_L$ (BLUE)}

From Figure 22, the current load starts at 8A and decreases to 0A instead of vice-versa, so as to examine how the IC responds to a large voltage and current entering through the IC during start-up. Q1 dissipates the largest power at almost 380W during start-up, and so the IC cannot handle such large power dissipations without a heatsink with a low thermal resistance.

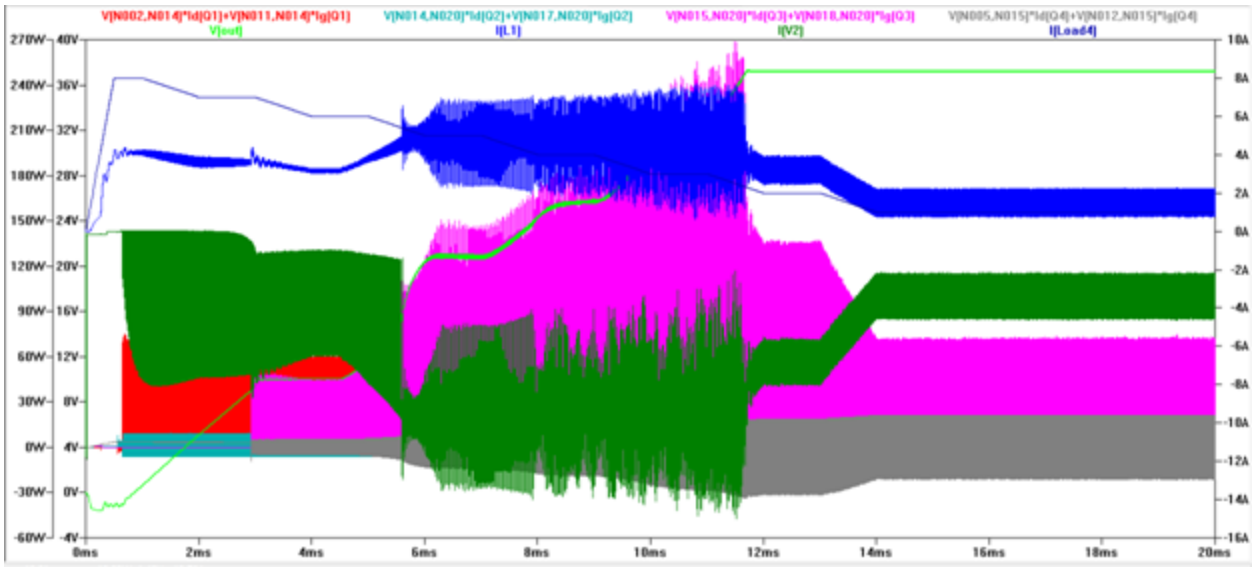


FIGURE 23

SIMULATIONS FOR TEST CASE #5, 15V INPUT AND VARYING CURRENT LOAD {Q1 POWER (RED), Q2 POWER (TEAL), Q3 POWER (PINK), Q4 POWER (GREY), $V_{OUT}$ (GREEN), $I_{IN}$ (DARK GREEN), INDUCTOR CURRENT $I_L$ (BLUE)}

From Figure 23, the low input voltage 15V causes the IC to require more current for a higher power efficiency, as evident during between 0ms to 12ms where $V_{OUT}$ doesn't peak at 36V. Since the output must peak at 36V and some output current, and the input voltage remains at 15V, then the input current must also rise in order for the IC to achieve a high power efficiency. For example, 90% power efficiency means an output of 36V and 3.6A, or 129.6W, and an input of 15V and 9.6A, or 144W. Since the elliptical cannot supply 9.6A, this simulation shows a non-realistic situation for our project. So, Figure 23 does show that 15V input can prove difficult to implement within this project. Thus, this IC needs more alterations to handle such low input voltages.

### 7.4 Choosing the Design Based on Simulations

Based on the simulations so far, both parallel IC designs have their strengths and weaknesses. So, I chose to use the two parallel design because this design requires less components, which means less time to solder on the components and less time to check connections when troubleshooting the circuitry during the testing phase. Also, since the three parallel design simulations took too long to simulate, I abandoned this design and stayed with the two parallel design. Thus, with the two parallel design finalized, I needed to design the PCB layout of the circuit, discussed in Chapter 8.

# Chapter 8: PCB Layout

### 8.1 Introduction

While determining all the component designs and while running simulations, the author also needs to design the PCB layout to place the components together onto one board. In this project, two 3.8"x2.5" boards are needed to design the two parallel ICs, where each board contains the LT3791 and DC-DC converter. Express PCB was used to design the PCB layout, since the company Express PCB offers a cheap price for three 4-layered boards at $91. The company also offers three 2-layered boards at $51, but designing the project with only two boards may prove difficult. So, two PCB layout drafts have been initially created to determine the best design choice for this project.

### 8.2 First PCB Layout - 2-Layered Board

The goal for the first PCB layout was to determine whether the two parallel IC design can run on a 2-layered or 4-layered board. Using a 2-layered board lowers overall cost of the project; the

2-layered board costs $51 and the 4-layered boards costs $91, and both costs didn't account for shipping fees or taxes. However, a 4-layered board allows designers to create the components and traces without too much restriction from limited space like the 2-layered board has. If one uses a 2-layered board, the top layer must act as the power layer and the bottom layer must act as the ground layer. A 4-layered board has the power and ground layers already established in addition to the top and bottom layers for designing the circuitry. Thus, the 4-layerd board can help designers easily design a PCB layout without too much time invested being creative with circuitry on a 2-layered board.

From a sustainability standpoint, the 2-layered board uses less components, or less materials, than the 4-layered board. A sustainable product can remain sustainable indefinitely as long as the product doesn't interfere with an ecosystem or release harmful by-products within the environment [26]. So, while the 2-layered board doesn't necessarily fulfill this definition, the 2-layered board at least doesn't impact the environment as much as the 4-layered board. Figure 24 shows the first attempt of the PCB layout for a 2-layered board.

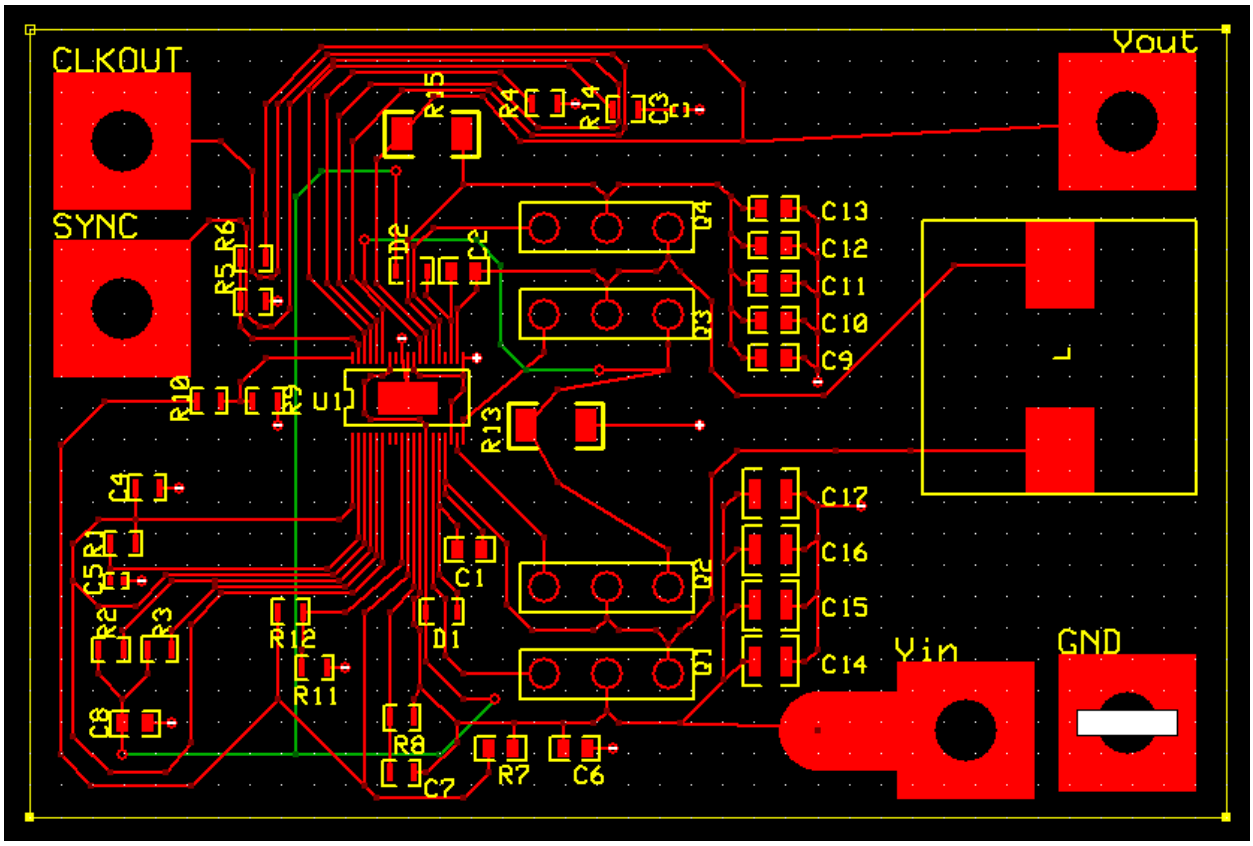


FIGURE 24
FIRST PCB LAYOUT DRAFT

From Figure 24, the traces remain thin for purposes of determining whether a 2-layered board was feasible. Based on the first PCB layout, a 2-layered board proves difficult to design with because the traces have to loop around other traces, where these traces have high sensitivity to noises. This PCB layout also neglects considering in adding heatsinks to the MOSFETs, which would take more space on the board. So, a 4-layered PCB layout was established in the next section.

### 8.3 Second PCB Layout - 4-Layered Board

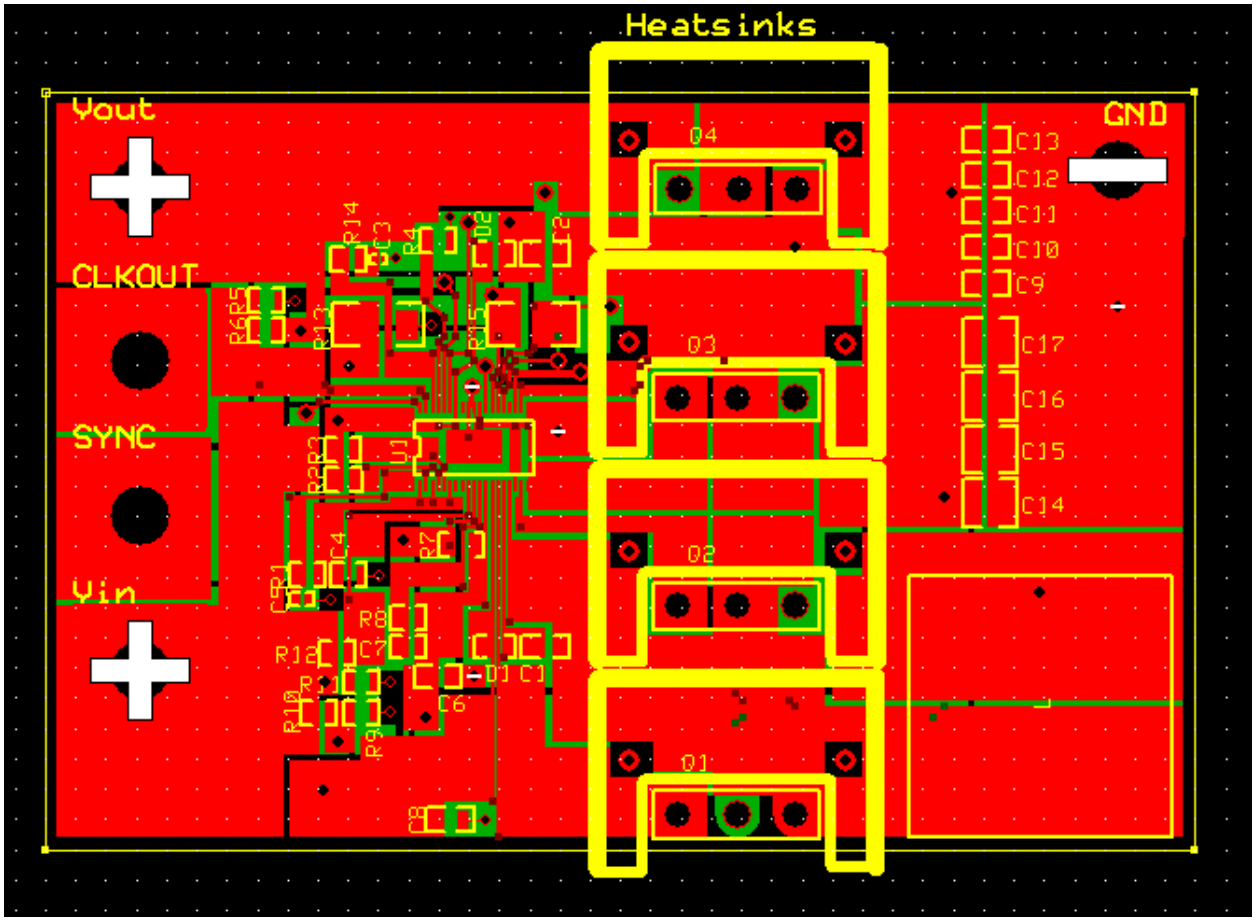


FIGURE 25
SECOND PCB LAYOUT DRAFT - TOP LAYER

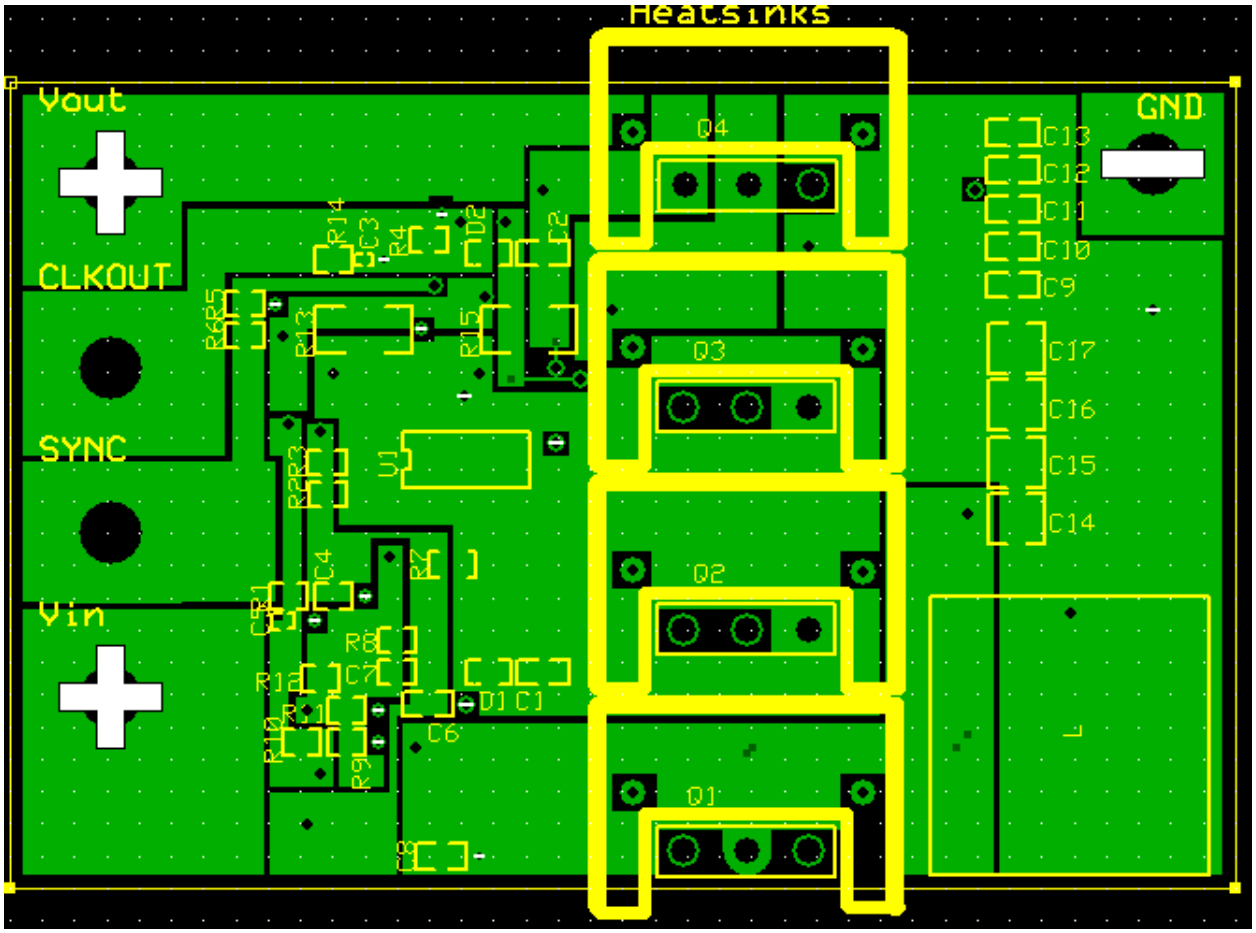


FIGURE 26
SECOND PCB LAYOUT DRAFT - BOTTOM LAYER

From Figures 25 and 26, the new PCB draft has the heatsinks added onto the 4-layered board, and more thicker traces added. This design helps lower heat dissipation across the board, but neglects several issues. For example, the top and bottom layers contain large traces overlapping each other, which would create large capacitances across the board and slow down the circuitry. Since this project aims for 6ookHz and contains small, sensitive resistors (i.e. 0.7mΩ), the revised draft must eliminate any traces overlapping each other.

This draft also neglects to use the ground layer properly, so another revision was needed to ensure the ground layer splits into the power and signal grounds. If the two sets of ground do not

meet at a single point on the board, the sensitive signal ground would become noisy from the power ground. Several dedicated ground points (SGND and PGND) have also been ignored, where two PCBs need to connect between the ground layers instead of two separate ground layers.

The heatsinks were also too close together, which would otherwise make the heatsinks redundant for their purposes of dissipating heat throughout the air. So, the revised draft must also separate the heatsinks away from each other. Ideally, the heatsinks should be far enough apart from each other to dissipate heat based on the specified thermal resistance (i.e. 8°C/W).

Finally, several test points must be made on the PCB layout to determine whether this PCB layout can actually operate or not. Test points needed include the $V_{CC}$, EN, FB, and $V_{REF}$ pins. These test points aid designers to determine whether the expected DC voltages or AC voltage signals actually occur.

# Chapter 9: Revisions and Combining Teams

## 9.1 Introduction

Due to time constraints, Sheldon Chu, David Vuong, and I cooperated together to create the DC-DC converter. We used Sheldon's and David's design, the LT3791-1, since this design had the most simulations that suggests that this design could work; my simulations disregarded using parasitic resistances across the input voltage source and had unrealistic input currents coming from the input voltage source.

### 9.2 Revised Design

The revised design now uses the LT3791-1, which was an alternative to the LT3791 [16]. The LT3791-1 was made since the LT3791 was made for LED driving, whereas the LT3791-1 acts purely as a DC-DC converter. Thus, the LT3791-1 has a few pins different from the LT3791-1. For example, the LT3791-1 has a CCM pin for ensuring the IC operates in continuous conduction mode. Figure 27 shows an example LT3791-1 circuit.

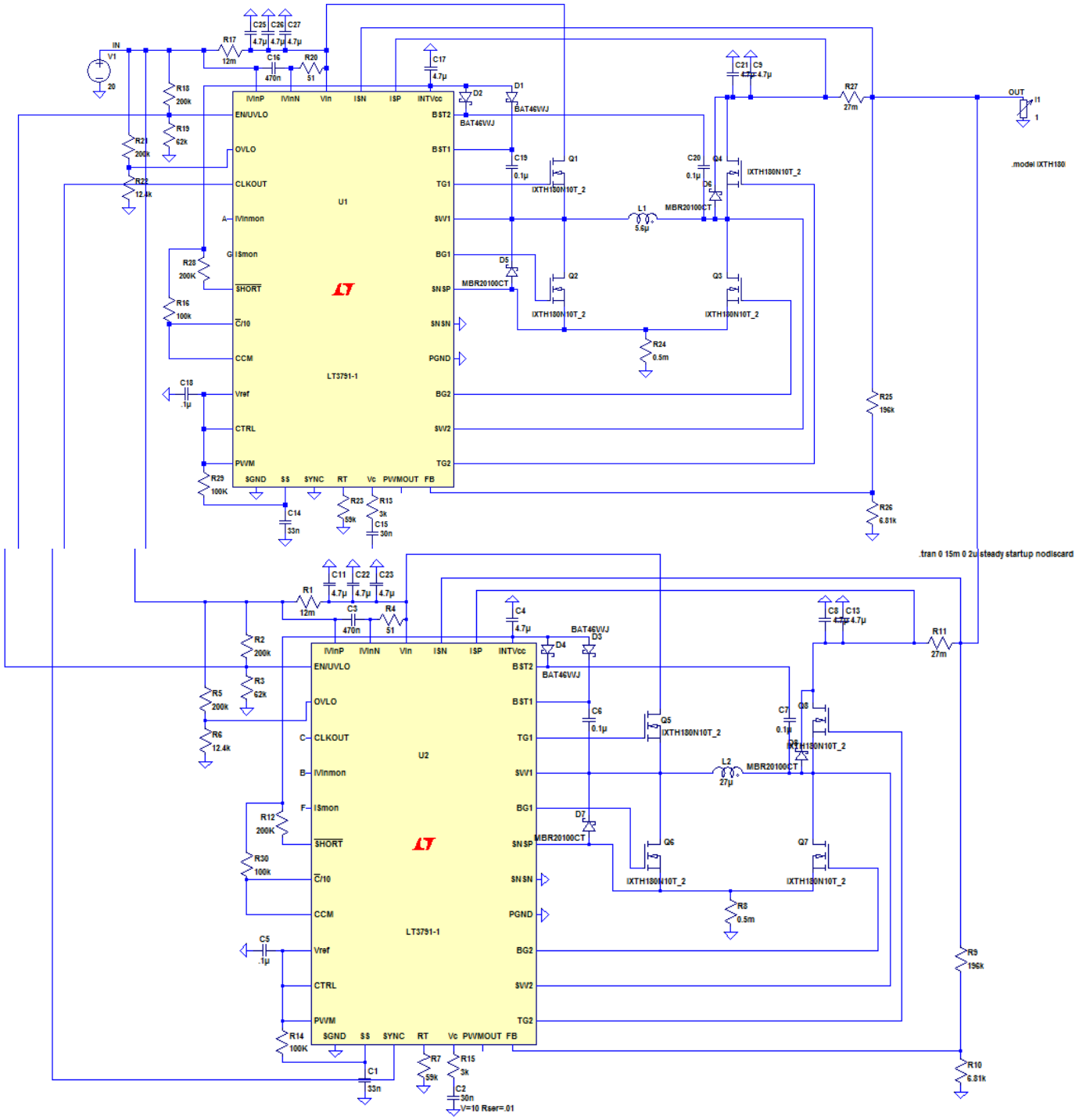


FIGURE 27
EXAMPLE LT3791-1 CIRCUIT DESIGN

From Figure 27, one of the CLKOUT pins, IVINmon, and ISmon pins have connections to 1GΩ resistors for simulation purposes only. These pins have no connection and were left open for the final project. Comparing Figure 27 and Figure 11, the different component values stem from that David's and Sheldon's design calculated using a 400kHz system, a 22µH, and exact 36V output through the feedback resistors. Thus, most of the resistors and capacitors used in Figure 11 do not apply for this revised design.

However, the overall goal for this project remains the same, where we require a 36V output from the DC-DC converter and at most 8A output. This design uses a 7.5A output limit, a 4.1667A input limit, and a 0.5mΩ sense resistor. The MOSFETs remain the same as in Figure 11. The Schottky diodes were switched with a different set of diodes than the previous design, though both the previous and revised diodes can work appropriately for the revised design.

Though not shown in Figure 27, optional capacitors can be placed at the FB pin to ensure the pin doesn't receive any noisy signals, which could otherwise cause the IC to shut off unintentionally when the DC-DC converter correctly outputs 36V.

### 9.3 Revised Component List

Table XIX shows the revised component list, provided by Chu's and Yoo's Senior Project Design [14]. This table doesn't include the cost of the PCBs, wire connections (i.e. banana-to-banana connections for connecting the ground layers between two PCBs), and test point lead

| Type | Component | Value | Component | $/unit | QTY | Sum | P/N | Description | Company |
|---|---|---|---|---|---|---|---|---|---|
| Inductor | Power Inductor | 39u | Inductor | $6.08 | 2 | $12.16 | AIRD-03-270K | INDUCTOR PWR DRUM CORE 27UH | Abracon |
| Resistors | In-Curr Sense Res | 12m | R1 | $1.17 | 2 | $2.34 | ERJ-8BWFR012V | RES 0.012 OHM 1W 1% 1206 SMD | Panasonic |
| | EN/UVLO | 200k | R2 | $0.10 | 2 | $0.20 | RC2012F204CS | RES 200K OHM 1/8W 1% 0805 | Samsung |
| | EN/UVLE | 62k | R3 | $0.10 | 2 | $0.20 | ERJ-6ENF6202V | RES 62K OHM 1/8W 1% 0805 SMD | Panasonic |
| | Compensation | 51 | R4 | $0.89 | 2 | $1.78 | CRCW080551R0FKEA | RES 51.0 OHM 1/8W 1% 0805 SMD | Vishay Dale |
| | OVLO | 200k | R5 | $0.10 | 2 | $0.20 | ERJ-6ENF2003V | RES 200K OHM 1/8W 1% 0805 SMD | Panasonic |
| | OVLO | 12.4k | R6 | $0.10 | 2 | $0.20 | ERJ-6ENF1242V | RES 12.4K OHM 1/8W 1% 0805 SMD | Panasonic |
| | RT | 59k | R7 | $0.10 | 2 | $0.20 | ERJ-6ENF5902V | RES 59K OHM 1/8W 1% 0805 SMD | Panasonic |
| | Rsense | 1.5m | R8 | $1.11 | 2 | $2.22 | ERJ-M1WTF1M5U | RES 0.0015 OHM 1W 1% 2512 SMD | Panasonic |
| | FB1 | 196k | R9 | $0.10 | 2 | $0.20 | ERJ-6ENF1963V | RES 196K OHM 1/8W 1% 0805 SMD | Panasonic |
| | FB2 | 6.98k | R10 | $0.10 | 2 | $0.20 | ERJ-6ENF1202V | RES 12K OHM 1/8W 1% 0805 SMD | Panasonic |
| | ROUT | 27m | R11 | $1.25 | 2 | $2.50 | WSL2512R0270FEA18 | RES .027 OHM 2W 1% 2512 SMD | Vishay Dale |
| | RSHORT | 200k | R12 | $0.10 | 2 | $0.20 | ERJ-6ENF2003V | RES 200K OHM 1/8W 1% 0805 SMD | Panasonic |
| | C/10 | 100k | R13 | $0.10 | 2 | $0.20 | ERJ-6ENF1003V | RES 100K OHM 1/8W 1% 0805 SMD | Panasonic |
| | RSS | 100k | R14 | $0.10 | 2 | $0.20 | ERJ-6ENF1003V | RES 100K OHM 1/8W 1% 0805 SMD | Panasonic |
| | RVC | 3k | R15 | $0.10 | 2 | $0.20 | ERJ-6ENF3001V | RES 3K OHM 1/8W 1% 0805 SMD | Panasonic |
| Switches | | | Q1-Q8 | $1.06 | 8 | $8.48 | IPP230N06L3 G | MOSFET N-CH 60V 30A TO220-3 | Infineon |
| Capacitors | CSS | 33nF | C1 | $0.24 | 2 | $0.48 | C0603C333K8RACTU | CAP CER 0.033UF 10V 10% X7R 0603 | Kemet |
| | VC | 33nF | C2 | $0.24 | 2 | $0.48 | C0603C333K8RACTU | CAP CER 0.033UF 10V 10% X7R 0603 | Kemet |
| | IN | 470n | C3 | $0.12 | 2 | $0.24 | C1005X5R1A474K050BB | CAP CER 0.47UF 10V 10% X5R 0402 | TDK |
| | INTVCC | 4.7u | C4 | $1.40 | 2 | $2.80 | C3225X7S2A475M200AB | CAP CER 4.7UF 100V 20% X7S 1210 | TDK |
| | VREF | 0.1uF | C5 | $0.10 | 2 | $0.20 | C1608X7R1E104K080AA | CAP CER 0.1UF 25V 10% X7R 0603 | TDK |
| | BST | 0.1uF | C6 and C7 | $0.10 | 4 | $0.40 | C1608X7R1E104K080AA | CAP CER 0.1UF 25V 10% X7R 0603 | TDK |
| | COUT | 4.7u | C8 | $0.48 | 4 | $1.92 | CL32B475KBUYNNE | CAP CER 4.7UF 50V 10% X7R 1210 | Samsung |
| | Cap_IN | 4.7u | C11 | $0.45 | 2 | $0.90 | CGA6M3X7S2A475K200AB | CAP CER 4.7UF 100V 10% X7S 1210 | TDK |
| Schottky | | | D1-D4 | $0.44 | 4 | $1.76 | BAT46WJ,115 | DIODE SCHOTKY 100V 0.25A SOD323F | NXP Semicond. |
| Controller | LT3791-1 | | Controller | $11.21 | 2 | $22.42 | LT3791IFE-1#PBF | IC REG CTRLR BUCK BST 38TSSOP | Linear Tech |
| | | | | | TOTAL | $63.28 | | | |

TABLE XIX
REVISED COMPONENT LIST

### 9.4 Revised Simulations

Due to different components used for their design, David's and Sheldon's simulations contain different results than my simulations. For example, their simulations show that the LT3791-1 can

handle 40V or more input voltage and output the desired 36V at efficiencies higher than 90%, as opposed to my simulations which outputs 37V at 90%. Also, their simulations show that their IC can operate for input voltages 20V or higher at 90% efficiency. Figure 28 shows the power efficiencies for varying $V_{IN}$ from Sheldon's and David's simulations.

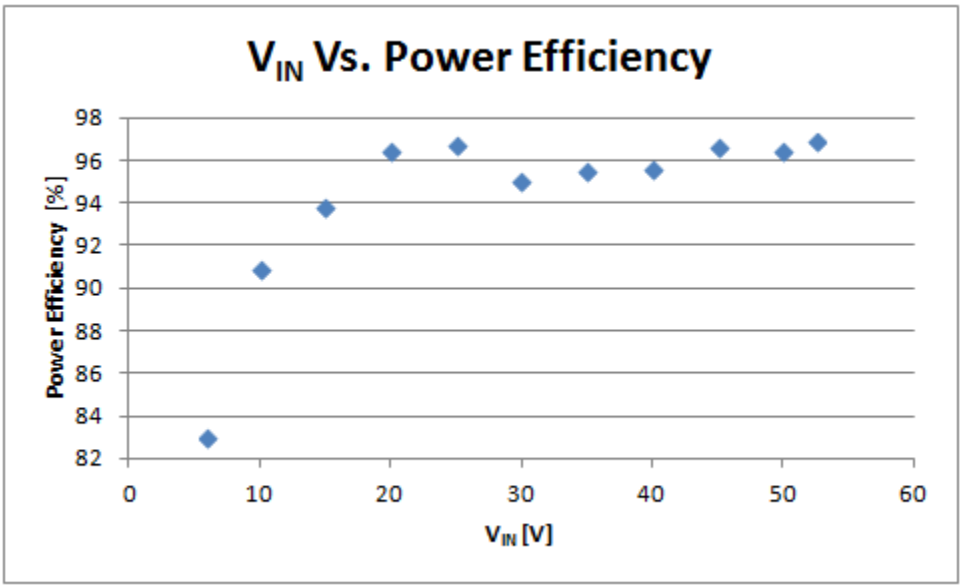


FIGURE 28
LT3791-1'S SIMULATED POWER EFFICIENCY VS. INCREASING VIN [14]

To simulate the revised design, we used several test cases based around changing input voltage, type of output load, power efficiency, etc. The revised simulations used the following test cases in Table XX.

TABLE XX
TEST CASE FOR REVISED DESIGN

| Test Case # | $V_{IN}$ (V) | $I_{IN}$ (A) | $P_{IN}$ (W) | Efficiency (%) | $P_{OUT}$ (W) | $I_{OUT}$ (A) | Output Resistance (Ω) |
|---|---|---|---|---|---|---|---|
| 1 | 6 | 0.6 | 3.6 | 90 | 3.24 | 0.09 | 400 |
| 2 | 7 | 0.7 | 4.9 | 90 | 4.41 | 0.1225 | 293.88 |
| 3 | 10 | 1 | 10 | 90 | 9 | 0.25 | 144 |
| 4 | 20 | 2 | 40 | 90 | 36 | 1 | 36 |
| 5 | 30 | 3 | 90 | 90 | 81 | 2.25 | 16 |
| 6 | 40 | 4 | 160 | 90 | 144 | 4 | 9 |
| 7 | 50 | 5 | 250 | 90 | 225 | 6.25 | 5.76 |

The test cases from Table XX determine whether the revised design can actually handle the specified voltage inputs and can also output the desired 36V and output currents. We calculated the $I_{IN}$ values based on the elliptical's 10Ω output resistance, the power efficiency by assuming the system can achieve 90% as described in the LT3791-1's datasheet, and the output current based on power efficiency ($P_{OUT}/P_{IN}$) and assuming 36V output.

Test case #1 involves determining whether the revised design can actually output 36V when the DC-DC converter receives a 6V input, the lowest input value determined by UVLO. Figure 29 shows the simulation results for test case #1, where the 6V input cannot allow the DC-DC converter to output 36V as desired.

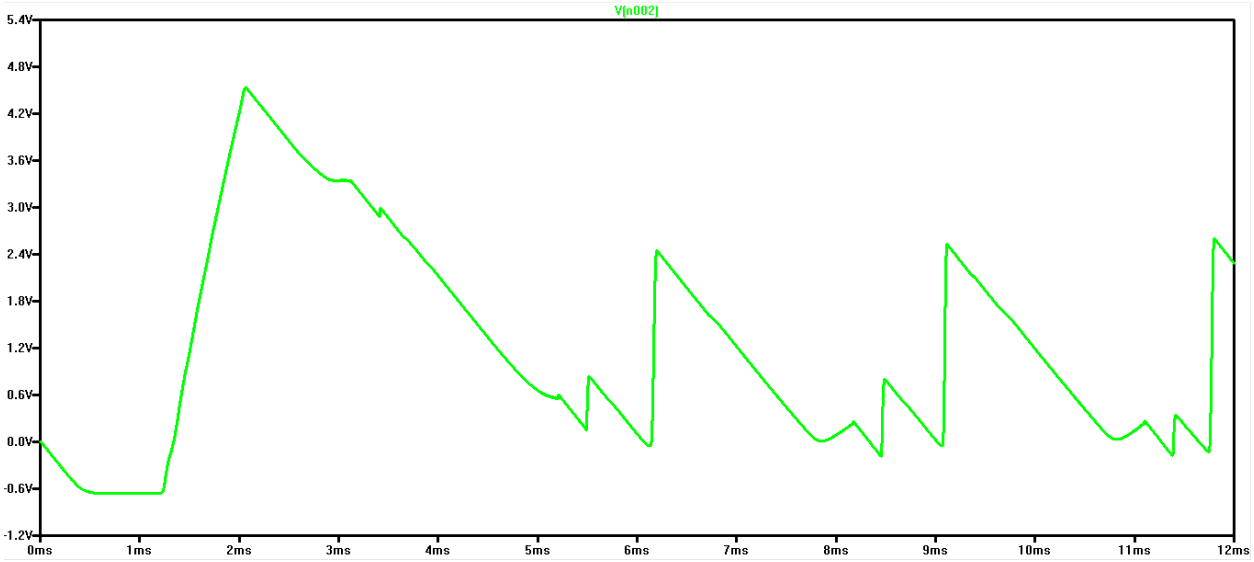


FIGURE 29
TEST CASE #1 FOR REVISED DESIGN {$V_{OUT}$ (GREEN)}

Test case #2 involves determining the minimum input voltage needed to output 36V, where we ran several simulations in order to determine the 7V input voltage. Figure 30 shows the simulation results, where the desired output voltage outputs 36V. However, the input current peaks at 8A when $V_{OUT}$ increases from 8V to 36V. This discrepancy stems from that the input voltage source assumes infinite input current, so a realistic simulation needs some parasitic resistance in series with the source in order to lower the input current below 5A as described by the ellitipcal's output performance.

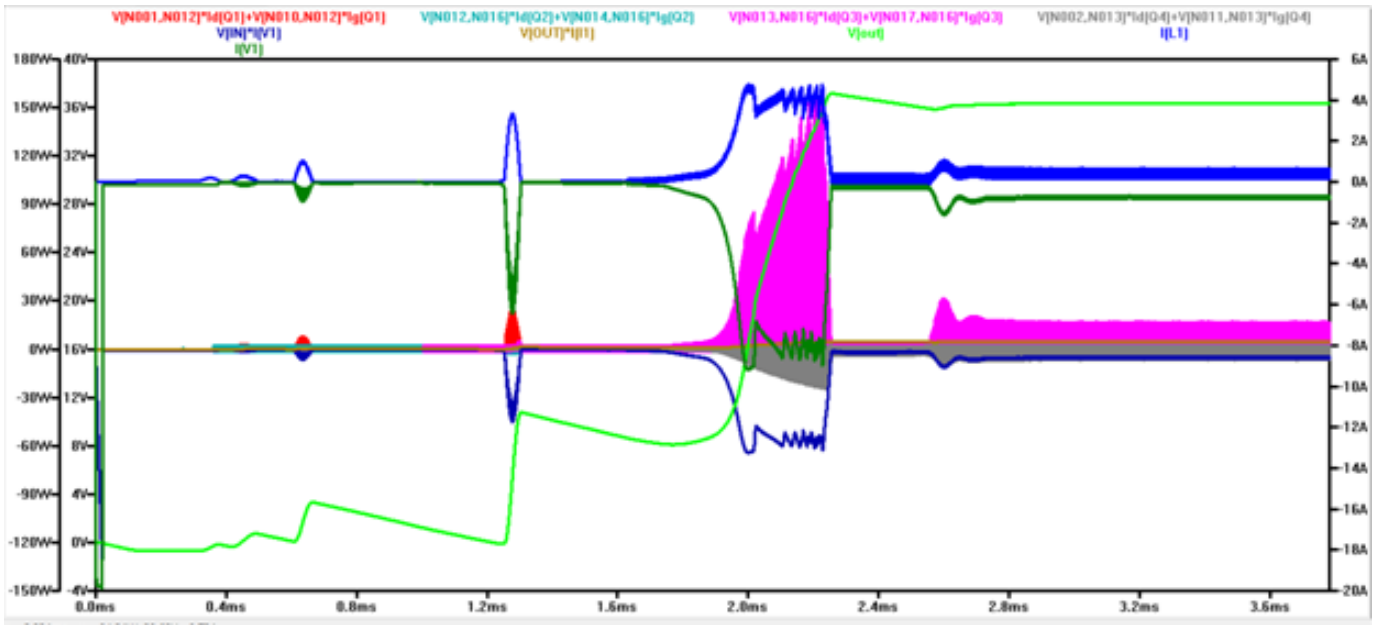


FIGURE 30

TEST CASE #2 FOR REVISED DESIGN {Q1 POWER (RED), Q2 POWER (TEAL), Q3 POWER (PINK), Q4 POWER (GREY), $V_{OUT}$ (GREEN), $I_{IN}$ (DARK GREEN), INDUCTOR CURRENT $I_L$ (BLUE), $P_{IN}$ (DARK BLUE), $P_{OUT}$ (BROWN)}

Test cases #3 and #4 both experience similar simulations results; both #3 and #4 can output 36V if one adds in parasitic resistances to the sources, but the input current does goes a bit over the 5A maximum input current. So perhaps more tweaking to the parasitic resistance can result in the desired output voltage and input current. However, the fact that the sources need more current than what the test cases imply (i.e. a 10V input case simulation needs 5A input instead of the expected 1A input) suggests that the revised design cannot accomplish these test cases for various reasons (i.e. the revised designs demand more power than expected). Figures 31 and 32 show the simulation results.

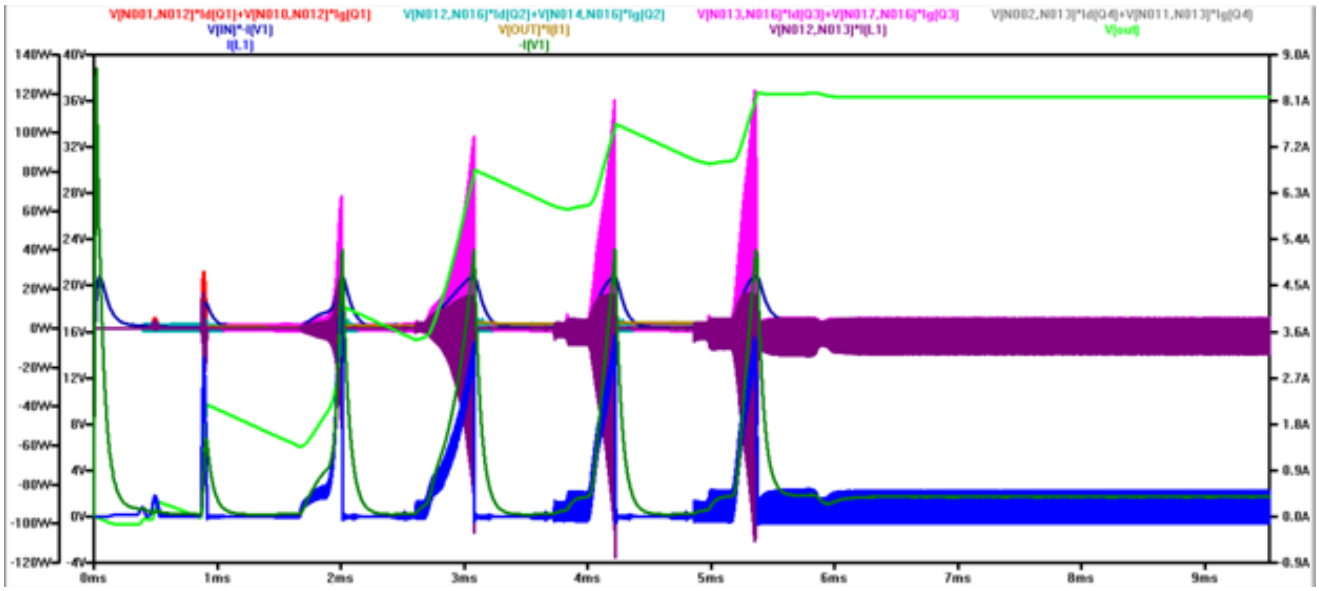


FIGURE 31

TEST CASE #3 FOR REVISED DESIGN {Q1 POWER (RED), Q2 POWER (TEAL), Q3 POWER (PINK), Q4 POWER (GREY), $V_{OUT}$ (GREEN), $I_{IN}$ (DARK GREEN), INDUCTOR CURRENT $I_L$ (BLUE), $P_{IN}$ (DARK BLUE), $P_{OUT}$ (BROWN), INDUCTOR POWER $P_L$ (PURPLE)}

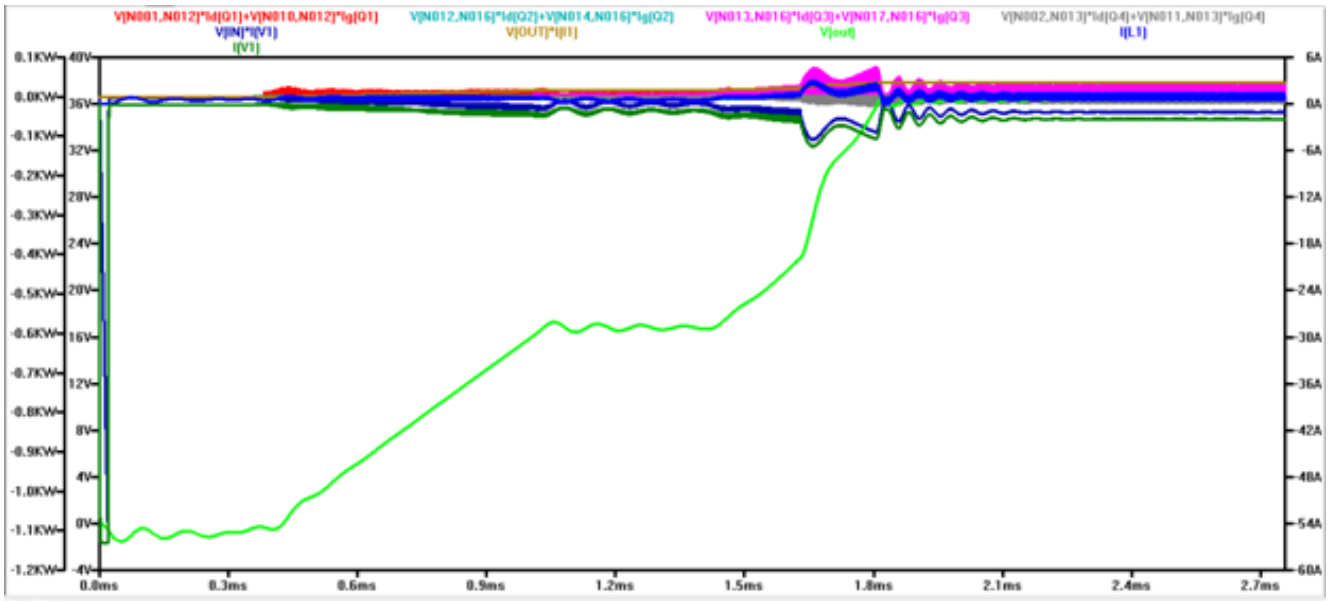


FIGURE 32

TEST CASE #4 FOR REVISED DESIGN {Q1 POWER (RED), Q2 POWER (TEAL), Q3 POWER (PINK), Q4 POWER (GREY), $V_{OUT}$ (GREEN), $I_{IN}$ (DARK GREEN), INDUCTOR CURRENT $I_L$ (BLUE), $P_{IN}$ (DARK BLUE), $P_{OUT}$ (BROWN)}

In Figure 31, the input current peaks at 5.4A, which exceeds the intended 5A input limit. Figure 32 also shows similar results, where the input current peaks at 5.8A. These input current spikes, however, only occur when the DC-DC converter charges the inductor with more energy in order for the DC-DC converter to output 36V (or when $V_{OUT}$ rises from some smaller value voltage up to 36V). So, charging the inductor might require more current than the elliptical can provide, or the charging time might take longer than a few milliseconds in order to compensate the simulated high input current spikes.

Test case #5 also shows the current spike, and Figure 33 shows the simulation result.

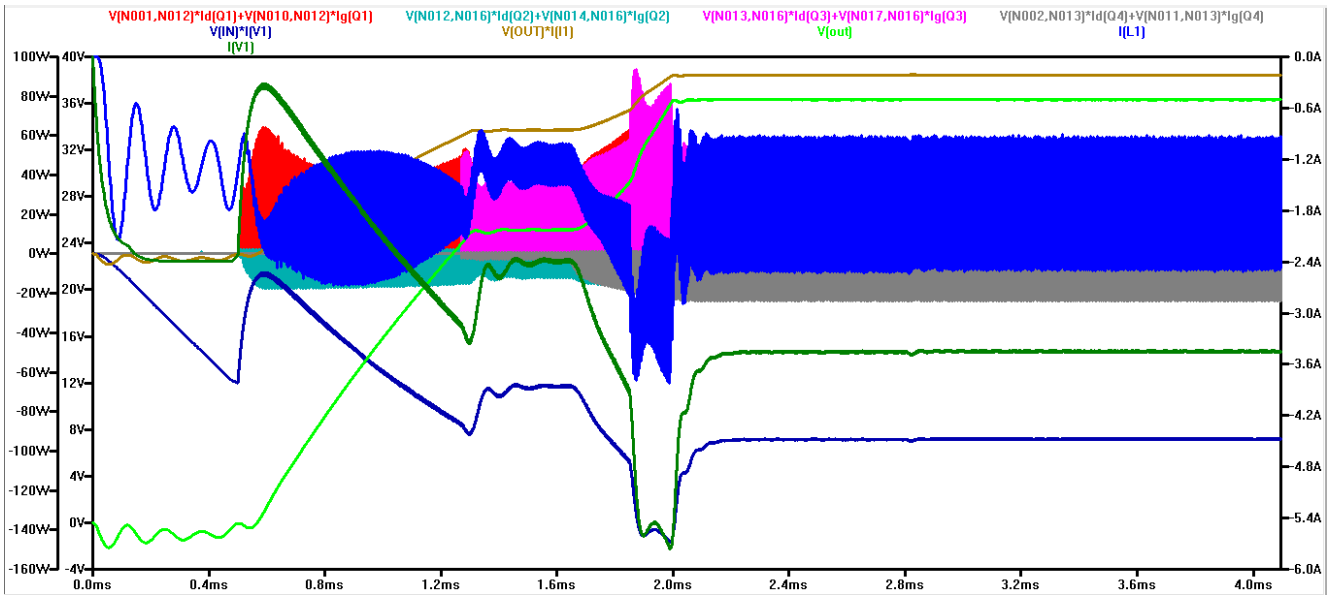


FIGURE 33

TEST CASE #5 FOR REVISED DESIGN {Q1 POWER (RED), Q2 POWER (TEAL), Q3 POWER (PINK), Q4 POWER (GREY), $V_{OUT}$ (GREEN), $I_{IN}$ (DARK GREEN), INDUCTOR CURRENT $I_L$ (BLUE), $P_{IN}$ (DARK BLUE), $P_{OUT}$ (BROWN)}

Test case #6 shows the input current still exceeding over the 5A input current. Figure 34 shows the simulation result for test case #6.

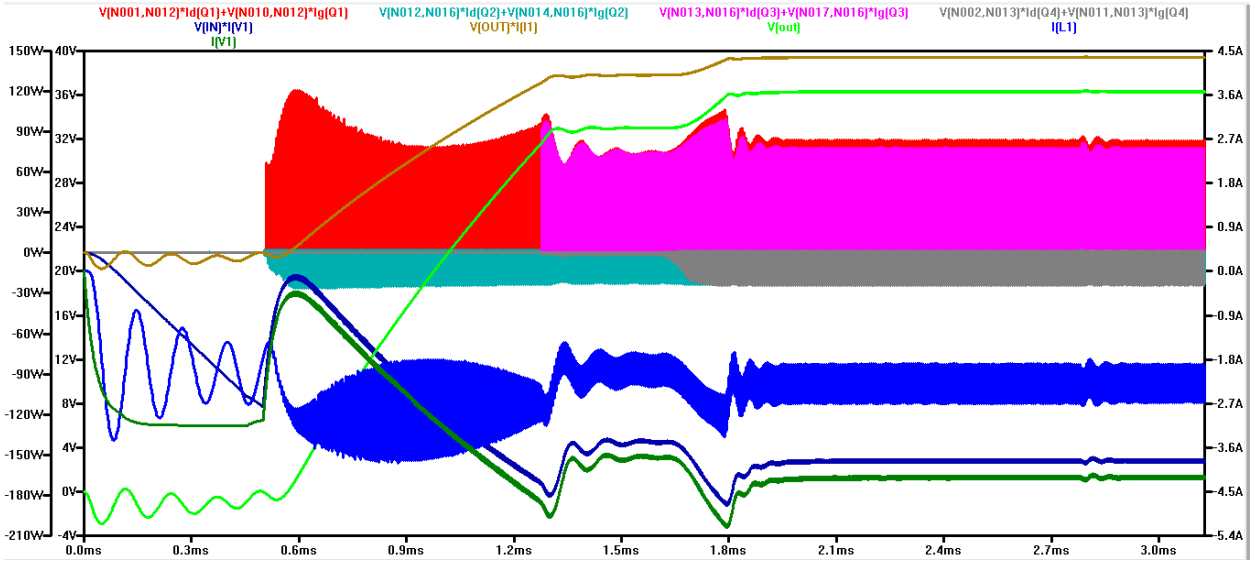


FIGURE 34

TEST CASE #6 FOR REVISED DESIGN {Q1 POWER (RED), Q2 POWER (TEAL), Q3 POWER (PINK), Q4 POWER (GREY), $V_{OUT}$ (GREEN), $I_{IN}$ (DARK GREEN), INDUCTOR CURRENT $I_L$ (BLUE), $P_{IN}$ (BROWN), $P_{OUT}$ (PURPLE)}

Test case #7 finally shows the input current not exceeding over 5A. Figure 35 shows the simulation results.

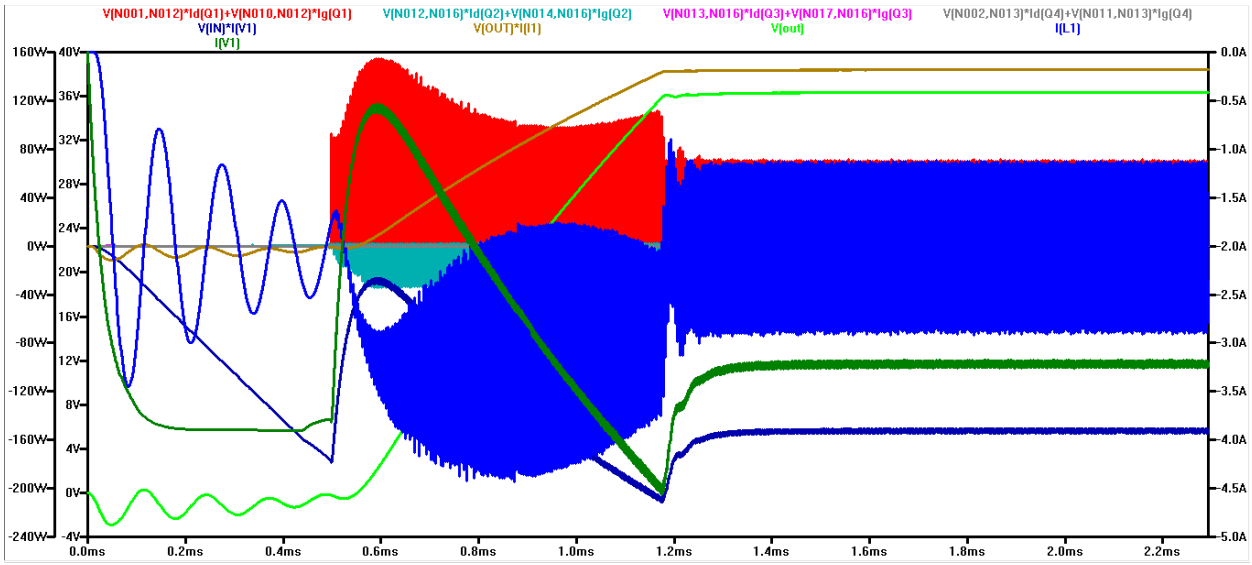


FIGURE 35

TEST CASE #7 FOR REVISED DESIGN {Q1 POWER (RED), Q2 POWER (TEAL), Q3 POWER (PINK), Q4 POWER (GREY), $V_{OUT}$ (GREEN), $I_{IN}$ (DARK GREEN), INDUCTOR CURRENT $I_L$ (BLUE), $P_{IN}$ (BROWN), $P_{OUT}$ (PURPLE), $I_{OUT}$ (DARK BROWN)}

Since most of the simulations had input currents exceeding 5A, these simulations either show us an inaccurate portrayal of our actual circuit or our circuit would need more current than expected. Also, we tried to emulate the expected input current in several ways, including putting in a parasitic resistance at the source or changing the input sensing resistor to different values. But, we had trouble figuring out how to emulate the input current the way we wanted because we couldn't know the exact parasitic resistance value without running several simulations to see how the input current responds, which would take more time than we had. Overall, the higher input voltages appear to behave as expected compared to the lower input voltages since the lower input voltages required much more input current than the higher input voltages.

Also of note, the power dissipation across all MOSFETs remains lower than 200W peaks as opposed to the pre-revised simulations which saw nearly 1kW peaks. Thus, this revised design

can possibly operate within our specifications as long as the power dissipations actually do remain lower than 200W. However, if we expect these 200W peaks to occur, we still need heatsinks and possibly a fan in order to lower the temperature on the PCBs.

### 9.5 Revised PCB Layout

The revised designs follow Sheldon's and David's previous designs, where they have their own inductor, resistors, capacitors, and diodes than what I've used. All three of us combined some design elements from our own designs to build the following PCB layouts. We continued to use the 4-layered boards, so as to allow more design freedom with overlapping connections and also have a dedicated ground layer.

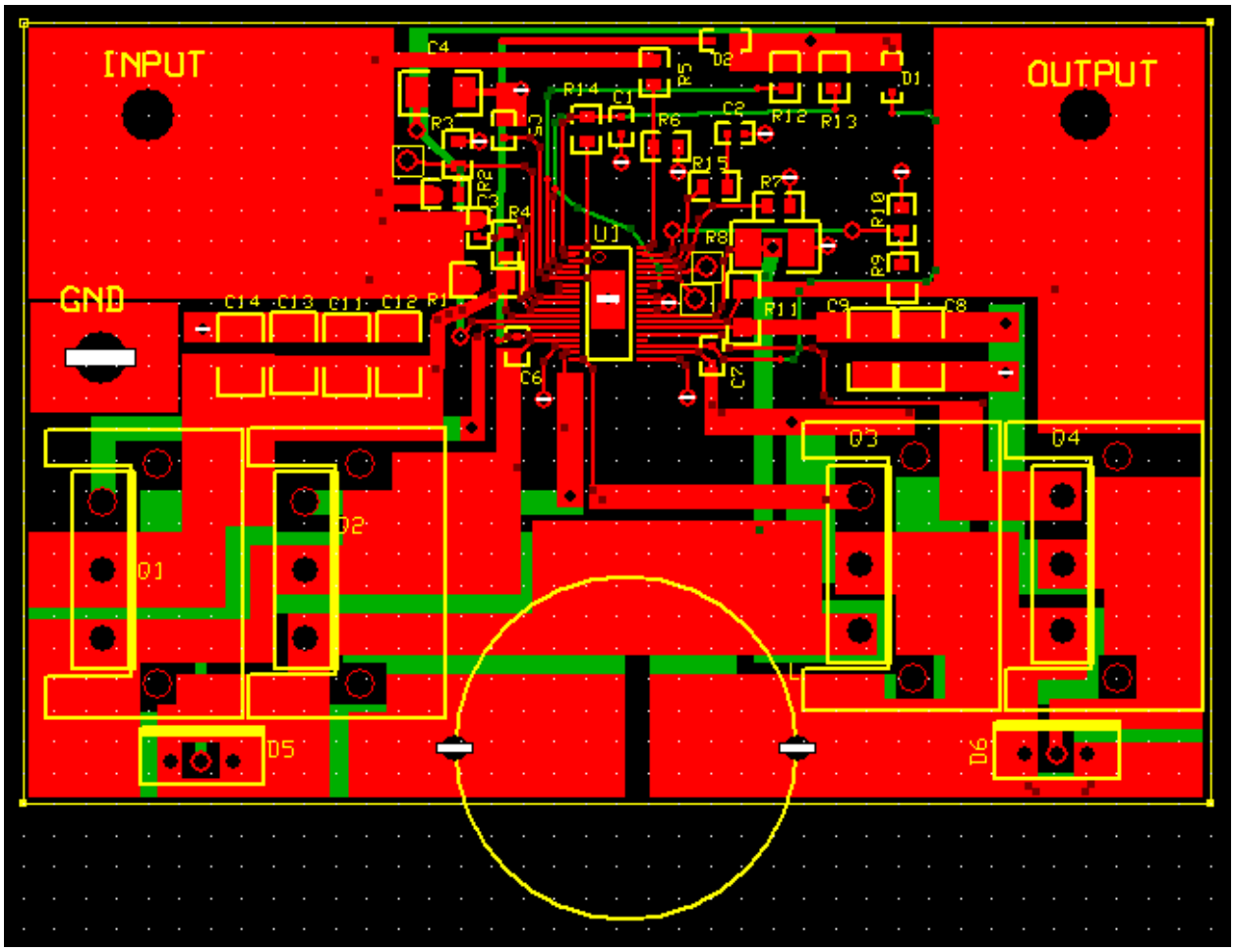


FIGURE 36
FIRST REVISED PCB LAYOUT - TOP LAYER

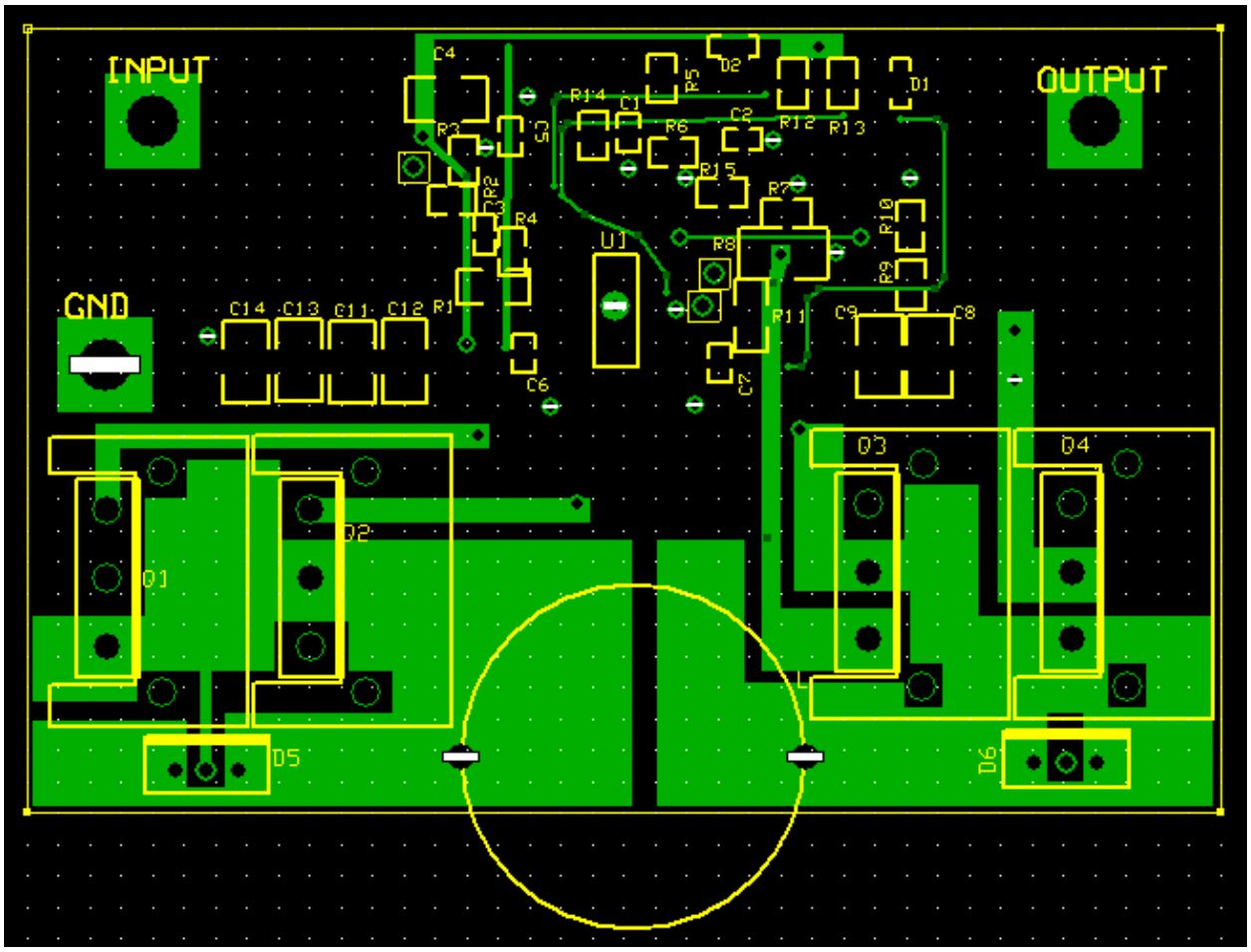


FIGURE 37
FIRST REVISED PCB LAYOUT - BOTTOM LAYER

Figure 36 shows the initial revised PCB layout, where we initially used a coiled, unshielded, through-hole 30µH inductor with a circular shape. This design has similar problems like the PCB layouts in Figures 25 and 26, where all PCBs lack several testing points needed to test the PCB's functionality. They also all have several traces overlap on the top and bottom layers, creating parasitic capacitances. The PCBs also need designated power and signal ground connections instead of one ground connection. The ground layer, sandwiched between the top and bottom

layer, does not have any trace yet since we want to first establish how the top and bottom layers should connect each other.

Before we considered adding the ground and test point connections, however, we first wanted to determine how to place the heatsinks away from each other and have the inductor not stick out of the board. As described before with the previous PCB layouts, the heatsinks should not stay close together or else the functionality of the heatsink to dissipate or reflow heat elsewhere remains redundant if the heatsinks stay in close proximity; the heat would flow from one heatsink to the next heatsink, thus the heatsinks do not dissipate the heat through the air efficiently. The inductor, though, should not stick out of the board because the exposed inductor could potentially touch some other metal object within the elliptical machine and cause shorts or shocks. Addressing these two issues, however, means leaving more room for these heatsinks and inductor and less space for other components, such as the $V_{IN}$ and $V_{OUT}$ traces. The second revised PCB layout addresses these two issues, as shown in Figures 38 and 39.

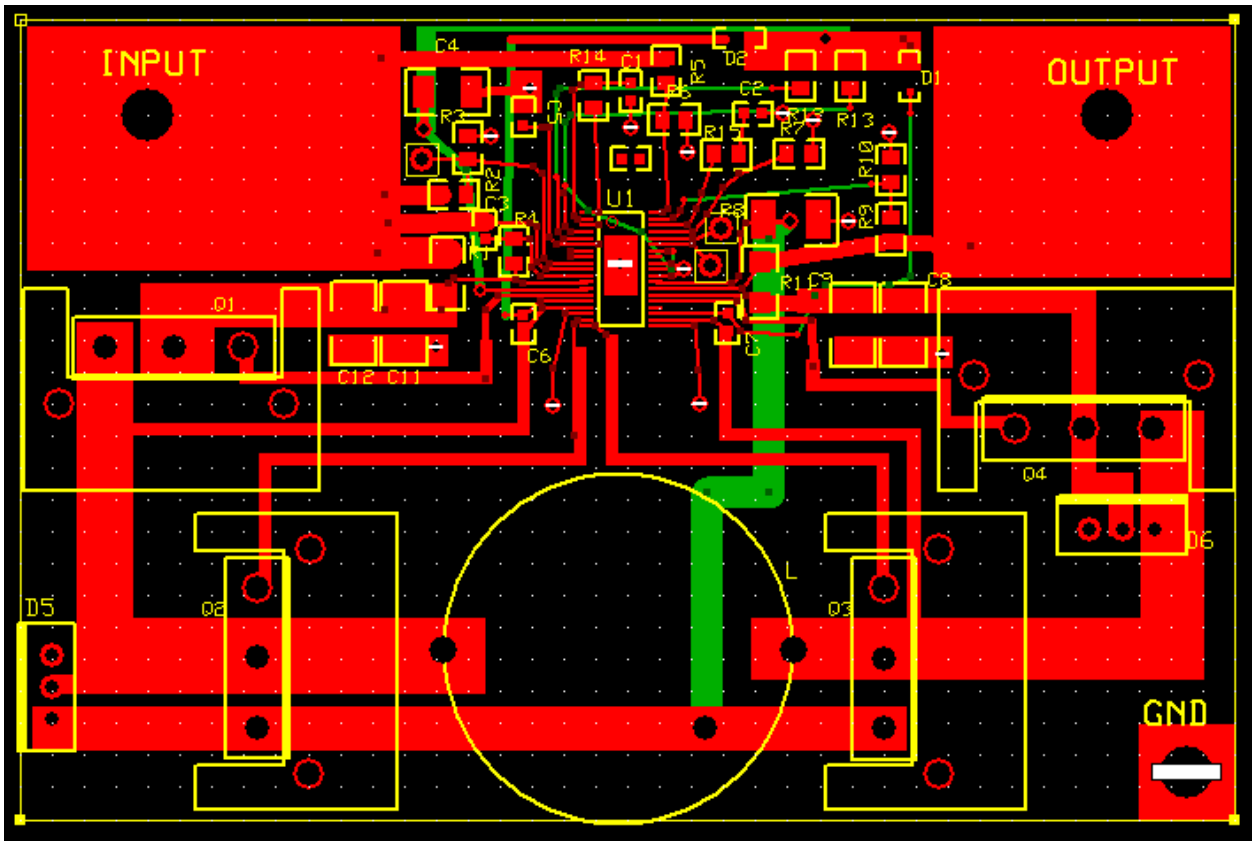


FIGURE 38
SECOND REVISED PCB LAYOUT - TOP LAYER

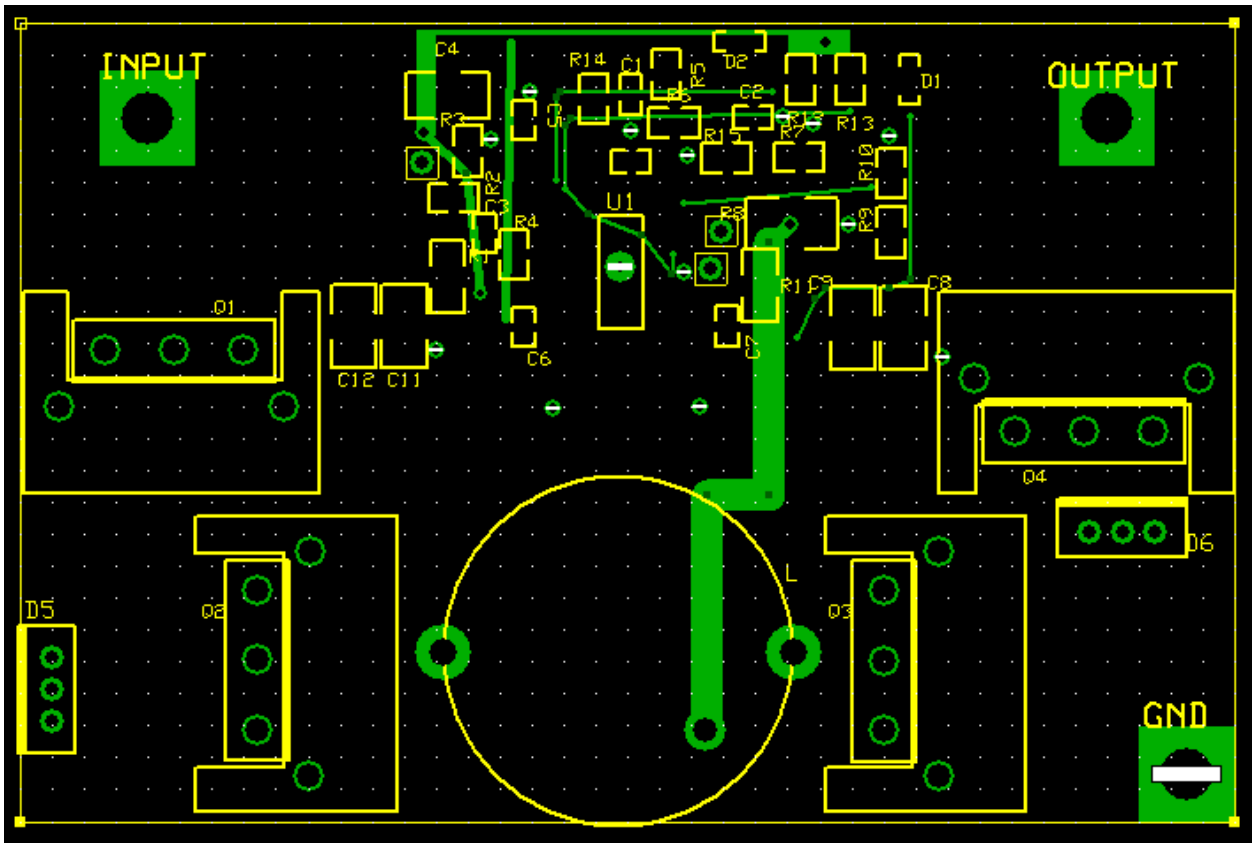


FIGURE 39
SECOND REVISED PCB LAYOUT - BOTTOM LAYER

In Figures 38 and 39, the heatsinks face different directions to allow heat and airflow to not interact with the other heatsinks as much as before, though Q1 (top left MOSFET) still has some heat directs toward Q2 (bottom left MOSFET). The inductor also does not stick out, but it does overlap traces as seen in Figure 38 where Q2 and Q3 connect together directly and the inductor hovers over the trace connection. Since this inductor remains unshielded, the inductor could interfere with the trace connection in unexpected ways, such as changing the amount of current through the trace. Thus, we changed this inductor into a SMT shielded inductor to ensure the inductor doesn't interfere with the traces and also allow more space on the board, as seen in the final revised PCB layout.

Finally, we considered adding more parallel capacitors at the input and output voltages to lower equivalent series resistance (ESR) across each capacitor. However, more capacitors means more space needed on the board. So, we decided to try place (or stack) capacitors on top of each other to save space. Figures 40 to 42 show the final revised PCB layouts for this project, with the added test points and ground connections.

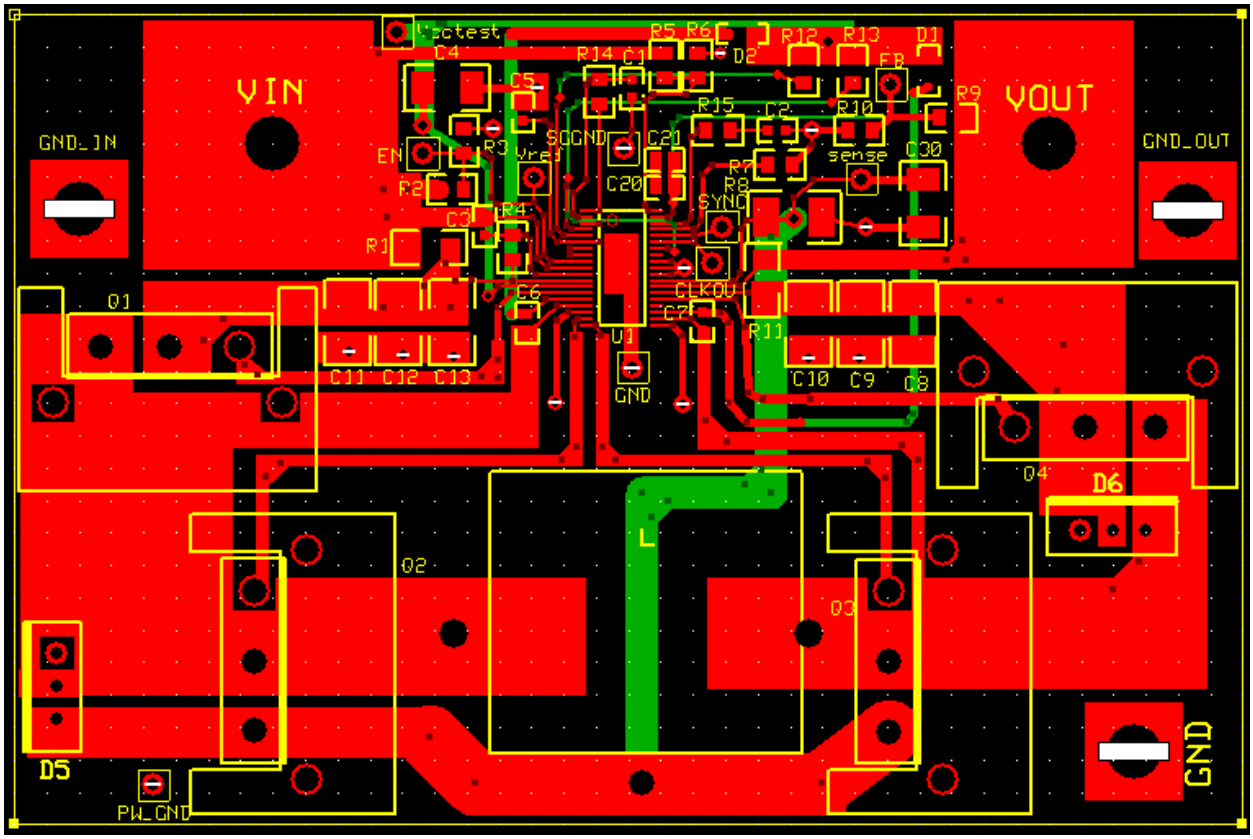


FIGURE 40
FINAL REVISED PCB LAYOUT - TOP LAYER

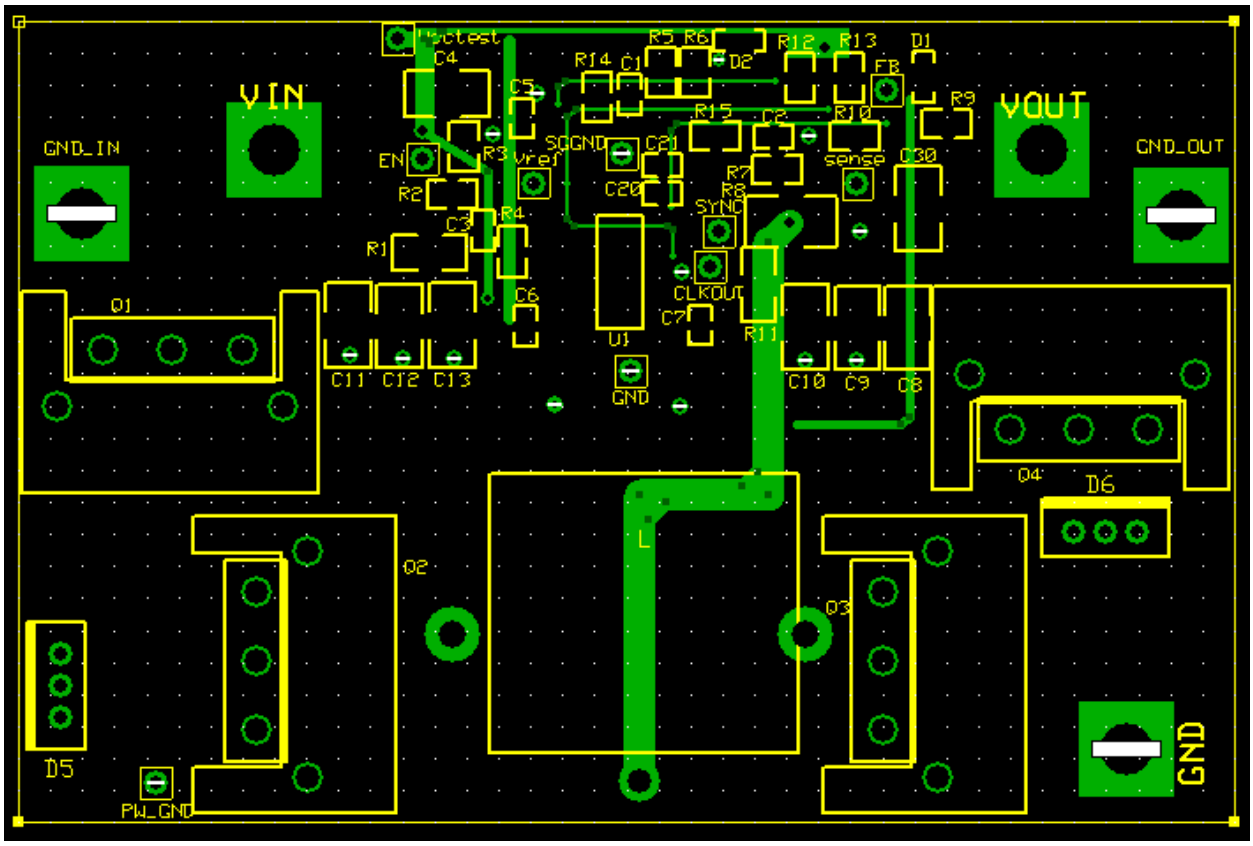


FIGURE 41
FINAL REVISED PCB LAYOUT - BOTTOM LAYER

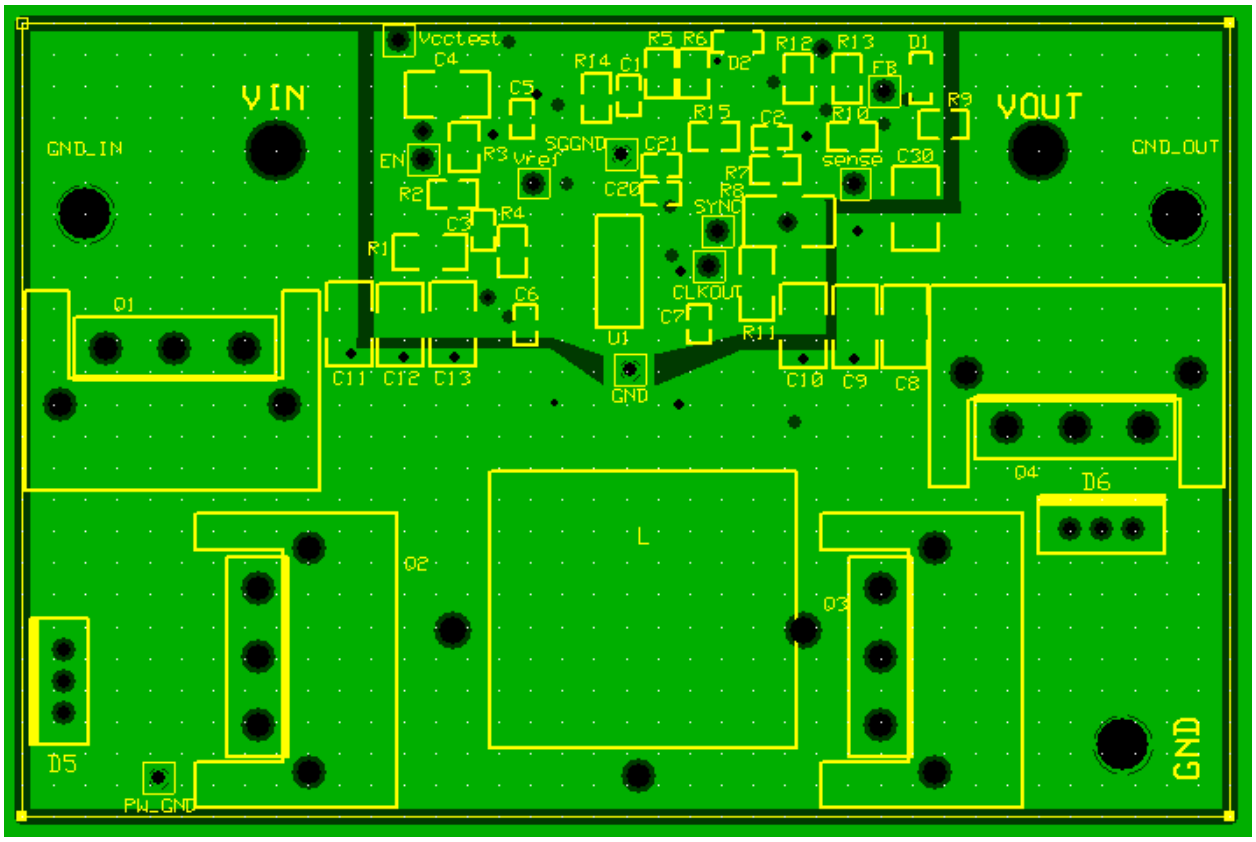


FIGURE 42
FINAL REVISED PCB LAYOUT - GROUND LAYER

We added the test points around the IC since these points have signal grounds. Thus, these testing points reside within the signal ground region as shown in Figure 42, within the top middle region; the traces included highlighted areas and the darker regions remain non-conductive areas. The ground connections include the signal ground below the IC, the power ground on the bottom left corner, the $V_{IN}$ ground on the left, and the $V_{OUT}$ ground on the right. With the inductor swap and rearrangement with the components (resistors, capacitors, and diodes) around the IC, we had enough room to place the testing points and ground connections. Also, we had to change the SGND under the IC (large pad under the middle of the IC) to move below the IC (compare Figures 38 and 40) because soldering the pad on top of the via would have been difficult.

We also added more traces at corners so as to prevent electromigration on the traces. Electromigration means electrons breaking apart metal ions due to large currents flowing through metal traces. These filled-corners (triangular-shaped) should prevent the traces from breaking apart when the DC-DC converter operates under high current, high voltage cases.

With the final PCB layout done, we continued on with ordering the parts and boards, then soldering the parts onto the manufactured boards. We then created a test plan to follow when testing the PCBs, shown in the next chapter.

# Chapter 10: Testing

## 10.1 Introduction

After soldering the components onto the PCBs, we next have to test the revised design to determine whether the design can operate as expected through the LTSpice simulations. We created another test case, similar to Table XX, so as to compare the simulations with the measured results.

## 10.2 Test Cases and Guidelines

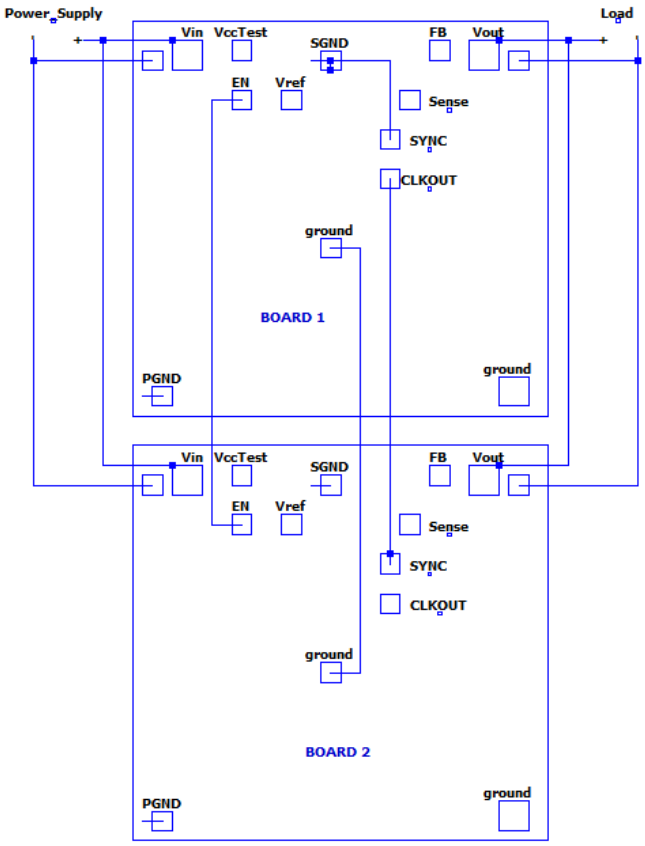


FIGURE 43
LT3791-1 TEST PLAN SCHEMATIC

TABLE XXI
TEST CASE FOR TESTING PROCEDURE

| Input Voltage [V] | Input Current [A] | Input Power [W] | Estimated Efficiency [%] | Output Voltage [V] | Output Current [A] |
|---|---|---|---|---|---|
| 6 | 0.6 | 3.6 | 90 | 36 | 0.09 |
| 10 | 1 | 10 | 90 | 36 | 0.25 |
| 20 | 2 | 40 | 90 | 36 | 1 |
| 30 | 3 | 90 | 90 | 36 | 2.5 |
| 40 | 4 | 160 | 90 | 36 | 4 |
| 50 | 5 | 250 | 90 | 36 | 6.25 |

Figure 43 and Table XXI show the test plan schematic and cases used to test the DC-DC converter. In Figure 43, the Board 1 represents the master board and the Board 2 represents the

slave board. The connections from one board to another represent jumper wires, while the connections to $V_{IN}$ and $V_{OUT}$ represent banana-to-spade connectors. The jumper wires should handle the small currents (less than 0.5A), while the banana-to-spade connectors handle the larger currents (more than 1A). We used the following guidelines and procedure:

1. Jumper wires connect:
    a. EN pins together
    b. Grounds in center of board (below each IC) together
    c. CLKOUT of master board to SYNC of slave board
    d. SYNC of master board to SGND of master board
2. Banana-to-spade connectors connect:
    a. Power supply to positive and negative terminals of VIN
    b. Electronic load to positive and negative terminals of VOUT

Procedure

1. Connect all analog signals together (follow 1. Jumper wires connect).
2. Turn on power supply and electronic load.
3. With power supply and electronic load outputs disabled, connect $V_{IN}$, $V_{OUT}$, and ground connections (follow 2. Banana-to-spade connectors connect).
4. Table XXI displays tests cases where input voltage and input current were set/limited by the power source and the electronic load was configured for corresponding output voltage/current.
5. Set input voltage and input current limits on the power source. Set corresponding test case output voltage and output current characteristics on the electronic load.
6. Enable the electronic load first, then enable the power source.
7. Record $V_{IN}$, $I_{IN}$, $V_{OUT}$, and $I_{OUT}$.
8. Turn off the power source first then the electronic load.
9. Alter power source and electronic load parameters based on provided test cases.
10. $P_{IN}$ vs. $P_{OUT}$ defines power efficiency for all test cases. $P_{IN}$ is calculated using $P_{IN} = V_{IN} * I_{IN}$. Output efficiency will be measured using $P_{OUT} = V_{OUT} * I_{OUT}$. Multi-meters may be used to measure $V_{OUT}$ and $I_{OUT}$ if the electronic load is not capable of direct readings.
11. Readings using multi-meters or oscilloscopes must be connected to proper grounds. Probes measuring analog signal ground to SGND. Probes measuring power signals ground to PGND.
12. A sample results table is shown in Table XXI. Input current, output voltage, and output current are measured, assuming a constant voltage source with limited output current.

Input Power and output power are calculating using P = V*I. Efficiency is calculated using $\eta = \frac{P_{OUT} - P_{IN}}{PIN}$.

TABLE XXII
SAMPLE TESTING RESULT

| Input Voltage [V] | Input Current [A] | Input Power [W] | Output Voltage [V] | Output Current [A] | Output Power[W] | Efficiency [%] |
|---|---|---|---|---|---|---|
| 6 | | | | | | |
| 10 | | | | | | |
| 20 | | | | | | |
| 30 | | | | | | |
| 40 | | | | | | |
| 50 | | | | | | |

After this setup, we tested the DC-DC converter by first using the 6V input case. Once enabling the electronic load and power supply, we noticed that the power supply provided an input current of 0.57A and input voltage of 5.7V and the load read a 0A output current and 10.91V output voltage. We also noticed the power supply remained in CC (constant current) and the load remained in CV (constant voltage). Since the power supply supplied less current and current than expected, we probed (from oscilloscope) the boards to determine whether the DC-DC converter operates correctly or not. Figures 44 to 51 show the probed results.

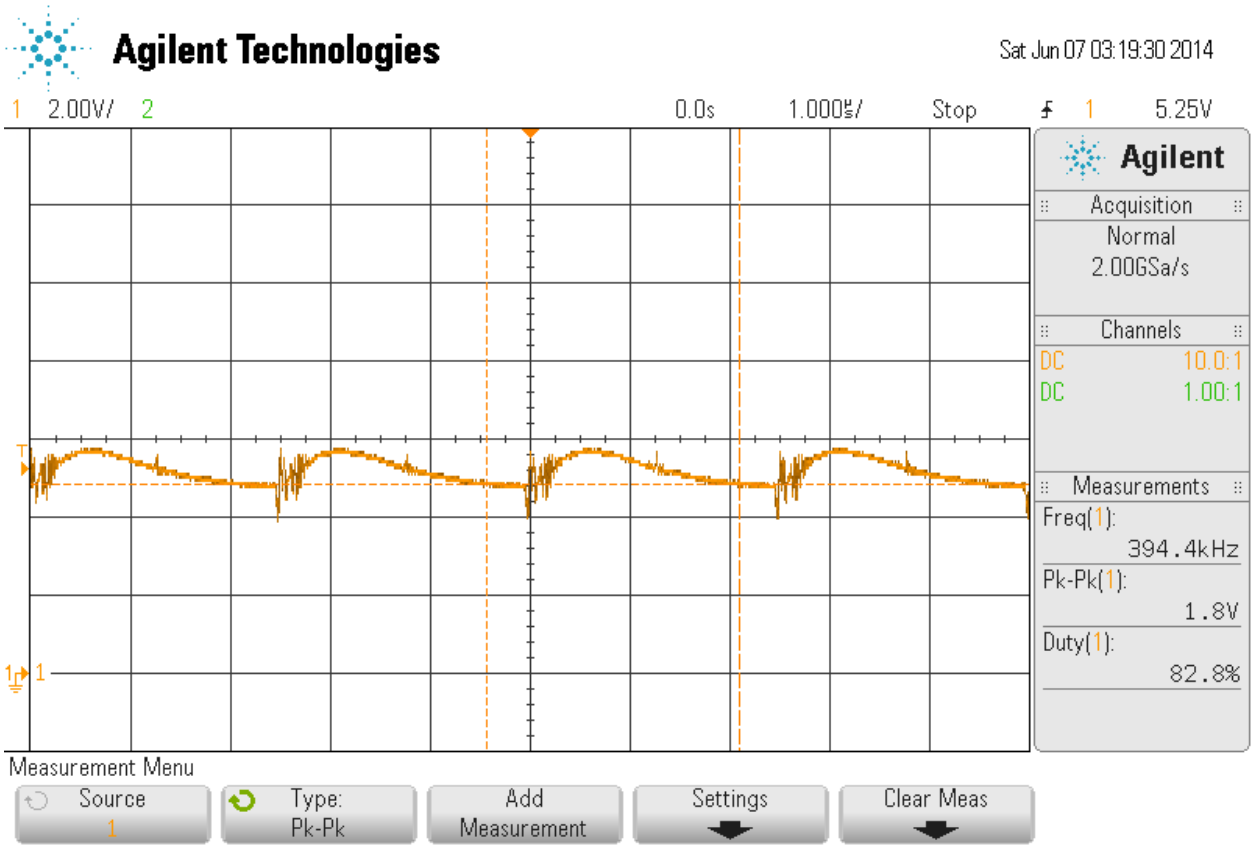


FIGURE 44
MASTER, Q1 GATE WAVEFORM, 6V INPUT CASE

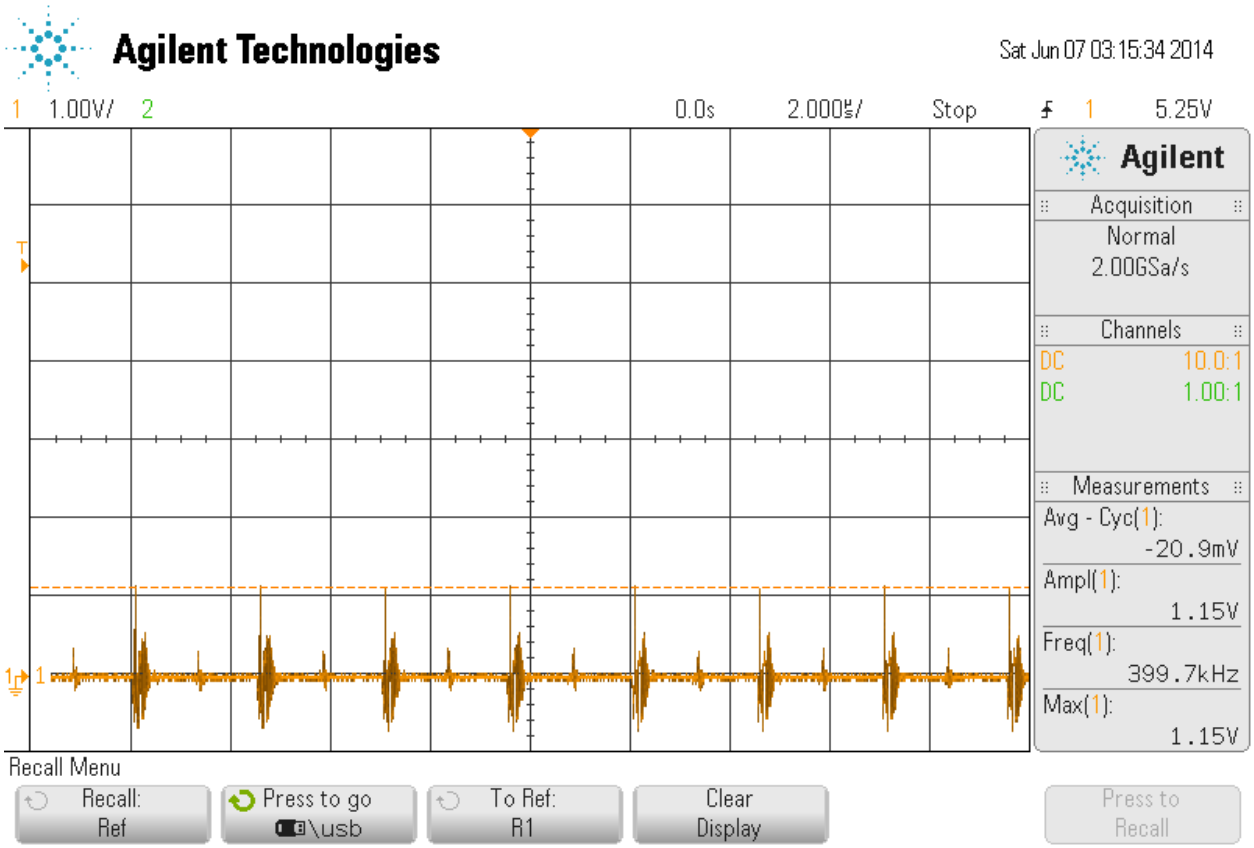


FIGURE 45
MASTER, Q2 GATE WAVEFORM, 6V INPUT CASE

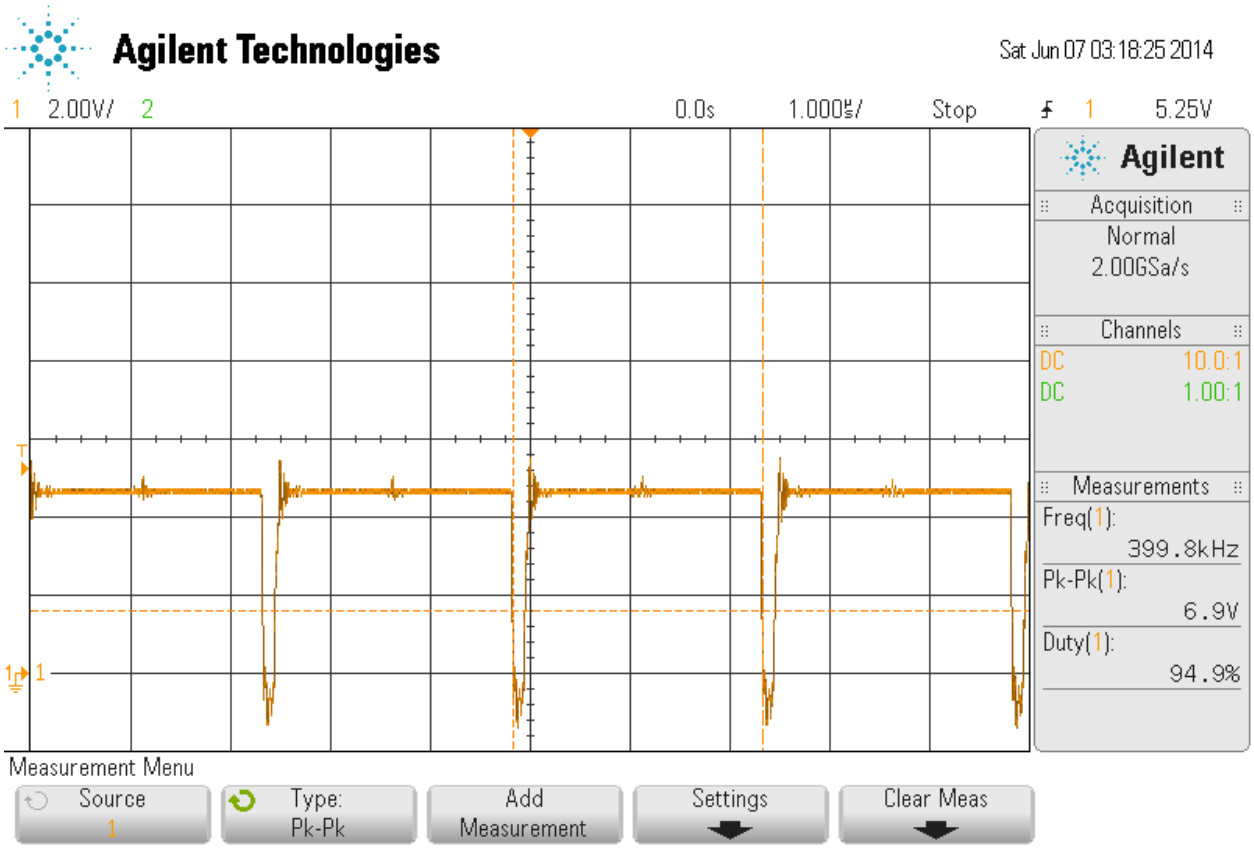


FIGURE 46
MASTER, Q3 GATE WAVEFORM, 6V INPUT CASE

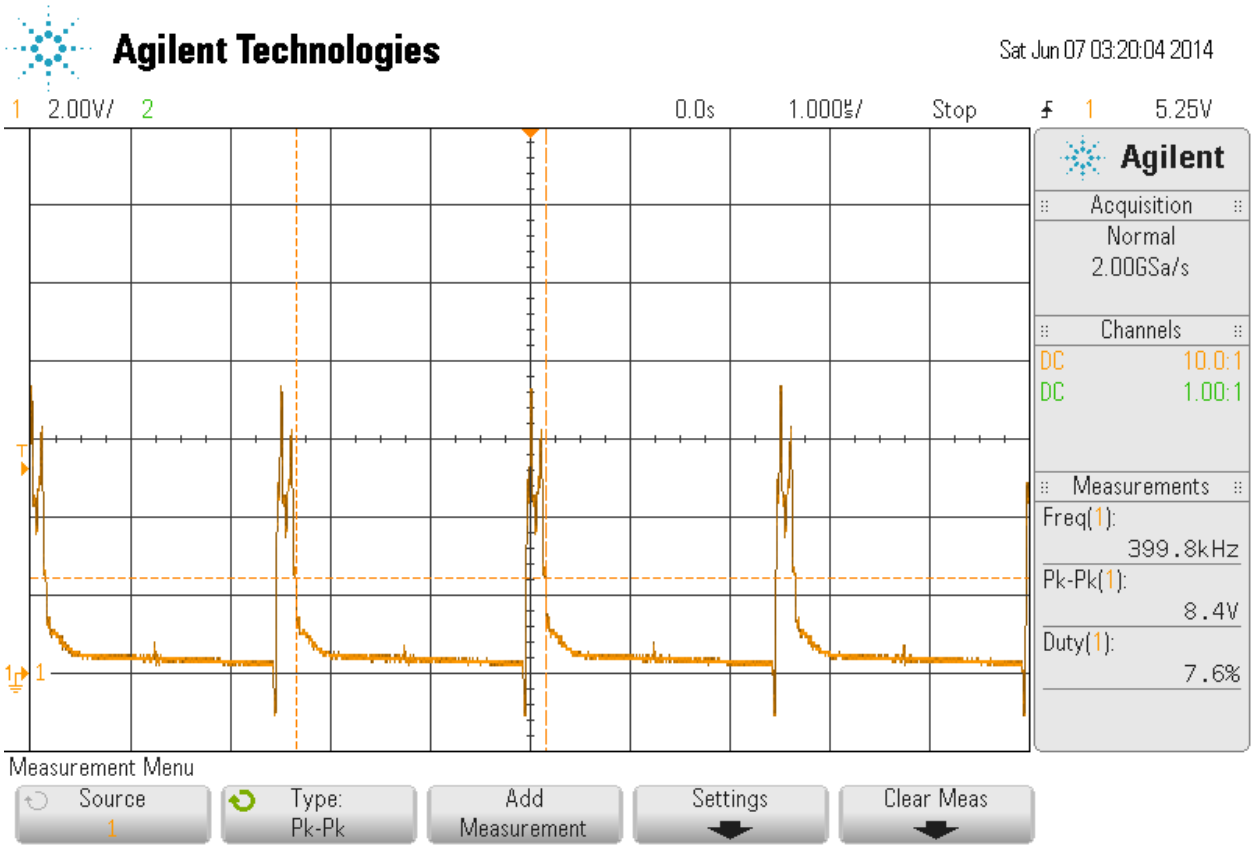


FIGURE 47
MASTER, Q4 GATE WAVEFORM, 6V INPUT CASE

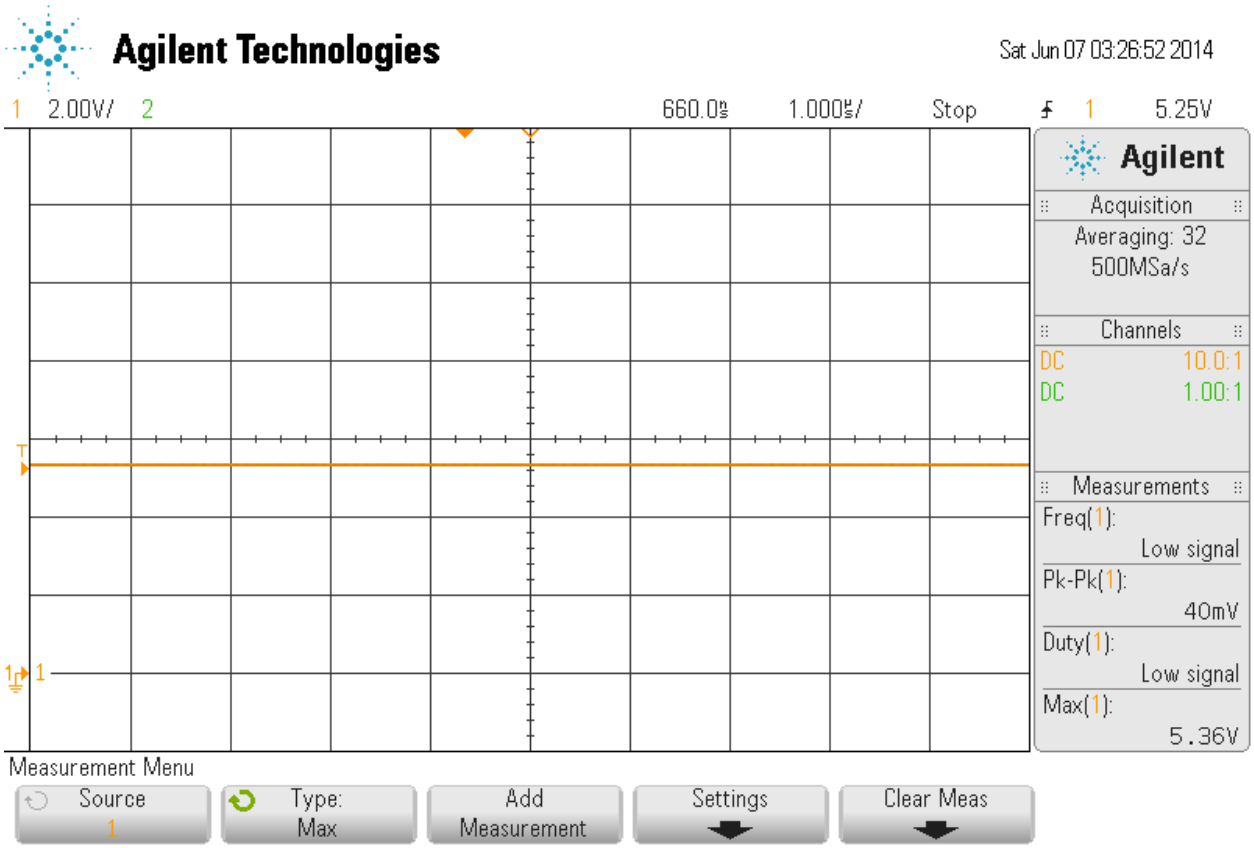


FIGURE 48
SLAVE, Q1 DRAIN WAVEFORM, 6V INPUT CASE

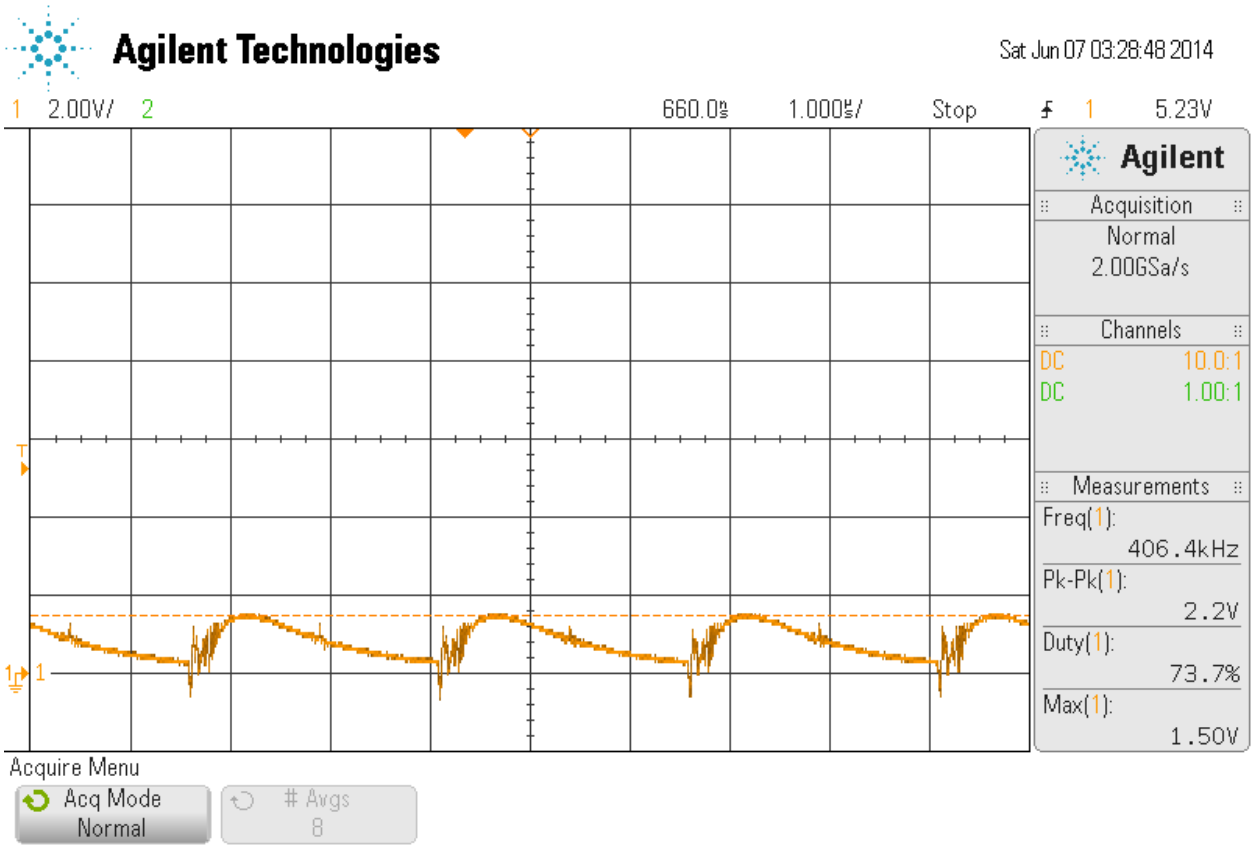


FIGURE 49
SLAVE, Q2 DRAIN WAVEFORM, 6V INPUT CASE

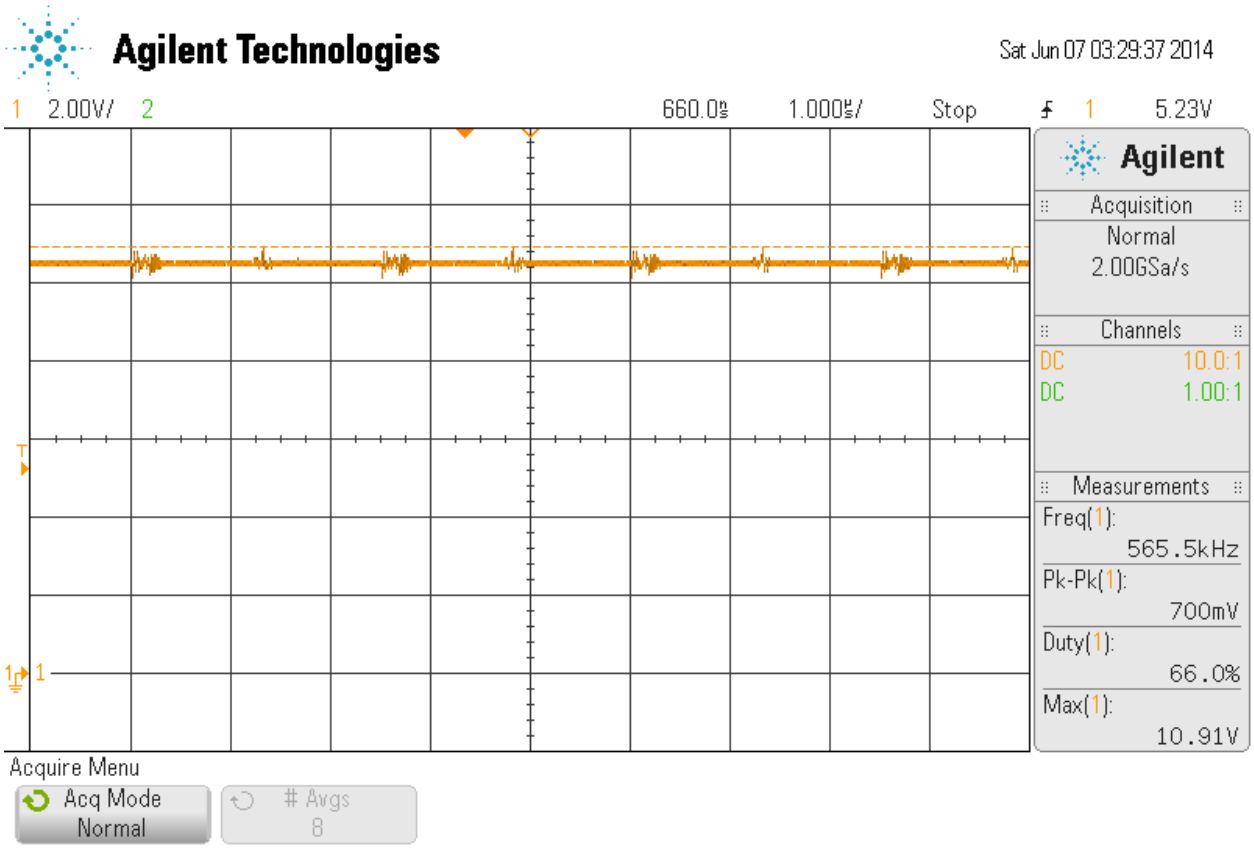


FIGURE 50
SLAVE, Q3 DRAIN WAVEFORM, 6V INPUT CASE

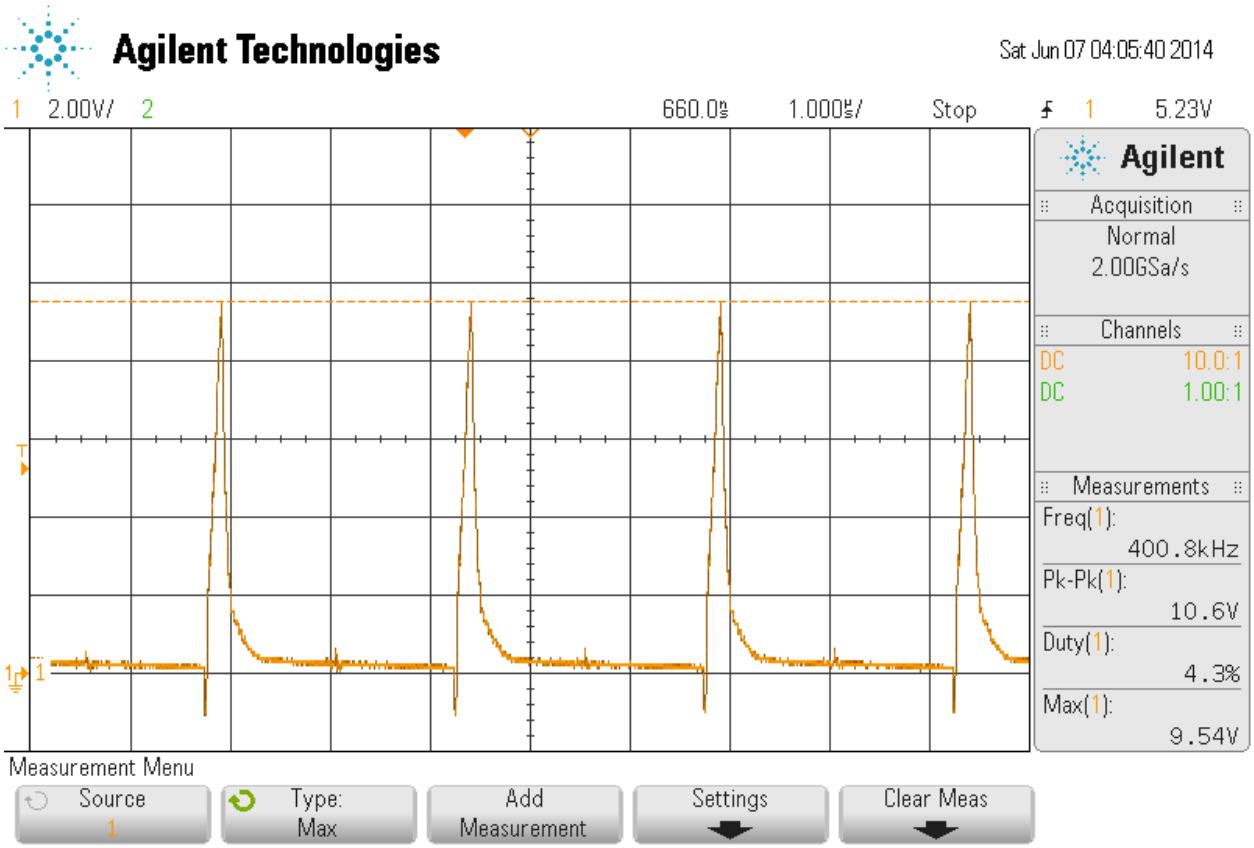


FIGURE 51
SLAVE, Q4 DRAIN WAVEFORM, 6V INPUT CASE

Based on Figures 44 to 47, the gate voltages suggested that the master DC-DC converter remained in boost mode as expected; Q1 remained on while Q2 remained off, and Q3 and Q4 alternated from switching on and off (refer to Appendix B for an example boost converter). However, Figures 48 and 49 shows that the input voltage didn't exceed the Q1 drain voltage, where we expected the input voltage to exceed the drain of Q2; Q1 drain saw 5.7V from the power supply, but Q2 drain saw below 1.5V instead of the expected 5.7V. For 5.7V to exceed the Q2 drain voltage, the gate of Q1 must switch from a low voltage to a high voltage of $5.7V+V_{GS(th)}$. But, Q1 gate (Figure 44) only sees about 5.8V max, and the MOSFETs have a gate

voltage threshold between 2.5V to 4.5V. So, Q1 gate needs, assuming 4.5V gate voltage threshold, at least 10.2V in order for Q2 drain to exceed 5.7V.

Also, the load provided a CV instead of a CC, but we need a CC at the load because the DC-DC converter should handle outputting the desire voltage. So, Figures 50 and 51 cannot accurately represent our converter since the load provides the CV instead of the converter providing the CV. However, when we had the load in CC and the power supply in CV at 6V, the output voltage stayed at 0V and the output current remained around 45mA while the input current remained below 0.15A. Since our simulations for test case #1 (6V input case) showed that our converter shouldn't output 36V for a 6V input case, we assumed the simulations and manufactured product agreed with each other.

However, when we tested the 30V input case, we received similar results to the 6V input case, where the load remains at CC and the supply remains at CV. We troubleshoot our board to determine what could have gone wrong; we tested each IC pin to see whether each pin saw the expected voltage as the simulations. Figures 52 to 75 show the probed results at different pins.

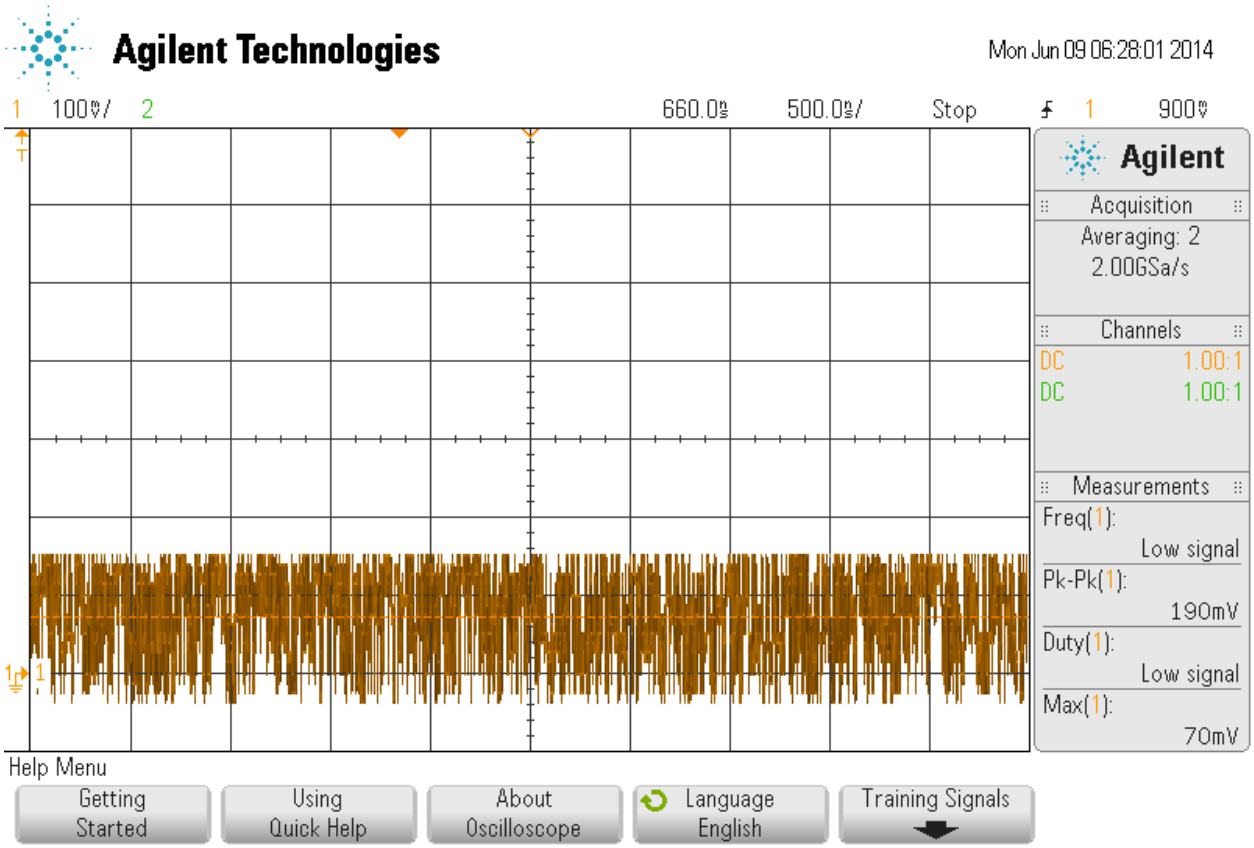


FIGURE 52
MASTER, SHORT PIN, 30V INPUT CASE

The SHORT pin should see (based on the simulations) 5V, but Figure 52 shows that the pin appears grounded and noisy. The noise could stem from that the ground connects to the signal ground, where small noises are expected. The reason the pin sees a low voltage or ground means that the IC senses a short at the output, which remains true as long as the load provides 0V. So, this pin appears functional since the load only provided 0V for our 30V input case.

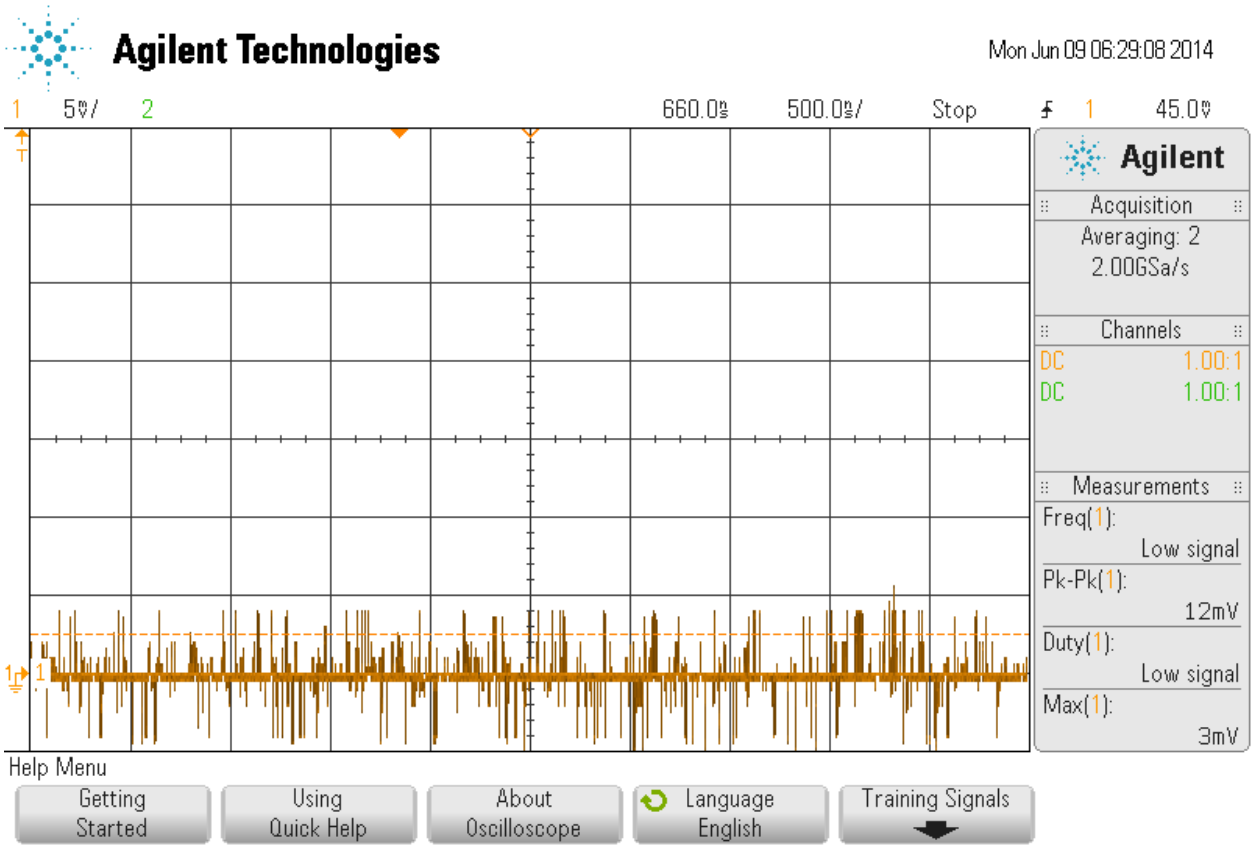


FIGURE 53
MASTER, FB PIN, 30V INPUT CASE

Similarly, the FB pin should remain low as long as output voltage remains low. Figure 53 shows that this statement remains true; the FB pin sees only small noises at ground.

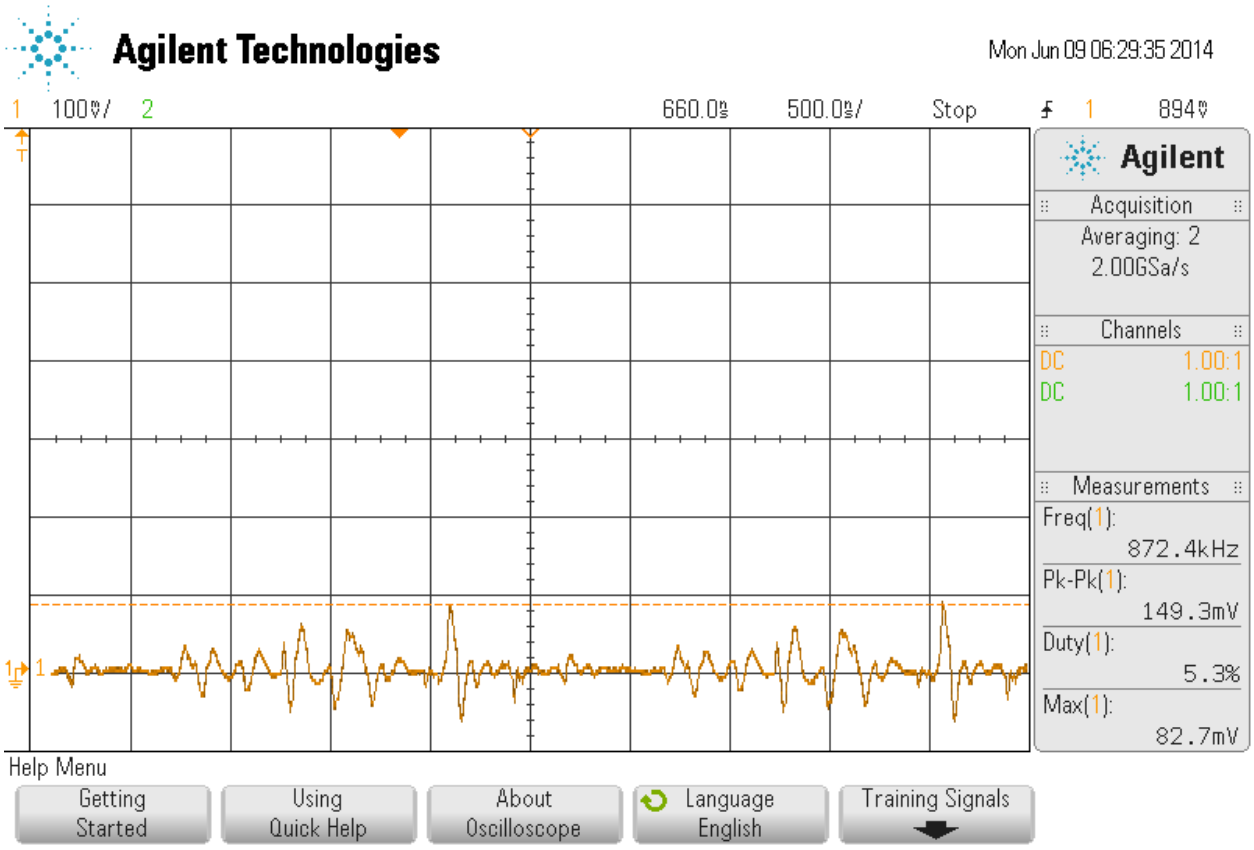


FIGURE 54
MASTER, INDUCTOR SENSING RESISTOR, SNSP PIN, 30V INPUT CASE

Inductor sensing resistor in the simulations comes out at a maximum 3mV with an average of 757µV. From Figure 54, however, the voltage peaks at 82.7mV. However, since we expect a 3mV max based on simulations, measuring such a low voltage would prove difficult to measure accurately without specialized equipment. Also, since we measured a small voltage below 100mV, we assumed that this pin doesn't experience any problems as of yet.

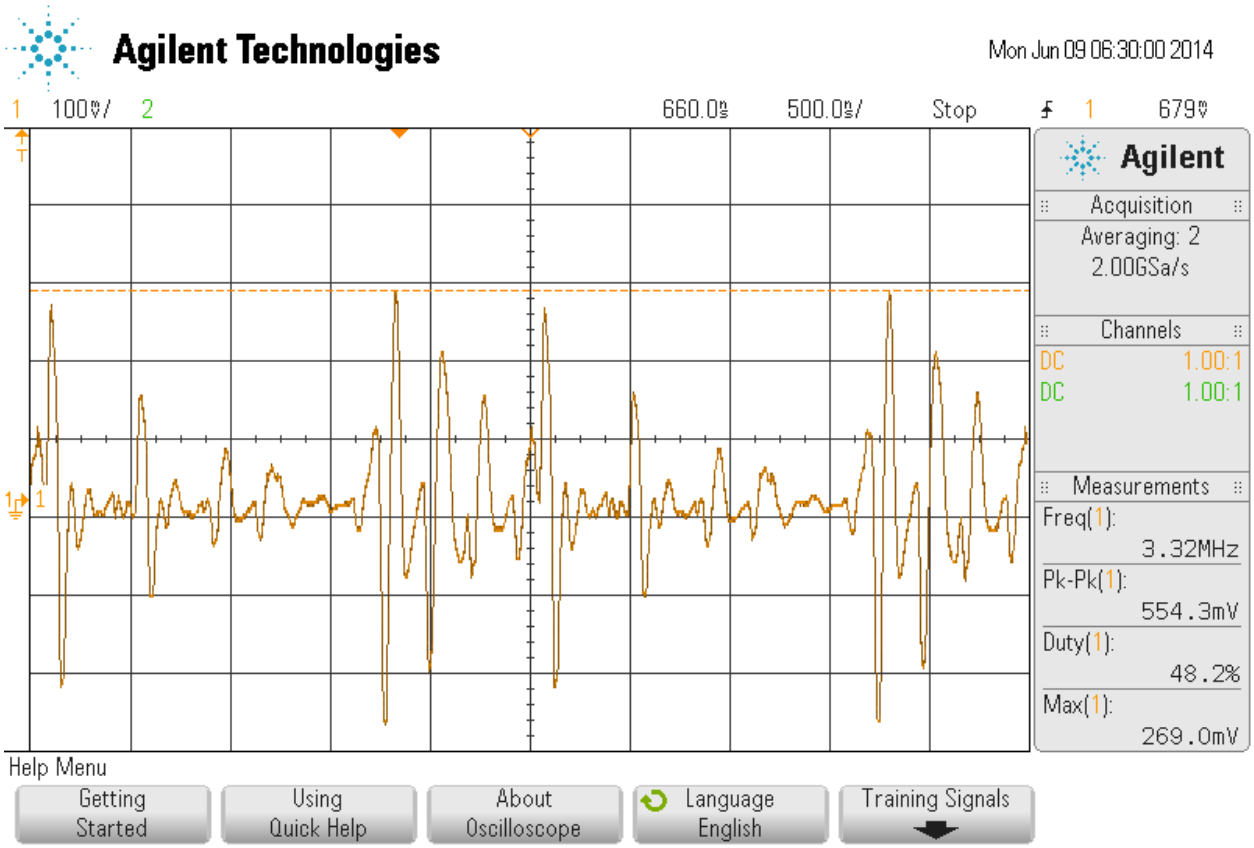


FIGURE 55
MASTER, SOURCE Q2 AND Q3, SNSP PIN, 30V INPUT CASE

Figure 55 shows the voltage at Q2 source and Q3 source, where the voltage remains less than 500mV. These points also connect to pin SNSP, but we want to ensure the connections between the source and resistor see the same results. It appears, though, that Figures 54 and 55 see different voltages. Perhaps the large trace between the two sources carry more noises than the sensing resistor, or the inductor may have affected the current flow of the trace between the sources and the sensing resistor since this trace runs underneath the inductor.

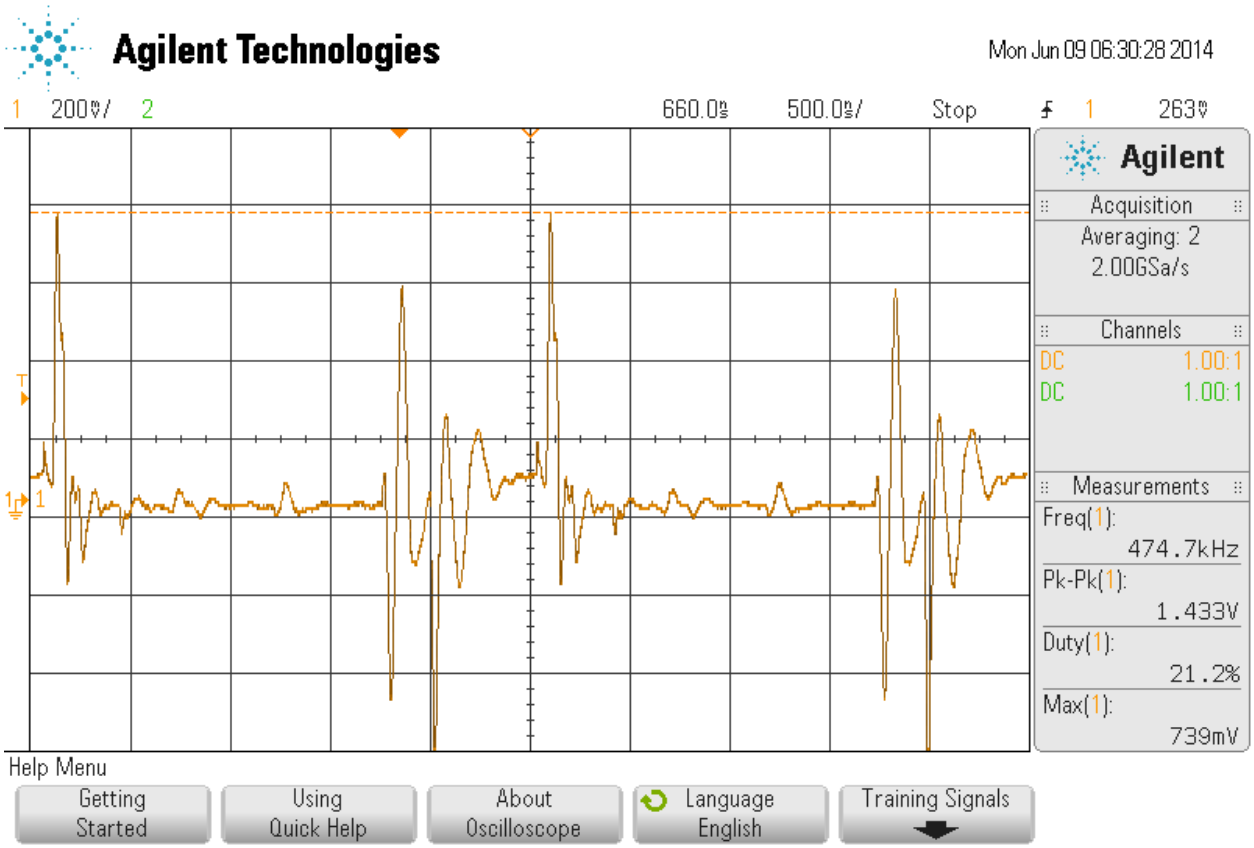


FIGURE 56
MASTER, DRAIN Q2 AND Q3, SNSP PIN, 30V INPUT CASE

Similarly, Figure 56 shows that the Q2 and Q3 drains also peaks at low voltages less than 600mV. So, Q1 and Q4 do not turn on and the voltages at Q1 and Q4 drains do not reach Q1 and Q4 sources (or Q2 and Q3 drains).

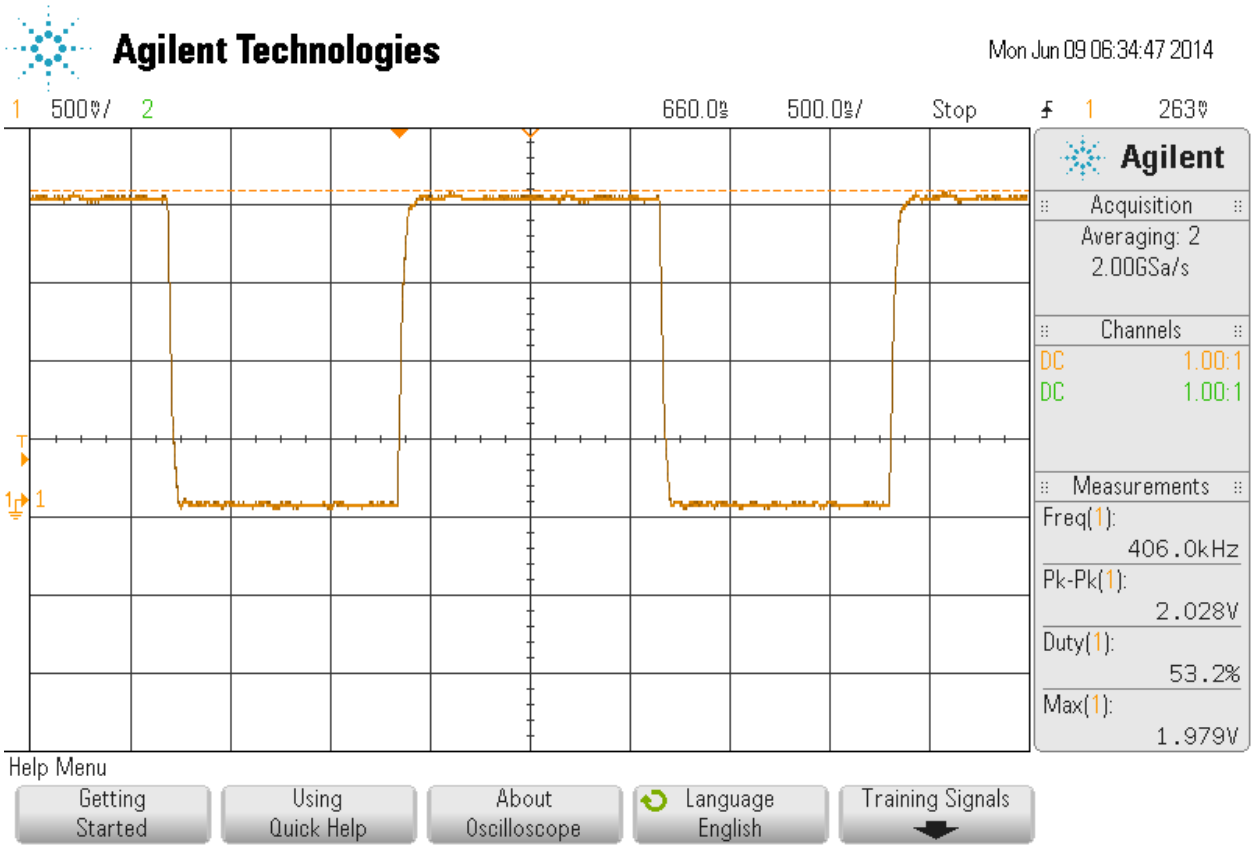


FIGURE 57
MASTER, CLKOUT PIN, 30V INPUT CASE

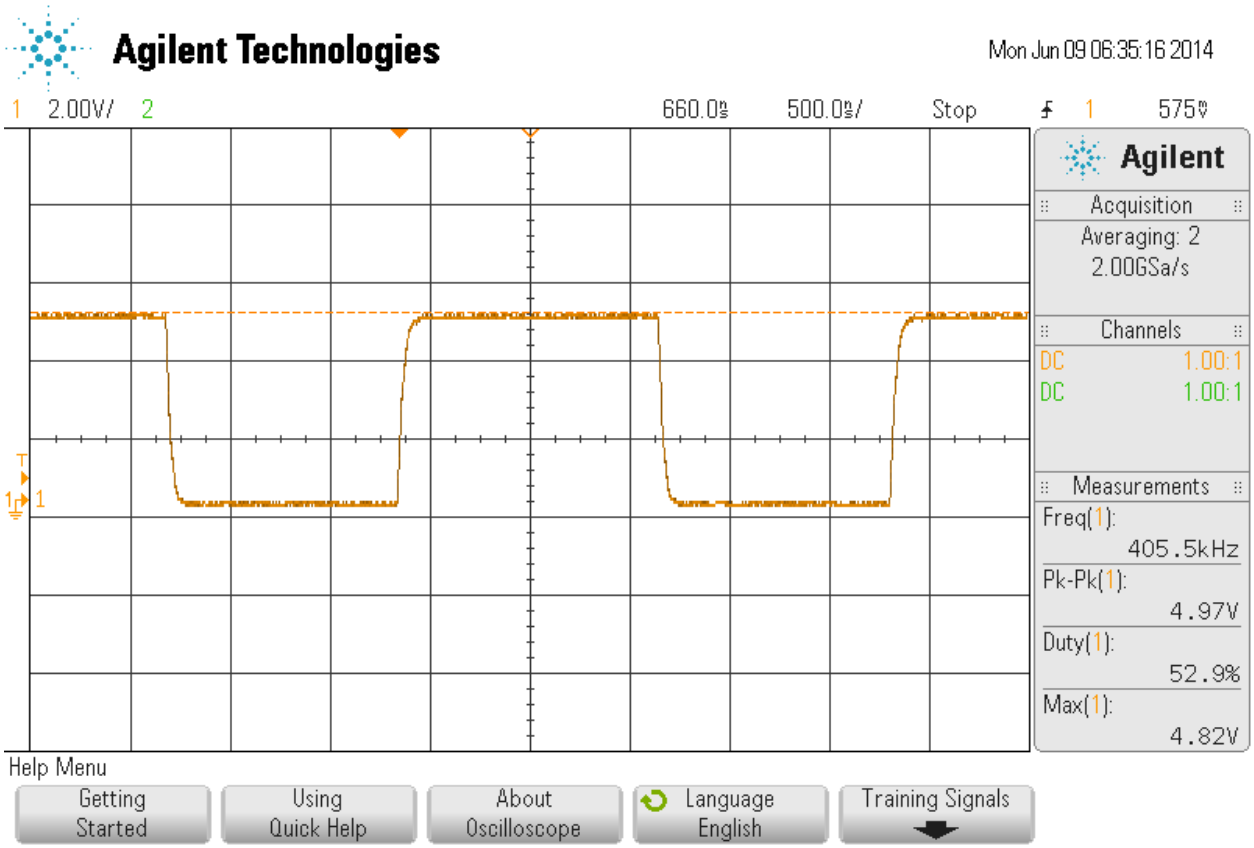


FIGURE 58
SLAVE, CLKOUT PIN, 30V INPUT CASE

The simulations showed that the CLKOUT pin has a $5V_{p-p}$ at 400kHz, but Figure 57 shows a $2V_{p-p}$ at 406kHz for the master board and Figure 58 shows a $5V_{p-p}$ at 405.4kHz for the slave board. The CLKOUT pin from the slave board doesn't connect to anything, but we measured this point to compare with the simulations; both the simulations and this point agree with each other. The smaller voltage peak-to-peak at the master board, however, suggests that resistance has lowered the expected $5V_{p-p}$ to $2V_{p-p}$. This resistance could stem from the jumper wires, though most unlikely. Whether this smaller voltage somehow affects the DC-DC converter remains inconclusive, since this small voltage could be a symptom from another issue of the board (i.e. since there is no voltage output, then the FB pin also doesn't see a voltage level).

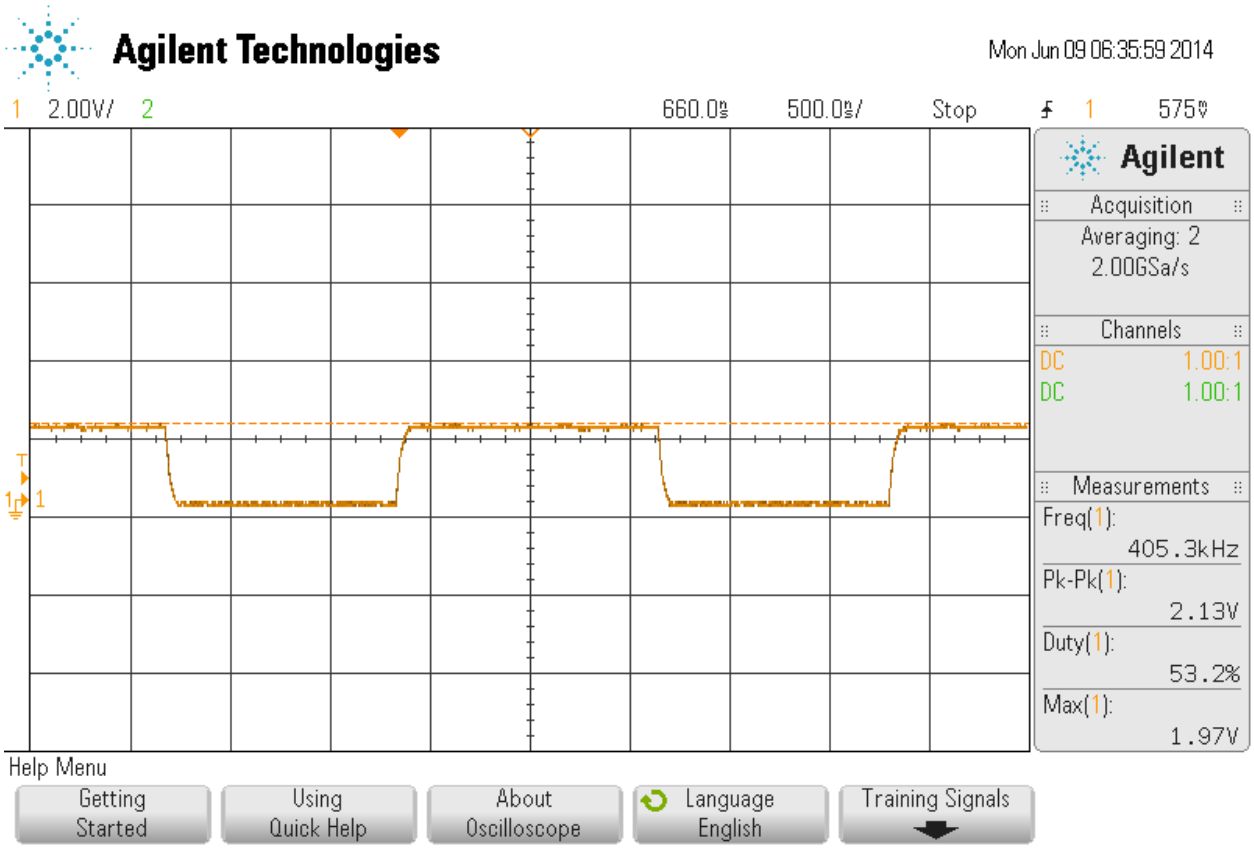


FIGURE 59
SLAVE, SYNC PIN, 30V INPUT CASE

Similarly, the simulations show the slave SYNC pin receiving the $5V_{p-p}$ at 400kHz, but Figure 59 shows a $2V_{p-p}$ at 405.3kHz. Again, we do not know whether this small voltage somehow negatively affects the DC-Dc converter or not.

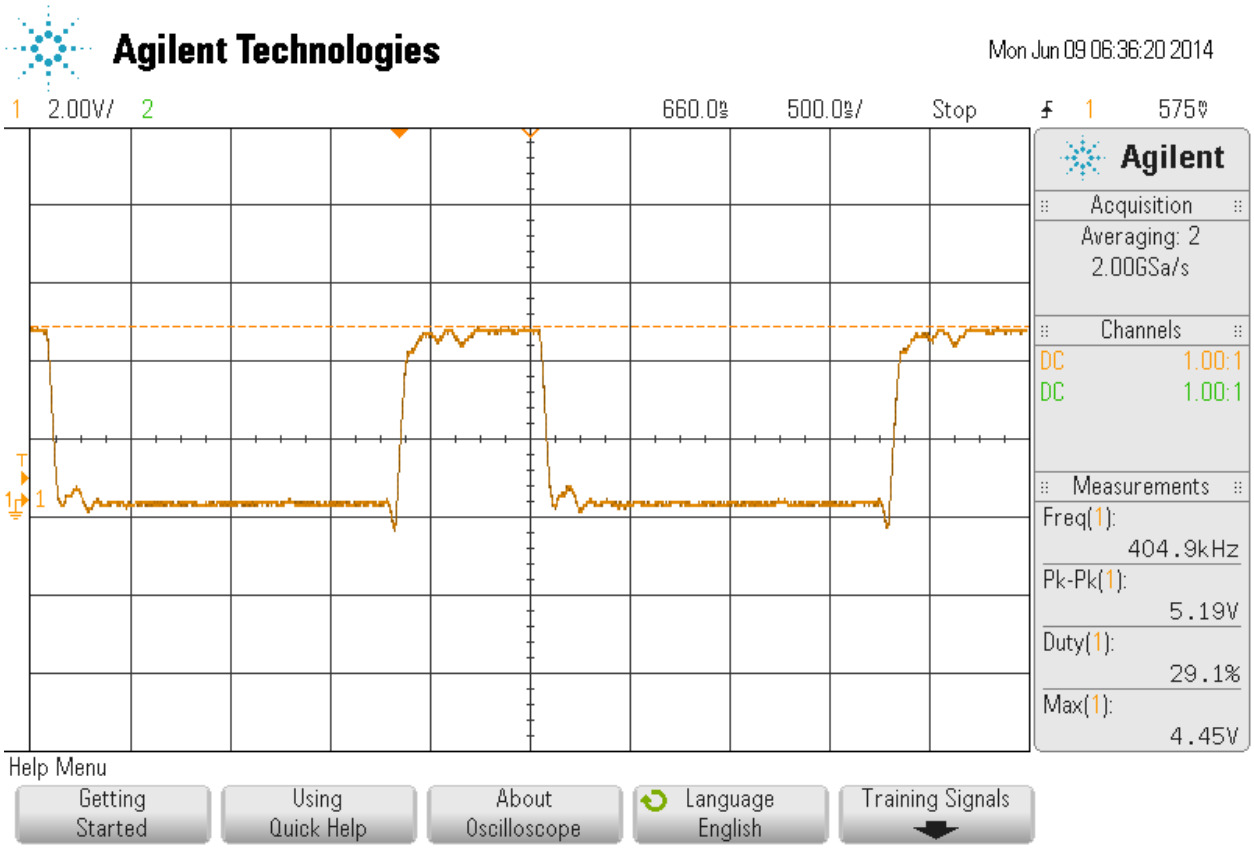


FIGURE 60
MASTER, TG2 PIN, 30V INPUT CASE

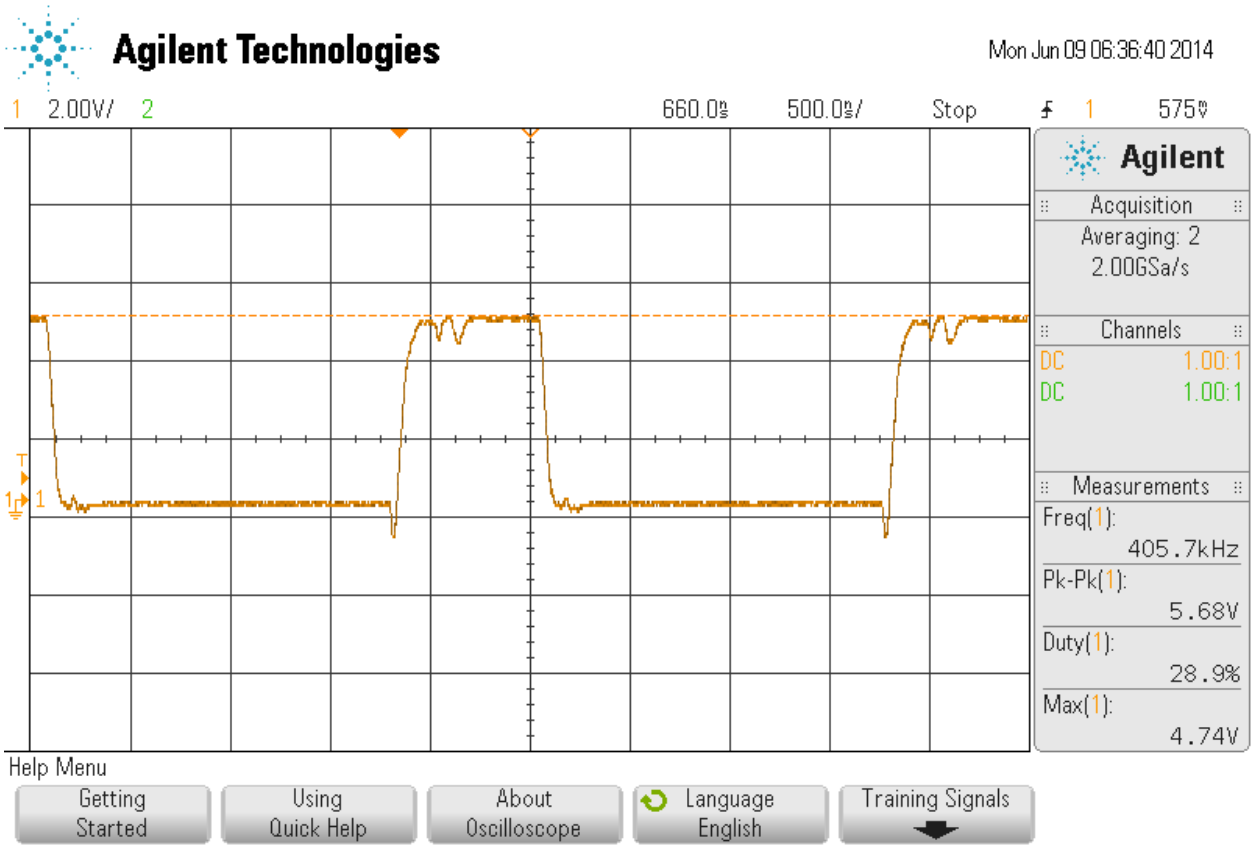


FIGURE 61
SLAVE, TG2 PIN, 30V INPUT CASE

The TG2 pin connects to Q4 gate, and Figure 60 shows the master board having a 5.19$V_{p-p}$ at 404.9kHz. But, the simulations show a 41$V_{p-p}$ at 400kHz, since a 30V case means the converter remains in boost mode. So ideally the gate voltage should exceed the drain (or $V_{OUT}$) voltage in order for Q4 to turn on and allow Q4 source and drain to have the same voltage. Also, the simulated Q4 gate has 70% duty cycle, but Figures 60 and 61 show a 30% duty cycle. This lower duty cycle suggests that $V_{OUT}$ would obtain a smaller value than the simulated results, based on the following equation of $V_{OUT}$, $V_{IN}$, and duty cycle D of Q3 (opposite of Q4's duty cyle; i.e. Q3 has 25% and Q4 has 75% duty cycles) for a boost converter:

$$Vout = \frac{Vin}{1 - D}$$

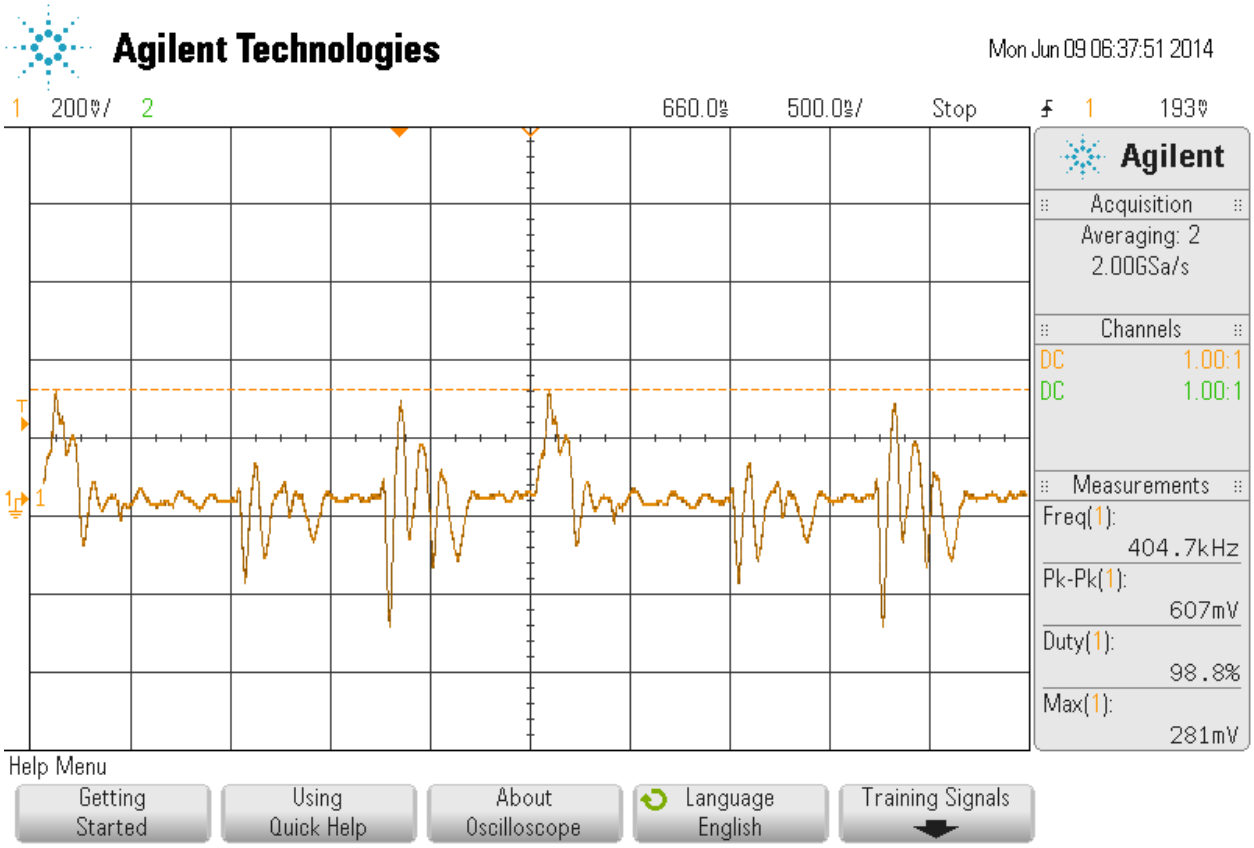


FIGURE 62
MASTER, Q4 SOURCE, SW2 PIN, 30V INPUT CASE

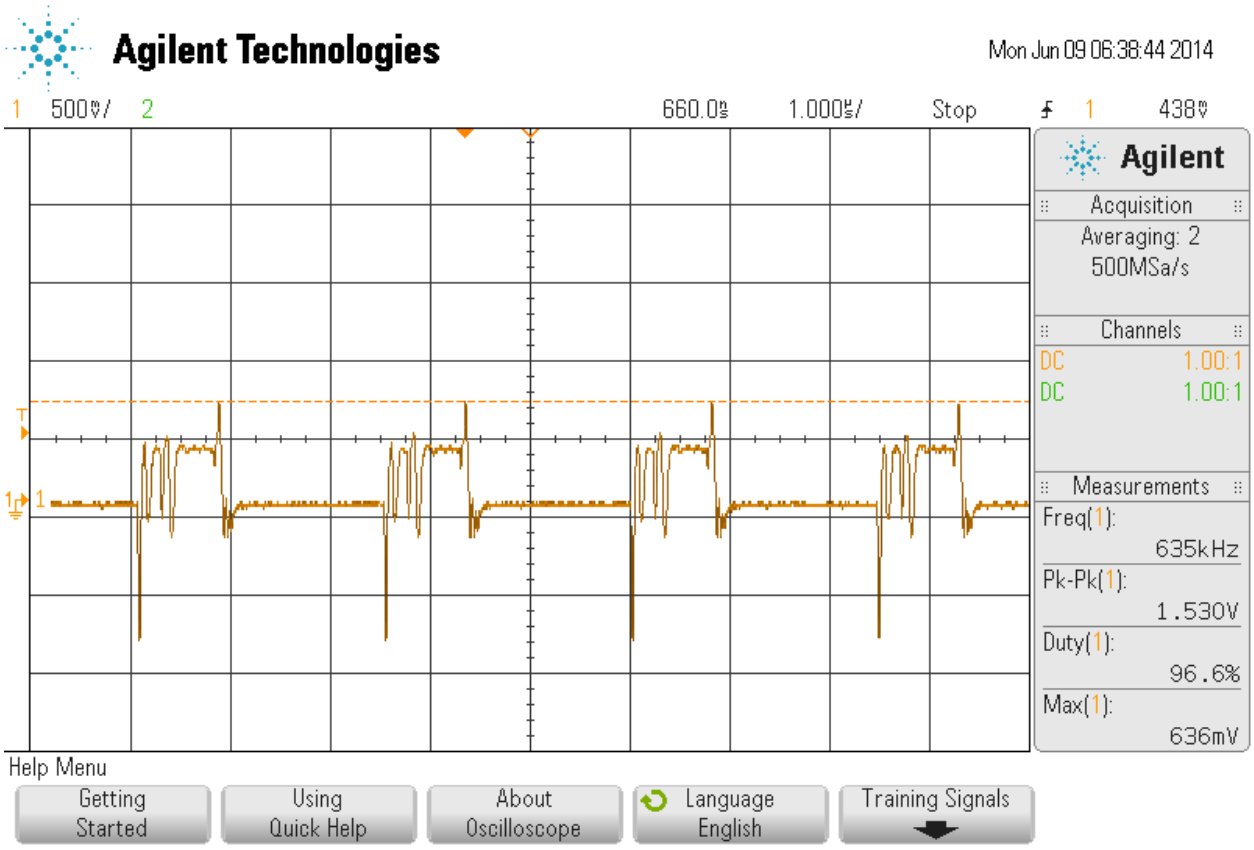


FIGURE 63
SLAVE, SW2 PIN, 30V INPUT CASE

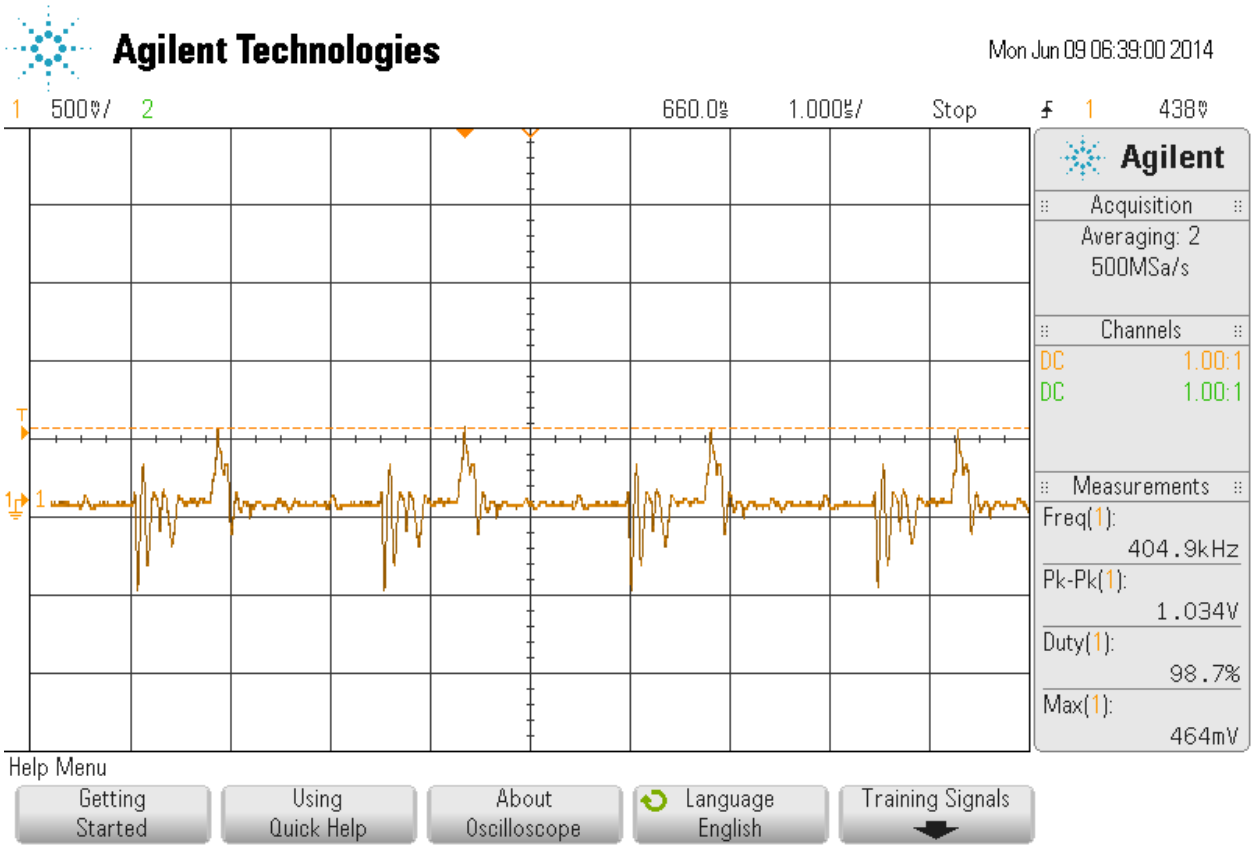


FIGURE 64
MASTER, Q3 DRAIN, SW2 PIN, 30V INPUT CASE

The SW2 pin connects to both the Q4 source and Q3 drain, where we expected both test points to experience the same voltage. However, Figure 62 and 64 show different results where Q4 source has a smaller voltage peak-to-peak than Q3 drain. Again, this difference could stem from interferes on the traces. Both Figures also have much lower voltage peak-to-peaks than the expected simulated results of $36V_{p-p}$. Since the gates of Q4 and Q3 remain much lower than $1V_{p-p}$, we can expected SW2 to remain low since Q4 and Q3 do not turn on. Also, Figure 63 shows the slave board's result at pin SW2, where an apparent square waveform appears. This means that pin SW2 on the slave board must be experiencing some form of switching, yet the pin master board doesn't experience switching. Referring back to Figures 60 and 61, the gate voltages on

TG2 do have different $V_{p-p}$, where the slave TG2 has a higher $V_{p-p}$ than the master TG2. Perhaps the slave TG2 had enough voltage to overcome the gate voltage threshold of the MOSFET, so then Figure 63 would show the square-like waveform.

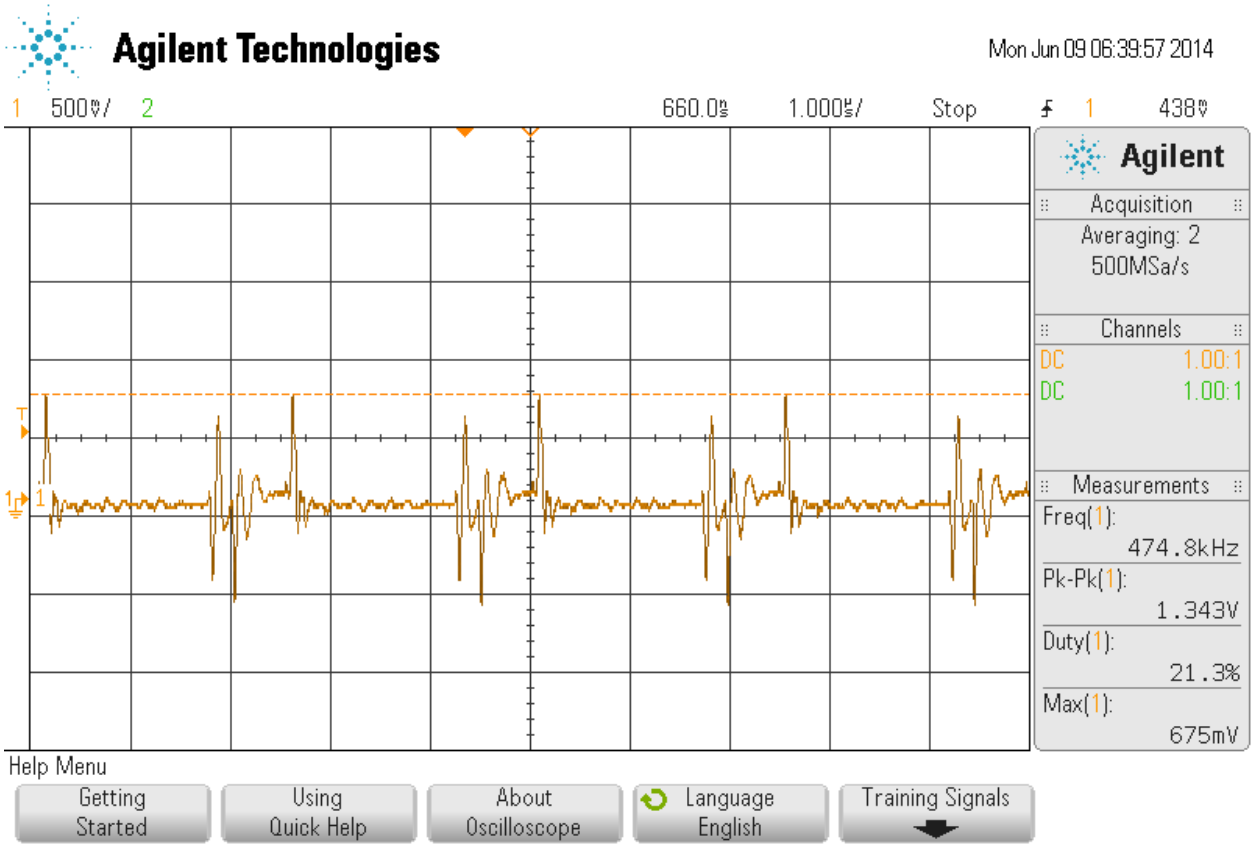


FIGURE 65
MASTER, SW1 PIN, 30V INPUT CASE

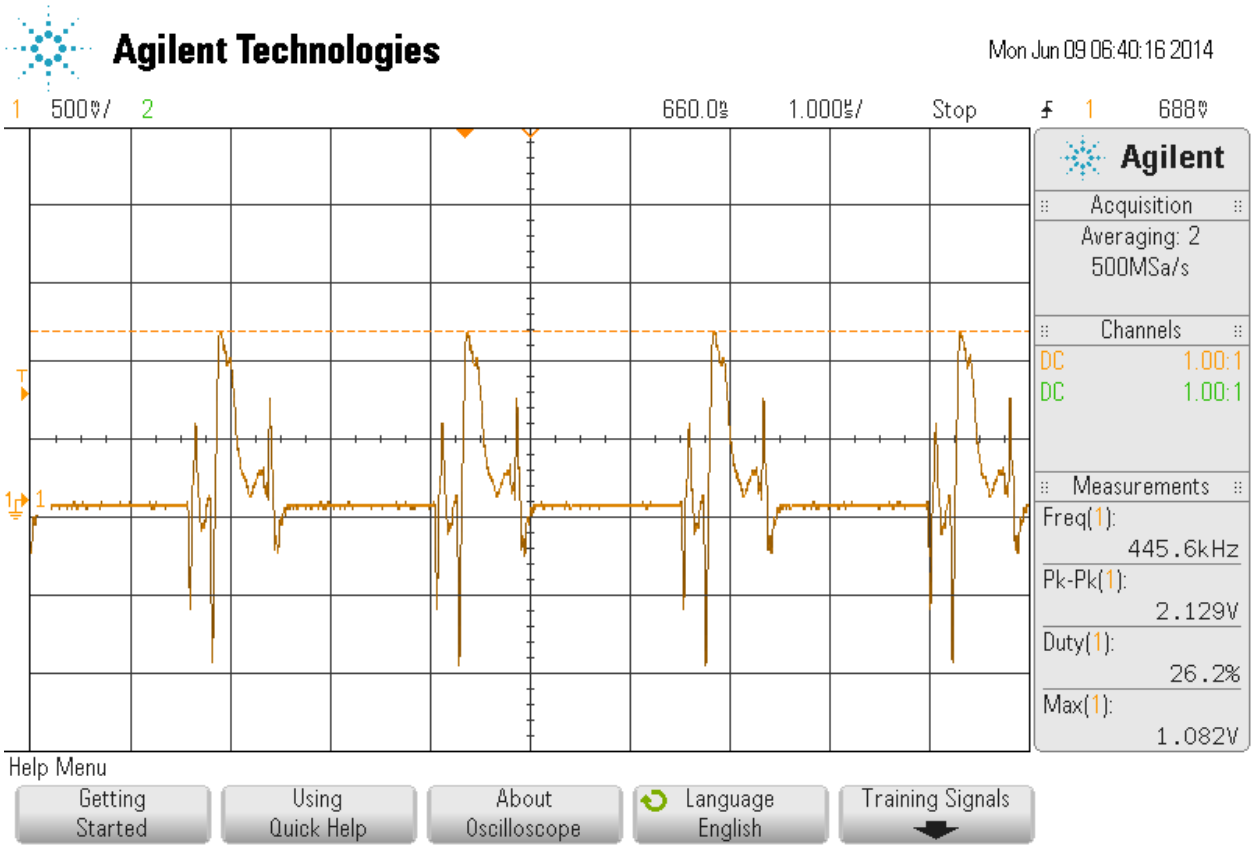


FIGURE 66
SLAVE, SW1 PIN, 30V INPUT CASE

Figure 55 shows the measurement at the master pin SW1, which represents mostly noise just like Figures 62 and 64. For the slave board, however, Figure 66 shows the SW1 pin not having a square waveform like Figure 63. Since the SW1 and SW2 pins have an inductor in-between, the inductor could have stored in the peaks voltages at the SW1 pin and outputted the square-like waveform at SW2. But, since these voltage remain much lower than 2.129V, this again confirms our MOSFETs do not turn on.

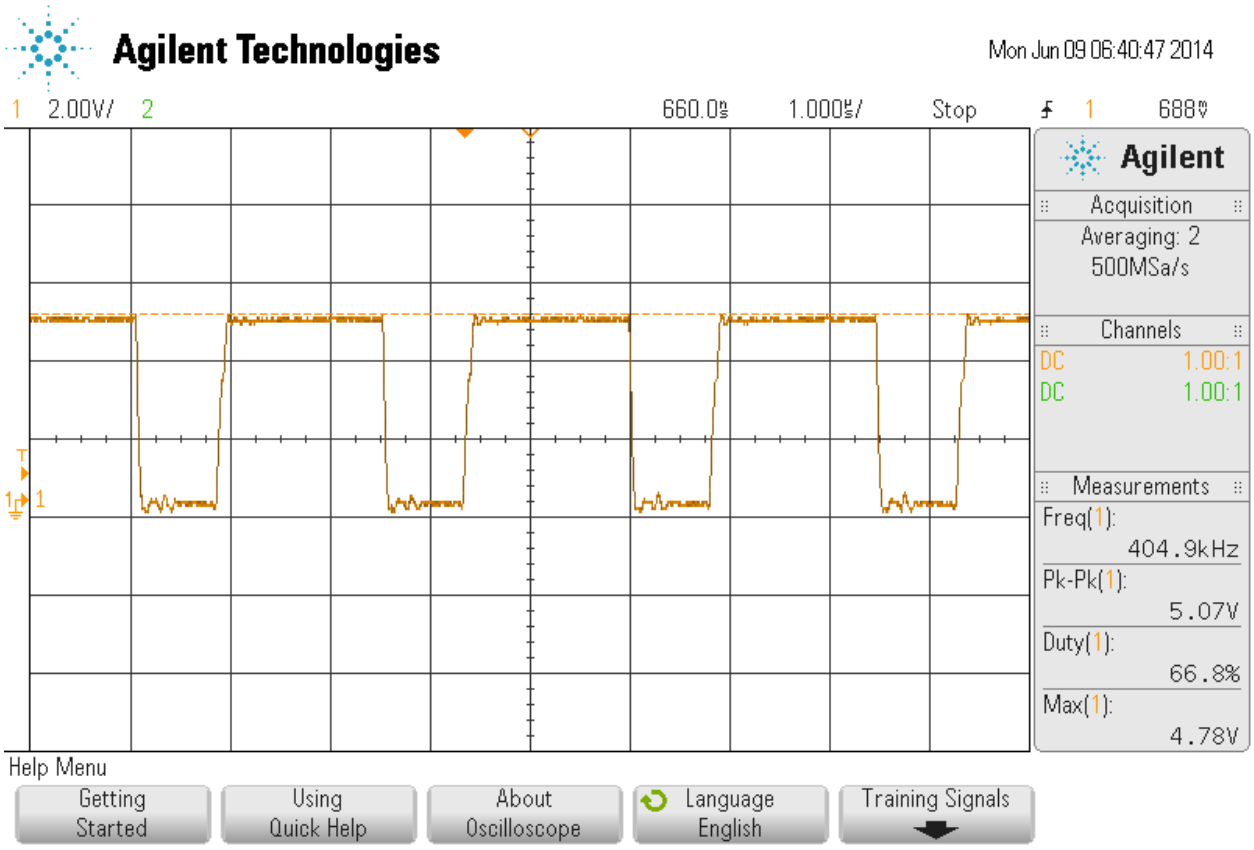


FIGURE 67
MASTER, BG2 PIN, 30V INPUT CASE

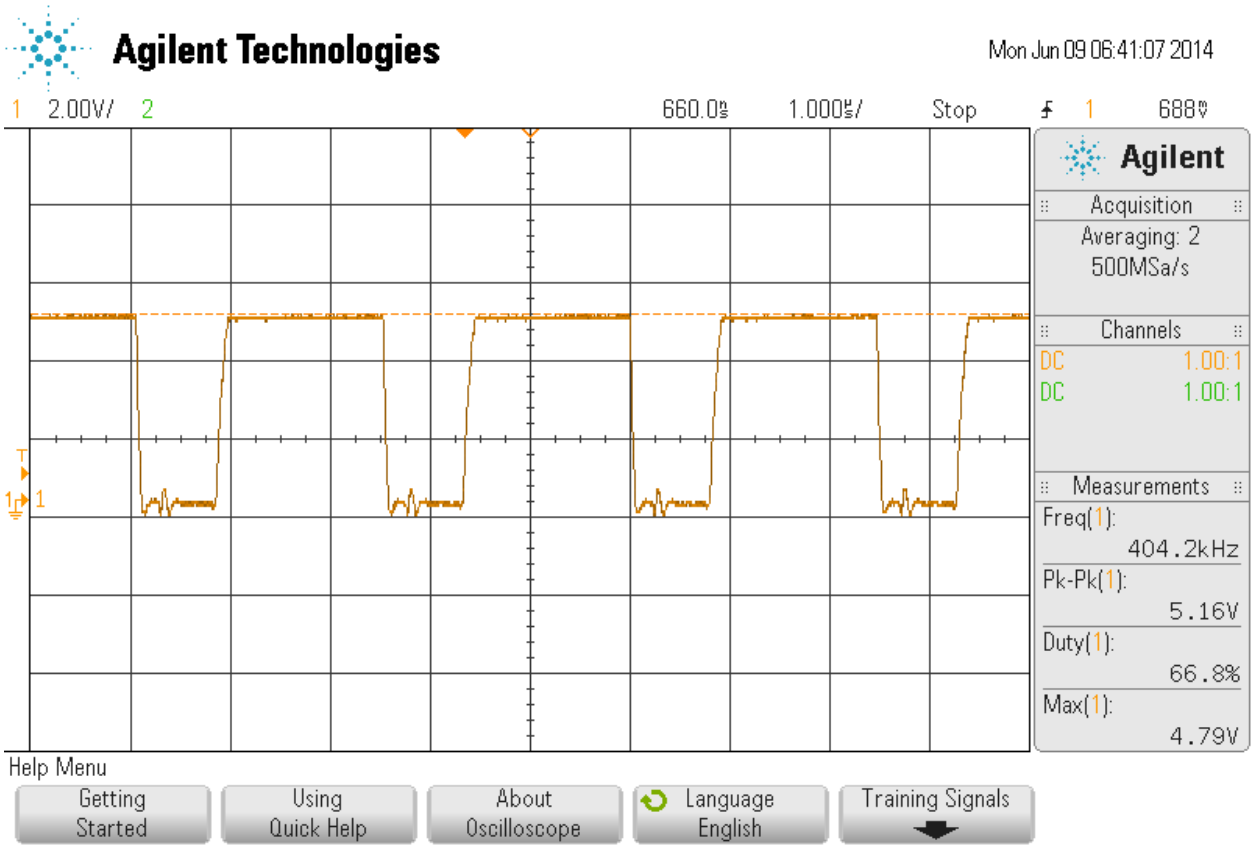


FIGURE 68
SLAVE, BG2 PIN, 30V INPUT CASE

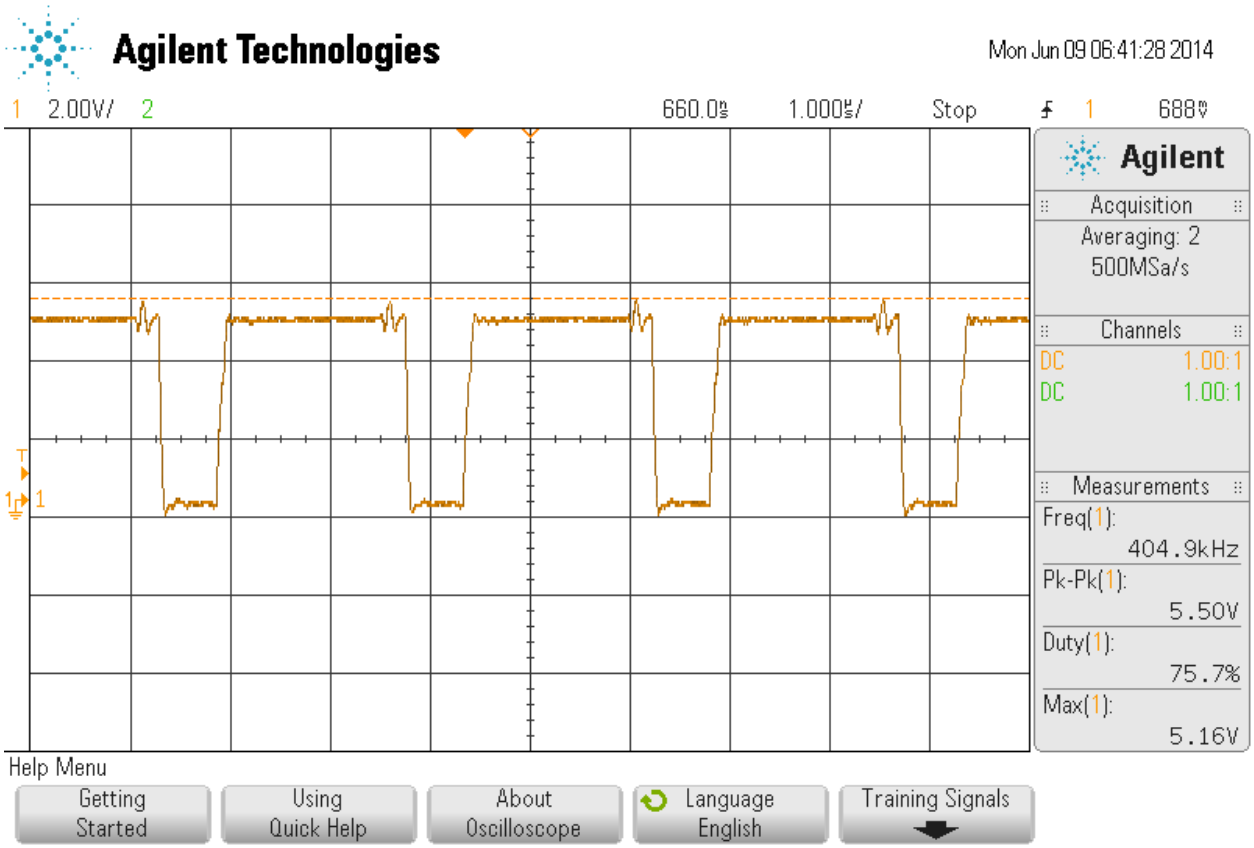


FIGURE 69
MASTER, BG1 PIN, 30V INPUT CASE

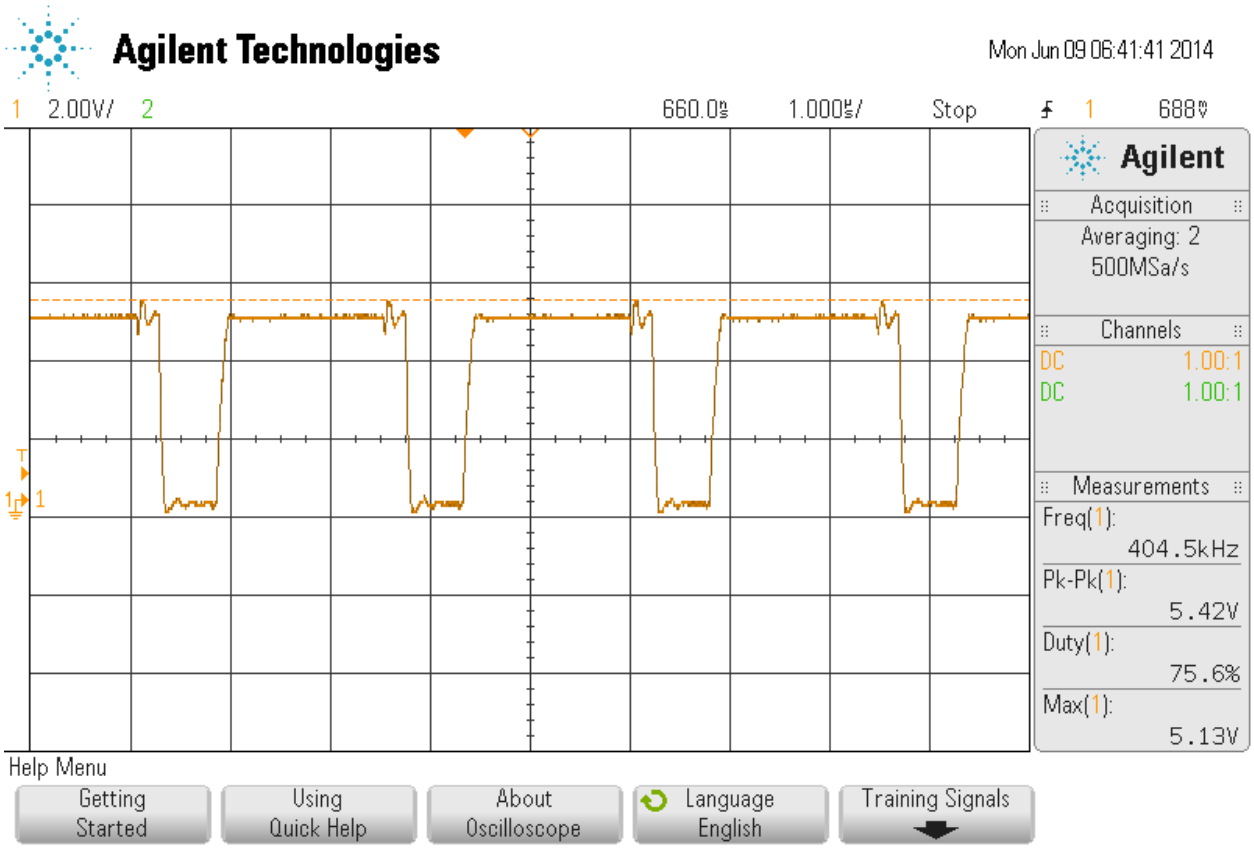


FIGURE 70
SLAVE, BG1 PIN, 30V INPUT CASE

Figures 67 to 70 show the gate voltages at Q2 (BG1) and Q3 (BG2) for both the master and slave boards. We expected these voltage peak-to-peaks to reside around $5V_{p-p}$ with 27% duty cycle, but we measured about $5.1V_{p-p}$ and 66.8% duty cycle at the BG2 pins and $5.45V_{p-p}$ and 76% duty cycle at the BG1 pins. The higher duty cycle at BG2 somewhat corresponds with the 30% duty cycle at pin TG2, meaning these two pins do alternate each other.

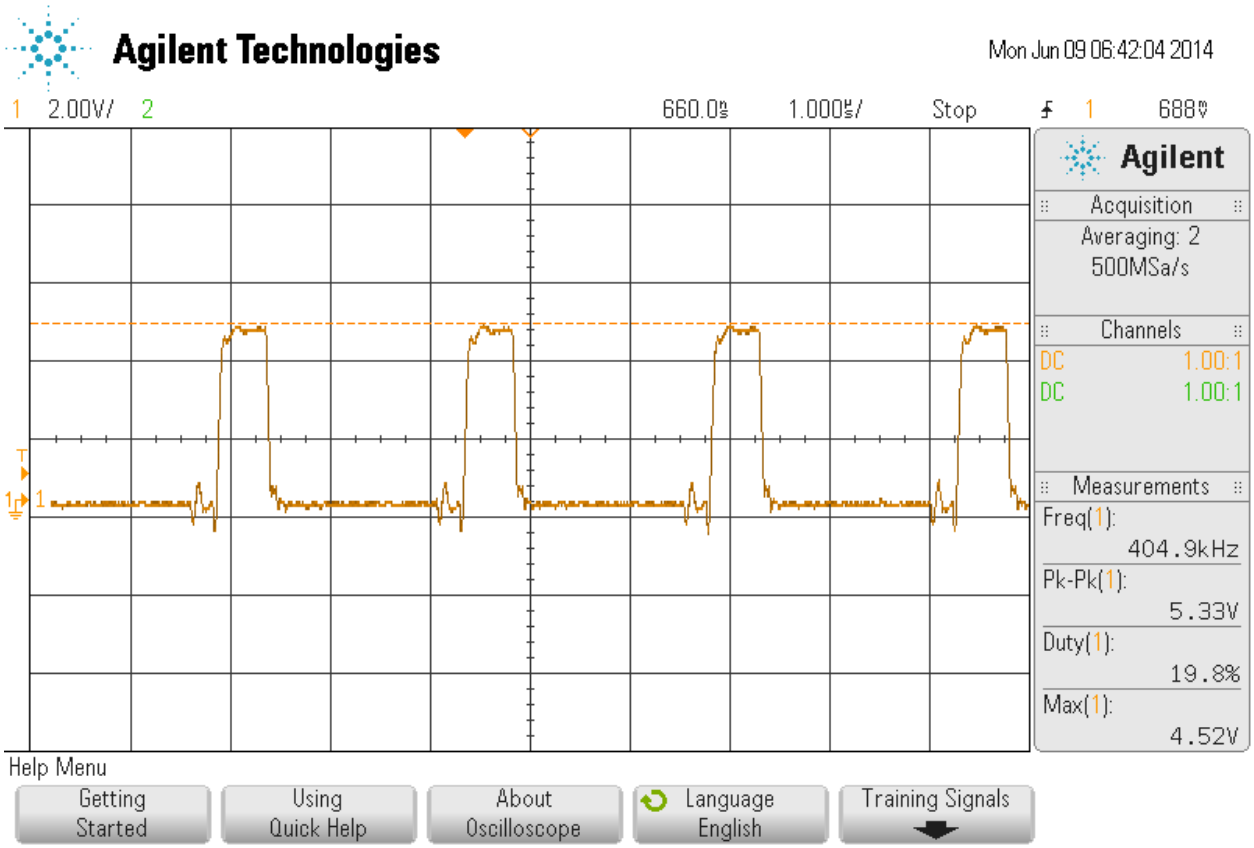


FIGURE 71
MASTER, TG1 PIN, 30V INPUT CASE

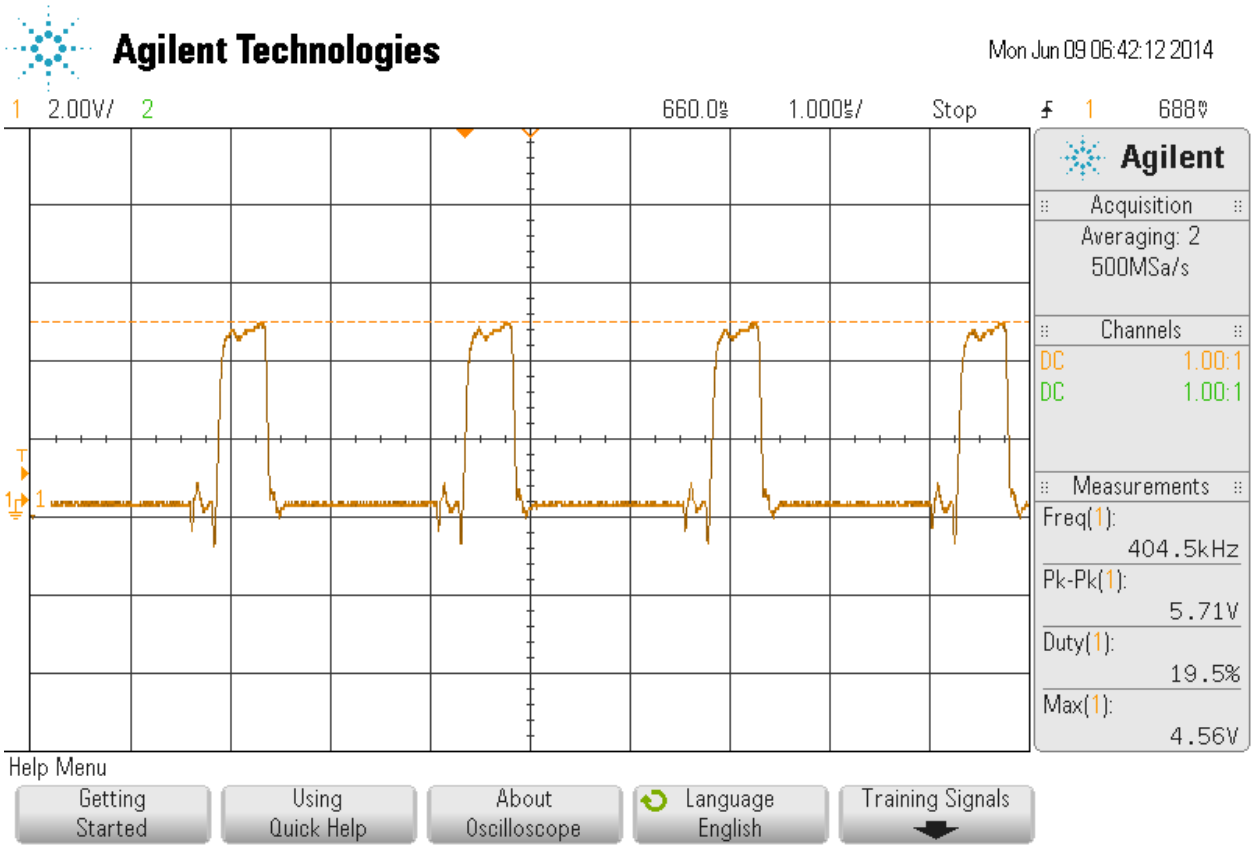


FIGURE 72
SLAVE, TG1 PIN, 30V INPUT CASE

The TG1 pins connect to the gates of Q1, and Figures 71 and 72 show gate voltages switching at the master and slave TG1 pins. The simulations showed a $34V_{p\text{-}p}$ at 10% duty cycle, but we measured $5.5V_{p\text{-}p}$ and $5.7V_{p\text{-}p}$ at 19.8% duty cycle. This difference between the duty cycles suggest that the inductor will not see a lot of voltage at Q1 source even if Q1 ever turns on. The IC should have provided the expected gate voltage of 30+V at Q1 gate, but for some reason the IC only provides 5.71V at most. So, either the internal functions in the IC do not function properly or some connection on the board doesn't provide the correct voltage to activate the gate voltage to rise higher than 5.71V. Compared to the BG1 waveforms in Figures 69 and 70, though, the TG1 and BG1 pins do somewhat alternate each other as expected.

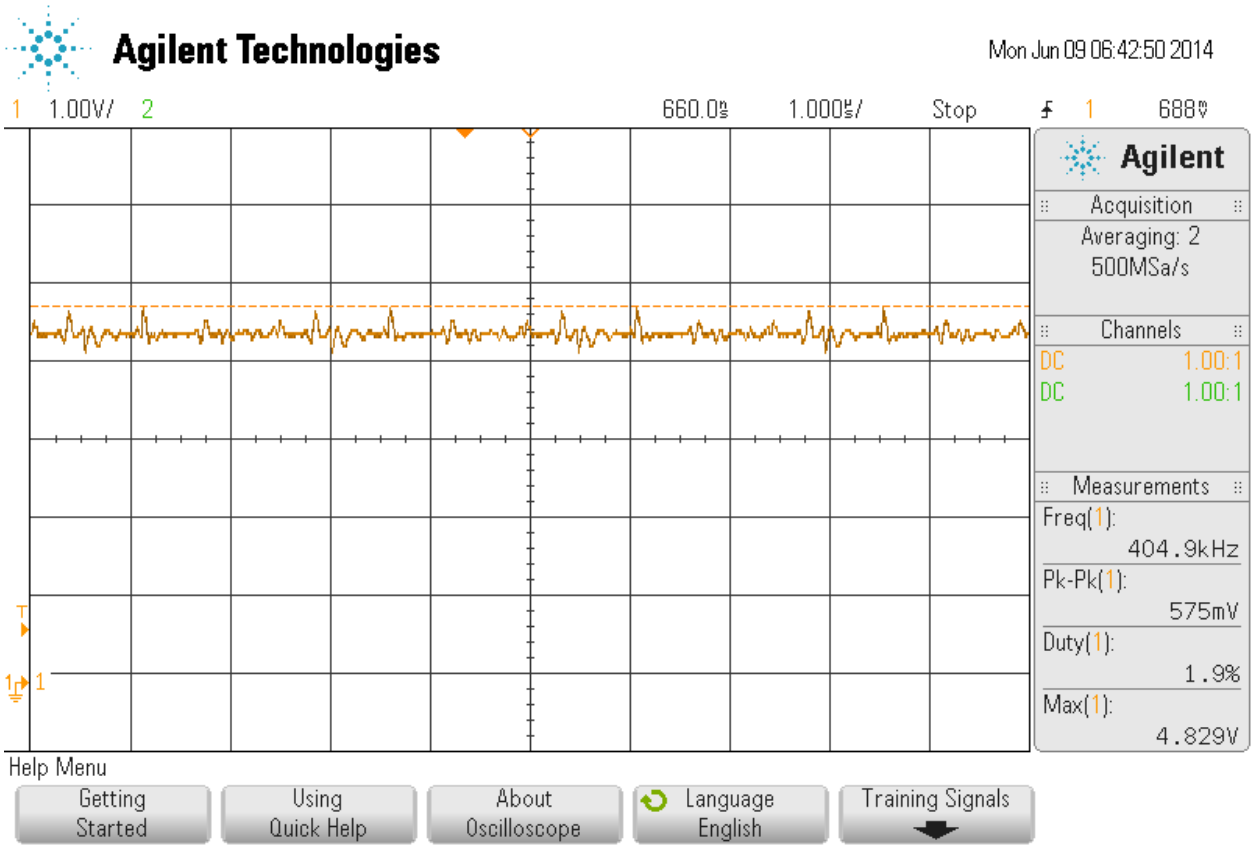


FIGURE 73
MASTER, BST1 PIN, 30V INPUT CASE

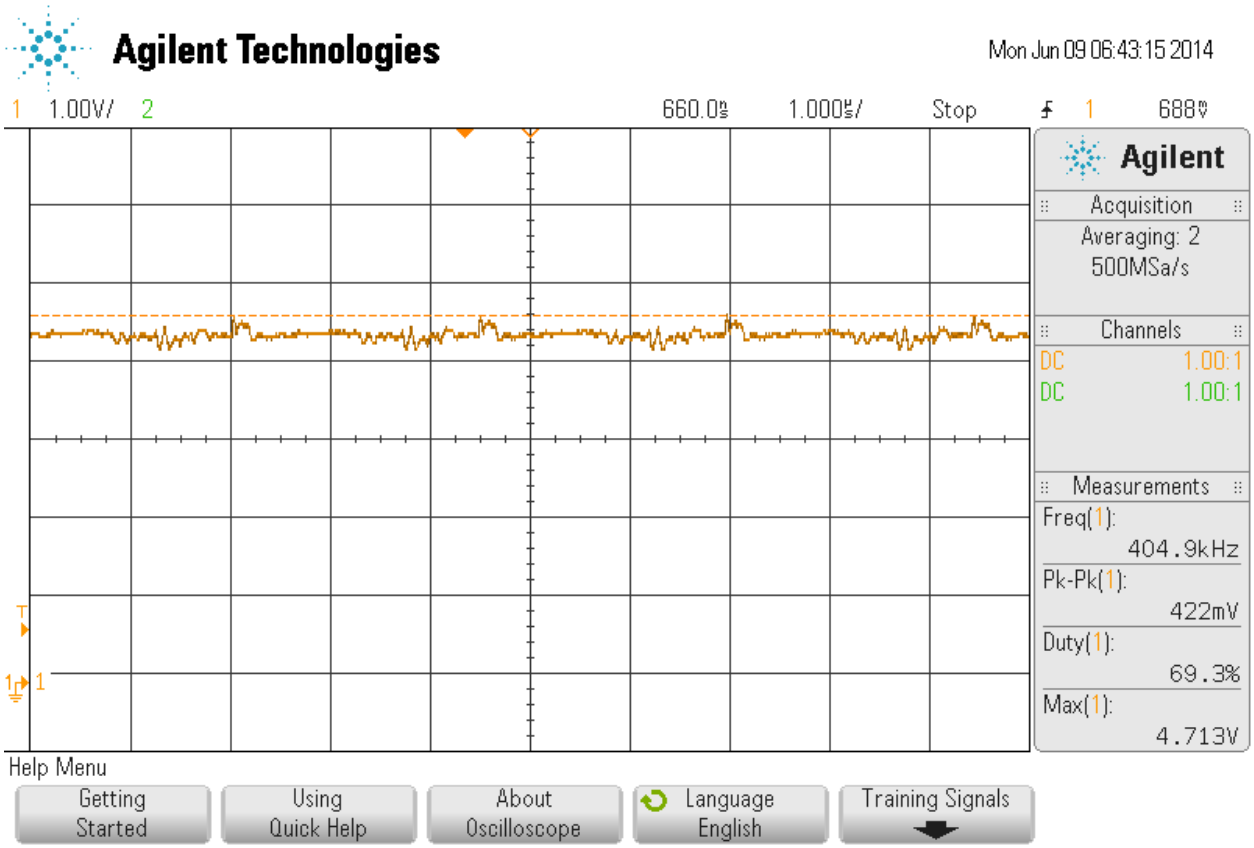


FIGURE 74
MASTER, BST2 PIN, 30V INPUT CASE

The BST1 and BST2 pins on the master board also see only 5V, as seen in Figures 73 and 74. The simulations show that BST1 should output 32V and BST2 should output 42V, yet since Q1 cannot turn on due to low gate voltage, these two pins cannot output a high voltage.

We also tested several other pins and connection points on the board, though we didn't take oscilloscope captures of these points since these points provided very little information. For example, the ISP and ISN pins only had low noise since these pins correspond with $V_{OUT}$, which remains 0V. We also tested the voltage at the $V_C$ pin, where the simulations showed a 1.2V, but we measured 1.7V. We do not know how this voltage difference actually affects our circuit, but we suspect that this could be more of a symptom of the converter not operating than it being a

cause for the converter not operating. Similarly, we measured pins C/10 and CCM at 4.35V, but we expected 5V. Also, pin SS measured 1.7V when we expected 2V. Again, these lower measured voltages could be symptoms of the converter not operating correctly.

### 10.3 Final Testing

Based on the data we gathered, we first thought that the MOSFETs may have issues switching on as expected. So, to finalize our project, we took out Q1 from the master board and characterized its $R_{DS(on)}$ vs. $V_{GS}$ and $I_D$ vs. $V_{GS}$. A multi-meter was used to measure the resistance across drain and source of the IXTH180N10T MOSFET. The gate voltage was attached to a voltage source which outputs a 60Hz square-wave at 50% duty cycle. The MOSFET's source was used as a common ground. The gate voltage was initially set to 0V. We then increased the gate voltage until the multi-meter's resistance measurement was readable. The multi-meter read "OL" until VGS was 2V. From henceforth, RDS continued to drop as VGS increased. No voltage was applied to the drain from a source. Therefore, VDS is theoretically approximately 0V aside from the voltage induced by the multi-meter.

The Keithley Source-Meter was used to measure drain voltage and current when a separate power source applied a varying 60Hz, 50% duty cycle square-wave to the gate. The Keithley Source-Meter's output was applied to the MOSFET's drain at 0.4V with a 1A current limit. For this test, $V_{GS}$ was slowly increased until $I_D$ increased, then data was recorded.

The same process was used to measure $I_D$ vs. $V_{GS}$ at a 6V $V_D$. $V_D$ was increased to 6V from 0.4V so the setup and test methodology were the same as in the 0.4V case. For $V_{GS}$ greater than 5V, $I_D$ limited itself to 53mA, even though the current source was limited to 1V. Figures 75 and 76 show the resulting measurements.

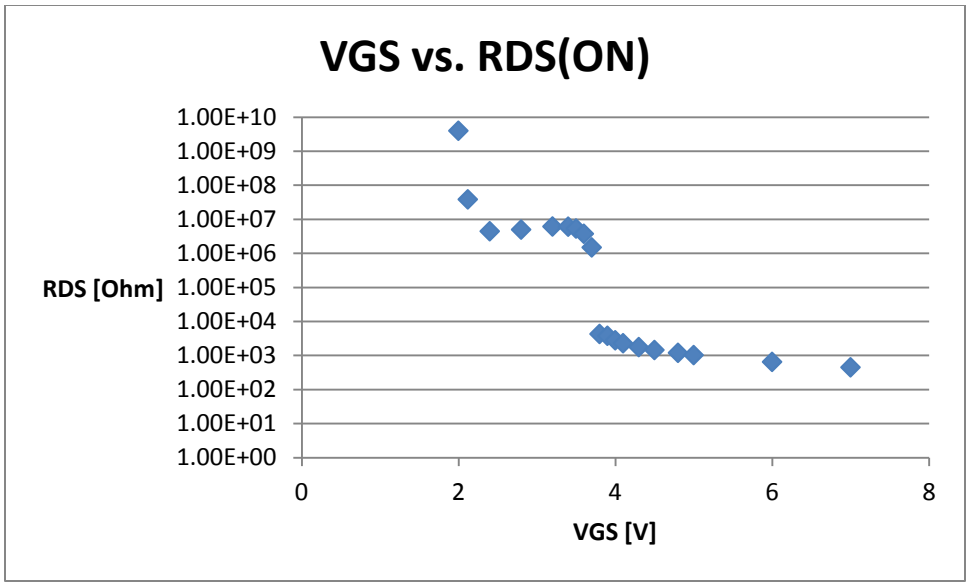


FIGURE 75
$V_{GS}$ VS. $R_{DS(ON)}$ GRAPH FOR Q1 MOSFET

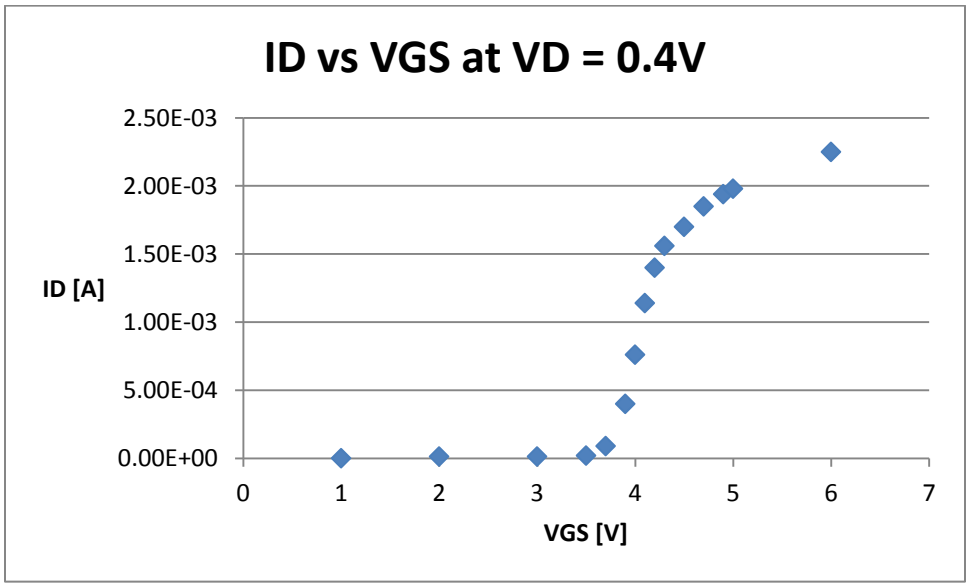


FIGURE 76
$I_D$ VS. $V_{GS}$ AT $V_D$ = 0.4V GRAPH FOR Q1 MOSFET

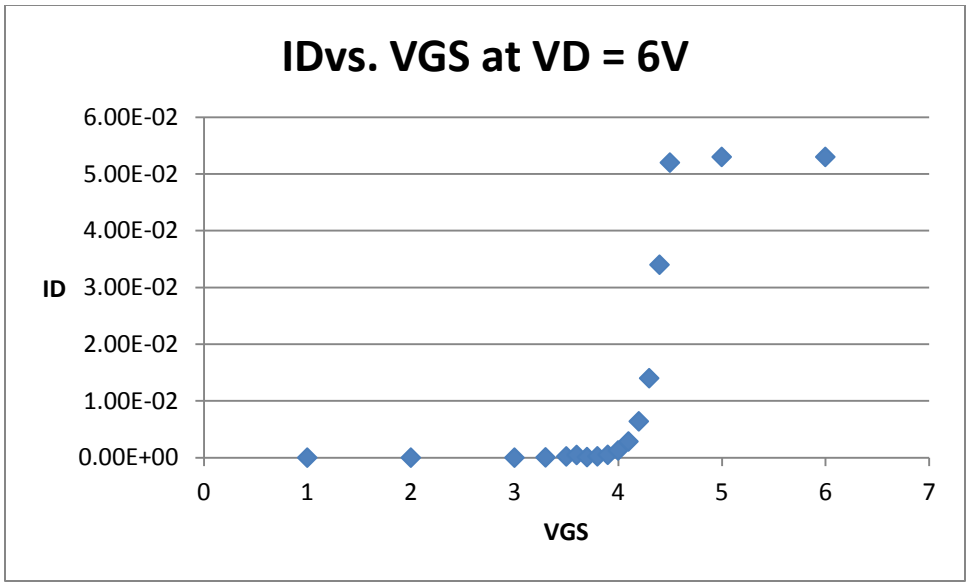


FIGURE 77
$I_D$ VS. $V_{GS}$ AT $V_D$ = 6V GRAPH FOR Q1 MOSFET

Based on Figures 75, we noticed that the $R_{DS(on)}$ values contained two different resistance levels, though both remained above 1kΩ. We soon found out that we neglected to take into account the body diode within the power MOSFET, so most of the data here cannot be taken in for consideration.

With the minimal testing we executed, we didn't learn exactly what the boards' issues were. Since we didn't have enough time to troubleshoot the boards, we can only conclusively say that testing must begin much earlier than what we accomplished.

# Chapter 11: Conclusion

The results we gathered suggested that we failed in producing a product that can meet the customer needs and required specifications. This project shows that both the LT3791 and LT3791-1 designs may not be able to handle the elliptical trainer's high power output. Or, the components we soldered onto the boards may have been mishandled. For example, when handling the MOSFETs, we may have accidently touched the MOSFETs without being properly grounded. So, we may have created static charge on the MOSFET and short-circuited some internal parts of the MOSFET. Also, we did have one board that stopped working when we were measuring test points on it, where we accidently shorted the gate and source of Q1. Thus, we may have mishandled our boards.

If our mishandling didn't affect the boards, however, then we also speculated that the MOSFET may not be switching as it should. We tried characterizing Q1 during the final testing, but due to the body diode of the power MOSFET, we couldn't develop a test plan in time that accounts for the body diode. Thus, the characterization testing we measured in the previous section remains unsuccessful.

Finally, we considered that the IC may be at fault, where the IC didn't provide the necessary gate voltage for Q1 (pin TG1). Though we expected a gate voltage exceeding Q1 drain, we only obtained around 5V maximum. The circuitry involved with controlling the gate voltage at Q1 resides within the IC, specifically the buck logic shown in page 11 of the LT3791-1 datasheet [16]. The pins FB, CTRl, OVLO, $V_C$, CCM, SNSP, and SNSN control the buck logic circuit. But specific details about how these pins control the circuit remain minimal, so we cannot determine exactly where the pin fault occurs.

Overall, this year-long project provided several key important notes to consider for future projects. First, the simulation runs must begin as soon as possible, in order to save time for designing the PCB layout and testing procedures. The simulation runs for this project took the longest time to execute, so future groups should consider having several group members running different simulations. Second, the PCB layout design must meet specific requirements, both provided our advisor and what he datasheets suggest. Since we only met requirements provided by the advisor and not the LT3791-1 datasheet, we may have designed a PCB layout that wouldn't satisfy all of the IC's quirks or functionalities. Finally, a solid time schedule should be followed at all times. While we made an initial Gantt chart to follow as a guideline (appears within Appendix A), we soon found out that the initial Gantt chart didn't account the enormous time consumed with simulations and PCB design. Thus, future groups should better prepare for these time-consuming processes in order to execute their projects effectively. So on a final note, this project only provides ideas on what to avoid, what the LT3791's and LT3791-1's capabilities require, and what the EHFEM project should acquire to fulfill its customer needs.

# APPENDIX A – SENIOR PROJECT ANALYSIS

**Energy Harvesting from Exercise Machines (EHFEM) – DC-DC Buck Boost Converter (LT3791)**

**Student: Matthew Wong** **Student's Signature:_____**

**Advisor: David Braun** **Advisor's Initials: _____** **Date: _____**

## A.1 Summary of Functional Requirements

This project involved designing a DC-DC Buck-Boost converter, which attached to an elliptical machine, generator, inverter, and grid. The converter converts DC input voltage from the generator to a bucked or boosted DC output voltage, which connects to an inverter. The inverter converts DC to AC, which returns to the grid. Currently, two previous DC-DC converter designs contain different results. The SEPIC topology design by Martin Kou resulted in a desired output DC voltage, but at the cost of efficiency below 80% [1]. Hilario's four switch converter achieved high efficiency (around 94%), but with limited input voltage [2]. So, this project's DC-DC converter must achieve high efficiency and the desired output voltage 36 ± 2V. Also, the converter must not hinder the elliptical machine's other hardware devices and functions. An example includes the machine's resistance levels remaining the same before and after installing the proposed converter.

## A.2 Primary Constraints

The following constraints affect this project's design approach:

- The converter must tolerate different voltage levels which users generate through the elliptical machines and must generate power to the bus through acceptable levels

- The converter and overall machine's system must follow electrical safety standards per the IEEE, PG&E, and NEC safety requirements, ensuring the end-users remain safe.
- The converter and the elliptical machine's other devices must operate compatibly.

The elliptical machine can generate 5V minimum, but the maximum voltage generated can exceed pass 65V when users apply large enough physical effort onto the machine. Previous EHFEM projects experimented between 5V and 65V, since end-users could typically generate these voltages through normal exercise routines. So, this project's converter must tolerate these expected voltages and higher voltages.

The elliptical machine's devices and converter must also operate compatibly. This includes no loading between devices and not exceeding the devices' maximum voltage, current, and power ratings [7, 8]. Loading can occur when a device's input resistance appears small to another device's output resistance. When loading occurs, the input resistance receives less power. If the input resistance appears large, then the input resistance receives more power. Thus, the Enphase inverter and converter must operate compatibly together, so the grid can receive the most power and not damage any devices.

Finally, the converter and overall machine's system must follow electrical safety standards. The IEEE, PG&E, and NEC provide the safety requirements and standards to ensure safety for end-users.

## A.3 Economic

| Buck-Boost DC-DC Converter | | | 2013 | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Deliverables | Name | Weeks Total | Sept/ Week 37 | 38 | 39 | Oct/ Week 40 | 41 | 42 | 43 | 44 | Nov/ Week 45 | 46 | 47 | 48 | Dec/ Week 49 | 50 | 51 | 52 | 53 | Jan/ Week 1 | 2 |
| Planning phase | | 5 | | 1 | 2 | 3 | 4 | 5 | | | | | | | | | | | | | | |
| Initial Documentation phase | | 11 | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | | | | | | |
| Research phase | | 5 | | | | | | | | 1 | 2 | 3 | 4 | 5 | | | | | | | | |
| Simulation phase | | 6 | | | | | | | | | | | | | 1 | 2 | 3 | 4 | 5 | 6 | | |
| Purchase Parts | | 2 | | | | | | | | | | | | | | | | | | 1 | 2 | |

FIGURE 78
INITIAL GANTT CHART, FALL 2013

| Buck-Boost DC-DC Converter | | | 2014 | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Deliverables | Name | Weeks Total | 53 | Jan/ Week 1 | 2 | 3 | 4 | Feb/ Week 5 | 6 | 7 | 8 | Mar/ Week 9 | 10 | 11 | 12 | 13 | Apr/ Week 14 | 15 | 16 | 17 | May/ Week 18 | 19 | 20 | 21 | Jun/ Week 22 | 23 |
| Second Documentation phase | | 13 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | | | | | | | | | | | |
| First Design and Test phase | | 7 | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | | | | | | | | | | | | | | |
| EE Department Wide Design Review | | 1 | | | | | | | | | 1 | | | | | | | | | | | | | | | |
| EE463 Report and Demo Device | | 1 | | | | | | | | | | | | 1 | | | | | | | | | | | | |
| Troubleshoot phase (for both First and Second Design and Test phases) | | 10 | | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | | | | | | | | | | |
| Second Design and Test phase | | 4 | | | | | | | | | | 1 | 2 | 3 | 4 | | | | | | | | | | | |
| Finalize Design phase | | 4 | | | | | | | | | | | | | | | 1 | 2 | 3 | 4 | | | | | | |
| Final Documentation phase | | 8 | | | | | | | | | | | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | | | |
| EE464 Report and Demo Device | | 1 | | | | | | | | | | | | | | | | | | | | | | | | 1 |
| ABET Senior Project Analysis and Expo | | 1 | | | | | | | | | | | | | | | | | | | | | | | | 1 |

FIGURE 79
INITIAL GANTT CHART, WINTER/SPRING 2014

Figures 4 and 5 show this project's proposed timeline, or Gantt Charts, measured in approximate weeks. Each deliverable estimates an extra week or more for considering unforeseen delays and mishaps. An example includes the deliverable "Purchase Parts" shown as two weeks, because delays from delivery companies may occur.

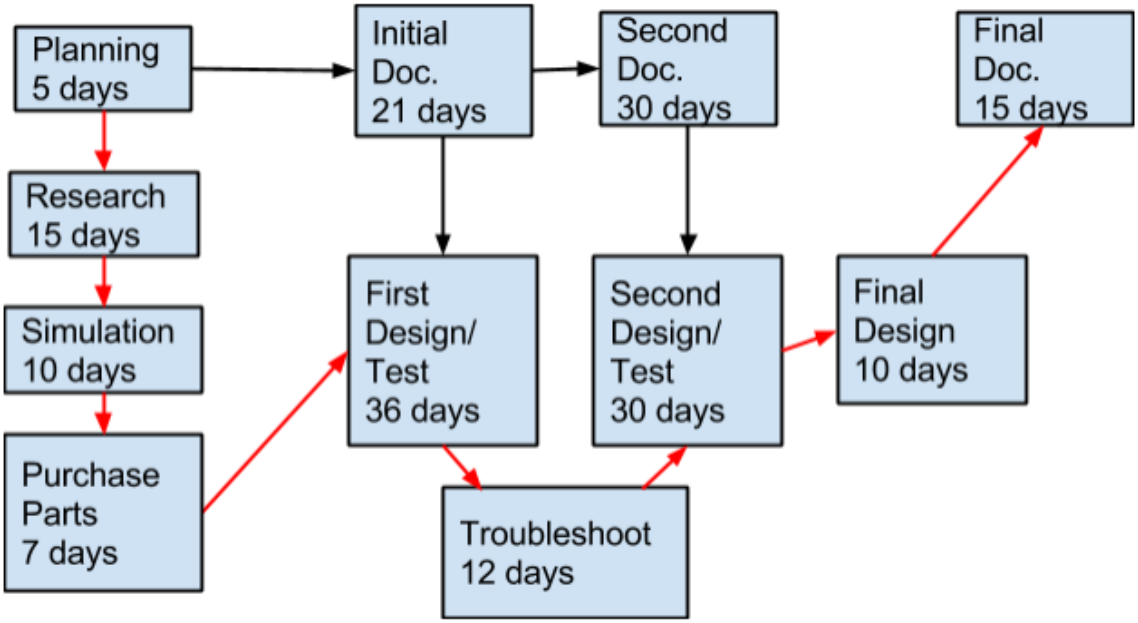


FIGURE 80
NETWORK DIAGRAM WITH CRITICAL PATH

TABLE XXIII
COST ESTIMATES

| | Quantity | Cost Per ($) | Total |
|---|---|---|---|
| Controller LT3791 | 3 | 6.79 | 20.37 |
| Power Diodes | 4 | 0.52 | 2.08 |
| Transistors | 4 | 2.83 | 11.32 |
| Inductor | 1 | 3.60 | 3.60 |
| Capacitors | 10 | 1.00 | 10.00 |
| Resistors | 12 | 0.25 | 3.75 |
| High Power Resistors | 3 | 4.00 | 12.00 |
| Heat Sinks | 3 | 4.00 | 12.00 |
| Labor | 210 (Hours) | 15 | 3150 |
| | | | |
| Total Costs | | | 3225.12 |

$$Cost = \frac{cost_a + 4 * cost_m + cost_b}{6} = \frac{\$2140 + 4 * \$3225.12 + \$4350}{6} = \$3231.75$$

Table XXIII represents the expected parts and labor costs. Estimating 1.5 labor hours per day, the labor hours total 210 hours per 140 days. Each labor hour, although not actually paid work, values around $15, bringing the total labor cost around $3150. The cost equation represents the optimistic, most expected, and pessimistic cost estimates. Optimistically, the minimum hours spent each day total 1 hour per day, or 140 hours ($2100). The parts would total $40, where heat sinks, transistors, and power diodes cost less than the expected costs. Pessimistically, the maximum hours spent each day total 2 hours per day, or 280 hours ($4200). The parts would total $150, where the heat sinks, power diodes, transistors, an inductor, capacitors, and high power resistors would cost more than the expected costs. Specifically, this project could demand more efficient heat sinks, specialized electrolytic capacitors and an inductor which handle higher voltages and currents, and power diodes containing higher voltage tolerances. Overall, the costs estimate around $3231.75.

Figure 6 shows the critical path, represented as red arrows. The critical path approximates around 140 days, or 20 weeks. The initial documentation works simultaneously with the research, simulation, and parts purchase phases. The second documentation works simultaneously with the first design and test phase and the troubleshoot phase.

The actual Gantt chart, the chart that shows what actually happened during the year, appears in Figure 81 and 82.

| Buck-Boost DC-DC Converter | | | 2013 | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Deliverables | Name | Weeks Total | Sept/ Week 37 | 38 | 39 | Oct/ Week 40 | 41 | 42 | 43 | 44 | Nov/ Week 45 | 46 | 47 | 48 | Dec/ Week 49 | 50 | 51 | 52 | 53 |
| Planning phase | | 5 | | 1 | 2 | 3 | 4 | 5 | | | | | | | | | | | |
| Initial Documentation phase | | 11 | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | | | |
| Research phase | | 10 | | | | | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |

FIGURE 81
ACTUAL GANTT CHART, FALL 2013

| Buck-Boost DC-DC Converter | | | 2014 | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Deliverables | Name | Weeks Total | 2 | 3 | 4 | Feb/ Week 5 | 6 | 7 | 8 | Mar/ Week 9 | 10 | 11 | 12 | 13 | Apr/ Week 14 | 15 | 16 | 17 | May/ Week 18 | 19 | 20 | 21 | Jun/ Week 22 | 23 |
| Simulation phase | | 20 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | | |
| Purchase Parts | | 2 | | | | | | | | | | | | | | | | | | | | 1 | 2 | |
| Second Documentation phase | | 11 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | | | | | | | | | | | |
| First Design and Test phase | | 3 | | | | | | | | | | | | | | | | | | | | 1 | 2 | 3 |
| EE Department Wide Design Review | | 1 | | | | | | | 1 | | | | | | | | | | | | | | | |
| EE463 Report and Demo Device | | 1 | | | | | | | | | | 1 | | | | | | | | | | | | |
| Troubleshoot phase (for both First and Second Design and Test phases) | | 2 | | | | | | | | | | | | | | | | | | | | | 1 | 2 |
| Third Documentation phase | | 10 | | | | | | | | | | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
| Finalize Design phase | | 4 | | | | | | | | | | | | | 1 | 2 | 3 | 4 | | | | | | |
| Final Documentation phase | | 1 | | | | | | | | | | | | | | | | | | | | | | 1 |
| EE464 Report and Demo Device | | 1 | | | | | | | | | | | | | | | | | | | | | 1 | |
| ABET Senior Project Analysis and Expo | | 1 | | | | | | | | | | | | | | | | | | | | | | 1 |

FIGURE 82
ACTUAL GANTT CHART, WINTER/SPRING 2014

The EHFEM project returns AC power back to the grid, thus lowering utility costs. So, one machine should pay for itself in some estimated time, including all the components, installation equipment, and labor costs. The components and labor costs estimate around $3231.75 for the first machine installation, based on the cost calculations. All the installation equipment or hardware tools cost around $75. All these costs include research and testing times, so factoring out these times make the actual cost for only the components, installation equipment, and labor become much lower than $3231.75.

The EHFEM project takes place within Cal Poly's Recreation Center, so the school pays for this product. The modified machines must pay off the long-term installation costs. Once the machines pay off those costs, the machines start paying back to the school through saving utility energy costs. Thus, implementing this project saves energy costs and also raises electricity conservation awareness for the students and faculty using the modified elliptical machines.

### A.4 Manufactured on a Commercial Basis

If this project manufactured through a commercial basis, each modified elliptical machine must not exceed $360, based on Braun's EHFEM proposal [3]. This proposal states that each modified machine pays off its implementation costs ($360) in 10 years when each machine operates at 80% DC-DC conversion efficiency and 90% inverter efficiency. Thus, each modified machine gains profit after 10 years if each machine efficiently converts power.

Achieving costs under $360 involves buying the most cheaply, durable, and environment-friendly components available. Since the elliptical trainers can cost around $2200 each and the installation costs should estimate below $360, then the total costs for each machine costs $2560. If one sold 1,000 units per year, then one gains $2,560,000 per year.

Users would spend $2560 plus any maintenance costs required to extend the machine's lifecycle. Pessimistically, replacing the machine's parts every 7.5 years means the maintenance costs estimate an extra $360 every 7.5 years, or $48 per year. Optimistically, replacing the parts every 15 years means the maintenance costs estimate $24 per year.

### A.5 Environmental

This project provides a "green" energy alternative, but the project does contain a few environmental issues. The renewable energy resource (physical exercise) meets electricity needs while not releasing harmful by-products. However, this project must contain minimum use of components, while ensuring maximum safety for end-users, because the components' materials include precious resources. Also, when retiring the machines for a better product, the machines' electronics must achieve proper disposition. If not disposed properly, the electronics could release harmful chemicals around the environment. Thus, minimum use of components ensures

less environmental impact both before and after the project's retirement. Also, minimum use of precious materials can sustain a better renewable resource, where scarce resources remain rarely used and manufactured when other environmental-friendly products become available.

### A.6 Manufacturability

Installation and implementation costs must remain low, or else the elliptical machines cannot pay off its manufacturing costs after 10 years. Thus, these manufacturing costs must consider future modifications, including improving efficiency and lowering maintenance labor. These modifications, however, must remain within the machine's confines, where these modifications must stay away from endangering end-users. So, when making improvements and adding additional circuitry, manufacturers must consider the machine's dimensions, which limits how many components install inside the machine.

Also, installing the DC-DC converter and other devices within the machine's confines remains difficult because the machine has limited room within its confines. While initial installation of only the DC-DC converter remains fairly simple to execute, adding more devices after initial installation can prove tedious and difficult when space within the machine remains an issue. Also, these added devices must not interfere with the machine's original devices.

### A.7 Sustainability

This project sustains the use of scarce resources through implementing physical exercise as a renewable resource, thus providing less environmental impact. Maintaining this product involves the product having long term usage, low maintenance, and minimum use of resources. The long term usage ensures the product can continue generating renewable energy and eliminate any

additional resources to create energy since physical exercise replaces the additional resources. Low maintenance ensures the product can last a long term, while using minimal resources improves the sustainability of the environment. Maintenance involves ensuring the electronics withstand long-term usage, where each electrical component must justify against costs after ten year operation. If any component must continually replace other old components, then this project fails paying itself off. Thus, minimum use of resources achieves the ten year operation runs smoothly and long-lasting components ensure low maintenance.

Upgrading the product would include increasing power efficiency, using more environment-friendly materials, and further lowering maintenance costs. Efficiency defines how much power outputs against power input. Ideally, inputting power (physical energy) means outputting exact amount of power (electrical energy). However, some energy remains lost since heat dissipation occurs through resistances. Today's efficiency design can only obtain between 80% and 90%, if using specialized components [1]. So, future modifications should consider improving efficiency, where ideally the future could contain better efficiency designs.

Environment-friendly materials ensure sustain use of precious resources. Thus, future modifications and upgrades must consider replacing any non-environmental friendly materials, or else this project could harm the environment when disposed of after the project's lifetime use. Further lowering maintenance costs require replacing all electrical components with cheaper, more durable, and more environmental-friendly components. Thus, this project can quickly pay itself off, withstand long-term usage, and remain environmentally-friendly. If this project did require high maintenance, costs would mainly pay the maintenance workers and this project's costs would rapidly increase.

### A.8 Ethical

Fulfilling ethical decisions must follow some ethical framework [27] and satisfy the IEEE Code of Ethics [28]. Using ICARE, provided through Santa Clara University's Markkula Center:

(1) Recognizing an Ethical Issue

(2) Obtaining Facts

(3) Evaluating Alternate Actions

(4) Making and Testing the Decisions

(5) Acting Out and Reflecting on the Outcome.

The ethical decisions recognized for this project involve providing safety among end-users, using expensive and non-harmful materials over cheaper and harmful materials, and establishing who receives monetary benefits from generating electricity through users' exercises. Once recognizing these issues, one must obtain facts about these issues. An example fact includes knowing what constitutes safety and how one obtains safety records or standards. Thus, safety includes following IEEE, NEC, and PG&E wiring standards. Even if more time and money expends this project, the standards must follow throughout the project and ensure safety. One can obtain facts through surveying stakeholders, consulting through professionals, and researching reliable online sources (IEEE website).

The next step evaluates alternate actions, where not one decision overwhelmingly trumps other decisions. Fulfilling this step requires evaluating several ethical frameworks; one could follow the Golden Rule and Kant's Categorical Imperative as ethical frameworks. An example ethical decision includes deciding whether one should follow either one wiring standard or fulfilling multiple standards. NEC and PG&E wiring standards follow different methods, and following both standards means obtaining these institutions' permissions and evaluations, which

takes time. If one had little time left, then one would make a decision of either following only one standard or several standards. Making this decision involves knowing all the facts about the issue and weighing the alternate decisions against IEEE code of ethics. The Golden Rule states one must treat others as one would like to be treated. So, one would most likely want maximum safety involved with any electronic device (i.e. no shocks, discharges, or burns should occur). The Categorical Imperative states one's actions must be seen as universal laws. So, an example universal law could include not hurting other people unless in retaliation. Thus, one must follow wiring standards to avoid potentially hurting people. Ultimately, safety must always follow through [27]. Following these first three steps, one now makes a decision and tests this decision through some preliminary course. An example includes telling someone one respects and knowing how someone would respond about the decision. The Cal Poly Recreation Center obtains this project and hopefully ensures money generated after a long-term usage. If the Recreation Center knew about the wiring decision, how would it respond? While this project must generate monetary benefits for the Cal Poly Recreation Center, thus lowering energy costs for the school, more time and money should expend this project for ensuring safety because this project must have long term usage, meaning monetary benefits gained outweigh paying any potential damages to users. So, following both NEC and PG&E wiring standards fulfills the safety standard and respects the Recreation Center's reputation. Finally, one now acts out this decision, ensuring all stakeholders remain safe and respected, and reflect upon the decision for future decision-making situations. Hopefully, following the two wiring standards ensure the maximum safety while also respect the Recreation Center's reputation.

While ensuring the wires follow wiring standards, this project's components must also follow an ethical decision of safe component usage. Using the framework example, cheaper and leaded

components saves money and gain monetary benefits quickly. But, the leaded components release harmful chemicals into the atmosphere, which affects end-users and the environment. Knowing these issues and facts, one must use non-leaded, albeit more expensive, components to ensure safety for users and the environment. Again, safety remains number concern throughout this project.

Lastly, establishing who receives monetary benefits from generating electricity remains questionable. Students and faculty exercise on the machines, but the Recreation Center would receive the monetary benefits instead of the users. However, the Recreation Center receives these benefits to lower its energy costs, and eventually paying back to the school where the students and faculty attend. Thus, both the school and users receive benefits from this project. Knowing these facts and issues, the monetary benefits should return to the Recreation Center only if the benefits only pay the energy costs. The users also obtain health benefit and awareness for using the exercise machines, so users do gain some benefits when using this project.

**A. 9 Health and Safety**

When modifying the elliptical machine, safety remains an ultimate concern because high, lethal voltage levels reside within the machines. The machine's devices must transfer energy while not physically or mentally affecting users. These negative effects include burning, shocking, or scarring the users. The devices must also include protective covering from liquids and food, which reside around the Recreation Center. So, shielding these devices from affecting users and getting affected by external substances remains a major concern.

Since this product attaches to an elliptical machine, users benefit improved physical health when using these machines. Raising awareness for generating renewable energy from exercise

machines encourages people to exercise more, allowing people to maintain or improve their health while saving costs and sustaining the environment.

### A.10 Social and Political

Since this project takes place within the Cal Poly Recreation Center, the students' and faculties' experiences on the modified machines must remain the same before and after the modifications. If the users' exercise experiences changed after the modifications, users find the machines unfamiliar and uncomfortable to use because the users must accommodate a change they didn't ask for. Also, the components installed within the machine must either remain unseen or visually appealing for users, since the machines should remain familiar and approachable.

The current trend involving finding "green" energy alternatives remains a concern around the world. The renewable energy from physical exercise fulfills this "green" aspect because, excluding the components used to modify the elliptical machine, no harmful by-products appear when generating energy through the machine. Thus, implementing this machine to gyms, and perhaps even homes, in the U.S. can provide people access and awareness to renewable energy.

### A.11 Development

This project involves many topics and concepts implemented through safety and high performance. An example includes Babaei's paper, which discusses improving the output voltage ripple (OVR) for buck-boost DC-DC converters [12]. An ideal DC output involves no ripples, but practical converters consider OVR because ripples occur nonetheless. Babaei discusses several techniques, including incomplete inductor supply mode, complete inductor

supply mode, discontinuous conduction mode, and continuous conduction mode. He also discusses the benefits and disadvantages each technique establishes in combinations and solo.

I learned much from Babei's paper when considering how ripple voltage affects my project, especially when the converter deals through fluctuating voltages. Since the generator's output voltage can fluctuate based through a user's exercise experience (a user not exercising through a steady pace), then Babei's paper helps establishing which kind of mode fixes the fluctuation.

The following paragraphs describe the Literature Search:

1. A. Emadi , A. Khaligh , Z. Nie , and Y. J. Lee, *Integrated Power Electronic Converters and Digital Control.* Boca Raton, FL, CRC Press/Taylor and Francis Group, 2009. [eBook] Cal Poly Kennedy Library.

   This book contains some general information about DC-DC converters and buck/boost topologies. So the information provides helpful ideas when constructing this project's DC-DC converter. According to Google Scholar, this book has been cited 21 times.

2. Kou, Martin, *Energy Harvesting from Elliptical Machines: DC-DC Converter Design Using SEPIC Topology. Cal Poly Digital Commons.* 2012. [Online] http://digitalcommons.calpoly.edu/theses/753/

   Kou's Master Thesis provides important issues this project's DC-DC converter should address, including loading issues and output current limiting circuitry. Kou's thesis entails reliable information since he presented his thesis to the Cal Poly EE department, including Professors Braun, Taufik, and Nafisi, and submitted his presentation for peer-review.

3. Hilario, Alvin J., *Energy Harvesting from Elliptical Machines Using Four-Switch Buck-Boost Topology. Cal Poly Digital Commons.* 2011. [Online] http://digitalcommons.calpoly.edu/theses/511/

   Both Hilario's Master Thesis and this project's proposal use a DC-DC converter controller. So, Hilario provides this project potential design techniques. Hilario's thesis entails reliable information exactly as Kou's thesis entails reliable information.

4. J. Yuen; M. Lum; C. Cinkornpumin; J. Chan. "Energy Harvesting from Exercise Machines (EHFEM) Self-generator Elliptial Machine," Cal Poly Digital Commons. 2008. [Online]. http://digitalcommons.calpoly.edu/eesp/12

   This thesis provides the EHFEMs' previous projects' costs, parts, and designs used. Thus, this thesis provides what worked, what needs improvement, etc. Since senior projects after this presented thesis used the thesis's data, this thesis has some credibility because the senior projects followed up on this thesis's data.

5. Taufik and D. Dolan, *Introduction to Power Electronics*. Cal Poly State University, San

Luis Obispo. 11th Revision, 2013.

This lecture notebook provides basic DC-DC conversion functions and performance measurements, or the building blocks for creating the DC-DC converter. The notebook also includes boost and buck conversion topologies. And since multiple students designed or created senior projects, including Kou and Hilario, using this notebook, then this notebook has reliable information.

6. Linear Technology. Datasheet – LT3791- 60V 4-Swtich Synchronous Buck-Boost LED Driver Controller, 2012. [Online] http://cds.linear.com/docs/en/datasheet/3791fa.pdf

This project uses the LT3791 controller, so this necessary datasheet provides the controller's characteristics and limitations. This datasheet provides reliable information since Linear Technology issued this datasheet after testing under certain typical conditions (Vin=12V, $T_A$=25°C, etc.).

7. Enphase Energy. Datasheet - Enphase Micro-Inverter, M175-24-240. [Online] http://enphase.com/downloads/8261_Datasheet_24_32.pdf

The Enphase inverter datasheet provides maximum input voltage and current characteristics, which affect this project's DC-DC operation because the DC-DC converter output must not exceed the inverter's maximum inputs. Kou's and Hilario's senior projects used this datasheet to test the inverter's maximum input capabilities, so this datasheet provides reliable information since other people used and proved the datasheet's information.

8. Precor, "EFX® 546i Elliptical Fitness Crosstrainer™ Specifications," 2010. [Online] http://www.precor.com/en-us/home/products/catalog/product/view/id/33#

These specs contain the elliptical machine's dimensions, weights, and power requirements. The modified elliptical machine must operate under these constraints, so these specs provide important information. A given 546i elliptical machine matches the specs. If the machine didn't match the specs, then the company Precor has lied and its reputation tarnishes. So, these specs should have reliability.

9. Yoshida, Yutaka, *DC-DC Converter*, U.S. Patent 7,061, 213. Date of Patent Jun. 13, 2006.

This patented item involves a DC-DC converter overcoming the semiconductor switching losses. This project's DC-DC converter considers these losses important since any losses affect the power efficiency of the converter. Patent cited 32 times, according to Google Scholar.

10. E Babaei, Mahmoodieh, M.E. Seyed, and Mahery, H. Mashinchi, *Operational Modes and Output-voltage-ripple Analysis and Design Considerations of Buck-boost DC-DC Converters.* Published IEEE Transactions on Industrial Electronics, volume 59 issue 1 (Jan 2012), pages 381-390, 2012.

This journal article discusses improvements on previous analysis and design considerations of buck-boost DC-DC converters, specifically the output voltage ripple (OVR). An ideal DC output involves no ripples, but practical converters consider OVR, so this article helps discover new designs or techniques overcoming any OVR. Article cited 15 times according to Google Scholar.

# APPENDIX B – DC-DC CONVERTER DESIGN EXAMPLES

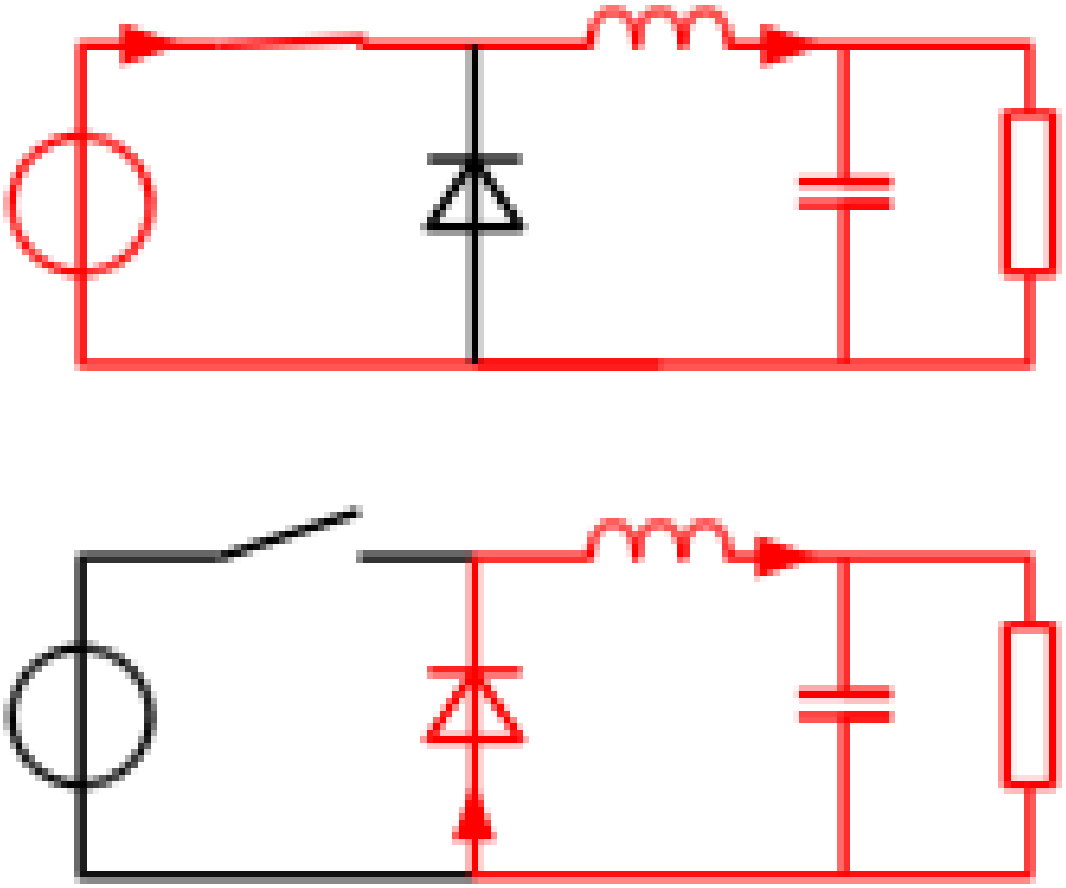

FIGURE 83
BUCK CONVERTER EXAMPLE - ON-STATE (TOP) AND OFF-STATE (BOTTOM)

As seen in Figure 83, a buck converter bucks or lowers $V_{IN}$ based on the switch's duty cycle. The following equation shows the calculation between $V_{IN}$ and $V_{OUT}$.

$$Vout = Vin * D \quad (23)$$

Where D is the switch's duty cycle. Compared to the four-switch converter, MOSFETS Q1 and Q2 represent the switch and diode in Figure 83. Thus, for the four-switch converter to operate in buck mode, Q3 stays off, Q4 stays on, and Q1 and Q2 alternate.

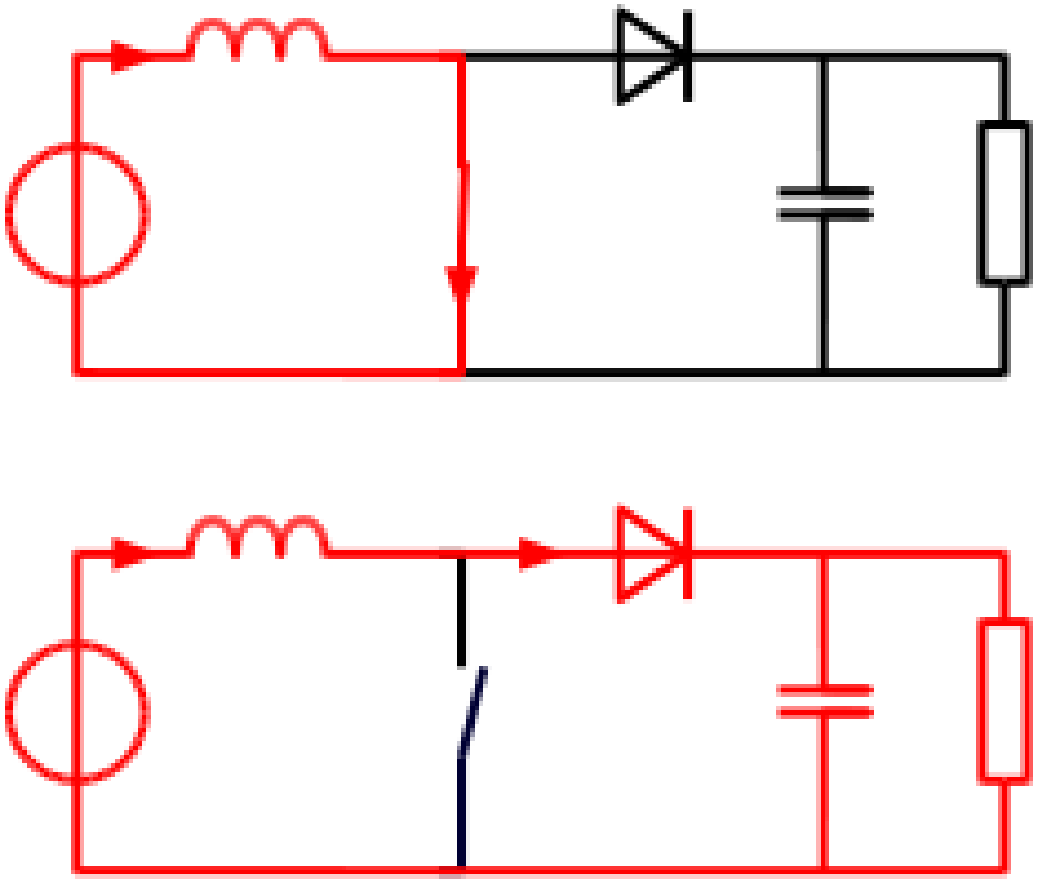

FIGURE 84
BOOST CONVERTER EXAMPLE - ON-STATE (TOP) AND OFF-STATE (BOTTOM)

As seen in Figure 84, a boost converter boosts $V_{IN}$ based on the switch's duty cycle. The following equation shows the calculation between $V_{IN}$ and $V_{OUT}$.

$$Vout = \frac{Vin}{1 - D} \quad (24)$$

Where D is the switch's duty cycle. Compared to the four-switch converter, MOSFETS Q3 and Q4 represent the switch and diode in Figure 84. Thus, for the four-switch converter to operate in boost mode, Q2 stays off, Q1 stays on, and Q3 and Q4 alternate.

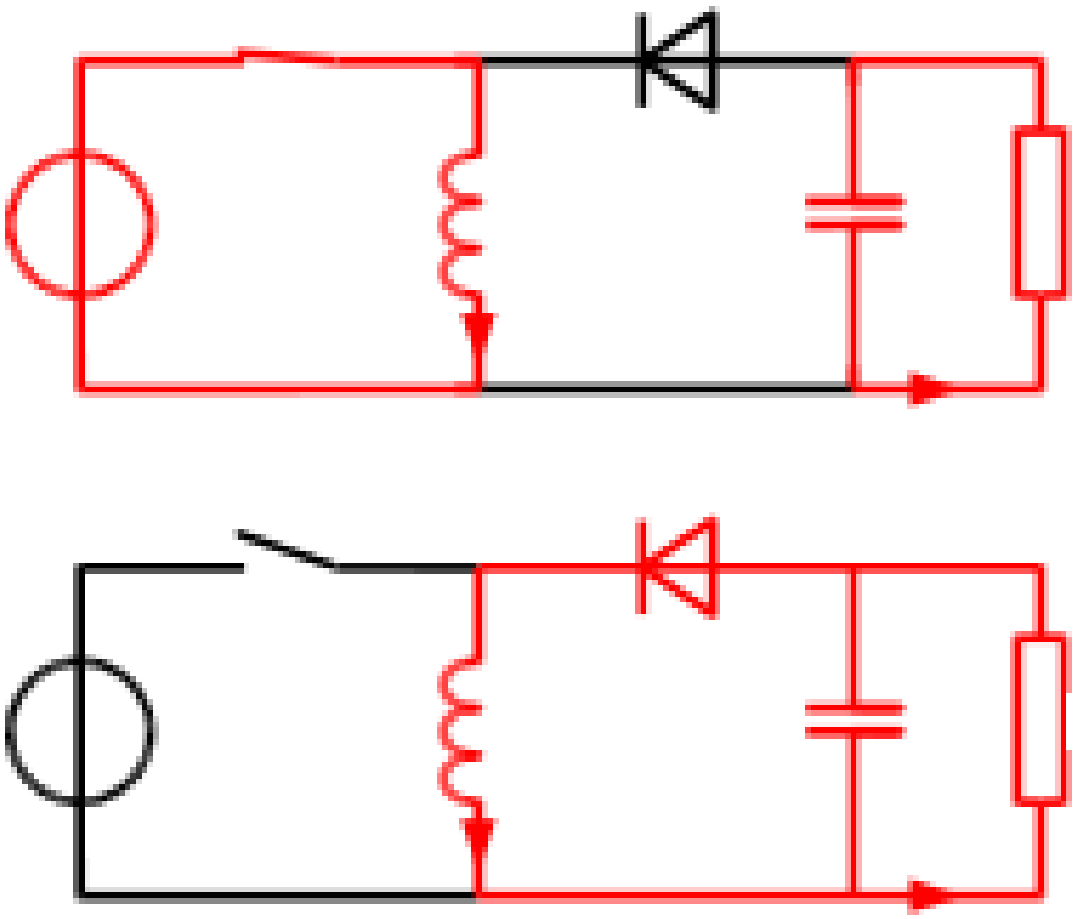

FIGURE 85
BUCK-BOOST CONVERTER EXAMPLE - ON-STATE (TOP) AND OFF-STATE (BOTTOM)

As seen in Figure 85, a buck-boost converter either bucks or boosts $V_{IN}$ based on the switch's duty cycle. The following equation shows the calculation between $V_{IN}$ and $V_{OUT}$.

$$Vout = \frac{Vin * D}{1 - D} \quad (25)$$

Where D is the switch's duty cycle. Compared to the four-switch converter, Figure 85 doesn't accurately represent the four-switch converter in buck-boost mode. The ICs LT3791 and LT3791-1 determined that buck-boost mode occurs when $V_{IN}$ approximates to $V_{OUT}$. Thus, for the four-switch converter to operate in buck-boost mode, the MOSFETs have to alternate from

each other. For example, Q1 and Q4 both turn on while Q2 and Q3 stay off. Then, Q3 turns on and Q4 turns off, where Q1 and Q3 stay on for some time. Then, Q4 turns back on and Q3 turns off, where Q1 and Q4 stay on for some time. Then, Q2 turns on and Q1 turns off for some time. Then, Q1 turns back on and Q2 turns off, where Q1 and Q4 stay on and the cycle continues again. Figure 86 shows an example buck-boost operation.

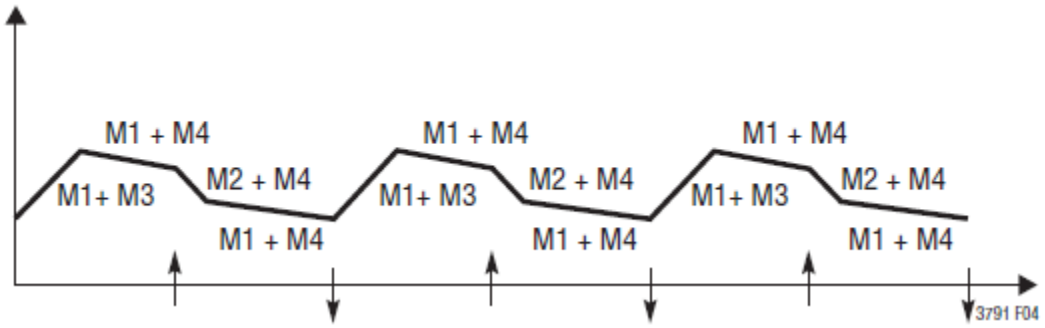


FIGURE 86
EXAMPLE BUCK-BOOST OPERATION

# References


[1] M. Kou. (2012). *Energy Harvesting from Elliptical Machines: DC-DC Converter Design Using SEPIC Topology.* [Online]. Available: Cal Poly Digital Commons http://digitalcommons.calpoly.edu/theses/753/

[2] A. J. Hilario. (2011). *Energy Harvesting from Elliptical Machines Using Four-Switch Buck Boost Topology. Cal Poly Digital Commons.* [Online]. Available: Cal Poly Digital Commons http://digitalcommons.calpoly.edu/theses/511/

[3] D. Braun. (2010). *Soft Switching DC-DC Conversion to Harvest Exercise Machine Electricty EISG Proposal*. Available e-mail: dbraun@calpoly.edu Message: Get Braun's Project Proposal.

[4] J. Yuen, et al. (2008). *Energy Harvesting from Exercise Machines (EHFEM) Self-generator Elliptial Machine.* [Online]. Available: Cal Poly Digital Commons http://digitalcommons.calpoly.edu/eesp/12

[5] A. Emadi , et al. *Integrated Power Electronic Converters and Digital Control.* Boca Raton, FL: CRC Press/Taylor and Francis Group, 2009. [eBook]; Available: Cal Poly Kennedy Library.

[6] Taufik, et al, *Introduction to Power Electronics*, 11th Revision. Cal Poly State University, San Luis Obispo. 2013.

[7] Linear Technology. (2012) Datasheet – "LT3791- 60V 4-Swtich Synchronous Buck-Boost LED Driver Controller," Linear Technology. [Online]. Available: http://cds.linear.com/docs/en/datasheet/3791fa.pdf

[8] Enphase Energy. (2008). Datasheet – "Enphase Micro-Inverter, M175-24-240," Enphase Energy. [Online]. Available: http://enphase.com/downloads/8261_Datasheet_24_32.pdf

[9] R. Ford and C. Coulston, *Design for Electrical and Computer Engineers*. New York City: McGraw-Hill, 2007, ch. 3, sec. 2, p. 37.

[10] *IEEE Std 1233, 1998 Edition*. p. 4 (10/36), DOI: 10.1109/IEEESTD.1998.88826.

[11] Precor. (2010). "EFX® 546i Elliptical Fitness Crosstrainer™ Specifications." [Online]. Available: http://www.precor.com/en-us/home/products/catalog/product/view/id/33#

[12] M. E. Babaei, et al., *Operational Modes and Output-voltage-ripple Analysis and Design Considerations of Buck-boost DC-DC Converters,* IEEE Trans. Ind. Electron., volume 59, no. 1, pages 381-390, Jan. 2012.

[13] R. Turner, et al. *DC-DC Converter Input Protection System for the Energy Harvesting from Exercise Machines (EHFEM) Project.* [Online]. Available: Cal Poly Digital Commons http://digitalcommons.calpoly.edu/eesp/214/

[14] S. Chu and D. Yoo, *BUCK-BOOST DC-DC CONVERTER with INPUT PROTECTION SYSTEM FOR THE ENERGY HARVESTING from EXERCISE MACHINES PROJECT.* June 2014.

[15] Y. Yoshida, "*DC-DC Converter*," U.S. Patent 7 061 213, Date of Patent June 13, 2006.

[16] Linear Technology. (2012) Datasheet – "LT3791-1 - 60V 4-Swtich Synchronous Buck-Boost Controller," Linear Technology. [Online]. Available: http://www.linear.com/product/LT3791-1

[17] Wurth Electronics. Datasheet - "Inductor Power 10uH 21A SMD," Wurth Electronics. [Online]. Available: http://www.digikey.com/product-detail/en/74435581000/732-4235-1-ND/3672794

[18] IXYS Datasheet - "TrenchMV Power MOSFET IXTH180N10T," IXYS Corporation. [Online]. Available: ixdev.ixys.com/DataSheet/9eb2cdbc-abd0-45fc-9422-4c3d8305fcd7.pdf

[19] D. F. Poeth, "Introduction to Surface Mount Technology and Surface Mount Devices for the Small Manufacturer and Hobbyist: Prototype Manufacturing, Rework, and Repair Techniques." CQ Magazine. April, 2003. [Online]. Available: http://poeth.com/smtmfg.htm

[20] I. Poole, "What is SMT Surface Mount Technology - Tutorial." Radio-Electronics. [Online]. Available: http://www.radio-electronics.com/info/data/smt/what-is-surface-mount-technology-tutorial.php

[21] W. S. Lee, J. Yang, T. Yang, C. Y. Su, Y. L. Hu, Yageo. "Ultra High-Q NPO MLCC with Ag Inner Electrode for Telecommunication Application," Passive Components Industry. May/June 2004, Vol. 6, issue 3, page 27.

[22] M. Kahn. "Multilayer Ceramic Capacitors - Materials and Manufacture," AVX Corporation. Myrtle Beach, SC.

[23] K. Dennehy. "For metals of the smartphone age, no Plan B," Yale News. [Online]. Available: http://news.yale.edu/2013/12/02/metals-smartphone-age-no-plan-b

[24] Linear Technology, Design Tools. [Online]. Available: http://www.linear.com/product/LT3791#simulate

[25] Renesas. (2013) Datasheet – “RJK0651DPB,” Renesas. [Online]. Available: http://am.renesas.com/products/discrete/pmosfet/device/RJK0651DPB.jsp

[26] S. R. Euston and W. E. Gibson, "The Ethic of Sustainability," *Earth Ethics* **6**, 1995 p. 5-7.

[27] Santa Clara University. (2012). *A Framework for Thinking Ethically*. [Online]. Available: http://www.scu.edu/ethics/practicing/decision/framework.html

[28] IEEE. (2013).*7.8 IEEE Code of Ethics.* [Online]. Available: http://www.ieee.org/about/corporate/governance/p7-8.html