Design of a Low-Cost Underwater Acoustic Modem

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***Abstract*—There has been an increasing interest in creating short-range, low data rate, underwater wireless sensor networks for scientific marine exploration and monitoring. However, the lack of an inexpensive, underwater acoustic modem is preventing the proliferation of these sensor networks. Thus, we are building an underwater acoustic modem starting with the most critical component from a cost perspective—the transducer. The design substitutes a commercial transducer with a homemade transducer using cheap piezoceramic material and builds the rest of the modem's components around the properties of the transducer to extract as much performance as possible. This letter describes the high level design, and cost and power characteristics of each of the major modem components: the transducer, the analog transceiver, and the digital signal processor of our modem prototype.**

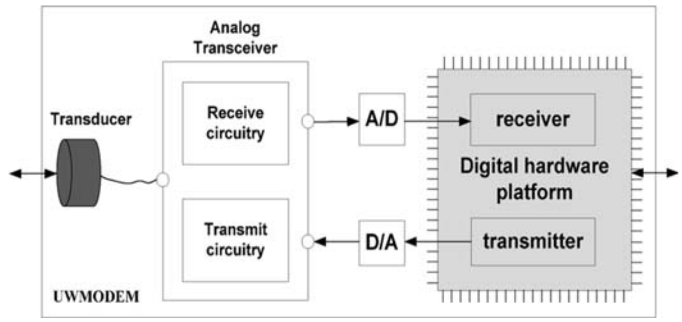

Fig. 1. Major components of an underwater acoustic modem.

I. Introduction

THERE is increasing interest in the design and deployment of underwater acoustic communication networks. For example, the persistent littoral undersea surveillance network (PLUSNet) demonstrates multisensor and multivehicle anti-submarine warfare (ASW) by means of an underwater acoustic communications network [1]. A short-range shallow water network to monitor pollution indicators in Newport Bay, CA, is proposed in [2]. A network of acoustic modems akin to motes is proposed for low power, short-range acoustic communications for seismic monitoring [3]. A swarm of acoustically networked autonomous drifters is envisioned to monitor phenomena as they are subjected to ocean currents [4]. The proposed underwater communication networks need access to tens to hundreds of inexpensive, low-power underwater acoustic modems, but existing commercial modems are too expensive and power consuming to be practical for these applications [5]. For example, Linkquest, Benthos, and DSPComm underwater modems all cost more than \$8000 dollars [6]–[8], and require a minimum of 4 W transmit power. In order to make more short-range underwater acoustic communication networks a reality, the cost and power consumption of underwater acoustic modems must come down.

As shown in Fig. 1, underwater acoustic modems consist of three main components: an underwater transducer, an analog transceiver, and a digital hardware platform for control and signal processing. The most costly component is the underwater transducer as commercially available underwater omnidirectional transducers (such as those seen in existing research modem designs [9]–[11]) cost from \$2000 to \$3000. Therefore, much of the design for a low-cost modem lies in finding an appropriate substitute for the custom commercial transducer. Jurdak *et al.* substituted the transducer with generic, inexpensive speakers and microphones, but were only able to obtain a data rate of 42 bits per second (bps) for a transmission range of 17 m [12]. Benson *et al.* substituted a custom transducer with a commercially available fish finder transducer (which costs \$50 dollars), but were only able to obtain a data rate of 80 bps for a transmission range of 6 m [13].

Thus, in this letter we present an overview of the design of an underwater acoustic modem starting with the most critical component from a cost perspective—the transducer. The design substitutes a commercial underwater transducer with a homemade underwater transducer using cheap piezoceramic material and builds the rest of the modem's components around the properties of the transducer to extract as much performance as possible. The goal of the design is to provide a low-cost, underwater acoustic modem that will be suitable for short-range sensor network applications.

The rest of this letter describes the high level design, cost and power characteristics of each of the major modem components: the transducer (Section II), the analog transceiver (Section III), and the digital signal processor (DSP) (Section IV). We conclude with a summary of the cost and power characteristics of the full design and a discussion of future work in Section V.

Fig. 2. From left to right: The raw piezoelectric ring ceramic, the potted ceramic, and the transducer in the potting compound mounted to a prototype plate to be attached to a modem housing.

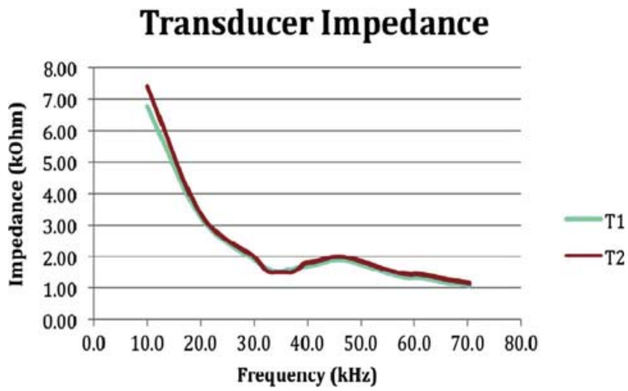

Fig. 3. Two transducers' (T1, T2) impedance at various frequencies. The resonant frequency occurs where the impedance first reaches a minimum.

II. Transducer

Underwater transducers are typically made from piezoelectric materials—materials (notably crystals such as lead zirconate titanate and certain ceramics) that generate an electric potential in response to applied mechanic stress and produce a stress or strain when an electric field is applied. The piezoelectric transducer needs to be encapsulated in a potting compound to prevent contact with any conductive fluids (Fig. 2). Commercial transducers are expensive, on the order of thousands of dollars, due to time-consuming characterization and the subsequent optimization of the analog circuitry, which is further exacerbated by low volume production. However, the raw piezoelectric materials themselves are not very expensive and alternative cheaper, less accurate ways of characterizing and manufacturing the transducers exist. The key to our low-cost design is to forego a commercial underwater transducer, and use a homemade one built from low-cost piezoelectric material. The rest of the system is built around the properties of this inexpensive transducer to extract as much performance as possible.

Underwater transducers are typically omnidirectional in the horizontal plane and do not transmit in the vertical plane to reduce reflections off the surface and bottom [14]. This is especially important for shallow water communications. Our transducer uses a radially expanding ring that provides 2-D omnidirectionality in the plane perpendicular to the axis. Our transducer makes use of a $10 dollar Steminc model SMC26D22H13 SMQA lead zirconate titanate (PZT) ceramic ring and a two-part urethane potting compound manufactured by Cytec Industries (Fig. 2). This particular potting compound was chosen because it has a density identical to that of water, which provides for efficient mechanical to acoustical energy coupling the water. Experimental tests have shown the ceramic maintains a linear output response up to 1000 V and 50 W. Frequency response tests of two of our transducers (Fig. 3) indicate that the resonant frequency of the transducer is 35 kHz with a $\sim$6 kHz bandwidth. Calibration tests giving the transducer's transmitting voltage response (TVR) and receiving voltage response (RVR) indicate it produces 140 dB re uPa/V/m at 35 kHz and receives -195 dB re V/1 uPa. When produced in large quantities, the estimated cost of the entire transducer including ceramic, potting, and labor is less than $50 dollars.

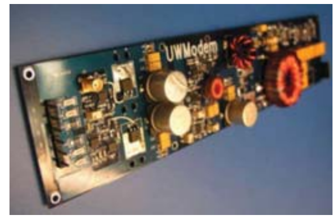

Fig. 4. Analog transceiver.

III. Analog Transceiver

The analog transceiver (Fig. 4) consists of a high power transmitter and a highly sensitive receiver both of which are optimized to operate in the transducer's resonant frequency range. When produced in large quantities, the estimated cost of the transceiver is $125 dollars. The transmitter and receiver portions of the analog transceiver are described in more detail in the following subsections.

A. *Transmitter*

The transmitter was designed to operate for signal inputs in a range from 0 to 100 kHz. The architecture is unique as it consists of two different amplifiers working in tandem. The primary amplifier is a highly linear Class AB amplifier that provides a voltage gain of 23 while achieving a power efficiency of about 50%. The output of the Class AB amplifier is connected to current sense circuitry that in turn controls the secondary amplifier, which is a Class D switching amplifier. The Class D amplifier is inherently nonlinear, but possesses an efficiency of approximately 95%. With both of the amplifiers driving the load and working together *in parallel*, the transmitter achieves a highly linear output signal while maintaining a power efficiency greater than 75%. Because of its high linearity, the transmitter may be used with any modulation technique that can be programmed into the digital hardware platform.

A power management circuit is provided to adjust the output power in real-time to match it to the actual distance between transmitter and receiver. The ability to provide a low-power output has several important benefits: less interference for nearby ongoing communications; reduced noise pollution; and considerable power savings. The current configuration of the transmitter is equipped with a power management system that can switch between output levels of 2, 12, 24, and 40 W, which is efficiently coupled into the transducer in over its operating frequencies. The power management system has been designed so that the transmitter will maintain maximum efficiency over this wide range of power output levels. The system is controlled by a low-current 5 V signal from the digital hardware platform so that the power may be dynamically controlled for different operating conditions.

B. Receiver

The receiver's architecture consists of a set of narrow (high-Q) filters with high gain. These filters are based on biquad band-pass filters, and essentially combine the tasks of filtering and amplification. The receiver is configured so that it only amplifies signals around 35 kHz (to match the resonant frequency of the transducer), while attenuating low frequencies at a rate of 120 dB per decade and high frequencies at rate of 80 dB per decade. The receiver must be able to amplify only the frequencies of interest because of the large amount of noise associated with underwater acoustic signals. The current receiver configuration consumes about 375 mW when in standby mode and less than 750 mW when fully engaged. The relatively high power consumption [in comparison to that of the Woods Hole Oceanographic Institute (WHOI) Micromodem (200 mW)] is a result of the receiver's high gain (65 dB) which is capable of sufficiently amplifying an input signal as small as 10 mcV allowing the receiver to pick up signals at longer distances. An ultralow-power wake up circuit will be added to the receiver to considerably reduce power consumption. A few receiver component values can be changed to widen its bandwidth (but decrease its gain) to allow for transmission of modulation schemes that require more bandwidth.

IV. Digital Signal Processor

Our digital hardware platform makes use of reconfigurable hardware, particularly a field-programmable gate array (FPGA), for all the digital signal processing and control required for the modem. Reconfigurable devices provide a suitable digital hardware platform for the low-cost, low-power underwater acoustic modem as they strike a balance between solely hardware and solely software solutions. They have the programmability and nonrecurring engineering costs of software with performance capacity and energy efficiency approaching that of a custom hardware implementation [17]. Reconfigurable systems are known to provide the performance needed to process complex digital signal processing applications and especially provide increased performance benefits for highly parallel algorithms [15]–[18]. Furthermore, they are programmable allowing the same device to be used to implement a variety of different communication protocols. Unfortunately, they require substantially longer design time than a DSP.

We selected to implement frequency shift keying as our first physical layer communication protocol as it is a simple, but robust modulation scheme that requires a small bandwidth (to match the characteristics of our transducer and analog circuitry), and has been widely used in underwater communications over the past two decades due to its resistance to time and frequency spreading of the underwater acoustic channel [9], [19]. Our design platform is flexible and can be used to accommodate other modulation schemes in the future.

Table I shows the modem's time and frequency parameters. The "mark" frequency represents the frequency used to represent a digital "1" when converted to baseband and the "space" frequency represents the frequency used to represent a digital "0" when converted to baseband. The sampling frequency is used for sending and receiving the modulated waveform on the carrier frequency while the baseband frequency is used for all

TABLE I
FSK Modem Parameters

Properties	**Assignment**
Modulation	FSK
Carrier frequency	35 kHz
Mark frequency	1 kHz
Space frequency	2 kHz
Symbol duration	5 ms
Sampling Frequency	192 kHz
Baseband Frequency	16 kHz

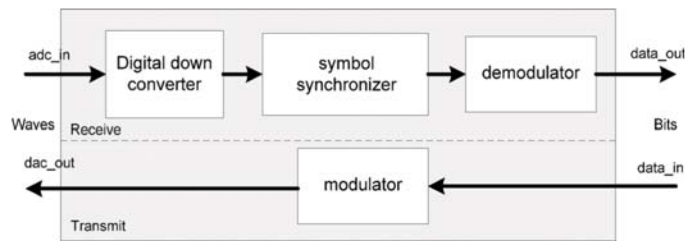

Fig. 5. Block diagram of a digital underwater acoustic modem.

TABLE II
FPGA Resource Usage

	Occupied slices	**LUTs**	**BRAMs**
Modulator	95	184	9
DDC	284	541	9
Demodulator	1025	1980	1
Synchronizer	12000	22101	2

baseband processing. These frequencies were selected to provide sufficient oversampling of the desired frequency component while being integer multiples of one another.

Fig. 5. illustrates a block diagram of our FPGA implementation of an FSK modem. The most complicated block of the modem is the symbol synchronizer which is used to locate the correct start of the data sequence to set accurate sampling and decision timing for subsequent demodulation. The synchronizer is based on correlation with a known reference sequence (a 15-bit Gold code translated to an FSK waveform where a "-1" is represented with the space frequency and a "1" is represented with the mark frequency). When the reference and receiving sequence exactly align with each other, the correlation result reaches a maximum value and the synchronization point is located. Details of the symbol synchronizer's implementation can be found in [20].

The design was implemented and successfully tested on a DINI Group DNMEG AD-DA evaluation board [21]. Hardware simulation results with packet lengths of 10 000 symbols achieved a bit error rate of 10^{-2} at 10 dB SNR. Transmitting at 35 kHz, given a transmit source level of 170 dB re 1 uPa and a noise level of 50 dB re 1 uPa, using the passive sonar equation with no directivity index, the signal may obtain 10 dB SNR at 1140 m. Packets of 100 symbols were sent underwater in a 12-inch plastic bucket and achieved 0% bit error rate.

Table II shows the FPGA hardware resources required for the components of the acoustic modem design with standard optimization. These resources are reported for a Xilinx Spartan 3 xc3s4000 FPGA. The power consumption, determined by XPower Estimator 9.1.03, is 0.379 W. The design offers a

TABLE III
ESTIMATED LARGE VOLUME COSTS

	Cost ($)
Transducer	50
Transceiver	125
Digital Components	75
Batteries	100
Housing	150
Power Supply	100
Total	**600**

TABLE IV
MODEM POWER CHARACTERISTICS

	Power (W)
Analog Transmitter	2, 12, 24, 40
Analog Receiver	0.75
Digital Modem	0.379
ADC	TBD
DAC	TBD

compact implementation capable of fitting into a low-power device that costs less than $70 dollars.

V. CONCLUSION

We have described the major design components of our prototype low-cost, underwater acoustic modem intended for short-range, low data rate sensor network applications. Currently, the digital hardware platform has been tested and supports data rates of up to 200 bps with 10^{-2} bit error rate at a low signal to noise ratio (SNR) of (10 dB). Initial in-water tests of the transducer and analog transceiver in Mission Bay, CA, indicate our design is capable of detecting a signal at distances greater than 350 m. We are currently developing a power supply board, battery pack, and watertight housing (that can withstand pressures at depth of up to 100 m) to be able to test the modem in the open ocean in order to assess its performance. Table III provides cost estimates for a fully packaged underwater modem and Table IV summarizes its current power consumption.

The power consumption of the analog-to-digital converter (ADC) and digital-to-analog converter (DAC) are specified to be determined (TBD) as the devices on our evaluation board are over specified and too power consuming for our low-power design. In the future, to further reduce power consumption, we plan to explore the possibilities to provide signal detection at even lower power levels. This is paramount to building a modem that has low listening power, which is also a key requirement to ensure long lifetime on a limited battery supply. We plan to eventually utilize a design that has a programmable gain, which is dynamically controlled by the digital hardware platform. In addition, further changes to the circuit design of the transceiver will be made to further increase its efficiency.

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