

Parallel AC-AC Converters Using Stationary Master Slave Control

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Abstract - This study proposes parallel ac-ac converters using Stationary Master Slave Control with Sinusoidal Pulse Width Modulation to achieve voltage regulation and equal current sharing among parallel generators such that it minimizes the total production cost. Development of Pspice model representing the parallel ac-ac converters is presented and then simulated. In addition, computer simulations are also used to perform robustness study on the parallel converters.

I. INTRODUCTION

In the operation of generators, it is a common practice to connect more than one generator in parallel to fulfill load demand. This action has several good reasons such as the ability to supply more power to a load than one generator can produce, to take a generator off-line for repairs without interrupting the power supplied to the load, and to provide redundancy in the event of a failure in one of the generators such that the others may continue to supply power without interruption to the load.

Since the 1980's, researchers have extensively studied the possibility to adapt microturbine-powered electric generators or simply called turbogenerators, for other applications besides its original use in aircraft. They have tried for example to install turbogenerators in U.S. army tanks, to utilize turbogenerators for electric power and water-heating cogeneration systems for the U.S. Gas Research Institute, and to apply turbogenerator technology to power up future hybrid electric vehicles. The most recent development on turbogenerator application, however, has been its potential implementation and commercialization as a small-scale effective and clean electric power generation system for both industrial and residential uses.

Along with the revolution of turbogenerator technology for building a pint-size power plant, there is a need to further

investigate how several units of turbogenerators can be connected in parallel to achieve a given level of output power. This is necessary since the turbogenerator itself despite its miniature size can only produce tens of kilowatts per unit at present time. A typical unit, which is currently available in the market for an instance, produces 30KW at normal operating conditions, although a higher output power is under development and is near its finishing stage. Since the turbogenerator is a 2-pole permanent magnet generator running at speeds of up to 96,000 rpm, it produces a frequency output of up to 1600Hz which is much higher than the standard 60Hz needed for most applications. Therefore, parallel converters are also needed to convert the high frequency output to a frequency that is required by the load. More importantly, the parallel converters should also be capable of performing equal current sharing among the parallel turbogenerators. This equal current sharing also means equal share of power to supply the load since identical turbogenerators being connected in parallel have identical voltage. Furthermore, the equal sharing performance is significant due to the fact that it leads to an economically optimal solution for production cost of electricity of the parallel system.

Parallel converters require an explicit equal current sharing mechanism to ensure even distribution of current and thermal stresses among the modules. Most of the studies reported recently concentrate on the development of control schemes for parallel dc-dc converters in which the power converter modules share the same load. Different approaches, with various complexities and current sharing performances, have been proposed, developed, and analyzed. The basic parallel control scheme is the droop method [1], [2]. Voltage droop is produced by using the output current to adjust the reference voltages, which are used to program the output impedance of each power converter module in order to achieve load sharing. Poor load regulation is found to be a major deficiency of the droop method, and therefore it is not suitable for applications where a tight regulation is required. Another scheme known as active current sharing ensures the desired current sharing by adjusting the

reference voltages of the voltage feedback error amplifiers of the individual modules so that the deviations of the modules' current from the average current are eliminated. Variations of this schemes include the so called "Democratic" scheme, where modules share currents in proportion to their ratings [3], [4], and the Master Slave Control scheme where a master converter is used to achieve the output voltage regulation through the voltage feedback loops [5], [6].

For ac-ac application, there exist several current sharing control schemes that are being used in applications today. Droop method [1] is one example that is known to have a very simple implementation especially when tight load regulation is not required. However, for the application where tight regulation is expected, such as that of turbogenerators, the droop method is not well suited because it will regulate the load voltage poorly in addition to its known steady state current imbalances and its sensitivity to voltage source drift. The Ring method [8] is another known control scheme that has the advantage in reducing the connection to the Master Converter, but with a more complex circuitry and thus relatively costly circuits as the tradeoffs. Another method is the Priority Rotating Window [8] scheme whereby no master unit is predetermined and thus it improves redundancy and reliability. The shortcoming however is not less crucial since the topology involves increased amount of interconnections. This is true since one module will have $n-1$ inputs and 1 output, where n is the number of modules in parallel. This, in turn, increases the cost.

Another option is to use the Stationary Control [7], which to date has only been used for dc-dc. This method gives several advantages including its use of a common control signal that will simplify the control and circuitry. This, of course, brings about its low cost implementation. Another advantage is that this method is also known to have a very good equal load sharing performance independent of variations in power densities of each module. The only thing that is lacking from the method is its absence of redundancy. This is due to the fact that the stationary control depends on the predetermined master generator. However, for the purpose of paralleling turbogenerators, this method is well suited due to its simplicity, low cost, and very good load voltage regulation.

In this study, the evaluation of the proposed parallel ac-ac converters is presented

using computer simulations. This requires the modeling of components in the system. The advantages are that all quantities can be readily observed and parameters altered to investigate their effect and to help debug estimation and control routines. However, computer simulation suffers from the disadvantage of being slow compared to hardware approach.

This work will demonstrate the feasibility of parallel ac-ac converters using Stationary Master Slave Control and Sinusoidal PWM to achieve voltage regulation and equal current sharing among the parallel generators.

2. STATIONARY MASTER SLAVE CONTROL

In the stationary Master Slave Control, one converter is designated to be the master. The master converter output current is the common reference current and is tracked by the slave converter currents. Figure 1 shows a simplified functional block diagram of two parallel ac-ac converters using stationary Master Slave Control. The figure depicts a system of two parallel ac generators connected together to share the same load. For this study, the source voltage is a balanced three-phase system of sinusoidal voltages and thus only one phase needs to be considered. The top module is predetermined to be the master, while the bottom one is assigned to be the slave. The master's output current I_m is taken to be the current reference into the controller for the slave. The output current I_s of the slave module is then delivered to the load and at the same time is also fed back into the controller to form a closed loop control.

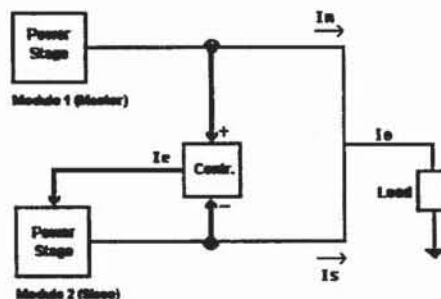


Figure 1. Block diagram of Stationary Master Slave Control with 1 master and 1 slave

The controller is a proportional and integral (PI) controller whose inputs are the current reference taken from the master module and the output current

of the corresponding slave module. The output of the PI controller is then inserted into a comparator whose task is to compare the error voltage to a high frequency triangular waveform. Since the error voltage is sinusoidal, we then have what is known as the Sinusoidal Pulse Width Modulation scheme to control the turning on and off of the switches.

3. PRODUCTION COST

In its functionality, the parallel converters should be capable of performing voltage regulation and equal load sharing or equal current sharing among the identical parallel generators. This equal current sharing also means equal share of power to supply the load since the generators being connected in parallel have identical voltage, are of identical type. Furthermore, the equal sharing performance is important due to the fact that it leads to an economically optimal solution for production cost of electricity of the parallel system. This is true since the generators are identical and use an identical fuel, henceforth the production cost of electricity that varies quadratically with the power generated as described by [9]:

$$F(P_{Gi}) = a_{oi} + b_{oi} \cdot P_{Gi} + c_{oi} \cdot P_{Gi}^2 \quad (1)$$

where $F(P_{Gi})$ is the production cost of unit i , P_{Gi} is the power generated by unit i , a_{oi} , b_{oi} , c_{oi} all greater than zero are the cost coefficients of unit i , and $i = 1, 2, 3, \dots, N$

Equation (1) can be simplified by realizing that for identical units and using the same fuel, the cost coefficients are equal for all units, such that for all i :

$$a_{oi} = a_o; b_{oi} = b_o; c_{oi} = c_o$$

to yield:

$$F(P_{Gi}) = a_o + b_o \cdot P_{Gi} + c_o \cdot P_{Gi}^2 \quad (2)$$

The objective function to be minimized is the total production cost given by:

$$C = \sum_{i=1}^N F(P_{Gi}) = \sum_{i=1}^N a_o + b_o \cdot P_{Gi} + c_o \cdot P_{Gi}^2 \quad (3)$$

$$\text{subject to} \quad \sum_{i=1}^N P_{Gi} = P_D \quad (4)$$

where P_D is the load demand.

To determine the amount of power to be generated by each unit, so that C is minimized, we form an augmented cost function which includes the equality constraint, denoted by C^* :

$$C^* = \sum_{i=1}^N \left(a_o + b_o \cdot P_{Gi} + c_o \cdot P_{Gi}^2 + \lambda \left[P_D - \sum_{i=1}^N P_{Gi} \right] \right) \quad (5)$$

where λ is known as the Lagrange multiplier. Differentiating C^* with respect to P_{Gi} and setting the derivative to zero yields:

$$\frac{\partial C^*}{\partial P_{Gi}} = b_o + 2c_o P_{Gi} - \lambda = 0 \quad (6)$$

from which the optimality condition can be obtained as:

$$\lambda = b_o + 2c_o P_{Gi} = \frac{dF(P_{Gi})}{dP_{Gi}} \quad (7)$$

which is known as the equal incremental cost condition of optimality. Therefore, the power generated by unit i , P_{Gi} , can be obtained from equation (7):

$$P_{Gi} = \frac{\lambda - b_o}{2c_o} \quad (8)$$

Using equation (8) into equation (4) gives:

$$\sum_{i=1}^N \frac{\lambda - b_o}{2c_o} = P_D$$

or,

$$N \frac{(\lambda - b_o)}{2c_o} = P_D$$

equivalently,

$$\frac{(\lambda - b_o)}{2c_o} = \frac{P_D}{N} \quad (9)$$

Substituting equation (8) into equation (9) yields:

$$P_{Gi} = \frac{P_D}{N} \quad (10)$$

which states that for every i the optimal solution is to load the generators identically.

To show that this solution is the absolute minimum, we can differentiate C^* with respect to P_{Gi} with λ a constant yielding:

$$\frac{\partial^2 C^*}{\partial P_{Gi}^2} = 2c_o > 0 \quad (11)$$

4. CONVERTER MODEL

The parallel converter model will be derived using components provided by the existing Pspice library.

As in all system design activity, it is useful to divide the system into smaller functional blocks and then design and test each individually. In this paper, the parallel converters will be implemented in the same way for the purpose of modeling as illustrated in Figure 2.

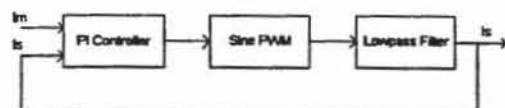


Figure 2. Proposed parallel ac-ac converter using Stationary Master Slave Control

In the PI Controller block, the control action is defined by:

$$\frac{U(s)}{E(s)} = K_p \left(1 + \frac{1}{T_i s} \right) = \frac{K_p (1 + T_i s)}{T_i s} \quad (12)$$

where K_p is the proportional gain, and T_i is the integral time. Both of these values are adjustable. One form of circuit realization of the PI controller using an opamp is shown in Figure 3.

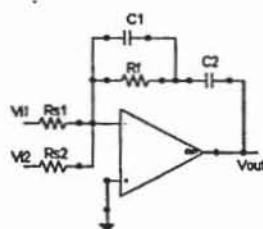


Figure 3. Electronic PI controller using opamp

With $R_{a1} = R_{a2} = R$, the transfer function of Figure 3 is:

$$V_{out} = \frac{1}{R} (V_{in} - V_{ref}) \left(\frac{1 + s\tau_1}{s[\tau_2 + \tau_1]} \right) \quad (13)$$

where $\tau_1 = R_F (C_1 + C_2)$, $\tau_2 = C_2 C_1 R_F$, and $\tau_3 = C_2$. In the sine PWM block, the output of the PI controller is compared to a triangular waveform whose result controls the switches. For ease of explanation, it will be assumed that the midpoint of the DC rail voltage V_d is available, and thus each of the two switches will go either from 0 to $+V_d/2$ or from 0 to $-V_d/2$. This type of PWM

switching scheme is known as the Unipolar voltage switching. The Unipolar switching has several advantages over the Bipolar switching such as the voltage jumps in the output voltage at each switching that are reduced by half from $2V_d$ in the case of Bipolar voltage switching to V_d with the Unipolar scheme. This in turn reduces the stresses and losses experienced by the switching devices and therefore improve their longevity. More importantly, it will also reduce the cost associated with the switching devices due to the lower voltage ratings. Finally, the lowpass filter is used to eliminate the unwanted harmonics.

In this study, MOSFET's, such as irfp250, are used as the switching devices. A development of an improved MOSFET model, introduced in [10], will be used since the current Pspice model of a power MOSFET considers only a constant value of the gate-to-drain capacitance. Therefore, the current Pspice model fails to predict the actual behavior of the device during switching. Therefore, to accurately model the nonlinear gate-to-drain capacitance, the first step is to develop an analytical representation of the gate-to-drain capacitance.

Figure 4 shows the plot of Gate-Drain capacitance C_{gd} for irfp250. At 1V, C_{gd} is about 4000pF. However, C_{gd} goes up to about 4500pF at zero volt and under forward bias conditions (left-hand side of the diagram), it exceeds 5000pF. Because this parameter is of most importance during switching, a method must be determined to characterize C_{gd} below 1V and in the forward bias region for any transistor.

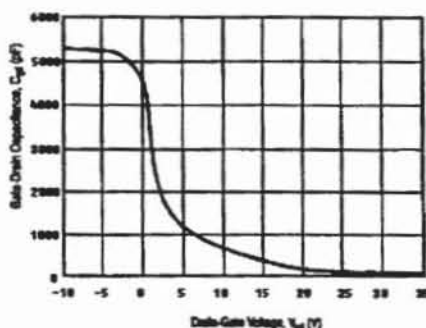


Figure 4. C_{gd} vs bias voltage for irfp250

C_{gd} will be first approximated with an analytical expression in the reverse bias region only (i.e. drain voltage higher than gate voltage). In the forward bias region, C_{gd} is modeled by a constant capacitance whose value is simply equal to the plateau observed in Figure 4. Therefore the goal is then to model C_{gd} in the reverse bias region using a

single diode, so the reverse bias portion of C_{gd} will be matched to an expression of the form:

$$C_{gd}(V_{gd}) = \frac{C_{jo}}{\left[1 - \frac{V_{gd}}{V_j}\right]^M} \quad (14)$$

where V_{gd} is the gate-to-drain voltage (negative in the reverse bias region), and C_{gd} is the gate-to-drain capacitance. Note that equation (14) is exactly the way the junction capacitance of a diode is modeled in Pspice. Therefore, once we have found the parameters C_{jo} , V_j , and M by matching the C_{gd} curve found in irfp250 data sheet to the above function, we can then define a diode in Pspice having parameters identical to the ones found above and whose junction capacitance under reverse bias conditions will be very close to the C_{gd} of the real MOSFET. The values of the three parameters are calculated from three arbitrary points in Figure 4 to be $C_{jo} = 4500\text{pF}$, $V_j = 2.18\text{V}$, and $M = 5$. We can now add these parameters into the intrinsic diode model that will be used in conjunction with the MOSFET model. This result is then translated into Pspice which implies the introduction of components external to the intrinsic model whose electrical parameters correspond to the numerical parameters found in the first step. The complete Pspice model of the improved MOSFET model is shown in Figure 5 where diode DCGDN represents the negative biased capacitance when the MOSFET is turned off. CGDP represents the positive biased capacitance when the MOSFET is turned on.

In its operation, the switch connected in parallel with DCGDN closes when the voltage at node G1 is higher than the voltage at Drain.

Source inductance L_s was extracted from irfp250 data sheet for a typical device. Gate resistance, R_G , was reported in [10] to have an average value of 0.75Ω for a typical gating circuit.

The MOSFET model of Figure 5, along with the PI controller and sine PWM circuits are then incorporated into one subcircuit as depicted in Figure 6. Notice that the MOSFET model is packaged into its own subcircuit. Also note that, in order to reduce the large dv/dt stress on each switch, a snubber capacitor is connected in parallel to the switch.

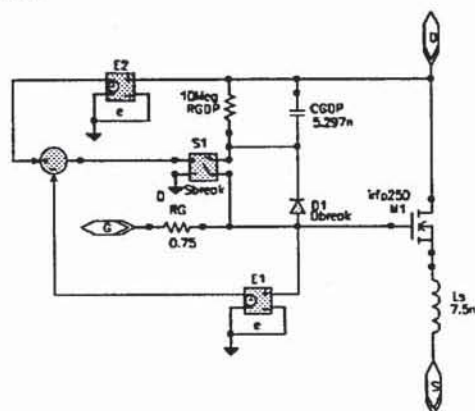


Figure 5. Complete Pspice model of the irfp250

The voltage controlled voltage source located between the switch and the comparator serves as the gating circuit for the switch. The MOSFET is turned on when the voltage across the gate and source of the MOSFET, V_{GS} is higher than a certain threshold voltage value. Otherwise, the MOSFET is turned off. This threshold voltage is called the Gate Threshold Voltage $V_{GS(th)}$. For irfp250, a typical threshold value is 2.0V .

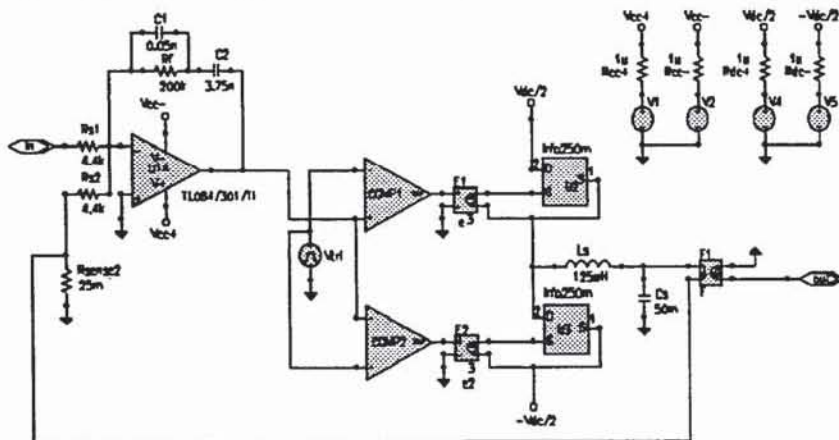


Figure 6. Subcircuit with modified MOSFET model

5. COMPUTER SIMULATION

The parallel converters model with one master unit and one slave unit is simulated with a constant sinusoidal source as shown in Figure 7. The parallel converter for the slave unit is represented by one subcircuit whose content was previously shown in Figure 6.

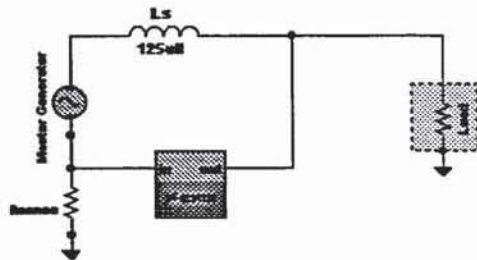


Figure 7. Parallel ac-ac converters with 1 master and 1 slave

The results of the computer simulation, as shown in Figures 8 and 9, show that each unit shares the load current equally as expected. Moreover, the load voltage is also shown to be nicely regulated at 120V.

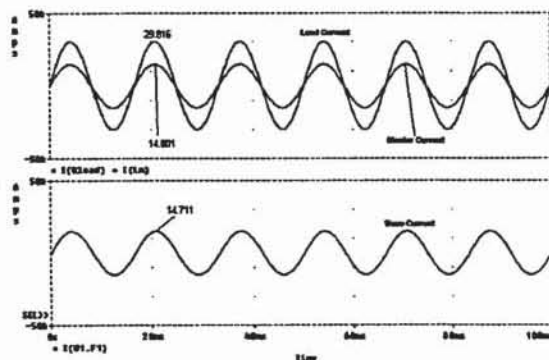


Figure 8. Current waveforms

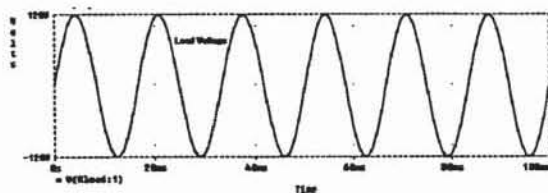


Figure 9. Load voltage waveform

Figure 10 shows the ripples observed by zooming into the load current and voltage waveform. These high frequency ripples are associated with the 20kHz switching frequency that was used in the simulation. The value peak

to peak load current ripple was calculated to be 0.707%, while the peak to peak load voltage ripple was found to be 0.712%.

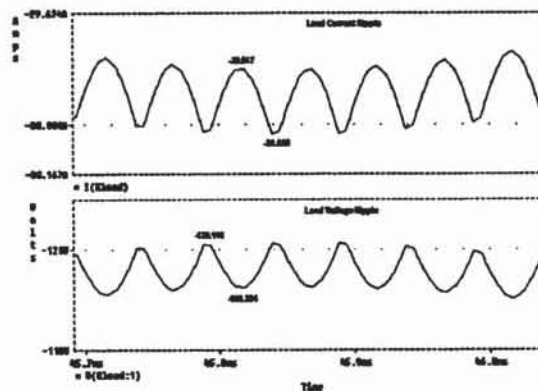


Figure 10. Load current and voltage ripples

6. ROBUSTNESS STUDY

In this study, several different disturbances are imposed to the parallel converters system to investigate the robustness of the parallel converters system, i.e. whether the system remains stable under these disturbances. These include step changes in load, an inherent delay due to digital implementation, and a unit added to or taken off from the system during operation. Also, ac induction motor model is used as load to the converters.

In a real implementation, a digital interface may be used to process the reference current before it is sent to the slave converters. In doing so, unfortunately an inherent delay associated with a digital system is unavoidable. Therefore it will be important to study the effect of this digital delay on the stability of the system.

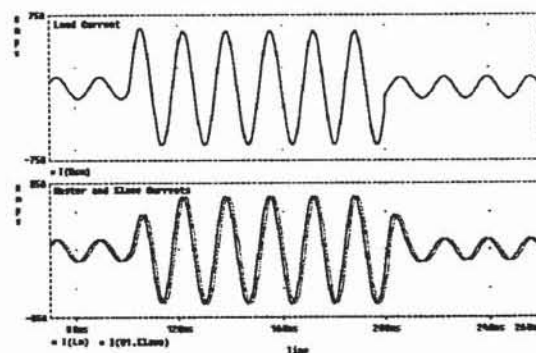


Figure 11. Current waveforms with real ac, induction motor load, 2 units and 1ms delay

A relatively large digital delay of 1 ms is simulated in the parallel system including the step up and down changes in the mechanical load of the induction motor, whose results are shown in Figure 11. Notice that the equal current sharing is still performed by the parallel converters even with the presence of delay. Moreover, stability during step up and down in the load is also maintained by the parallel converters.

Another type of real contingency such as the removal or the insertion of a unit will be considered in the study. During normal operation, a unit may be taken out from the parallel system for routine maintenance. Similarly, a unit taken out of service for maintenance may be reconnected to the system after service completion. In these cases, not only the units should quickly adjust their new equal sharing of the load current but they should also maintain system stability. Figure 12 depicts a circuit configuration that will be implemented to simulate the removal or the addition of one unit from or to the parallel system respectively. As shown in the Figure, initially there are 3 units (1 master and 2 slaves) in the parallel system and therefore each unit should have $1/3$ of the load current. At the time when a unit is disconnected from the system, the remaining 2 units should now share $1/2$ of the load current. The result, as shown in Figure 13, indicates that the equal current sharing of load current before and after 1 unit is disconnected is retained and the stability is maintained by the parallel converters throughout the process. Moreover, Figure 14 shows that load voltage is also regulated.

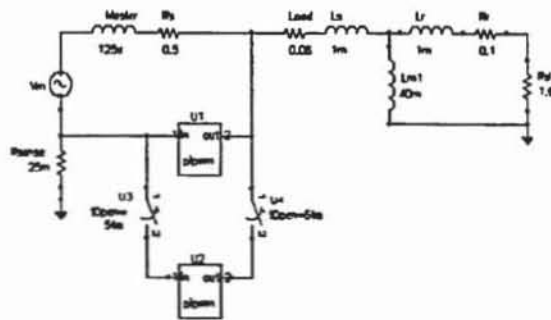


Figure 12. Removal of one unit during operation

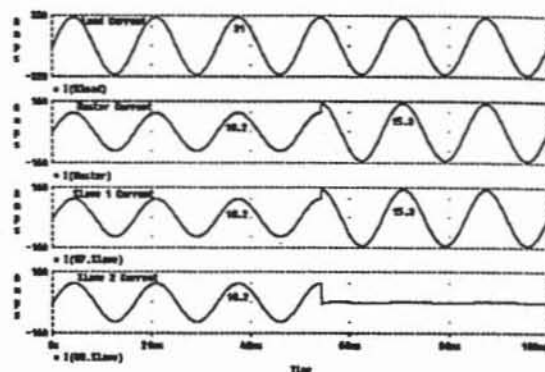


Figure 13. Current waveforms when 1 unit is removed during operation

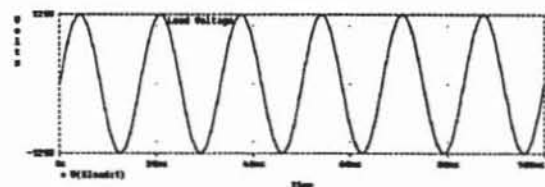


Figure 14. Load voltage waveform when 1 unit is removed during operation

The reverse operation where one unit is added into the system during its operation was also studied. The circuit configuration is similar to the one shown in Figure 12, except now the switches are being closed to represent the insertion of the one unit. The result, depicted in Figure 15 shows that the equal current sharing property and system stability that are again maintained by the parallel converters prior to and after the insertion, while Figure 16 indicates the well regulated load voltage.

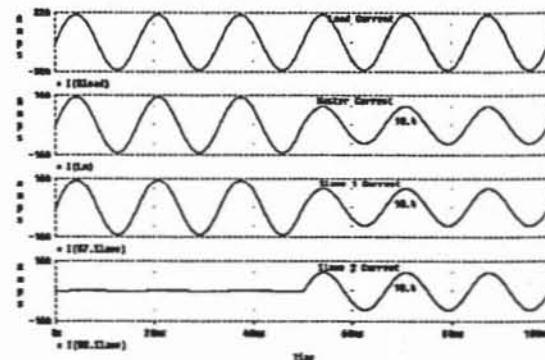


Figure 15. Insertion of one unit during operation

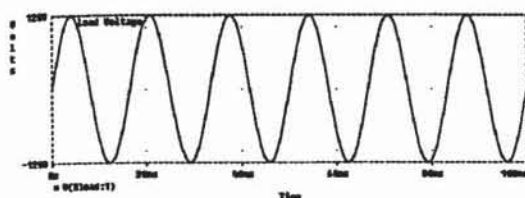


Figure 16. Load voltage waveform when 1 unit is inserted during operation

CONCLUSION

A proposed parallel ac-ac converter using Stationary Master Slave Control and sinusoidal PWM has been presented in this study. The main objective of the converter is to obtain voltage regulation and equal current sharing among the paralleled units such that total cost of operation is minimized. A converter model using Pspice and implementation of an improved MOSFET model was also presented from which numerous computer simulations were conducted [11]. The results of the computer simulations show that the proposed parallel ac-ac converters, despite its simple configuration, provides voltage regulation and equal current sharing control among parallel modules. Furthermore, robustness study was also discussed to show that the parallel converters maintain system stability due to several different disturbances applied to the system. These simulated results demonstrate the feasibility of the proposed parallel ac-ac converters to achieve the equal current sharing.

REFERENCES

- [1] C. Jamerson, C. Mullet, "Paralleling Power Supplies via Various Droop Methods", *High-Frequency Power Conversion Conference*, April 1994, pp. 68-76.
- [2] I. Batarseh, K. Siri, and H. Lee, "Investigation of the output droop characteristics of parallel connected dc-dc converters", *IEEE Power Electronics Specialists Conference Record*, 1994, pp. 1342-1351.
- [3] R. Wu, T. Kohama, Y. Kadera and T. Ninomiya, "Load-Current Sharing Control for Parallel Operation of DC-to-DC Converters", *IEEE Power Electronics Specialist Conference Record*, 1993, pp. 101-107.
- [4] I. Batarseh, K. Siri, J. Banda, "An Alternative Approach for Improving Current Sharing in Parallel Connected DC-DC Converter Systems", *High-Frequency Power Conversion Conference*, 1994, pp. 102-118.
- [5] J. Rajagopalan, K. Xing, Y. Guo, F. Lee, B. Manners, "Modeling and Dynamic Analysis of Paralleled DC/DC Converters with Master Slave Current Sharing Control", *IEEE Applied Power Electronics Conference Record*, 1996, pp. 678-684.
- [6] Panov, Y., J. Rajagopalan, and F.C. Lee, "Analysis and Design of N Paralleled DC-DC Converters with MSC Sharing Control", *Proceedings IEEE Applied Power Electronics Conference and Exposition*, Vol. 1, 1997, pp. 436-442.
- [7] Moussaoui, Z., I Batarseh, H. Lee, and C. Kennedy, "An Overview of the Control Scheme for Distributed Power Systems", *IEEE Southcon Conference Record*, 1996, pp. 584-591.
- [8] Petruzzello, F., P.D. Ziogas, and G. Joos, "A Novel Approach to Paralleling of Power Converter Units with True Redundancy", *IEEE Power Electronics Specialist Conference Record*, 1990, pp. 808-813.
- [9] Wood, A.J., *Power Generation Operation and Control*, Wiley-Interscience, New York, 1996.
- [10] Gotti, E., "Power MOSFET Pspice Model Accurately Simulates Nonlinear Gate-to-Drain Capacitance", *Power Conversion & Intelligent Motion*, Vol. 24, No. 3, March 1998, pp. 16-23.
- [11] Taufik, *Parallel AC-AC Converters Using Master Slave Control*, Doctor of Engineering Dissertation, Cleveland State University, 1999.