A New AC-DC Converter Using Bridgeless SEPIC

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***Abstract*-A new bridgeless power factor correction circuit (PFC) based on single ended primary inductance converter (SEPIC) is proposed. The number of component conducted at each subinterval mode is reduced compared to the existing topologies. Analysis of the converter operated in discontinuous-conduction mode (DCM) is discussed. Experimental circuit for the proposed converter is developed with universal input voltage capability for 50V DC output voltage connected to 100W load. The simulation and experimental results are presented to show the performances of the proposed circuit.**

I. INTRODUCTION

The active power factor correction (PFC) circuits are widely used to effectively draw the energy from the mains via an AC to DC converter. These PFC circuits are normally consists of full bridge diode rectifier and DC-DC converter. If only one DC-DC converter is used, then it will be classified as a single-stage converter while two-stage converter utilizes two-DC-DC converter. On the other hand, some PFC circuits are realized without the full-bridge rectifier circuit, which is known as the bridgeless PFC topology. D.M Mitchell has proposed the very first bridgeless PFC topology back in 1983 [1]. Actually, these bridgeless PFC circuit combines the operation of bridge rectifier and DC-DC converter into a single circuit.

With a simple circuit analysis, it can be identified that the bridgeless PFC topology namely the Boost bridgeless has less number of components conduct at each switching cycle compared to the conventional Boost PFC circuit. Numerous works on bridgeless PFC have been reported which focus on several key issues such as newly proposed topology, higher power factor and higher efficiency capability [2]-[7], compared to the conventional PFC converters. Recently, a new bridgeless PFC circuit based on single ended primary inductance converter (SEPIC) has been proposed [8] and the schematic diagram is depicted in Figure 1(a). It is reported that this converter offer several advantages as a PFC circuit such as lower input current, easily implemented as isolated converter and less electromagnetic inference (EMI).

However, several drawbacks has been identified in this converter such as; too many components conducted at each switching period, isolated gate drive circuit is required to drive the MOSFETs and two sets of output capacitors at two different terminals are required. On top of that it is found that the output load terminal is floating between the two separated output capacitor.

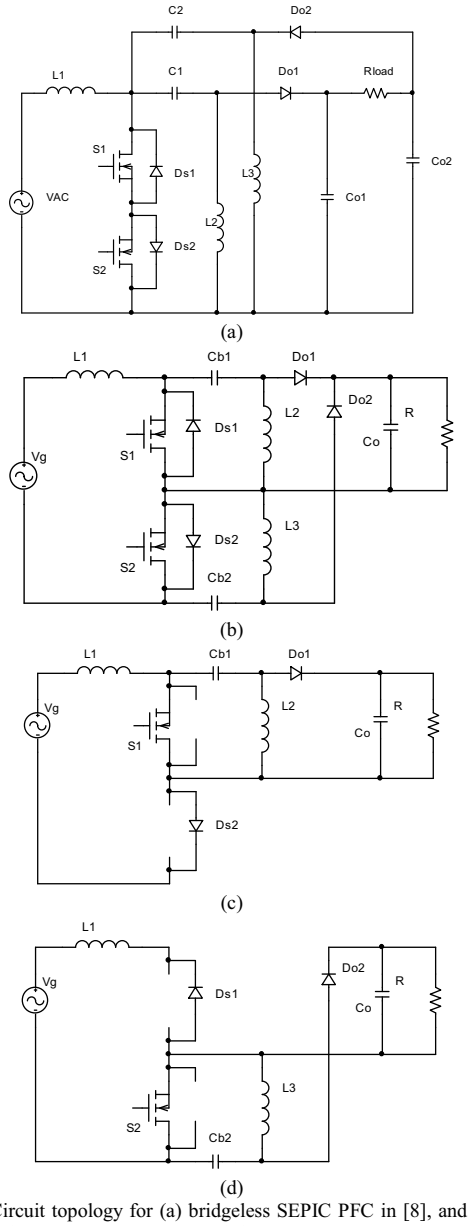


Fig. 1. Circuit topology for (a) bridgeless SEPIC PFC in [8], and (b) the proposed bridgeless SEPIC operated during (c) positive and (d) negative half line cycle

In this paper, a new bridgeless power factor correction circuit (PFC) based on SEPIC is proposed. The circuit diagram of the proposed bridgeless PFC circuit is shown in

Figure 1(b). Interestingly, the proposed circuit is much simpler compared to the one proposed in [8] in several aspects namely: (1) less number of components operated at each input-voltage cycle, (2) the minimum number of output capacitor (Co) required is one, (3) driving the MOSFETs gate terminal is simpler due to both '*source*' terminals of the MOSFETs are connected to a common node and last but not least, (4) no gate-driver circuit with isolation is required.

As the analysis goes deeper, it is found that the circuit analysis can be divided into two main parts which are the operation during positive half-line cycle and negative half-line cycle as shown in Fig 1 (c) and (d). During positive half-line cycle, all components will conduct except Ds1, S2, C2, L3 and Do2. During negative cycle, the components that will not conduct are Ds2, S1, C1, L2 and Do1. Thus only eight components will be conducted at each half-line cycle compared to eleven in the bridgeless SEPIC converter proposed in [8]. Note that at each half line cycle of the input voltage, the proposed converter operated more or less like a SEPIC DC-DC converter.

II. CIRCUIT OPERATION

In this paper, only the operation during positive half line-cycle will be discussed while the same operation can be performed for the negative half-line cycle. The proposed converter will operate in Discontinuous Conduction Modes (DCM) since this type of mode offers several advantages namely capability to operate as PFC is inherent, suitable for low power applications and lower component stress. As depicted in Figure 2 and Figure 3, the circuit operation of the proposed converter within each switching period, T_S, can be divided into three subinterval modes, namely MODE 1 (d_1T_S), MODE 2 (d_2T_S) and MODE 3 (d_3T_S). Throughout the circuit analysis, it is assumed that all the components are ideal and lossless.

In MODE 1, the equivalent circuit is shown in Figure 2(a). As can be seen, when the upper MOSFET, S1, is turned on, the current from the source, Vg, will flow through the input inductor and continue to S1 and Ds2 before completing the current path through Vg. At the same time, as shown in Figure 3, the current through L1 increased linearly to its peak

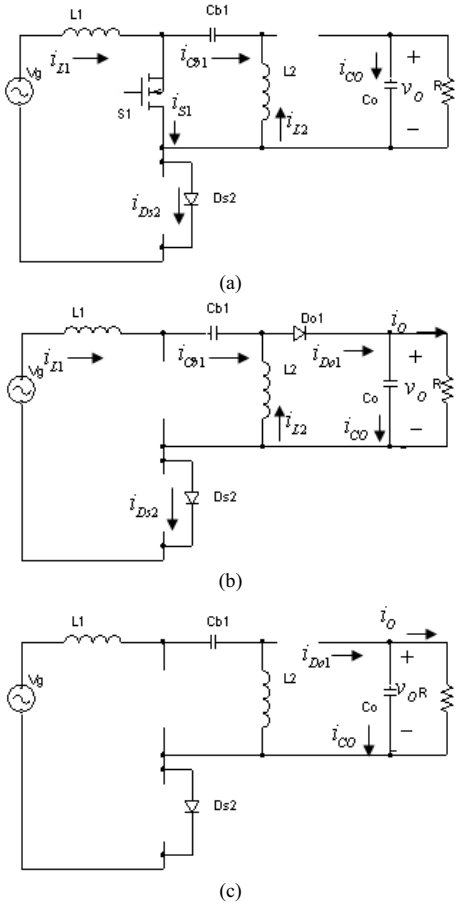


Fig. 2. Equivalent circuit during (a) MODE 1(d_1T_S), (b) MODE 2(d_2T_S) and (c) MODE 3(d_3T_S).

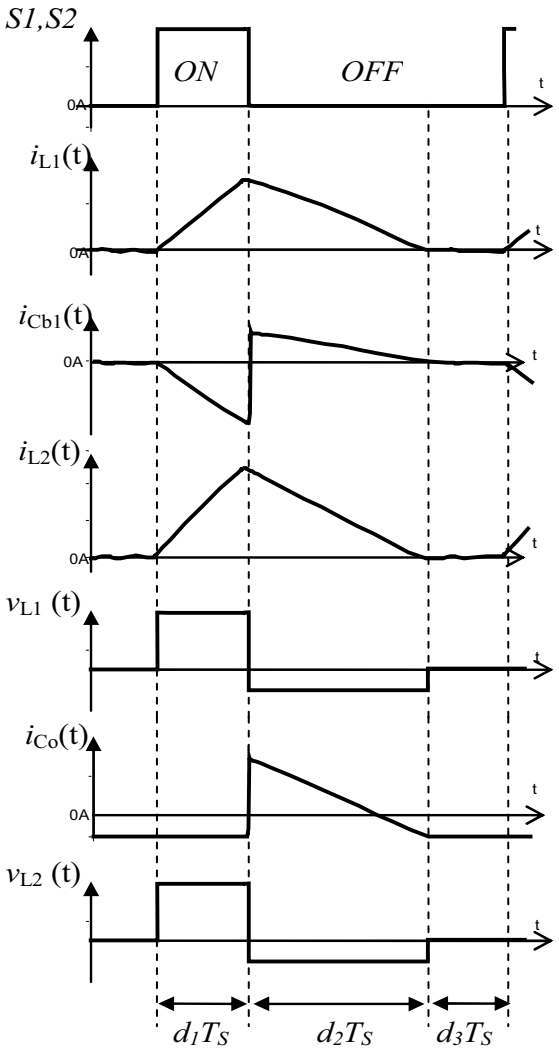


Fig. 3. Waveforms within each switching period for several components.

value,

$$i_{L1-peak} = \frac{v_g}{L_1}(d_1 T_S) \quad (1)$$

where d_1 is the duty cycle. On the other hand, the second inductor, L2 discharged its energy linearly to Cb1 and creates a current path to MOSFET S1 before returning to L2. It is found that the current flowing through S1 is the addition of the current through L1 and L2. At this point, the output voltage is equal to the capacitor voltage, Vo, due to output diode, Do1 being reverse-biased.

Figure 2(b) shows the circuit in MODE 2. Obviously at this mode, S1 is turned off such that no current will flow through it, but now Do1 is forward-biased. At this point, together with Vg, the current through L1 falls linearly due to the process of discharging its current to the load through i_{Cb1} and i_{Do1} and create the return path through Ds2. At the same time, L2 will also discharge its current linearly to the load through i_{Do1}. Now, the current flowing through Do1 is the summation of i_{L1} and i_{L2}. Thus, the peak current for Do1 is

$$i_{Do1-pk} = i_{L1-pk} + i_{L2-pk} = d_1 T_S \left(\frac{v_g}{L_1} + \frac{v_{Cb1}}{L_2} \right) \quad (2)$$

Since $v_{Cb1} \approx v_g$, equation (2) can be further simplifies to

$$i_{Do1-pk} = d_1 T_S \left(\frac{v_g}{L_a} \right) \quad (3)$$

where $L_a = L_1 // L_2$. In addition, the peak current flowing through MOSFET S1 is exactly the same with Do1 due to the summation of current at L1 and L2. Interestingly, the current stress as shown in equation (3) for the proposed circuit is similar with Figure 1(a). However, it should be noted that in Figure 1(a), the equivalent inductance, L_a, consist of three parallel inductors [8], whereas in this circuit, only two inductors are paralleled. In other word, the L_a value for the circuit in Figure 1(a) is smaller than L_a in the proposed circuit which will result smaller current stress in the proposed circuit. From Figure 3, the d_2 width can be determine by examining the ripple current at L1 such that,

$$d_2 = \frac{v_g}{(v_{Cb1} + v_O - v_g)} d_1 \quad (4)$$

Finally, in MODE 3, both S1 and Do1 are turned off resulting only two closed current path which is at the input and the output side. It is assumed that at this point, the energy at L1 and L2 are equal while Vg is equal to V_{Cb1}. As a result, the input current is approximately equal to zero. However, an almost DC current exist at this mode and the amount of current at L1 and L2 are equal but on the opposite direction. By equating the average current of Do1 with the output current, $i_O = V_O/R$, the relationship between input and output voltage or normally known as voltage conversion ratio is,

$$M = \frac{v_O}{v_g} = d_1 \sqrt{\frac{RT_S}{2L_a}} \quad (5)$$

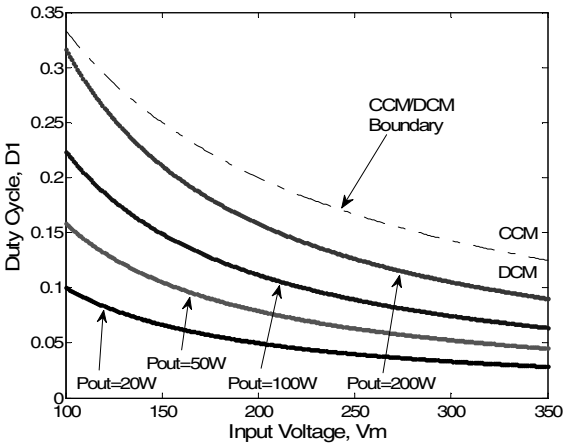


Fig. 4. Boundary condition for CCM and DCM operation.

Where R is the resistive load value. On the other hand, to ensure DCM operation for each switching period, the component selection must follow this equation,

$$1 - d_1 > \sqrt{\frac{2L_a}{RT_S}}. \quad (6)$$

By using equation 5, the boundary between CCM and DCM operation can be visualized as dotted line shown in Figure 4. If the converter operates above the dotted line, it will be operating in the CCM region while operation below the dotted line means that it is operating in the DCM region. Thus, from the figure, it is obvious that with any load condition, when the converter operated at certain duty cycle and input voltage values, it will either operate in CCM or DCM. In this work, a suitable duty cycle and load condition should be determined at first place in order to secure DCM operation.

III. RESULTS AND DISCUSSION

The proposed circuit is designed based on the parameters given in TABLE I. All the parameters are selected based on the equations discussed in previous chapter especially equation (6) which will ensure the circuit operation in DCM. As can be seen, the proposed circuit is capable to operate with universal input voltage source ranging from 115 Vrms to 230 Vrms at 100W output load condition.

TABLE I
DESIGN PARAMETERS OF THE PROPOSED CICRCUIT

Input voltage, Vg	115-230V_{rms} at 50Hz
L_1	150uH
L_2 and L_3	70uH
Bulk capacitor, C_{B1} & C_{B2}	1uF
Output voltage, Vout	50V DC
Switching frequency, f_S	50kHz
Rated output power, Po	100W
Output capacitor, C_O	1410uF

Using PSpice, the input voltage and current waveforms based on simulation are presented in Figure 5 (a) & (b) for 115Vrms and 230Vrms input voltage respectively. The current rigidly follows the input voltage which justifies the inherent PFC capability when operated at DCM. With the given duty cycle, the output voltage has successfully achieved the desired 50 VDC having a15% voltage ripple at twice the line frequency, as shown in Figure 5(c). In Figure 5(d), the input current is obviously operated in DCM, with three modes of operations.

The experimental circuit is also developed based on the design parameters specified in Table 1. All the components are selected based on its availability in the market such that its values are similar to the designed ones. Figure 6 shows the experimental results for the proposed circuit.

From Figure 6(a), the input current follows the voltage waveform and is in phase with the 115 Vrms input voltage with power factor for this condition recorded at 0.98. The same results can be observed for 230 Vrms input voltage in Figure 6(b) with 0.97 power factor. It is proved that without

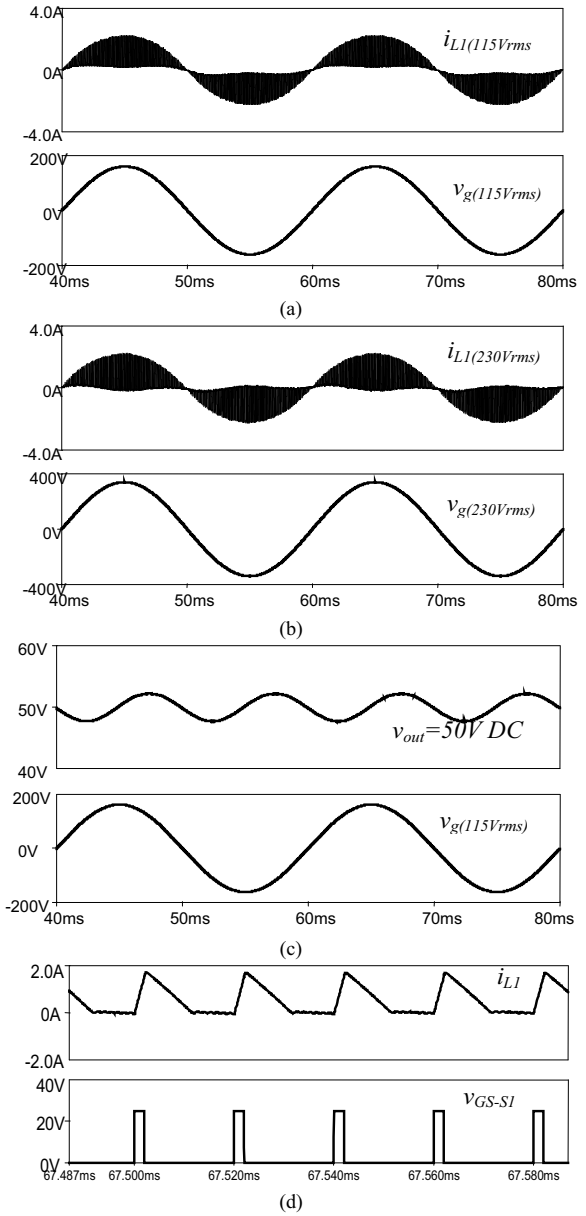


Fig. 5. Simulation results for (a) input voltage and input current with |Vg|=115Vrms, (b) input voltage and input current with |Vg|=230Vrms, (c) output voltage and, (d) input current and gate drive signal within each switching period.

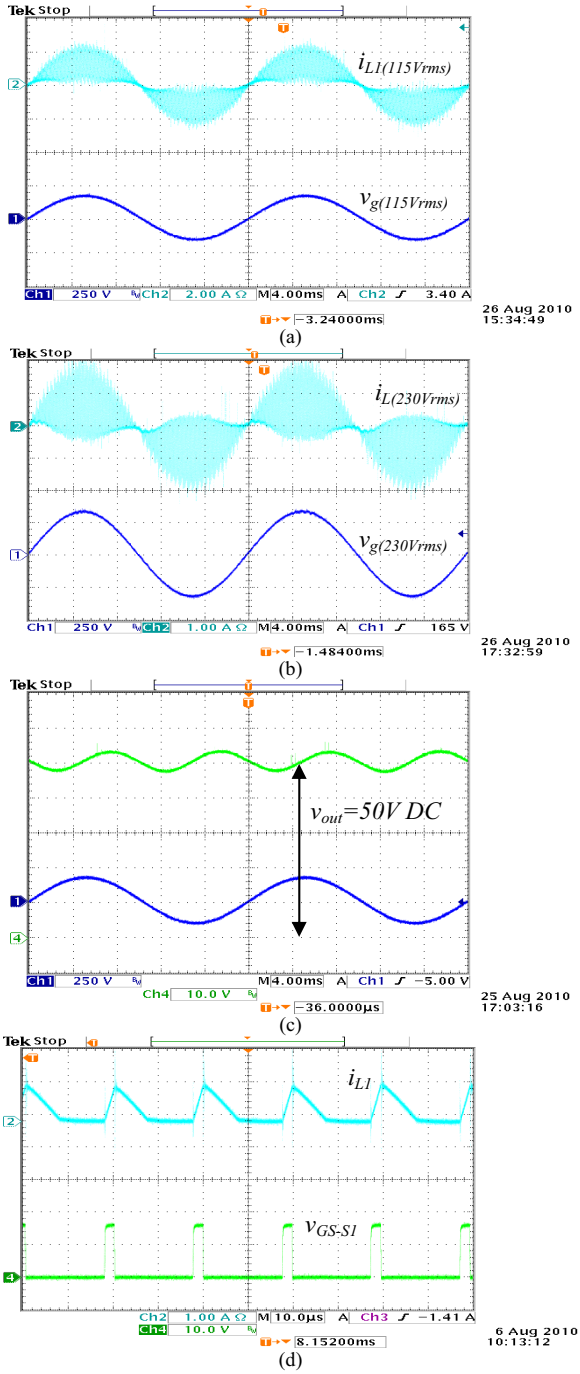
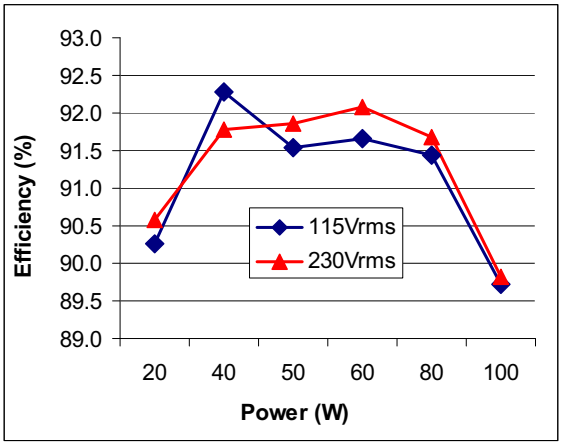


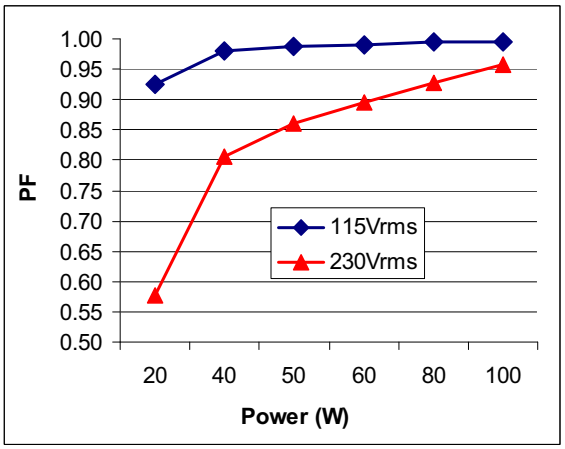
Fig. 6. Experimental results for (a) input voltage and input current with |Vg|=115Vrms, (b) input voltage and input current with |Vg|=230Vrms, (c) output voltage and, (d) input current and gate drive signal within each switching period.

any current regulation, the input current is capable to be reshaped to sinusoidal waveform and in phase with the input voltage due to DCM operation. In addition, this circuit can achieve high power factor. In Figure 6(c), the output voltage is set at 50 VDC with 16% 100 Hz voltage ripple. . Finally, as depicted in Figure 6(d), the input current waveform shows the operation in DCM with respect to the desired duty cycle value which is used to drive the two MOSFETs, S1 and S2.

Figure 7(a) shows the efficiency of the proposed converter operated at two distinctive input voltage values, 115Vrms and 230Vrms. As can be seen, the proposed converter is capable to obtain high efficiency at light load condition, which is above 90% efficiency for both input voltage values. It should be noted that this efficiency is including the LC input filter. Without this input filter, the efficiency should be higher. On the power factor values as shown in Figure 7(b), the PF is always greater than 0.9 for 115Vrms input voltage but for 230Vrms input voltage, the converter suffer low power factor especially for power below 60W. The power factor values are measured for the filtered input current.



(a)



(b)

Fig. 7. (a) The efficiency and (b) power factor for the proposed converter at 115Vrms and 230Vrms input voltages.

IV. CONCLUSIONS

In this paper, a new Bridgeless PFC circuit based on SEPIC DC-DC converter has been proposed and verified by simulation and experimental works. It is showed that the proposed circuit is capable to achieve high power factor under universal input voltage condition. The capability to reshape the input current is inherent when the circuit is operated in DCM. This circuit would be most suitable to be used as a switch mode power supply application for low power equipments especially those requiring high quality input power

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