Multiplicative Feedback Audio Distortion Circuit

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2013

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ACKNOWLEDGMENTS

I would like to thank my parents for all of their assistance, knowledge, support and encouragement – and their patience as well. I'd also like to thank my advisor, Prof. Vladimir Prodanov, for supplying the overall design, keeping the project on track, and providing assistance whenever it was needed – and for being a great instructor for EE 306 and EE 308, which gave me the background knowledge I needed to do this project. In addition, I'd like to thank Sara Mason for providing moral support, especially when my schedule got hectic near the end of the quarter.

ABSTRACT

This circuit aims to distort an audio signal input in a novel and aesthetically pleasing manner. When it comes to the timbre of a note, even harmonics generally sound better than odd harmonics. Most forms of audio signal distortion (usually for electric guitar) primarily add odd harmonics to a signal, as this is easily accomplished by clipping the waveform. This project instead utilizes a signal multiplier in a feedback loop, with one multiplier input coming from the circuit's input, and the other from the multiplier's own output. This process creates even harmonics. A delay line is placed in the loop, adding complexity to the sound. The circuit as a whole consists entirely of analog solid-state electronics.

I. Introduction

The electric guitar, despite being a revolutionary invention for the world of music, has always sounded rather dull when run through a purely linear sound system. As a result, guitarists and sound engineers have been devising ways to produce a better sound since the onset of electronic amplification. In the beginning were vacuum tube amplifiers. Expensive and fragile, circuits utilizing tubes were very simple by necessity. They also required very high voltages to function, producing further trouble for engineers. These were superseded in the following decades by analog transistor amplifiers, which were much easier to work with and could produce more complex circuits at a significantly lower cost.

With the advent of the digital era, modeling amplifiers have come to the forefront, using software to process a guitar's signal. However, modeling amplifiers have a mixed reputation among musicians, and many will not use them as anything more than a practice amp. Many low-cost digital amps are not treated as serious tools by guitar players, amateur and professional alike.

The bad reputation of modeling amps comes partly from the fact that analog amplifiers are difficult—if not impossible—to accurately emulate in real time. The BJT—a simple component for an analog transistor amplifier—requires an incredible amount of math to model. As a result, either shortcuts are taken, or the model uses some arbitrary transfer function not based on transistors or other real-world components. Such an amplifier can sound decent, but is often decried as having a "fake" and "superficial" sound by seasoned musicians.

In fact, many musicians eschew analog transistor amplifiers as well, preferring the "warm,

vintage” sound of vacuum tubes. Despite their issues, vacuum tubes are still in use today in many amplifiers because of the popularity of their sound—particularly the fact that they tend to produce even harmonics when overdriven, while transistor amps primarily produce odd harmonics. This is not simply cultural – even harmonics sound more aesthetically pleasing because the human ear-brain system is set up to perceive even harmonics (particularly power-of-two harmonics, i.e. octaves) as consonant.

This project attempts to reconcile the portability of transistor amplifiers with the well-liked sound of vacuum tube amplifiers, by using a unique configuration to produce even harmonics with transistors. The design is all-analog, and consists primarily of a linear signal multiplier and a bucket-brigade delay (BBD), fed through a closed loop.

II. Background

The “typical” distortion circuit works by clipping the input waveform. Most of the time it is some variation of this:

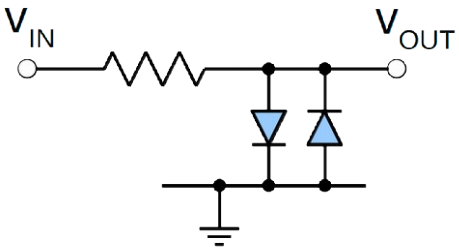

Figure 1.1: Resistor-diode clipping circuit

This simple resistor-diode clipping circuit works by limiting the waveform to ±0.7V, creating distortion.

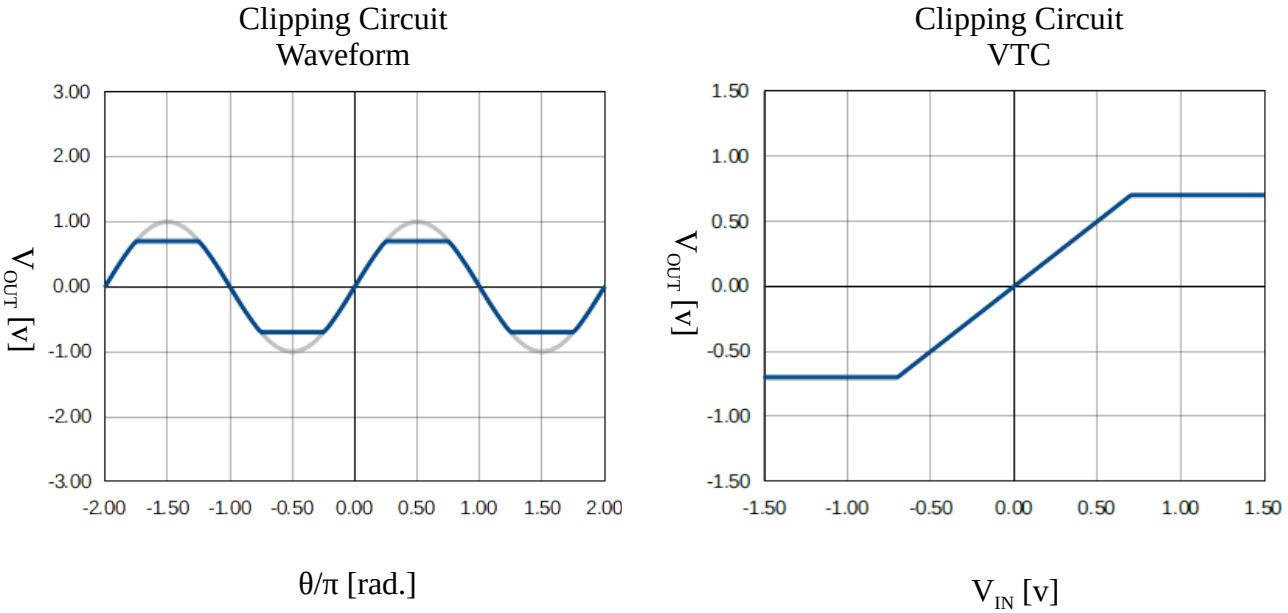

Figure 1.2: Behavior of RD clipping circuit (assuming V_{CLIP} = 0.7V)

The primary issues with this circuit are that it produces “hard” clipping (since once the waveform hits 0.7V there’s no further change) and that it creates only odd harmonics.

If coupled with linear gain (which is usually the case with such a circuit) the output waveform of a clipping circuit begins to resemble a square wave as gain increases.

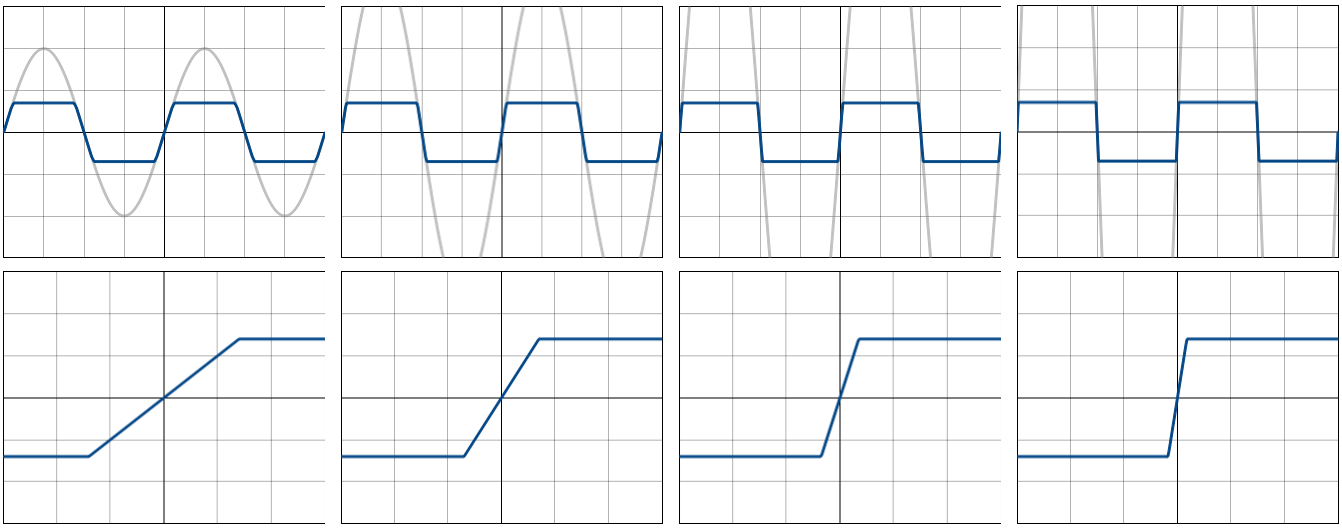

Figure 1.3: RD circuit behavior with various gain levels (2x, 4x, 8x, 16x)
Axes are same as on Figure 1.2

The Taylor Series for a square wave contains only odd multiples of the fundamental frequency, meaning a filter which produces a square-wave-like output will be rich with odd harmonics.

In addition, the VTCs all have perfectly odd-symmetry, meaning such a filter creates no even harmonics at all.

Despite these drawbacks, many distortion circuits rely on this type of filter, since it is simple and can produce a heavy amount of distortion. As a result, this project does not rely on waveform clipping, and instead produces distortion using a signal multiplier in a feedback loop.

For the project's form of multiplicative feedback, the general schematic looks like this:

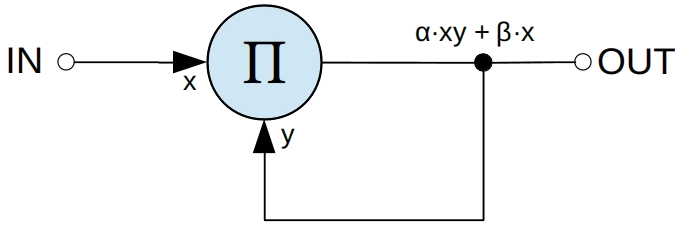

Figure 1.4: Multiplicative feedback, basic form

In Figure 1.3, a signal multiplier feeds back into itself. There is also a parallel linear gain for channel x. The diagram can be expanded slightly to reflect this:

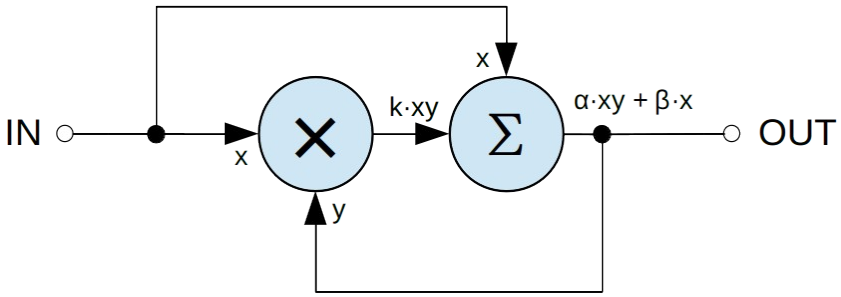

Figure 1.5: Multiplicative feedback, expanded to show linear gain

For inputs x and y, and constant values α and β, the feedback loop is of the form

$$y = \alpha \cdot xy + \beta \cdot x$$

which reduces to

$$y = \frac{\beta x}{1 - \alpha x}$$

It has been determined empirically that this works best when α and β are both negative, giving the equation the form

$$y = \frac{-|\beta| x}{1 + |\alpha| x}$$

This goes to $-\frac{\beta}{\alpha}$ as $x \to \infty$, and to $-\infty$ as $x \to \frac{1}{\alpha}^{+}$. The expansion in one direction and contraction in the other is evidence that even harmonics are being created.

This basic design can be enhanced by inserting signal processing into the feedback loop. For this project, a delay line is used. (Analog, bucket-brigade.) This addition, along with input and output handling, creates Figure 2.2 (page 8) out of Figure 1.3.

III. Requirements

The product should follow the conventions used by guitar effects pedals as closely as possible. Commercially available pedals vary in their input/output requirements, but most of them have a few things in common.

Requirements for project:

- Operates on a –9V supply. (Either external or a 9V battery.)
- Has a high-impedance input (≥100kΩ) and a mid-to-low-impedance output (≤10kΩ).
  - Ideally, input impedance is ~250kΩ and output impedance is ~1kΩ.
- Input and output are both AC-coupled.
- Has predictable behavior; is generally time-invariant for larger time intervals (>1s).
- Does not consume excessive power (preferably <3W).
- Poses no direct risk of harm to user.
  - Indirect risk (i.e. loud output from a transient) is minimized or zero.
- Can tolerate external RF interference; does not generate RF interference.
- Input and output are both scaleable, to account for various scenarios.
- Signal is distorted in a way that:
  - Is aesthetically pleasing to the human ear
  - Consists primarily of even harmonics

IV. Design

Level 0 – Black Box

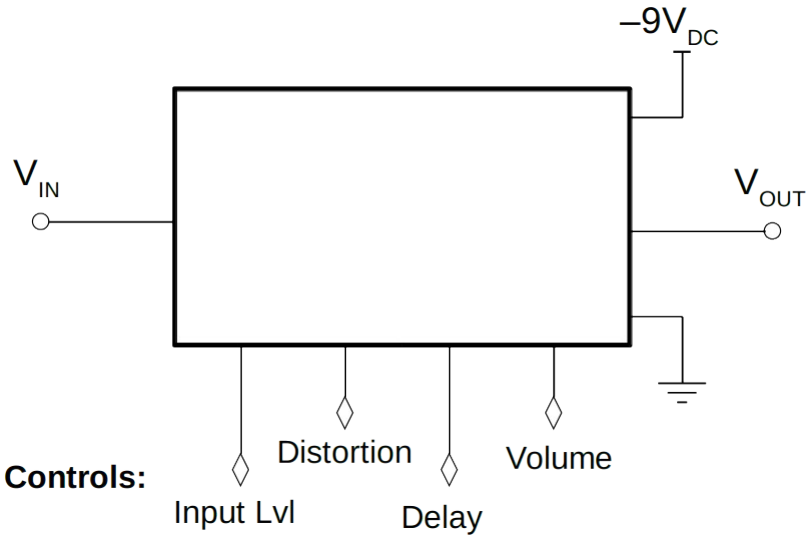

Figure 2.1: Level 0 Block Diagram

Interface aims to give user as much control as is practical without being overly complicated.

Consists of the following:

Electrical connections

- **$-9V_{DC}$:** Power supply. Can be DC plug or battery.
- **GND:** Signal and power ground.
- **V_{IN}:** Signal input. AC coupled, high (≥100kΩ) impedance.
- **V_{OUT}:** Signal output. AC coupled, mid-to-low (≤10kΩ) impedance.

Potentiometer knobs

- **Input Lvl:** Prescalar, gain control for signal input
  - Not labeled as “gain” as that can be synonymous with “distortion” for guitarists
- **Distortion:** Gain control for feedback loop
- **Delay:** Control for BBD delay time
  - Varies frequency of 555 timer
- **Volume:** Output gain control

Level 1 – Block Diagram

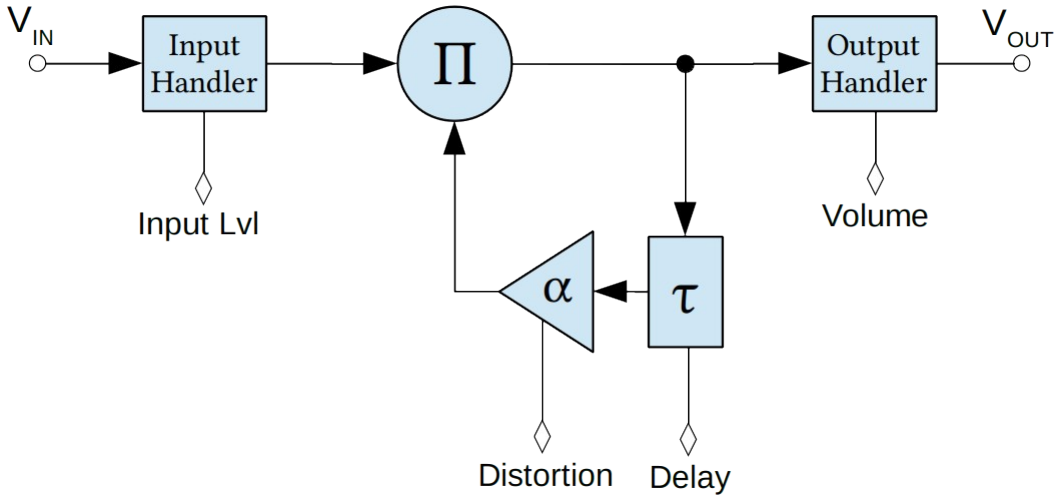

Figure 2.2: Level 1 Block Diagram

Internal design consists of five blocks, each with an input (two for Π), an output, access to power (–9V and GND) as well as a half-supply reference voltage (V_R, set to –4.5V). All except Π have a user-accessible control. (Power and half-supply not shown on diagram.)

Consists of the following:

- **Input Handler:** Buffers input, DC biases to V_R.
  - High-impedance input (~250kΩ), low-impedance output (op-amp output terminal).
  - User-controllable gain.
  - Non-inverting.
- **Signal Multiplier (Π):** Multiplies two signals (from Input Handler and α), sums with buffered signal 0 (from Input Handler).
  - Mid-impedance input (~10kΩ), low-impedance output (op-amp out).
  - Inverting.
- **Signal Delay (τ):** Delays input (from Π) by ~30ms.
  - High-impedance input (input to BBD), low-impedance output (op-amp out).
  - User-controllable delay time.
  - Inverting.

- **Distortion Gain (α):** Controls output level of τ, limits high-frequency output.
  - Mid-impedance input (10kΩ), low-impedance output (op-amp out).
  - User-controllable gain.
  - Inverting.
- **Output Handler:** Controls final amplitude of output signal, DC-biases to GND.
  - Mid-impedance input (10kΩ), low-impedance output (~1kΩ).
  - User-controllable gain.
  - Inverting.

Conventions & Components

Different audio processing products require very different voltages – some use as little as 1.5V, some use up to $12V_{DC}$, and some run on 110V AC power. However, most guitar effects boxes run on $9V_{DC}$, and so this is the convention which was followed. Most audio ICs can work with a 9V supply, and 9V DC power supplies (and batteries) are commonly available.

A wide variety of op-amps are available on the market, but most of them are not suited to the needs of this project. Of those that are, many are out of manufacture, prohibitively expensive, or otherwise impractical. A suitable op-amp for this project is one that can run on a 9V single supply, has rail-to-rail output and a slew rate suited for audio signal processing, and is still being manufactured (and sold for a reasonable price). Of the op-amps commonly available, Linear Technology's LT1677 chip was chosen for this project, as it met all of the requirements.

The delay block required comparators in order to function properly. The best ones for the job would be fast (less than 1µs switch time), have rail-to-rail output, and have push-pull output. The

LT1677 and LM301 chips were both considered for the job in early development, but LT1677 makes a poor comparator and LM301 is not rail-to-rail. Eventually LT1011s were chosen. They do not have a push-pull output, but are sufficiently fast and have rail-to-rail output. With the right pull-up resistors, they perform their job properly.

For the following schematics (level 2), LT1677s are shown in yellow, LT1011s in gray, and both are given access to the power rails (not shown).

In addition, a reference voltage, V_R, is used throughout the circuit. This half-supply voltage is created in lieu of a true split-supply power source, allowing the circuit to work on a single 9V supply.

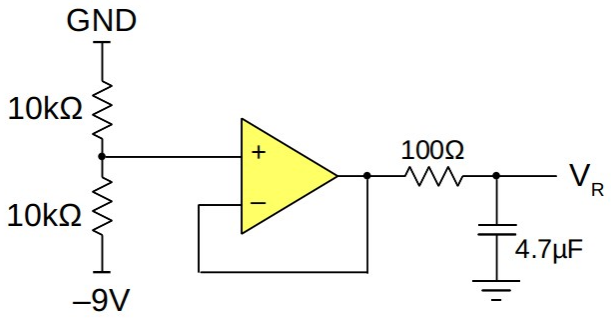

Figure 2.2.1: V_R (half-supply) generator

Level 2 – Schematics

Input Handler:

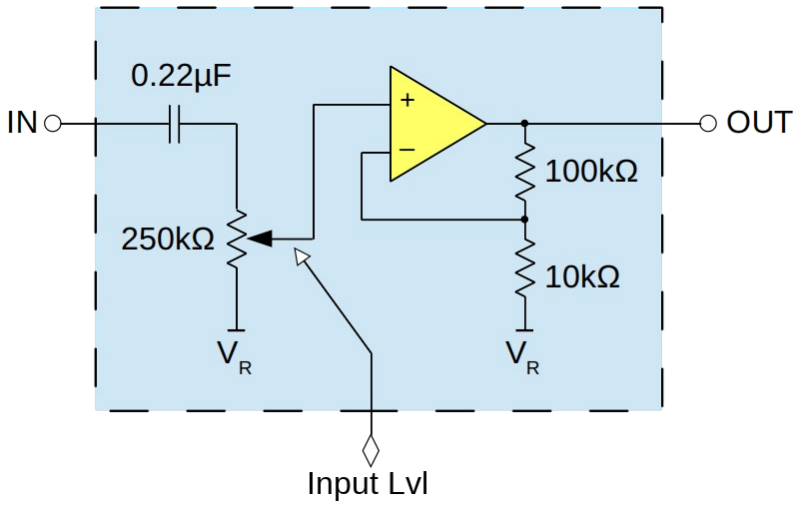

Figure 2.3: Input Handler schematic

DC-biases input to V_R, and contains a user-controllable voltage divider in conjunction with a fixed-gain amplifier.

Also current-buffers the input signal, as passive instruments (e.g. an electric guitar) often provide very high-impedance outputs.

Gain: 0x to 11x, non-inverting.
RC Filtering: High-pass, cutoff = 3Hz.

Multiplier (Π):

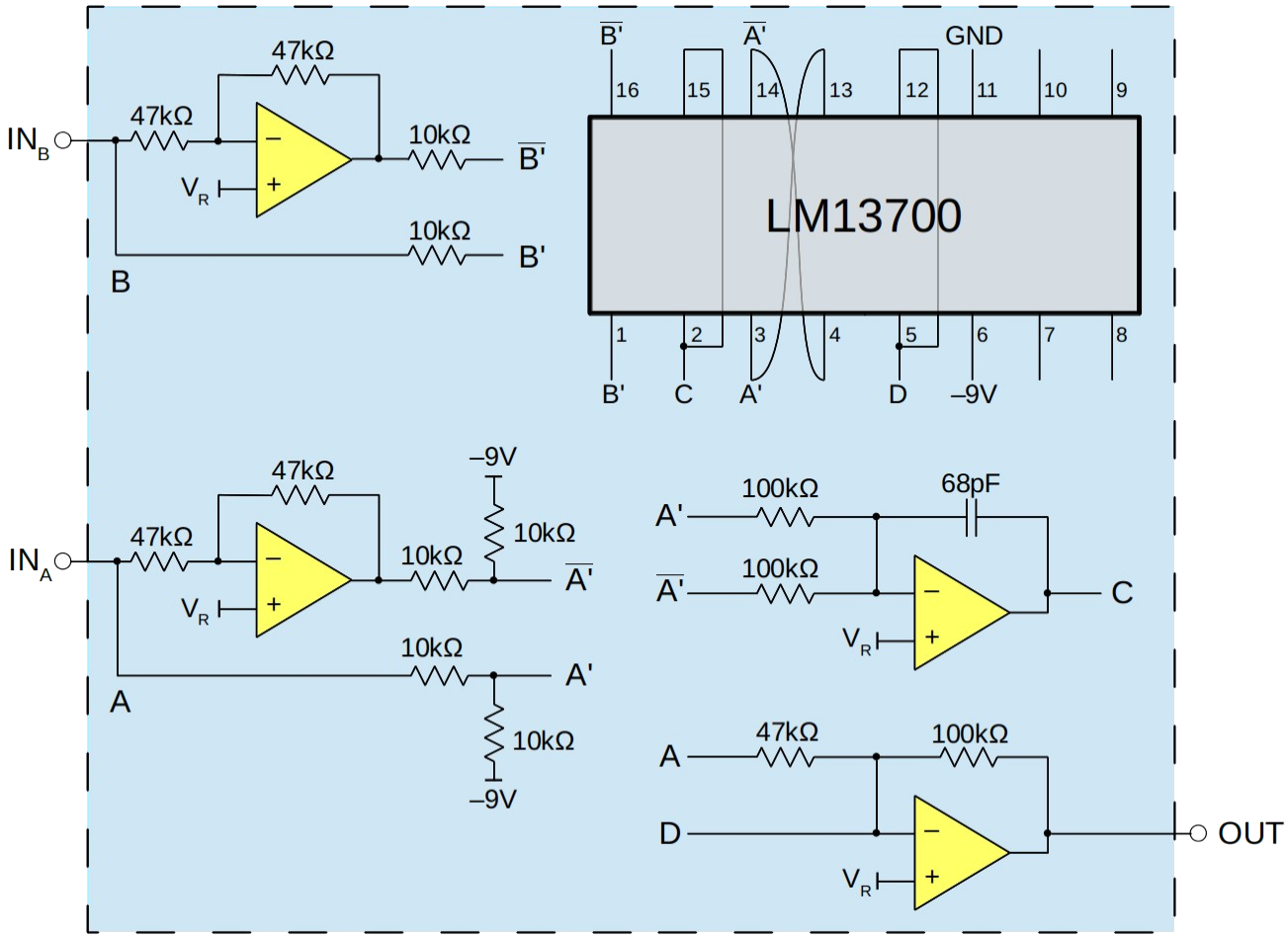

Figure 2.4: Multiplier schematic

This block generates a signal which is the product of inputs A and B, summed with a signal which is a linear scaling of A.

At the core of this component is the LM13700 operational transconductance amplifier, which when in this configuration functions as a current-mode four-quadrant multiplier.

Because of the way the LM13700 works, the handling circuitry is designed to translate voltage inputs into pairs of opposing current signals, and then sum the chip's two outputs together and translate that back to voltage mode. In addition, input A is summed directly with the LM13700's outputs at the end, using the op-amp as a summing junction. This provides a final signal which

contains a “clean” signal (directly from input A) summed with the distortion produced by the transconductance amplifier.

Multiplier: Handling Circuitry for LM13700

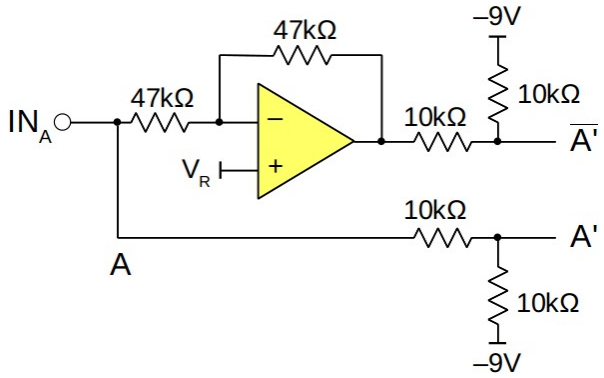

Figure 2.4.1: Handling for Input A

Input A (low-impedance voltage source) is processed to create two current sources, A' and $\overline{A'}$. 10kΩ pull-down resistors are used because the inputs these sources connect to (pins 3 and 13 for A', 4 and 14 for $\overline{A'}$) utilize pn junctions and require a continuous outflow of current.

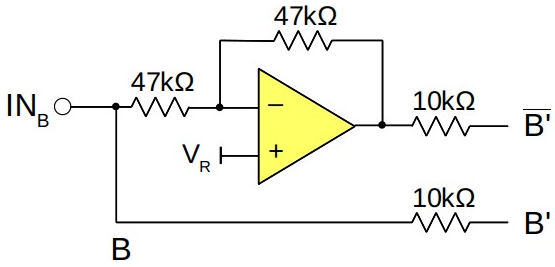

Figure 2.4.2: Handing for Input B

This is identical to the handling for input A, except without the pull-down resistors. B' and $\overline{B'}$ are connected to pins 1 and 16, which require a continuous inflow of current. (The current then flows out through the negative rail, which is far enough below V_R that pull-up resistors are not needed.)

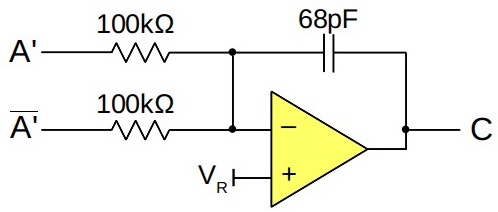

Figure 2.4.3: Handling for LM13700 diode biasing

This component's appearance is a little deceiving, so it's worth mentioning: this is *not* an integrator. Node C is connected to the LM13700's four internal input diodes, and this component ensures proper biasing across those junctions. The "true" feedback loop for this op-amp—diodes leading from C to A' and $\overline{A'}$—is not shown in the image, since it exists within the 13700 chip. The 68pF capacitor is simply there to prevent overshooting and oscillations on the part of the op-amp.

This component ensures the average of A' and $\overline{A'}$ is always V_R, effecting current outflow through pins 3, 4, 13, and 14 in the process.

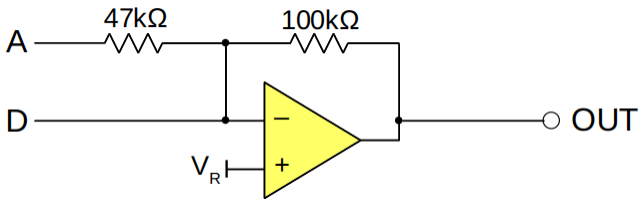

Figure 2.4.4: Handling for the multiplier output

This component serves two purposes: it converts the LM13700's current output into voltage, and it sums that result with a scaling of Input A. Note that D does not require an input resistor because it is a current source.

The resistor values for this chip are important because they determine the final output level. It's easy to overdrive the delay block if the feedback resistor has too high of a value.

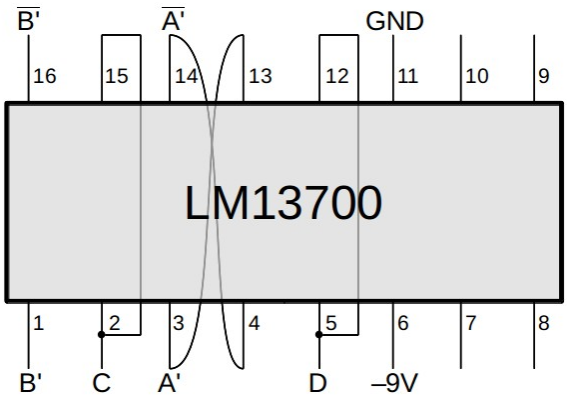

Figure 2.4.5: LM13700 pin connections

For the LM13700 itself, pins 1 and 16 are connected to B' and $\overline{B'}$, respectively. These are the amp bias inputs. Pins 2 and 15 are both connected to node C, which provides the diode biasing for inputs A' and $\overline{A'}$ (see Figure 2.4.3 for details). Pins 3 and 13 are connected to A', while 4 and 14 are connected to $\overline{A'}$.

Pins 5 and 12 are the outputs. They can be summed by direct connection because they operate in current-mode. Pins 6 and 11 are for the negative and positive voltage rails, respectively. Pins 7, 8, 9, and 10 are unused.

Signal Delay (τ) & Distortion Gain (α):

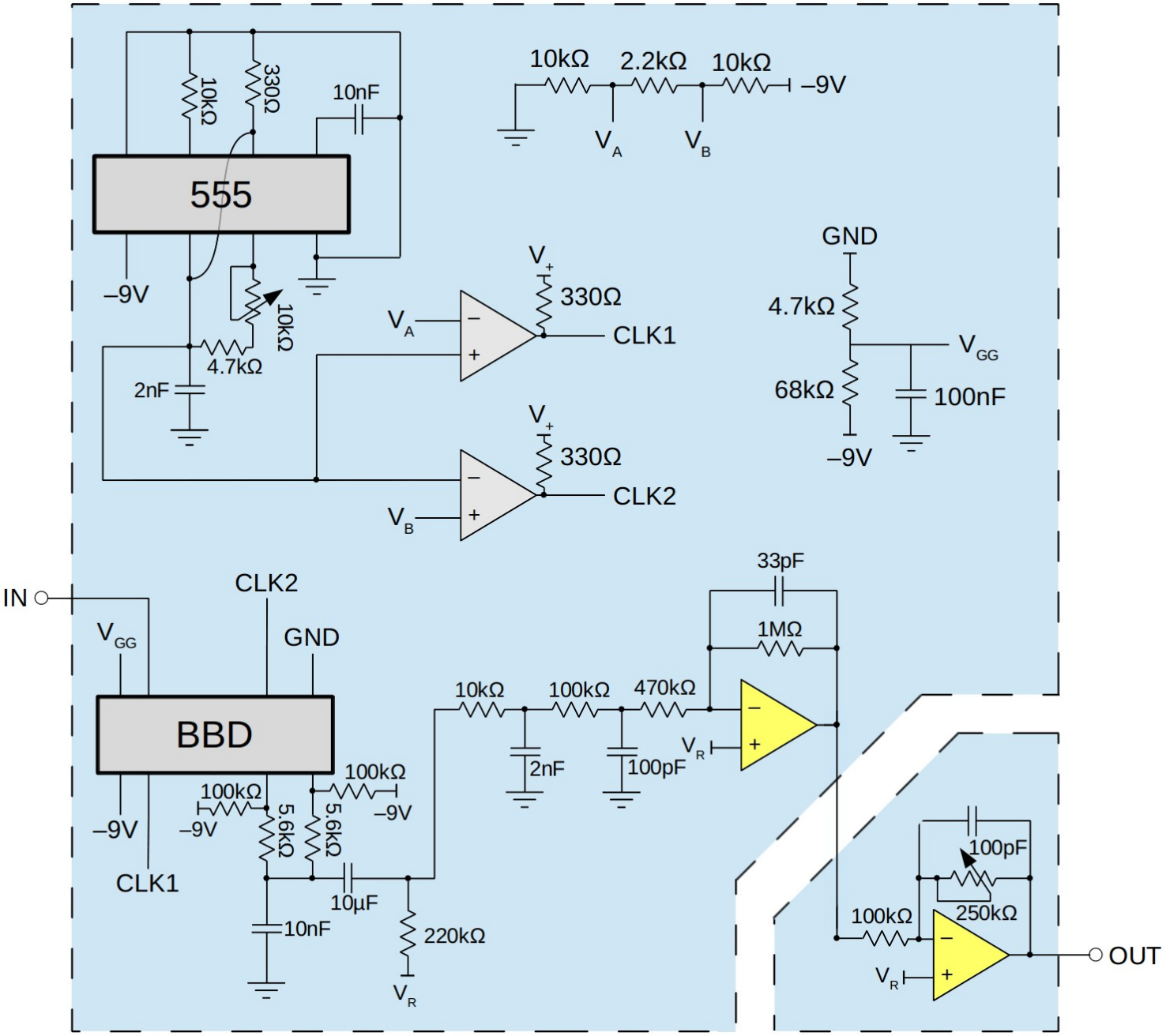

Figure 2.5: Signal Delay (main) and Distortion Gain (bottom right) schematic

This block produces a delayed version of the input, with higher frequencies (~5kHz and up) reduced. It consists primarily of a bucket-brigade delay and a 555 timer, along with the circuitry needed to handle them.

Signal Delay: Clock

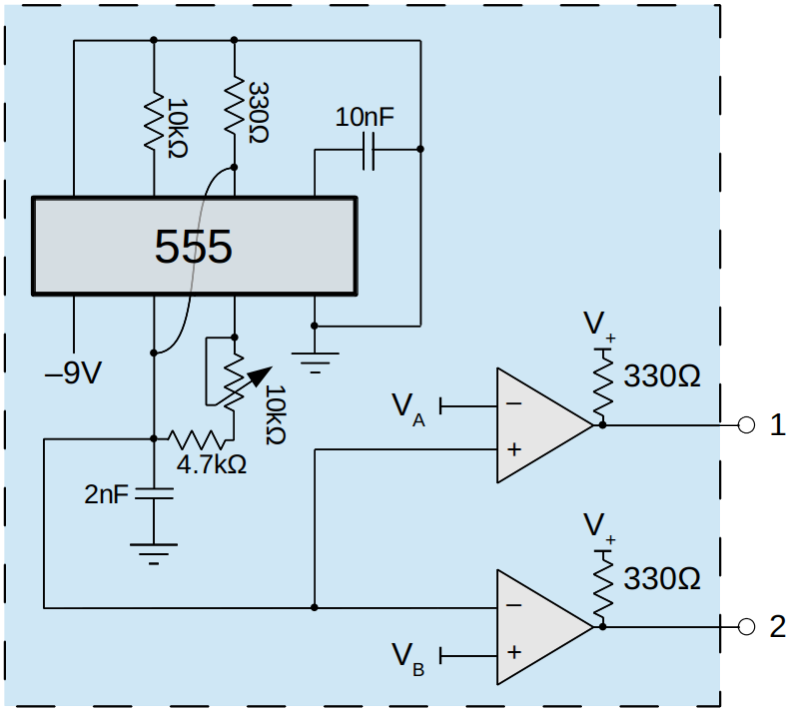

Figure 2.5.1: Signal Delay Clock

This component is designed specifically to meet the needs of the bucket-brigade delay, which requires two alternating clocks with non-overlapping “high” times. This was accomplished by using a 555 timer to generate a quasi-traigle wave (alternating RC curves) and running that into two comparators, each of which was given a slightly different DC reference voltage with which to compare it. V_A is slightly above V_R, while V_B is slightly below. This causes Output 2 to go low slightly before Output 1 goes high, and vise versa.

The BBD also requires the clocks to have a frequency between 10kHz and 100kHz. A potentiometer has been inserted into the 555’s accompanying RC circuitry to allow for user-controllable varying frequencies.

Clock – Design History

The clock for the τ block took the most design iterations out of any component. It began as a Schmitt trigger in conjunction with an integrator, with two LT1677 op-amps serving as the output stage.

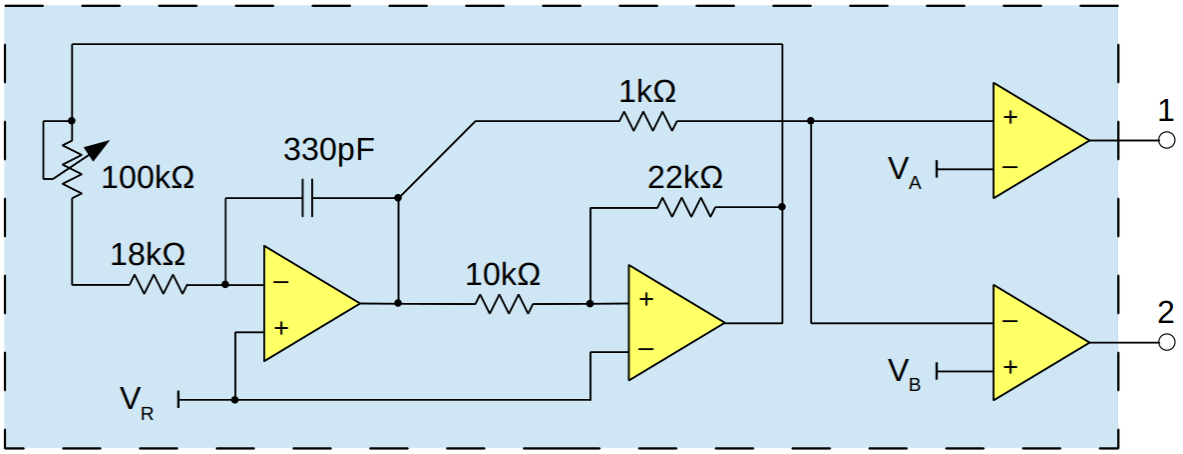

Figure 2.5.1A: Old clock for BBD

This produced a stable oscillation, but the slew rate of the LT1677 prevented a proper square wave from forming at higher frequencies. (See Figure 4.1 for a sample image.)

The LT1677 is designed to work with audio signals. Those are almost always limited to 20kHz, while this particular configuration requires a 100kHz square wave. As such, this was outside the expected usage of this op-amp, and the slew rate became a problem. As a result, a faster device would be needed.

The next iteration replaced most of the LT1677s with LT1011 comparators, in an attempt to speed up the circuit.

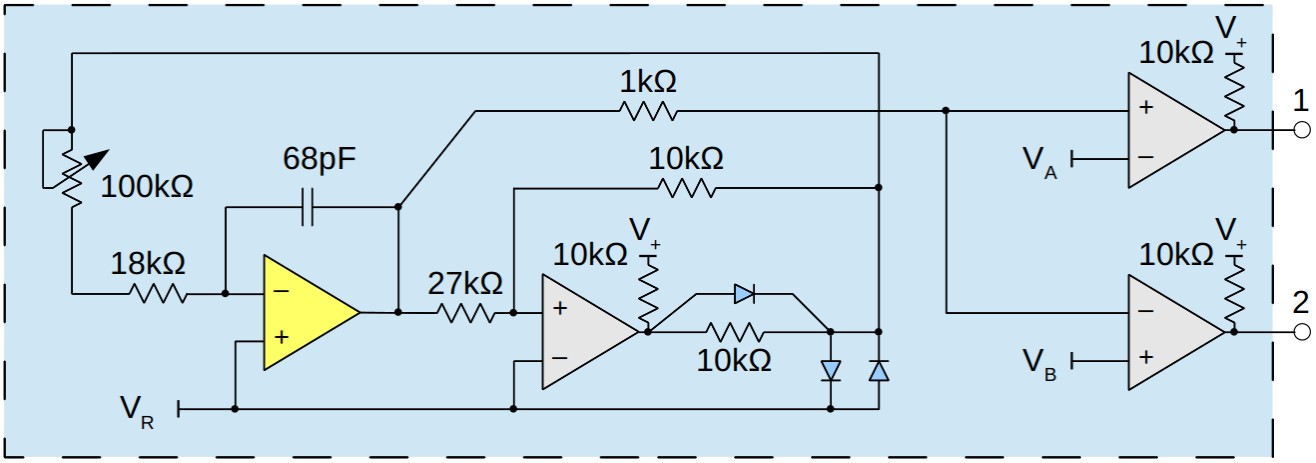

Figure 2.5.1B: Old clock, version 2

This change increased the complexity of the circuit. LT1011 chips require a bit more "handling" than LT1677s (pull-up resistors, additional control signals, etc), and at the same time diodes were added to limit the square wave to $V_R \pm 0.7V$.

This worked properly when simulated in LT Spice, but did not produce a clock signal at all when actually built and tested.

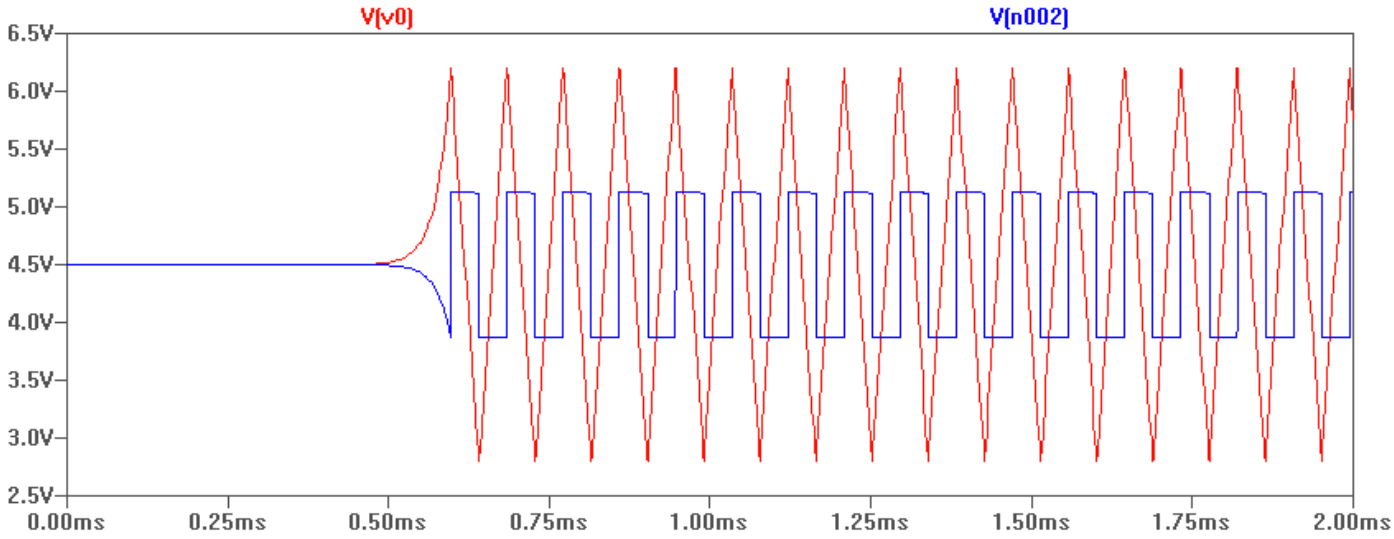

Figure 2.5.1C: Old clock v2 waveform in LT Spice, square and triangle waves.
Worked fine in simulation, did not function when built.

This deviation from real life could have been for any number of reasons. At this point, the circuit had become unnecessarily complicated and unwieldy. When troubleshooting provided no hints as to what the problem could be, the integrator/trigger design was abandoned and replaced with one utilizing a 555 timer. This was a significant deviation from the earlier designs, but it functioned as desired and became the final design.

Signal Delay: BBD

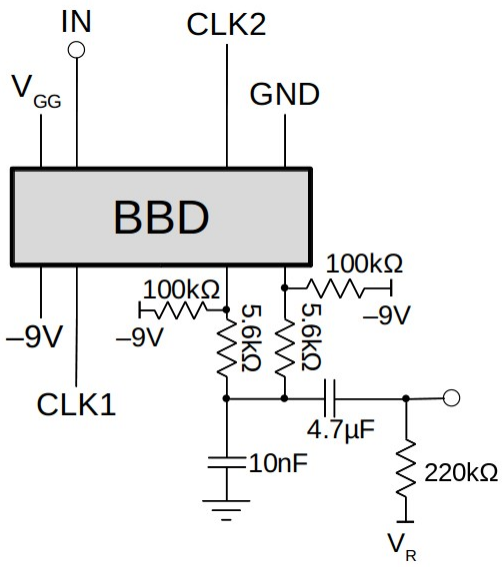

Figure 2.5.2: BBD Config for Delay Block

A bucket-brigade delay is one of the few circuits (if not the only circuit) which can delay an audio signal using nothing but analog electronics. However, they require significant associated circuitry in order to function properly.

The chip used in this circuit is the MN3205. Like most analog signal processing chips, it has pins for a power supply, and for an input and output. In addition, though, the MN3205 requires alternating non-overlapping clocks (CLK1 and CLK2), a special reference voltage which is $\sim{}^{14}/_{15}$ the distance to the positive rail from the negative rail (V_{GG}), and rather specific circuitry to handle the output.

The MN3205 has two output pins, each of which requires its own pull-down resistor. The outputs

are then run through a summing junction and AC-coupled to V_R. There's also a 10nF capacitor to ground at the summing junction, which allows that junction to function as the first part of a fifth-order lowpass filter.

Signal Delay: Lowpass Filter

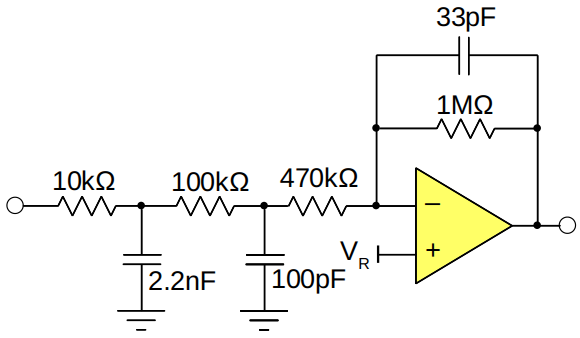

Figure 2.5.3: (most of the) Signal Delay Lowpass Filter

The lowpass filter itself is relatively simple. The first RC junction is the BBD output summing junction (see Figure 2.5.2), the next three compose the above circuit, and the final one is built into the distortion block (see Figure 2.5.5).

Only simple mathematical calculations made when designing this filter. The math for higher-order filters gets rather complicated (plus the BBD has an unknown, nonlinear output impedance) and so first-order calculations were made to determine the correct ballpark RC values, and component values were then adjusted empirically.

Signal Delay: Reference Voltages

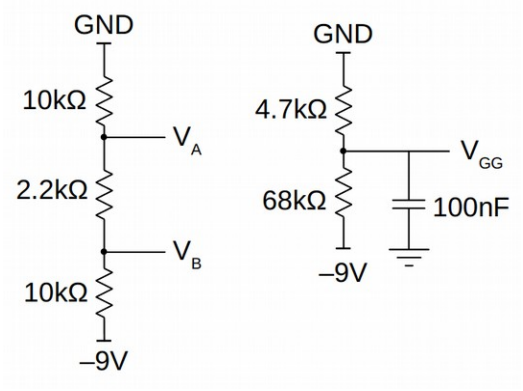

Figure 2.5.4: Signal Delay Reference Voltages

The reference voltages required for the clock and BBD are not subjected to much current draw, and therefore can be generated using simple voltage dividers.

V_A (-4.05V) and V_B (-4.95V) straddle across V_R (-4.5V). Their values were determined empirically using a trim pot, which was then replaced by a 2.2kΩ resistor.

V_{GG} (0.58V) is $^1/_{15}$ the value of the negative rail, to within 5% tolerance. This value was specified by the MN3205 BBD's datasheet.

Distortion Block

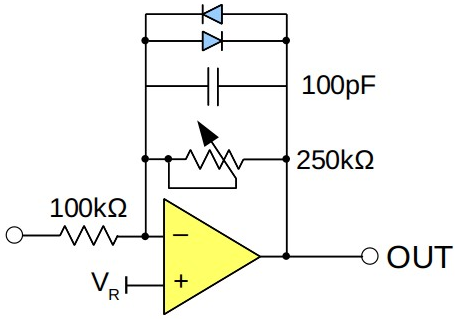

Figure 2.5.5: Distortion Block

This block serves three purposes. The first is to provide a user-controllable distortion gain level, the second is to function as a lowpass filter (the fifth such filter in the BBD's output handling), and the third is to limit the output of the Delay & Distortion circuitry to ±0.7V relative to V_R.

A capacitor in parallel with a potentiometer is somewhat atypical for this sort of lowpass filter. In this case it enforces an upper limit on the circuit's gain-bandwidth product, which holds true regardless of the user-specified distortion level.

Output Handler

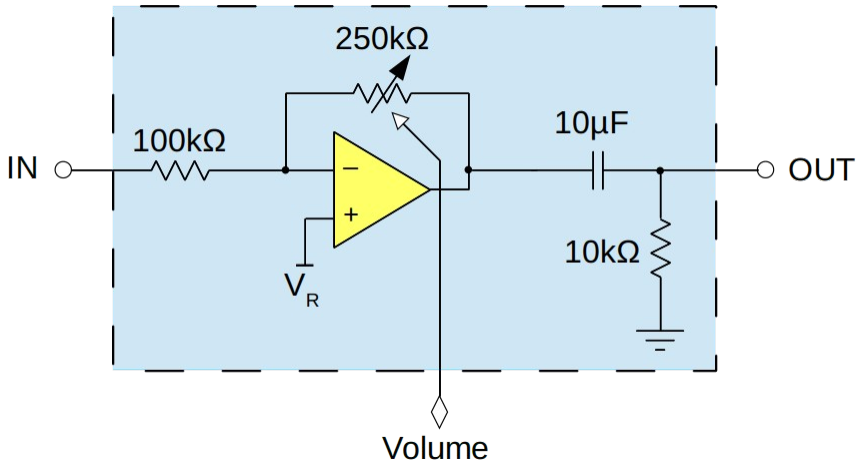

Figure 2.6: Output Handler schematic

This component DC-biases the output to GND, and provides an amplifier with user-controllable gain to control the final output volume.

Gain: 0x to 2.5x, inverting.
RC Filtering: High-pass, cutoff = 1.6Hz w/open load, 18Hz with 1kΩ load.

V. CONSTRUCTION

Construction of the circuit began on a breadboard, with small components being tested before larger components were built. In the early stages, circuit components were continuously tweaked – a small-scale DBT process repeated itself over and over, until components were stable and behaved as desired.

The multiplier and delay were by far the most complex components to build, and each required several DBT iterations before functioning properly.

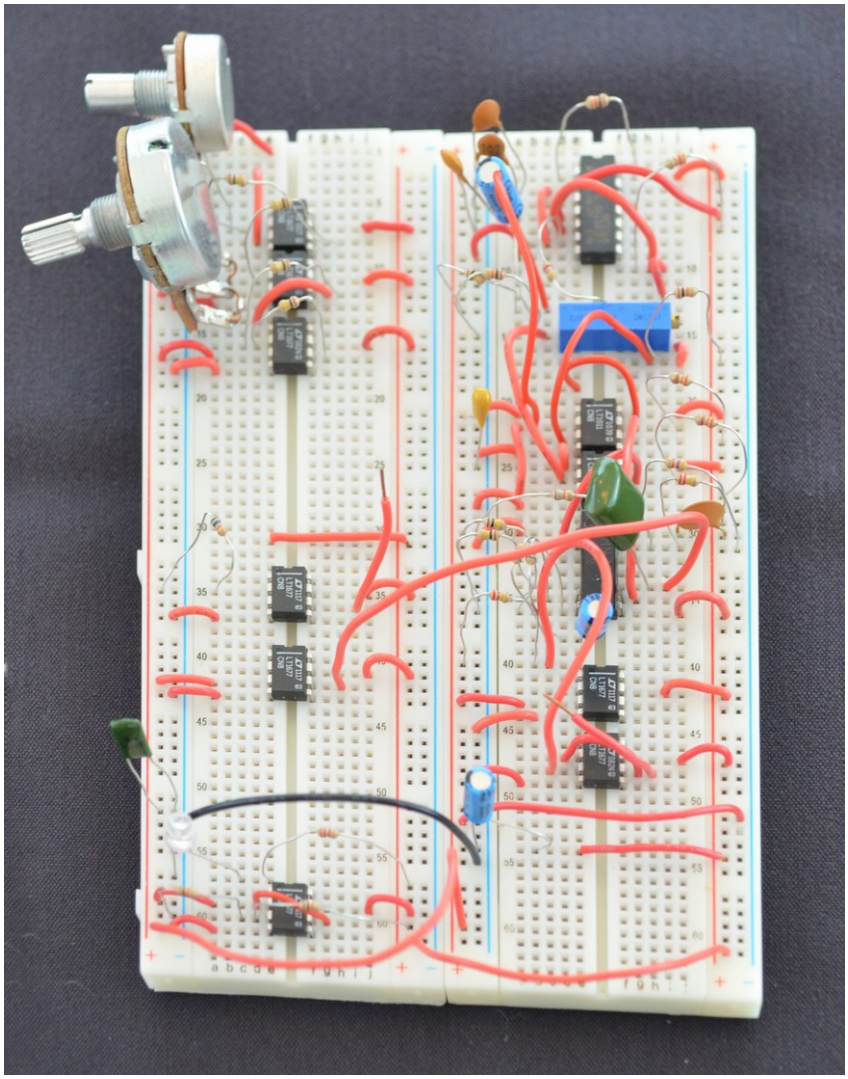

Figure 3.1: Delay Block on breadboard
(along with miscellaneous handling circuitry)

Once designed, built, and tested successfully on a breadboard, a solder diagram was drawn up for each component. This process began with the signal multiplier, since that was the first major component to have its design completed.

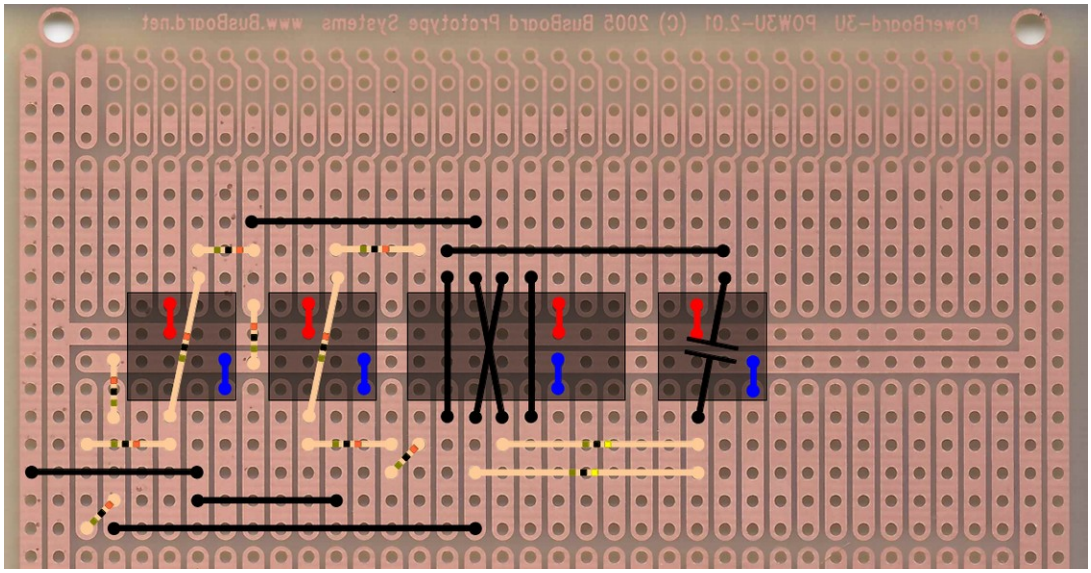

Figure 3.2: Signal multiplier solder diagram

After each the multiplier had its layout drawn up, it was assembled on the solderboard. It was tested after soldering to ensure it had been built properly.

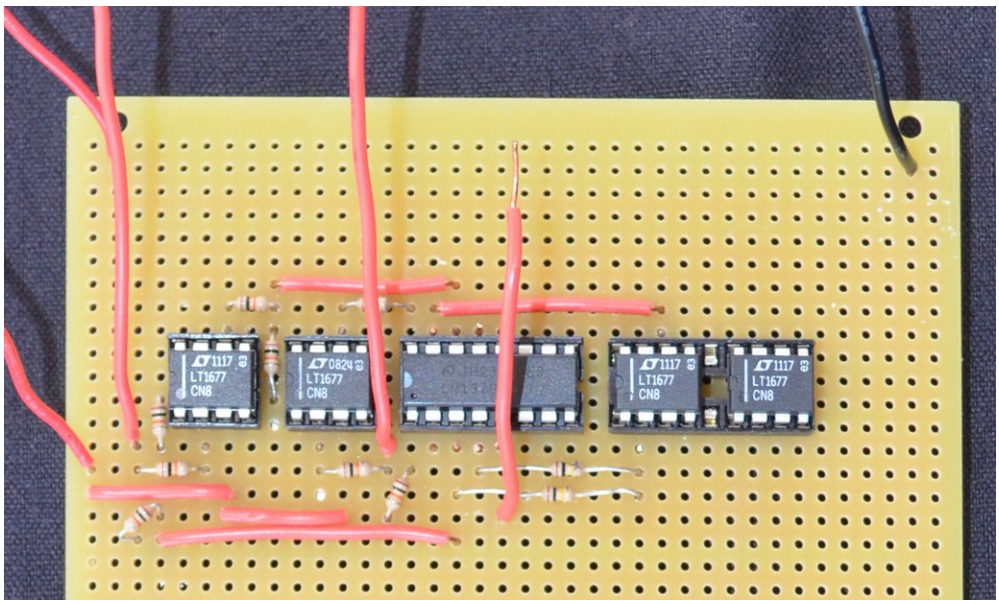

Figure 3.3: Signal Multiplier alone on solderboard

Once the delay block was done, a solder diagram was drawn up for the whole circuit.

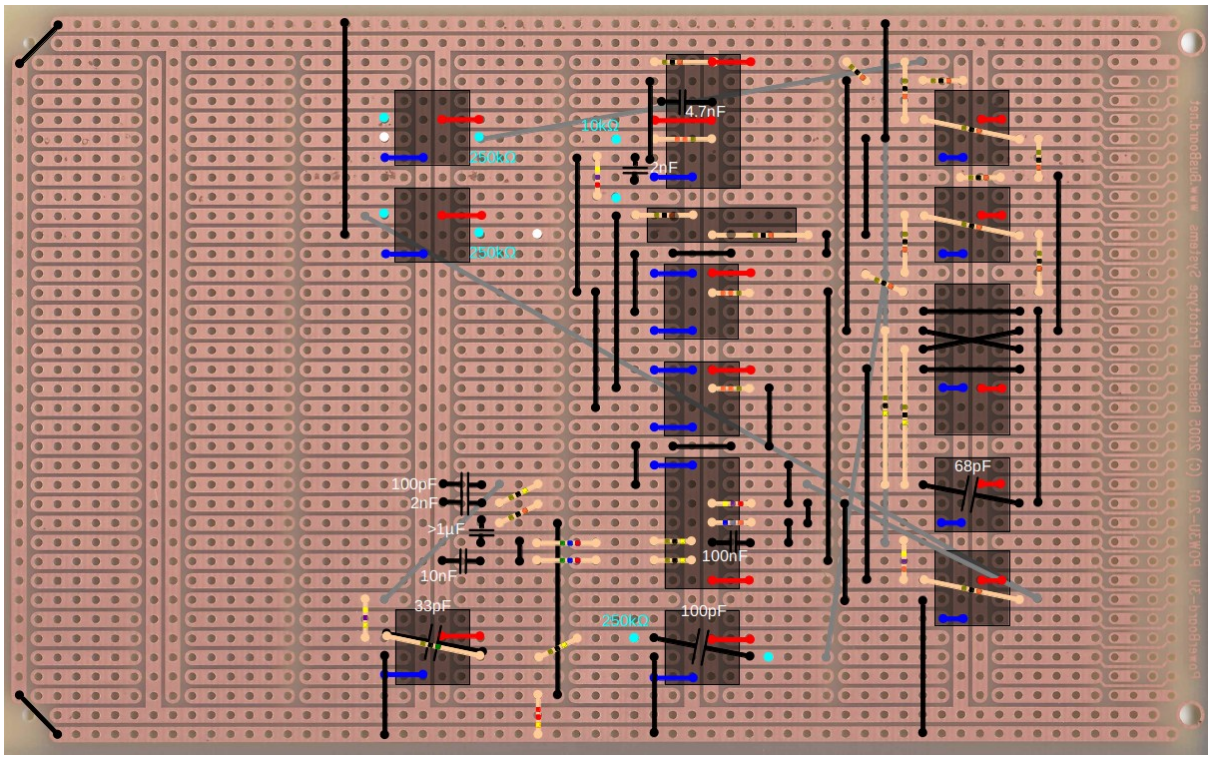

Figure 3.4: Solder diagram of entire circuit

This was not meant to be a perfect representation of the final circuit layout – it served as a guide for where to lay out the components, allowing for improvisation if needed.

The figure above (along with Figure 3.3) is a mirror image of the solderboard's underside, overlayed with circuit components. This results in a diagram of the components in their positions on the solderboard's front, with copper traces from the back shown as well.

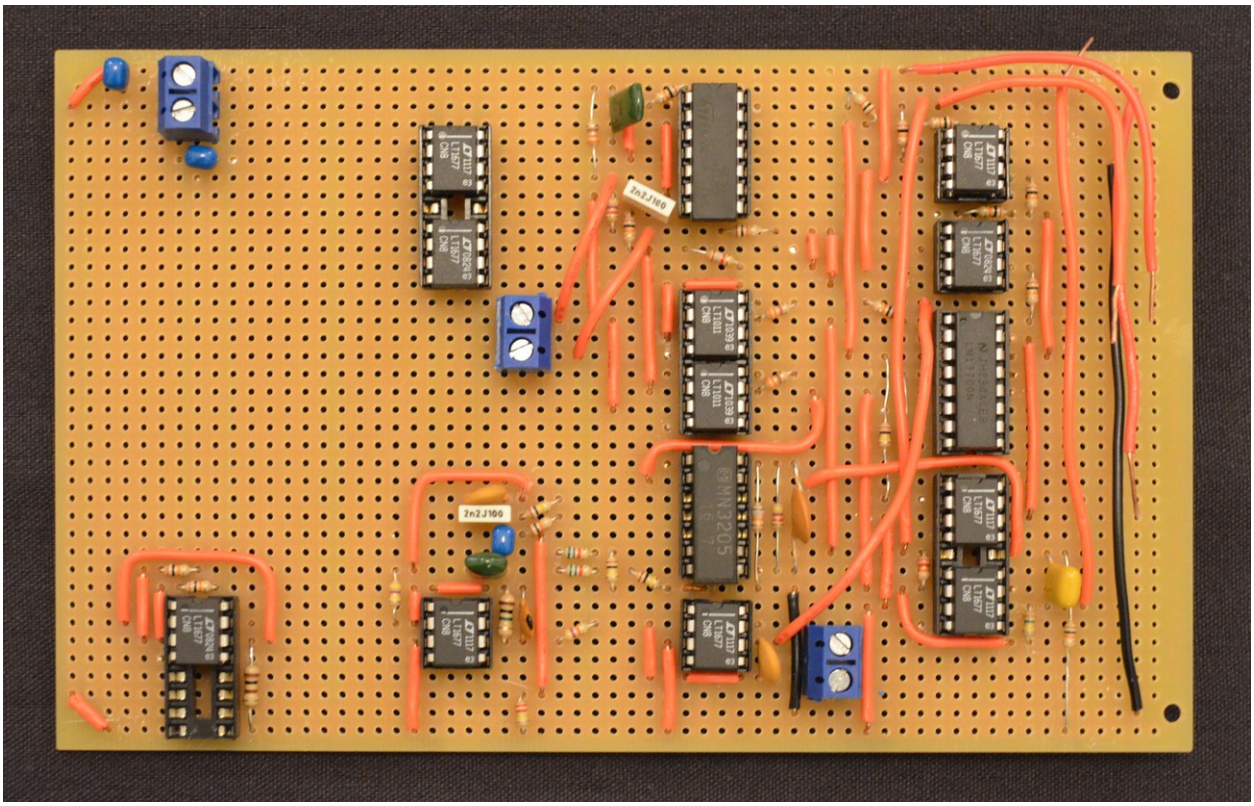

Figure 3.5: Circuit soldered according to diagram

The rest of the circuit was then soldered into place. The wiring was kept as neat and tidy as possible, although a couple connections necessitated the use of a long, arcing wire from one part of the board to the other. The ICs were placed in sockets, so they could easily be removed and replaced if need be.

VI. TESTING

Before the final circuit was assembled, each component was tested individually.

Delay Block (τ)

The delay circuit was the most troublesome, and the most thoroughly tested.

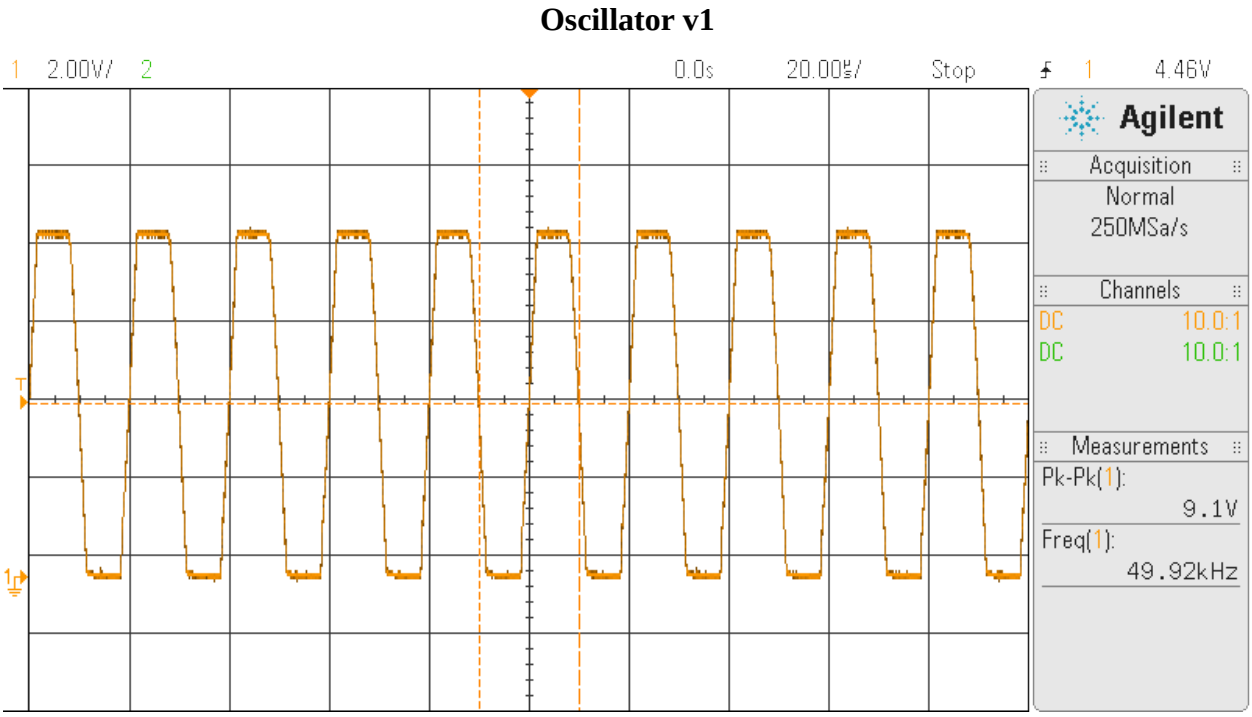

Figure 4.1: Early oscillator design. Used op-amps instead of a 555.

Initially the delay block used a pair of op-amps (LT1677) to generate oscillation; it was replaced with the 555 timer used in the final design due to slew rate issues as seen above. (See Figure 2.7 for schematic.)

Oscillator v2

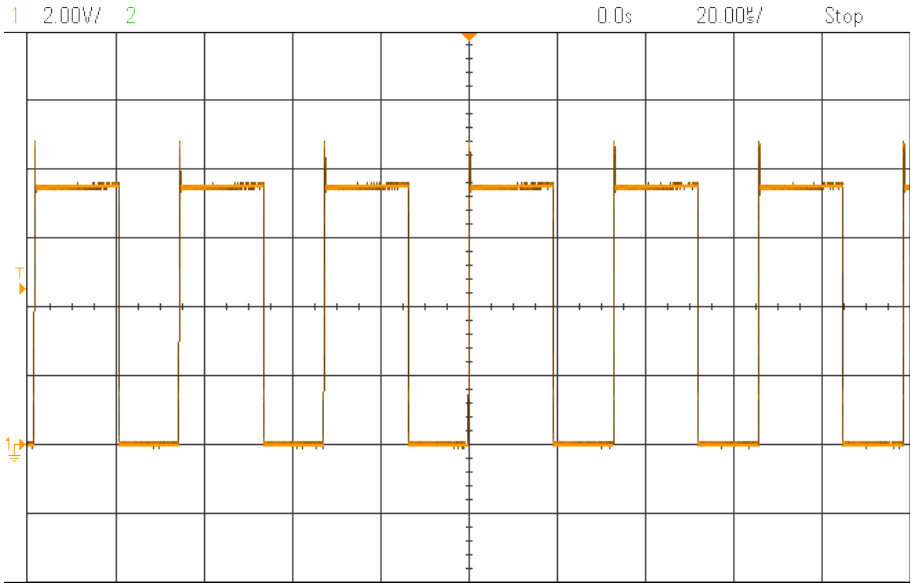

Figure 4.2: 555 timer behavior (early 555 design)

Early testing of the 555 oscillator circuit for the delay block. The 555 timer did not reach the positive rail (+9V in this case) and did not have a 50% duty cycle.

Pull-up Resistor

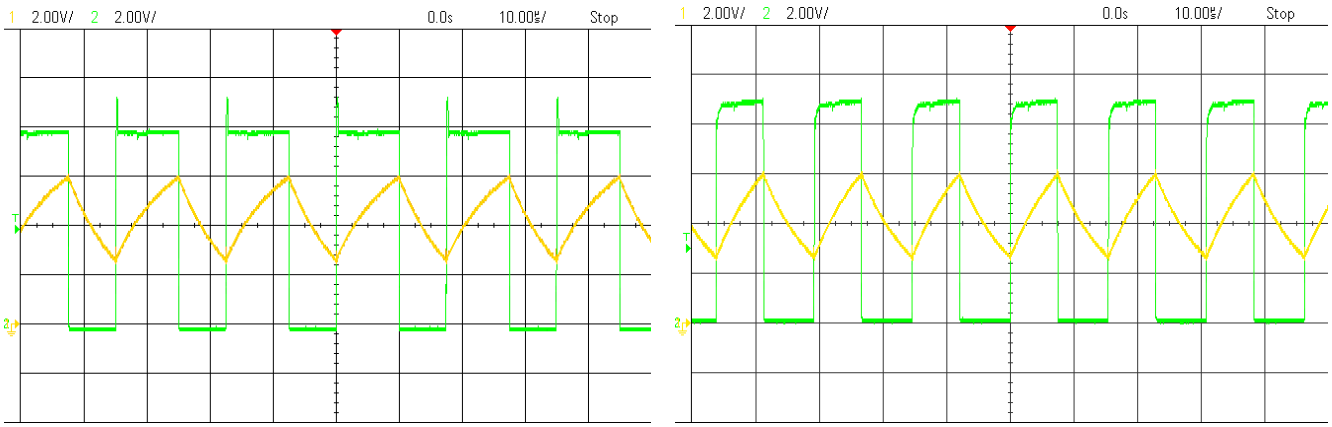

Figure 4.3: 555 behavior without (left) and with (right) 330Ω pull-up resistor

The 555's off-nominal behavior was fixed by using a 330Ω pull-up resistor. With that in place, it gave a much better square-wave output (50% duty cycle, reached both rails), and the resulting RC curve of the oscillator circuit had proper symmetry.

Comparator Outputs (Alternating clocks)

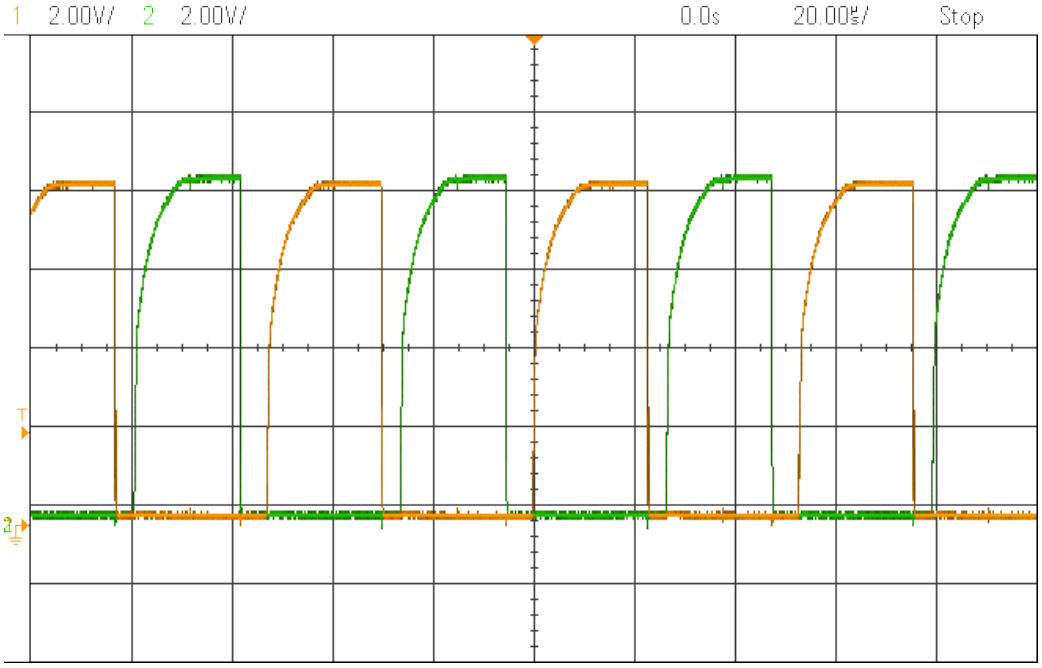

Figure 4.4: Comparator clock behavior (early design)

Alternating clocks driving the BBD within the delay block. Note how they are not perfect square waves.

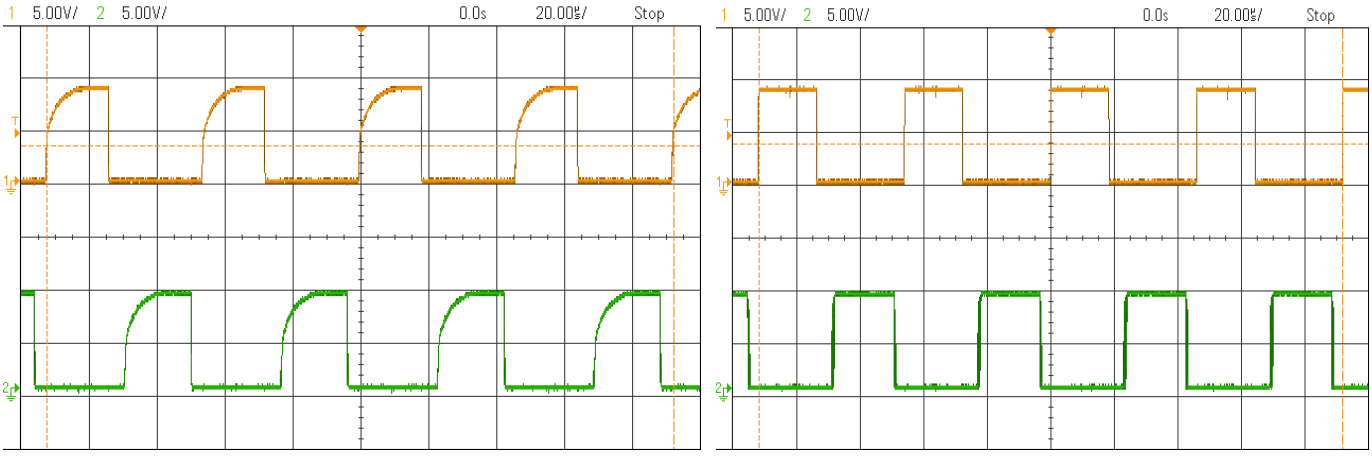

Figure 4.5: Alternating clocks with (left) and without (right) the load (BBD) attached

The comparator outputs were tested with and without the bucket-brigade delay attached. The resulting scope images suggested that the non-ideal clock behavior is a result of the pull-up

resistors being too large for the load and frequency in question.

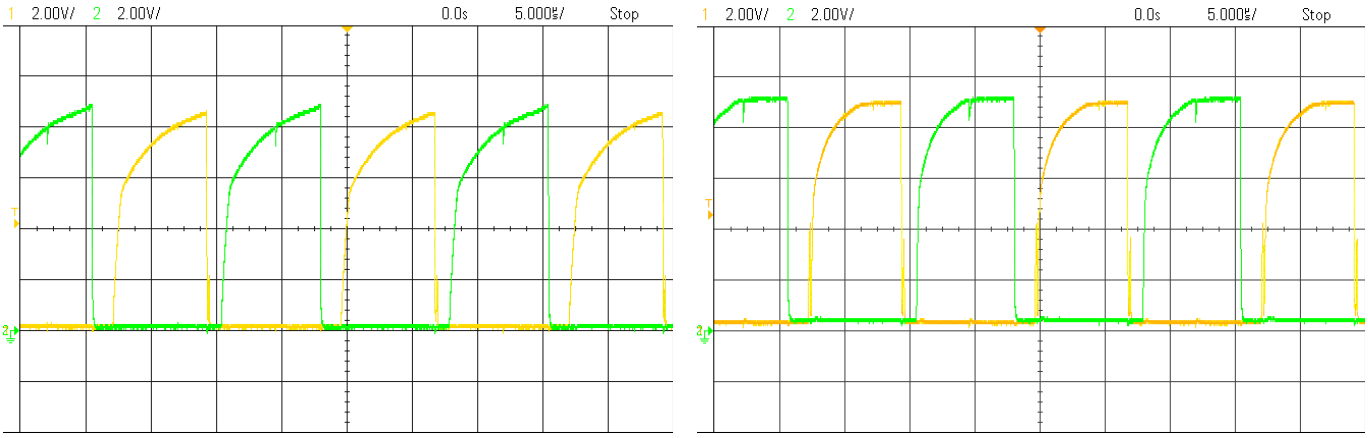

Figure 4.6: Clocks with 1kΩ resistors (left) and 330Ω resistors (right)

In the next iteration, the comparators were given smaller pull-up resistors, and their behavior (while still not perfect) improved significantly. (Note that Figure 4.6 works on a smaller timescale than Figure 4.4.)

Signal I/O

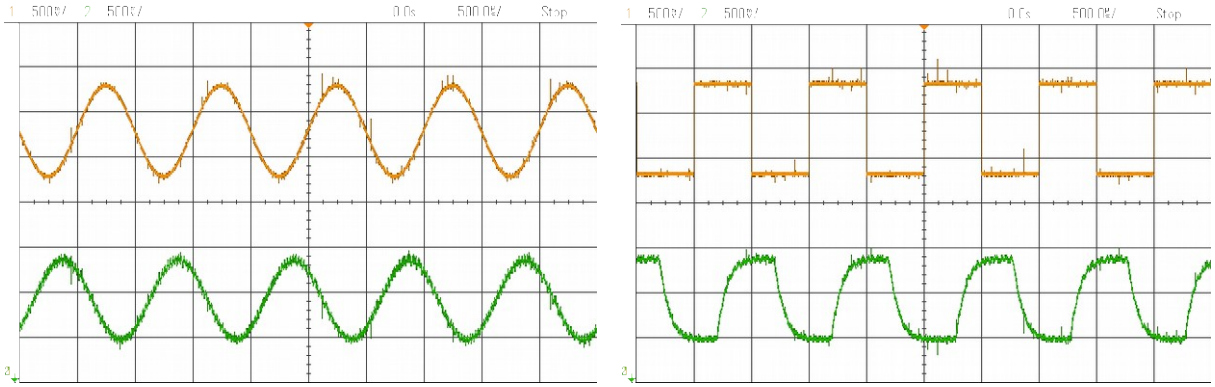

Figure 4.7: In/out for sine and square waves (early design)

The above scope captures are from early testing I/O testing of the delay block. Despite flaws in the timer, the delay block did pass a sine wave properly. The square wave lost its high end, demonstrating the low-pass properties of the block.

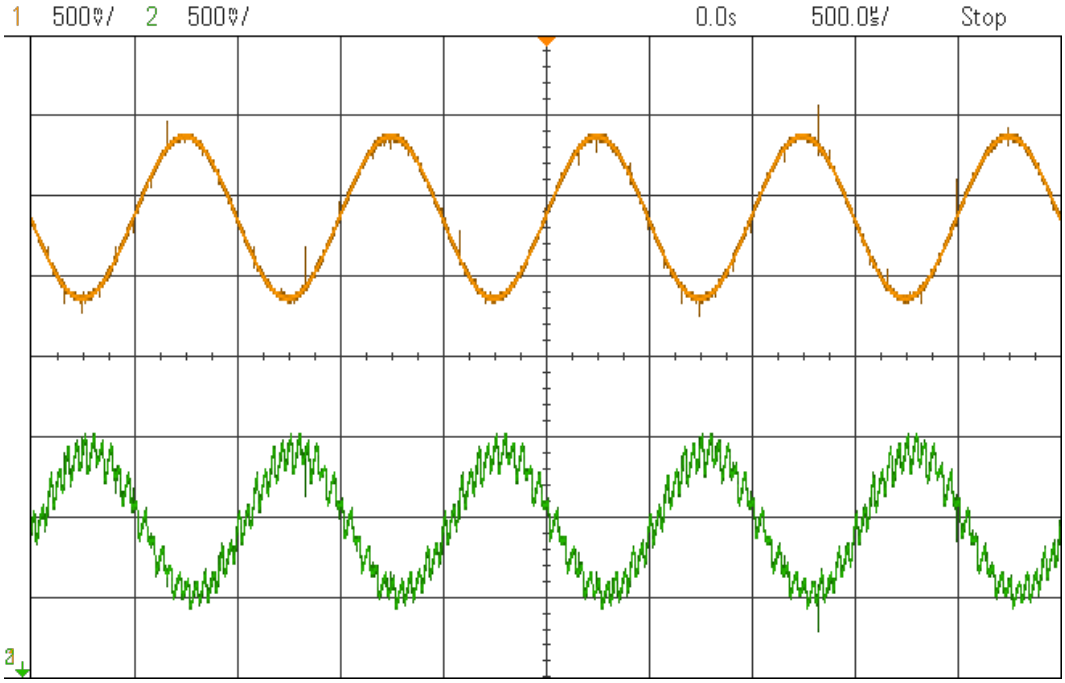

Figure 4.8: Sine wave in/out with slower clock (early design)

I/O with 555 set to a lower frequency, demonstrating issues which can arise when the clock is set too slow. As a result, the clock's design was modified to give it a more constrained frequency range.

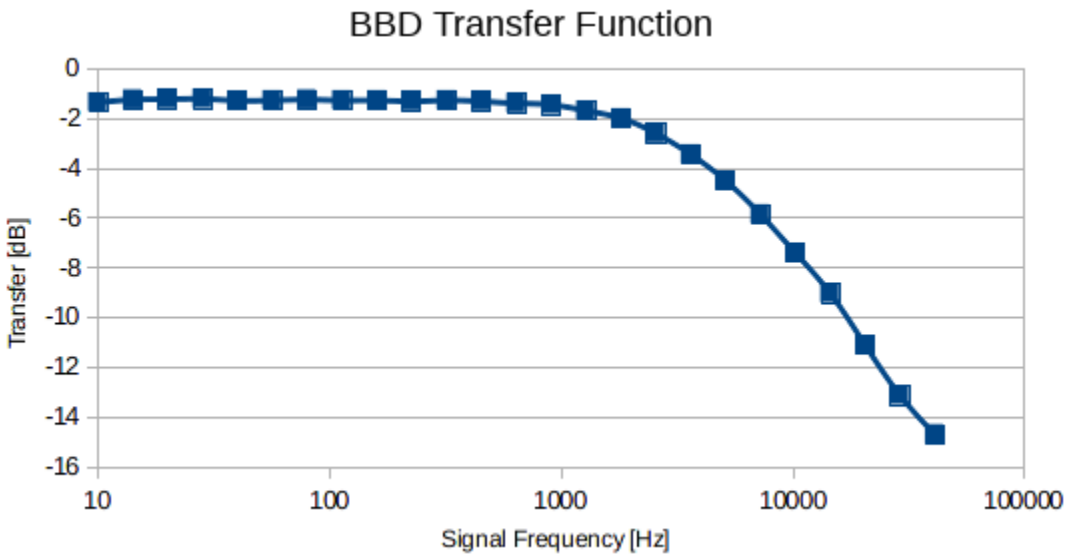

Figure 4.9: Bode plot of "raw" BBD (without output RC filter)

During the DBT process, the BBD was tested with minimal input/output handling (i.e. the signal was given no RC filtering, except for AC coupling) to determine its transfer characteristics.

Based on the resulting graph above, and on the noise properties of the BBD, it was determined that the output was best handled by a high-order (4^{th} or more) low-pass filter with a cutoff frequency of roughly 3-10kHz.

Signal Multiplier (II)

The signal multiplier required significant testing, although not as much as the delay block. Much of the testing was done in “pure multiplier” configuration, without the linear summing for input A.

Linear Range

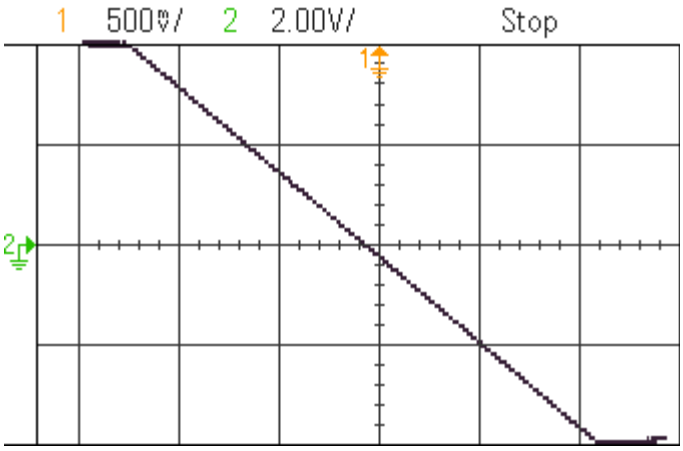

Figure 4.10: Output linear range of multiplier

The output linear range of the multiplier was tested and found to be ±4V, relative to V_R. (The output reached its min/max at 0.5V away from the rail, in both directions.)

Step Response

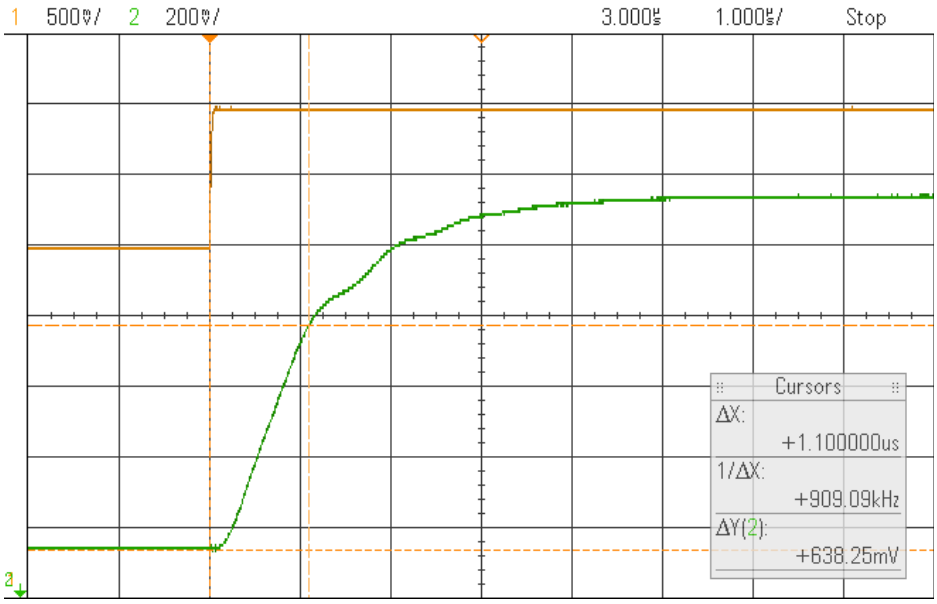

Figure 4.11: Step response of multiplier

The multiplier has a step response of 1.1µs, which is fast enough for audible frequencies with plenty of headroom.

Response to Sine × DC inputs

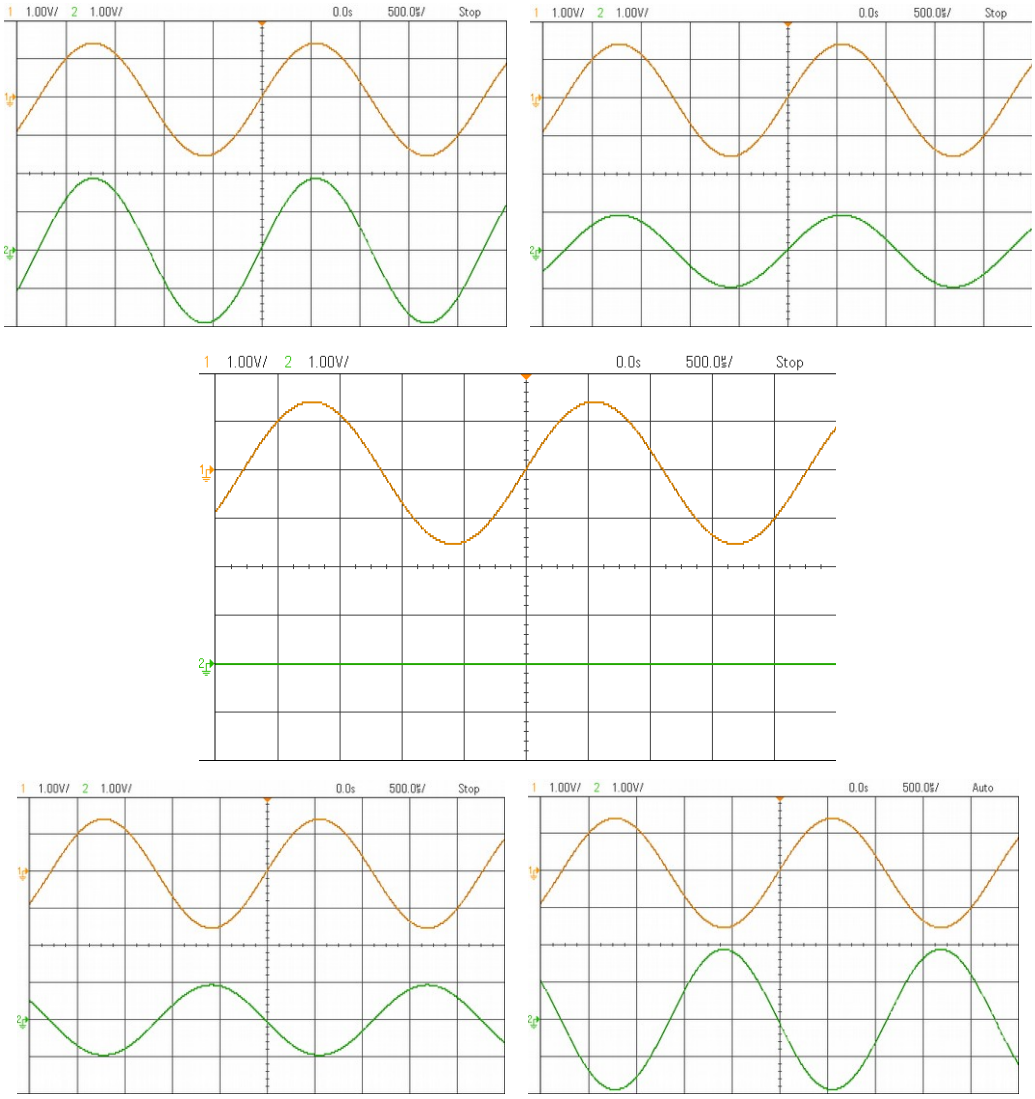

Figure 4.12: Response (bottom) to sine wave (top) and DC inputs
(In order: -2V, -1V, 0V, +1V, +2V relative to V_R)

The multiplier was tested with a sine wave in the A input and a DC voltage in the B input. Output increased in magnitude as DC voltage deviated further from V_R, switched phase as DC voltage crossed over V_R, and dropped to 0V when DC voltage was set to V_R.

Inputs A and B were swapped, and the behavior of the multiplier did not change noticeably.

Sine × Sine

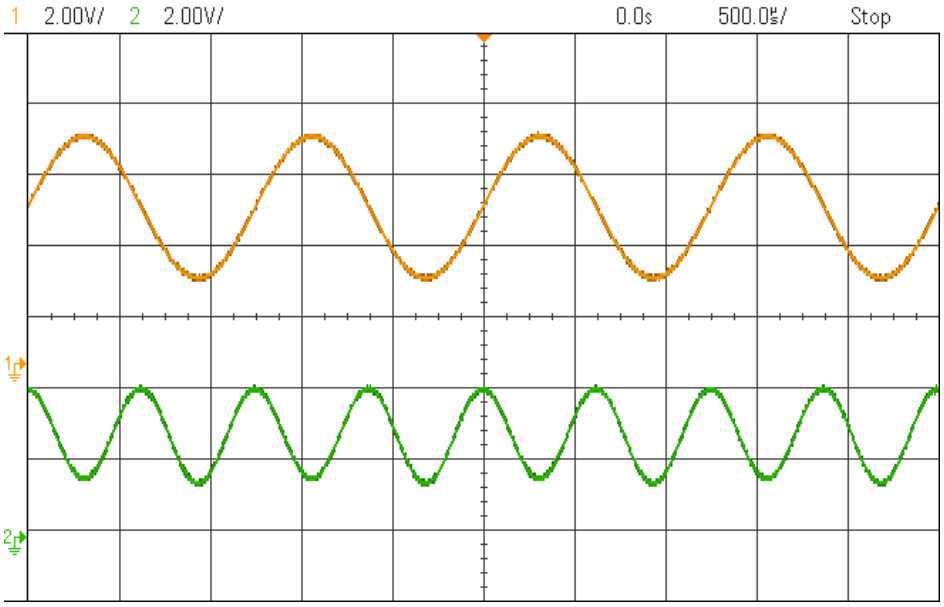

Figure 4.12: Squaring of a sine wave

Plugging the sine wave into both inputs yielded a sine wave with twice the frequency. No noticeable distortion or excess noise was created.

Triangle × Triangle

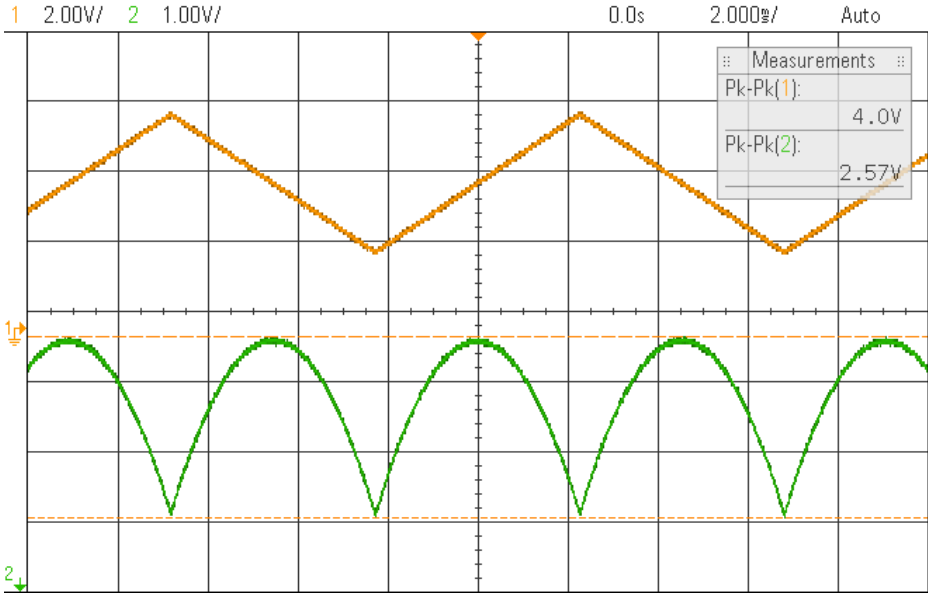

Figure 4.13: Squaring of a triangle wave

Giving both inputs a triangle wave yielded a repeating parabolic arc, with twice the input frequency. Both of these scope images were evidence that the multiplier worked as expected.

Behavior of Completed Circuit

Once fully assembled, the circuit functioned as intended. It created a moderately distorted sound containing both even and odd harmonics.

One interesting facet of its behavior is that there's no dynamic range limiting. For clipping circuits, increasing input amplitude does not necessarily increase output amplitude, while for this circuit that was not the case. In fact, the use of a multiplier in a feedback loop is more likely to cause dynamic range expansion than compression. This is consistent with the characteristics of even harmonics – they expand a signal rather than clamping down on it.

Another point to note is that the circuit requires a bit more "tuning" than a clipping circuit. The input gain must be set to the right level, and so must the feedback loop gain. But if either gain is set too high the output is too noisy, and if either is too low the output sounds too clean.

If set up correctly, however, the circuit produces a novel, unique tone. There's a loud, clear second harmonic in the output, which sounds like a second instrument playing the same note one octave up. Also, pitch bends can cause tremolo, especially when there's a long delay time.

VII. Conclusion

Despite early troubles, the circuit worked in the end. The goal was for the circuit to produce distortion via an unconventional method (specifically multiplicative feedback) which creates a different harmonic profile. In this, it succeeded: the circuit produced a type of distortion very different than what is normally heard, and it created even harmonics, all using an analog transistor design.

Getting everything to behave was not easy, however. The bucket-brigade delay required a bulky multi-order lowpass filter in order to function properly, and the operational transconductance amplifier required a lot of handling circuitry to translate signals to and from current mode. Signal multiplication and delay are not usually implemented in the analog domain, and indeed it is tricky to do so. It *is* doable, however, and that fact is a good sign that many esoteric things can indeed be performed with purely analog circuitry.

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IX. APPENDICES

Appendix A: Analysis of Senior Project Design

The multiplicative feedback audio distortion circuit works by running a signal multiplier and delay line together in a feedback loop. One input to the multiplier is the signal input for the circuit, while the other is the output of the delay line. This setup multiplies the input by a delayed version of the output, creating even harmonics in the process.

Perhaps the largest hurdle of this project is that a signal multiplier and a delay line are not usually implemented in the analog domain. This circuit, however, is all analog. The multiplier was made out of an LM13700 operational transconductance amplifier, while the delay line was made out of an MN3205 bucket-brigade delay. Both required significant auxiliary circuitry to function properly.

Also of issue was determining power supply voltage conventions. Most guitar effects pedals work on a 9V supply, but it's never made clear which end is treated as "hot" and which as "ground". When working with a floating supply such as a 9V battery this is not much of an issue. When working with an external DC supply, however, it is possible for a ground loop to occur if the locations of power ground and signal ground are not properly anticipated by the circuit and instead set to different voltages.

Appendix B: Specifications

Modes of Operation

- Distortion mode
- Bypass mode

Interface

- –9V power supply, ground
- High-impedance input
- Low-impedance output
- Control knobs
    - Input lvl
    - Distortion
    - Delay
    - Volume

Appendix C: Cost Table

Component	Number	Price/unit	Price	Bulk $/unit	Bulk price	Source
LT1677	9	$2.60	$23.40	$2.30	$20.70	Linear Technologies
LT1011	2	$1.58	$3.16	$1.40	$2.80	Linear Technologies
LM13700	1	$1.13	$1.13	$0.69	$0.69	Mouser Electronics
NE555	1	$0.45	$0.45	$0.17	$0.17	Mouser Electronics
MN3205	1	$8.00	$8.00	$8.00	$8.00	eBay
Resistor	38	$0.05	$1.90	$0.03	$1.14	Mouser Electronics
Capacitor	11	$1.00	$11.00	$1.00	$11.00	Mouser Electronics
Solder Board	1	$11.00	$11.00	$1.00	$11.00	Amazon.com
Project Enclosure	1	$21.00	$21.00	$21.00	$21.00	Amazon.com
¼" Phone Jack	2	$1.04	$2.08	$0.74	$1.48	Mouser Electronics
DPDT Stomp Switch	1	$3.50	$3.50	$3.50	$3.50	Amazon.com
Total			**$86.62**		**$81.48**	

Figure C1: Cost Table

The most expensive components are the op-amps, the project enclosure, and the solder board. These three alone account for about 60% of the product's cost. Cost could be reduced by using less-expensive models for op amps which aren't on the signal path, and by finding a cheaper project enclosure. The enclosure was expensive partly because it was so large, and so product miniaturization could lead to reduced costs.

The "bulk" prices were taken from listed prices when purchasing quantities of 100 or more. The bulk price is only 6% cheaper than the non-bulk price; the difference is small partly because no bulk discount for the solder board and project enclosures could be found, and because many of the devices which did have bulk discounts were not that expensive in the first place (e.g. resistors and the 555 timer).

Appendix D: Schedule & Time Estimates

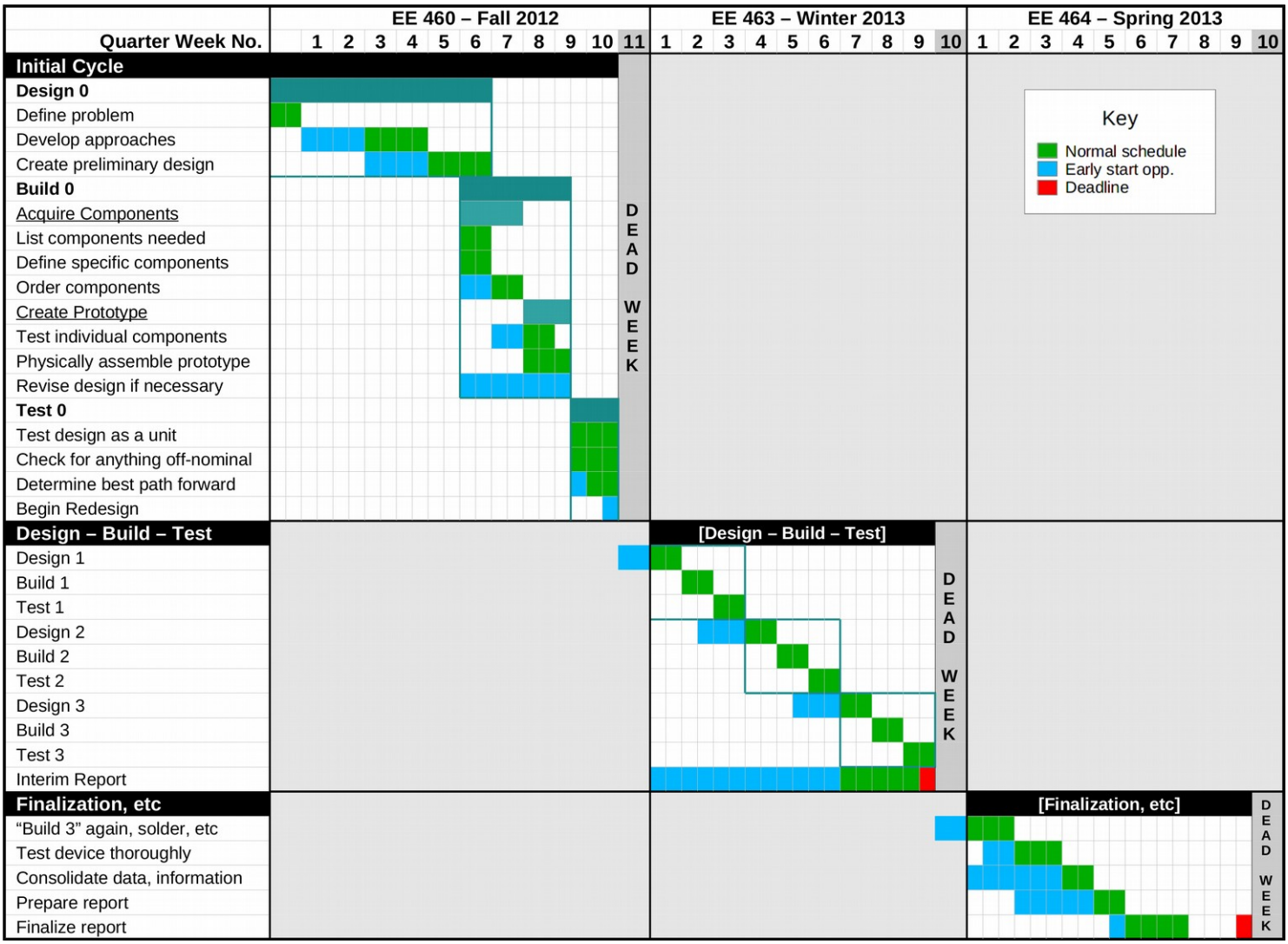

Figure D1: Original Gantt Chart

Shown above is the project's original timeline created at the beginning of the academic year. When compared with reality, it was overly optimistic. Numerous setbacks prevented a working prototype from being built until much later than originally anticipated. The design-build-test process wound up happening for each component individually through many iterations before working components were put together in a single circuit.

The actual development timeline looks more like this:

Fall 2012:

- Selected project
- Designed L0 and L1 block diagrams
- Determined which components to use
- Created preliminary report for EE 460

Winter 2013:

- Acquired components
- Designed preliminary circuits
- Tested components on breadboard
- Built delay block on breadboard
- Built signal multiplier on breadboard
- Created interim report

Spring 2013:

- Finalized multiplier design
- Redesigned delay block
- Soldered multiplier
- Re-redesigned delay block
- Acquired proper-valued potentiometers, plastics knobs, etc.
- Fixed issues with delay block
- Soldered project together
- Created final report