

Constant Conduction Angle Bias Generation for Monolithic RF Power Amplifiers

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Table of Contents

Background	4
Constant Conduction Angle Theory.....	5
Class B Operation	6
Class C Operation	6
Maintaining a Constant Conduction Angle.....	6
Proposed Circuit	7
Equal Input Voltages, Unequal DC Currents.....	8
Equal Input Voltages, Unequal DC Currents.....	9
The Hybrid Approach	10
Sample Waveform Simulations.....	11
Forcing a Class B Curve to Bias a Class C Amplifier	14
Implementing with Actual Transistors	15
Class B I_{DC} vs. V_{IN} Generation.....	16
Scaled Class B V_{IN} vs. I_{DC}	17
Constant Conduction Angle Biased Class C I_{AC} vs. I_{DC}	18
Simulations Demonstrating Effect of Current and Voltage Ratios on Linearity.....	20
Constant Current Drain to Adjust Bends in Linearity Plots.....	26
Two Tone Intermodulation Distortion.....	27
Two Tone Intermodulation Simulations for 18 kOhm Bias Resistor.....	28
Two Tone Intermodulation Simulations for 100 kOhm Bias Resistor.....	29
Tuning Intermodulation Distortion with Constant Current Drain.....	30
Suggested Method For Tuning Amplifier.....	32
Conclusion	32

Figures

Figure 1) Voltage and current waveforms for the ideal turn on approximation	5
Figure 2) Proposed constant conduction angel bias generation circuit	7
Figure 3) Equal input voltage, unequal DC current scaling implementation	8
Figure 4) Equal DC current, unequal input voltage scaling implementation	9
Figure 5) Current in collector of Class B biased transistor, Q1	11
Figure 6) Current in collector of Constant Conduction Angle biased transistor, Q3.....	11
Figure 7) Input voltage to Class B biased transistor, Q1.....	12
Figure 8) Input voltage to Constant Conduction Angle biased transistor, Q3.....	12

Figure 9) DC Voltage at inverting op amp input	13
Figure 10) DC voltage at non inverting op amp input	13
Figure 11) Op amp output voltage, bias level for Class C biased transistor, Q3	13
Figure 12) I_{DC} vs. V_{IN} for ideal Class B amplifier and I_{DC} vs. V_{IN} for ideal Class C amplifier	14
Figure 13) I_{AC} vs. V_{IN} , V_{IN} vs. I_{DC} , and I_{AC} vs. V_{IN} for ideal Class C amplifier	15
Figure 14) Current voltage characteristic of Class B biased CA3096 with 26 Ohm emitter degeneration	15
Figure 15) Class B bias circuit, and sample current output waveforms for various input magnitudes	16
Figure 16) I_{DC} vs. V_{IN} for various bias currents in a CA3096 Class B amplifier	16
Figure 17) V_{IN} vs. I_{DC} for a CA3096 Class C amplifier with different zero input bias currents, and the same conduction angle.....	17
Figure 18) MATLAB simulation demonstrating effect of knee on ratio of DC to AC current in Class C	18
Figure 19) I_{AC} vs. I_{DC} in CA3096 CCA amplifier for various forced Class B curves	19
Figure 20) Circuit used to generate plots demonstrating effect of knee on amplifier linearity	20
Figure 21) Simulation #1 I_{AC} and V_{IN} vs. I_{DC}	21
Figure 22) Simulation #1 I_{AC} vs. V_{IN}	21
Figure 23) Simulation #2 I_{AC} and V_{IN} vs. I_{DC}	22
Figure 24) Simulation #2 I_{AC} vs. V_{IN}	22
Figure 25) Simulation #3 I_{AC} and V_{IN} vs. I_{DC}	23
Figure 26) Simulation #3 I_{AC} vs. V_{IN}	23
Figure 27) Simulation #4 I_{AC} and V_{IN} vs. I_{DC}	24
Figure 28) Simulation #4 I_{AC} vs. V_{IN}	24
Figure 29) Simulation #5 I_{AC} and V_{IN} vs. I_{DC}	25
Figure 30) Simulation #5 I_{AC} vs. V_{IN}	25
Figure 31) I_{AC} and V_{IN} vs. I_{DC} for Simulation #1 with various constant current drains	26
Figure 32) I_{AC} vs. V_{IN} for Simulation #1 with various constant current drains.....	26
Figure 33) Frequency and time domain two tone intermodulation test.....	27
Figure 34) Two tone intermodulation distortion results for 18 kOhm bias resistor and various scaling ratios	28
Figure 35) Two tone intermodulation distortion results for 100 kOhm bias resistor and various scaling ratios	29
Figure 36) Two Tone Intermodulation Data for 18 kOhm bias resistor, $V_{DC,B}/V_{DC,C} = 0.5$, $I_{DC,C}/I_{DC,B} = 1$ and various constant current drain values	30
Figure 37) Two Tone Intermodulation Data for 100 kOhm bias resistor, $V_{DC,B}/V_{DC,C} = 0.9$, $I_{DC,C}/I_{DC,B} = 0.555$ and various constant current drain values	31

Abstract

There is a need for linear, efficient monolithic power amplifiers used for the wireless transmission of signals with amplitude variations. This paper proposes a circuit that actively biases a bipolar transistor so that it operates as a Class C amplifier, with a conduction angle that is constant over a range of output powers. This results in a linear amplifier with a very low two tone intermodulation distortion. By forcing a scaled DC current vs. input magnitude curve from a Class B amplifier on to a Class C amplifier, a constant conduction angle can be maintained in the Class C amplifier. The effect of, and compensation for, a knee in the current voltage characteristics of an amplifier is simulated and analyzed. The tuning of a sweet spot in the two tone intermodulation of an amplifier is addressed. A linear constant conduction angle amplifier with a minimum two tone intermodulation distortion of -53.9 dBc and conduction angle of 137 degrees is presented.

Background

Solid state power amplifiers are inherently inefficient devices, and there seems to be a linearity vs. efficiency tradeoff in the classes of power amplifier available today.

The linearity of a power amplifier is a measure of how constant the gain of the amplifier is over a range of input powers. The efficiency is a measure of much energy the amplifier uses to produce the needed output power.

A Class A amplifier utilizes a transistor that is biased so that it is always conducting. The theoretical efficiency is 25%. Any amplitude input sinusoid can be applied and will be amplified equally, so this is an amplifier that is very linear.

A Class B amplifier utilizes a transistor that is biased at cut off so that it is conducting for 50% of the input waveform. The theoretical efficiency is 78.5%. Any magnitude sinusoid can be applied, and the transistor will theoretically still conduct for 50% of the waveform. Due to deviations from the ideal transistor model, the Class B amplifier is less linear than the Class A amplifier.

A Class C amplifier utilizes a transistor that is biased so that it is conducting for less than 50% of the input waveform. As the conduction percentage of the Class C amplifier approaches 0%, the efficiency of the power amplifier approaches 100%. It has been shown that for an ideal Class C power amplifier, the gain is a function of the percentage of the input waveform that the transistor is conducting. For a Class C amplifier to maintain a conduction percentage that is constant over a range of input powers, the bias level must be changed. Thus a statically biased Class C amplifier would exhibit greater gains for higher input power signals, due to a greater conduction percentage. This leads to a very non linear amplifier, since the gain greatly changes when the input power changes.

Some digital modulation schemes, like QPSK, have a constant output power. A statically biased Class C power amplifier is suitable to amplify signals modulated this way. Since the digital data in a QPSK modulated signal is presented only as phase shifts, and not as amplitude variations, the Class C biased transistor will always be conducting for the same percentage of the input waveform, thus the gain of the amplifier is constant.

Higher data transmission rates are available with modulation schemes that employ phase shifts and amplitude variations. Schemes like QAM64, and multi carrier communication schemes, like CDMA, have high peak to average power ratios. If these signals are amplified with a statically biased Class C power amplifier, the times that the signal has a large magnitude would experience greater gain. This nonlinearity results in undesired out of band signals. This paper deals with increasing the linearity of a Class C amplifier by actively controlling the bias, but maintaining the efficiency.

Constant Conduction Angle Theory:

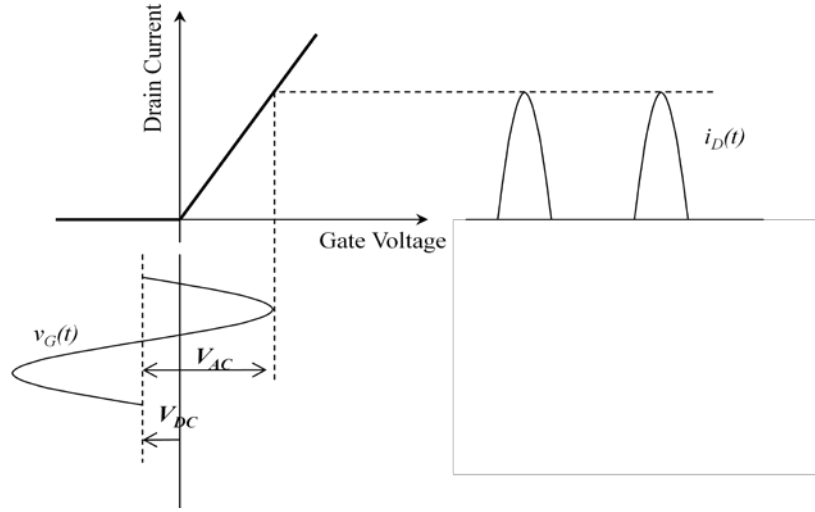


Figure 1) Voltage and current waveforms for the ideal turn on approximation

Consider an ideal transistor amplifier, as shown in figure 1, where the current voltage characteristics are given by:

$$I_d = \begin{cases} 0 & V_i < 0 \\ g_m V_i & V_i > 0 \end{cases} \quad (1)$$

Consider some input sinusoid, also shown in figure 1:

$$V_G(t) = V_{AC} \cos(\omega t) - V_{DC} \quad (2)$$

The portion of the input waveform that the transistor is conducting is defined as the conduction angle:

$$\theta = 2\pi \frac{t_{ON}}{T} = 2 \arccos \left(\frac{V_{DC}}{V_{AC}} \right) \quad (3)$$

Where :

$$t_{ON} = \theta_2 - \theta_1 = \arccos \left(\frac{V_{DC}}{V_{AC}} \right) + \arccos \left(\frac{V_{DC}}{V_{AC}} \right) \quad (4)$$

It has been shown, by taking the Fourier transform of the collector current, that the DC output current is:

$$I_{DC} = \frac{g_m}{\pi} \left(\sin \left(\frac{\theta}{2} \right) - \frac{\theta}{2} \cos \left(\frac{\theta}{2} \right) \right) V_{AC} \quad (5)$$

And the magnitude of the fundamental harmonic output current is:

$$I_{AC} = \frac{g_m}{\pi} \left(\frac{\theta}{2} - \frac{1}{2} \sin \theta \right) V_{AC} \quad (6)$$

Class B Operation:

Class B operation can be considered a special case of the above, where $V_{DC} = 0$ V and $\theta = 180$ degrees.

From (5), the ratio of DC current to AC input is given as:

$$\frac{I_{DC,B}}{V_{AC,B}} = \frac{g_m}{\pi} \quad (7)$$

From (6), the fundamental AC current is given as:

$$I_{AC,B} = \frac{g_m}{\pi} \left(\frac{\theta}{2} - \frac{1}{2} \sin \theta \right) V_{AC} = \frac{g_m}{2} V_{AC,B} \quad (8)$$

Class C Operation:

Class C operation is defined as any case where the conduction angle is less than 180 degrees, so, from (5) the DC current to AC input ratio is given as:

$$\frac{I_{DC,C}}{V_{AC,C}} = \frac{g_m}{\pi} \left(\sin \left(\frac{\theta}{2} \right) - \frac{\theta}{2} \cos \left(\frac{\theta}{2} \right) \right) \quad (9)$$

and the AC current, from (6), is given as:

$$I_{AC,C} = \frac{g_m}{\pi} \left(\frac{\theta}{2} - \frac{1}{2} \sin \theta \right) V_{AC,C} \quad (10)$$

Maintaining a Constant Conduction Angle

From (10), it is seen that for a Class C amplifier, I_{AC} is a linear function of V_{AC} if the conduction angle, θ , is kept constant. For a constant conduction angle to be maintained for input signals of different magnitudes, the DC bias voltage for the class C amplifier must be adjusted by (3). If the input voltage is large, the bias voltage must be reduced so that the transistor is only conducting for a portion of the input waveform.

To generate a constant V_{DC} bias to V_{AC} input ratio, which is required for a constant conduction angle, a scheme of comparing the DC currents in a dummy Class B amplifier and a dummy Class C amplifier which are driven with the same input signal of different magnitudes, is developed. This bias voltage can then be used to bias a large output transistor such that it always conducts with the same conduction angle and the fundamental output current is linear with the input magnitude.

The following equation determines the ratio of DC current in the class B dummy to the DC current in the class C dummy, and the ratio of input magnitudes to the two dummy transistors, needed to maintain a constant conduction angle. If this product of ratios is kept constant, a DC bias voltage will be generated that maintains a constant conduction angle. From (7) and (9):

$$\frac{I_{DC,C}}{V_{AC,C}} \frac{V_{AC,B}}{I_{DC,B}} = \left(\sin \left(\frac{\theta}{2} \right) - \frac{\theta}{2} \cos \left(\frac{\theta}{2} \right) \right) \quad (11)$$

Proposed Circuit

The circuit proposed in this paper is shown in the figure below:

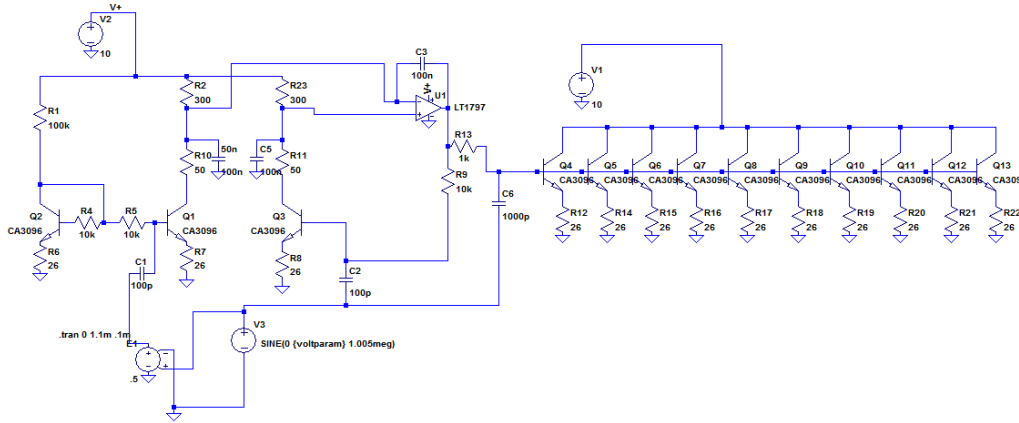


Figure 2) Proposed constant conduction angle bias generation circuit

Q1 operates as a Class B amplifier, with the bias voltage generated by Q2. The bias current is determined by the collector resistance of Q2, R1. Q2 is driven with a voltage controlled voltage source, which is set to multiply the main input signal by some constant that is normally less than unity.

Q3 is operated as a Class C amplifier. The collector resistances and capacitances of Q1 and Q2 are used to generate a DC voltage that is representative of the DC current flowing through each amplifier. These DC voltages are compared by op amp U1. Op amp U1 then sets the DC bias voltage for the Class C amp so that the DC currents in each amplifier are the same.

By changing the ratio of R2 and R3, the ratio of the DC currents that is apparent to the op amp is set. By changing the constant of the voltage controlled voltage source, the ratio of input voltage to the two amplifiers can be set. From equation (11), these parameters set the conduction angle.

Q4 through Q13 are all in parallel, and form the output transistor. This large output transistor is driven with the same input and DC bias as the Class C amplifier, so it will be biased in Class C and at the same conduction angle as Q3. Matched transistor all operating at the same temperature are needed to ensure that the biasing circuitry produces the correct bias voltage. These are the conditions that would be found in a monolithic integrated circuit.

Q1 is said to be the dummy Class B and Q3 is said to be the dummy Class C. The sole purpose of these transistors is to generate a DC voltage that will be used to bias the large output transistor. Q1 and Q3 are much smaller than the large output transistor so that they do not consume much power, but still generate the needed DC bias voltage.

Ultimately, the output transistor will drive a resonant matching network. This matching network will remove harmonics of the signal and reconstruct the input signal.

The next two sections demonstrate variations of the biasing circuitry that can be used to determine the conduction angle.

Equal Input Voltages, Unequal DC Currents

Assuming the piecewise current voltage characteristics as above, but with a turn on voltage, V_{ON} : If a Class B amplifier and a Class C amplifier are both operated with the same input signal, and the bias voltage to the Class C is chosen so that the DC current in the class C amplifier is a fraction of the DC current in the Class B, the conduction angle is determined by:

$$\frac{I_{DC,C}}{I_{DC,B}} = \left(\sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2} \cos\left(\frac{\theta}{2}\right) \right) \quad (12)$$

The following circuit demonstrates how this could be implemented:

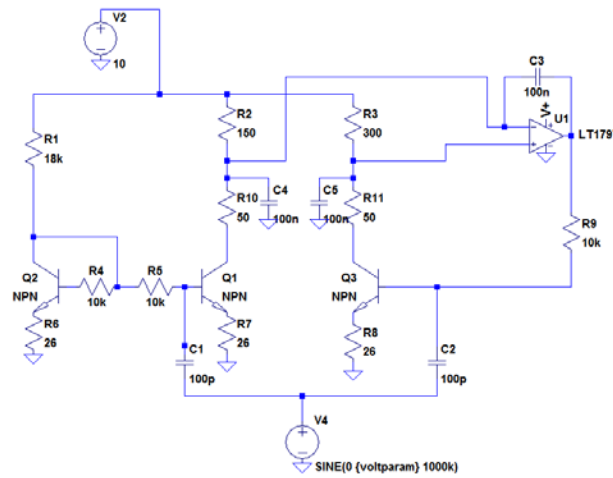


Figure 3) Equal input voltage, unequal DC current scaling implementation

The DC current ratio, and thus the conduction angle, is determined by the collector resistances $R2$ and $R3$:

$$\frac{I_{DC,C}}{I_{DC,B}} = \left(\sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2} \cos\left(\frac{\theta}{2}\right) \right) = \frac{R2}{R3} \quad (13)$$

The bias points for both amplifiers are found to be:

$$\begin{aligned} V_{DC,B} &= V_{ON} \\ V_{DC,C} &= V_{ON} - V_{AC} \cos(\theta) \end{aligned} \quad (14)$$

Equal DC Currents, Unequal Input Voltages

Assuming the same piecewise model used in the previous section, if the DC currents in the Class B and Class C are held equal, but the class B is given a smaller input signal than the class C, then the conduction angle is determined by:

$$\frac{V_{AC,B}}{V_{AC,C}} = \left(\sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2} \cos\left(\frac{\theta}{2}\right) \right) \quad (15)$$

The following circuit demonstrates how this could be implemented:

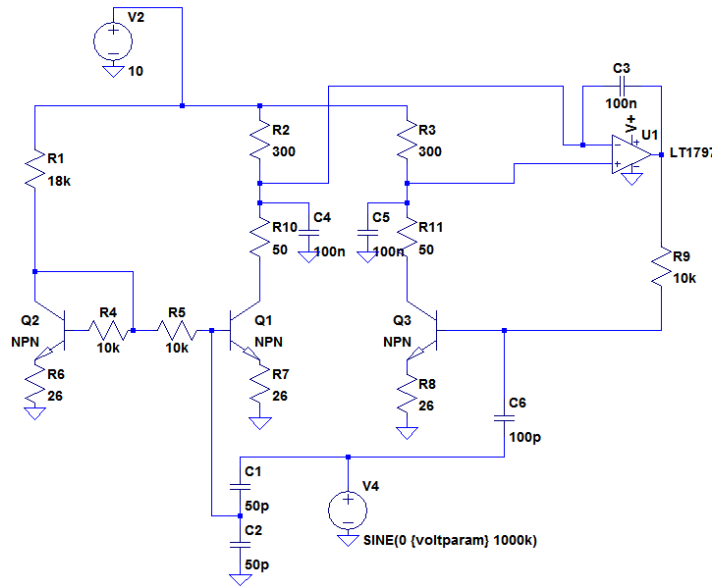


Figure 4) Equal DC current, unequal input voltage scaling implementation

The input voltage ratio, and thus the conduction angle, is determined by C1 and C2:

$$\frac{V_{AC,B}}{V_{AC,C}} = \left(\sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2} \cos\left(\frac{\theta}{2}\right) \right) = \frac{C1}{C1 + C2} \quad (16)$$

The bias points are found to be:

$$\begin{aligned} V_{DC,B} &= V_{ON} \\ V_{DC,C} &= V_{ON} - V_{AC,C} \cos(\theta) \end{aligned} \quad (17)$$

While both this approach and the previous approach can be used to generate the same bias point, and thus the same conduction angle for the class C, this approach has the added benefit of giving a smaller input voltage to the class B, thus larger inputs can be used without applying too large a voltage to the class B input. This is especially useful for small conduction angles.

The Hybrid Approach

The hybrid approach employs a combination of the previous two approaches. By making the product of the current and voltage ratios to be a constant that is less than one, a constant conduction angle can be set. The following table demonstrates some sample resistance and capacitance ratios, and the corresponding conduction angle:

$\theta = 137^\circ$, Product = 0.5					
$\frac{V_{AC,B}}{V_{AC,C}} = \frac{R2}{R3}$	0.5	0.6	0.707	0.866	1
$\frac{I_{DC,C}}{I_{DC,B}} = \frac{C1}{C1 + C2}$	1	0.833	0.707	0.577	0.5

$\theta = 127^\circ$, Product = 0.4					
$\frac{V_{AC,B}}{V_{AC,C}} = \frac{R2}{R3}$	0.4	0.5	0.632	0.8	1
$\frac{I_{DC,C}}{I_{DC,B}} = \frac{C1}{C1 + C2}$	1	0.8	0.632	0.5	0.4

$\theta = 114^\circ$, Product = 0.3					
$\frac{V_{AC,B}}{V_{AC,C}} = \frac{R2}{R3}$	0.3	0.4	0.548	0.8	1
$\frac{I_{DC,C}}{I_{DC,B}} = \frac{C1}{C1 + C2}$	1	0.75	0.548	0.375	0.3

$\theta = 99^\circ$, Product = 0.2					
$\frac{V_{AC,B}}{V_{AC,C}} = \frac{R2}{R3}$	0.2	0.3	0.447	0.7	1
$\frac{I_{DC,C}}{I_{DC,B}} = \frac{C1}{C1 + C2}$	1	0.667	0.447	0.286	0.2

Additionally, ratios can be set that so they are greater than unity. The only requirement for maintaining a constant conduction angle is that the product of ratios is a constant that is less than unity.

Sample Waveform Simulations

To demonstrate the constant conduction angle concept, and to demonstrate the validity of the proposed circuit, sample plots are given. These are generated by SPICE simulations of a CA3096 transistor. Effects of using real transistor amplifier as opposed to ideal amplifiers are addressed later.

The following simulations are obtained with $R2/R3 = 0.5$, $V_r = 0.5$. This is a hybrid approach that in the ideal case will obtain a constant conduction angle of 107 degrees.

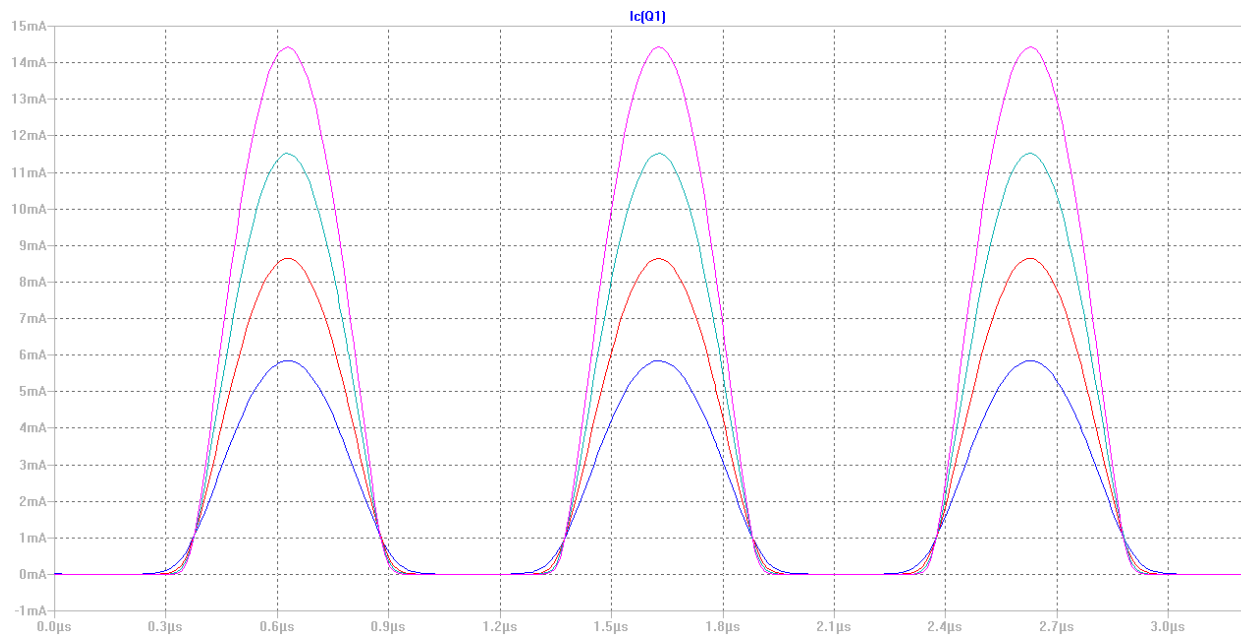


Figure 5) Current in collector of Class B biased transistor, Q1

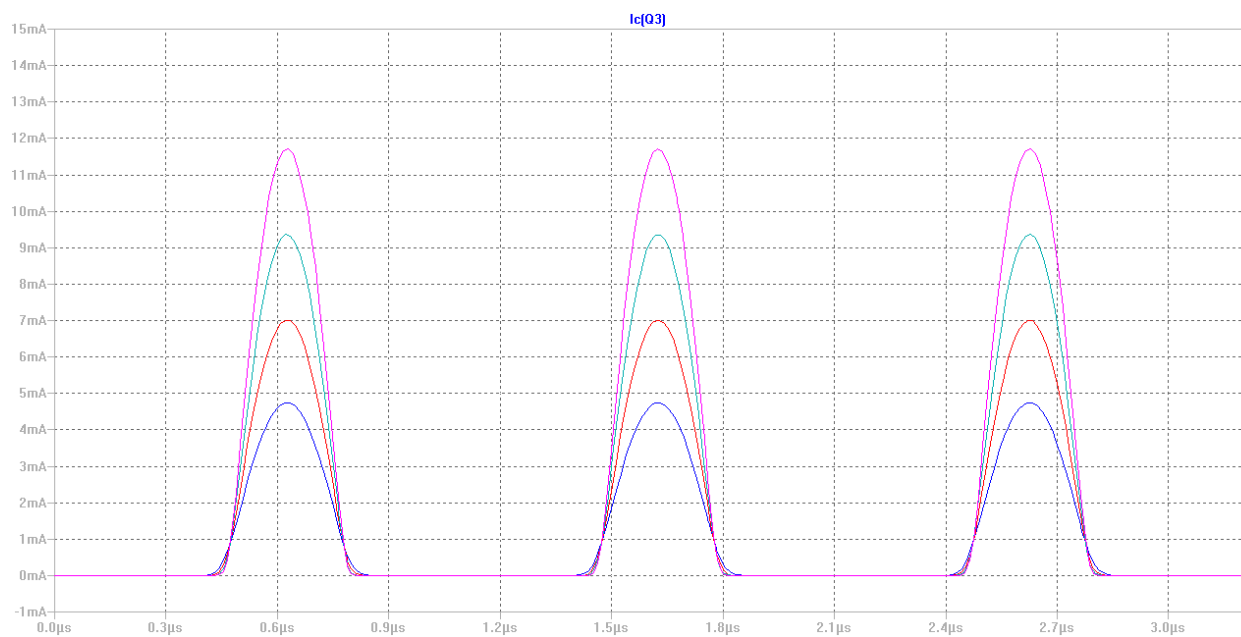


Figure 6) Current in collector of Constant Conduction Angle biased transistor, Q3

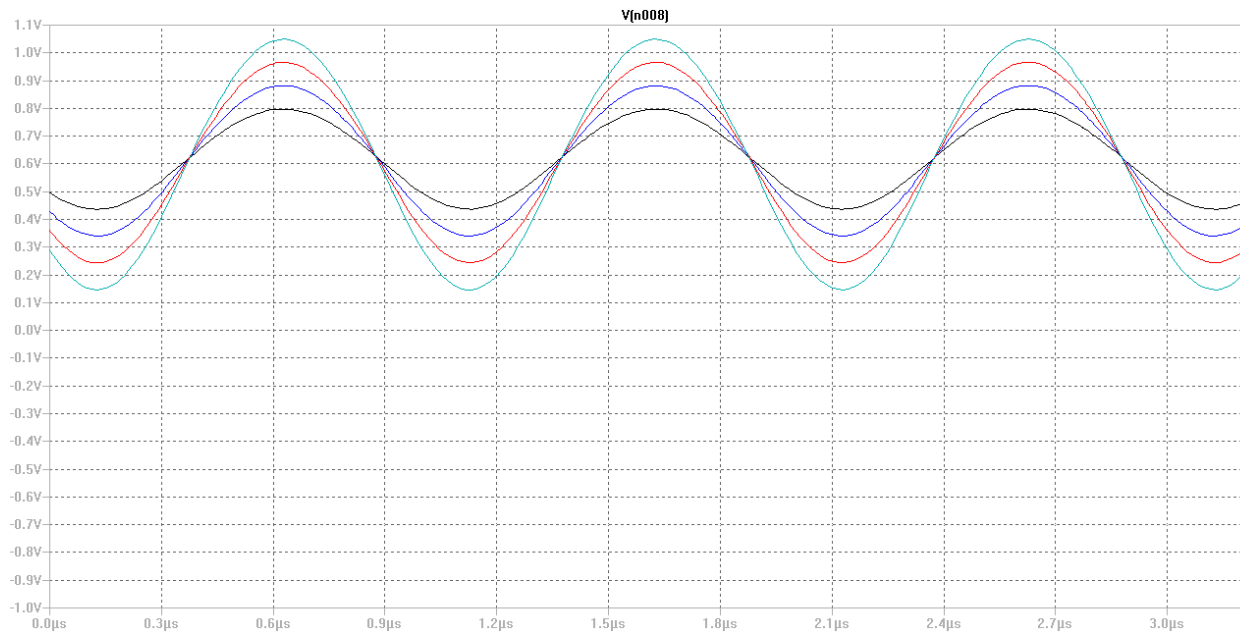


Figure 7) Input voltage to Class B biased transistor, Q1

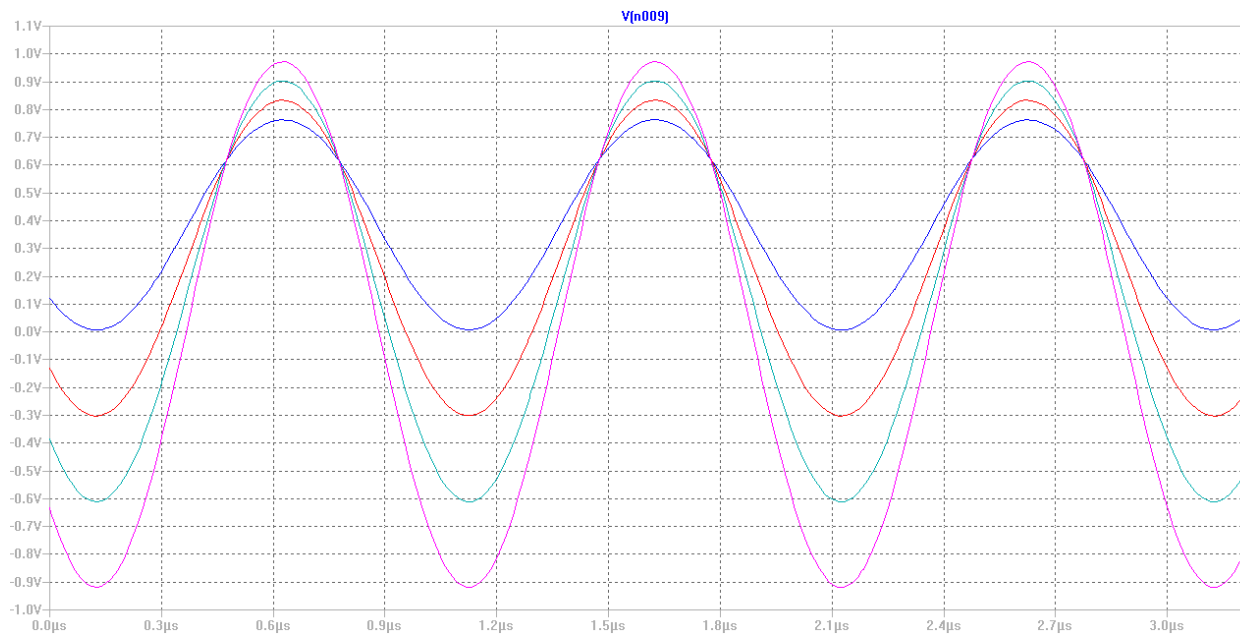


Figure 8) Input voltage to Constant Conduction Angle biased transistor, Q3

Figures 5 and 6 demonstrate the reduction in conduction angle achieved. Figures 7 and 8 demonstrate the DC bias shift that is applied to each input sinusoid of different magnitude that is needed to force a constant conduction angle.

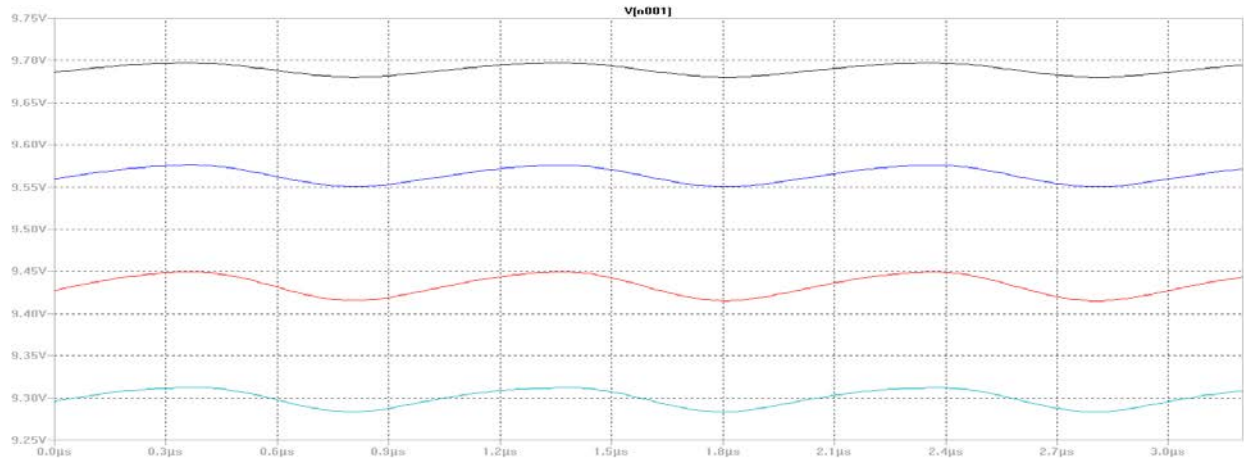


Figure 9) DC Voltage at inverting op amp input

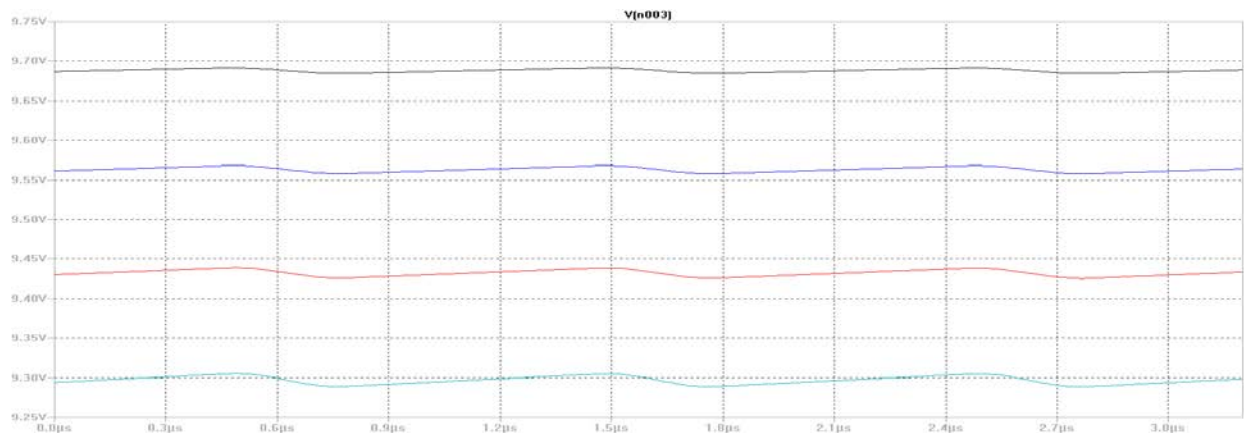


Figure 10) DC voltage at non inverting op amp input

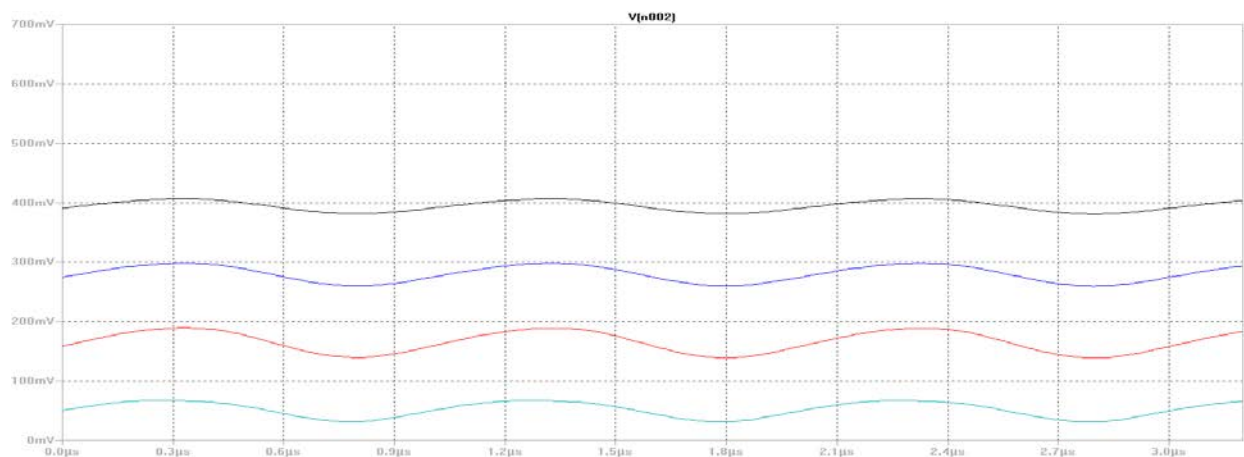


Figure 11) Op amp output voltage, bias level for Class C biased transistor, Q3

Figures 9 and 10 demonstrate the DC inputs to the op amp terminals, from the Class B and Class C amplifier respectively. Figure 11 demonstrates the bias voltage that is produced and given to the Class C amplifier.

Forcing a Scaled Class B Curve to Bias a Class C Amplifier

In order to apply concepts from the idealized amplifier model to real transistors with non ideal current voltage characteristics, consider the following ideal plots in figure 7, from equations (7) and (9):

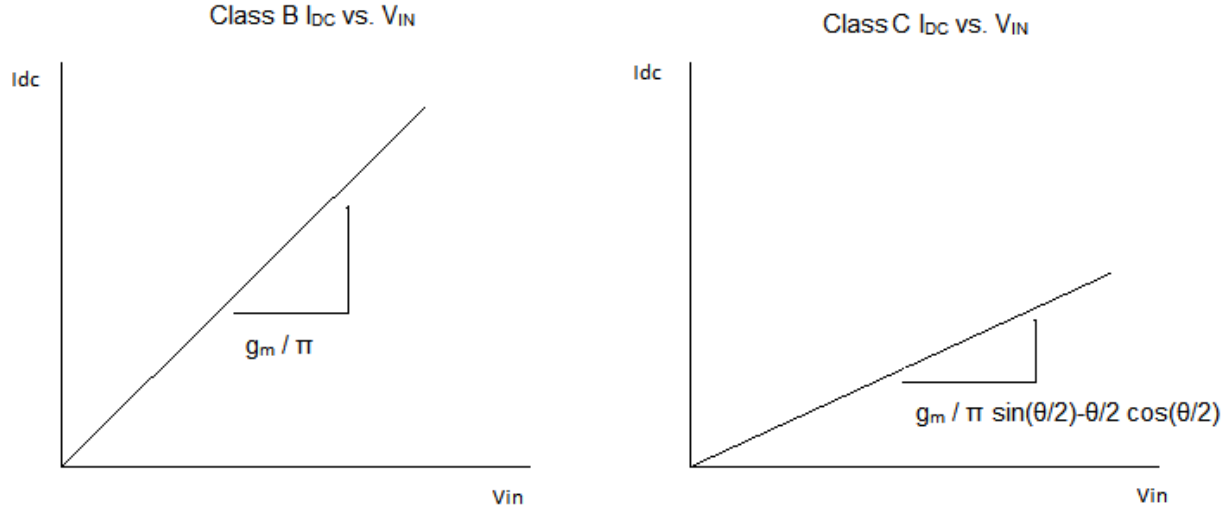


Figure 12) I_{DC} vs. V_{IN} for ideal Class B amplifier and I_{DC} vs. V_{IN} for ideal Class C amplifier

In order to set the DC bias for the Class C transistor, a I_{DC} vs. V_{IN} curve must be generated. This is done with a Class B amplifier. This curve is then scaled so that it matches the desired Class C curve. Finally, by forcing this scaled curve onto a Class C amplifier, the class C amplifier is made to conduct at a constant conduction angle. The class B curve can be scaled in any of the following ways:

- Divide I_{DC} by a constant that determines the conduction angle
- Multiply V_{IN} by a constant that determines the conduction angle
- Hybrid Approach, multiply V_{IN} and divide I_{DC} by constants whose product is a constant that determines the conduction angle

By forcing a scaled version of the Class B I_{DC} vs. V_{IN} curve onto an amplifier, the bias voltage will be automatically set so that the amplifier will operate as a Class C amplifier with a conduction angle that is constant and independent of the input voltage.

Extending the ideal case, by assuming that conduction angle is held constant, from (equation) it is seen that

$$\begin{aligned} I_{AC,C} &= K_I I_{DC} \\ V_{IN} &= K_V I_{DC} \end{aligned} \tag{18}$$

Combining:

$$I_{AC,C} = \frac{K_I}{K_V} V_{IN} \tag{19}$$

From this analysis and the plots in figure 13, it can be seen that if the I_{AC} vs. I_{DC} and V_{IN} vs. I_{DC} characteristics of a Class C amplifier are known, then the I_{AC} vs. V_{IN} characteristic can be determined. This will be useful when analyzing the effect of a non ideal transistor on the overall linearity of the amplifier.

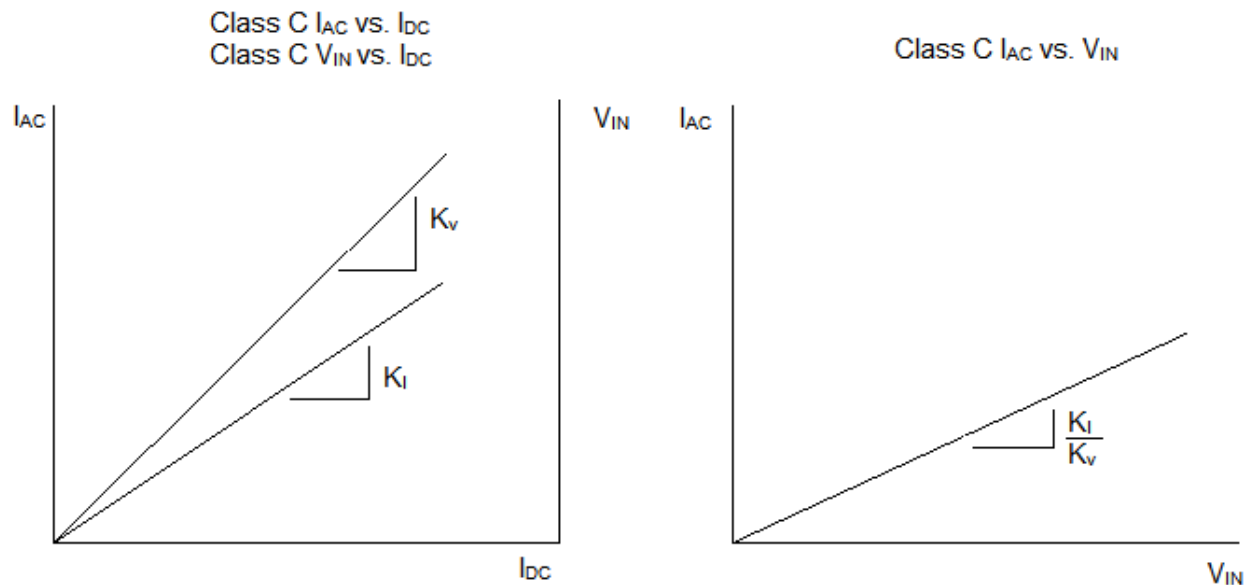


Figure 13) I_{AC} vs. V_{IN} , V_{IN} vs. I_{DC} , and I_{AC} vs. V_{IN} for ideal Class C amplifier

As seen in figure 13, the slopes of the Class C curves combine to produce the overall circuit linearity plot.

Implementing with Actual Transistors

The main problem that arises when attempting to implement a constant conduction angle scheme comes from the deviation of a transistor's current voltage characteristic from the piecewise, sudden turn on approximation used in the derivation of equations above.

For the purposes of this paper, SPICE simulations will be done with a spice model for the CA3096 transistor.

A DC sweep of the amplifier used is shown below to demonstrate the knee in the current voltage characteristic.

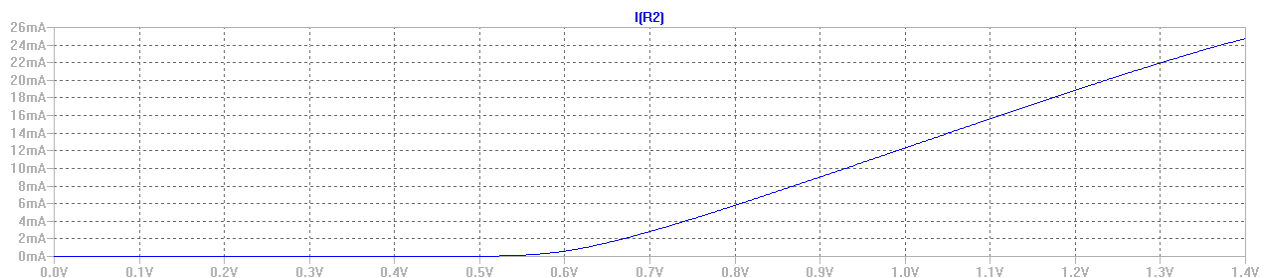


Figure 14) Current voltage characteristic of Class B biased CA3096 with 26 Ohm emitter degeneration.

The problem that needs to be dealt with is how the “knee” in the current voltage characteristic affects the DC current vs. DC Input Voltage of a Class B amplifier, and how the knee affects the AC current vs. DC current in a Class C amplifier.

The analysis above demonstrates that if the I_{AC} vs. I_{DC} and V_{IN} vs. I_{DC} characteristics of a Class C amplifier are known, then the I_{AC} vs. V_{IN} characteristic can be found to analyze the linearity of the amplifier. The plots above apply only to the ideal case, and deviations from this are addressed later.

Class B I_{DC} vs. V_{IN} Generation

When the amplifier is biased at Class B, as shown in the circuit below, the DC current deviates from the ideal as follows:

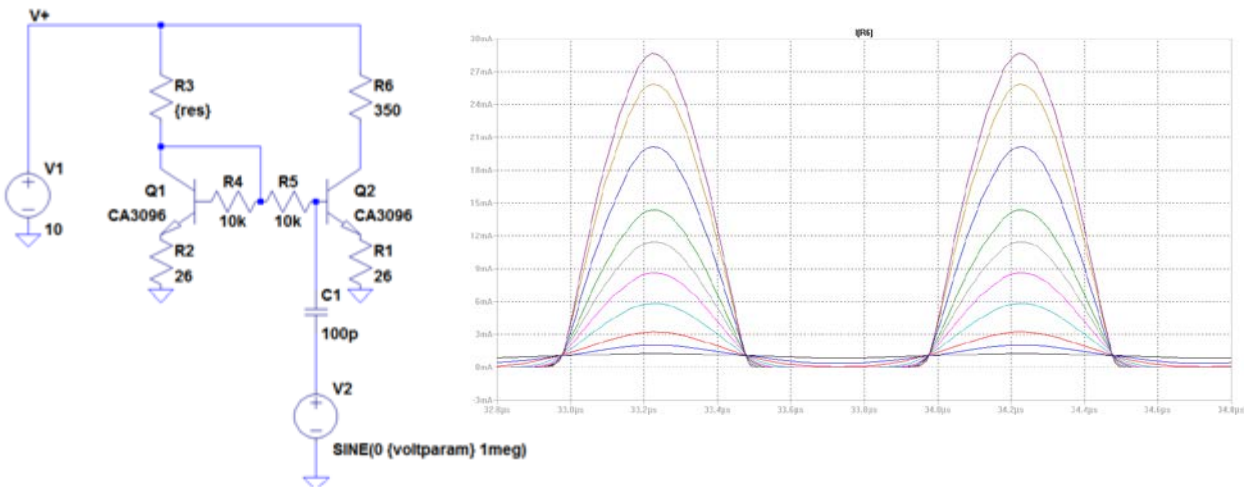


Figure 15) Class B bias circuit, and sample current output waveforms for various input magnitudes

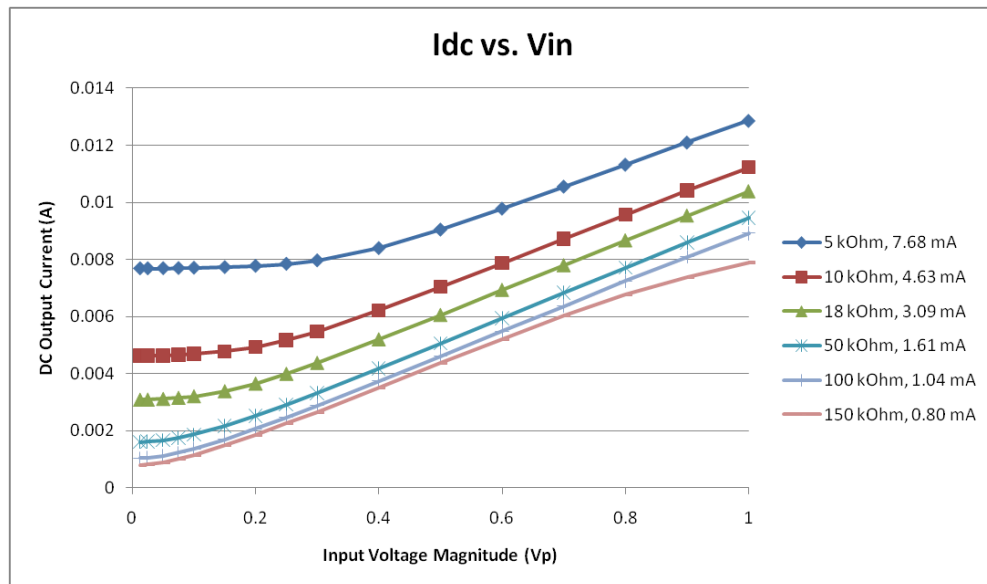


Figure 16) I_{DC} vs. V_{IN} for various bias currents in a CA3096 Class B amplifier

The knee in the current voltage characteristic has the effect of forcing more DC current at low input levels when compared to the ideal case. This is because the transistor must be biased at a point where there is DC current flow for zero AC input. It is seen that by changing the collector resistor of the bias transistor, the curve can be made to more closely resemble the ideal case.

Scaled Class B V_{IN} vs. I_{DC}

The class B I_{DC} vs. V_{IN} curve will be scaled and then forced onto the Class C amplifier in order to maintain a constant conduction angle. For later analysis purposes, it is helpful to display the curve as V_{IN} vs. I_{DC}

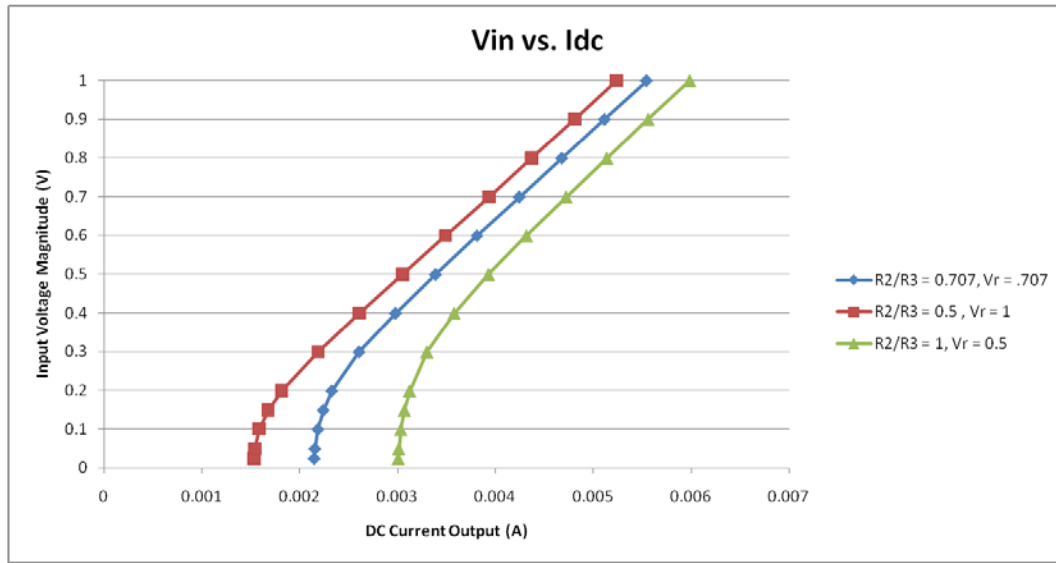


Figure 17) V_{IN} vs. I_{DC} for a CA3096 Class C amplifier with different zero input bias currents, and the same conduction angle

It is shown that scaling the Class B amplifier will result in different I_{DC} vs. V_{IN} curves being forced on to the Class C. By changing the resistors $R2$ and $R3$, the $I_{DC,C} / I_{DC,B}$ current ratio can effectively be reduced. This results in a curve with a lower zero input DC current, and a linear region that is closer to passing through the origin if extended.

Increasing the $V_{AC,B} / V_{AC,C}$ ratio is needed if the $I_{DC,C} / I_{DC,B}$ is reduced. This ensures the same conduction angle with different ratios. There is a severe repercussion of increasing the voltage ratio. The larger that this ratio is, the closer the Class B is to a region where the output suffers gain compression. By keeping the voltage ratio low, gain compression in the Class B can be avoided. It would be very beneficial if this voltage ratio could be kept low, since a Class C biased amplifier naturally needs a larger input than a Class B does, but it was seen that increasing the voltage ratio was often needed to maintain linearity.

Constant Conduction Angle Biased Class C I_{AC} vs. I_{DC}

Since the Class B I_{DC} vs. V_{IN} curve has a bend in it that can only be scaled, and cannot be eliminated, then in order to obtain a linear amplifier, the Class C I_{AC} vs. I_{DC} curve must also have a bend that cancels out the bend in the Class B curve. This can then lead to a linear I_{AC} vs. V_{IN} curve, which is the ultimate goal.

To justify the bend in the I_{AC} vs. I_{DC} curve, consider the following MATLAB simulation:

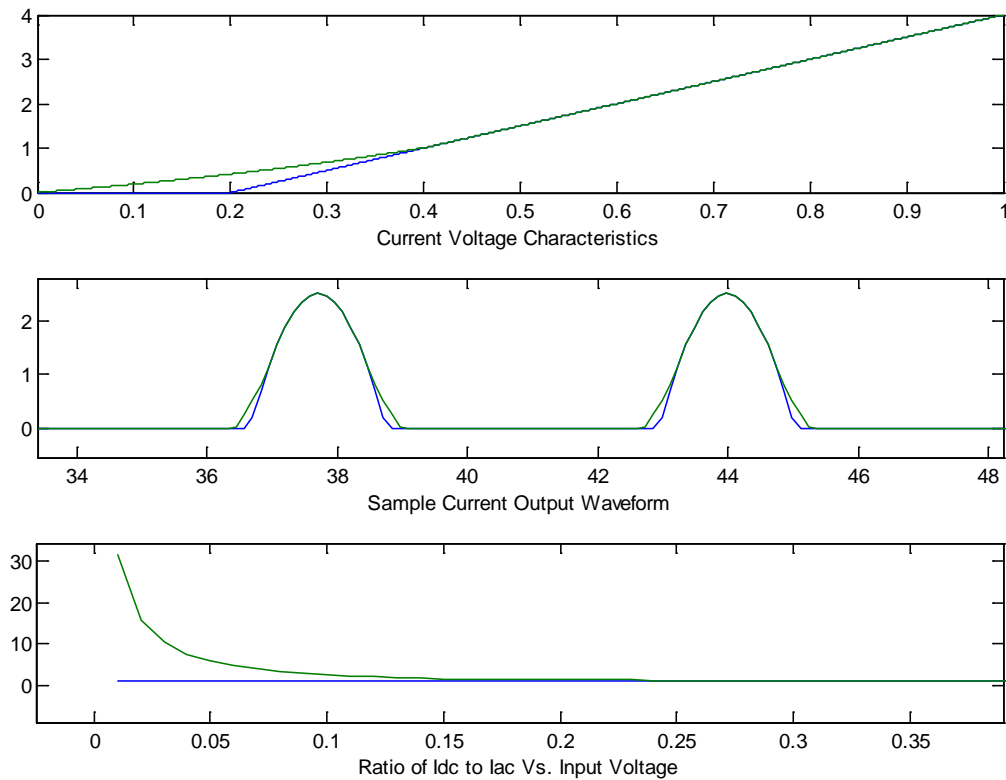


Figure 18) MATLAB simulation demonstrating effect of knee on ratio of DC to AC current in Class C

The plots of Figure 18 were generated by a MATLAB program that creates the current output waveform for two transistor characteristic curves, and a bias voltage results in the same conduction angle, independent of input voltage. The top plot shows the two transistor characteristics that were simulated. The middle plot is a sample output waveform, and the bottom plot is the ratio of DC to fundamental AC current. For the sudden turn on characteristic, the ratio of DC to AC is always a constant, as predicted in the theory section. For the characteristic that has a knee around the turn on voltage, the DC to AC ratio is very high for small inputs, but then approaches a constant as the input voltage is increased.

This result makes sense, as the input voltage increases, the effect of the knee becomes reduced. At lower input voltages, the conduction angle is greater. This is necessary to obtain the correct AC current. As the input voltage is increased, the knee has a smaller effect, and the actual conduction angle closely follows the set conduction angle.

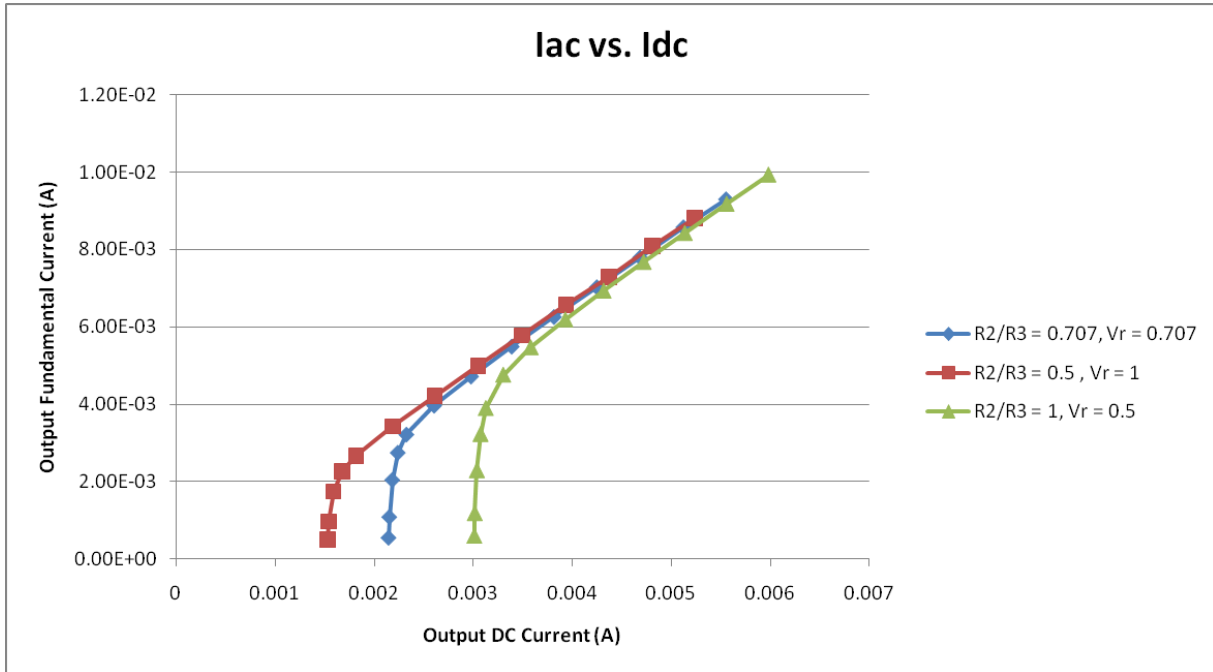


Figure 19) I_{AC} vs. I_{DC} in CA3096 CCA amplifier for various forced Class B curves

The plot of Figure 19 is obtained by forcing the scaled Class B curves from Figure 17 onto a Class C amplifier, and measuring the fundamental output current vs. input current. The voltage and current ratios are set to have a product of 0.5, and as the output current gets large enough that the effect of the knee is neglected, all three cases exhibit the same slope, this suggests that the constant conduction angle mechanism is functioning properly.

The steep portion of each curve corresponds to the Class C amplifier obtaining much more AC current for a given amount of DC current increase. This is the region where the Class C amplifier is overcoming the knee in the current voltage characteristic. The amplifier has a very poor AC current to DC current ratio for low input ratios because of the knee, and this steep portion is the amplifier overcoming that very poor ratio.

This steep portion is shorter for amplifiers where the voltage ratio is set to a higher value. This is due to a different scaled I_{DC} vs. V_{IN} from the Class B amplifier for each case.

Simulations Demonstrating Effect of Current and Voltage Ratios on Linearity

To demonstrate the effect of the current ratios and voltage ratios on the overall circuit linearity, several cases are simulated and analyzed with the following circuit:

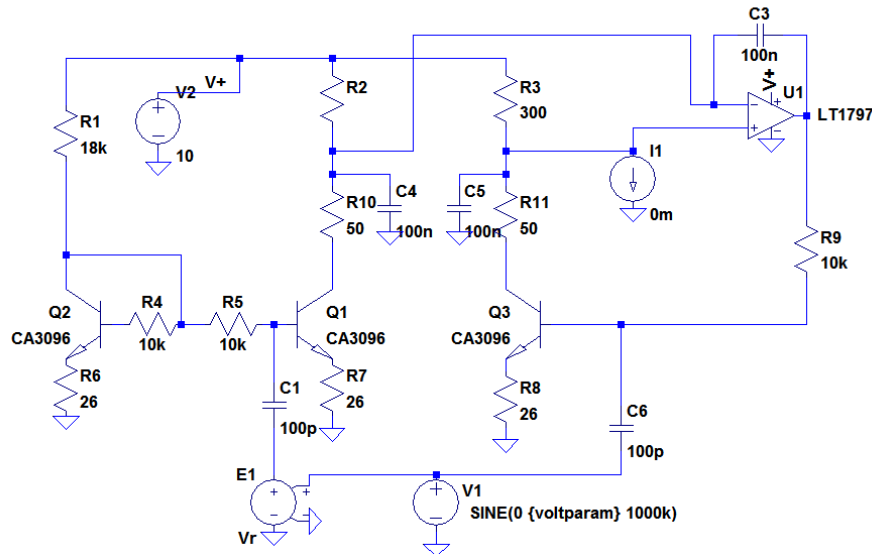


Figure 20) Circuit used to generate plots demonstrating effect of knee on amplifier linearity

The simulation is run for 600 μ s to reach steady state, then data is collected for 400 μ s. The input voltage is swept, the DC current forced on the Class C amplifier is measured, and the AC current in the Class C is measured. The first simulations use an 18k bias resistor on the collector of Q2, which demonstrates the effects of the knee by having a pronounced bend in the I_{DC} vs. V_{IN} characteristic. Later simulations use a 100k bias resistor in an attempt to generate the most linear I_{AC} vs. V_{IN} characteristic.

All simulation use $R3 = 300$ Ohms, and V_r is the value given to the voltage controlled voltage source that drives the Class B amplifier. If the current ratio is less than unity, $R2$ will be less than 300 Ohms.

For each of the following five simulations, the bias resistor, $R1$, the current ratio, and the voltage ratio, will all be given. Comparisons are then made between the simulations, and then effect of the plots on the overall linearity is addressed. First, sample waveforms are given, and then plots that are used to evaluate system linearity:

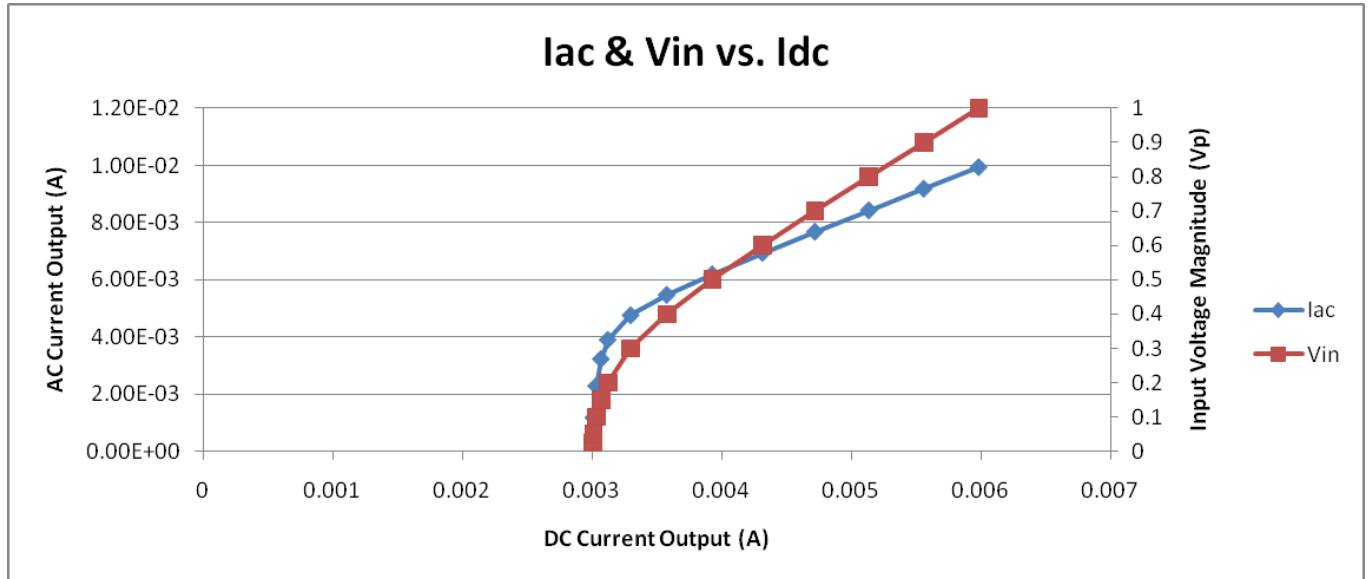
Simulation #1 : 18 kOhm bias, $V_r = 0.5$, $R_2/R_3 = 1$


Figure 21) Simulation #1 I_{AC} and V_{IN} vs. I_{DC}

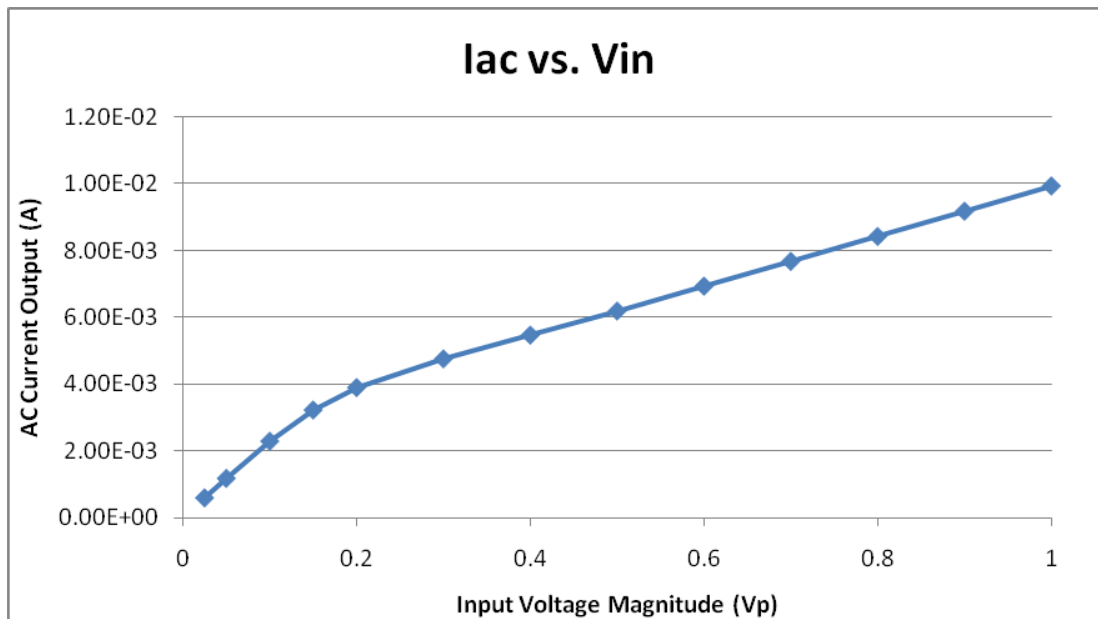
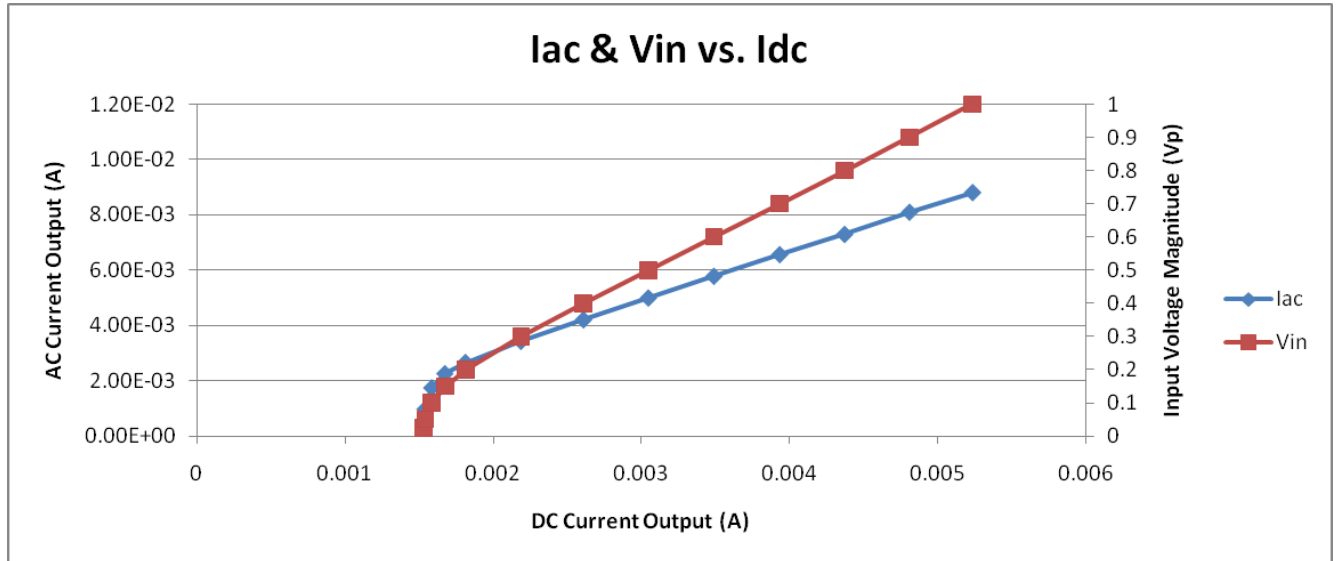
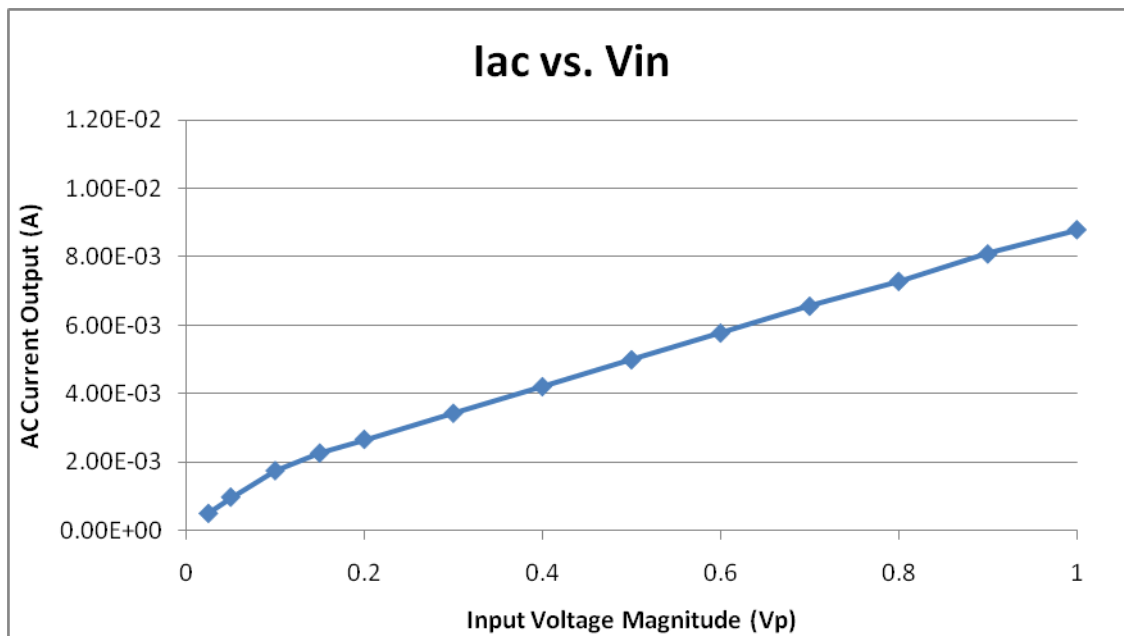


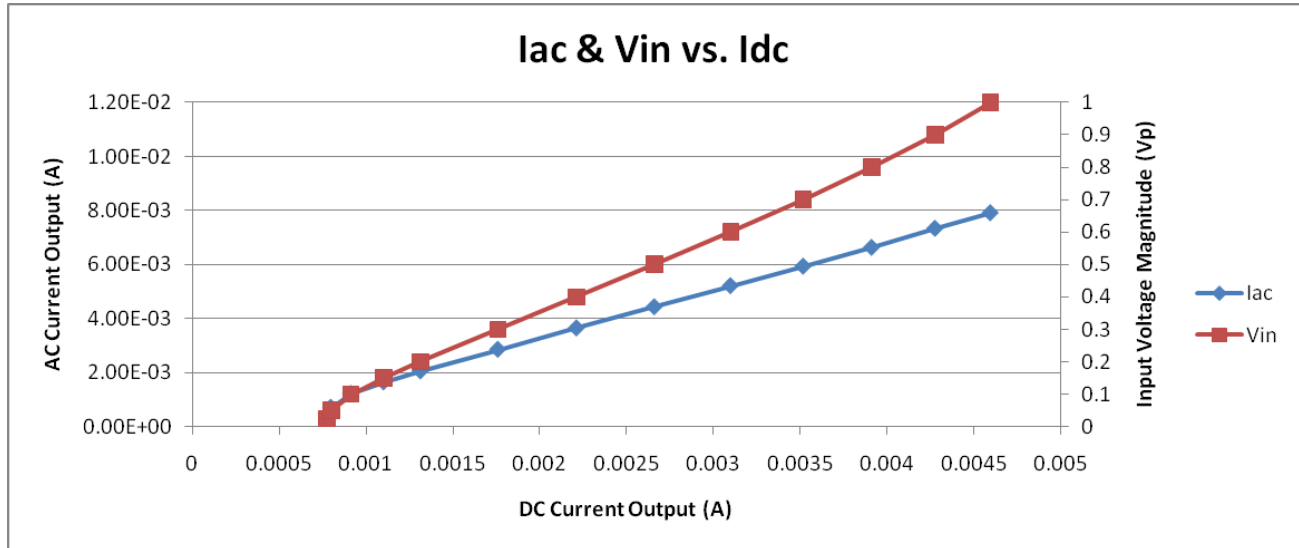
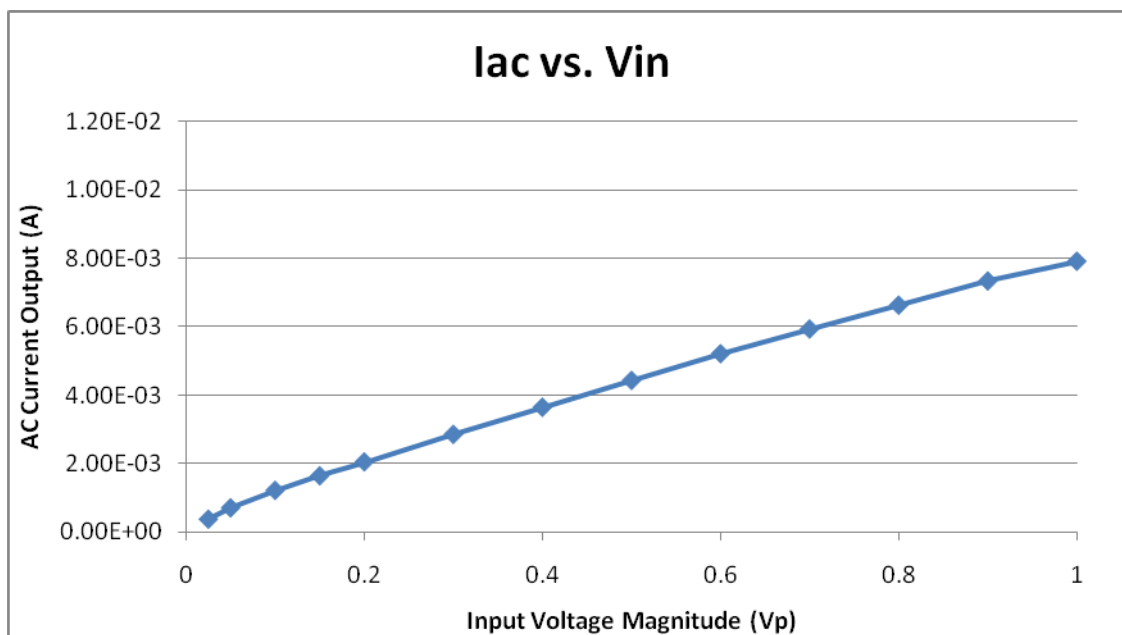
Figure 22) Simulation #1 I_{AC} vs. V_{IN}

The slopes of the I_{AC} and V_{IN} vs. I_{DC} in Figure 21 divide to produce the I_{AC} vs. V_{IN} characteristic seen in Figure 22. Since the I_{AC} curve has a large bend that does not match then bend in the V_{IN} curve, there is a large bend in the lower curve, and the main linear section of the curve does not pass through the origin if extended. This is a result of the scaled Class B curve not matching well to the I_{AC} vs. I_{DC} curve. This amplifier is not very linear.

The following simulations will demonstrate ways to increase the linearity of the amplifier.

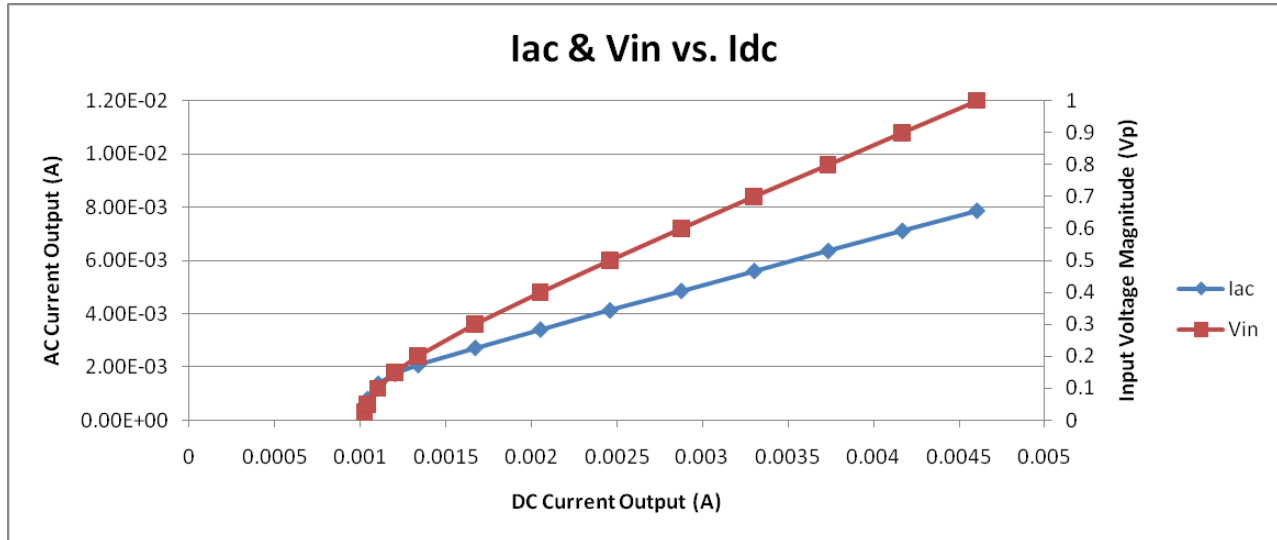
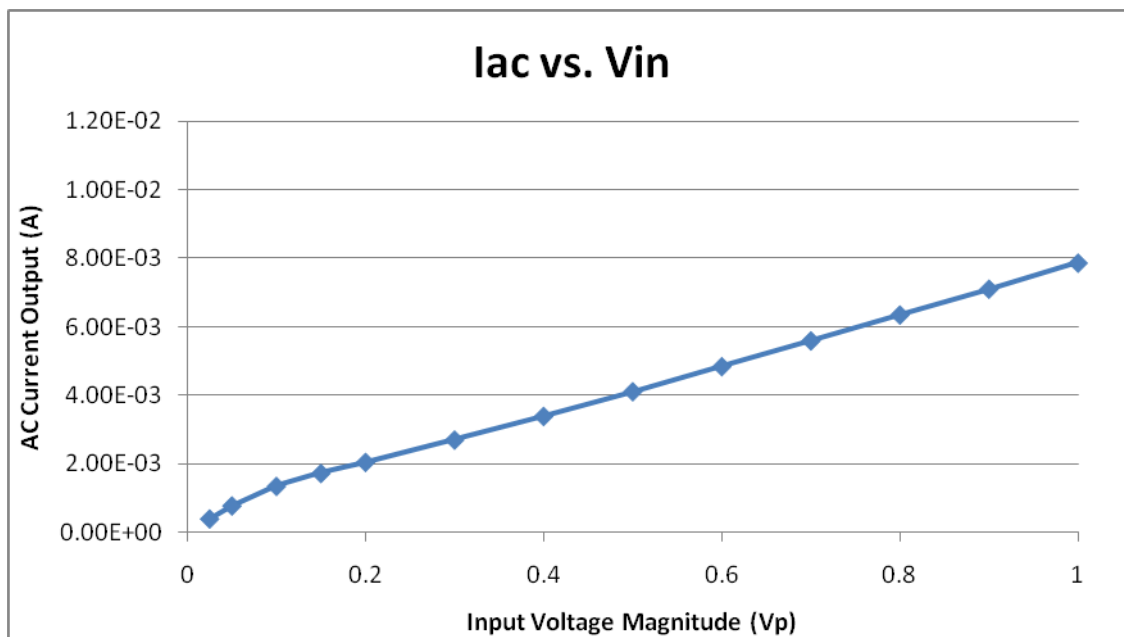
Simulation #2 : 18 kOhm bias, $V_r = 1$, $R_2/R_3 = 0.5$

 Figure 23) Simulation #2 I_{AC} and V_{IN} vs. I_{DC}

 Figure 24) Simulation #2 I_{AC} vs. V_{IN}

By scaling the Class B curve differently, namely applying the full input voltage to the Class B and then dividing the output current by a factor of two, the overall amplifier can be made more linear than Simulation #1. The DC bias current is reduced, but the input voltage to the Class B is doubled. The result is that the bends in the I_{AC} and V_{IN} curve match more closely than Simulation #1, leading to a more linear I_{AC} vs. V_{IN} , as seen in Figure 24.

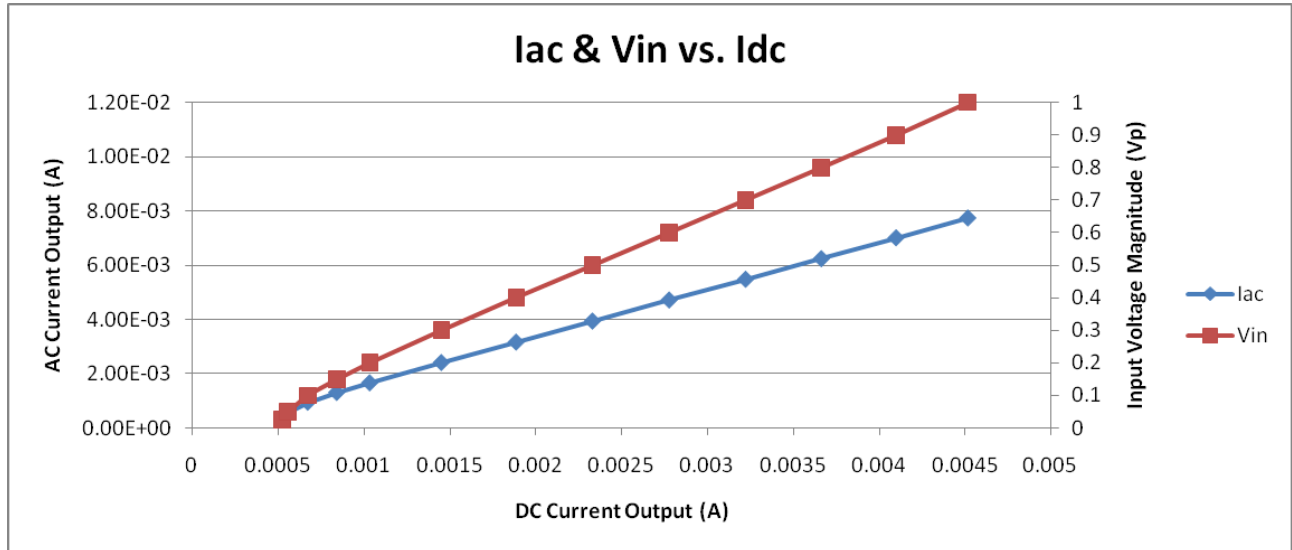
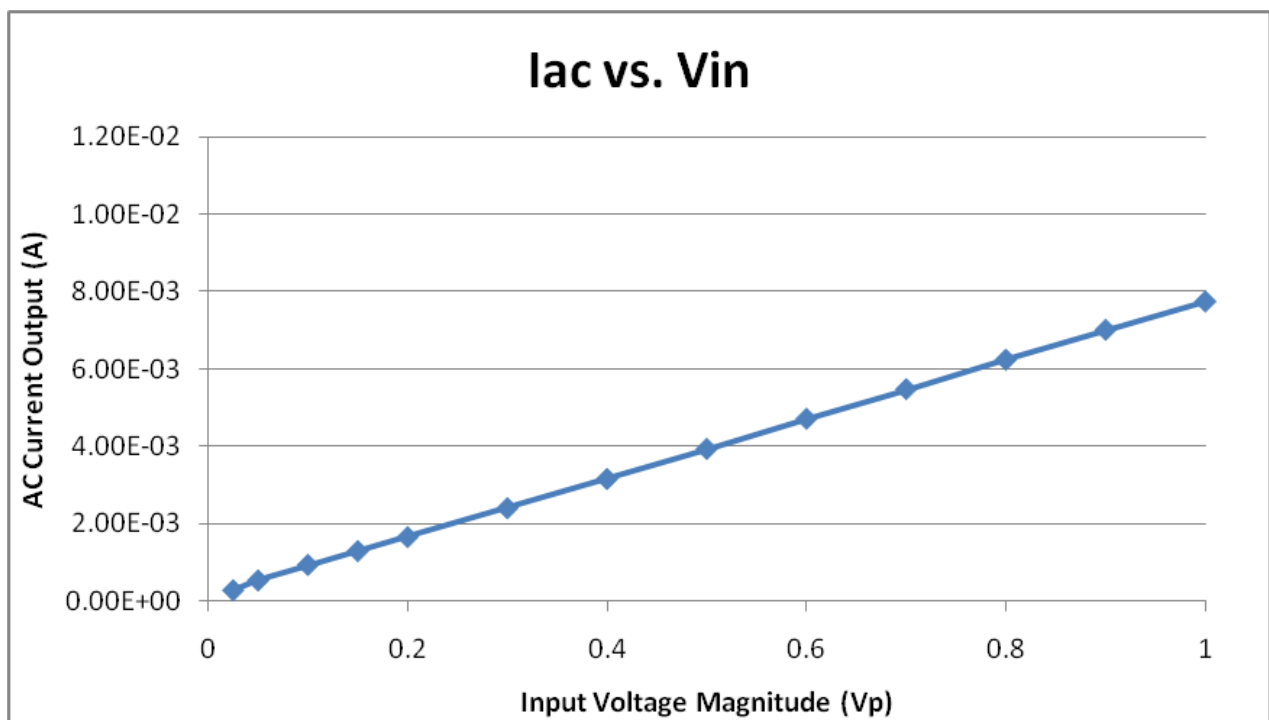
Simulation #3 : 18 kOhm bias, $V_r = 2$, $R2/R3 = 0.25$

 Figure 25) Simulation #3 I_{AC} and V_{IN} vs. I_{DC}

 Figure 26) Simulation #3 I_{AC} vs. V_{IN}

This simulation is an extreme case where the Class B amplifier is driven with a sinusoid that is twice as large as the sinusoid given to the Class C. The I_{AC} and V_{IN} curves match much more closely, and when the slopes are divided to produce the I_{AC} vs. V_{IN} , the result is much more linear than Simulations #1 and #2.

The problem with having such a large voltage ratio is that the Class B will enter a gain compression stage for lower input voltages. The reason that such a large voltage ratio was necessary was because the 18 kOhm bias resistor did not result in a good I_{DC} vs. V_{IN} curve. The next simulations address this issue.

Simulation #4 : 100 kOhm bias, $V_r = 0.5$, $R_2/R_3 = 1$

 Figure 27) Simulation #4 I_{AC} and V_{IN} vs. I_{DC}

 Figure 28) Simulation #4 I_{AC} vs. V_{IN}

By changing the bias resistor, the bias current is reduced. Additionally, the I_{AC} and V_{IN} curves match more closely, resulting in a I_{AC} vs. V_{IN} curve that is more linear than Simulation #1, which had the same current and voltage ratios, but a smaller bias resistor.

Simulation #5 : 100 kOhm bias, $V_r = 1$, $R_2/R_3 = 0.5$

 Figure 29) Simulation #5 I_{AC} and V_{IN} vs. I_{DC}

 Figure 30) Simulation #5 I_{AC} vs. V_{IN}

Finally, increasing the voltage ratio and decreasing the current ratio from Simulation #4 results in the most linear amplifier yet. It will be later shown that an amplifier that is very close to this one will result in the best linearity.

Constant Current Drain to Adjust Bends In Linearity Plots

It was found that by placing a constant current drain to ground on the Class C input to the op amp, the I_{AC} vs. I_{DC} curve for the Class C amplifier could be adjusted. By adjusting this curve, the overall linearity of the amplifier can be altered. This constant current source is shown as I1 in Figure 2.

The following simulation data demonstrate the effect of stealing current on the amplifier.

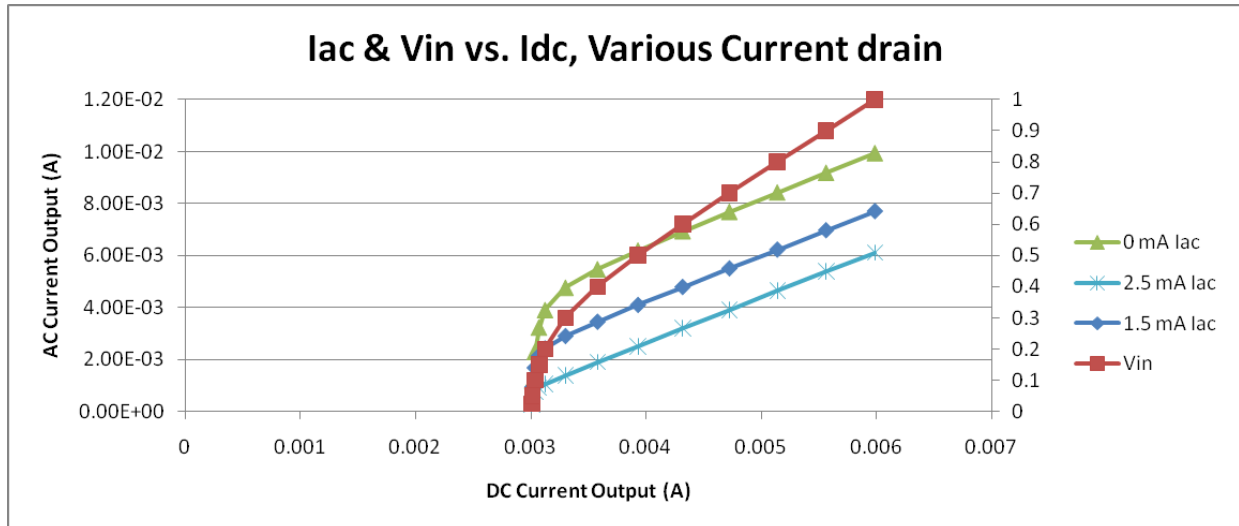


Figure 31) I_{AC} and V_{IN} vs. I_{DC} for Simulation #1 with various constant current drains

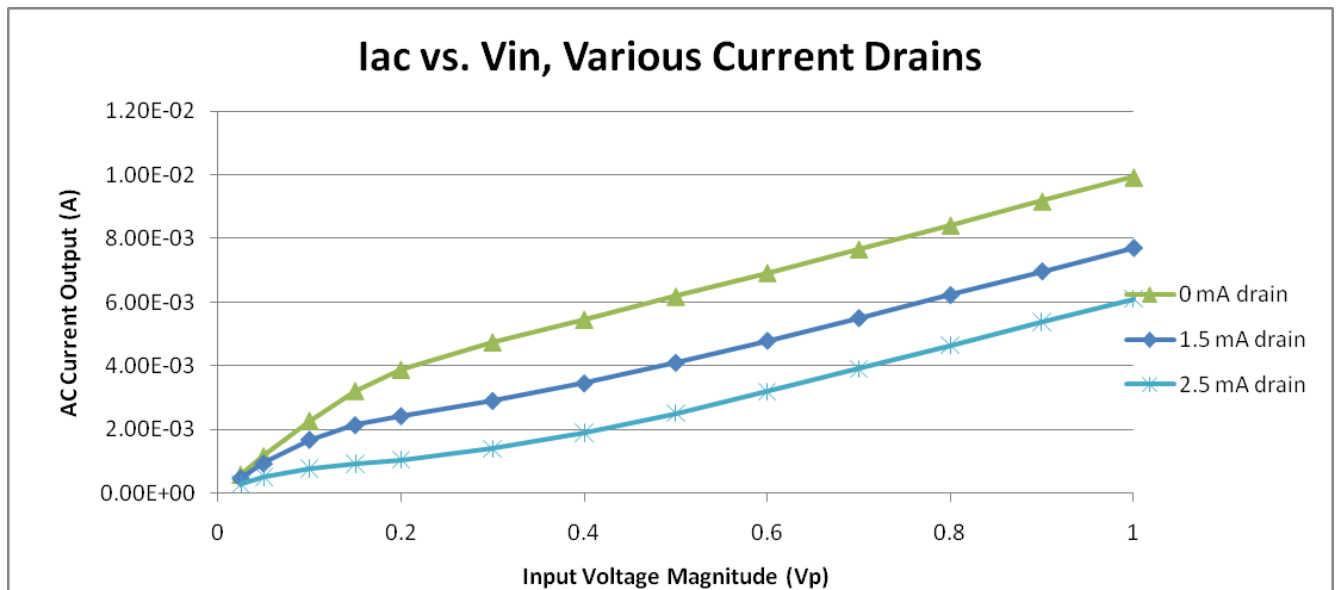


Figure 32) I_{AC} vs. V_{IN} for Simulation #1 with various constant current drains

The 1.5 mA curve in Figure 31 seems to cancel out the bend in the V_{IN} vs. I_{DC} curve the best. The result of this is seen in Figure 32, the 1.5 mA drain current is the most linear.

Two Tone Intermodulation Distortion

An amplifier that has a non linearity in its I_{AC} vs. V_{IN} curve will produce intermodulation products when amplifying inputs that have amplitude variations. To measure the linearity of an amplifier, a two tone intermodulation test can be done.

To perform a two tone intermodulation test, two sinusoids that are close in frequency are applied to the input, and then the intermodulation products are measured by performing the FFT. Intermodulation products occur at integer multiples $(f_2 - f_1)$, specifically $f_2 + n(f_2 - f_1)$ and $f_1 - n(f_2 - f_1)$

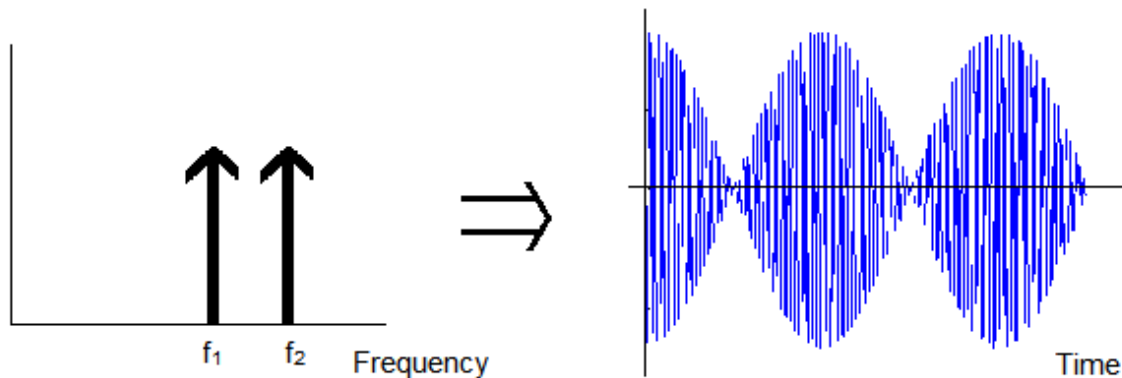


Figure 33) Frequency and time domain two tone intermodulation test

The data for a two tone intermodulation test is given as the magnitude of the intermodulation product as a function of output power. The intermodulation distortion varies as a function of output power due to the sweeping nature of the intermodulation test of the I_{AC} vs. V_{IN} curve. Sweet spots can arise at certain output powers. These sweet spots are output powers where the intermodulation distortion is very low. These result from some non-linearities on the I_{AC} vs. V_{IN} curve that cancel out at that output power.

The intermodulation distortion tests are done at inputs of 999 kHz and 997 kHz. It was found that if this spacing is too large, the feedback cannot keep up with the changing input.

The linearity of constant conduction angle amplifiers with different current and voltage ratios, and different current drains, will be simulated and analyzed by measuring the third order intermodulation products for a two tone input of 999 kHz and 1001 kHz. Graphs will be presented that show the 997 kHz component compared to the 999 kHz component.

Intermodulation Distortion Simulations for 18 kOhm Bias Resistor:

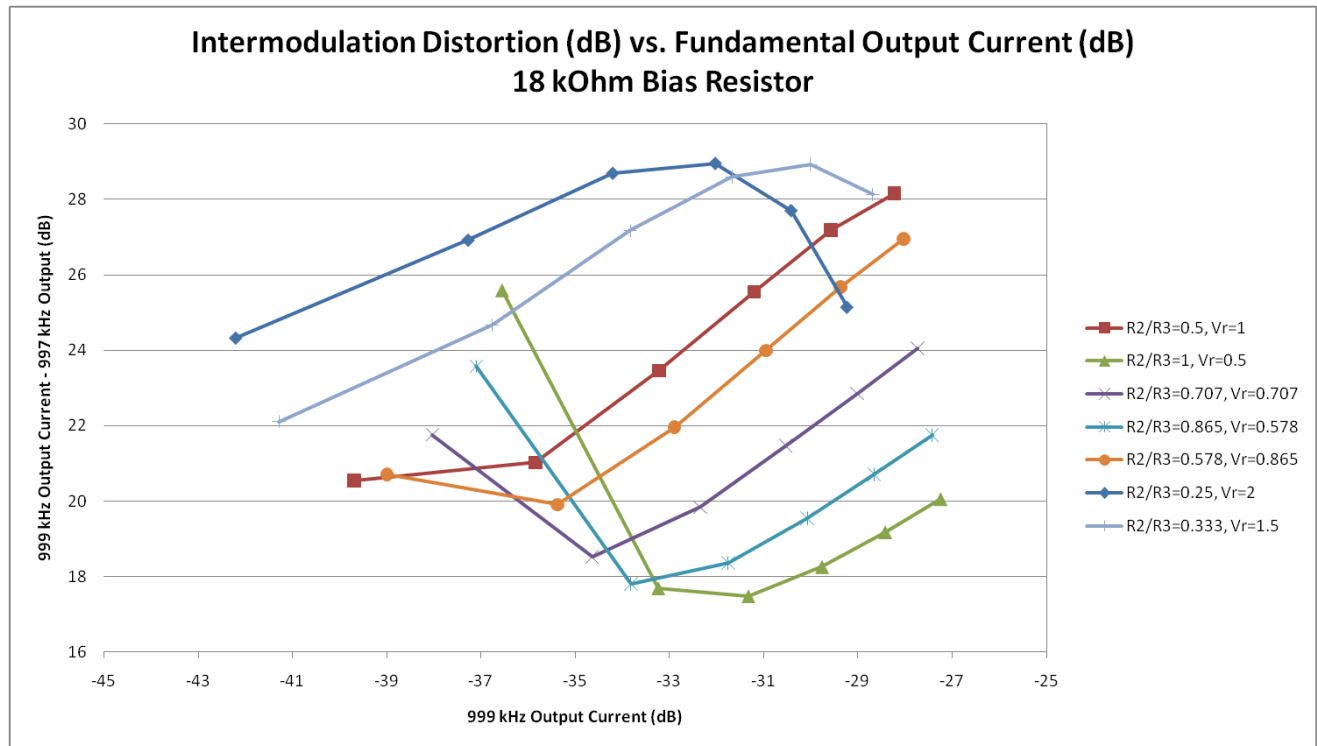


Figure 34) Two tone intermodulation distortion results for 18 kOhm bias resistor and various scaling ratios

Figure 34 shows simulated data for the amplifiers of Simulations #1, #2 and #3, and other current voltage ratio combinations that result in the same conduction angle. There seems to be a peak that shifts towards lower output power levels with increasing voltage ratio.

It is seen that the maximum intermodulation distortion reaches a minimum of -29 dBc.

Intermodulation Distortion Simulation for 100 kOhm Bias Resistor:

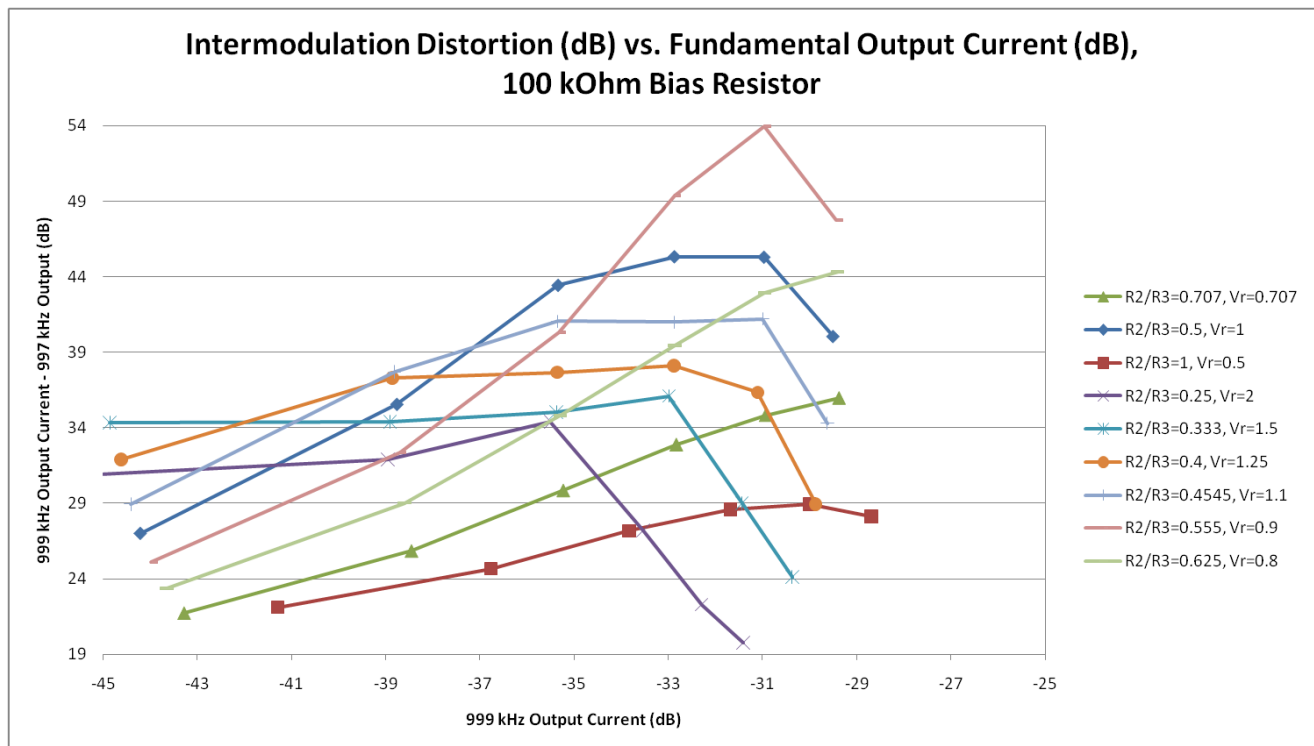


Figure 35) Two tone intermodulation distortion results for 100 kOhm bias resistor and various scaling ratios

Simulations #4 and #5 suggested that the most linear amplifier was likely to come from an amplifier that biased the Class B resistor with a 100 kOhm resistor. This is verified with intermodulation distortion simulations. Overall the best intermodulation distortion was found to be -53.9 dBc, which is 24.9 dB smaller than the best case intermodulation found with a 18 kOhm bias resistor.

A sweet spot was found where the voltage ratio is equal to 0.9 and the current ratio is equal to 0.5555. Changing the ratios away from these sweet spot ratios seems to shift the peak left and right, but it also severely reduces the magnitude of the peak. The next section deals with moving this peak and not greatly affecting its magnitude.

Reducing Intermodulation Distortion with Constant Current Drain

A constant current drain was shown previously to affect the linearity of the constant conduction angle amplifier, thus it will also effect, and can also be used to minimize, the intermodulation distortion. Increasing the drained current was shown to lower the I_{AC} vs. I_{DC} curve for the class C amplifier. When the Class C amplifier is forced to follow a scaled Class B I_{DC} vs. V_{IN} curve, increasing the current drained results in lowering a portion of the I_{AC} vs. V_{IN} curve, which can be used to reduce the intermodulation distortion.

It is difficult to choose a current drain value that works best with a certain voltage and current scaling ratio. From simulations, it seems that the best current drain value is related to the scaled DC bias current of the Class B amplifier. For smaller bias currents, or larger $I_{DC,C} / I_{DC,B}$ current ratios, the optimal current drain is smaller.

To illustrate the effect of changing the current drain on the Intermodulation distortion, consider the following plot. The curves maintain the same current and voltage ratios, but the amount of constant current drain is changed.

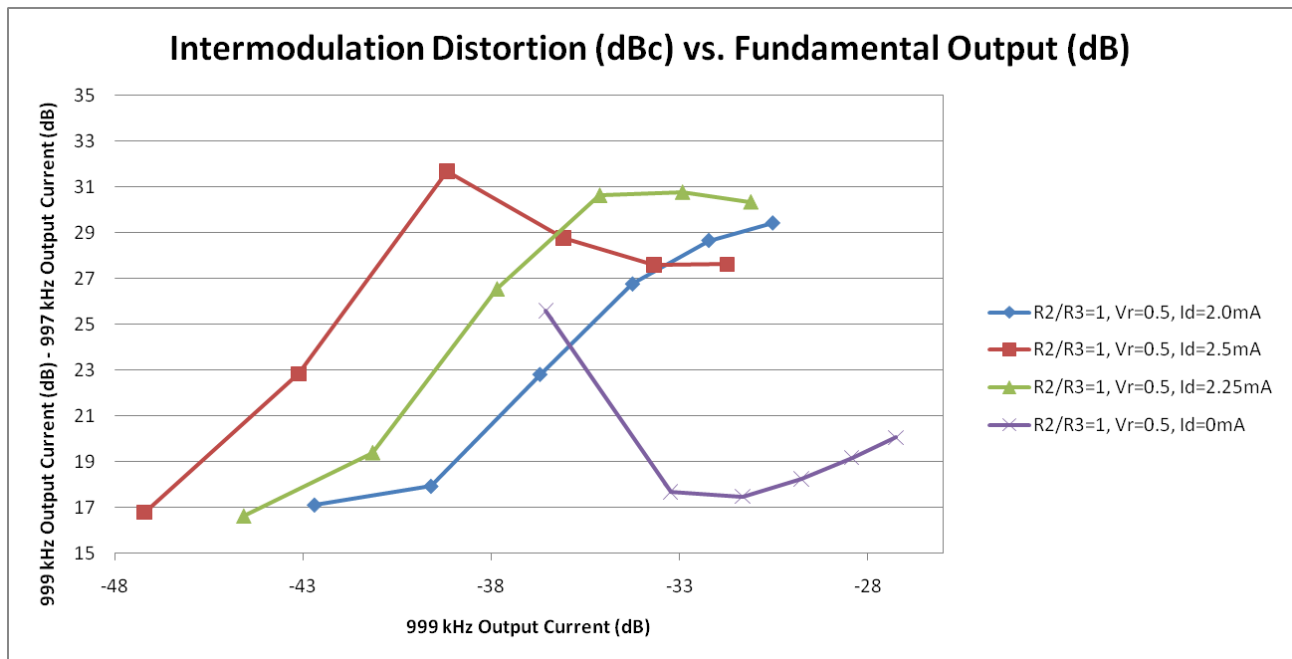


Figure 36) Two Tone Intermodulation Data for 18 kOhm bias resistor, $V_{DC,B}/V_{DC,C} = 0.5$, $I_{DC,C}/I_{DC,B} = 1$ and various constant current drain values

From Figure 36, it is seen that changing the constant current drain value can be used to find a minimum intermodulation distortion, or can be used to move that sweet peak in intermodulation distortion to different Output powers. Changing the constant current drain can be used to tune the sweet spot to some specific output power.

To demonstrate the effect of changing the constant current drain on an amplifier that has already been optimized for a best intermodulation distortion by tuning the current and voltage ratios, consider the following bias current, and current and voltage ratios: 100 kOhm bias resistor, $V_{DC,B}/V_{DC,C} = 0.9$, $I_{DC,C}/I_{DC,B} = 0.555$. This is the configuration that was found to have the best intermodulation distortion at -53.9 dBc.

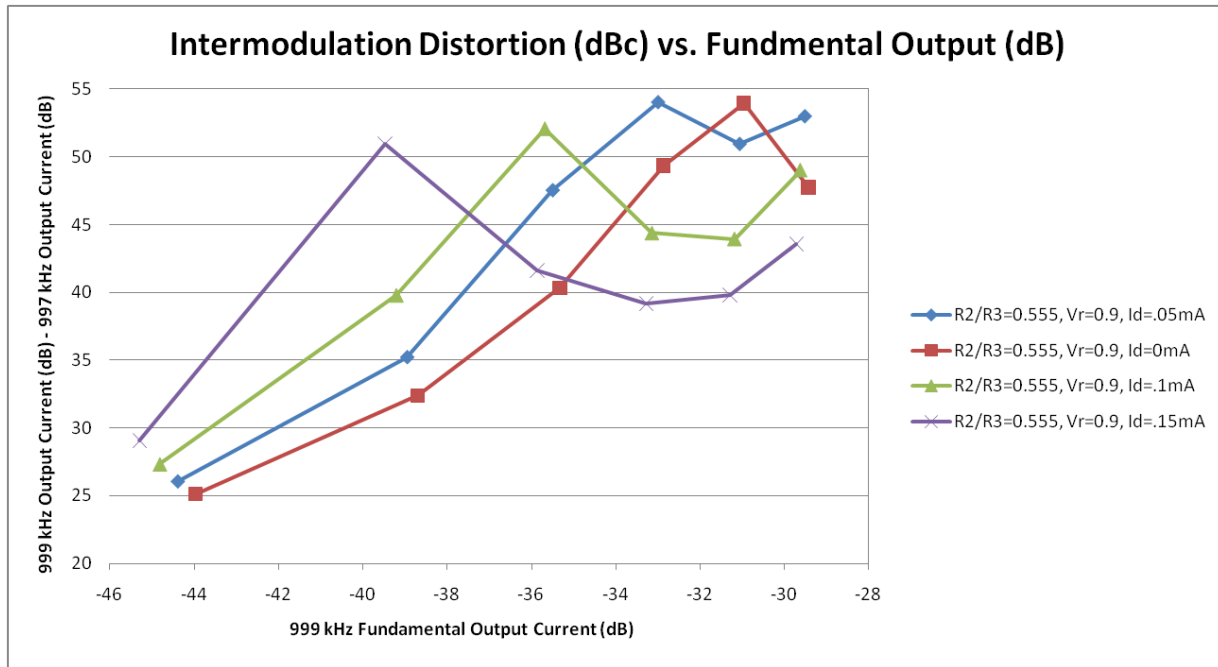


Figure 37) Two Tone Intermodulation Data for 100 kOhm bias resistor, $V_{DC,B}/V_{DC,C} = 0.9$, $I_{DC,C}/I_{DC,B} = 0.555$ and various constant current drain values

It is seen that an amplifier that has already been optimized to achieve the best intermodulation distortion at some output power, can be adjusted by a constant current drain, to shift at what power level that intermodulation distortion sweet spot occurs. Shifting the sweet spot with a current drain does not affect the magnitude of the sweet spot as much as shifting the sweet spot by changing current and voltage ratios. The peak was shifted down 9 dB in output power and only lost 2 dB of intermodulation suppression, while the method of shifting the peak by changing current and voltage ratios suffered over 20 dB of intermodulation distortion to shift the peak the same amount.

Suggested Method For Tuning A Constant Conduction Angle Amplifier

To obtain a constant conduction angle amplifier with the optimum current and voltage ratios, and constant current drain value, for a desired two tone intermodulation distortion at a specific output power, the following steps are suggested:

1. Find the bias resistor that leads to the most linear I_{DC} vs. V_{IN} for the Class B amplifier. This curve should have a large linear segment that if extended will pass through the origin.
2. Determine the desired conduction angle and various ratios that would achieve it.
3. Obtain an I_{AC} vs. V_{IN} plot for the Class C amplifier at some current and voltage ratio. Assess the linearity of the plot by extending the linear segment to see how close it comes to passing through the origin. Compare to linearity plots presented in this paper to assess how the current voltage ratio should be adjusted.
4. Adjust the current and voltage ratios to obtain a linear I_{AC} vs. V_{IN} plot. This is the starting point ratio.
5. Apply a two tone intermodulation distortion test and measure the level of the third order intermodulation product. Adjust current and voltage ratios to find a minimum intermodulation distortion at some output power.
6. Apply a constant current drain to shift the peak in the intermodulation distortion to the desired output power. Small changes to the current and voltage ratios determined in step 5 may help to minimize intermodulation distortion.

Conclusion

This paper presented a circuit to bias a Class C amplifier to have a constant conduction angle that adapts to the input power presented to it. This results in an efficient, yet very linear, Class C amplifier that can be used with signals that have amplitude variations.

This circuit works by comparing the DC currents in a dummy Class C to a dummy Class B amplifier, and adjusting the DC bias voltage of the dummy Class C amplifier so that the DC current in the dummy Class C amplifier is some scaled version of the dummy Class B DC current. The bias voltage that is generated is then used to bias a larger scaled output transistor, which is given the same input as the dummy Class C. Because the large output transistor is a scaled version of the smaller dummy Class C amplifier, it will be biased the same and exhibit the same conduction angle and linearity.

The conduction angle of the amplifier can be set by either adjusting the ratio of the magnitudes of the input voltages to the two amplifiers, adjusting the DC current forced on the Class C by some constant, or both.

The effect of a knee in the current voltage characteristics of an amplifier is addressed. It was shown that a real Class B amplifier has a DC current flow when the input voltage is zero. Since the Class C amplifier is forced to follow a scaled version of the Class B I_{DC} vs. V_{IN} curve, the Class C I_{AC} vs. V_{IN} curve must have a bend to account for it. It was shown that adjusting the current and voltage ratios between the dummy Class C and dummy Class B could be used to maximize make these two bends cancel each other out, leading to a linear I_{AC} vs. V_{IN} for the Class C.

Linearity was measured with a two tone intermodulation test. Certain current and voltage ratios lead to peaks in the intermodulation distortion. Shifting these peaks to different output powers by a constant current drain was demonstrated.