# Comparative Study of Sinusoidal Pulse-Width and Hysteresis Modulations in Current Source Inverter

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***Abstract*—In this paper, modeling and comparative analysis of Current Source Inverter (CSI) using Sinusoidal Pulse-Width-Modulation (SPWM) and Hysteresis Modulation (HM) will be presented. The modeling of both CSI-SPWM and CSI-HM are implemented using OrCAD Pspice. Results from the simulations will be presented along with the performance analysis of both inverters. More specifically, comparative analysis pertaining to output current regulation, harmonic contents, and transient response will be discussed. Moreover, further investigation about the effect of current THD, power factor and efficiency for balanced and unbalanced three-phase input sources with ±1%, ±3%, ±5% rms variation at the converter stage to various output loads will be described.**

## I. Introduction

Until now, the constant frequency and magnitude AC power has remained generally superior to other forms for generation and transmission purposes. However, it has been long recognized that this form of power is not suitable for many industrial processes and residential applications. For example, many chemical processes required controllable Direct Current (DC) voltage source, and most AC motors require three phase AC voltage with controllable frequency and magnitude. In addition, many precision machines and strategically important devices require constant magnitude AC voltage source with high reliability and continuous power flow regardless of the utility line unbalances and fault conditions. Therefore, in most of these applications the utility line power cannot be directly utilized; interfaces and devices to convert the form of the line power are necessary. The strong demand for power conversion and conditioning devices to achieve these tasks has led to the establishment of the power electronics field early in twentieth century. High performance semiconductor power switches, efficient power converter circuit topologies, and intelligent control algorithms have been invented. As a result of this evolution, today's many industrial and residential loads are connected to the AC power line through cost effective power converter circuits which enhance the overall performance, efficiency, and reliability.

It is in the application area of adjustable speed AC motor drives that modern progress in power electronics is having the most significant impact. Historically, the two most important categories of AC motors, induction motor and synchronous motor, were considered unsuitable for adjustable speed applications since the AC power system frequency is fixed at 60Hz or 50Hz. However, AC motors have definite advantages in cost, size, weight, and require much less maintenance compare with DC motors. Progress in power electronics has made it possible to build inverters that could provide AC power with adjustable frequency and adjustable voltage.

Pulse width modulation (PWM) is a popular technique that is widely used in many adjustable speed drive (ASD) applications. There are a number of schemes of PWM. Prominent among these are sinusoidal pulse width modulation (SPWM), phase-shift PWM, hysteresis modulation (HM), and optimal PWM techniques based on the minimization of certain performance criteria – for example, selective harmonic elimination, optimization of efficiency, and minimization of torque pulsations [1]. SPWM is commonly used and is well-documented in many literatures such as in [2] [3]. The method of HM has existed for years; however, many circuit implementations have not been examined extensively or documented in details. A couple of examples of papers that discussed HM CSI are [4] and [5]. The purpose of this paper is to study a CSI using SPWM topology for the switching scheme and then compare its performance with HM topology for the switching scheme. A computer simulation of the two designs using OrCAD Pspice will be the method to compare the two models.

## II. Modeling of SPWM CSI

### A. Converter Stage

A general model of CSI consists of the converter stage, the inverter stage and the load stage. A three-phase, full bridge diode rectifier circuit may be used to simulate the rectification of a three-phase source. The following equations are used to calculate the rectified DC current produced by this circuit:

$$v_a(t)=V_A\sin(\omega t) \tag{1}$$

$$v_b(t)=V_B\sin(\omega t-\frac{2\pi}{3}) \tag{2}$$

$$v_c(t)=V_C\sin(\omega t-\frac{4\pi}{3}) \tag{3}$$

$$V_\phi=\frac{V_{LL}}{\sqrt{3}} \tag{4}$$

$$V_{\phi m}=\sqrt{2}V_{\phi rms} \tag{5}$$

$$A_d=\int_{\frac{-\pi}{6}}^{\frac{\pi}{6}}\sqrt{2}V_{LL}\cos(\omega t)\cdot d(\omega t)=\sqrt{2}V_{LL} \tag{6}$$

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$$V_d = \frac{A_d}{\frac{\pi}{3}} = \frac{3\sqrt{2}}{\pi} V_{LL} = 1.35 V_{LL} \quad (7)$$

$$I_d = \frac{V_d}{Z} = \frac{V_d}{\sqrt{R_d{}^2 + (\omega L_d)^2}} \quad (8)$$

$$I_{dm} = \sqrt{2}\, I_{drms} \quad (9)$$

Above equations reveal that with balanced three-phase $480V_{rms}$ line to line input voltages, the expected unfiltered DC output voltage is 648V. Also, in order to obtain a 14.14A ($10A_{rms}$) DC current, a resistor and a sufficiently large inductance are needed to smooth out the current. For this paper, the load uses $R_d = 45\Omega$ and $L_d = 1H$.

*B. Inverter Stage*

With OrCAD Pspice, the inverter stage is modeled with a piecewise linear current source, IPWL, and six ideal switches, Sbreak. The piecewise linear current source is chosen in order to avoid convergence errors for the rest of SPWM simulations. The line-to-line capacitors are used to filter the output current at the loads.

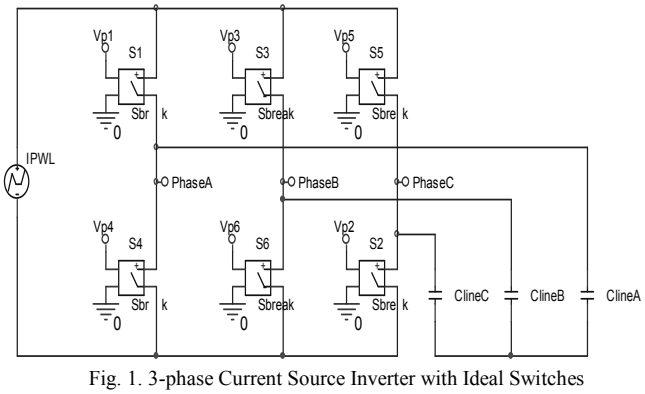


Fig. 1. 3-phase Current Source Inverter with Ideal Switches

*C. Switching control scheme and Feedback*

The circuit used for the switching and feedback control of phase A is shown in Figure 2. A sensing resistor ($R_{s\text{-}ref}$) is inserted in the sinusoidal reference current to give a sinusoidal reference voltage to the PI controller or error amplifier with compensation. The sinusoidal reference voltage is followed by two ideal comparators. The comparator is used to compare its two inputs: one from the output of the PI controller (error voltage), and the other one from the triangular voltage waveform. The top comparator generates gating pulses for the top switch (Vp1) while the bottom comparator drives the bottom switch (Vp4). The switch is turned on when the sinusoidal error voltage is greater than the triangular voltage waveform. The switch is turned off when the sinusoidal error voltage is less than the triangular voltage waveform. Once the switch starts conducting, it causes the resistive and inductive load to see the DC current. The load current is fed back through a sensing resistor ($R_{s\text{-}fb}$) to give a feedback voltage. To compare the sinusoidal reference voltage and the feedback voltage, a PI controller or a compensated error amplifier is employed [6].

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{Z_{fb}}{Z_{in}} = -\frac{(R_f + \frac{1}{sC_1})\frac{1}{sC_2}}{R_{s1}(R_f + \frac{1}{sC_1} + \frac{1}{sC_2})} \quad (10)$$

Assuming $C_2 << C_1$ and rearrange terms in equation (10):

$$\frac{V_{out}(s)}{V_{in}(s)} \approx -\frac{s + \frac{1}{R_f C_1}}{R_{s1} C_2 s(s + \frac{1}{R_f C_2})} \quad (11)$$

The PI gain may be adjusted through selection of $R_f$ and $R_{s1}$. For a satisfactory performance, a gain of 40 will be used. To accomplish this, resistor values of $R_f = 200k\Omega$ and $R_{s1} = 5k\Omega$ are selected. The cutoff frequency of the error amplifier is 1.013 kHz. The values of $C_1$ and $C_2$ are chosen such that the output voltage of the error amplifier is sinusoidal as close as possible and to ensure the overall system is stable.

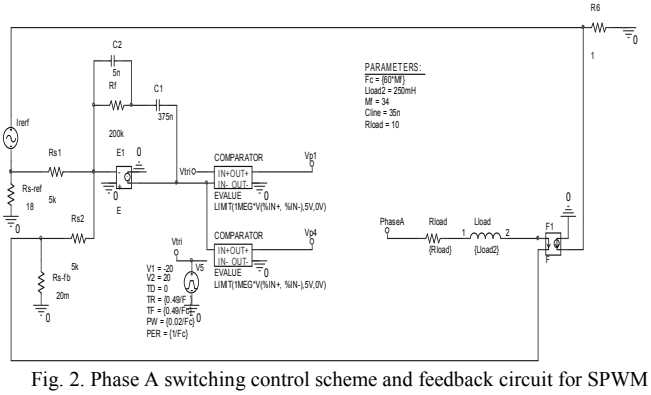


Fig. 2. Phase A switching control scheme and feedback circuit for SPWM

## III. Modeling of HM CSI

*A. Hysteresis Modulation*

Hysteresis Modulation (HM) is a voltage or current feedback control method. Its purpose is to synthesize the switch gating signals in such a way that the output voltage or current waveform tracks the reference voltage or current waveform within a hysteresis band. As Figure 3 shows, a reference waveform of desired magnitude and frequency is compared with the actual output waveform, and the intersection points determine the switching and pulse widths. If the actual output waveform exceeds the upper limit of the hysteresis band, the top switch is turned off and the bottom switch is turned on. As a result, the output waveform starts to decay. If the output waveform crosses the lower limit of the hysteresis band, the bottom switch is turned off and the top switch is turned on. As a result, the output waveform gets back into the hysteresis band. Hence, the actual output waveform is forced to track the reference waveform within the band, or mathematically [1]:

$S_1$ is on when $i_A > i_{LOWER\text{-}BAND}$ $S_4$ is on when $i_A < i_{UPPER\text{-}BAND}$
$S_3$ is on when $i_B > i_{LOWER\text{-}BAND}$ $S_6$ is on when $i_B < i_{UPPER\text{-}BAND}$
$S_5$ is on when $i_C > i_{LOWER\text{-}BAND}$ $S_2$ is on when $i_C < i_{UPPER\text{-}BAND}$

*B. Converter Stage*

Figure 4 illustrates the model for the input or converter stage of the HM-CSI. Balanced 3-phase line to line $480V_{rms}$

input voltages are sent to three (1:240) step up transformers. The output voltage of the transformers is fed into the 3-phase full bridge diode rectifier circuit and is used to simulate the rectification. A large capacitor, $C_d$, is added in parallel at the output of the rectifier in order to filter out the ripple voltage.

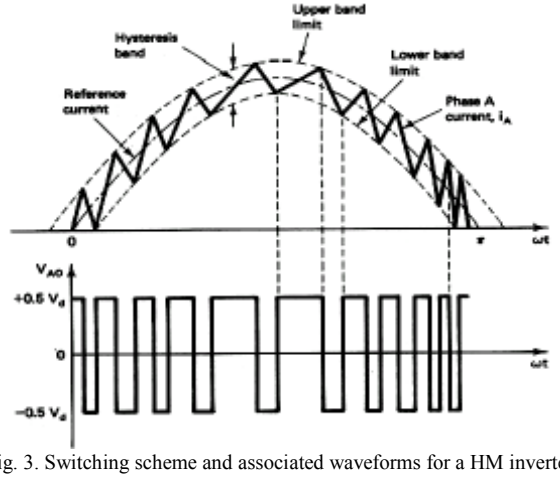


Fig. 3. Switching scheme and associated waveforms for a HM inverter

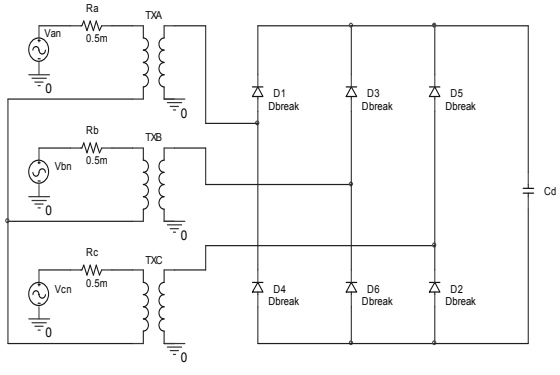


Fig. 4. Three-phase Full-bridge Rectifier

*B. Inverter Stage*

The CSI is modeled with a piecewise linear voltage source, VPWL, and six ideal switches, Sbreak as shown in Figure 5. Similar to SPWM switching control scheme, the piecewise linear voltage source is chosen in order to avoid convergence errors for the rest of HM simulations.

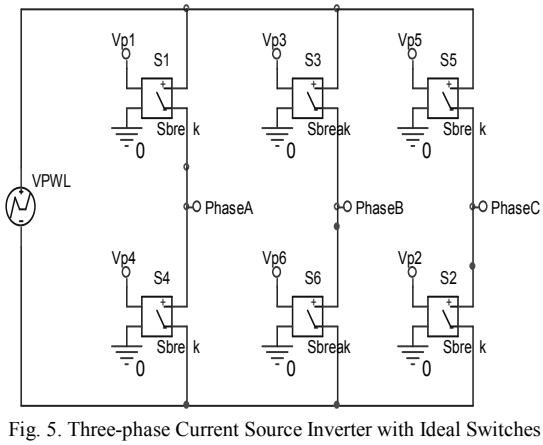


Fig. 5. Three-phase Current Source Inverter with Ideal Switches

*C. Switching control scheme and Feedback*

Only one phase of the circuit is shown in Figure 6 for the following discussion. Since the load is balanced, the circuit implementation of the remaining two phases is identical with a 120˚ and 240˚ phase difference respectively for the sinusoidal reference current.

As in the switching control of SPWM, a sensing resistor ($R_{s\text{-}ref}$) is inserted in the sinusoidal reference current to give a sinusoidal reference voltage to the compensated PI controller. The sinusoidal reference voltage is followed by two ideal comparators. The top comparator is used to compare its two inputs: one from the output of the PI controller (error voltage), and the other one from the upper voltage band limit. The bottom comparator is used to compare its two inputs: one from the output of the PI controller, and the other one from the lower voltage band limit. Unlike SPWM, the outputs from the two comparators cannot directly feed to the top and bottom switches since there is an overlapping time period when both comparators are turned on. The switching control scheme needs to ensure that only one switch is turned on/off at a time. Hence, the outputs from the two comparators are first fed into a set-reset (SR) latch implemented by two NAND gates. The truth table for the NAND-gates SR-latch is as follows:

Table 1. Truth table for a NAND-gates SR-latch

| Input R | Input S | Output Q | Output $\bar{Q}$ |
|---|---|---|---|
| 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

As in SPWM, to compare the sinusoidal reference voltage and the feedback voltage, a compensated error amplifier is employed. Similar to SPWM, the error amplifier has a gain of 40 using equation. The cutoff frequency is 1.013 kHz. The values of the capacitors are chosen such that the output voltage of the error amplifier is forced within the voltage band limit and to ensure the overall system is stable.

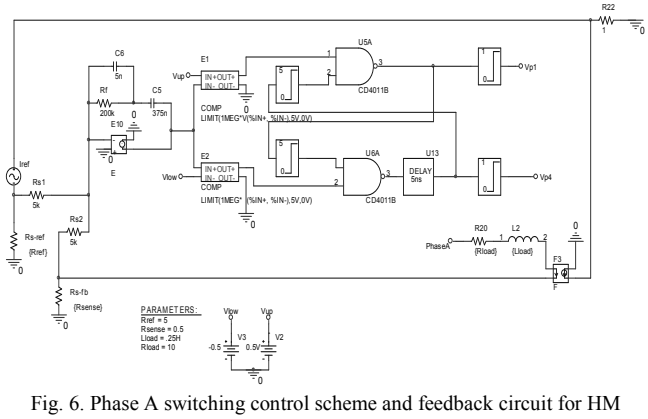


Fig. 6. Phase A switching control scheme and feedback circuit for HM

## IV. Simulation Results

*A. SPWM CSI*

Figure 7 verifies that the SPWM CSI regulated the sinusoidal output current at 14.14 $A_{pp}$ (10 $A_{rms}$). By adding

line-to-line capacitors at the inverter stage, SPWM CSI has maintained a less than 1A of output ripple current.

The harmonic measurements are made when the load current reaches steady state conditions. The output file for the simulation lists the current THD as 2.2975%. As expected for SPMW, the harmonics should appear as side bands around 60 Hz and its multiples, as shown in Figure 8. The fundamental component at 60Hz is 14.79A. The rest of harmonics are from the switching frequency of the SPWM inverter.

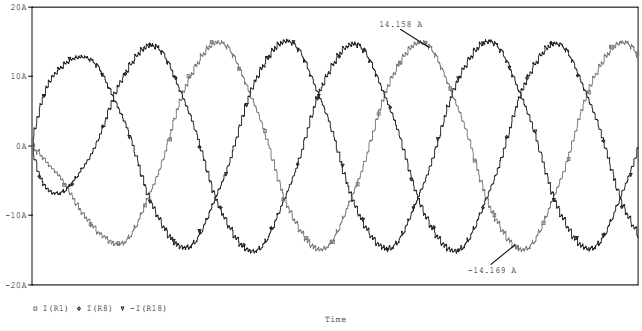


Fig. 7. Output currents of SPWM CSI

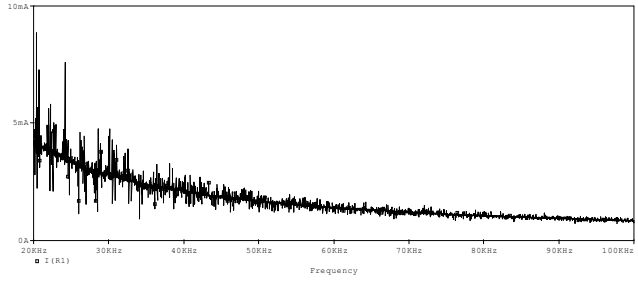


Fig. 8. Fast Fourier transform of the current for the SPWM CSI

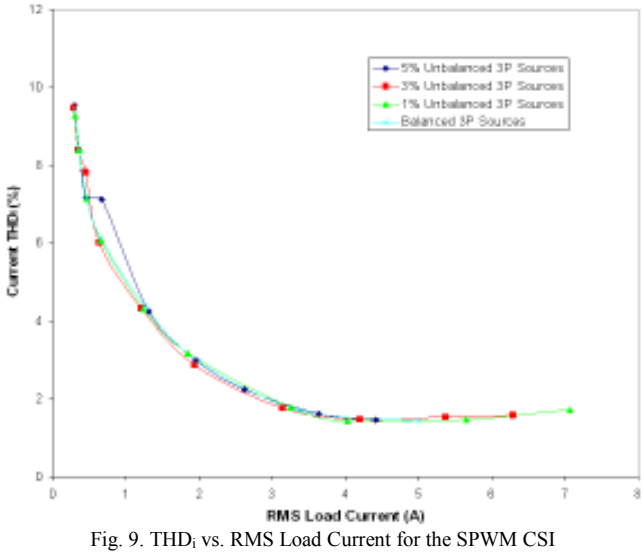


Fig. 9. $THD_i$ vs. RMS Load Current for the SPWM CSI

Further investigation is studied on the effect of current THD and power factor balanced and unbalanced three-phase input sources with ±1%, ±3%, ±5% rms variation at the converter stage to various output loads. Figure 9 shows the relationship between current total harmonic distortion and the RMS load current. The graph of balanced 3-phase input sources exhibits an exponentially decay curve. With unbalanced three-phase input sources at the converter stage, the current THD curves behave similarly compare to the balanced three-phase input sources. However, they have lower current harmonics at lower RMS load current and remain relatively identical at higher RMS load current. As percentage of RMS variation increases at the converter stage, the output rectified DC current used by the inverter slightly decreases. The current reduction at the inverter stage also decreases the RMS load current at the output stage. Current harmonics can simply defined as the ratio of ripple current divided by the RMS load current. With the ripple current remains constant, the change in the ratio between these two numbers is less severe at higher RMS load current. However, the change in the ratio between these two numbers is more sensitive at lower RMS load current. The sensitivity can be shown on the current THD curve of unbalanced three-phase input sources with ±5% RMS variation. It has a visible hump around 1 $A_{rms}$ and becomes less smooth compare to the other three cases.

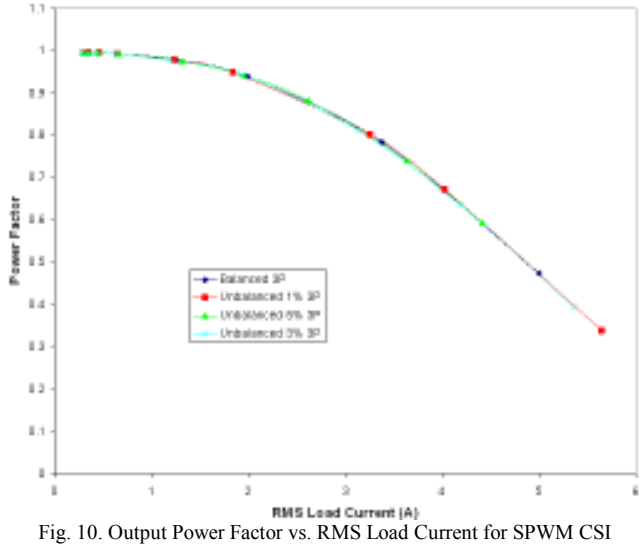


Fig. 10. Output Power Factor vs. RMS Load Current for SPWM CSI

Since the inverter is driving inductive loads, the output power factor is always a lagging power factor. SPWM exhibits a gradual decrease in output power factor as the RMS load current proportionally decrements. Output power factor ranges from 0.3 at higher RMS load current to 0.99 at lower RMS load current. As observed in Figure 10, the distortion power factor does not trigger the dramatic decrease in the output power factor since all current THDs are less than 10%. The major contribution is from the displacement power factor. The dramatic decrease in displacement power factor at higher RMS load current can be caused by the line-to-line capacitive filtering which creates the phase difference between the output voltage and output current. Figure 10 also shows that all four cases display almost identical power factor curves. This means that the unbalanced input sources have little effect on the output power factor despite the lower rectified DC current at the converter stage.

*B. HM CSI*

Figure 11 verifies that the HM CSI regulated the sinusoidal output current at 14.14 $A_{pp}$ (10 $A_{rms}$). With 1V error limit in

the control circuitry, the HM CSI tries to minimize the output ripple current to be less than 1A in order to maintain a 1:1 relationship of voltage error limit and output ripple current.

The harmonic measurements are made when the load current reaches steady state conditions. The fundamental component at 60Hz is 14.78 A. Compare with that of SPWM, HM CSI has a noisier fast Fourier transform. HM has harmonic components appear at every multiples of 60Hz. The harmonic components are from the three-phase full-bridge rectifier due to the harmonics order of 6n ± 1. Others come from the fact that HM has random switching frequency since the switching frequency is controlled by the voltage error limit in the control circuitry.

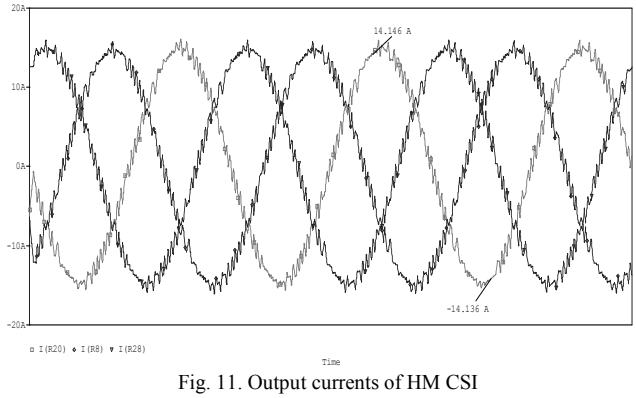


Fig. 11. Output currents of HM CSI

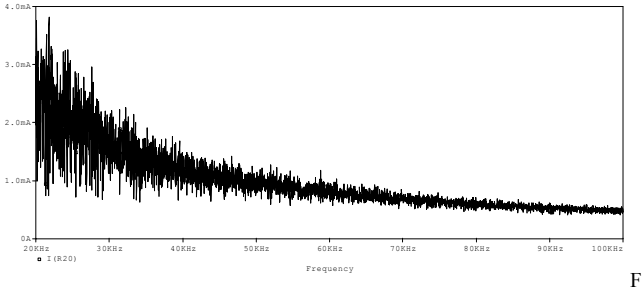


Fig. 12. Fast Fourier transform of the current for HM CSI with 1V Error Limit

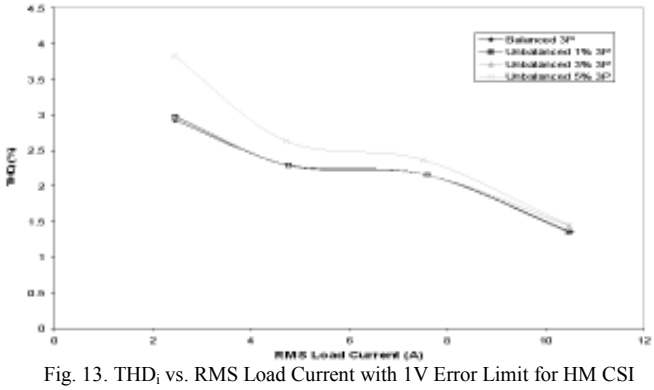


Fig. 13. $THD_i$ vs. RMS Load Current with 1V Error Limit for HM CSI

Further investigation is studied on the effect of current THD, power factor and efficiency for balanced and unbalanced three-phase input sources with ±1%, ±3%, ±5%. Similar to SPWM, HM exhibits a decrease in RMS load current translates to higher current THD, whereas an increase in RMS load current translates to lower current THD. With ripple current regulated by the voltage error limit in the control circuitry, the change in the ratio between these two numbers is less severe at higher RMS load current. However, the change in the ratio between these two numbers is more sensitive at lower RMS load current. Figure 13 validates this relationship between $THD_i$ and RMS load current. The current THD comparison studies of balanced and unbalanced three-phase input sources at the converter stage with same voltage error limit are also shown in Figure 13. It shows with the unbalanced input sources with ±5% RMS variation, a 27.7% noticeable deviation is noted compared to the balanced case. The other two unbalanced cases curves remain close to the balanced curve, with unbalanced input sources with ±1% RMS variation display almost identical to the balanced case. This means to maintain current THD performance, input voltage sources need to be maintained within the ±3% RMS variation.

Similar to SPWM, the output power factor is always a lagging power factor since the inverter is driving the inductive load. HM maintains a 0.99 or above lagging output power factor in all cases. The output power factor comparison studies of balanced and unbalanced three-phase input sources at the converter stage with same voltage error limit are shown in Figures 14. The graph shows that the unbalanced ±5% RMS variation input sources display a V-shape curve, while the other three curves exhibit a gradual increase in output power factor as the RMS load current proportionally increments and remain very close to each other. The unbalanced ±5% RMS variation should be avoided since it greatly deviates from the other three cases. Once again, the 0.913% average increase for the rectified DC voltage at the inverter stage translates some noticeable amount of deviation for output power factor.

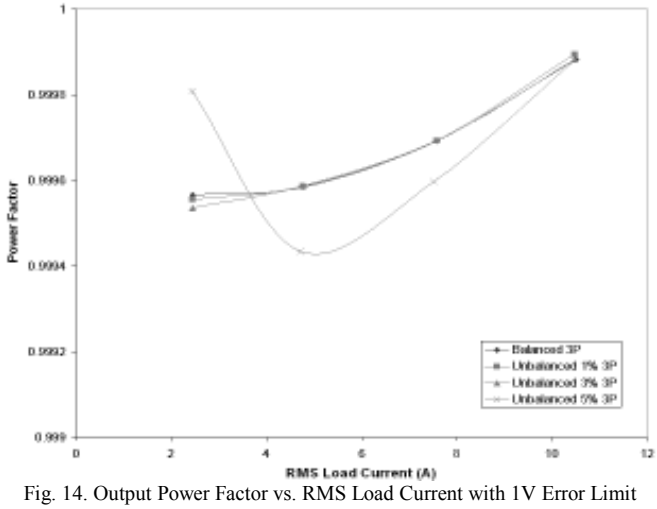


Fig. 14. Output Power Factor vs. RMS Load Current with 1V Error Limit

## V. Conclusion

Both SPWM and HM designs are effective in regulating the output load current to be sinusoidal and at its regulating value. The filtering at the load is done by adding external line-to-line capacitors in SPWM, while the filtering at the load depends on the voltage error limit internally within HM. Both circuits have similar percentage of current total harmonic distortion at various output loads. However, the HM is noisier at higher

frequency by observing the current fast Fourier transform. In this thesis, the minimum voltage error limit is 1V in the switching control circuitry. To further reduce the noise and provides better filtering is to continuously lower the voltage error limit. Even though it is desirable to use as high as a switching frequency as possible, one significant drawback is switching loss in the inverter switches increases proportionally with switching frequency. Hence, the switching frequency was selected to be either less than 6 KHz or greater than 20 KHz to be above the audible range.

Results from both studies showed the benefit of using SPWM and HM CSI when imbalances were imposed to their inputs. Both studies revealed results from the ±3% RMS variation unbalanced input sources at the converter stage are satisfactory and can be tolerated compare to the balanced case. Both studies show that ±5% RMS variation unbalanced input sources at the converter stage should be avoided since results deviated the most compare to the other three cases.

Further study of this project should extend the model from using ideal switches in the models to a more realistic design and implementation. Additionally, hardware implementation could be built to further validate the results from this paper.

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## BIOGRAPHIES

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