Efficiency Performance Analysis of Series Loaded Resonant Converter

Michael McCarty
Electrical Engr. Dept.
Cal Poly State University
San Luis Obispo, USA

Taufik Taufik
Electrical Engr. Dept.
Cal Poly State University
San Luis Obispo, USA

Andre Pratama
Electrical Engr. Dept.
Cal Poly State University
San Luis Obispo, USA

Makbul Anwari
Faculty of Electrical Engr.
Univ. Teknologi Malaysia
81310 UTM, Malaysia

***Abstract*—Series Loaded Resonant (SLR) converter is a well known topology typically used in kilowatt-range power supplies. The topology may operate in either continuous or discontinuous conduction modes whose switching properties are covered in many power electronic text books. However, information related to the actual converter's efficiency for each conduction mode is lacking and thus will be addressed in this paper. The development of a lab scale SLR converter will be described along with results of computer simulation. Efficiency performance from hardware results for each conduction mode when output power and switching frequency are varied will also be discussed.**

***Keywords*—Resonant Converter; Power Supply**

I. INTRODUCTION

One of the trends in the Power Electronics field is the pursuit of highly efficient power supplies. This has motivated engineers to come up with new designs that drastically improve power conversion. Switching power supplies have typical efficiency of 70% to 80% compared to the 50% to 60% of regular linear power supplies making them highly preferable [1]. These power supplies transform energy by basically turning on and off the input voltage very fast, so the output voltage is the average of the switched input voltage over a period of time.

The efficiency of a converter is determined by how well the input power is being processed to deliver the desired output power to the load. Efficiency then is the ratio of the average output power over the average input power. As previously stated, switching power supplies provide an efficiency of about 80%, and so the remaining 20% or less is the power that "stays" in the power converter in the form of semiconductor forward drop loss, ac switching loss, and dc conduction loss, among others.

A resonant converter is a power supply topology that enables improved efficiency by introducing sinusoidal switching waveforms instead of the more commonly used square switching waveforms [2]. This causes the provision of Zero Current Switching (ZCS) and the Zero Voltage Switching (ZVS) modes. With these modes, the switch in the converter is turned on or off when the current or voltage across it is zero, thus switching losses are minimized [3].

To produce the sinusoidal waveforms, the resonant converter utilizes an LC resonant tank circuit. Another main advantage of having sinusoidal switching besides efficiency is that the total harmonic distortion and electromagnetic interference will also be reduced which are important in many applications that require a "quiet" power supply.

Due to the aforementioned advantages, resonant converter is an obvious choice for high-voltage high-frequency power supplies commonly found in medical equipment [4]. To achieve a high-voltage converter, the transformer would be a step-up transformer and a voltage multiplier circuit would be added [5]. This paper presents one type of resonant converter called the Series Loaded Resonant (SLR) converter. Like in any other resonant converters, the SLR may also operate in either continuous or discontinuous conduction modes. References on the switching characteristics of each mode in SLR are plentiful. However, there seems to be minimum information on how each mode impacts converter's actual efficiency both over load and switching frequency operations.

This paper presents results of a study which investigated the efficiency performance of SLR when operated in its three different modes. To aid in the hardware, computer simulation was first performed whose results will be described. A lab scale SLR converter was then built and tested to assess the actual efficiency performance of SLR in the three different modes. Results of the hardware tests will be explained.

II. SLR DESIGN

Figure 1 illustrates the basic power stage of the SLR converter. The design of the SLR converter presented in this paper considered the main parameters such as resonant frequency, component stresses, and transistor losses were each considered in the design. For the hardware, the output power (<100W) and output voltage (15V) ratings were chosen to be low enough such that no transformer would be needed for the converter.

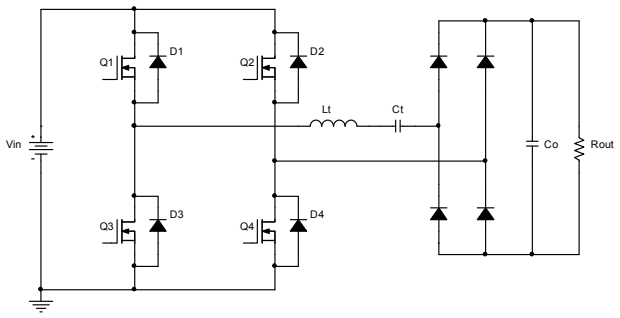

Figure 1.Power stage of SLR converter

The power MOSFETs Q1 through Q4 were chosen based on its low $R_{DS(on)}$ due to the large inductor peak current of the SLR. The MOSFETs used also have fast switching capability such that they can be switched reliably at 11.1 MHz. It was determined that a resonant frequency around 90 kHz would provide good testing ground considering that diode losses increase with operating frequency. The characteristic impedance of the resonant tank was chosen to be 50 Ohms. This would be high enough so that the tank current would not be too high, but low enough to allow enough current for the output. With the resonant frequency and characteristic impedance chosen, the values of the resonant components can be calculated using $\omega_o = 1/\sqrt{LC}$, and $Z_o = \sqrt{L/C}$.

$$C = \frac{1}{\omega_0 Z_0} = \frac{1}{2\pi \cdot 90kHz \cdot 50\Omega} = 35.4nF \tag{1}$$

$$L = \frac{1}{C\omega_0^{\,2}} = \frac{1}{33nF \cdot (2\pi \cdot 90kHz)^2} = 94.7\mu H \tag{2}$$

In order to determine peak values for the resonant current and voltage, two equations for resonant circuits are needed. The equations for inductor current and capacitor voltage in an undamped series resonant circuit are:

$$i_L(t) = I_{L0}\cos\omega_0 t + \frac{V_d - V_{c0}}{Z_0}\sin\omega_0 t \tag{3}$$

$$v_c(t) = V_d - (V_d - V_{c0})\cos\omega_0 t + Z_0 I_{L0}\sin\omega_0 t \tag{4}$$

where I_{L0} is the initial inductor current, V_{C0} is the initial capacitor voltage, and V_d is the source voltage. To find the maximum resonant inductor current and capacitor voltage:

$$i_L(t) = (0)\cos\omega_0 t + \frac{30-(-2V_0)}{53\Omega}\sin\omega_0 t = 1.13A \tag{5}$$

$$v_c(t) = 30 - (30-(-30))\cos\omega_0 t = 90V \tag{6}$$

A large core was used for the inductor, which was wound with AWG 16 solid copper wire. Large core and thick wire were used to reduce both copper and core losses. Ceramic multilayered capacitors were chosen for use in the design since they typically have a low equivalent series resistance (ESR) value and, therefore, fewer losses.

Each of the three types of diodes was a standard TO-220 package. The choice in package was made to ensure that parasitic capacitances and thermal properties would be similar for all diodes. Since the diodes were required to handle the full supply voltage, their blocking ability had to be rated for at least 30V. The maximum peak current they were required to handle was 1.13A, the same as the maximum peak current through the inductor. The maximum average current would depend on how long each diode was turned on in a given cycle. In the worst case scenario, a given diode would be operating at a 25% duty cycle. With the current assumed to be sinusoidal, the maximum average diode current was:

$$\bar{I} = \frac{1}{T}\int_0^{0.25T} 1.13\sin\left(\frac{2\pi}{T}t\right)dt = 180mA \tag{7}$$

The DC output voltage of the SLR converter cannot exceed the input voltage. Hence, the maximum peak forward voltage that the output rectifier diodes would need to handle is $V_{max} = \sqrt{2}V_d = 42\,\mathrm{V}$. The maximum peak current of these diodes is the same as the anti-parallel diodes, or 1.13A. However, maximum average current for the rectifier diodes would be doubled, since their duty cycle is 50%, as opposed to 25%.

III. COMPUTER SIMULATION

Following the design as described in the previous section, the SLR converter was simulated using Orcad PSpice. Figure 2 depicts the schematic used for the simulation incorporating those values calculated from the design.

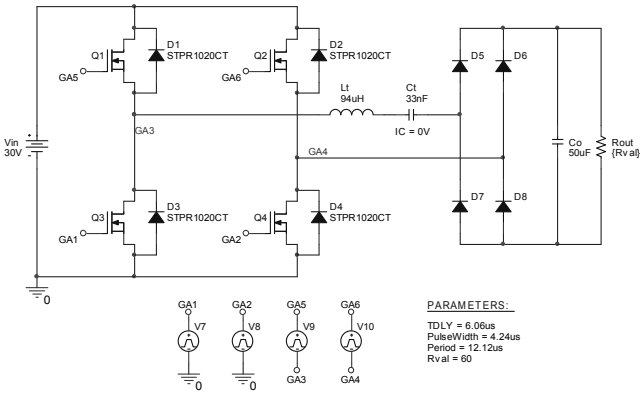

Figure 2. OrCAD schematic of SLR converter

The SLR converter model was carefully done in order to provide the most meaningful results. For example, the diode characteristics such as forward voltage drop, junction capacitance, reverse leakage, reverse breakdown voltage, and reverse recovery time were modified from the given values in their manufacturer's datasheets to simulate the real model of the diodes.

To simulate the converter in Discontinuous Conduction Mode (DCM), the frequency was set to 28.5 kHz. The

load resistance was 41.3 Ohms. The maximum resonant current obtained was 766 mA. For Continuous Conduction Mode below resonance (CCM 1), with fs = 56.5 kHz, the maximum resonant current obtained by simulation was 871 mA. In CCM 2 above resonance, with fs = 100 kHz, the maximum resonant current obtained by simulation was 1.1 A. Figures 3-5 show the inductor current waveforms for DCM, CCM 1, and CCM 2 respectively. As shown in Figure 3 that the resonant inductor current waveform is indeed discontinuous. The width of the discontinuity in the waveform is determined by the switching frequency of the converter. Figure 4 shows the same inductor waveform when the switching frequency is below resonant frequency. When comparing Figures 3, 4 and 5, it is evident that DCM waveform is the most distorted waveform (away from sinusoidal). This implies that the waveform contains the most harmonics compared to the other two modes. In turn, the larger harmonic content will cause more losses in the circuit in the form of more copper loss due to skin effect, and more core loss due to increased hysteresis and eddy current losses. Consequently, for the same output power, the DCM mode would suffer more copper and core loss and hence would impact the efficiency of the converter. Figure 6 shows an example of efficiency plot of the SLR converter in CCM 1 mode.

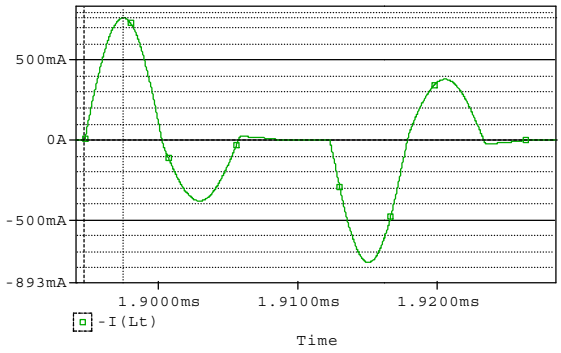

Figure 3. DCM inductor current waveform

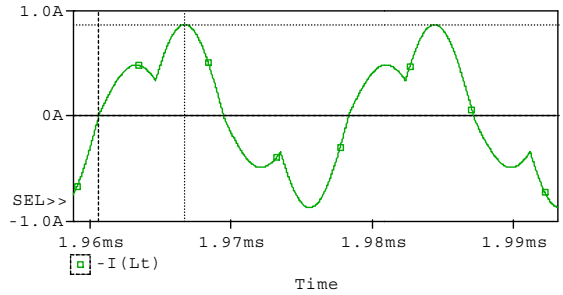

Figure 4. CCM 1 inductor current waveform

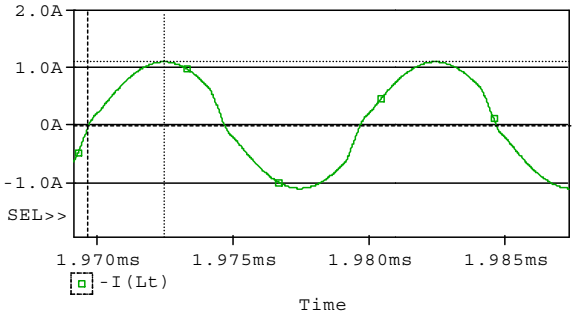

Figure 5. CCM 2 inductor current waveform

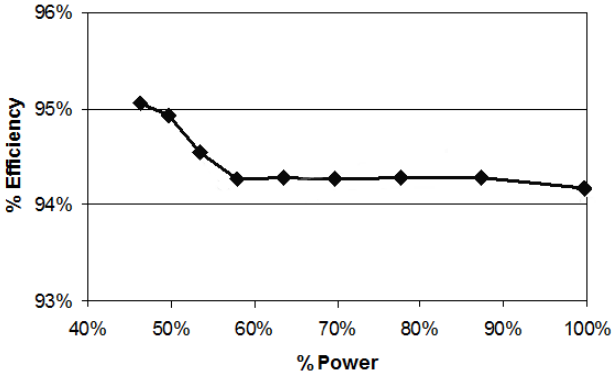

Figure 6. Efficiency of SLR in CCM 1 mode

IV. HARDWARE MEASUREMENTS

To assess the real impact of different operating modes on the SLR converter's efficiency, a lab scale SLR converter was built as shown in Figure 7. The switching frequencies were set to the same frequencies used in the simulations. As shown in Figure 7, the circuit is built on a prototype board with the different stages of the circuit labeled.

In DCM, CCM 1, and CCM 2 the maximum resonant currents were 0.672 A, 1.02 A, and 0.680 A, respectively. These waveforms are shown in Figures 8-10. When compared to Figures 3 to 5, we can see that, although there are differences in the peak values of the inductor current, the shape of the waveform in all three modes is in agreement with those obtained from simulation.

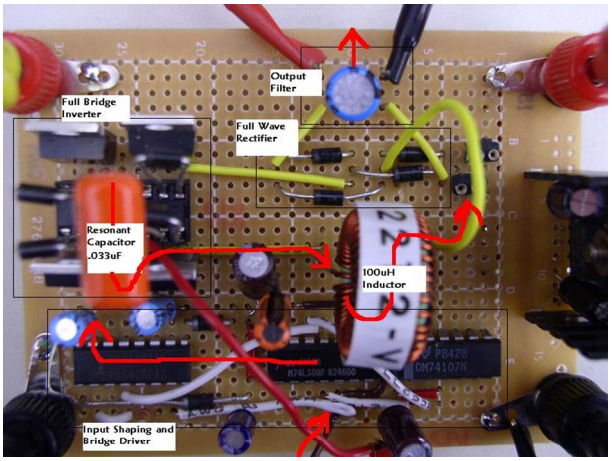

Figure 7. SLR converter circuit

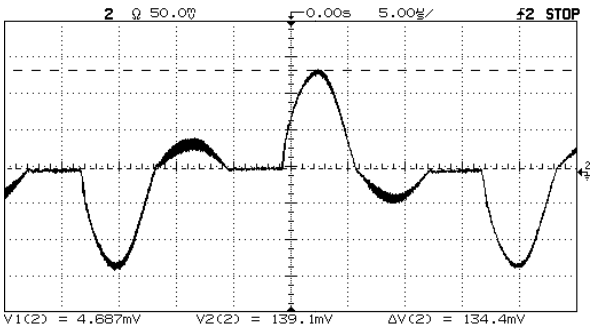

Figure 8. DCM inductor current waveform

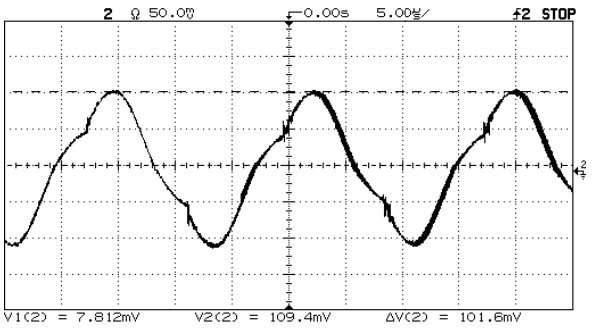

Figure 9. CCM 1 inductor current waveform

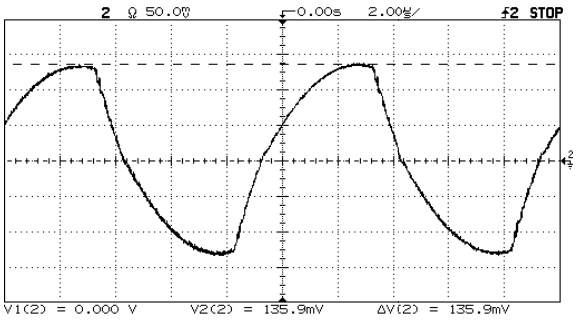

Figure 10. CCM 2 inductor current waveform

Next, the efficiency of the SLR converter was measured as a function of load resistance and frequency. The load resistance was varied while the output voltage was fixed. The switching frequency had to be continually adjusted to regulate the voltage. The input voltage was held at a constant 30V. In DCM, the load resistance was varied from 60 ohms at full load to 240 ohms at light load. In CCM 1, the load resistance was varied from 40 ohms to 80 ohms. In CCM 2, the load resistance was varied from 40 ohms to 100 ohms. The results are shown in Figure 11.

A frequency versus efficiency plot was also obtained from the performance data as shown in Figure 12. An efficiency trend was observed in each mode; however the curve is not a continuous one. This is because the converter efficiency typically declines as the output voltage is reduced and each mode was evaluated at a different output voltage. Also recall that the operating mode of the converter depends on the switching frequency used. So, the operating mode of the converter shifts from DCM to CCM 1 and to CCM 2 as the switching frequency is increased. Despite the discontinuity of the efficiency in Figure 12, nevertheless, meaningful information can still be obtained from this plot about diode performance at different frequencies.

From the two scenarios in measuring the efficiency, we can conclude that the DCM is indeed the mode that yields the lowest efficiency. As discussed previously, this is in agreement with the expectation that DCM contains the most harmonics which will degrade the efficiency.

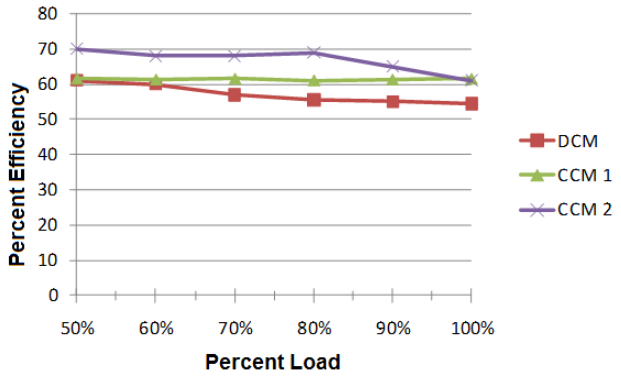

Figure 11. Percent efficiency as a function of load

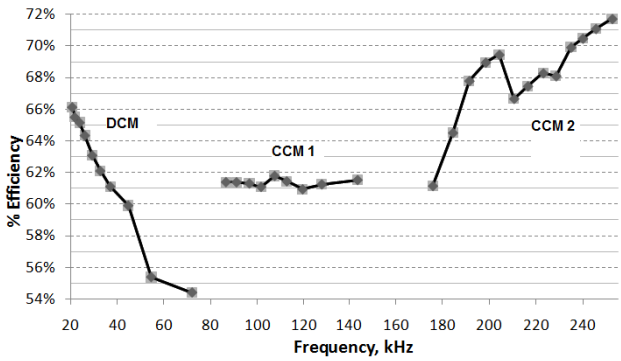

Figure 12. Percent efficiency for as a function of switching frequency

The maximum resonant current obtained in hardware varied slightly from the simulated results. In DCM, the simulated value approximated the actual result fairly accurately. However, in CCM 1 the simulated result was lower than the actual result. This is because the simulation and hardware have different resonant frequencies. In simulation, the resonant frequency is exactly 90 kHz. However, it was found that the actual resonant frequency is less than 90 kHz. The resonant current depends on the relationship between the switching frequency and the resonant frequency. Since the switching frequency in the simulation was further away from resonance than it was in hardware, it would be expected that the resonant current be lower in simulation. When observing CCM 2, the maximum resonant current was higher in simulation than in hardware. This is also due to a shift in the resonant frequency. Since the switching frequency in the simulation is closer in relation to resonance than in hardware, it is expected that the current would be lower in hardware. Another explanation for this is since although losses are modeled in PSpice, actual circuit losses due to switching are greater. The PSpice inductor and capacitor models do not include core losses or ESR which are emphasized at higher frequencies. Table 1 summarizes and compares the results obtained from simulation and from hardware measurements. The results from simulation and hardware show overall consistency and agreement from each other.

Table 1. Maximum Resonant Current Obtained from Simulation and Hardware

	DCM	CCM 1	CCM 2
Simulation	0.766 A	0.871 A	1.10 A
Hardware	0.672 A	1.02 A	0.680 A

V. CONCLUSION

In this paper, the efficiency performance of the SLR converter was investigated. The difference in converter efficiency was most noticeable in CCM 1, but even then most of the time it wasn't much more than a one percent difference. Although the efficiency measured was relatively low for a resonant converter, the efficiency data still correlates with one another. From the hardware results, it was observed that the efficiency of DCM was the lowest among the three conduction modes, both when load was varied and when the switching frequency was varied. This is in agreement with the fact that DCM produces the highest harmonics since its resonant current waveform is the most distorted among all three conduction modes. The higher harmonics then translates to increased losses in the converter due to skin effect and core loss. It is therefore expected that CCM 2, having the least distorted resonant waveform, turned out to be the most efficient among the three conduction modes.

An example of a follow up study is to conduct efficiency measurement where all three modes are operated at a same switching frequency. This consequently will have to be done by adjusting the resonant frequency of the converter. To maximize accuracy of the measurement, resonant frequency adjustment may be performed by adjusting the resonant capacitance value.

REFERENCES

[1] Masters, G., *Renewable and Efficient Electric Power Systems*, 1st Edition, Wiley-IEEE, 2004.

[2] Erickson, R.W. and Maksimovic, D., *Fundamentals of Power Electronics,* Springer, 2001.

[3] Johnson, S. D., Witulski, A. F., and Erickson, R.W., "Comparison of Resonant Topologies in High-Voltage DC applications", *IEEE Transaction on Aerospace and Electronic Systems*, Volume 24, Issue 3, Page(s): 263 – 274, May 1998.

[4] Kazimierczuk, M.K. and Czarkowski, D., *Resonant Power Converters*, Wiley-Interscience, April 1995.

[5] Nathan, B.V. and Ramanarayanan, V., "Analysis, simulation and design of series resonant converter for high voltage applications", *Proceedings of IEEE International Conference on Industrial Technology*, pp. 688-693, 2000.