2010 Seventh International Conference on Information Technology

Multiphase Interleaving Buck Converter With Input-Output Bypass Capacitor

Taufik Taufik, Randyco Prasetyo, Arief Hernadi
Electrical Engineering Departement
California Polytechnic State University
San Luis Obispo, California, USA
taufik@ieee.org

Dodi Garinto
Indonesian Power Electronics Center
Jakarta, Indonesia
dodi.g@ieee.org

***Abstract*—As the number of transistors in microprocessors increases per Moore's Law their power requirement increases accordingly. This poses design challenges for their power supply module especially when microprocessors operate at sub voltage range. This paper presents a new multiphase topology that addresses these challenges. Laboratory tests on a hardware prototype of the topology shows improved performance compared to a commercially available power supply module.**

***Keywords*—power electronics, voltage regulator modules**

I. INTRODUCTION

A voltage regulator module (VRM) is a dc-dc converter that provides the necessary power into a microprocessor. This converter can be either soldered on to the motherboard or it could be provided by a module attached to the board. Design specifications of VRMs are typically determined by microprocessor's manufacturers. For example, Intel has established design guidelines for VRM called Intel VRM11.0. Today's VRMs are based on a topology called the multiphase synchronous buck converter as shown in Figure 1 [1,2,3,4,5].

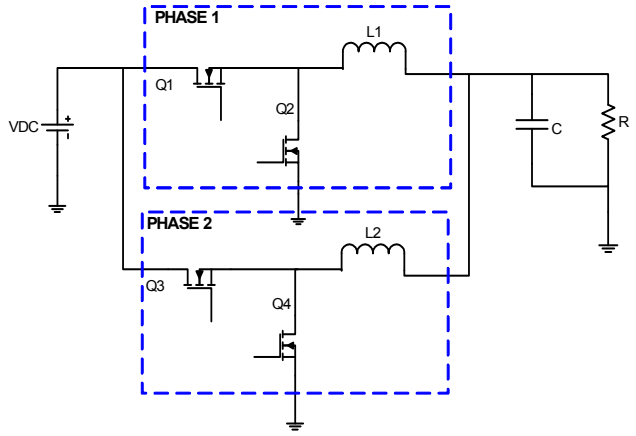

Figure 1. Multiphase synchronous buck topology

In the multiphase buck converter topology, one important operating parameter is called the duty cycle D. For buck converter, the ideal duty cycle is the ratio of the output voltage and input voltage. The basic multiphase buck converter worked very well in earlier VRMs where 5V was required at the input. However, as microprocessor technologies advances, new challenges in VRM design have arisen [6]. For example, today's microprocessors for desktop computers, workstations, and low-end servers, require VRMs to operate with 12V input. Laptops required VRMs to directly step down the battery charger voltage of 16-24V down to the microprocessor voltage of 1.5V. Future microprocessors are also expected to supply voltage to decrease below 1V in order to further reduce power dissipation [6]. This means that for these applications, the VRM and hence the multiphase buck converter will have to operate at very small duty cycles. The small duty cycle further translates into an increase in conduction loss of the multiphase buck converter which gets worsen as the required output power is increased [7].

Another challenge comes in the form of transient speed. Since further microprocessors call for fast operation, hence the VRM consequently is required to keep up with the speed. For dc-dc converters, this means the switching frequency has to be increased. However, when the switching frequency is increased, then more switching loss will occur at the top MOSFET as well as an increase in MOSFET's gate drive and body diode losses. Consequently, efficiency will drop to less than 80% when switching frequency is increased into multi-MHz [3].

Yet another challenge when designing today's VRMs would be the tradeoff between efficiency and transient response of the converter. In order to increase inductor current slew rate, a small inductance is required, but the small inductance also increases peak to peak current ripple; thus reducing the overall efficiency of the converter itself. This is true since an increase in the peak to peak current ripple translates to an increase in the top switch turn-off loss [7].

In this paper, a new multiphase buck topology that addresses the aforementioned technical challenges by utilizing storage components will be presented. A hardware prototype was built and tests were conducted to assess its performance.

978-0-7695-3984-3/10 $26.00 © 2010 IEEE
DOI 10.1109/ITNG.2010.97

II. THE PROPOSED MULTIPHASE BUCK CONVERTER

Figure 2 shows the proposed topology of multiphase buck converter. There are two major modifications from the basic multiphase. First, the topology comprises of cells each consisting of two buck converters. To operate the converter, a minimum of two cells will be required. Doing so will enable us to interleave individual bucks with proper sequencing of their control signals. For example, in the basic 4 phase multiphase buck converter, the control signal sequence is Phase 1, 3, 2, 4. In the proposed topology, the sequence is changed to Phase 1, 2, 3, 4 hence allowing the interleaving of buck converters to occur. This results in improved thermal distribution and hence less heat-sinking requirement and better efficiency.

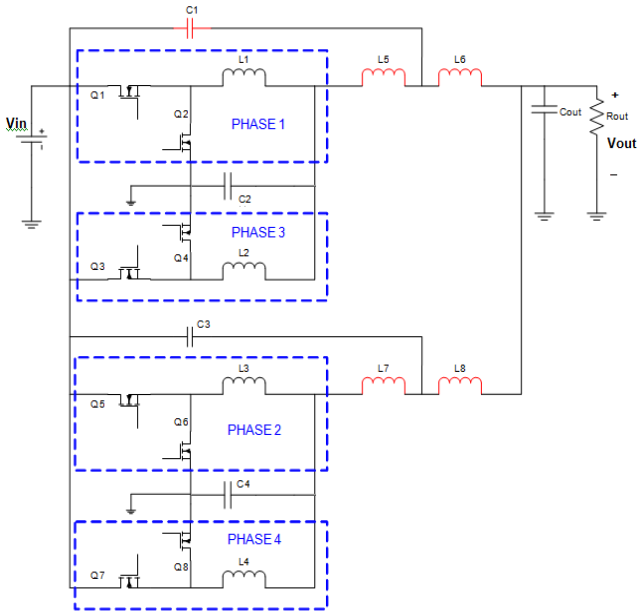

Figure 2. Proposed multiphase interleaved buck topology

Secondly, the proposed multiphase synchronous buck topology incorporates additional storage components that serve different purposes. For example, the additional output inductors (L5, L6, L7, L8) are placed to minimize output current ripple useful in reducing rms loss at the output capacitor (Cout) or from the copper loss of the inductors themselves, including from the main inductors (L1, L2, L3, L4). However, these inductors will consequently slow down the transient response which may be overcome by increasing the switching frequency of the converter, and by adding the input-output bypass capacitor in each cell (C1 and C3) for energy support required by the load during transient.

To illustrate interleaving operation, Figure 3 shows the timing diagram of control signals to the four bucks. In an N-phase multiphase, the duty cycle for each phase is equal to Vout/Vin and it is the same for all phases due to parallel configuration. A phase shift should therefore be implemented between the timing signals of the top switch from the first and second phases. The value of the phase shift follows the equation 360°/N where N is number of phases. For example, in the 2-phase case, the amount of phase shift will be 360°/2 = 180°.

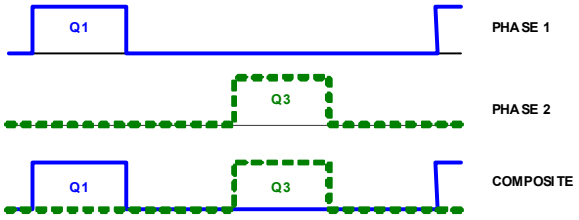

Figure 3. Timing diagram for Top MOSFETs

Figure 4 shows inductor current in each time segment from T_o to T_8. IL1 corresponds to inductor current flowing through inductor L1, IL2 through inductor L2, and so on, while Iout is the output current. The linear ramp-up of each inductor current signifies the charging of inductor, while linear ramp-down depicts the discharging of inductor. One advantage of multiphase is exhibited on the output current. Due to the ripple cancellation effect, the output current possesses 1/4 of the peak to peak ripple and 4 times the frequency of main inductor current. These provide the benefits of reducing rms loss, fast transient time, and small output filtering requirement.

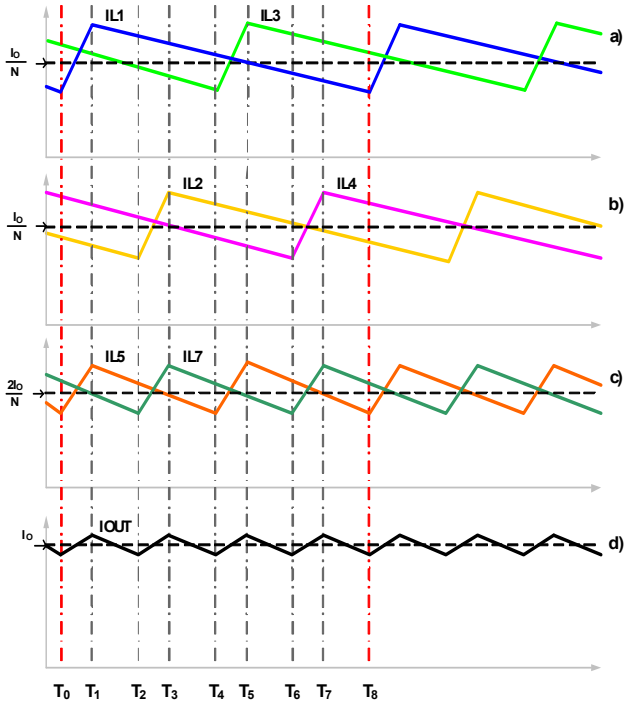

Figure 4. Inductor currents for phases (a) 1&3, (b) phases 2&4, (c) auxiliary inductor currents, and (d) output current

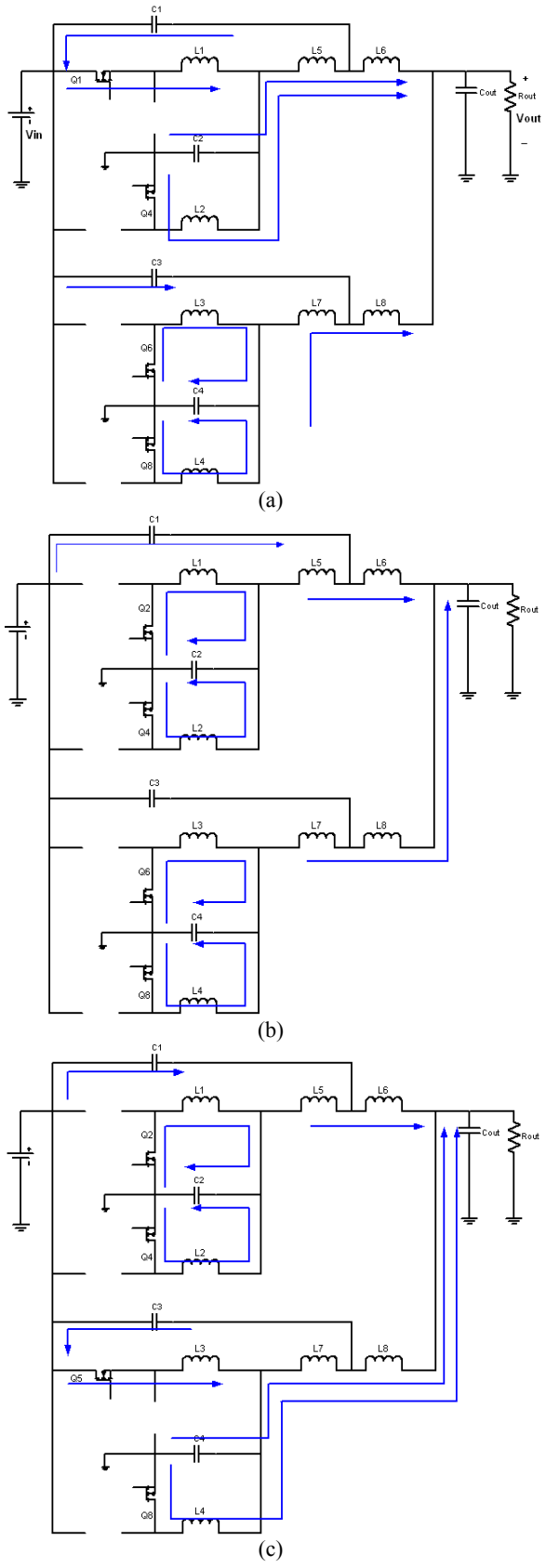

Figure 5. Energy flow during time (a) T_o–T_1, (b) T_1–T_2, and (c) T_2–T_3

Referring to times T_o to T_8 as shown in Figure 4, during interval T_o to T_1, Q1 turns on. As illustrated in Figure 5(a), current flows from Vin to output through Q1, L1, L5 and L6. In this case the current through L1, L5, and L6 increases linearly since the input and output voltages are both fixed at Vin and Vout respectively. At the same time, energy stored in C1 is being discharged through Q1 and L1, while the energy stored in C2 is also being discharged through L5 and L6. Meanwhile, L2 is also discharged through L5 and L6.

At time T_1 switch Q1 is turned off, and switch Q2 is turned on as illustrated in Figure 5(b). During T_1 to T_2, the energy stored in L1 together with energy left in L2 is now being used to charge C2. Energy stored previously in L5 and L6 flows to output. The energy in C1 would be charged by the input during this time.

The next transition from T_2 to T_3 is depicted in Figure 5(c). Switch Q5 is turned on, and the same sequence of energy flow occurs as the one described in the first phase (from T_o to T_2). Here, C3 replaces C1, C4 replaces C2, L3 replaces L1, L7 replaces L5, and L8 replaces L6. The same cycle will also repeat for phase 3 (Q3 and Q4) and phase 4 (Q7 and Q8)

III. HARDWARE PROTOTYPE AND TEST RESULTS

To test the actual performance of the proposed topology, a hardware prototype was designed and built with the design requirements shown in Table 1.

Table 1. Design requirements for the proposed converter

Parameter	Requirements
Nominal Input Voltage	12 V
Nominal Output Voltage	1 V
Maximum output current	40 A
Inductor ripple current	10 % of Maximum Phase Current
Output Voltage Ripple	< 15 mV_{p-p}
Switching Frequency	500 kHz per phase
Load Regulation	< 2 %
Line Regulation	< 5 %
Efficiency	> 80 % at Full Load

Based on these design requirements, each component in the proposed was selected. In addition, loss analysis was also performed over load variations. Table 2 summarizes components that contribute to major losses in the proposed multiphase buck topology calculated at full load condition.

Table 2. Power Loss on each device at 40 A Load Current

Components	Power Loss (W)
Input Capacitor	0.222
Top MOSFET	1.164
Bottom MOSFET	3.412
Main Inductor	1.252
Auxiliary Inductor	0.272

Figure 6 shows the final hardware prototype of a 4 phase version of the proposed topology. Each phase is running at 500 kHz switching frequency which makes both input and output components to have frequency component of 4 x 500 kHz = 2 MHz. The prototype was done on a multi-layer pcb, approximately 2.5 in. x 2.5 in. The top layer was dedicated for all the controller chips while the bottom layer was used specifically for the power components (inductors, MOSFETs). Laboratory tests were then conducted on the prototype to assess its performance on several standard dc-dc operating parameters. Results were then compared to those obtained from a commercially available VRM.

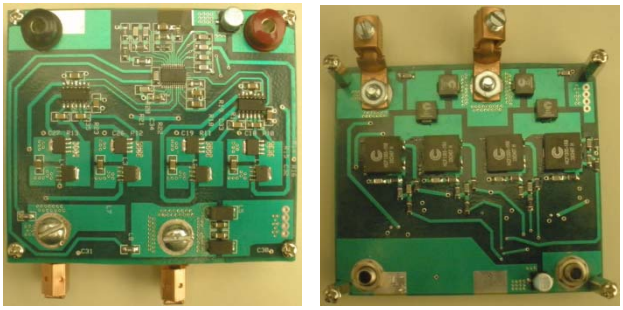

Figure 6. Hardware prototype of the proposed converter (a) top layer (b) bottom layer

First, the output voltage ripple was observed to be approximately 8.2mV at full load, see Figure 7. This peak to peak ripple is considerably less compared to that of the commercially available VRMs (typically 40-50mV). However, the output voltage of the proposed converter appears to have so much high frequency noise on top its actual peak to peak ripple. This may be explained by the fact that the frequency component of the output voltage is relatively high at 2 MHz (4 x 500 kHz). Hence, a better layout and/or filtering will be necessary to suppress this high frequency noise.

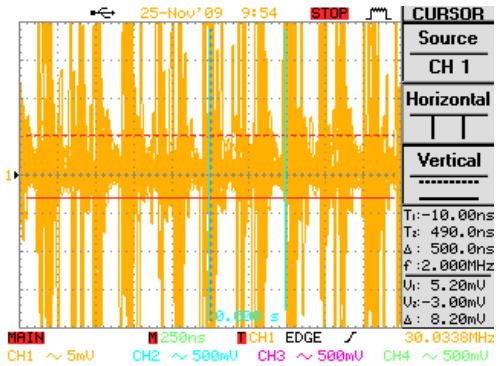

Figure 7. Output voltage ripple at full load

Next, load transient tests were performed to see how fast the proposed converter recovers upon a step change in the load. Figure 8 shows both step up and step down responses of the converter in terms of its output voltage.

The step up and step down responses as shown in Figure 8 were measured to be 136 us and 160 us respectively. This is comparable to the 150 us step responses measured in the commercially available VRM.

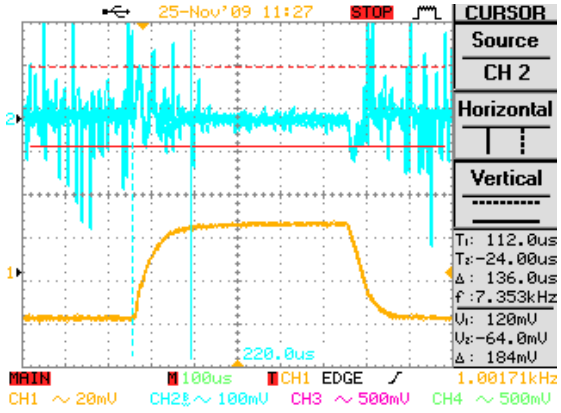

Figure 8. Step changes in load current (bottom) and the responses on the output voltage (top)

Table 3 lists results of measurements taken when the load was increased by 10% steps. The data were then used to calculate both load and line regulations as follows:

$$\text{Line Regulation} = \frac{V_{OUT(High\ Input)} - V_{OUT(Low\ Input)}}{V_{OUT(nominal)}} x\,100\% = \frac{1.006\,V - 1.006\,V}{1.006} x\,100\% = 0\%$$

$$\text{Load Regulation} = \frac{V_{OUT(No\ Load)} - V_{OUT(Full)}}{V_{OUT(Full)}} x\,100\% = \frac{1.006\,V - 1.006\,V}{1.006} x\,100\% = 0\%$$

When compared against the commercially available VRM, the proposed topology has a comparable line regulation (close to 0%) but it is superior in its load regulation (close to 0% as compared to 0.8%).

Table 3. Power Loss on each device at 40 A Load Current

Load (%)	Vin(V)	Iin(A)	Pin(W)	Vout(V)	Iout(A)	Pout(W)	Efficiency (%)
0	12.006	0.267	3.210	1.006	0.01	0.010	0.31
10	12.006	0.731	8.773	1.006	5	5.030	57.34
20	12.007	1.186	14.235	1.006	10	10.060	70.67
30	12.006	1.648	19.786	1.006	15	15.090	76.27
40	12.004	2.119	25.430	1.006	20	20.120	79.12
50	12.003	2.599	31.191	1.006	25	25.150	80.63
60	11.992	3.092	37.077	1.006	30	30.180	81.40
70	12.004	3.593	43.132	1.006	35	35.210	81.63
80	12.004	4.110	49.338	1.006	40	40.240	81.56
90	11.996	4.644	55.706	1.006	45	45.270	81.27
100	**12.004**	**5.189**	**62.294**	**1.006**	**50**	**50.300**	**80.75**

Finally, from Table 3 the efficiency plot of the proposed converter was generated as shown in Figure 9.

At full load, the efficiency of the proposed converter (80.75%) is slightly larger than that measured from the commercially available VRM (80%).

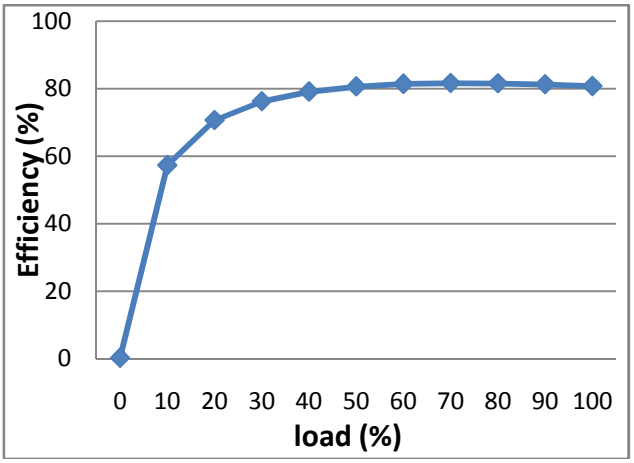

Figure 9. Efficiency of the proposed converter

IV. CONCLUSION

With the increasing demand for power in today's microprocessors, the design of VRM will become more challenging than ever before. Conventional or basic topology used in most commercially available VRMs will not be sufficient to satisfy the thirst of power and speed of today's and future microprocessors. The proposed topology presented in this paper is aimed to address this issue. Lab measurements on a hardware prototype of the proposed converter show promising results of its potential. Although the results are overall comparable to those obtained from a commercially available VRM, two particular results are worth noting. First, load regulation of the proposed converter was measured to be practically 0% which is a significant improvement from the one measured on the commercially available VRM. Load regulation becomes even crucial when output current is much higher than the 40A that was tested on this prototype. Thus, from this aspect, the proposed converter has shown its great potential for use in a very high output current applications with very tight load regulation such as those expected in future microprocessors.

Secondly, the efficiency plot of the proposed converter was actually sloping down gradually after the full load. This is much different from that measured on the commercially available VRM in which the efficiency dives down relatively faster. This means, again for much higher output current applications such as those expected in future microprocessors, the proposed converter exhibits a great potential for use in future VRMs.

REFERENCES

[1]. X. Zhou, X. Zhang, J. Liu, P. Wong, J. Chen, H. Wu, L. Amoroso, F. C. Lee, and D. Chen, "Investigation of Candidate VRM Topologies for Future Microprocessors", IEEE Transactions on Power Electronics, Volume 15, Issue 6, Nov 2000 Page(s):1172 – 1182.

[2]. X. Zhou, P. Xu, and F.C. Lee, "A High Power Density, High Frequency and Fast Transient Voltage Regulator Module with a Novel Current Sharing and Current Sharing Technique", Proceedings of IEEE APEC, 1999.

[3]. Y. Panov, M. Jovanovic, "Design considerations for 12-V/1.5-V, 50-A voltage regulator modules". IEEE Transaction on Power Electronics, Volume 16, Issue 6, Nov. 2001 Page(s):776 – 783.

[4]. P. Xu, X. Zhou, P. Wong, K. Yao, and F.C. Lee, "Design and Performance Evaluation of Multi-Channel Interleaving Quasi-Square-Wave Buck Voltage regulator Module", Proceedings of HFPC, 2000, pp. 82-88.

[5]. R. Miftakhutdinov, "Optimal Design of Interleaved Synchronous Buck Converter at High Slew-Rate Load Current Transients", Proceedings of Power Electronics Specialists Conference, 2001, Volume 3, June 2001 Page(s):1714 – 1718.

[6]. Intel Corporation, Intel Technology Symposium, September 2001, Seattle, WA.

[7]. D. Garinto, "A Novel Multiphase Multi-Interleaving Buck Converters for Future Microprocessors", Power Electronics & Motion Control Conference, Aug. 2006, Page(s):82–87.