Frequency dependent I/Q imbalance in real I/Q filter pairs compensation may be performed using a simple compensation module, placed in the receiver/transmitter chain, with a gain adjustment coefficient and a delay adjustment coefficient. The gain adjustment coefficient may be determined by amplitude measurements conducted at a selected frequency near the center of the band-pass region of the filters. The delay adjustment coefficient may be determined by phase measurements conducted at a selected frequency near the edge of the band-pass region of the filters. Statistical analysis may be used to determine types of real filters that are better suited for the compensation method and to select the test frequencies that should be used.
FIG. 1

MIXER/LOs IQ ERROR MODEL

LPFs IQ ERROR MODEL

ADCs IQ ERROR MODEL
FIG. 4

\[ A_{\text{leak}} = \begin{bmatrix} 1 & 0 \\ \delta G \sin \delta P & \delta G \cos \delta P \end{bmatrix} \]

\[ A_{\text{corr}} = \begin{bmatrix} 1 & 0 \\ -\tan \hat{\delta}P & \frac{1}{\delta G \cos \hat{\delta}P} \end{bmatrix} = A_{\text{leak}}^{-1} \]
FIG. 5

DIGITAL COMPENSATION

DIGITAL COMPENSATION MODULE

FFT (P/O DSP)
FIG. 7

MODE CONTROLLER (TEST)

TEST SIGNAL GENERATOR
1st FREQ. 2nd FREQ.

LPF ADC

COMPENSATION PARAMETER DETERMINATION MEANS

TEST OUTPUT MEASUREMENT MEANS

FFT (P/O DSP)
FIG. 8

- MODE CONTROLLER (OPERATE)
- TEST SIGNAL GENERATOR
  - 1st FREQ.
  - 2nd FREQ.
- TEST OUTPUTMEANS
- PARAMETER MEASUREMENT
- FFT (P/O DSP)
- COMPENSATION PARAMETER DETERMINATION MEANS
- TEST OUTPUT MEASUREMENT MEANS
FIG. 9

MIXER/LO BLOCK

ADC

FFT (P/O DSP)

TEST OUTPUT MEASUREMENT MEANS

COMPENSATION PARAMETER DETERMINATION MEANS

Mixer/LO Block

l01 I

l02 Q

ADC

ADC

LPF

DAC

LPF

DAC

MODE CONTROLLER (TEST)

TEST SIGNAL GENERATOR

3rd FREQ.

4th FREQ.
FIG. 11

- Diagram shows a graph with points labeled as follows:
  - $x[n-1]$ at $n-1$
  - $x[n]$ at $n$
  - $x[n+1]$ at $n+1$
  - $x_p[n]$ at $n$

- Diagram includes blocks labeled with:
  - $\frac{\delta P}{\omega_p}$
  - $sgn \{ \delta P \}$
  - $\frac{\delta P}{\omega_p T_s}$
  - $\frac{1}{\delta G}$

- Variables and annotations include:
  - $x_1$
  - $x_2$
  - $x_{p1}$
  - $x_{g2}$
FIG. 12

1200

RECEIVER FILTER PAIR I/Q IMBALANCE
COMPENSATION METHOD

1210

GENERATE/INJECT TEST SIGNAL(S)

1220

MEASURE RESPONSE

1230

determine compensation module values

1240

USE DETERMINED COMPENSATION VALUES TO
COMPENSATE FOR I/Q IMBALANCE

1250

RETURN TO NORMAL OPERATION
**FIG. 13**

TRANSMITTER FILTER PAIR I/Q IMBALANCE COMPENSATION METHOD

- GENERATE/INJECT TEST SIGNAL(S)

- MEASURE RESPONSE

- DETERMINE COMPENSATION MODULE VALUES

- USE DETERMINED COMPENSATION VALUES TO COMPENSATE FOR I/Q IMBALANCE

RETURN TO NORMAL OPERATION
FIG. 14

BUTTERWORTH CASCADE

CHEBYSHEV CASCADE

BUTTERWORTH LADDER

CHEBYSHEV LADDER

MEDIAN IMP [dB]

FREQUENCY [Hz]

MEDIAN IMP [dB]

FREQUENCY [Hz]
FIG. 15

BUTTERWORTH CASCADE

CHEBYSHEV CASCADE

BUTTERWORTH LADDER

CHEBYSHEV LADDER

YIELD [%]

IMR [dB]
FIG. 16

- Butterworth Cascade
- Chebyshev Cascade
- Butterworth Ladder
- Chebyshev Ladder

Estimation Error [deg]
Estimation Frequency [Hz]

x10⁷
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FIG. 17
FIG. 18

A graph showing the relationship between frequency (MHz) and the phase shift (dP) under different conditions.

- dP (phase)
- τ1 (8 MHz)
- τ2 (7 MHz)
I/Q COMPENSATION OF FREQUENCY DEPENDENT RESPONSE MISMATCH IN A PAIR OF ANALOG LOW-PASS FILTERS

FIELD OF THE INVENTION

The present invention concerns compensation of matched two-path real filter pairs. More specifically, the present invention concerns (I/Q) compensation of frequency dependent response mismatch for a pair of analog (low) pass filters.

BACKGROUND

Multiple channels of data can share a single transmission medium, but a receiver may desire data from one channel. Therefore, to isolate the desired channel for processing, transceivers typically perform at least three operations on the received signal: (1) the undesired channels are filtered out; (2) the desired channel is "shifted" to dc, where it can be processed; and (3) the signal is amplified. The order of the operations depends on the design of the transceiver. Shifting a signal may be accomplished by mixing the signal with a local oscillator signal.

In superheterodyne transceivers, the input signal (e.g., a Radio Frequency ("RF") signal) is amplified and filtered. Then, the filtered RF signal is shifted to an intermediate frequency ("IF") where it is passed through a highly selective bandpass filter. The bandpass filtered signal is then amplified and digitized. The digitized signal is then processed in the digital domain.

Direct conversion transceivers use techniques to avoid having to use an IF, thereby saving power, cost and allowing for a smaller physical design for some applications (e.g., mobile communications devices). A part of an exemplary direct conversion (zero-IF) receiver 100 is illustrated in FIG. 1. The receiver 100 includes an antenna (A) 102, a low-noise amplifier (LNA) 104, two mixers 106, 108, two real low-pass filters (LPFs) 110, 112, two analog-to-digital converters (ADCs) 114, 116, and a Fast Fourier Transform (FFT) module 118. The FFT module 118 may be included, e.g., as part of an exemplary Orthogonal Frequency Division Multiplexer (OFDM) Digital Signal Processor (DSP), used in the application of 802.11a, 802.11g or another OFDM standard.

Antenna 102 receives signal, x_A, which is input to the LPF 110. LNA 104 amplifies signal, x_LNA, and outputs signal, x_LNA. Signal, x_LNA, is input in parallel to each of the mixers 106, 108. Mixer 106 mixes signal, x_LNA, with local oscillator signal, x_LO1, "(I)" and outputs signal, x_I1. Mixer 108 mixes signal, x_LNA, with local oscillator signal, x_LO2, "(Q)" and outputs signal, x_Q1. The two local oscillator signals, x_LO1, "(I)" and x_LO2, "(Q)" are quadrature related (separated in phase by 90°). Signal, x_I1, is filtered by low-pass filter 110, outputting filtered signal, y_I. Signal, y_Q, is filtered by low-pass filter 112, outputting filtered signal, y_Q. Filtered signals, y_I, y_Q, are input to ADCs 114, 116, respectively, which sample the analog filtered signals, y_I, y_Q, at a sampling frequency, f_s. The digital outputs from ADCs 114, 116 are input to FFT 118 which processes and reforms the transmitted signal in the digital domain.

An exemplary zero-IF transmitter (TX) chain 200 is shown in FIG. 2. Transmitter (TX) chain 200 starts with a DSP 202, followed by a pair of digital-to-analog converters (DACs) 204, 206, a pair of LPFs 208, 210, a mixer/LO block 212, a power amplifier (PA) 214, and an antenna 216. DSP 202 generates and outputs pairs of digital quadrature signals, which are input to the DACs 204, 206. The DACs 204, 206 operate at a sample rate, f_s, converting the digital quadrature signals to analog quadrature signals. The analog quadrature signals are input to the pair of real low pass filters 208, 210. The real low pass filter pair 208, 210 filter the analog signals, and the filtered analog signals are input to the mixer/LO block 212. Mixer/LO block 212 mixes the input signal with x_LO1, "(I)" and x_LO2, "(Q)" and combines the two mixed signals. The output from mixer/LO block 212 is fed to a power amplifier 214, which amplifies the signal prior to transmission over antenna 216.

The two quadrature paths (I path and Q path), corresponding to the I and Q local oscillator signals, allow the direct conversion receiver/transmitter to avoid having to use an IF. Unfortunately, the characteristics of direct conversion receivers, transmitters, and transceivers are not ideal. I/Q mismatch (sometimes referred to as I/Q errors) causes I/Q imbalance (sometimes referred to as I/Q leakage). I/Q imbalance in receivers, transmitters, and transceivers, an area of concern to the present invention, shall now be described.

Main contributors of the RX 100 chain's (FIG. 1) I/Q imbalance are the gain error (6G1) 105 of the mixers 106, 108, the phase error (6P1) 107 in the local oscillator signals, the gain error (6G2(o)) 109 and phase (6P2(o)) 111 mismatch between the LPF's (208, 210) transfer functions, and the gain error (6G3) 115 between the ADCs (114, 116).

Slight differences in the components of the mixers 106, 108 may contribute to the gain error (6G1) 105. Slight differences in the I/Q relationship of the x_LO1 and x_LO2, and the I and Q signals that are not exactly in quadrature may cause phase error (6P1) 107. Component mismatches between filters 110, 112 may cause the gain (6G2(o)) 109 and phase (6P2(o)) 111 errors. If the components of filters 110, 112 are not perfectly matched, the transfer functions do not match (H1(o) ≠ H2(o)), where H1(o) represents the transfer function for LPF 110 and H2(o) represents the transfer function for LPF 112) then a non-zero transfer function H3(o), contributes to a leaked undesired or difference output component. Even when the filters are fabricated at the same time and on the same integrated chip, component mismatch of 0.2% to 0.5% or even larger may still occur. A parallel model of an imperfect low-pass filtering operation is illustrated in FIG. 3. The top branch represents the common component, h_m, of H1(o) and H2(o), which produces the desired output. The bottom branch represents the difference component, h_d, between H1(o) and H2(o), which produces the leaked signal. Returning to FIG. 1, slight differences in the components of the ADCs 114, 116 may contribute to the gain error (6G3) 115.

The I/Q imbalance contribution of gain and phase errors can be modeled as a two-input two-output linear network with some inter-coupling coefficients. These simple models can be individually applied to each block of mixers/LO, LPFs and ADCs, as shown in error model representations 120, 122, and 124, respectively of FIG. 1. Note that the LPF error model representation coefficients are a function of frequency, which significantly complicates the modeling and compensation.

Main contributors of the TX 200 chain's (FIG. 2) I/Q imbalance are the gain error (6G1) 211 of the mixer/LO block 212, the phase error (6P1) 213 in the local oscillator signals, the gain (6G2(o)) 207 and phase (6P2(o)) 209 mismatch between the LPF's (208, 210) transfer functions, and the gain error (6G3) 205 between the digital-to-analog data converters (204, 206). The I/Q imbalance contribution of gain and phase errors can be modeled as a two-input two-output linear network with some inter-coupling coefficients. These simple models can be individually applied to each block of mixers/LO, LPFs and ADCs, as shown in error model representations 218, 220, and 222, respectively of FIG. 2. Note that the LPF error model representation coefficients are a function of frequency, which significantly complicates the modeling and compensation.
FIG. 4 illustrates the concepts of leakage and compensation which may be applied to I/Q receivers, transmitters and transceivers using two-input two-output leakage and correction models.

In mathematical terms, a leakage stage 404 may be described as:

\[ y = A_{\text{leak}} x \]

where \( y = [y_1, y_2]^T \) (output), \( x = [x_1, x_2]^T \) (input) and \( A_{\text{leak}} \) (model) are given in FIG. 4. The resulting image rejection ratio (IMR) corresponding to the leakage stage 404 can be calculated by:

\[ \text{IMR} = 10 \log_{10} \left| \frac{1 + |G_2|^2 + 2|G_2| \cos(P)}{1 + |G_2|^2 + 2|G_2| \cos(P)} \right| [\text{dB}] \]

The concept of IMR shall now be described. An imperfect quadrature signal can be modeled in the phase domain as two rotating phasors with \( \omega_0 \) angular frequency by \((n/2-\phi)\) apart, and with \( A_I \) and \( A_Q \) magnitudes. The frequency domain representation of this two-path signal contains a desired component at \( \omega_0 \) and a leakage (undesired) component at \( -\omega_0 \). The image rejection ratio (IMR) may be used as a representation for the degree of I/Q imbalance. The IMR would be infinitely large (desirable) if the gain imbalance \( y = A_I/A_Q \) was unity and the phase imbalance \( \phi \) was zero; such an IMR (corresponding to leakage stage 404) would be represented in the \( A_{\text{leak}} \) model representation with \( 6G^I \) and \( 6P = 0 \).

The concept of I/Q imbalance compensation is straightforward: whatever “leaks” due to I/Q mismatch can be cancelled by deliberately “leaking back” the same amount. To compensate for this I/Q leakage, first, the coefficients of the error matrix \( A_{\text{corr}} \) should be estimated using off-line or on-line estimation methods. Off-line estimation methods refer to test methods conducted while normal operation of the receiver/transmitter is not in progress, e.g., normal operations have been suspended to inject test signals into the LPF pair and measure the response of those test signals. On-line estimation methods refer to estimation methods which may be conducted during normal receiver/transmitter operation, without suspending the receiver/transmitter normal functions.

Some known off-line estimation methods use sets of one or multiple test frequencies (tones) sent simultaneously into the I/Q chain; measurements are performed by the DSP (FFT) block at the output. Due to the frequency dependency of the LPFs, testing in these known methods is performed over a large number of sets of frequencies (tones) to determine the error matrix \( A_{\text{leak}} \). Other known compensation methods use test-signal based adaptive tuning algorithms, e.g., where testing is repeated iteratively and the \( A_{\text{leak}} \) may be gradually adjusted and allowed to converge over time. Examples of known on-line estimation methods are included in the following references:

5. X. J. Tao, “Frequency dependent I/Q calibration,” Technical memorandum, Agere Systems, (Oct. 9, 2001); and

Still other known compensation methods which avoid training (test) signals use blind, on-line adaptive methods to estimate and correct the I/Q imbalance. Examples of known on-line estimation methods are included in the following references:


Once \( A_{\text{leak}} \) is estimated, a correction matrix \( A_{\text{corr}} \) can be found by:

\[ A_{\text{corr}} = A_{\text{leak}}^{-1} \]

The correction matrix \( A_{\text{corr}} \) may be used to cancel the I/Q leakage. The concept of I/Q leakage compensation is illustrated in FIG. 4 with respect to a single input frequency. Signal \( X_0 \) (shown in the frequency domain) including no I/Q mismatch (no component at \( -\omega_0 \)), is input to an I/Q leakage stage 404. The leakage stage 404 has transfer function \( A_{\text{leak}} \). The output of leakage stage 404 is an uncorrected signal \( Y_0 \). Signal \( Y_0 \) includes a desirable component at \( \omega_0 \) and an undesirable (leakage) component at \( -\omega_0 \). Signal \( y_c \) is input to a correction stage 410 with transfer function \( A_{\text{corr}} \). The output from the correction stage 410 is signal \( Z_4 \). Since \( A_{\text{corr}} \) should be tunable and requires high precision, it is usually implemented in the digital domain. The amplitude of the component at \( -\omega_0 \), for compensated signal \( Z_4 \) has been reduced with respect to the corresponding component of the uncompensated signal \( Y_4 \). Due to imperfect error estimation and finite word-length digital correction, some residual I/Q mismatch (component at \( -\omega_0 \)) will remain in the corrected output \( Z_4 \).

Note that the above described I/Q imbalance compensation concept is valid for both receiver (RX) and transmitter (TX) applications. The RX implementation applies digital “corrections” or “compensation” following the I/Q leakage in the receiver \( A_{\text{leak}} \). The TX implementation applies digital “pre-distortion” to the digital signal before the signal is subjected to I/Q leakage in the transmitter circuitry \( A_{\text{leak}} \). The I/Q mismatch \( (6G_2(\omega) \text{ and } 6P(\omega)) \) of the filters is frequency dependent, while the I/Q mismatch of the front-end \( (6G_1 \text{ and } 6P_1) \) and the ADCs and/or DACs \( (6G_c) \) can be considered frequency independent in first order. Therefore, the error matrix \( A_{\text{leak}}(\omega) \) should be estimated for several frequencies. Thus, the implementation of the correction matrix \( A_{\text{corr}}(\omega) \) becomes costly since it should be effective over the whole band of frequencies of interest. Known fre-
frequency-dependent \( I/Q \) estimation/correction methods treat the zero-IF filters as a black box.

Some known methods (previously referenced) to determine the characteristics of this "black box" require the insertion of an extensive range of test signals obtaining measurements over a large number of frequencies. Then elaborate correction models with numerous modeling variables are determined and implemented. The incorporation of elaborate testing circuitry and elaborate correction circuitry (e.g., sometimes including 1,000 to 100,000 or more gates) may consume significant power, may occupy a significant amount of limited circuit board space available, and may add significant cost to the device. In many low cost, limited power, miniature size applications (e.g., hand-held mobile battery operated communication devices) such test signaling and correction circuitry is highly undesirable. In addition, the use of significant amounts of time required to conduct the tests is also highly undesirable. For a battery operated mobile communications device, the time required to conduct the model characterization testing, drains valuable energy from the battery, limiting normal communications operating time. In some embodiments, the time required to obtain compensation module parameters is minimal.

In addition, since the measurements for compensation parameter determination may be obtained from one set of measurement frequency and a selected phase measurement frequency, is generated and inserted as a single input to both of the LPF paths. An output signal corresponding to each filter of the pair is measured for gain at the first frequency and for phase at the second frequency, e.g., using an FFT as part of a DSP. Relative data between the amplitude measurements of the two output signals at the first frequency, e.g., at the gain frequency, is used to determine the gain error estimate. Relative data between the phase measurements of the two output signals at the second frequency, e.g., the phase frequency, is used to determine the phase error estimate. Since the invention may use a common test signal input to both LPF paths and rely on relative data for compensation parameter determination, the test signal need not be precisely controlled in terms of exact amplitude and/or frequency. This accommodation of the invention to an imprecise test signal facilitates a simple and inexpensive test signal generation implementation. In addition, since the measurements for compensation parameter determination may be obtained from one set of output measurements from a single input signal, the off-line time required to obtain compensation module parameters is minimal.

In some embodiments of the invention, two single tone test signals are generated and applied at different times, e.g., a first signal at a selected gain measurement frequency and a selected phase measurement frequency, is generated and inserted as a single input to both of the LPF paths. An output signal corresponding to each filter of the pair is measured for gain at the first frequency and for phase at the second frequency, e.g., using an FFT as part of a DSP. Relative data between the amplitude measurements of the two output signals at the first frequency, e.g., at the gain frequency, is used to determine the gain error estimate. Relative data between the phase measurements of the two output signals at the second frequency, e.g., the phase frequency, is used to determine the phase error estimate. Since the invention may use a common test signal input to both LPF paths and rely on relative data for compensation parameter determination, the test signal need not be precisely controlled in terms of exact amplitude and/or frequency. This accommodation of the invention to an imprecise test signal facilitates a simple and inexpensive test signal generation implementation. In addition, since the measurements for compensation parameter determination may be obtained from one set of output measurements from a single input signal, the off-line time required to obtain compensation module parameters is minimal.

In some embodiments of the invention, two single tone test signals are generated and applied at different times, e.g., a first signal at a selected gain measurement frequency followed, e.g., almost immediately, by a second signal at a selected phase measurement frequency. The two signals, each occurring at different time with a different frequency may be thought of as a single composite signal.

In some embodiments, the compensation module values may be measured, determined, and loaded into the compensation module once, e.g., at the factory. Alternatively, or in addition, the compensation module values may be measured, determined and loaded into the compensation module once per power on cycle, e.g., at turn-on. In still other embodiments, the compensation module values may be measured, determined, and loaded into the compensation module periodically and/or multiple times during a turn-on cycle, e.g.,
once initially at turn-on and then periodically at opportunist times such as when the transmitter/receiver is not being used for communications.

In some embodiments in accordance with the invention, e.g., using transceivers, various components already available may be reused for the test signal generation, measurement, and/or determination. For example, when performing operations related to the compensation of the transmitter’s LPFs, the receiver’s ADCs may coupled to the output of the transmitter’s LPFs. The ADCs may be coupled to an existing DSP. The ADCs and DSP may then be used for output signal measurements. In such embodiments, the effect of the receiver’s ADCs, e.g., any I/Q path frequency independent gain imbalance, may be removed by performing a second set of measurements with the inputs to the ADCs switched. When performing operations related to the compensation of the receiver, one of the transmitter’s DACs may be used to generate an analog test signal.

In some embodiments in accordance with the invention, the gain error estimate used in the compensation module is a constant gain value set to the gain estimation test frequency at the single gain test frequency. In some embodiments, the gain factor in the compensation module may be 1/δG(f_p), where δG(f_p) is the determined estimated gain error at selected gain measurement test frequency f_p. The delay error estimate (a time delay) used in the compensation module may be a constant with respect to frequency. The delay error estimate may be determined using the determined phase error estimate value at one test frequency if it is assumed that the phase changes linearly with frequency. In some embodiments, the delay error estimate is determined using the equation:

r ≈ (δG(f_p)) (2πf_p) (δG(f_p)),

where δG(f_p) is the determined estimated phase delay at selected phase measurement test frequency f_p. The compensation module of the present invention lends itself to simple digital design implementations, and may have a digital design implementation.

Different types of LPFs, e.g., those filters that have a relatively constant gain over the intended bandwidth and have a relatively linear phase error over the intended bandwidth, may be better suited for use with the compensation module of the present invention. Statistical analysis may be used to determine types of real filters that are better suited for the compensation method of the present invention and to select the test frequencies that should be used. Median data from simulation runs may be used to determine the test frequencies selected, e.g., a frequency to use for phase test measurement estimation. One approach is to select the phase test frequency near the cutoff frequency producing the minimal RMS error over the bandpass of the filter. A second approach is to select the phase test frequency near the cutoff where the phase error is minimal in the simulation to be dominant. Filter type selection may vary with receiver, transmitter, and/or transceiver design in order to accommodate the simple compensation module of the present invention. The method used for selection of the frequency estimation test frequency may be chosen to suit the requirements of the specific application.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates an exemplary receiver I/Q chain and I/Q error models.
FIG. 2 illustrates an exemplary transmitter I/Q chain and I/Q error models.
FIG. 3 illustrates a parallel model of an imperfect low-pass filtering operation.

FIG. 4 illustrates the concept of I/Q leakage compensation.
FIG. 5 illustrates an exemplary I/Q receiver chain including a two parameter digital compensation (correction) module in accordance with the present invention.
FIG. 6 illustrates an exemplary I/Q transmitter chain including a two parameter digital compensation (pre-distortion) module in accordance with the present invention.
FIG. 7 illustrates an exemplary I/Q receiver chain showing signal routing used for compensation parameter determination in accordance with the present invention.
FIG. 8 illustrates an exemplary I/Q receiver chain, including an exemplary compensation (correction) module of the present invention, showing signal routing used for normal receiver operation.
FIG. 9 illustrates an exemplary I/Q transmitter chain showing signal routing used for compensation parameter determination in accordance with the present invention.
FIG. 10 illustrates an exemplary I/Q transmitter chain, including an exemplary compensation (pre-distortion) module of the present invention, showing normal transmitter operation.
FIG. 11 illustrates an exemplary variable delay (first-order interpolation) filter and an exemplary digital compensation (correction/pre-distortion) circuit in accordance with the present invention.
FIG. 12 is a flowchart of an exemplary receiver filter pair I/Q imbalance compensation method in accordance with the present invention.
FIG. 13 is a flowchart of an exemplary transmitter filter pair I/Q imbalance compensation method in accordance with the present invention.
FIG. 14 shows statistical results for simulations of four exemplary filters.
FIG. 15 shows yield curves corresponding to the statistical results for the four exemplary filters.
FIG. 16 shows estimation error vs estimation frequency for the four exemplary filters.
FIG. 17 summarizes comparison results for the four filters evaluated.
FIG. 18 shows estimation error of the linear approximation of phase imbalance.

DETAILED DESCRIPTION

The present invention involves novel methods and apparatus for compensating frequency dependent mismatch such as frequency dependent mismatch in a pair of analog real low pass filters. The following description is presented to enable one skilled in the art to make and use the invention, and is provided in the context of particular embodiments and methods. Various modifications to the disclosed embodiments and methods will be apparent to those skilled in the art, and the general principles set forth below may be applied to other embodiments, methods and applications. Thus, the present invention is not intended to be limited to the embodiments and methods shown and the inventors regard their invention as the following disclosed methods, apparatus and materials and any other patentable subject matter to the extent that they are patentable.

FIG. 5 illustrates an exemplary I/Q receiver chain 500 implemented in accordance with the present invention. Receiver chain 500 includes an antenna 502, a low noise amplifier (LNA) 504, a pair of I/Q mixers 506, 508, a pair of real LPFs 510, 512, a pair of ADCs 514, 516, a digital compensation (correction) module 518, and a FFT 524. Antenna 502, LNA 504, and I/Q mixer pair 506, 508, may be similar or identical to components 102, 104, 106, and 108, respectively.
of FIG. 1 and shall not be further described. LPFs 510, 512 may be a real I/Q filter pair, selected in accordance with the invention, such that the filter has a relatively frequency-independent pass-band gain error and a relatively linear pass-band phase error (i.e., a delay) for the pair of filters. An exemplary real I/Q filter pair 510, 512 may be a seventh-order Butterworth low-pass filter. The ADCs 514, 516 output signals x_p, x_g, respectively, to the digital compensation module 518. The exemplary digital compensation (correction) module 518, implemented in accordance with the invention, includes a delay 520 which has been set to a tuned value (Δt_{LP}) and a gain 522 which has been set to a tuned value (1/ΔG). The digital compensation (correction) module 518 provides an estimated correction for the I/Q leakage (I/Q imbalance) of the low pass filters 510, 512 (and perhaps of the ADCs 514, 516). The output of the digital compensation (correction) module 518 signals x_p and x_g are input to the FFT 524.

FIG. 6 illustrates an exemplary I/Q transmitter chain 600 implemented in accordance with the present invention. Transmitter chain 600 includes a DSP 602, a digital compensation (pre-distortion) module 604, a pair of LPFs 614, 616, an IQ mixer block 618, a power amplifier 620, and an antenna 622. DSP 602 outputs I path signal x_I and Q path signal x_Q to the digital compensation (pre-distortion) module 604. The exemplary digital compensation (pre-distortion) module 604, implemented in accordance with the invention, includes a delay 606 which has been set to a tuned value (Δt_{LP}) and a gain 608 which has been set to a tuned value (1/ΔG). The digital compensation (pre-distortion) module 604 provides an estimated adjustment to the x_I and x_Q signals from DSP 602 to compensate for the I/Q leakage (I/Q imbalance) of the low pass filters 614, 616 (and perhaps the DACs 610, 612). The output of the digital compensation module 604 signals x_{IP} and x_{IQ} are input to the DACs 610, 612, respectively of FIG. 2 and shall not be further described.

FIG. 7 illustrates an exemplary I/Q receiver chain 700 showing exemplary signal routing used for compensation parameter determination (e.g., off-line test mode) in accordance with the present invention. Receiver chain 700 includes an antenna 702, a LNA 704, a pair of I/Q mixers 706, 708, a switching module 710, a pair of LPFs 712, 714, a pair of ADCs 716, 718, a switching module 720, a digital compensation (correction) module 722, a switching module 730, a FFT 732, a mode controller 734, a test signal generator 736, a test output measurement means (e.g., a module) 738, and a compensation parameter determination means (e.g., a module) 740.

Mode controller 734 controls the switching modules 710, 720, and 730 to interconnect the various components of the receiver appropriately for the mode selection. Mode controller 734 may also control the activation/deactivation of various components within the receiver depending upon the mode of operation thus conserving power. In FIG. 7, the receiver chain 700 is shown in test mode. In test mode, the antenna 702, the LNA 704 and the mixers 706, 708 do not need to be used and may be deactivated. Mode controller 734 directs test signal(s) from the test signal generator 736 in parallel to each of the LPFs 712, 714. The outputs of the ADCs 716, 718, are routed to the input of the FFT 732 (e.g., directly, bypassing the compensation module 722).

The test signal generator 736 generates a first frequency 742 and a second frequency 744. In accordance with the invention, the frequency values of the first test frequency 742 and the second test frequency 744 are selected to match the LPF pair (712, 714) in the receiver chain 700. First frequency 742, referred to as f_p, should be positioned near the middle of the pass-band of the filter (712, 714), and is used in measuring the gain I/Q imbalance. Second frequency 744, referred to as f_q, should be positioned near the edge of the band pass filter (712, 714), and is used in measuring the phase I/Q imbalance. In accordance with the invention, the first test frequency f_p and/or the second test frequency f_q may be selected using statistical analysis (e.g., median information) of simulations of the two-path real filter (712, 714) characteristics. Such simulations may be over a set of distinct frequencies encompassing the pass-band of the filter and for many sets (e.g., 2000) of simulated component mismatches within the filter. First test frequency f_p, may be selected near the center of the pass-band in an approximately flat (constant) region. One method to select the second test frequency f_q includes simulating an IMR (phase contribution) estimating (using a first order linear approximation) IMR (phase) for each of various simulation test frequencies (located near the edge of the pass-band region), determining RMS errors between the simulation IMR (phase) and each estimation IMR (phase), and selecting the simulation test frequency resulting in minimal RMS error over the band-pass of the filter as f_q. Using another approach, second test frequency f_q may be selected as the test frequency at the edge of the band-pass where the phase error is observed in the simulation to be dominant. Such a selection will improve the delay estimate near the pass-band edge, but the rms average over the pass-band range might suffer. This trade-off between good pass-band edge and low rms may drive the choice of second test frequency f_q depending on the application. Different applications may use different coding schemes and may tolerate different levels of transmission signal quality.

For example, choosing f_p=5 MHz and f_q=7 MHz is one possible scenario for an exemplary seventh-order 8.8 MHz Butterworth filter used in applications requiring low rms error. Alternately, choosing f_p=5 MHz and f_q=8 MHz is another possible scenario for an exemplary seventh-order 8.8 MHz Butterworth filter used in applications requiring low band-pass edge error.

In some embodiments, a two-tone (f_p, f_q) test signal is generated by signal generator 736 and injected into the input of both LPFs simultaneously. In other embodiments, a one-tone (f_p or f_q) test signal may be generated by signal generator 736 and injected into the input of both signals during a first interval of time, followed by a different one-tone (f_p or f_q, respectively) test signal during a second interval of time. Since both ΔG and Δp are subsequently determined by comparing the relative difference between t_1 and t_2, the amplitude and frequency accuracy of the injected test signal(s), e.g., a two-tone test signal, are not critical. The test signal(s) may be, and generally is, a real one wire base-band signal. There is no need to generate precise quadrature I/Q calibration tones to be used as test signals. The digital outputs t_1 and t_2 of the ADCs 716, 718, respectively, are routed into the FFT 732. When a signal including first test frequency f_p 742 is input to LPFs (712, 714), test output measurement means 738 measures the amplitudes of signals t_1 and t_2 at first frequency f_p 742 using FFT 732, obtaining T_1(f_p) and T_2(f_p). When a signal including second test frequency f_q 744 is input to LPFs (712, 714), test output measurement means 738 measures the phases of t_1 and t_2 at frequency f_q using FFT 732 obtaining angle T_1(f_q) and angle T_2(f_q). Compensation parameter deter-
information to determine an estimated gain error

\[
\delta G(f_p) = \left[ \frac{G(f_p)}{G(f_p_0)} \right] 
\]

and an estimated phase error

\[
\delta \Phi(f_p) = -\frac{\pi}{2} \angle T_2(f_p) - \angle T_1(f_p).
\]

Next, compensation parameter determination means 740 uses the measured gain and phase information to determine an estimated gain error

\[
\delta G(f_p) = \left[ \frac{G(f_p)}{G(f_p_0)} \right] 
\]

and an estimated phase error

\[
\delta \Phi(f_p) = -\frac{\pi}{2} \angle T_2(f_p) - \angle T_1(f_p).
\]

Mode controller 938 controls the switching modules 910 and 920 to interconnect the various components of the transmitter appropriately for the mode selection. Mode controller 938 may also control the activation/deactivation of various components within the transmitter depending on the mode of operation, thus conserving power. In FIG. 9, the transmitter chain 900 is shown in test mode. In test mode, the DSP 902, the mixer block 922, the power amplifier 924, and the antenna 926 are not needed and may be deactivated. Mode controller 938 directs test signal(s) from the test signal generator 940 in parallel to each of the DACs 912, 914. The outputs of the DACs 912, 914, are routed (e.g., directly) to the input of the LPFs 916, 918, respectively.

The test signal generator 940 includes a third frequency 942 and a fourth frequency 944. In accordance with the invention, the frequency values of the third test frequency 942 and the fourth test frequency 944 are selected to match the LPF pair (916, 918) in the transmitter chain 900. Third frequency 942, referred to as \( f_{TP} \), should be positioned near the middle of the band pass of the filter (916, 918), and is used in measuring the gain I/Q imbalance. Fourth frequency 944, referred to as \( f_{TP} \), should be positioned near the edge of the band pass filter (916, 918), and is used in measuring the phase I/Q imbalance. (Note: subscript \( T \) is used in FIGS. 9, 10 and 13 to designate correspondence to the transmitter chain.)

In accordance with the invention, the third test frequency \( f_{TP} \) and/or the fourth test frequency \( f_{TP} \) may be selected based upon statistical analysis (e.g., median information) of simulations of the two-path real filter (916, 918) characteristics. Such selection methods, previously described with respect to the receiver chain 700 of FIG. 7, are also applicable with respect to the transmitter chain 900 of FIG. 9.

In some embodiments, a two-tone (\( f_{TP} \) or \( f_{TP} \)) test signal is generated by test signal generator 940 and injected to the input of both DACs (912, 914) simultaneously. In other embodiments, a one-tone \( f_{TP} \) or \( f_{TP} \) test signal is generated by test signal generator 940 and may be injected into the input of both DACs during a first interval of time, followed by a different one-tone \( f_{TP} \) or \( f_{TP} \) test signal during a second interval of time.

The testing of FIG. 9 is used to model I/Q imbalance of the LPFs 916, 918 (and perhaps the DACs 912, 914). The ADCs 928, 930 are used for testing purposes and are not in the operational transmission chain. Therefore, any I/Q imbalance contribution during the testing due to the ADCs 928, 930 should be removed. One exemplary method to remove ADC (928, 930) I/Q imbalance contribution is to perform two sets of measurements for each frequency \( f_{TP} \) or \( f_{TP} \). A first set of measurements may be conducted with the ADCs 928, 930 and LPF 918 coupled to ADC 928 (shown by solid lines). A second set of measurements may be conducted with LPF 916 coupled to ADC 928 and LPF 918 coupled to ADC 930 (shown by dotted lines). Since the I/Q imbalance errors due to the ADCs 928, 930 are primarily gain errors, in some embodiments, only one set of measurements are performed at \( f_{TP} \). The switching of the routing between ADCs 928, 930 may be controlled by the mode controller 938. The digital outputs \( T_{TP1} \) and \( T_{TP2} \) of the ADCs 930, 928, respectively (solid line configuration) are routed into the FFT 932. The digital outputs \( T_{TP1} \) and \( T_{TP2} \) of the ADCs 928, 930, respectively (dashed line configuration) are routed into the FFT 932. When a signal including third test frequency \( f_{TP} \) is input to DACs (912, 914), test output measurement means 840 are performed to measure the amplitudes of signals \( T_{TP1} \) and \( T_{TP2} \) at frequency \( f_{TP} \) using FFT 932 and obtain \( |T_{TP1}(f_{TP})| \) and \( |T_{TP2}(f_{TP})| \) or \( |T_{TP1}(f_{TP})| \) and \( |T_{TP2}(f_{TP})| \). When a signal including fourth test frequency \( f_{TP} \) is input to LPF's.
Digital pre-distortion (correction) module 1004 performs a compensation of the LPF pair (1016/1018) and DAC pair (1012/1014) I/Q leakage. The compensation of module 1004 applied is a constant gain compensation 1008 and a constant delay compensation 1006, in accordance with the invention.

In some embodiments of the invention, e.g., a transceiver including both a receiver chain and a transmitter chain, some generated and injected at the input to both LPFs 916, 918. In such an embodiment, the I/Q imbalance, from such testing, could be determined for LPFs 916, 918, but would exclude the effect from DACS 912, 914. In accordance with the invention, the LPFs may be the most important components through which the test signals (used for compensation module tuning in accordance with the invention) should pass, since they include a frequency dependent I/Q imbalance.

The digital compensation module, of the present invention, includes a tunable delay and a tunable gain. The examples of receiver and transmitter chains of the present invention have shown the tunable delay in the I path and the tunable gain in the Q path. Other embodiments of the compensation module are possible, in accordance with the invention. For example, the tunable gain may be in the Q path and the tunable delay may be in the I path. Alternatively, the tunable delay and the tunable gain may be both in the I path or the tunable delay and the tunable gain may be both in the Q path. The tunable delay, of the compensation module, can be well approximated by a first-order interpolation filter since the delay mismatch is expected to be small compared to the sampling period $T_s = 1/f_s$. Graph 1100 of FIG. 11 illustrates a variable delay with a first-order interpolation. Block 1150 illustrates an exemplary conceptual digital compensation module that may be used as a compensation (correction) module in a receiver chain, or as a pre-distortion (correction) module in a transmitter chain, in accordance with the invention. Module 1150 includes an upper branch, used for phase correction operations, and a lower branch, used for gain correction operations. Module 1150 includes two multipliers 1114 (with a tunable coefficient $1/\delta G$), 1116 (with a tunable coefficient $\delta P/\omega_0 T_s$), two adders 1118, 1120 and two delay elements 1106, 1108. When a signal $x(n)$ is delayed by $\tau = \delta P/\omega_0 T_s$, then the resulting signal $x(n)$ can be calculated from $x(n+1)$ and $x(n)$ as illustrated in FIG. 1100 and represented by switch 1122 in the up position in drawing 1150. The gain correction branch includes a $T_s$ delay (represented by delay element 1112) for $\tau > 0$, in order for the gain correction branch to be synchronized with the phase correction operations. If the delay is negative, (i.e., $\tau < 0$), then $x(n-l)$ and $x(n)$ are used to determine $x(n)$, and the module is represented with switch 1122 in the down position in drawing 1150.
In some embodiments of the invention, the compensation module of the present invention may be an analog implementation rather than a digital implementation.

FIG. 12 is a flowchart 1200 illustrating an exemplary receiver filter pair I/Q imbalance compensation method in accordance with the present invention. The test signal(s) are generated and injected into the filter chain (1210). The response to the injected test signals is measured (1220). Compensation module values are determined (1230). Next, the determined compensation values are used to compensate for I/Q imbalance (1240). The receiver then returns to normal operation (1250).

The blocks of the flowchart 1200 of FIG. 12 shall now be discussed in more detail in the context of an exemplary receiver I/Q filter pair I/Q compensation operation in accordance with the methods of the present invention. The compensation operation starts, when the receiver is configured in a filter leakage test mode. FIG. 7 represents such an off-line filter leakage test mode. Mode controller 734 has controlled the switching modules 710, 720, and 730 to disconnect the mixers 706, 708 from the LPFs 712, 714 and to bypass the compensation module 722. In step 1210, test signal(s) are generated by test signal generator 736 and injected in the filter chain; the response output is measured (1220) by the test output measurement means 738 using FFT 732.

Two exemplary techniques of the signal generation/injection and measurement operations (1210 and 1220) are described below. In the first approach, two analog test signals, each at a distinct frequency are sequentially generated/injected and measured. A first analog test signal (e.g., exemplary test signal: testB(fp) at a first frequency (fp), 742, is generated by test generator 736 and applied to the inputs of both receiver I/Q LPFs 712, 714. The test output measurement means 738 measures the amplitude of the output signals t1(fp), t2(fp) from each ADC 716, 718, respectively using FFT 732. Then, the determined receiver I/Q gain and delay values 726, 724 are applied (installed) in the I/Q filter compensation “correction” module 722 (1240).

The receiver chain is returned to normal (e.g., on-line) operational mode (1250). Here, the mode controller 734 may direct the switching modules 710, 720, and 730 to reconfigure the receiver chain. Such a reconfigured receiver chain may be represented by FIG. 8. The gain and delay values installed in the compensation module 722, may remain and be used until another test signal compensation operation is performed.

In some embodiments, the compensation operation of FIG. 12 may be performed once, e.g., at the factory prior to shipment. In such an embodiment, some modules (e.g., the test signal generator 736, the test output measurement means 738, and the compensation parameter determination means 740) may be external testing devices and not included in the receiver. Alternatively or in addition, the test signal compensation operation may be performed intermittently during operations (e.g., once at power-on, occasionally or periodically during the operation at time intervals or per cycle (e.g., at turn-on as part on an initialization sequence). Such turn-on tuning during initialization may remove some component errors due to aging, current ambient temperature, and/or current supply voltage. Alternatively or in addition, the test signal compensation operation may be performed intermittently during operations (e.g., once at power-on, occasionally or periodically during the operation at time intervals where the receiver is not utilized for normal communications). Such occasional or periodic tuning may allow for adjustments as components in the receiver change due to self-heating of the components within the receiver, and/or errors due to supply voltage fluctuations. In some embodiments, a re-tuning compensation operation may be initiated by an observed degradation in the quality of the received signal (e.g., a bit error rate exceeding a threshold level).

FIG. 13 is a flowchart 1300 illustrating an exemplary transmitter filter pair I/Q imbalance compensation method in accordance with the present invention. The test signal(s) are generated and injected into the filter chain (1310). The response to the injected test signals is measured (1320). Compensation module values are determined (1330). Next, the determined compensation values are used to compensate for I/Q imbalance (1340). The transmitter returns to normal operation (1350).

The acts of the flowchart 1300 of FIG. 13 shall now be discussed in more detail in the context of an exemplary transmitter I/Q filter pair I/Q compensation operation in accordance with the methods of the present invention. The compensation operation starts when the transmitter is configured in a filter leakage test mode. FIG. 9 represents an exemplary off-line filter leakage test mode configuration. Mode controller 938 has controlled the switching modules 910 and 920 to disconnect the mixer block from the LPFs 916, 918 and to disconnect the compensation module 904 from the DACs 912, 914. Mode controller 938 has controlled switching module 920 to connect LPT 916 to ADC 930 and LPF 918 to ADC 928 (solid line configuration).

A receiver I/Q filter gain error value 726 is determined by the compensation parameter determination means 740 using the measured amplitude and phase information (1320). A receiver I/Q filter gain error value 726 is determined by the compensation parameter determination means 740 upon the phase measurements at the second frequency as described below. An estimated gain error at frequency fp is determined (ΔG(fp))=IT1(fp)/IT2(fp) and a gain compensation parameter (ΔGC 726) is determined by module 740 where ΔG=ΔGC(fp).

Two exemplary techniques of the signal generation/injection and measurement (1310 and 1320) are described below. In
the first approach, two digital test signals, each at a distinct frequency are sequentially generated/injected and measured. A first digital test signal (e.g., exemplary test signal: testAfrg, (frg)) at a third frequency (fTg), 942, is generated and applied to the inputs of both transmitter DACs 912, 914. Then, the amplitudes of output signals T1A(frg) and T2A(frg) from ADCs 930, 928 are measured by the test output measurement means 934 obtaining |T1A(frg)| and |T2A(frg)|. Next, the inputs to the ADCs 928, 930 are switched (to the dotted line configuration) such that LPF 916 couples to ADC 928 while LPF 918 couples to ADC 930. This switching operation is performed so that data may be collected to mathematically remove the I/Q gain imbalance present in the ADC pair (928/930). ADC pair (928/930) is not in the normal operational transmitter chain (See FIG. 6), and thus it is desirable that ADC pair (928/930) I/Q imbalance not influence the determination of transmitter chain pre-distortion (correction) module coefficients. Next, a first digital test signal (testAfrg, (frg)) at the third frequency (fTg), 942 is generated and applied to the inputs of both transmitter DACs 912, 914. The amplitudes of output signals T1A(frg) and T2A(frg) from ADCs 928, 930 are measured by the test output measurement means 934 obtaining |T1A(frg)| and |T2A(frg)|. Next, a second digital test signal (e.g., exemplary test signal: testB(frp)) at a fourth frequency (frp), 944 is generated and applied to the inputs of both transmitter DACS 912, 914. The test output measurement means 934 measures the phase of the output signals T1B(frp) and T2B(frp) from each of the ADCs. 928, 930 using FFT 932, obtaining angle T1B(frp), and angle T2B(frp).

A second approach to the signal generation/injection and measurement operations (1310 and 1320) shall now be described. In the second approach, a digital test signal, with two distinct frequencies is generated by test output measurement means 934, injected into the DACs 912, 914 and measured by the test output measurement means using FFT 932. A first digital test signal (e.g., exemplary test signal: testAfrg, (frg)) at a frequency (fTg), 942 and a component at a fourth frequency (frp), 944 is generated and input to both transmitter DACs 912, 914. Next, the test output measurement means 934 measures the amplitude of output signals T1A and T2A at the third frequency (fTg), 942 and measures the phase of the output signals T1A and T2A at the fourth frequency (frp), 944 using FFT 932, obtaining |T1A(fTg)| and |T2A(fTg)|, angle T1A(fTg), and angle T2A(fTg). Next, the inputs to the ADCs 928, 930 are switched (to the dotted line configuration) such that LPF 916 couples to ADC 928 while LPF 918 couples to ADC 930. Then, the first digital test signal (testB(frp)) including a component at a third frequency (fTg), 942 and a component at a fourth frequency (frp), 944 is generated and input to both transmitter DACs 912, 914. The amplitudes of output signals T1B and T2B are measured by the test output measurement means 934 using FFT 932, obtaining |T1B(frp)| and |T2B(frp)|. This repeat application of the test signal and collection of a second set of measurements is performed in order to obtain sufficient data to remove the I/Q gain imbalance due to the ADCs 928, 930, elements not in the operational transmitter chain.

Next, compensation parameter determination means 936 determines a gain error value and a filter delay error value based upon the measurements (1330).

Compensation parameter determination means 936 determines a compensation gain value 908 using the amplitude measurements collected at the third frequency (fTg), 942 as described below. An estimated gain error at frequency (fTg), 942 is determined:

$$\delta G(f_{rg}) = \sqrt{\frac{T_{T2A}(f_{rg})}{T_{T1A}(f_{rg})}} - \frac{T_{T2A}(f_{rg})}{T_{T1A}(f_{rg})}$$

A gain compensation parameter (1/\delta G) 908 is determined by module 936 where \( \delta G = -\delta G(f_{rg}) \).

Compensation parameter determination means 936 determines a compensation delay error value 906 using the phase measurements collected at the fourth frequency (frp), 944 as described below. An estimated phase error (\delta \phi (f_{rg}) at angle T_{T1A}(f_{rp}) or \delta \phi (f_{rp}) at angle T_{T2A}(f_{rp}) or angle T_{T1B}(f_{rp}) or angle T_{T2B}(f_{rp})/2) at frequency f_{rp}, 944 is determined. Next, compensation parameter determination means 936 determines a delay compensation parameter (\delta \rho(f_{rpm})) 906 where \( \delta \rho = -\delta \rho(f_{rpm}) \).

The determined transmitter I/Q gain and delay values (908, 906) are installed (loaded) in the IQ filter compensation pre-distortion (correction) module 904 (1340).

The transmitter chain may then be returned to normal (e.g., on-line) operational mode (1350). Here, the mode controller 938 may direct the switching modules 910 and 920 to reconfigure the transmitter chain. An exemplary reconfigured transmitter chain is shown in FIG. 10. The gain and delay values installed in the compensation module 904, may remain and be used until another test signal compensation operation is performed. In some embodiments, the compensation operation of FIG. 13 may be performed once (e.g., at the factory prior to shipment). Alternatively, or in addition, the test signal compensation operation may be performed once during each power on cycle (e.g., at turn-on as part of an initialization sequence). Alternatively, or in addition, the test signal compensation operation may be performed intermittently during operations (e.g., once at power-on, occasionally or periodically during the operation at time intervals where the transmitter is not being utilized). In some embodiments, a re-turning transmitter compensation operation may be initiated by an observed degradation in the quality of the received signal corresponding to transmissions from said transmitter.

Variations of the methods of the exemplary receiver I/Q compensation operation of FIG. 12 or the exemplary transmitter I/Q compensation operation of FIG. 13 are possible in accordance with the invention. For example, the order of signal generation/injection and measurements (with respect to gain and phase test frequencies) may be varied. The switching point for interchanging the inputs to ADCs 928, 930 may be performed at different points in the testing sequence. In addition, two individual test signals each with a single test frequency at a different time may be grouped together and viewed as a single test signal, in accordance with the invention.

The selection of various real low pass filters for the I/Q receiver and/or transmitter chain shall now be discussed with respect to the I/Q compensation module of the present invention. A proposed method for I/Q frequency dependent error compensation, in accordance with the present invention, apriori designates and designs the correction module to a simple digital implementation using a gain coefficient and a delay coefficient. The expected gain and phase imbalance, for a specific real low pass filter may be identified based on an extensive statistical analysis. These statistical results may be used to evaluate whether the pair of filters has a relatively frequency-independent pass-band gain error and a relatively linear pass-band phase error (i.e., a delay). In other words,
to I/Q phase imbalance as a function of frequency. Curve transfer function was investigated for an implementation (correction) method. However, the proposed method uses these assumptions, so it is less effective for filters with different behavior.

For filters, where these strict assumptions (described above) hold, the proposed I/Q compensation method of the present invention has the advantage that it provides a fast-estimation (non-iterative) and hardware-efficient compensation (correction) method. However, the proposed method uses these assumptions, so it is less effective for filters with different behavior.

Statistical evaluations indicate that a cascade-of-pole Butterworth filter (7th order transfer function with 8.8 MHz bandwidth) significantly benefits from the delay-based correction of the present invention. In order to check the validity of the proposed method for other filters, first, the same Butterworth transfer function was investigated for an implementation using a ladder topology. In addition, a 7th-order 0.5-dB ripple 8.8-MHz wide Chebyshev transfer function was investigated for both cascade-of-poles and ladder topologies.

FIG. 14 shows the frequency dependence of the uncompensated/compenated median IMR (\(\bar{w}\)) and gain/phase errors based on a 2000-trial statistical analysis for the four filter types described above. Graph 1410 plots median IMR (dB) on vertical axis 1411 vs frequency on horizontal axis 1412 for the Butterworth cassecker filter. Curve 1413 represents total uncorrected IMR (\(\bar{w}\)); curve 1414 represents total corrected IMR (\(\bar{w}\)) when a test frequency=8 MHz is used for the phase measurements; curve 1415 represents total corrected IMR (\(\bar{w}\)) when a test frequency=7 MHz is used for the phase measurements; curve 1416 represents the gain component \(dG\) (gain) of the uncorrected IMR (\(\bar{w}\)); curve 1417 represents the phase component \(dP\) (phase) of the uncorrected IMR (\(\bar{w}\)).

Graph 1420 plots median IMR(dB) on vertical axis 1421 vs frequency on horizontal axis 1422 for the Butterworth ladder filter. Curve 1423 represents total uncorrected IMR (\(\bar{w}\)); curve 1424 represents total corrected IMR (\(\bar{w}\)) when a test frequency=8 MHz is used for the phase measurements; curve 1425 represents total corrected IMR (\(\bar{w}\)) when a test frequency=7 MHz is used for the phase measurements; curve 1426 represents the gain component \(dG\) (gain) of the uncorrected IMR (\(\bar{w}\)); curve 1427 represents the phase component \(dP\) (phase) of the uncorrected IMR (\(\bar{w}\)).

(Slope of the phase error vs frequency curve can be reasonably approximated by a straight line).

FIG. 18 illustrates exemplary delay approximations of phase imbalance for an exemplary 7th order Butterworth filter with an 8.8 MHz bandwidth. FIG. 18 includes a graph 1800 of phase (deg) on the vertical axis 1801 vs frequency on the horizontal axis 1802. Curve 1803 illustrates phase error due to I/Q phase imbalance as a function of frequency. Curve 1804 illustrates a compensation approximation model with a constant delay \(\tau_x\) that may be obtained as a straight line approximation based on a phase measurement test frequency selection of 7 MHz. Both \(\tau_x\) and \(\tau_y\) approximate \(dP\) (phase) reasonably well.

Graph 1430 plots median IMR(dB) on vertical axis 1431 vs frequency on horizontal axis 1432 for the Chebyshev cascade filter. Curve 1433 represents total uncorrected IMR (\(\bar{w}\)); curve 1434 represents total corrected IMR (\(\bar{w}\)) when a test frequency=8 MHz is used for the phase measurements; curve 1435 represents total corrected IMR (\(\bar{w}\)) when a test frequency=7 MHz is used for the phase measurements; curve 1436 represents the gain component \(dG\) (gain) of the uncorrected IMR (\(\bar{w}\)); curve 1437 represents the phase component \(dP\) (phase) of the uncorrected IMR (\(\bar{w}\)).

Graph 1440 plots median IMR(dB) on vertical axis 1441 vs frequency on horizontal axis 1442 for the Chebyshev ladder filter. Curve 1443 represents total uncorrected IMR (\(\bar{w}\)); curve 1444 represents total corrected IMR (\(\bar{w}\)) when a test frequency=8 MHz is used for the phase measurements; curve 1445 represents total corrected IMR (\(\bar{w}\)) when a test frequency=7 MHz is used for the phase measurements; curve 1446 represents the gain component \(dG\) (gain) of the uncorrected IMR (\(\bar{w}\)); curve 1447 represents the phase component \(dP\) (phase) of the uncorrected IMR (\(\bar{w}\)).

Graph 1500 plots Yield (%) on vertical axis 1510 vs IMR(dB) on horizontal axis 1512 for the Butterworth cassecker filter. Curve 1513 represents yields for minimum of IMR (uncorrected); curve 1514 represents yields for minimum of IMR (corrected) when a test frequency=8 MHz is used for the phase measurements; curve 1515 represents yields for minimum of IMR (corrected) when a test frequency=7 MHz is used for the phase measurements; curve 1516 represents yields for minimum of IMR (corrected) when a test frequency=8 MHz is used for the phase measurements; curve 1517 represents yields for minimum of IMR (corrected) when a test frequency=7 MHz is used for the phase measurements.

Graph 1520 plots Yield (%) on vertical axis 1521 vs IMR (dB) on horizontal axis 1522 for the Butterworth ladder filter. Curve 1523 represents yields for minimum of IMR (uncorrected); curve 1534 represents yields for minimum of IMR (corrected); curve 1535 represents yields for minimum of IMR (corrected) when a test frequency=8 MHz is used for the phase measurements; curve 1526 represents yields for minimum of IMR (corrected) when a test frequency=7 MHz is used for the phase measurements; curve 1527 represents yields for minimum of IMR (corrected) when a test frequency=8 MHz is used for the phase measurements; curve 1528 represents yields for minimum of IMR (corrected) when a test frequency=7 MHz is used for the phase measurements.

Graph 1530 plots Yield (%) on vertical axis 1531 vs IMR (dB) on horizontal axis 1532 for the Chebyshev cascade filter. Curve 1533 represents yields for minimum of IMR (uncorrected); curve 1534 represents yields for minimum of IMR (corrected); curve 1535 represents yields for minimum of IMR (corrected) when a test frequency=8 MHz is used for the phase measurements; curve 1536 represents yields for minimum of IMR (corrected) when a test frequency=7 MHz is used for the phase measurements; curve 1537 represents yields for minimum of IMR (corrected) when a test frequency=8 MHz is used for the phase measurements; curve 1538 represents yields for minimum of IMR (corrected) when a test frequency=7 MHz is used for the phase measurements.

Graph 1540 plots Yield (%) on vertical axis 1541 vs IMR (dB) on horizontal axis 1542 for the Chebyshev ladder filter. Curve 1543 represents yields for minimum of IMR (uncorrected); curve 1544 represents yields for minimum of IMR (uncorrected); curve 1545 represents yields for minimum of IMR (corrected) when a test frequency=8 MHz is used for the phase measurements; curve 1546 represents yields for minimum of IMR (corrected) when a test frequency=7 MHz is used for the phase measurements; curve 1547 represents yields for minimum of IMR (corrected) when a test frequency=8 MHz is used for the phase measurements; curve 1548 represents yields for minimum of IMR (corrected) when a test frequency=7 MHz is used for the phase measurements.
measurements; curve 1546 represents yields for minimum of IMR (corrected) when a test frequency of 8 MHz is used for IMR (corrected); curve 1547 represents yields for rms of IMR (corrected) when a test frequency of 8 MHz is used for the phase measurements; curve 1548 represents yields for minimum of IMR (corrected) when a test frequency of 7 MHz is used for IMR (corrected).

Estimation error (dgr) vs estimation frequency is shown for each of the four filters evaluated in FIG. 16. Graph 1610 shows a curve 1613 plotting estimation error (dgr) on the vertical axis 1611 vs estimation frequency on the horizontal axis 1612 for the Butterworth cascade filter. Graph 1620 shows a curve 1623 plotting estimation error (dgr) on the vertical axis 1621 vs estimation frequency on the horizontal axis 1622 for the Butterworth ladder filter. Graph 1630 shows a curve 1633 plotting estimation error (dgr) on the vertical axis 1631 vs estimation frequency on the horizontal axis 1632 for the Chebyshev cascade filter. Graph 1640 shows a curve 1643 plotting estimation error (dgr) on the vertical axis 1641 vs estimation frequency on the horizontal axis 1642 for the Chebyshev ladder filter. The optimal f_p frequency (the test frequency to use for phase measurements) may be determined based on FIG. 16.

Table 1700 of FIG. 17 summaries comparison results for the four filters evaluated for a rms IMR (dB) with phase measurement test frequency f_p=7 MHz and gain measurement test frequency f_p=5 MHz.

The uncompensated IMR (un) results will be discussed first. Using Butterworth over Chebyshev transfer functions improves the amount of the rms IMR by about 3-5 dBs (FIG. 17). Also, the use of a ladder topology yields to about 2-4 dB better IMR than cascade-of-poles topology. This indicates, confirms the reduced sensitivity to circuit element mismatch of ladder filters. Interestingly, the gain error of the cascade-of-poles Chebyshev gradually bends over frequency (See curve 1436 of FIG. 14), so the constant gain-error assumption does not hold well for this filter. However, the gain error of a ladder Chebyshev flattens out except a sharp increase of about 10 dB close to the pass-band edge (See curve 1446 of FIG. 14). Butterworth filters show an approximately flat gain-error response with a slight bend near the pass-band edge (See curves 1416, 1426 of FIG. 14). FIG. 16 shows that the best phase-error estimation occurs for f_p of about 7 MHz for the four filters. Although there is a global minima at about 8 MHz for the Chebyshev transfer function, the local minima at about 7 MHz is not significantly higher and, more importantly, is much flatter. Therefore, f_p=7 MHz should be used for each of the four filters for "best" rms phase-error estimation. Note that Butterworth filters introduce roughly 5-dBs rms estimation error for f_p=7 MHz (i.e., -0.2° for Butterworth versus -1° for Chebyshev, FIG. 16). Therefore, Butterworth filters are much better candidates for delay-based compensation, of the present invention, due to their maximally-flat response than their ripples, but more selective, Chebyshev counterparts.

The effectiveness of the proposed compensation can be determined from FIGS. 14, 15 and 17. Clearly, a pair of ladder Butterworth filters is the best choice from the four candidate filters evaluated. Ladder Butterworth filters are the least affected by circuit-element mismatch to start with (i.e., uncorrected median rms IMR=35.2 dB, FIG. 17), and they can be the most effectively corrected by the proposed delay-based correction of the present invention (i.e., corrected median rms IMR=46.1 dB). Both the cascade-of-Poles Butterworth and ladder Chebyshev filters significantly benefit from the correction, which improves their performance by about 6-10 dB (FIG. 17). The approximately 2-dB improvement for a cascade-of-poles Chebyshev filter shows less improvement.

To ease the analog filtering requirements, in accordance with the invention, oversampling may be used in the TX and/or RX chain. In that case, the filter’s bandwidth may be slightly increased by, e.g., 10% or 20%, at the expense of some selectivity loss. From the results in FIG. 14, one may conclude that opening up the filter has the advantage that it reduces the uncompensated I/Q imbalance affecting the actual signal. In addition, the compensated IMR improves even more.

For example, the compensated median rms IMR of ladder Butterworth filters increases by 4.9 dB and 8.2 dB for 10% and 20% bandwidth increase, respectively, while the uncorrected median rms IMR gets improved by only 1.7 dB for the 20% bandwidth stretching (FIG. 14). Both Chebyshev filters show about 6-dB compensated and 3-dB uncompensated IMR improvement for 20% bandwidth increase. These values are 3-dB and 0.7 dB for the cascade-of-pole Butterworth case.

Based on analysis and in accordance with the methods of the invention, a "backward thinking" filter-design methodology may be used. A system-level designer may consider the I/Q imbalance as a constraint (like the stop-band attenuation, bandwidth or group delay) in choosing the transfer function and the topology. By making a choice which is apriori favorable for the proposed delay-based compensation of the present invention (e.g., choosing a ladder Butterworth filter), a simple and effective I/Q compensation, in accordance with the invention, is possible. In contrast, when the I/Q-imbalance constraint is ignored, laborious, complicated and/or costly known frequency-dependent I/Q correction schemes (previously referenced) may be required.

Although the invention has been described in the context of a low-pass real filter pair used for I/Q compensation, the method of the present invention may be also applicable to pairs of band-pass real filters. In such applications, the test frequency used to tune the compensation module to obtain the gain coefficient may selected near the center of the band-pass region. In addition the present invention may be used in applications other than I/Q receivers, transmitters, and/or transceivers which utilize filter pairs and may benefit from the compensation methods of the present invention.

In some embodiments various features and/or elements of the present invention are implemented using modules. Such modules may be implemented using software, hardware or a combination of software and hardware. Some of the above described methods can be implemented using machine executable instructions, such as software, included in a machine readable medium such as a memory device, to control a machine, with or without additional hardware, to implement all or portions of the above described methods, e.g., in one or more elements. Accordingly, among other things, the present invention is directed to a machine-readable medium including machine executable instructions for causing a machine, e.g., processor and associated hardware, to perform one or more of the steps of the above-described method(s).

What is claimed is:

1. A method for determining a gain error estimate and a delay error estimate in a pair of filters comprising:
   a) applying a test signal to an input of both filters;
   b) measuring an output signal at the output of each filter;
   c) determining the gain error at a first frequency and a phase error at a second frequency;
   d) determining the delay error estimate using the determined phase error, wherein the delay error estimate is constant with frequency.
23. The method of claim 22, further comprising:
i) providing the output of each pair of filters to the other one of the pair of analog to digital converters; and
ii) again measuring the output signal at the output of each of the analog to digital converters.

24. The method of claim 23, wherein determining the gain error at a first frequency removes a contribution from the analog to digital converter pair.

25. Apparatus for use in determining a gain error estimate and a delay error estimate in a pair of filters comprising:
a) a signal generator for applying a test signal to an input of each of the filters;
b) means for measuring an output signal at the output of each of the filters;
c) means for determining the gain error at a first frequency and a phase error at a second frequency;
d) means for determining the delay error estimate using the determined phase error, wherein the delay error estimate is constant with frequency;
e) means for compensating for the determined delay error using an implementation of a delay function, wherein, the delay function is substantially constant with frequency; and
f) means for compensating for the determined gain error using an implementation of a gain function, wherein the gain function is substantially constant with frequency.

26. The apparatus of claim 25, wherein the pair of filters are IQ filters.

27. The apparatus of claim 25, wherein the first frequency is different from the second frequency.

28. The apparatus of claim 25, wherein the first frequency is less than the second frequency.

29. The apparatus of claim 25, wherein the first frequency is well within a pass-band of the pair of filters.

30. The apparatus of claim 25 wherein the first frequency is at approximately a pass band center and wherein the pair of filters are low pass filters.

31. The apparatus of claim 25 wherein the first frequency is at a point in the upper portion of the transition region having a 0-3 dB attenuation from an average value.

32. The apparatus of claim 25 wherein the first frequency is at approximately DC and wherein the pair of filters are low pass filters.

33. The apparatus of claim 25 wherein the first frequency is at a point in the upper portion of the transition region having a 0-3 dB attenuation from an average value.

34. The apparatus of claim 25 wherein the first frequency is at approximately a band-pass center and wherein the pair of filters are band-pass filters.

35. The apparatus of claim 25 wherein the first frequency is a multi-tone signal including the first and second frequencies.

36. The apparatus of claim 25 wherein the test signal includes the first tone at a first time and the second tone at a second time other than the first time.

37. The apparatus of claim 25 wherein determining the delay error estimate uses the determined phase error estimate at the second frequency.

38. The apparatus of claim 25 wherein the second frequency is at a point in the upper portion of the transition region having a 0-3 dB attenuation from an average value.

39. The apparatus of claim 25 wherein determining the delay function is substantially constant with frequency.

40. The apparatus of claim 25 wherein the delay function is substantially constant with frequency.

41. The apparatus of claim 25 wherein the second frequency is at a point in the upper portion of the transition region having a 0-3 dB attenuation from an average value.

42. The apparatus of claim 25 wherein the pair of filters are band-pass filters.

43. The apparatus of claim 25 wherein the first frequency is at approximately DC and wherein the pair of filters are low pass filters.

44. The apparatus of claim 25 wherein the first frequency is at approximately a band-pass center and wherein the pair of filters are band-pass filters.

45. The apparatus of claim 25 wherein the second frequency is in a transition region of a cutoff frequency of the filters.

46. The apparatus of claim 25 wherein the second frequency is at a point in the upper portion of the transition region having 0-20 dB attenuation from an average value.

47. The apparatus of claim 25 wherein the second frequency is at a point in the upper portion of the transition region having 0-3 dB attenuation from an average value.

48. The apparatus of claim 25 wherein the first frequency is at approximately a pass band center and wherein the pair of filters are low pass filters.

49. The apparatus of claim 25 wherein the first frequency is a multi-tone signal including the first and second frequencies.

50. The apparatus of claim 25 wherein the test signal includes the first tone at a first time and the second tone at a second time other than the first time.

51. The apparatus of claim 25 wherein determining the delay error estimate uses the determined phase error estimate at the second frequency.

52. The apparatus of claim 25 wherein the second frequency is at a point in the upper portion of the transition region having 0-20 dB attenuation from an average value.

53. The apparatus of claim 25 wherein the second frequency is at a point in the upper portion of the transition region having 0-3 dB attenuation from an average value.

54. The apparatus of claim 25 wherein the filters are low-pass filters.

55. The apparatus of claim 25 wherein the test signal is two-tone signal including the first and second frequencies.

56. The apparatus of claim 25 wherein the test signal includes the first tone at a first time and the second tone at a second time other than the first time.

57. The apparatus of claim 25 wherein determining the delay error estimate uses the determined phase error estimate at the second frequency.

58. The apparatus of claim 25 wherein the second frequency is at a point in the upper portion of the transition region having a 0-3 dB attenuation from an average value.

59. The apparatus of claim 25 wherein determining the delay function is substantially constant with frequency.
41. The apparatus of claim 25, wherein the second frequency improves the delay compensation near the bandpass edge.

42. The apparatus of claim 25 wherein, the pair of filters are part of a receiver chain.

43. The apparatus of claim 42 wherein, the determined gain error at a first frequency includes gain error from an analog to digital converter pair in the receiver chain in addition to gain error due to said pair of filters.

44. The apparatus of claim 43 wherein, the receiver chain is part of a transceiver and wherein the generator for applying a test signal includes a digital to analog converter which is part of a transmitter chain in said transceiver.

45. The apparatus of claim 25 wherein the pair of filters are part of a transmitter chain.

46. The apparatus of claim 45 wherein, the determined gain error at a first frequency includes gain error from a digital to analog converter pair in the transmitter chain in addition to gain error due to said pair of filters.

47. The apparatus of claim 25 wherein the means for measuring an output signal at the output of each filter includes a pair of analog to digital converters, means for providing the output of each of the pair of filters to a corresponding one of the pair of analog to digital converters, and means for measuring an output at each of the analog to digital converters.

48. The apparatus of claim 47 further comprising:
   i) switching means for providing the output of each of the pair of filters to the other one of the pair of analog to digital converters; and
   ii) measuring means for again measuring the output signal at the output of each of the analog to digital converters.

49. The apparatus of claim 48 wherein the means for determining the gain error at a first frequency removes a contribution from the analog to digital converter pair.

50. The apparatus of claim 47 wherein the pair of filters is part of a transmitter chain, the pair of analog to digital converters is part of a receiver chain, and the receiver and transmitter chains are part of a transceiver.

51. The apparatus of claim 25 wherein the means for compensating for the determined delay error and the means for compensating the determined delay error are included in a compensation module in series with said filter pair.

52. The apparatus of claim 25 wherein the compensation module is a digital implementation and precedes a digital to analog converter pair and the filter pair in a transmitter chain.

53. The apparatus of claim 25 wherein the compensation module is a digital implementation and is situated downstream to said filter pair and an analog to digital converter pair in a receiver chain.

54. The apparatus of claim 25 wherein the apparatus is part of a mobile communications device.

55. Apparatus for use in compensating I/Q imbalance in a low pass filter pair in at least one of a receiver, a transmitter, and a transceiver, using a delay error and a gain error determined using a test system including:
   a generator for applying a test signal to the inputs of the low path filter pair;
   means for measuring an output signal at the output of each filter in the low pass filter pair;
   means for determining the gain error at a first frequency and a phase error at a second frequency; and
   means for determining the delay error estimate using the determined phase error, wherein the delay error estimate is constant with frequency, said apparatus comprising:
   a) means for compensating for the determined delay error using an implementation of a delay function, wherein, the delay function is substantially constant with frequency; and
   b) means for compensating the determined gain error using an implementation of a gain function, wherein the gain function is substantially constant with frequency.

56. The apparatus of claim 55 wherein the at least one of a receiver, a transmitter, and a transceiver is part of a mobile communications device.

57. A method for determining a gain error estimate and a delay error estimate in a pair of filters comprising:
   a) applying a test signal to an input of both filters;
   b) measuring an output signal at the output of each filter;
   c) determining the gain error at a first frequency and a phase error at a second frequency; and
   d) determining the delay error estimate using the determined phase error,
   wherein the delay error estimate is constant with frequency; and
   wherein the pair of filters are part of a transmitter chain.

58. The method of claim 57 wherein the determined gain error at a first frequency includes gain error from a digital to analog converter pair in the transmitter chain in addition to gain error due to the pair of filters.

59. The method of claim 57 wherein the act of measuring an output signal at the output of each filter includes providing the output of each of the pair of filters to a corresponding one of a pair of analog to digital converters and measuring an output at each of the analog to digital converters.

60. The method of claim 59 further comprising providing the output of each the pair of filters to the other one of the pair of analog to digital converters; and again measuring the output signal at the output of each of the analog to digital converters.

61. The method of claim 60 wherein determining the gain error at a first frequency removes a contribution from the analog to digital converter pair.

62. Apparatus for use in determining a gain error estimate and a delay error estimate in a pair of filters comprising:
   a) a signal generator for applying a test signal to an input of each of the filters;
   b) means for measuring an output signal at the output of each of the filters;
   c) means for determining the gain error at a first frequency and a phase error at a second frequency; and
   d) means for determining the delay error estimate using the determined phase error,
   wherein the delay error estimate is constant with frequency, and
   wherein the pair of filters are part of a transmitter chain.