New CMOS Universal Constant-Gm Input Stage

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Abstract— Conceptually new constant-gm input-stage architecture is presented. It provides near constant net transconductance independent of transistor operating region - strong, moderate or weak inversion. One possible implementation of the proposed architecture is discussed in details. Its operation has been experimentally verified. Results from performed measurements are included.

1   Introduction

One way to achieve near rail-to-rail operation of an op-amp which is to be used in unity-gain configuration is to employ a complementary input stage. The simplest such stage consists of an n-channel and p-channel diff-pairs driven in parallel. This simple input stage however is rarely used because its net transconductance g_{m_T} varies by a factor of two over the common-mode input range. In mid-supply, where both pairs operate, the net transconductance is given by:

$$g_{m_T} = g_{m_{n0}} + g_{m_{p0}} \qquad (1)$$

where $g_{m_{n0}}$ and $g_{m_{p0}}$ denote respectively the nominal transconductance of the n-channel and p-channel differential pairs. However, when the input common-mode voltage approaches V_{sup} (ground) the p-channel (n-channel) pair is not functioning and g_{m_T} reduces to $g_{m_{n0}}$ ($g_{m_{p0}}$) respectively. This variation does not allow optimal frequency compensation of multi-stage op-amps. This effect has been disscussed extensively elsewhere [2].

In the last several years a few input stage topologies with reduced g_{m_T}-variation have been reported. Those structures are often referred to as "constant-g_m rail-to-rail" input stages. Most of these circuits are either "strong-inversion" [1],[2],[8] or "weak-inversion" architectures [7], [9]. That is: they can provide near constant net transconductance in strong or weak inversion mode of operation, but not in both of them.

An interesting input topology was reported in [3]. It was designed to provide low gm-variation in weak as well as strong inversion mode of operation. Architectures having such a property are called "universal". This structure appears to be the first attempt of a design of a universal input stage.[1] This structure can be viewed as being comprised of a pair of constant-gm weak-inversion input stages connected in parallel[2] (see Fig. 1(a). When this topology is operated in weak inversion, its transconductance remains constant over the entire rail-to-rail input

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[1]Three other universal input stage topologies has been described recently [4], [5], [6].

[2]Same is the configuration of the structures reported in [5] and [6].
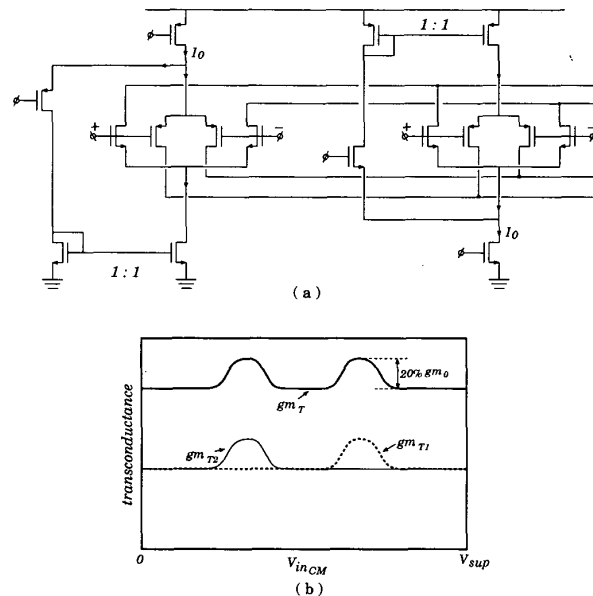

Figure 1: Universal constant-g_m consisting of two "weak-inversion" architectures connected in parallel.

common-mode range. When it is operated in strong inversion within the corresponding transition region, the region where the switching between pairs occurs, the transconductance of each stage exhibits an increase of 40% from its nominal value (see Fig. 1(b)). However, since the two "bumps" do not coincide they cause only a 20% variation in the total transconductance.

In this paper we describe alternative way of configuring universal constant-gm input stage. The proposed circuit was fabricated via MOSIS. Measured results are presented.

2   New Class of Universal Constant-Gm Input Stages

As mentioned in the introduction there are many different CMOS rail-to-rail input stages. They all, however, have a common feature:

Their net transconductance is the sum of two (or more) individual transconductances, each a non-negative function of the input common-mode voltage.
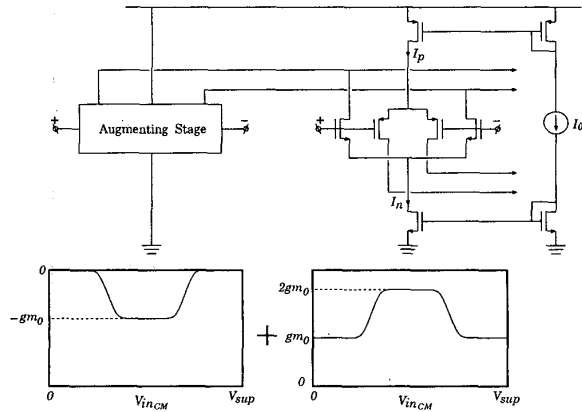
Figure 2: Proposed constant-gm architecture.

Theoretically, there exists another alternative:

Constant net transconductance formed as a sum of positive as well as negative individual transconductances.

In this section, we will discuss the implementation and the properties of rail-to-rail input stages whose operation is based upon the above-stated general idea.

2.1 The Architecture

Fig. 2 shows the conceptual schematic of an input stage, whose flat transconductance is achieved by combining two positive (those of the diff. pair stages) transconductances and a suitably chosen negative transconductance. The negative one is contributed by the additional stage labeled "augmenting stage." Clearly, any implementation of this general architecture would require at least three differential pairs driven in parallel.

To implement the general Fig. 2 topology we first need to design a differential stage whose transconductance is non-zero only in the mid-supply region. Such a circuit is shown in Fig. 3(a). It utilizes an n-channel and a p-channel diff. pair. The n-channel pair is the core of the augmenting stage, while the p-channel one is embedded into the branch providing the biasing.

The operation of the Fig. 3(a) structure can be explained as follows. For low common-mode input voltages transistor M_7 is biased in saturation. Thus, the presence of the p-channel pair will not alter the operation of the M_b-M_7 branch and the current conducted by the diode-connected transistor M_4 would be I_0. In this region, the operation of the input stage as well as the variation of its transconductance will be identical to that of an n-channel diff. pair with regular (constant) biasing (e.g. Fig 3(b)) and will be solely determined by the operating region (saturation or triode) of M_3.

In the mid-supply region M_7 as well as M_3 will be in saturation. Thus, the tail current will take its nominal I_0 value and the transconductance in this region will be almost constant and equal to $gm_n(I_0)$ (see the equivalent
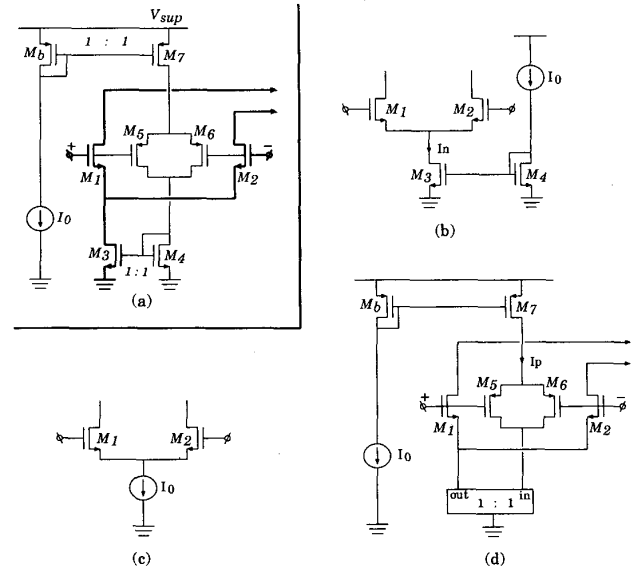

Figure 3: (a) Schematic of the required augmenting stage. Equivalent circuits: (b) for near-ground and mid-supply region; (c) for mid-supply region; (d) for mid-supply and near-rail region;

Fig. 3(c) circuit).

As the input common-mode voltage approaches the supply rail, due to the presence of the p-channel diff. pair, M_7 will go into the triode region. The current conducted by this transistor (I_p) is mirrored by the fully operational (in this region) $M_3 - M_4$ current mirror (e.g. Fig. 3(d)) and provided as a bias current for the n-channel diff. pair. As I_p reduces, so does the transconductance of the n-channel pair $gm_n(I_0) \geq gm_n(I_p) \geq 0$.

The configured constant-gm input stage is shown in Fig. 4. For proper operation all transistors comprising the augmenting stage should be made identical to the corresponding complementary stage transistors. It is important to note that the input terminals of the augmenting stage are interchanged when compared to those of the complementary stage. Thus, the small-signal currents of the augmenting and complementary stage will be 180° out of phase, which is equivalent to a negative gm-contribution from the augmenting stage.

The individual transconductances as well as the net transconductance of the Fig. 4 input stage for all five distinct common-mode regions are summarized in Table 1. This table clearly shows that the input stage can have constant transconductance over the entire common-mode input range provided the n-channel transistors have the same $gm - I$ relation as that of the p-channel transistors; i.e.,

$$gm_n(I) = gm_p(I) \quad for \ any \ value \ of \quad I \quad (2)$$

Note that the actual gm vs. I relation is not important. This suggests that the developed input stage can potentially provide constant net transconductance independently of the operating mode (strong, moderate or weak

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Figure 4: Schematic of proposed universal constant-gm input stage.
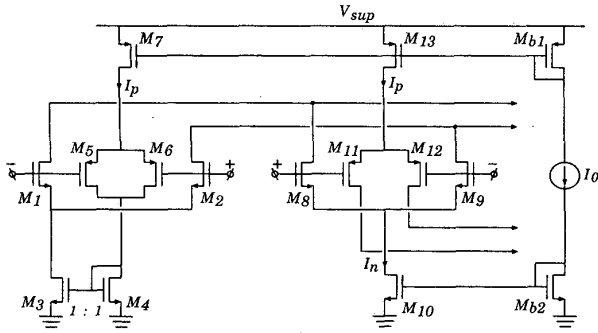
all augmenting stage transistors are matched to the corresponding complementary stage transistors

Regions of Operation	TRANSCONDUCTANCE of		
	Complementary Diff. Pair Stage	Augmenting Stage	Constant-Gm Input Stage
near-ground	$gm_p(I_o)$	0	$gm_p(I_o)$
transition (low common-mode)	$gm_p(I_o) + gm_n(I_n)$	$gm_n(I_n)$	$gm_p(I_o)$
mid-supply	$gm_p(I_o) + gm_n(I_o)$	$gm_n(I_o)$	$gm_p(I_o)$
transition (high common-mode)	$gm_n(I_o) + gm_p(I_p)$	$gm_n(I_p)$	$gm_n(I_o) + gm_p(I_p) - gm_n(I_p)$
near-supply	$gm_n(I_o)$	0	$gm_n(I_o)$

Table 1: Summary of the transconductances of Fig. 4 circuit for all five distinct common-mode regions.

inversion).

Using the EKV gm expression of a saturated MOS transistor [11]

$$gm = \sqrt{\frac{2\beta I_D}{n}} \; G\left(\frac{I_D}{I_S}\right) \qquad (3)$$

where $G(x) = \frac{1}{\sqrt{1+\sqrt{1/x+1/x}}}$, n – is the slope factor and $I_S = 2n\beta U_T^2$, it is easy to show that (2) requirement will be satisfied provided:

$$\beta_n = \beta_p \qquad and \qquad n_n = n_p \qquad (4)$$

are satisfied. In practice however neither of those two conditions can perfectly be met. Experimental results (to be presented next) show that beta and slope-factor mismatches cause a certain gm-variation, but do not alter the "universal" nature of this topology.

2.2 Experimental Results

The Fig. 4 input stage was fabricated using *HP SCN*12 (a 1.2μ CMOS process) available via MOSIS. The aspect ratios of the used transistors were as follows:
M_1, M_2, M_8 and M_9 - 30/3.6;
M_3, M_4, M_{10} and M_{b2} - 2 × 30/3.6;
M_5, M_6, M_{11} and M_{12} - 2 × 34.8/2.4;
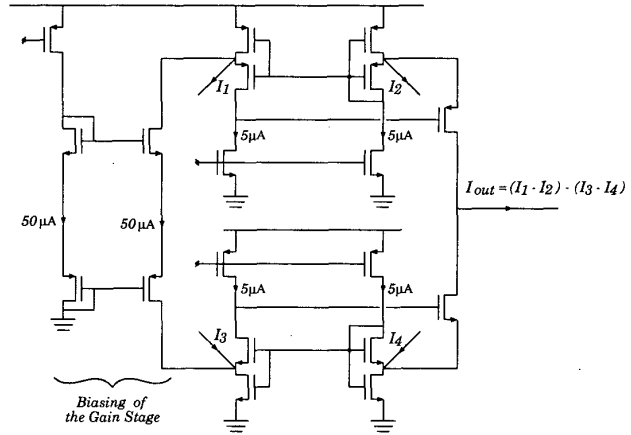M_7, M_{13} and M_{b1} - 4 × 34.8/2.4;

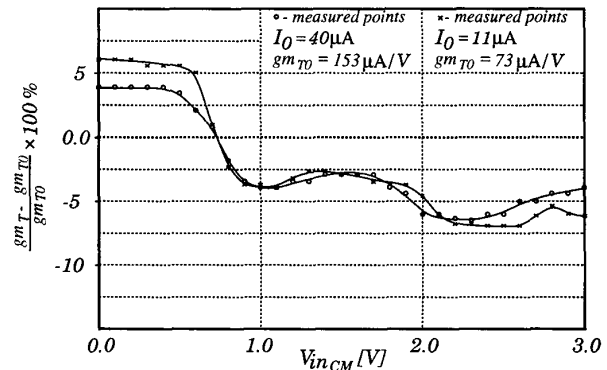Figure 5: High-swing gain stage used in the input stage evaluation.

Figure 6: Measured net transconductance variation of the Fig. 4 input stage vs. common-mode input voltage

The input stage was connected (externally) to a high-swing gain stage and its net transconductances was measured for thirty different points over the common-mode $(0-3V)$ input range. The schematic of the used gain stage is shown in Fig. 5. This circuit exhibits output resistance comparable to that of a cascode. Its output swing however is better than that of commonly used "high-swing" architecture. More details about this structure and its principle of operation can be found in [10].

To demonstrate the universal nature of this input stages the net transconductance of Fig. 4 input stage was measured for two different bias currents ($40\mu A$ and $11\mu A$). Fig. 6 shows a plot of the variation of its net transconductance expressed as percentage of the nominal transconductance value. Performed calculations, using data provided for run, showed that the observed variation is mainly due to the non identical and common-mode dependent slope factors (n_n and n_p) rather than β-mismatch.

Since the transconductance of an MOS transistor in strong inversion is proportional to $1/\sqrt{n}$ while in weak inversion is proportional to $1/n$, the slightly larger gm-variation in the
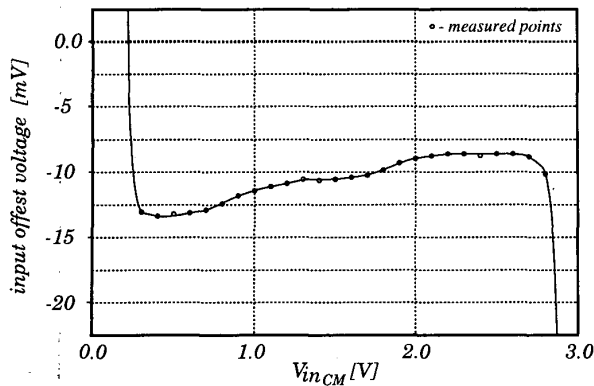
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Figure 7: Measured input offset vs. common-mode voltage of an unbuffered op-amp employing Fig. 4 rail-to-rail input stage.

$11 \mu A$ case is additional proof of the fact that the transconductance variation is due to slope-factor mismatch.

The input offset voltage of the unbuffered op-amp configured by connecting Fig. 4 input stage to Fig. 5 gain stage was measured as well. Its value as a function of the input common-mode voltage is plotted in Fig. 7. In general, a common-mode dependent offset is created whenever there is a mismatch between a pair of "matched" transistors and their bias currents vary with the common-mode voltage. Such pairs of transistors are present in both the input stage (the diff. pair transistors) and the gain stage[3]. Thus, the measured offset is an aggregate of the input-stage and the gain-stage offsets. Since transistor mismatches and thus the resulting offsets are random, one would need to take data over many chips in order to draw definite conclusions from the Fig. 7 plots.

3 Conclusions

CMOS op-amp input-stage architecture is presented. It has a rail-to-rail operating range with near constant transconductance. Unlike most such circuits, the variation of its net transconductance is little sensitive to the operating mode of the used MOS transistors (weak, moderate or strong inversion). The proposed circuit was fabricated and measured. Experimental results showed that the transconductance of this input stage exhibits some 5% variation over common-mode input range. Most of this variation can be attributed to mismatch of transistor slope factors.

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[3]The common-mode currents of the input stage are being injected into the gain stage and cause the bias currents of some gain-stage transistors to vary with the common-mode input voltage.

References

[1] R. Hogervost et al., "CMOS low-voltage operational amplifiers with constant-gm rail-to-rail input stage," *Proceedings, 1992 Int. Symp. on Circuits and Systems,* pp. 2876-2879.

[2] S. Sakurai and M. Ismail, *Low-Voltage CMOS Operational Amplifiers: Theory, Design and Implementation.*Boston, Kluwer Academic Publishers, 1995.

[3] R. Hogervorst et al., "A programmable 3-V CMOS rail-to-rail op amp with with gain boosting for driving heavy resistive loads," *Proceedings, 1995 Int. Symp. on Circuits and Systems,* pp. 1544-1547.

[4] C. Hwang, A. Motamed and M. Ismail, "Universal constant-gm input-stage architectures for low-voltage op amps," *IEEE Transactions on Circuits and Systems - Part I,* vol. 42, pp. 886-894, Nov. 1995.

[5] W. Redman-White, "High bandwidth constant gm and slew-rate rail-to-rail CMOS input circuit and its application to analog cells for low voltage VLSI systems," *IEEE J. of Solid-State Circuits,* vol. 32, pp. 701-712, May 1997.

[6] S. Lindfors, M. Ismail and K. Halonen, "Constant-g_m rail-to-rail CMOS input stages with improved robustness,"*Proceedings, 1997 Int. Symp. on Circuits and Systems,* pp. 1956-1959.

[7] J. H. Botma, R. F. Wassenaar and R. J. Wiegerink, "Simple rail-to-rail low-voltage constant-transconductance CMOS input stage in weak inversion," *Electronics Letters,* vol. 29, No. 12 pp. 1145-1147, June 1993.

[8] V. I. Prodanov and M. M. Green, "Simple rail-to-rail constant-transconductance input stage operating in strong inversion," *Proceedings, 1996 Midwest Symp. on Circuits and Systems,* pp. 957-960.

[9] V. I. Prodanov and M. M. Green, "Bipolar/CMOS (weak inversion)rail-to-rail constant-gm input stage," *Electronics Letters,* vol. 33, No. 5, pp. 386-387, Feb. 1997.

[10] V. I. Prodanov and M. M. Green, "CMOS current mirrors with reduced input and output voltage requirements," *Electronic Letters,* vol. 32, no. 2, pp. 104-105, 1996.

[11] C. C. Enz, F. Krummenacher and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," special issue of the *Analog Integrated Circuits and Signal Processing* on low-voltage and low-power design, Jan. 1995.