Design Techniques and Paradigms Toward Design of Low-Voltage CMOS Analog Circuits

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Abstract— **Techniques for the design of robust low-voltage CMOS analog circuits are given. It is shown that both V_t-independence and proper alignment between the input and output swings are crucial for effective design of low-voltage circuits.**

I. Introduction

Virtually everyone involved in the design of integrated circuits is aware of the strong push to operate at ever-decreasing supply voltages. Many IC companies are manufacturing circuits that operate at 3.3V for low-voltage/low-power operation such as laptop computers. Now many companies are looking toward operation at even lower supply voltages, even down to 1V, in the not-too-distant future.

Given that in a standard CMOS fabrication process most of the important parameters for design (e.g., threshold voltage) will be optimized for operation of digital circuits, without a doubt the possibility of robust analog circuits working down to 1V will require a major paradigm shift in the way we think about design. In this paper we will discuss some ideas for designs that can accommodate operation near $V_{DD} = 1$V without requiring any special process considerations. In particular, we make the following assumptions:

1. No special fabrication steps are required; in particular, all threshold voltages are dictated by considerations related to the *digital* circuitry.
2. All MOS transistors operate in strong inversion to allow high speed design (e.g., video/radio frequencies).

Low-voltage BJT circuits are already quite common. Designing CMOS analog circuits operating at similar low supply voltages is far more difficult, however, due to some fundamental differences in the behavior of these devices. These differences are illustrated in Table I. In this table, V_T denotes the thermal voltage kT/q; V_t denotes the MOS threshold voltage; V_A denotes the BJT Early voltage; W_B denotes the BJT base width; $\Delta V_{GS} \equiv V_{GS} - V_t$ for an MOS transistor. Notice that the intrinsic gain and unity-gain frequency are, in a first-order analysis, dependent only on processing parameters and fundamental physical constants for the BJT, not on the transistor biasing. Since the minimum supply voltage for a BJT circuit is determined only by $V_{BE(on)}$, obtaining low-voltage operation of BJT circuits while retaining sufficient performance parameters is straightforward. The dependence of these parameters on V_T for the BJT case, however, is replaced by ΔV_{GS} for the MOS case, which is of course bias dependent. The minimum supply voltage will be determined by $V_t + \Delta V_{GS}$, which is also bias dependent. Moreover, threshold voltages are unlikely to drop below $0.4 \sim 0.5$V even as MOS feature sizes continue to decrease due to constraints from the digital circuitry. Thus there exist significant obstacles to the design of low-voltage, high-performance analog CMOS circuits. These obstacles are exacerbated by the fact that ΔV_{GS} is much more sensitive to increases in bias current than V_{BE}, also illustrated in Table I. This fact impacts the low-voltage design of circuits that require adjustable bias currents, such as tunable continuous-time filters.

TABLE I
Comparison of BJT and MOS performance parameters.

Parameter	BJT	MOS
Intrinsic gain ($g_m r_o$):	V_A/V_T	$2\lambda^{-1}/\Delta V_{GS}$
Unity gain frequency (ω_T):	$2\frac{\mu}{W_B^2} \cdot V_T$	$\frac{3}{2}\frac{\mu}{L^2} \cdot \Delta V_{GS}$
Minimum supply voltage:	$V_{BE(on)}$	$V_t + \Delta V_{GS}$
Bias current $\times 10$ results in:	$V_{BE} + 60$mV	$\Delta V_{GS} \times 3.2$

To illustrate the difficulty of obtaining low-voltage operation of a CMOS circuit, consider the standard CMOS folded-cascode amplifier shown in Fig. 1(a). The output range ΔV_{out} of this circuit is determined by the values of V_{out} for which transistors M_7 and M_9 stay in the saturation region. In order to simplify this analysis, we assume that the threshold voltage and ΔV_{GS} are the same for all transistors. In this case, as illustrated by the chart shown in Fig. 1(a), V_{out} can swing within $V_t + 2\Delta V_{GS}$ of either rail. Likewise, the input common-mode swing ΔV_{CM} is determined by the values of V_{CM} for which transistors M_1, M_2 and M_3 stay in the saturation region. This range is also illustrated in the Fig. 1(a) chart. If we now assume that this amplifier is to be used in a unity-gain configuration (this is the most stringent condition with regard to dynamic range), then the overall swing $\Delta V \equiv \Delta V_{out} \cap \Delta V_{CM}$ which in this case is $\Delta V_{out} = V_{DD} - (2V_t + 4\Delta V_{GS})$. Clearly this circuit is not of much use for $V_{DD} < 5$V.

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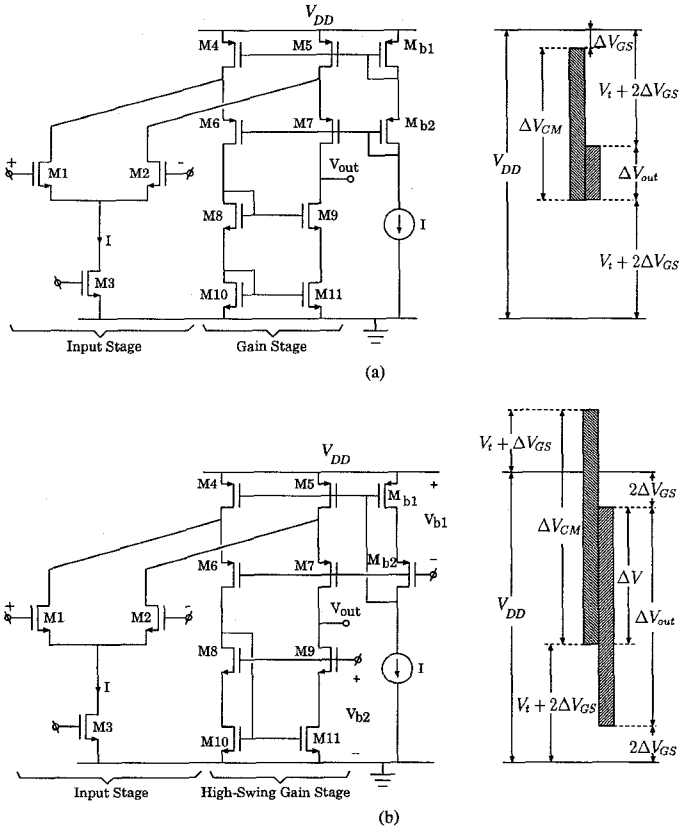

Fig. 1. (a) Standard folded-cascode CMOS amplifier; (b) High-swing folded-cascode amplifier.

A well known method for increasing the swing of the folded-cascode amplifier is shown in Fig. 1(b). In this "high-swing" amplifier, the transistors are biased such that V_{out} can swing V_t closer to either rail, as illustrated in the chart shown in Fig. 1(b); i.e., $\Delta V_{out} = V_{DD} - 4\Delta V_{GS}$. Notice that this expression for ΔV_{out} does not involve V_t. This property, called "V_t-independence," is very desirable for low-voltage operation. Using a similar analysis as before, the input common-mode swing $V_{CM} = V_{DD} - (V_t + 2\Delta V_{GS})$.

Although this structure can operate at lower supply voltages than the standard folded cascode amplifier, it has several disadvantages:

1. The V_t-independence of the output swing ΔV_{out} is based upon several transistors being biased on the edge of the their saturation region. In order to make the circuit more robust, there is usually a margin of 100 $\sim$ 200mV designed into the circuit. This margin detracts directly from the output swing.
2. The input stage is V_t -dependent, thereby making the overall swing V_t-dependent.
3. The supply voltage must be at least $2V_t$ in order to properly bias all transistors.

The following section addresses these disadvantages with some novel circuit topologies.

II. Design of Novel Low-Voltage Analog Blocks

A. Low-Voltage Current Mirrors

One can show that the voltage-current relation of the stacked-transistor configuration shown in Fig. 2, where M is biased in triode, is given by:

$$I_D + (1 + \frac{\beta}{\beta_b})I_b = \frac{\beta}{2}(V_{GS} - V_t)^2 \qquad (1)$$

Hence, the stacked-transistor topology with input current I_D has the same V_{GS} as that of a diode-connected MOS transistor conducting current $I_D + (1 + \frac{\beta}{\beta_b})I_b$. This idea can be used to configure linear current mirrors with reduced input and/or output voltage requirements (e.g. Fig. 3). The drawback of the Fig. 3(a) and Fig. 3(b) low-voltage current mirrors is the presence of an offset. An offset-free version of a low-voltage Wilson current mirror is shown in Fig. 3(c). It has V_t-independent input and output voltage requirements and output resistance on the order of $g_m r_o^2$. The constraint on the supply voltage for this circuit is given by:

$$V_{DD} \geq V_t + 2\Delta V_{GS} + V_{DS1,2}$$

Simulations show that the circuit behaves as a current mirror with $r_{out} > 10\text{M}\Omega$ for $V_{in} \geq 200\text{mV}$, $V_{out} \geq 250\text{mV}$ and $V_{DD} \geq 1.2\text{V}$ with $V_t = 0.9\text{V}$. More details on this circuit are given in [1].

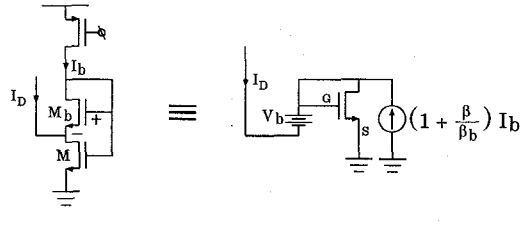

Fig. 2. Stacked-transistor topology and its equivalent.

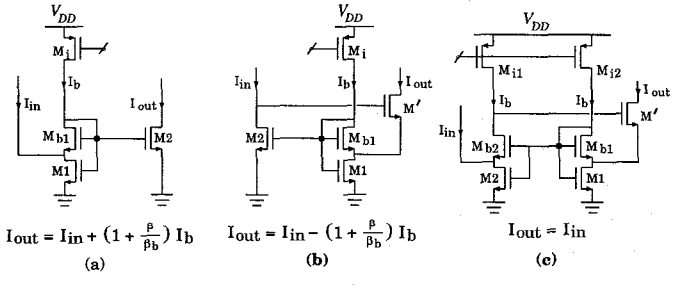

Fig. 3. Low-voltage current mirrors: (a) simple topology; (b) Wilson topology; (c) Offset-free Wilson-like topology;

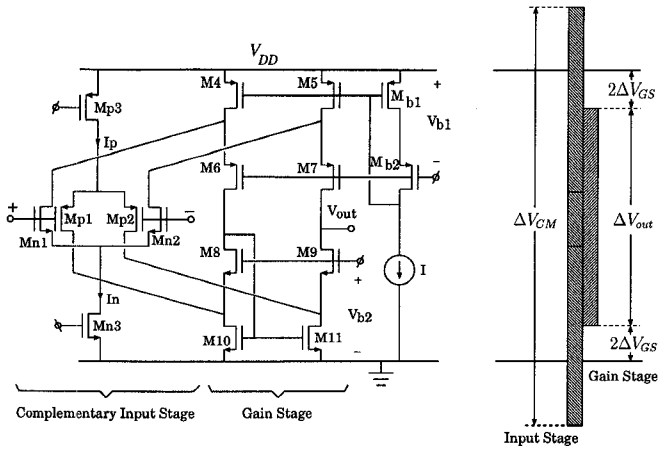

Fig. 4. Rail-to-rail op-amp using complementary input stage

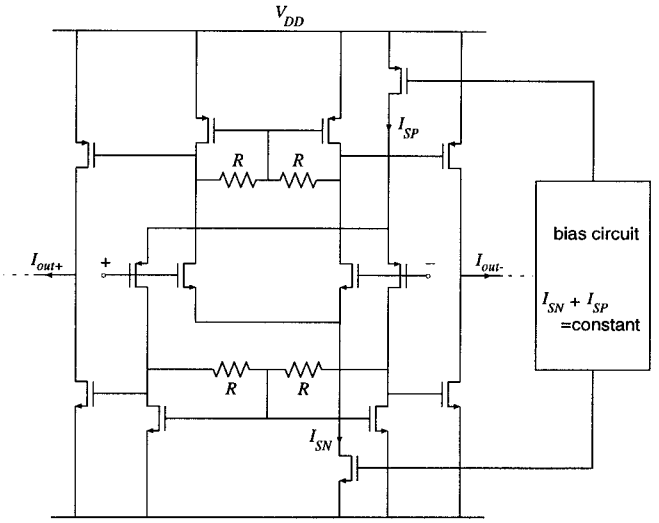

Fig. 6. Complementary input stage using two-stage differential pairs.

B. Constant-g_m Complementary Input Stage

The underlying reason for the V_t-dependence of the swing of the Fig. 1(b) amplifier is the fact that for sufficient common-mode rejection, a current source is required to bias the input differential pair. It is this transistor that limits the common-swing toward the negative rail. To achieve rail-to-rail input swing the use of complementary input stage, with an n-channel and p-channel differential pair driven in parallel (e.g. Fig. 4) has been proposed. If the tail currents are kept constant then this input stage will have a transconductance that varies with the common-mode input, which is very undesirable in an amplifier. However, if all transistors are biased in strong inversion and a constant transconductance is desired, then the relation

$$\sqrt{\beta_n I_n} + \sqrt{\beta_p I_p} = constant \tag{2}$$

must be satisfied. Circuits realizing (2) have been reported [2]-[5]. However, these circuits tend to be quite complex and most assume tracking of the k' between n-channel and p-channel transistors [3]-[5], which is undesirable for robust operation over processing variations.

A better approach is based upon using the two-stage structure shown in Fig 5. It can be shown, assuming the p-channel transistors are all of identical dimensions, that

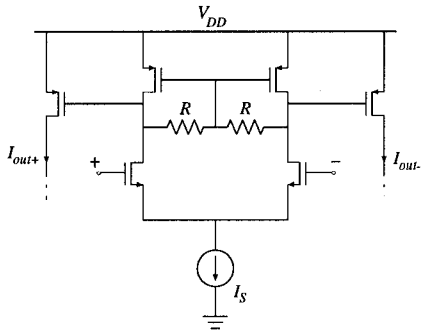

Fig. 5. Two-stage differential pair

the effective transconductance of this block is given by:

$$g_{m(eff)} \equiv \frac{i_{out+} - i_{out-}}{v_+ - v_-} = \sqrt{\beta_n \beta_p} R I_S \tag{3}$$

If this two-stage differential pair is used in a complementary fashion as shown in Fig. 6, then the overall effective transconductance is given by:

$$g_{m(eff)} = \sqrt{\beta_n \beta_p} R (I_{SN} + I_{SP}) \tag{4}$$

In order to keep $g_{m(eff)}$ constant, all that is needed to keep the sum of two dc currents constant, which requires only simple circuitry [7], [8]. Notice that no matching of n-channel and p-channel parameters is required.

Notice that the Fig. 5 two-stage input stage has a transconductance that is proportional to the bias current *itself*, rather than proportional to the *square root* of the bias current, as with conventional MOS strong-inversion differential pairs. Hence this block is also useful for wide-range tunable applications.

C. Input/Output Swing Alignment Using On-Chip Charge Pump

Although the complementary input stage discussed above is an improvement over previous reported results, there are two problems associated with any kind of complementary input stage. First, a complementary input stage does extend the common-mode swing however the *biasing* of both differential pairs still constrains $V_{DD} > 2V_t + 2\Delta V_{GS}$. Second, the nonlinear behavior inherent in such an input stage (i.e., switching between differential pairs) makes it very difficult to accommodate linear operation with a large differential input (e.g., a linear V–I converter). Attempts to design such circuits results in a high amount of complexity [9]. To overcome both of these obstacles, the following technique can be used.

First we observe from Fig. 1(b) that $\Delta V_{CM} \approx \Delta V_{out}$. Hence, the limitation on input/output swing is in fact not

due to the individual input/output swings, rather the relative *alignment* of these two ranges. If it could be arranged that the common-mode range is simply *shifted down* by V_t, then the two ranges would be aligned, thus giving a much higher overall swing. A technique for shifting the common-mode range is shown in Fig. 7. (The high-swing gain stage is not shown in the Figure.) The input range is shifted down by $V_t + \Delta V_{GS}$ by the source-follower transistors M_2. However, in order to keep current sources transistors M_3 properly biased for common-mode ranges near the positive rail, their sources must be higher than V_{DD}. Assuming that an on-chip clock is available from the digital circuitry, such a voltage can be generated using an on-chip charge pump [10]. Notice that this charge pump is only required to provide current $2I_{shift}$ which would typically be quite small. Hence, this charge pump, including the filtering capacitor, could be built entirely on the chip without the requirement of extra pins. Note that since this input stage is based on a simple differential pair, standard linearization techniques, such as source degeneration, can be used.

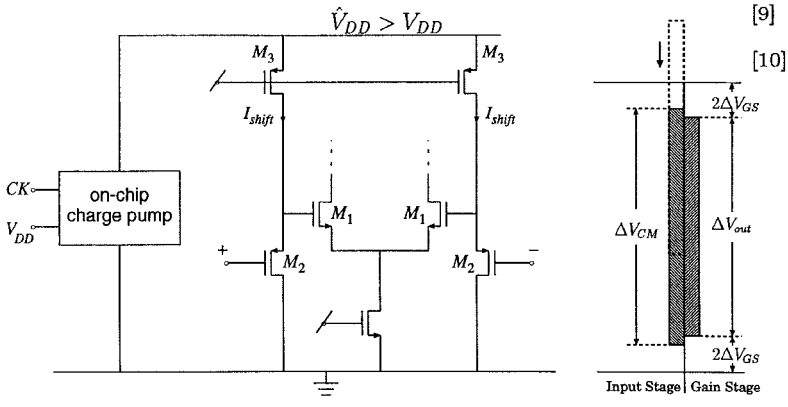

Fig. 7. Differential pair with on-chip charge pump to align its swing with that of the gain stage

III. Conclusion

A number of techniques for design of CMOS analog circuits for low-voltage applications have been presented. It was shown that V_t–independence and input/output swing alignment are powerful techniques for designing robust low-voltage analog circuits.

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