

# V-I CONVERTERS WITH TRANSCONDUCTANCE PROPORTIONAL TO BIAS CURRENT IN ANY TECHNOLOGY

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## ABSTRACT

In this paper we discuss circuits comprised of multiple differential pairs driven in parallel. We show that high linearity and linear with bias current tunability are intrinsic properties of any equidistant-offset multi-pair circuit. We argue that these two properties could potentially allow us to implement designs of analog filters, multipliers and other circuits that are (in first-order) technology independent. Simulations results are provided in support of presented simple intuitive explanation.

## 1. INTRODUCTION

Architectures using parallel combination of differential pairs, where each pair has suitably chosen offset voltage, have been studied and used extensively (see [1] and its many references). Due to the fact that bipolar transistor and for that reason bipolar differential pair have well-defined  $V-I$  characteristics ( $\tanh$  for the second one) most of the reported multi-pair structures are bipolar. Those, often called "multi- $\tanh$ " circuits [1], [2], have been used for synthesis of trigonometric functions [3], [4] and design of amplifiers with gain inversely proportional to control signal [5]. Multi- $\tanh$  circuits have also been used to implement continuous-time filters [6] and analog multipliers [7]. The properties that make multi- $\tanh$  circuits useful in filtering and analog multiplication applications are their *linearity* and *linear tuning* capability (transconductance proportional to bias current).

The aim of this paper is to show that linear (with respect to bias current) tuning is property of *any* equidistant-offset multi-pair transconductor and not only of those implemented in bipolar technology. The importance of the above stated fact is that multi-pair based circuits can be migrated from one technology to another without significant change in their operation.

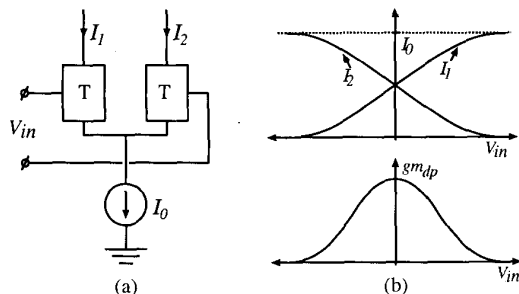


Figure 1: Differential Pair Circuit: (a) schematic; (b) voltage-current and transconductance characteristics;

## 2. FUNDAMENTAL PROPERTIES OF SIMPLE DIFFERENTIAL PAIRS

In this section we will identify those diff.-pair properties that are fundamental for the operation of a multi-pair equidistant-offset circuit.

In Fig. 1(a) a differential-pair circuit is shown. The reason for depicting the used devices as "boxes" is to emphasize the fact that *no assumptions* about the used technology (bipolar or MOS) will be made. We will however assume that the two devices comprising the diff. pair are identical, i.e. perfectly matched. Under this condition the incremental transconductance of the diff.-pair circuit,

$$gm_{dp}(V_{in}) = \left| \frac{\partial I_1}{\partial V_{in}} \right| = \left| \frac{\partial I_2}{\partial V_{in}} \right| \quad (1)$$

is symmetric function of  $V_{in}$ . The shape of the  $gm$  curve strongly depends on voltage-current characteristics of the used devices. *The area under the curve, however, is completely independent of the device characteristics.* This area equals the absolute change of  $I_{1,2}$ ; which, as depicted in Fig. 1, is the tail current  $I_0$ . Thus,

$$\int_{-\infty}^{\infty} gm_{dp}(x) dx = I_0 \quad (2)$$

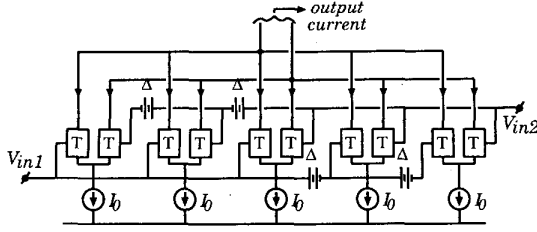


Figure 2: Conceptual Schematic of Multi-pair Equidistant-offset Circuit.

The symmetry of the  $gm_{dp}$  characteristic and the constancy of the area under the  $gm_{dp}$  curve are the two properties we will base our further discussion upon.

### 3. PROPERTIES OF EQUIDISTANT-OFFSET MULTI-PAIR ARCHITECTURES

The conceptual schematic of a multi-pair structure having equidistant offsets is shown in Fig. 2. The structure consists of many identical differential pairs, each having well-defined offset voltage. The pair in the middle does not have an offset while all others do. As we move off the central pair the offset increases progressively taking values  $\pm\Delta, \pm2\Delta$ , etc.

To simplify the discussion we will first consider a hypothetical multi-pair circuit consisting of infinitely many differential pairs.

#### 3.1. The infinite-pair case

As shown in Fig. 3(a) the transconductance function of an infinite-pair circuit is the sum of infinitely many identical  $\Delta$ -spaced  $gm_{dp}$  functions, i.e.

$$gm_{mdp}(V_{in}) = \sum_{k=-\infty}^{\infty} gm_{dp}(V_{in} + k\Delta) \quad (3)$$

The transconductance is obviously even periodic function of  $V_{in}$  (period of  $\Delta$ ). Thus, the resulting transconductance function can be written in the form:

$$gm_{mdp}(V_{in}) = \sum_{k=0}^{\infty} a_k \cos\left(2\pi k \frac{V_{in}}{\Delta}\right) \quad (4)$$

where all  $a_k$  coefficients have dimensions  $A/V$ .

The above expression can also be written as follows:

$$gm_{mdp}(V_{in}) = a_0[1 + R(V_{in})] \quad (5)$$

Here  $R(V_{in}) = \sum_{k=1}^{\infty} \frac{a_k}{a_0} \cos\left(2\pi k \frac{V_{in}}{\Delta}\right)$  is a dimensionless quantity that averages to zero in one  $\Delta$  period. Function  $R(V_{in})$  describes the variation of  $gm_{mdp}$ . For that

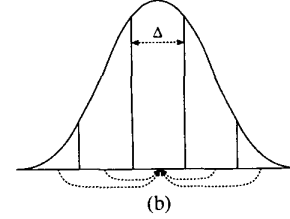
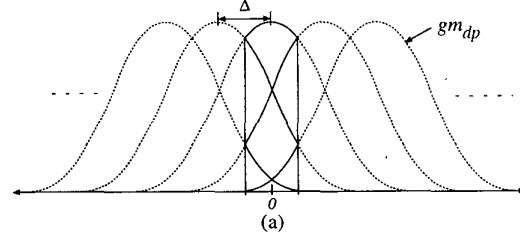


Figure 3: Transconductance of a multi-pair circuit ( $gm_{mdp}$ ) having equidistant offset voltages: (a)  $gm_{mdp}$  as a sum of identical  $\Delta$ -spaced  $gm_{dp}$  functions. (b) viewing  $gm_{mdp}$  in a  $\Delta$  region as "sliced & overlaid"  $gm_{dp}$  function.

reason we will call it "the ripple" of  $gm_{mdp}$ . Because of the periodicity it suffices to consider the behavior of  $gm_{mdp}$  only in the region  $\pm\frac{\Delta}{2}$ . Upon such consideration, we find the following: the  $gm_{mdp}$  in the region  $\pm\frac{\Delta}{2}$  can be viewed (see Fig. 3(b)) as a result of slicing a single  $gm_{dp}$  function into  $\Delta$ -pieces and overlaying them on top of each other. Thus, the area under the  $gm_{mdp}$  curve in the region  $\pm\frac{\Delta}{2}$  equals the total area under a single  $gm_{dp}$  curve.

$$\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} gm_{mdp}(x) dx = \int_{-\infty}^{\infty} gm_{dp}(x) dx = I_0 \quad (6)$$

Using equation (6) it is trivial to show that  $a_0$  is given by:

$$a_0 = \frac{I_0}{\Delta} \quad (7)$$

Thus,  $a_0$  depends only on the biasing ( $I_0$  and  $\Delta$ ) and not on the  $V-I$  characteristic of the used transistors, i.e. the average (over one  $\Delta$  period) transconductance value is *independent of technology*. The same result can be obtained in mathematically more rigorous way. It can also be shown that the higher-order coefficients do depend on  $V-I$  characteristic of the used devices. Luckily, all those coefficients and as a result the ripple

<sup>1</sup>An excellent framework for studying the relationship between  $gm_{mdp}$  and  $gm_{dp}$  results from the observation that  $gm_{mdp}$  can be viewed as convolution of  $gm_{dp}$  and an infinite train of  $\Delta$ -spaced  $\delta$  functions.

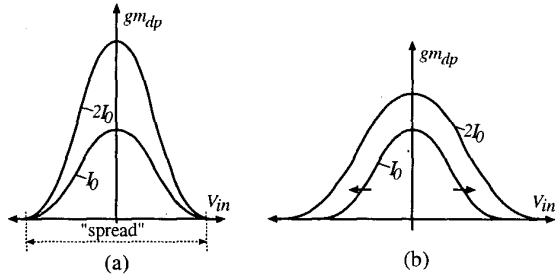


Figure 4: Qualitative depiction of the affect that tail current has on transconductance characteristic: (a) for BJT; (b) for MOS transistor;

$R(V_{in})$  are also functions of  $\Delta$  and diminish rapidly with its reduction. Thus, high linearity (small  $R(V_{in})$ ) can be achieved by proper selection of the offset voltage.

Assume that  $\Delta$  is selected such that  $R_{max} = \frac{\Delta}{I_0} |\sum_{k=1}^{\infty} a_k|$  is much smaller than 1, then we can write:

$$g_{m_{dp}}(V_{in}) \approx a_0 = \frac{I_0}{\Delta} \quad (8)$$

This equation clearly shows that as a multi-pair circuit is being linearized its effective transconductance becomes:

1) linearly dependent on the bias current.

2) insensitive to the  $V-I$  characteristics of the used active devices, i.e. to technology.

The above equation also suggests that the transconductance can be made nearly temperature, supply and process independent by making  $I_0$  and  $\Delta$  temperature, supply and process independent. This task can be accomplished in any technology using standard band-gap-based bias techniques.

### 3.2. The practical finite-pair case

The transconductance of a multi-pair circuit employing finite number of differential pairs has three different regions: a middle region and two end regions. The middle region is the range of input voltages  $V_{in}$  for which the following holds:

$$\int_{V_{in}-\frac{\Delta}{2}}^{V_{in}+\frac{\Delta}{2}} g_{m_{dp}}(x) dx = I_0 \quad (9)$$

Hence, in this region the operation and the properties of the finite-pair circuit are identical to those of an infinite-pair one. Depending on the number of used pairs, selected technology and  $\Delta$  such region may or may not exist.

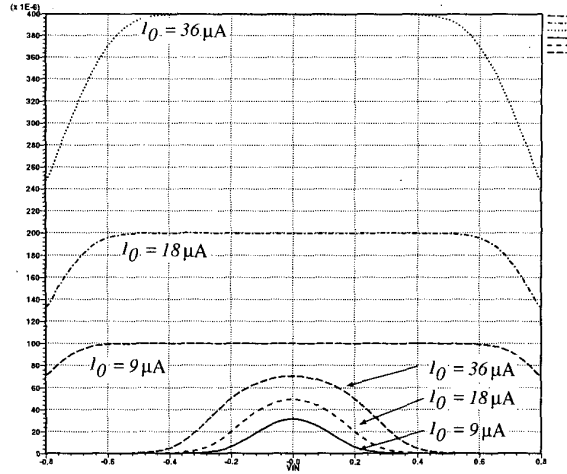


Figure 5: Transconductance of 19-pair equidistant-offset MOS circuit ( $\Delta = 90mV$ ) and that of one of its diff. pairs for three different bias currents (simulation).

The affect of having finite number of pairs is observed in the "end regions". There

$$\int_{V_{in}-\frac{\Delta}{2}}^{V_{in}+\frac{\Delta}{2}} g_{m_{dp}}(x) dV_x < I_0 \quad (10)$$

and  $g_{m_{dp}}$  has value that is smaller than the nominal (and desired)  $I_0/\Delta$ . The end regions of a bipolar circuit do not change with  $I_0$  while those of a MOS circuit grow with  $I_0$ . This difference is direct consequence of the fact that the spread of  $g_{m_{dp}}$  of a bipolar diff. pair does not change with  $I_0$  (see Fig. 4 (a)) while the spread of the  $g_{m_{dp}}$  of a MOS diff. pair (as depicted in Fig. 4(b) and demonstrated in Fig. 5) increases with  $I_0^2$ .

Fig. 5 simulation results are for  $0.25\mu m$  CMOS process. Diff. pair transistors have  $L = 0.32\mu m$  and  $W = 1\mu m$ . Ideal voltage sources were used to implement desired  $\Delta$ s.

As shown in Fig. 5 the increase of the end regions in MOS multi-pair circuits causes decrease of the available mid region. Nevertheless multi-pair MOS circuits can provide reasonable input linear range and a decade of linear-with-current tuning.

Fig. 6 compares the transconductances of two 19-pair CMOS circuits. Both circuits have the same  $\Delta$  and  $I_0$ . The used diff. pair transistors however have different aspect ratios ( $0.32\mu m/1\mu m$  and  $0.32\mu m/2\mu m$ ). Fig. 6 plots clearly demonstrate the fact that mid-

<sup>2</sup>in square-root fashion in strong inversion and linearly in the regime of mobility saturation.

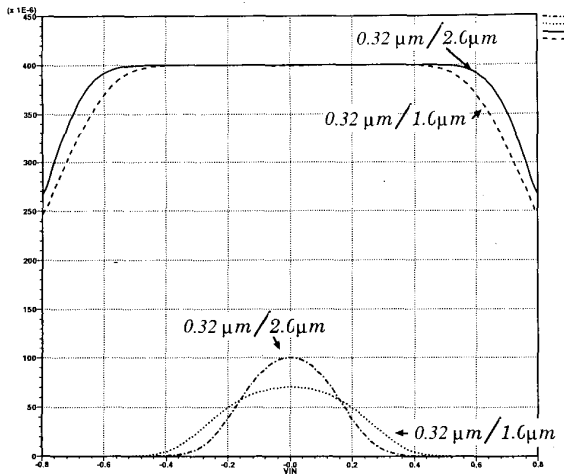


Figure 6: Transconductance of 19-pair MOS circuit and that of one of its diff. pairs for two different device widths (simulation).

region transconductance is mainly determined by biasing (e.g.  $\Delta$  and  $I_0$ ) and it is little sensitive to  $V - I$  characteristics of devices. This suggests that no matter what technology is used Fig. 7 bias arrangement will deliver predictable and nearly constant (over temperature and process variation) transconductance. The last was verified (via simulation) during the design of a decade-tunable (5 – 50 MHz)  $G_m/OTA/C$  CMOS filter. Experimental results are currently being collected.

#### 4. CONCLUSIONS

We have shown that linearity and linear (with bias current) tuning are properties of any multi-pair equidistant-offset circuit and not only to those implemented in bipolar technologies. This property can potentially allow us to implement designs of analog filters, multipliers and other circuits that are (in first-order) technology independent.

#### 5. REFERENCES

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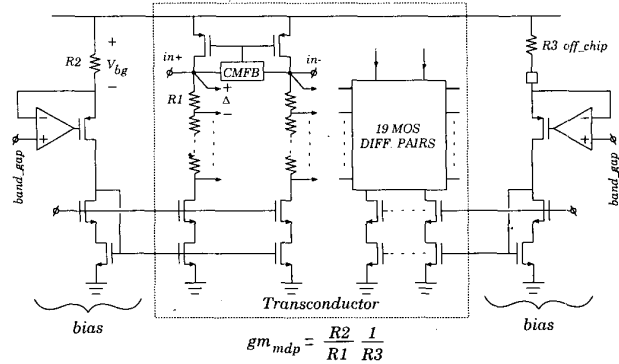


Figure 7: Conceptual schematic of bias arrangement of multi-pair transconductor used  $G_m/OTA/C$  filter.

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