FOCE Medium Voltage Load Switcher

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Thanks to the Electrical Engineering Department for the facilities used for circuit assembly and testing, as well as allowing this collaboration to happen in the first place.

We would also like to thank our friends and families. Without your support we would not be where we are today.
I. INTRODUCTION:

The Free Ocean Carbon Dioxide Enrichment, or FOCE project is one of the many ongoing projects that is funded for and operated by the Monterey Bay Aquarium Research Institute (MBARI). Since the start of the industrial era, the ocean has been absorbing an increasing amount of carbon dioxide. Several observations have confirmed a rise in acidity of the ocean, signified by a fairly significant pH drop. However, few tests were in place to study the long term effects of this phenomenon, and MBARI saw the need to investigate the impact of this acidification on marine ecosystems.

A more detailed summary of the FOCE project can be found here:


This specific project is a collaborative effort between MBARI and Cal Poly, in the hopes of developing an ongoing, mutually beneficial relationship. Chad Kecy, Cal Poly Alumni and current Electrical Engineer at MBARI, is responsible for both the partnership with Cal Poly as well as the inspiration and direction for the project itself. It is important to note that the timeline for the FOCE project far exceeds in length that of this Senior Project, and while a comprehensive design is the goal of this project, it is not in the best interest of the overall success of FOCE to rush a prototype to meet a deadline. Therefore, this Senior Project can be seen as an ongoing and open-ended collaboration, the result of which may or may not be the final design, but certainly is a thoroughly tested and functional circuit.
II. BACKGROUND:

The FOCE Medium Voltage Load Switcher is part of an upgrade package of the electronics on the currently deployed FOCE experiment. The current electrical system is functional, but is an early generation model which lacks some capabilities. The proposed design will implement various improvements, specifically in improved power monitoring of scientific instruments and user control. The project outlined a PIC controlled power monitoring circuit, with user programmable conditions, to communicate via SPI to the main onboard CPU. This allows all of FOCE’s core components to interact and react to each other seamlessly.
III. REQUIREMENTS:

The functional description and requirements of the project were provided at the onset of the project by Mr. Kecy, and can be seen in Appendices A and B, respectively. The preliminary design approach included a broad range of hardware and software requirements, which enveloped a completed four channel medium voltage load switching circuit. This project outline was presented to demonstrate the end product MBARI intends to produce, and ultimately give our project a specific direction. Since final design includes four identical channels, circuit trace outlines and component specification was constantly a matter of concern.
IV. DESIGN AND CONSTRUCTION:

Located in Appendix E are a series of schematics, with the initial concept schematic provided by Chad. Each successive schematic is a revision of the previous one, as the team realized additional problems and/or simplifications, and the resulting design grew in complexity and functionality.

Due to the complexity of the overall design and the existence of separate, distinct portions within the design, it is easiest to break up the project into simpler, more manageable circuits for specific descriptions. This section will discuss the main functional blocks that can be seen in the block diagram in Figure 1 below.

Figure 1: Top Level Block Diagram, Channel 1 of 4

Note: The design specifications require having four identical circuits, or channels, on one single PCB, in order to potentially provide power to four instruments simultaneously through the one circuit board. The design, by result, requires a variety of small-package surface mount parts, creating a significant design issue to be discussed throughout this section.
**Isolation Relay:**

**Approach:**
This component is required to galvanically isolate the power source from the load-switching circuit when need be. This allows complete isolation in the event of flooding at the load. The isolation relay is located prior to the circuit breaker in the schematic, and is controlled by a PIC signal. This allows a small control signal (3.3V at 100mA) to switch our larger channel voltage. The relay is just one step in the circuit design that is intended to operate as a user controllable isolation method.

**Design:**
The primary coil rating is low since constant current is needed to maintain channel operation. As a result, there is low power consumption while load is under constant current operation. Optimal relay design would have two-pull functionality so that a control signal would be needed to turn on the relay, and a separate signal to turn off the relay. This option was looked into extensively, with no results. Many devices met individual relay requirements, but none could be found to support our specific needs. Since the application required small components, yet needed medium voltage load-switching capability, the only relay we found was single pull, and bulky. This component provides adequate operational characteristics for our circuit, so for testing...
and prototyping purposes it worked well. MBARI has planned to further investigate relay options, but are content with the current selection. The finalized design of the isolation relay section can be seen below in Figure 2.

![Isolation Relay Schematic](image)

Figure 2: Isolation Relay Schematic
Circuit Breaker:

Approach:
The main purpose of the soft start and circuit breaker is to prevent high in-rush current from the power supply. The idea to use an IC to regulate in-rush current was dismissed since constant operation would require the component to handle a continual 194W. To simplify this approach, the design consisted of a power diode with an RC timing circuit. The circuit breaker component is required to handle the maximum load voltage and current, with some room for possible over-voltage and over-current conditions. Since we have surge detection and over-voltage monitoring, it would not make sense to rate our components based on steady state values. The best choice to perform fast switching and circuit isolation was a power MOSFET. These components are capable of 60V and 5A loads, which allow room for trip conditions.

Design:
The circuit breaker component to our schematic was designed to be controlled by a PIC signal, or D flip-flop output. Since these control methods are only capable of low current sourcing, a P and an N junction power MOSFET was used to allow source to
drain current to flow when circuit is under proper operation. The D flip-flop is set up to supply a positive voltage to the gate of the N MOS, which then creates a positive n-channel between source and drain. When this channel is active, the load can see the power supply voltage. Upon a trip condition, the D flip flop will drop to a low state, and the N-channel will no longer be conducting. This digital control circuitry will be discussed more thoroughly in the Digital Control section later. The soft start attached just prior to the input of the power MOS, theoretically ensures no damage to the MOS from high in-rush current. The final design for the circuit breaker section (and soft start) can be seen below in Figure 3.

![Figure 3: Circuit Breaker Schematic](image-url)
Current and Voltage Sensing Circuitry:

**Figure** Error! No text of specified style in document.-c: Updated Design Flow

**Approach:**

Any device being powered by this board must have the correct power characteristics supplied to it. In order to assure safe operation, these instruments must have the proper voltage and currents for their entire duration of use, and no current or voltage supplied when off. To meet these criteria, three main conditions will continually be sensed on the load line:

1. Voltage
2. Steady State Current
3. Surge Current

**Design:**

1. Voltage: In order to accurately sense voltage up to 48V, the load voltage must be scaled down. This can easily be done with a resistive divider. To maximize the accuracy of our measurements, it necessary to have the maximum output of this divider approach the voltage rail for the succeeding circuitry; this will ensure a maximum scale. As discussed in the next section, the selected voltage rail is 5V.

Therefore, the voltage divider will have to divide the voltage by about 10, or scaling
it down to roughly 10% of its actual value on the load. A basic voltage divider is shown in Figure 4 below, where

\[ V_{out} = \left( \frac{R_2}{R_1 + R_2} \right) \times V_{in} \]

![Figure 4: Basic Voltage Divider](image)

2. Steady State Current: The most effective package for this purpose, called a Current Sense Amplifier, was used to measure the voltage drop across a known resistance, called the Current Sense Resistor.

As this resistor is located directly on the load line, it will have a voltage drop across it, based on Ohm’s Law: \( V = IR \). This results in a very accurate voltage representation of the current flowing to the load. Therefore, to minimize voltage loss across the resistor (and therefore supply the load with the most accurate voltage), an extremely small resistance is required. For these types of applications, Kelvin Resistors, an example of which can be seen in Figure 5, are commonly used (recommended by Professor Prodanov).
Figure 5: Kelvin Resistor
These resistors have four terminals, which allow current to flow directly through the resistor, allowing the Current Sense Amplifier to sense the voltage drop without being damaged by potentially high currents.

For the selection of a particular Current Sense Amplifier, the following considerations were made:

a. The expected voltage range of the circuit is 24-48V.
b. The amplifier should be able to run off of the selected 5V rail.
c. The output of the Amplifier should be a scaled voltage (within 5V rail) to represent the current, whose range is 0-4A.
d. As recommended in Appendix C, a Maxim IC part will be sought.
e. With component size as an issue, a surface mount parts are ideal.

After a careful parts search, the MAX4080/4081 series was selected, and meets all the conditions listed above. Within this amplifier series, different options include various gains on the output, and the availability of a bidirectional input/output. As this design only deals with positive voltages and currents, the MAX4080 would suffice.

To select the gain (available gains were $A_v = 5, 20, \text{ or } 60$), the following formula was obtained from the datasheet:

$$V_{out} = R_{sense} \times I_{load-max} \times A_v.$$
Again, looking for a maximum output voltage (limited by the 5V rail) for the most accurate scale, the following values were selected:

\[ R_{\text{sense}} = 20\text{m}\Omega, \, I_{\text{load-max}} = 4\text{A}, \, A_v = 60, \, \text{for a } V_{\text{out}} = 4.8\text{V}. \]

The resulting part is MAX4080SASA. This gives the largest possible range for load values, which results in the most accurate readout.

3. Surge Current: The surge current circuitry is extremely similar to that of the steady state circuit, with one major exception. As an instrument could have a built up capacitance when being powered up, it is possible to have a negative surge being fed back into the circuit from the load. Conveniently, the MAX4081 is designed to be bidirectional, with the addition of an adjustable reference for the output voltage. This functionality allows for both positive and negative currents to be sensed, but only have a positive voltage output if referenced and scaled correctly. This is extremely important, as the Current Sense Amp must be able to perform within the 0-5V rails.

The functional requirements call out for surges no greater than +/- 10A. The following formula, obtained from the datasheet, was used to select the particular amplifier:

\[ V_{\text{out}} = V_{\text{ref}} +/- (R_{\text{sense}} \times I_{\text{load-max}} \times A_v). \]

With a symmetrical expectation for current at the input, \( V_{\text{ref}} = 2.5\text{V} \) was the logical selection, being halfway up the 5V rail.

The following components were selected, again with a full scale output in mind:

\[ R_{\text{sense}} = 10\text{m}\Omega, \, I_{\text{load-max}} = +/- 10\text{A}, \, A_v = 20, \, \text{for a } V_{\text{out}} = .5 - 4.5\text{V} \]

The resulting part is MAX4081TASA.
For specific parts for the sense resistors, the LVK series was chosen based on their available sizes (surface mount) and resistance values.

**Signal Filters:**

![Diagram](https://via.placeholder.com/150)

*Figure* Error! No text of specified style in document.-d: Updated Design Flow

The signals outputted from the current and voltage sensing circuitry are simply scaled versions of the source voltage to the scientific instruments and therefore could contain switching components from the main DC-DC converter. In order prevent unwanted trip conditions due to voltage/current spikes, these signals are low passed filtered. Each of the three signals is unique, however, and the use of three unique filters is necessary.

1. **Voltage:** From the voltage detection circuitry, a 10% scaled voltage reading is provided with an output of 0-5V.

This voltage should be a relatively constant DC voltage, so any high frequency noise on the signal needs to be filtered out. This is done using a low pass filter, a passive version of which is shown below in Figure 6.
With low frequency signals, the capacitor has time to charge and discharge, and can effectively mirror the input signal at the output. At high frequencies, however, the capacitor does not have to charge, and acts as a short circuit to ground, effectively blocking the input signal entirely. The specific frequency that defines when these two actions occur is called the break frequency. The cutoff frequency \( f_c \) is the inverse of the time constant, \( \tau \), which is defined as the product of the resistor and capacitor values:

\[
1/f_c = \tau = RC
\]

This basic circuit, however, does not have the capability to drive other circuitry, and the addition of active elements is needed.

Shown below in Figure 7 is a 2\(^{nd}\) order low pass filter in the Sallen-Key structure.

\[\text{Figure 6: Passive Low Pass Filter}\]

\[\text{Figure 7: Sallen-Key 2nd Order Low Pass Filter}\]
This particular filter is an excellent choice for this application because of its relative simplicity (just one op-amp, 2 capacitors and 2 resistors), and has an abrupt frequency response (defined by $Q$) at the cutoff frequency ($f_c$):

$$f_c = \frac{1}{2\pi \sqrt{R_1 R_2 C_1 C_2}}$$

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{C_2 (R_1 + R_2)}$$

The corner frequency, then, is the determining factor as to exactly what portions of the signal make it through to the next stage, and the determination of which is discussed in the testing section. Also discussed in the testing section, this filter cannot be driven by the basic resistive divider from the voltage detection circuitry. This is due to the filter having a high input impedance, and requires being driven by a device with high output impedance. A unity gain buffer has a high output impedance and can effectively drive a filter.

The above filter was also later upgraded later to a 3rd order low pass filter, by simply adding a 1st order filter with the same cutoff frequency in front of the existing filter. This further ensured a smoothed version of the input voltage at the output.

2. Steady State Current: The filter design for the steady state current precisely follows that of the voltage reading. The output of the current sense amplifier for this stage is a steady DC voltage, between 0-5V, and is potentially only tainted by high frequency noise.

The only difference between this and the circuitry discussed for voltage is the preceding circuitry driving it. Recall that the voltage circuitry needed to be driven by a buffer with a high output impedance. In the steady state current circuitry, however, the current sense amplifier conveniently has a buffer built into its output with drive
capability in mind. The low pass filter for the steady state current, then, is identical to that of the voltage with exception to the external driving buffer.

The cutoff frequencies are designed to be identical as well, although that particular value is not completely critical to the operation of these filters. An ideal DC signal has no frequency, and therefore any corner frequency set by these filters, within reason (greater than, say, 10Hz), would allow the DC content to pass through. The criteria for setting the corner frequencies is discussed later.

3. Surge Current: The surge current filtering presents a different issue than the previous filters discussed. Instead of seeking low frequency, DC content, the surge current circuitry needs to respond to fast changing, higher frequency current surges. Professor Prodanov suggested utilizing a high pass filter to only admit that high frequency content through to its next circuit stage. A high pass filter, shown below in Figure 8, utilizes the same basic concepts discussed earlier with the low pass filter, but their functions are switched:

![Figure 8: Passive High Pass Filter](image)

Again, at high frequencies, the capacitor acts as a short circuit. However, the capacitor now acts a short from input to output, not output to ground. This circuit, then, serves to admit only high frequencies, and the low frequency signals are lost across the resistor to ground.
For the same reasons as in the low pass filters, a sharp frequency response defines a clean attenuation at the cutoff frequency, and another Sallen-Key structure, shown in Figure 9 below, is used:

![Sallen-Key 2nd Order High Pass Filter](image)

**Figure 9: Sallen-Key 2nd Order High Pass Filter**
The structure is identical to that of its low pass counterpart, with the positioning of the resistors and capacitors switched. The similarities between the circuits go even further, with the defining equations for the cutoff frequency and Q factor being the same as well.

In order to be a completely safe design, every portion of the current should be seen by a portion of the circuitry; that is, ensuring that every part of the current signal is measured, will ensure that no current could pass through the circuit into an instrument undetected. Recall that for the low pass filters, the corner frequency value was not critical to the functionality of the filters (as long as it was set to greater than 10Hz). With the above reasoning, the low pass filters should have a corner frequency that is complimentary, or identical to, that of the high pass filter. This will ensure that no part of the signal will go undetected.

Therefore, the corner frequencies of all three filters will be the same, but exactly which frequency needs to be determined. Upon inquiry, Chad advised to plan for a
current surge lasting no longer than 10ms in duration. As frequency is inversely related to time \((1/t = f)\), this dictated a recommended corner frequency, \(f_c = 100\text{Hz}\).

Note: The operational amplifiers used in all of the above filters came by direct recommendation of Chad; he had used them before and their electrical characteristics met our requirements. Most importantly, they are rail-to-rail, low power, surface mount parts: AD8603 (single) and AD8607 (dual package).

**Comparators:**

![Diagram of Design Flow]

Part of the requirements for the overall design is to have the four tripping conditions be “user programmable.” This is accomplished by having the filtered signals feed into respective comparators, with reference values set directly by the PIC Microcontroller.

It is desired, however, to have minimized logic within the microcontroller (as per design suggestions by Chad), and digital potentiometers were suggested to set the reference voltage. Potentiometers act as a voltage divider from the 5V rail to ground; the use of digital pots, which communicate directly with the PIC through an SPI bus,

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1. So far in the design flow, the voltage portion of the circuit has been a single signal representing two possible trip conditions: over voltage and under voltage.
effectively set the reference voltages to the comparators while maintaining the desired user programmable functionality.

Note: This section on comparators signifies the end of the analog portion of the design. The comparators effectively check time-varying signals at their input against their respective reference levels, and output a digital 1 (V = 5V rail) or 0 (V = 0V), as designed.

Again, the design will be discussed according to the different sensed conditions:

1. **Voltage**: As mentioned earlier, the voltage that has been sensed, scaled, and smoothed out, is to be used to activate two tripping conditions: over voltage and under voltage. For the over voltage condition, it is desired for the circuitry to activate a “trip” (or output a digital logic high) when the sensed voltage goes over the desired voltage by a certain margin; this margin is set by the potentiometers. Similarly, the under voltage condition is to activate a trip when the sensed voltage goes under the desired voltage by the specified margin.

Typically, window comparators, an example is shown in Figure 10 below, are used in such situations when a signal is expected to be within a certain “window” or voltage range.

![Figure 10: Typical Window Comparator](image)
Window comparators typically send out a logic high when the sensed voltage is within the specified margins. However, this circuit requires the opposite response: when the voltage is within the margins, the circuit’s voltage reading is acceptable, and the circuit should be allowed to continue to operate. It is when the voltage is located outside the margins that a logic high should be outputted. This change is made easily to the window comparator, by simply switching the position of the two reference levels, and tying the opposite inputs together.

For added functionality, the outputs of each comparator feed to the PIC directly. This functionality allows the PIC to know exactly which trip condition was activated in real time.

2. Steady State Current: For the steady state current, an identical approach is taken. A comparator with a user-defined reference is tied to the sensed voltage value representing the steady state current. If the current reading rises above this reference, the comparator will output a logic high tripping signal. Also, as in the voltage circuitry, this output signal is tied directly to the PIC for real time monitoring.

3. Surge Current: Again, a similar approach is used. However, an added issue is present in the surge current portion of the circuit, as a high pass filter provides the signal to this particular comparator. High pass filters, by design, take out the DC bias that may be present in the signal. A DC bias was introduced by the current sense amplifier for this circuit by design, as the amplifier was set to sense for possible positive and negative current surges. However, this portion of the circuit does not care which type of surge is present in the circuitry: as long as the design effectively shuts down power
supplied to the load in the event of current surge, the polarity of the current surge is irrelevant.

Therefore, a comparator setup identical to the steady state current portion can be implemented: If the sensed current (scaled and represented by voltage) rises above the user defined value, the comparator will output a logic high tripping condition.

Part Selection: The factors for selecting particular parts for the comparators section of the design are similar to those of the rest of the design: small surface mount parts are ideal and a fast response is preferred. Also, as the comparators will be outputting a logic low (ideally, because logic highs represent unwanted circuit conditions) for most of the time, devices that consume little power when outputting a low output add a degree of power saving in a circuit growing in parts and complexity.

**Digital Circuitry:**

![Updated Design Flow](image)

*Figure Error! No text of specified style in document.*

At this point, the sensing circuitry is set up to send out a digital logic high if any of the tripping conditions are met: over voltage, under voltage, steady state current, and surge current. As discussed earlier in the circuit breaker section, the circuit breaker is turned off (no power is supplied to the load) when the digital circuitry outputs low.
Therefore, a digital solution needs to be implemented to pull the N-channel of the circuit breaker low if any of the trip conditions go high.

The following digital setup, shown below in Figure 11, is implemented to perform the previously described functionality.

This setup was recommended directly by Chad, who insisted on using discrete parts, not digital logic, to implement the described logic functions. Implementing the circuit breaker control circuitry in hardware increases reliability should there be a problem with the firmware in the microcontroller.

Starting from the right side of the schematic, the four trip conditions are fed into an OR gate. Logic OR gates are designed to output a logic high if one (or more) of the
inputs goes high. This effectively combines the four trip conditions into one signal, which will go high if any (one, multiple, or all) of the trip conditions are met.

This signal is then tied into a tri-state buffer. Tri-state buffers act like either a buffer (short circuit connection), or an open circuit (high impedance), depending on the status of the control signal. This particular buffer, being active high, allows the signal to pass through if and only if the control signal goes high. If the control signal goes low, the buffer will turn off, and output nothing.

The buffer then feeds the clock input of a D-Flip Flop. This D-Flip Flop is an edge triggered flip flop, which means it will only act on the input signal (D), when it sees a rising edge on the clock input. As D is tied high to the 5V rail, the flip flop is designed to output 5V at the Q output, and 0V at the Q(not) output, in normal operation, whenever the clock input sees a rising edge. Coming from the buffer, the clock input will see a rising edge immediately if a trip condition is met. As described earlier, to turn off the circuit breaker, the N-channel must be held to 0V to turn off. It can be seen in the schematic in Figure 9 that the Q(not) output, is used to drive the N-channel. This Q(not) output also drives one of the inputs to the AND gate.

The AND gate serves to set the control signal on the tri-state buffer mentioned earlier. AND gates are designed to output a logic high if and only if both inputs are a logic high. Therefore, for the buffer to work, both inputs must be 5V. As previously mentioned, the Q(not) will output 5V, so long as no trip conditions are met in the circuit, allowing for normal circuit operation. The other input to the AND gate is from a signal in the PIC. This signal is coded to output a high 5V in typical operation, and
only output low if one of the trip conditions is met. This PIC signal is also sent to the active low CLR (clear) signal on the D-Flip Flop. Consequently, whenever a trip condition is met, it resets the flip flop to allow for another signal to be read.

**ADC:**

The Analog to Digital Converter serves to provide accurate digital feedback of the current and voltage levels to the PIC, and by extension to the user. According to the supplied design requirements, the chosen ADC must meet the following conditions:

a. It must be able to operate within the 0-5V rail.

b. It must have at least 3 input channels, for voltage, steady state current, and surge current readouts.

c. It must have at least a 12bit resolution.

d. It must output data in an SPI.
As can be seen in the block diagram of Figure 1-g, the inputs to the ADC are fed in from the outputs of the signal filters, which are real time, scaled readings of the voltage and current running to the load.

**PIC24F Microcontroller:**

The PIC24F Microcontroller was one of the few absolute requirements provided at the outset of the project. This is to ensure a smooth integration of this board with the rest of the circuit boards operating in the FOCE project. For our design, the PIC input and output signals (I/O) are:

RELAY_01_ACT (O) - Turn relay on or off
RELAY_01_STATE (I) – Show user the current relay state
CKT_BRKR_01_STATE (I) – Show user the current circuit breaker state
CKT_BRKR_01_RST (O) – Sets or resets current circuit breaker state

*Figure 1-h: Final Design Flow*
CHAN_01_CU(R (I) – Shows steady state current values represented by voltage
CHAN_01_VOL(T (I) – Shows representation of steady state load voltage
CHAN_01_OC (I) – Shows when an over-current trip condition has occurred
POT_01_P0W (O) – Sets trip condition on comparator for steady state current
CHAN_01_SG (I) – Indicates when a surge trip condition has occurred
POT_01_P1W (O) – Sets trip condition reference on comparator for surge detection
CHAN_01_OV (I) – Indicates when an over-voltage trip condition has occurred
POT_01_P2W (O) – Sets trip condition on comparator for over-voltage
CHAN_01_UV (I) – Indicates when an under-voltage trip condition has occurred
POT_01_P3W (O) – Sets trip condition on comparator for under-voltage
V. TESTING:

The PIC24F chip and code selection have not been finalized, therefore SPI based components were not tested in our design stage. This included the ADC output and quad digital potentiometer output. However, input (I) signals to the PIC were tested with a current limiting resistor and LED in series to ground. This allowed a visual indication of a high signal. Also, PIC output (O) signals were simulated by a current limited 5V DC power supply.

Signal Filters:

Filter design relied primarily on corner frequency set by surge levels. All steady state values were sent through a low pass filter to minimize noise from an inconsistent load. This ensured accurate DC values from our current sense amplifiers. Early design consisted of a simple first order passive filter. Testing proved that this design would suffice for the low pass filters, but in order to maintain circuit integrity, a buffered 3rd order filter was later chosen to provide distinct cutoff frequencies. Since surge possibilities reside on both load and supply ends, a bidirectional current sense amp was used with a 2.5V offset. This allows a surge to be detected from either direction by sending the resulting AC waveform through an absolute value circuit and into the high pass filter; because the filter removes dc biasing, the resulting RMS value that passed through can be read by a comparator. The AC value that passes through the filter represents surge intensity. This method of filter design to capture AC signal
characteristics allows an exact surge frequency to be set with passive resistor and capacitor values. Therefore, a single potentiometer can easily alter trip conditions.

**Comparator Trip Conditions:**

Prior to circuit breaker completion for the load switching channel, the optical isolation relay was used with the comparators to test over voltage, under voltage, and steady state current. An electronic load machine was used to sink current, with the relay positioned between the current sense resistor and the supply voltage. The primary coils on the relay were connected to the source and drain of a P MOS. The gate was connected directly to the output of the comparators. This allowed a trip condition (high signal from comparator) to turn the relay off. Each condition was tested separately and the relay operated as a circuit breaker upon a trip condition.

Since the actual trip levels are intended to be user programmable and unique for each FOCE attachment, arbitrary values were used as conditions. In order to maintain consistent results and avoid signal bouncing, 75mV hysteresis was used on our comparators. This was easily added on the reference pin, which determines the hysteresis based on the amount of current sink between reference and ground. This design in specific to this type of comparator since it is an ultra-low power component.

As noted previously, power consumption during circuit operation was constantly in mind, and emphatically kept to a minimum where possible. Therefore large resistors were chosen (2MΩ) to set required hysteresis. Since over and under voltage detection
could be very specific for more delicate loads, a trip condition has 0.75V cushion between sending another high output and returning to the proper operating state.

**Surge Detection:**

The hefty single pull relay proved to be optimal for testing surge detection. Since our surge detection occurs across our current sense amplifier, a load to pull current was required. The issue is the power supply capable of sourcing 3A is DC only, and a sharp wave is required to simulate surge conditions (since it contains AC characteristics). This sharp voltage spike, called a burst, is available on function generators, but they are not capable of supplying the current required by our load. Therefore the 20V 3A testing conditions were applied to the main channel on the relay, which is capable of 60V 10A, and the burst function was attached to the primary coils of the relay. This allowed the Burst function to control the relay, and therefore the power to the load. This test required a testing frequency, which was set to 100Hz. This means any wave characteristic resembling a frequency greater than 100Hz is to be considered a surge. The optical relay was very capable at handling high frequency switching. The test was implemented by connecting our current sense amplifier and current sense Kelvin resistor with our 3rd order Butterworth high pass filter. Upon sensing a change in current, the high pass filter would receive a corresponding voltage signal. If this signal met or surpassed our surge level frequency, it would pass any resulting AC signal through the high pass filter. Since any DC signal is blocked by the high pass filter, the comparator following the filter
would see a voltage anywhere from 100mV to 2V whenever a surge occurs. When a reference level is set on the comparator, any surge can be detected. More testing showed that negative AC components (representing a surge from a capacitive load) were not being passed through. This problem conjured many different options, and was the initial reason for us choosing the bidirectional MAX4081. Early deliberation suggested a precision full-wave rectifier to implement an absolute value on the surge level, which could then be detected by the same comparator reference as a positive surge. This option typically requires a negative rail though, which was not available to us in this stage of design. Initially there was no negative rail available on the FOCE backplane, until Mr. Kecy decided it was imperative to the surge detection circuitry. His finalized design, as seen in the final schematic, utilizes the negative rail to supply a positive and negative referenced window comparator within the AD633. These outputs, unlike a typical comparator that outputs a digital high or low, will effectively output the exact value at the input if it fits outside the window. Any negative voltage will be rectified and made positive. This is then fed into the high pass filter circuitry then comparator, as previously planned. Since surge pulses have a very low duration, a latch was used (74LVC74) to hold the trip indication high until the PIC signal CKT_BRKR_01_RST resets the trip. This finalized aspect of the circuit was implemented and tested at MBARI by Mr. Kecy.
Soft Start & Circuit Breaker

The concept of a soft start led us to believe a linear regulator would be our best choice, but further research proved us wrong. The linear regulator concept was not practical because it would require a small voltage drop between supply and load. Although a known, constant voltage drop is possible to work around, we did not want to supply extra voltage at the input just to see the proper expected voltage at the load. In order to avoid elaborate design Mr. Kecy recommended a simple RC circuit for ramping functionality. As the capacitor charges, the source input is limited, but upon full charge of the capacitor, the entire input voltage can be seen by the load. This was calculated to be 10ms for preliminary testing purposes, which is a much slower rise than that of a surge detection level, to insure the ramping of the input did not trigger a trip condition. The soft start circuitry is positioned after the relay and before the circuit breaker, and the ramping of our input signal can be seen in our oscilloscope capture below in Figure 12.

Figure 12: Oscilloscope Capture of Soft Start Ramp
The power MOS proved to be a reliable method to control large load switching with a small control signal. MBARI has previous experience with implementing power MOSFETS for circuit breaker control, and their recommendations proved perfect for our circuit. We tested ramping conditions with a load sinking current. The values currently in use on Mr. Kecy’s design are a 25k resistor and 2.2uF cap. This produces a time constant of 18ms.
VI. CONCLUSIONS AND RECOMMENDATIONS

This Senior Project, again, is a redesign of a portion of the electrical system currently deployed in the FOCE project at MBARI. As the main goal of the project was to design, implement, and test a functional circuit, the project was certainly a success; through intensive research, direct consulting with Professor Prodanov and Mr. Kecy, and hours of assembly and testing, a carefully designed and thoroughly tested circuit design has been produced.

As for recommendations, all of the ongoing work for the Medium Voltage Load Switcher has been noted in the testing section. As indicated, the final design for the board will still require some additional tweaks and changes, as determined by further testing of the circuitry on the initial prototypes of the design.

As a result of this collaborative process, the aforementioned design will now be handed over to MBARI, and the project will transition from its collaborative nature with Cal Poly, to final prototyping and implementation by Mr. Kecy at MBARI.
VII. BIBLIOGRAPHY


5. Kecy, Chad. Electrical Engineer, Monterey Bay Aquarium Research Institute.

6. Prodanov, Vladimir, PhD. Assistant Professor, Electrical Engineering Department, California Polytechnic State University.

APPENDIX A: FUNCTIONAL DESCRIPTION

“FOCE Medium Voltage Load Switcher Functional Description

The MV Load Switcher is a modular circuit board meant to plug into the existing FOCE Chassis backplane. It will occupy one of the eight daughter slots on the backplane.

It is used to provide power to scientific instruments attached to FOCE which operate in the voltage range of 24V to 48V and up to 4A. The MV Load Switcher provides four main functions: load switching, circuit breaking, load soft-start, and power monitoring.

The load switching function is provided via an electromechanical relay; this provides extremely high resistance when opened, and thus provides nearly complete electrical isolation.

The circuit breaker functionality monitors four conditions at the load (the scientific instrument): over voltage, under voltage, over current, and current surges. The over/under trip levels are usable settable via a digital potentiometer. This allows the board to be easily changed on the fly in the event of switching out instruments. The current surge detection will look for fast surges above a user programmable level. The circuit breaker will automatically trip if any of these conditions are met and can only be reset from a command from the onboard microcontroller. A latching flip-flop could be used to retain the tripped state until reset.
The soft-start functionality prevents excessive inrush currents to the loads as they are powered up. This will help to prevent temporary brown outs when powering up capacitive loads.

The power monitoring is done by sending scaled down versions of the output voltage and current to an ADC. The current is measured via a current sense amplifier and a sense resistor. The voltage is via a voltage divider and buffer amp.

The MV Load Switcher will have an onboard microcontroller (PIC24F Family). It will communicate over the backplane via SPI bus #1 and will communicate to onboard devices via SPI bus #2.

There will also be common auto-addressing circuitry which allows the board to be plugged into any of the eight daughter slots. The use of a logic (address) comparator only allows the specific daughter board to respond to commands from the main CPU board. There is also interrupt generating circuitry. This circuitry has already been designed, built, and tested (in other daughter boards).

The MV Load Switcher has four channels, each with its own input and output connectors. This allows the four loads to have four separate input voltages. Onboard solderable straps between Inputs 1 and 2 and Inputs 3 and 4 allow two outputs to be fed from one source, if desired. Each of the four inputs also has a ground fault output connector. These will be fed to the Ground Fault Detection board.
APPENDIX B: FUNCTIONAL REQUIREMENTS

FOCE Medium Voltage Load Switcher Functional Requirements

Physical Requirements

Board dimension are 3.5 inches by 6.0 inches.

Placement of the backplane connector is fixed.

No connectors or externally accessible components on bottom edge of board.

Electrical Requirements

Provide load switching and protection to four channels.

Maximum load voltage is 48V

Maximum load current is 4A.

Each load has an individual input and output connector.

Each input connector will have an ground fault output connector.

Internal board communications done by SPI.

The MV Load Switcher will have it's own PIC24F microcontroller.

Minimum ADC resolution for load voltage is 10mV

Minimum ADC resolution for load current is 1ma

Operational Requirements

Individual loads must be galvanically isolatable via relay.

Individual load voltages and currents will be acquired and stored.

Individual loads will have their own circuit breakers.
Four conditions at load will be monitored and if exceeded will trip the circuit breaker:

- Overvoltage
- Undervoltage
- Overcurrent
- Current surge

The four tripping conditions will be user programmable.

**Backplane Interface**

- Auto-Addressing circuitry common to other daughter boards.
- SPI based communication to CPU board.
- Power to MV Load Switcher from Power Board via backplane (3.3V, 5V, 12V).
- Slot specific interrupts are generated on each daughter board.”
APPENDIX C: COMPONENT SELECTION RECOMMENDATIONS

“In general, we use SMD components. I tend to use 1206 sized passives, unless board space is an issue....which it may be for this design, in which case I would go to 0805, and then to 0603. For ICs, I like the SOIC package (easier to probe), but if size is an issue, the SOP styles are handy.

Microcontroller - has to be in the PIC24F family (from Microchip) to maintain consistancy with other boards.

We may run out of digital I/O in which I would suggest a SPI based digital expander (also from Microchip).

Digital Pot - Microchip makes some, but I'm open to others.

Input/Output connectors - we use the Phoenix Combicon connectors on most of our boards.

Relays - Panasonic/PEWA is my first choice, then TYCO.

Backplane connector - It has to be a Hirose PN# PCN10-44P-2.54DS(72)

Current sense amp - Maxim IC makes a series of nice current sense amps”
APPENDIX D: PARTS LIST

1. Assorted Resistor Values, 1% tolerance
2. Assorted Surface Mount Capacitor Values, 1% tolerance
3. STS4DPF30L (4)
4. G5CA_0609 (4)
5. A04611 (4)
6. MAX4080TASA+ (4)
7. MAX4081TASA+ (4)
8. AD8607ARMZ (8)
9. AD8603AUJZ (12)
10. AD633 (4)
11. MCP6564-E/ST (16)
12. SN74LVC1G74DCUR (8)
13. SN74LVC1G332DBVR (4)
14. SN74LVC1G32DBVR (4)
15. SN74LVC1G126DCKR (8)
16. SN74LVC1G08DRLR (5)
17. PCN10-44P-2.54DS(72) (1)
18. MAX3226E (1)
19. LM317L (1)
20. LM337L (1)
21. MCP23S18-E/SO (2)
22. MCP4531-503E/ST (4)
23. ADS8341E (2)
24. ADR395B (1)
25. PIC24FJ256GA106-I/PT (1)
26. 74HC85DB (1)
27. SN74CB3Q3251 (1)
28. SN74LVC1G00DCKR (2)
29. SN74LVC125 (2)
APPENDIX E: SCHEMATICS

See Attached.
Medium Voltage Load Switcher (Chan 1/4)