THERMAL CHARACTERIZATION OF A SYSTEM ON CHIP (SoC)

BY

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Abstract:

Electronics are getting more and more advanced. Companies are designing their product to be more powerful, but at the same time they are designing them to be smaller and more user friendly. Heat becomes a major factor with the limited amount of surface area. The objective of this project is to measure the junction temperature of three system on chips (SoC) under various loading conditions and their time constant. The junction temperature was measured based on the diode's I-V linear relationship. Both calibration and measurement of the junction temperature were conducted for three different SoC packages. The measurement results can be compared with the simulation results from a thermal design program such as Icepak or Solidworks. The results can also be used to optimize the board design.

Chapter 1. Introduction

The purpose of this project is to characterize thermal performance of a system on chip (SoC). The thermal performance characterization includes the junction temperature measurement of a SoC chip in three different configurations and the time constant measurement of the SoC chip under various conditions.

A SoC is a high performance microprocessor that can be housed in many different electronic packaging forms. This enables designers to put systems on a chip that move everything from the board to an individual chip. The benefits of a SoC are to lower cost per gate. Moore's law states that in the history of computer hardware the number of transistors can inexpensively be placed on an integrated circuit will double every eighteen months. This allows for lower power consumption and faster circuit implementation. Also one of the biggest benefits of a SoC is the small physical size. They can be designed to meet the requirements of electronic manufactures specifications. A SoC can be found in everyday electronics such as computer hard drives, personal computer interfaces and wireless communications.

The project will provide a basis for comparison between different forms of electronic packaging as well as provide a starting point for improving the heat dissipation of the chip. Consumers are demanding reliable electronic devices, and heat is one of the biggest factors. Having an abundance amount of heat can be detrimental to a SoC and the electronic device.

Using the data obtained from the test a 3-D model can be made to simulate the heat transfer using a program called Solid-Works. Running a fluid dynamic simulation of the SoC attached to the printed circuit board assembly (PCBA) allows us to see the heat dissipation of the SoC. This enables us to better configure the PCBA layout to obtain optimum heat dissipation. Later in the report talks about the design of the system that obtains the thermal characteristics on the SoC as well as results and attempts to improve heat dissipation.

Chapter 2. Literature Review

Electronics have come a long way. In 1826 Georg Simon Ohm discovered what is known today as Ohms Law. Ohms Law relates voltage between two ends, the current flow between them and the resistance in the path, it is formulated as $V = IR$. This equation is used on an everyday basis for manufacturing electronics. Hard disk drives (HDD) are one of those electronic devices that have come a long way. In 1956 IBM shipped the first hard drive, it held five megabytes (MB) of data and cost about $50,000. The system was also the size of two refrigerators (Farrance, 2006.) HDD's are a self contained storage device that uses a read and write cycle. Hard drives are a non-volatile type of storage where it does not require power to retain data. Most commonly used in computers the hard drive is where all of the user's files and folders are kept.

Over the years as technology increases companies must find ways to keep their product up to date. A major way to improve electronics is to increase the intake power capabilities. Power causes significant amounts of heat, and if that heat is not dissipated correctly it can be detrimental to the device (Gurumurthi, et al, 2005.) The power dissipated is unevenly distributed, causing localized hot spots with significantly greater die temperatures. Having excessive junction temperatures reduces the reliability and lead to catastrophic failures (Heo; et al. 2003.) Reliability of a computer disk drive is of paramount importance not only to corporations with terabytes of business and financial data, but also for anyone with a personal computer (Elerath &; Shah, 2003.)

Newer technology on a hard drive consists of a system on chip (SoC.) This chip uses a powerful iterative decoding process that allows a signal to noise ratio to become unprecedented compared to earlier technology (Galbraith &; Oenning, 2008.) Unfortunately the SoC obtains a significant amount of heat due to extensive work. One of the first steps in reducing the amount of heat from the SoC is to identify the actual temperature inside the package. To measure this key parameter is difficult if not impossible to do with direct methods

as a thermocouple. One possible method is by using a silicon semiconductor known as a diode. By designing a circuit that uses a constant current applied to the diode, it can become a temperature sensor (Jaeger and Blalock, 2011.) The current applied to the temperature sensing diode must be large enough to obtain a reliable forward voltage reading, but small enough to not cause significant self-heating. By supplying a constant current to a silicon diode it is possible to get a linear equation that relates the forward voltage across the diode and temperature (Maynard, 2009.) Using a specific calibration process the diode can determine the temperature with any given forward voltage across the diode.

A possible solution to reduce the overall heat in the system on chip is to apply thermal interface materials (TIMs). TIMs are thermally conductive materials that when applied increase thermal contact conductance. This application is to increase thermal transfer efficiency (Lee, 2010). TIMs come in a couple different forms, a thermal pad or a thermal paste or grease. The thermal pads normally come as a small sheet with various thicknesses to fit your desired clearance. The thermal grease is similar in consistency to toothpaste and is packaged in a small tube (Chung, 2000.)

Along with reducing overall heat is to determine the rate at which heat is dissipated. Silicon has a thermal time constant, and this time constant is the rate that silicon absorbs and dissipates heat. To achieve this thermal time constant will be very similar to a time constant from a resistor and capacitor (RC) circuit. The time constant in an RC circuit is the rate a capacitor charges and discharges voltage. The thermal time constant of silicon will become a base for experimentation, in hopes to increase the heat dissipation rate. To lower the silicon temperatures will require the use of smart circuit design techniques (Viswnath, et al, 2000).

Chapter 3. Design and Methods

Calibration Test:

The silicon of each SoC package can be used as a temperature sensor as long as the current across the diode is constant. This leads into the calibration step of the project. Referring to the circuit shown in Figure 1, running a low constant current through the circuit establishes a linear relation between temperature (in degrees Celsius) and the voltage across the forward bias diode. Applying 15 volts to an external 150KΩ resistor in series with an external 2.8μF capacitor and the package's internal silicon diode in parallel will achieve a constant 100μA current across the diode. Applying current to the diode produces heat, but since the current applied in on a very small scale it can be assumed that the diode's heat is irrelevant. Using 3 thermocouples located on the top and bottom of the package, as well as an ambient temperature thermocouple. Steady state can be assured when all thermocouple readings are at the same temperatures. The calibration process consists of using a convection oven to heat the PCBA (printed circuit board assembly) in increments of 30°C (starting at 30°C) until reaching 120°C. At each increment, the board and package are heated to a steady state before a reading is taken. A reading consists of 3 thermocouple measurements previously mentioned as the voltage across the diode. Each reading is plotted on a graph and is analyzed for linearity. Using Microsoft Excel, a linear trend line with a calculated R^2 is used to determine the temperature inside the package with any given forward voltage across the diode.

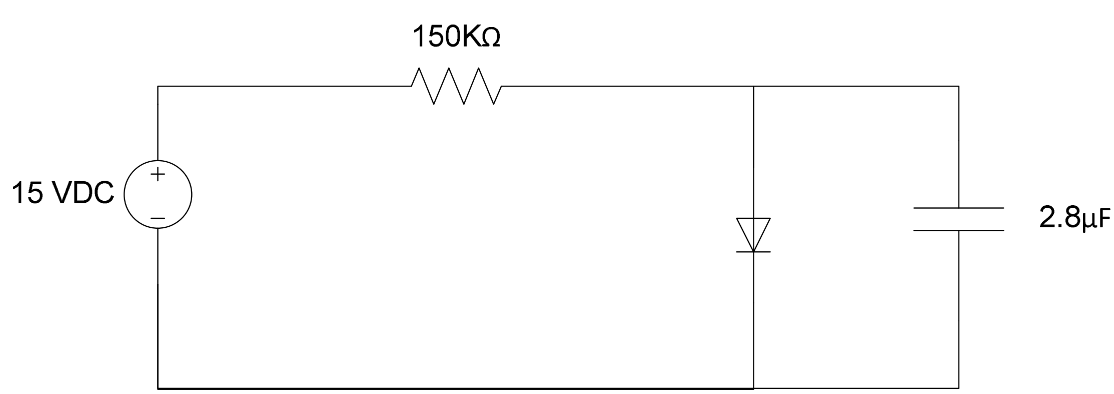

Figure 1: Circuit used for Constant Current Calibration.

The calibration step will be used for further experimental readings of the diode for each package. A rough estimate for a silicon diode used as a temperature sensor is approximately -1.8 $\frac{v}{°C}$. This approximation confirms the diode was calibrated correctly. Each diode will need to be calibrated due to different manufacturing processes and variation in package design and geometry. Individual calibration allows for precision temperature readings for each package.

Still Air Test:

The still air test is to simulate different temperatures when a power load is applied to the SoC package under a convection free environment. Figure 2 is a diagram of the package. There is a diode located in the middle of the package and it is surrounded by a series of resistors. The resistors are used to mimic a power load on the package. Applying a voltage across the resistors causes a current to flow; the current is used to heat the package. Using the data acquired from the calibration process, the package junction temperature can now be determined based on changes in the power load. Each package has specific power load requirements and cannot exceed a certain power load. Therefore Equation 1 is used to determine the voltage needed for a specific power load with a given resistance.

$$V = \sqrt{\frac{P}{R}} * R \qquad (1)$$

$V = Voltage$

$P = Power\ Load$

$R = Internal\ Resistance$

The setup for the still air test consists of using two power supplies. One power supply is used to achieve the required constant 100µA across the forward bias diode, same as the calibration

step. The other power supply is used to apply a voltage across the surrounding resistors to mimic a power load. The PCBA is screwed to the casting of the HDD assembly. The assembly is placed in the oven set at 60°C with a specific power load applied to it. Once the assembly reaches steady-state in the oven, the convection fan and oven are then turned off. Immediately after the oven is turned off, a data point is recorded every two minutes for the duration of twenty minutes (10 data points total). A data point consists of four thermocouple readings and the forward voltage across the diode. The thermocouples are placed on the top and bottom of the package, in a mounting hole of the casting and an ambient temperature reading from the convection oven itself. Using the data acquired, the thermal resistance can be calculated for each data point. The equation for thermal resistance can be seen in Equation 2. The still air test is ran for each SoC package.

$$\theta_{JA} = \frac{T_J - T_A}{P} \qquad (2)$$

$\theta_{JA} = Thermal\ Resistance$

$T_J = Junction\ Temperature\ of\ Package$

$T_A = Ambient\ Temperature$

$P = Power\ Load$

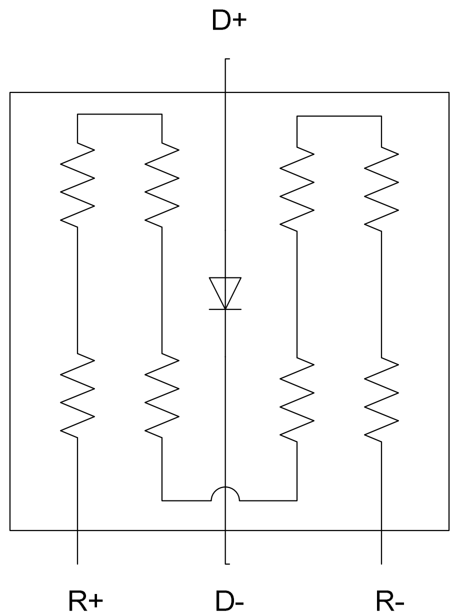

Figure 2: Package Circuit Diagram.

Forced Air Test:

The forced air test is used to determine the SoC package temperatures under various power load while in a forced air convection oven. This test is very similar to the still air test, but the power load increases and the oven's convection fan stays on. Using Equation 1 the voltages can be determined for the various power loads. Each package has a different maximum power load that it is able to withstand. Therefore the required voltages are calculated for each power load that is specific to the package without damaging the device.

The setup for the forced air test is very similar to the still air test in that they both use two power supplies for the constant current across the forward bias diode and to apply a power load to the package. The PCBAs were screwed into the aluminum casting to for the entire HDD assembly, and placed in the convection oven at 60°C. Once the assembly reached steady-state, a power load to the SoC package was applied. The voltage of the power load was incremented by 2 volts each trial and for a duration of 20 minutes elapsed before a data point was recorded to ensure a steady-state reading. The power load was incremented until the

maximum load was reached. A data point consisted of 4 thermocouple readings and the voltage across the diode. The thermocouples were placed on the top and bottom of the package, in a mounting hole of the casting, and floating mid-oven above the assembly for an ambient temperature. Similar to the still air test, the package junction temperature was calculated using the linear equation obtained by the calibration process. The thermal resistance was also calculated for each data point using Equation2.

Insulated Test:

The insulated test was designed to control the forced air velocities resulting from the convection oven, so the air in the insulated test can be treated as free/natural convection. The still air test could only eliminate some of the forced air convection. With an insulated environment, it was possible to limit unknown air velocities at the surface of the assembly and assume a free convection was occurring. This test was mainly used to dial in a 3-D model to simulate the steady-state response of the package. A key role in the simulation was to determine an overall convection coefficient, and it was impossible to achieve and accurate convection coefficient for air without limiting forced air convection. This process helped dial in the simulation for each PCBA.

The insulated test consisted of applying various power loads to the package enclosed in a Styrofoam box to control air convection. Each package would undergo power loads of ½ watt increments, starting at ½ watt, until reaching the maximum power capability of each package. Each increment in power would follow with a 20 minute waiting period until the PCBA reached steady-state. Once at a steady-state a data point was recorded. A data point consisted of 4 thermocouple readings and the voltage across the diode. The thermocouples were placed on both top and bottom of the package and 2 ambient temperatures inside the Styrofoam box. The 2 ambient temperature readings were to ensure that the thermal resistance measurements were correct with one another. It also provided assurance that steady-state was truly reached when both readings were identical. The ambient thermocouples were strategically placed to

make sure they would not be affected by increasing surface temperatures of the PCBA. If the thermocouples were affected, it would give incorrect values for the thermal resistance.

Thermal Time Constant:

The thermal time constant test was used to identify the rate at which each package can dissipate heat. It is very similar to a resistor capacitor (RC) circuit where the capacitor charges and discharges at a given rate. This rate is normally determined from an oscilloscope using a specified percentage of the maximum output. Figure 3 describes the waveform obtained from the oscilloscope. Once the time constant is determined for each package, the next step is to make adjustments in improving the rate at which the package can dissipate heat.

The thermal time constant test consisted of using a Tektronix DPO-5274 oscilloscope to capture the waveform of a power load to each package. Both power supplies from the previous tests were used. One power supply is used to obtain the constant current across the diode and the other is to apply a power load to the package. The oscilloscope is set to capture the waveform of the voltage across the forward bias diode. The oscilloscope is set to capture the waveform for 8 minutes; this is to determine that the waveform is completely saturated. The waveform must be completely saturated to accurately determine the time constant. Using the waveform, the time constant is measure by the time it takes for the waveform to reach 63% of the rising slope or 37% of the falling slope. Once the time constant is determined for each package, the casting and a thermal interface material is applied to determine if it enhances the time constant. The time constant must be taken after each adjustment to the PCBA in order to identify the increase in time constant.

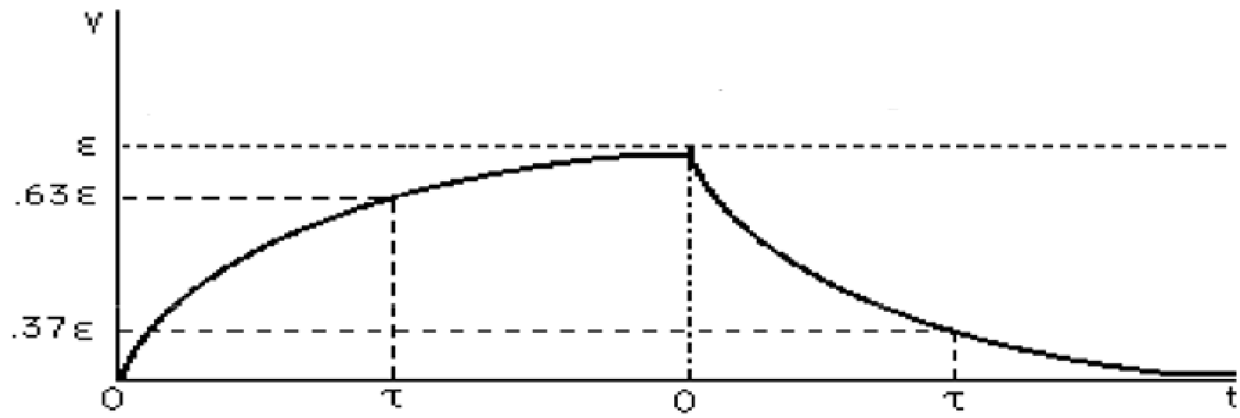

Figure 3: Time Constant Waveform.

Chapter 4. Results

The results below are for the X_1 SoC configuration. The X_1 configuration was one of three SoC packages tested. The results in Table 1 are from the calibration test. The calibration process involves varying the chamber temperature while extracting the voltage across the diode at temperature increments of 30°C. The voltage source was set at fifteen volts and is applied to a 150KΩ resistor in series with a 2.8µF capacitor and the SoC internal diode in parallel. This circuit keeps a constant current of 100 µA across the diode, and will lead to a linear relation between the voltage and temperature. Along with recording the voltage across the diode, three thermocouple measurements were recorded from the top and bottom of the encapsulation along with the ambient temperature. Figure 4 shows the linear relation between the diode voltage and temperature. This linear equation will be used to extract the junction temperature in later tests. This plot was done in Microsoft Excel and displayed is the linear equation specific to that SoC and board combination. The R^2 value confirms the results were successful. An R^2 value that is equal to 1 means that the graph is completely linear and the value that was obtained from the calibration test was 0.99994. Therefore the test was done correctly and the linear equation can be used in later testing to find the junction temperature under various conditions.

Table 2 shows the results obtained from the still air test. The still air test is run in conditions where there is no turbulent air. The power is kept constant at 1.72W and is applied to the internal resistors surrounding the SoC encapsulation. By applying the power to the SoC, this imitates the chip in use. The junction temperature is calculated by the V_diode and the equation obtained by the calibration test that is found in Figure 4. At time t=0, there is still convection in the environment and it is shown in the temperature results. The junction temperature is at 102.78°C. Once the convection is eliminated, the junction temperature increases substantially. This is expected, and shows the significance of having air flow in thermally critical situations. The casting is designed to meet certain thermal specifications, and that is the main reason a thermocouple is used to capture the temperature of the casting. The

thermal resistance (θ_{JA}) is calculated using equation 2. The thermal resistance is a heat property, and can be used to determine the heat flow for each SoC, board and casting combination. As the time increases the junction temperature decreases with no air flow. This is attributed to the physical characteristics of the SoC and PCBA being able to distribute heat. The PCBA is attached to the casting using metal screws. These screws, are able to transfer heat into the casting. As the junction temperature decreases the thermal resistance only fluctuates slightly. This shows the material heat flow is consistent.

The forced air test as seen in Table 3 also uses the internal series resistance to imitate different power loads on the SoC. Although unlike the still air test, the forced air test uses convection in the procedure. There are three total power loads applied to the SoC and the data recorded are steady state responses. Using the known internal resistance and a specific power load the voltage applied can be calculated from equation 1. As in the still air test, the diode voltage (V_Diode) is used with the linear equation from Figure 4 to obtain the junction temperature of the SoC during the forced air test. The power loads are varied from ¼ watt, 1 watt and 2.5 watts, as the power increases the junction temperature increases at an increasing rate. This is to be expected for this specific test, because heat will build up faster than the package can dissipate. As the power increases, the thermal resistance increases but then tends to plateau on the higher power loads. This can be attributed to the lower junction temperatures at the ¼ watt test. As the power load increases, the junction temperature is increasing at an increasing rate.

The insulated test is used to correlate the experimental data with the simulation data. The insulated test uses a Styrofoam box to eliminate as much turbulent air as possible. This was used to dial in a convection coefficient for simulation purposes. Solidworks was used to simulate heat transfer. It has a major emphasis on convection coefficient when running a thermal analysis. The insulated test was designed to reduce the convection coefficient, allowing for better correlation between experimental and simulation data.

The time constant was produced to determine the rate at which the SoC can dissipate heat. Each SoC package has different physical and geometrical characteristics. These

characteristics can lead to different rates the package can dissipate heat. Each package was connected to an oscilloscope and introduced a power load to the internal series resistors of the SoC. The waveform acquired is able to determine the rate at which each SoC can dissipate heat. The next step, after steady-state responses and simulations is to be able to simulate transient responses from each package.

Table1: Calibration results for Board: X_1

Chamber set (°C)	V_source (V)	i_Diode (uA)	R_series (Ω)	T1_Top (°C)	T2_Bottom (°C)	T3_Ambient (°C)	V_Diode (V)
30	15	100	58.1	34.1	34.5	34.2	0.614
60	15	100	58.1	60.8	59.3	61.8	0.562
90	15	100	58.1	89.6	88	92.2	0.5
120	15	100	58.1	119.5	117.5	123.2	0.436

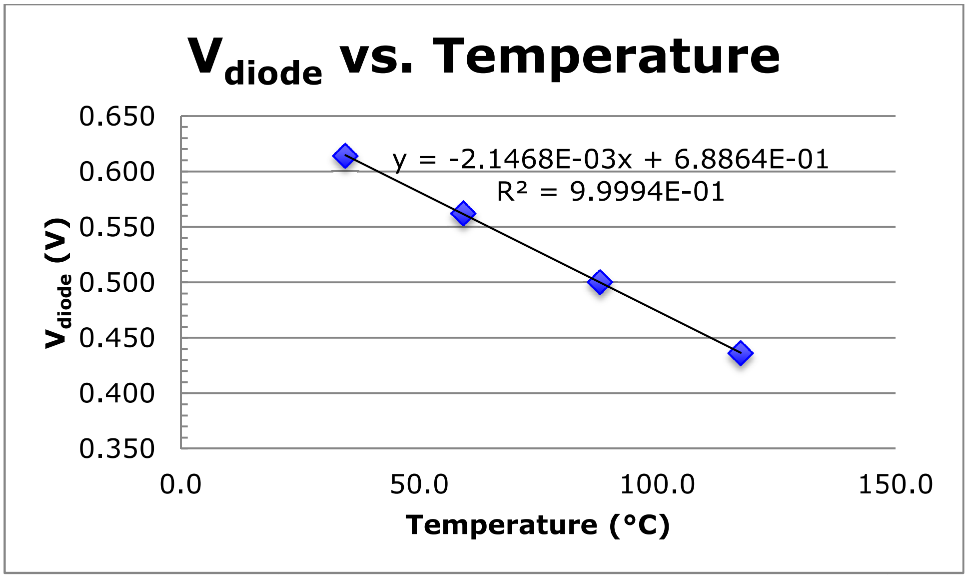

Figure 4: Calibration Plot for Board: X_1

Table 2: Still Air Results for Board: X_1

V_PS (V)	P (W)	Time Elapsed (min)	T1_Top (°C)	T2_Bottom (°C)	T3_Casting (°C)	T4_Ambient (°C)	V_Diode (V)	Junction Temp. (°C)	θJA
10.01	1.72	0	76.4	73.1	60.7	62.6	0.468	102.78	23.36
10.01	1.72	2	78.1	78.1	62	50.3	0.461	106.04	32.41
10.01	1.72	4	77.4	77.2	61	49.1	0.463	105.11	32.56
10.01	1.72	6	76.6	76.2	59.9	47.5	0.465	104.17	32.95
10.01	1.72	8	75.7	75.2	59	45.9	0.467	103.24	33.34
10.01	1.72	10	74.7	74.3	58.1	45.1	0.468	102.78	33.53
10.01	1.72	12	73.8	73.4	57	43.9	0.471	101.38	33.42
10.01	1.72	14	72.8	72.5	56	43.7	0.472	100.91	33.26
10.01	1.72	16	71.9	71.7	55	42.9	0.474	99.98	33.19
10.01	1.72	18	71.1	70.8	54.2	42.1	0.476	99.05	33.11
10.01	1.72	20	70.1	70	53.5	41.2	0.478	98.12	33.09
10.01	1.72		74.2	73.9	57.6	45.2	0.47	101.84	32.93

Table 3: Forced Air Results for Board: X_1

V_PS (V)	P (W)	R_series (Ω)	T1_Top (°C)	T2_Bottom (°C)	T3_Casting (°C)	T4_Ambient (°C)	V_Diode (V)	Junction Temp. (°C)	θJA
4	0.28	58.1	62	62.3	60.9	60.7	0.545	66.91	22.17
8	1.1	58.1	66.7	67.3	62.1	60.8	0.499	88.34	25.03
12	2.48	58.1	74.5	75.4	64	60.9	0.425	122.81	24.96

Table 4: Insulated Test Results for Board: X_1

P(W)	R(Ω)	V_PS	T1_Top (°C)	T2_Bottom (°C)	T3_Ambient (°C)	V_Diode (V)	Junction Temp. (°C)	θJA
0.25	58.3	3.82	30.5	29.3	24.8	0.615	34.43	38.52
0.5	58.3	5.4	38.5	36.4	28.1	0.591	45.9	35.60
1	58.3	7.64	54.2	49.9	34.3	0.542	69.32	35.02

Table 5: Time Constant Results for Board: X_1

SoC Package (sec)	Board with Casting (sec)	Board, Casting and TIM (sec)
0.949	0.529	0.329

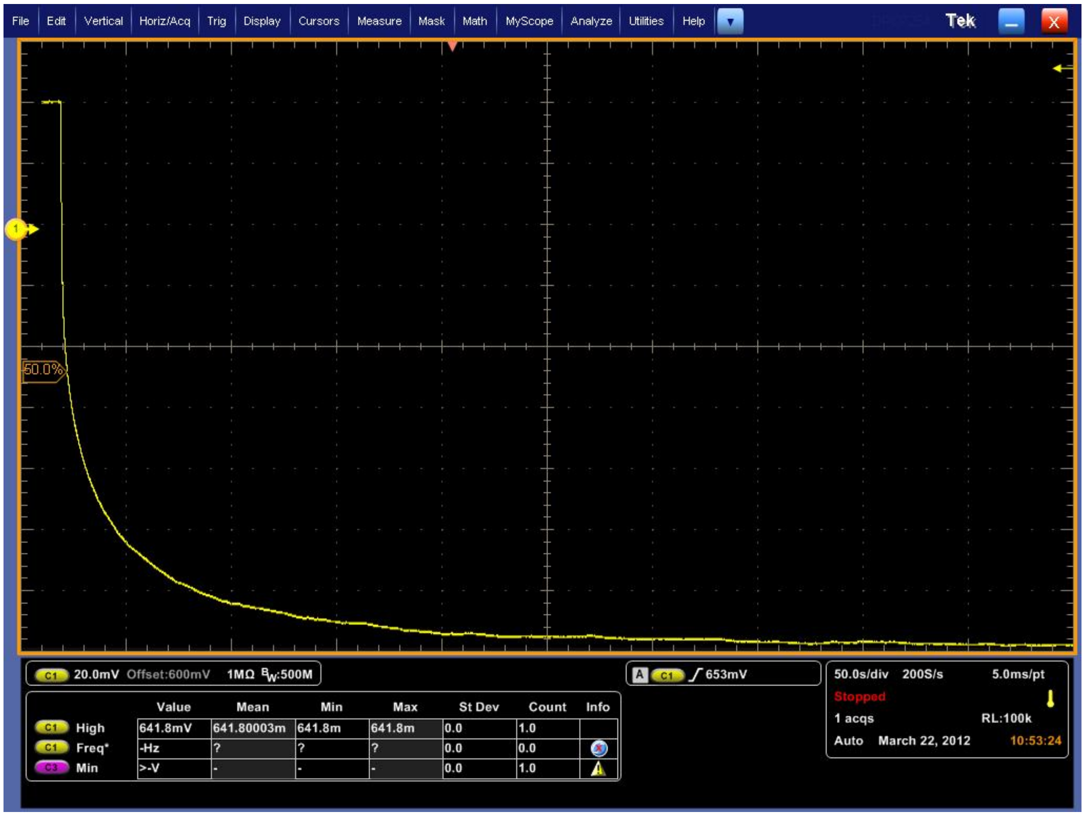

Figure 5: Time Constant Waveform for Board: X_1

Chapter 5. Conclusion

The system was designed to extract the junction temperature of a SoC with accuracy and a 3D model was created to simulate to heat distribution. Still air, forced air and insulated tests were conducted to extract the data. The data was correlated with the company to verify accuracy in the system that was designed. Overall, the experimental data collected was within 10% of the correlating data. This verifies the system designed was accurate and consistent. Although, the data collected from the still air and forced air tests were mainly for correlation purposes only. Those test results are very difficult to create a 3D model and simulate heat transfer. The data obtained from the still air and forced air tests do not entail the environmental convection coefficient. When running a thermal analysis through Solidworks, it requires a convection coefficient. If this coefficient is not very accurate, then the results are going to be difficult to correlate with the experimental data. After trying to determine the convection coefficient and not succeeding, it was time to eliminate convection altogether.

The insulated test was designed to eliminate the turbulent air inside the chamber. This would allow for a minimal convection coefficient. Therefore, this allows the ability to correlate the experimental data with the simulated data. In the simulation, the convection coefficient needs to be exact to create an accurate model. Although the still and forced air tests determined a correct system design, the insulated test was ideal in designing and simulating the 3D model. Solidworks is a 3D mechanical CAD program that allows the user to design very complex models. It also allows the user to run different design validation tools. More commonly, how the model is able to withstand physical objects and various types of straining forces. Unfortunately, Solidworks is not one of the leading programs for running thermal analysis simulations. One way to improve the simulation results would have been to create the model in a different program that specializes in thermal simulations. Ansys is a company that specializes in simulation-driven product development. They provide a program called Icepak which is powerful computational fluid dynamics software. This software specializes in thermal management of electronic devices. Icepak has significantly more thermal capabilities than Solidworks, and could produce a better simulating model overall.

The system was very accurate but also time consuming, each test could take several hours to complete. One way to improve time management would be to create a data acquisition system to extract the thermal measurements automatically. Python is a suggestion to improve the functionality of the system. It is an open source programming language that contains many modules that are free to the user. In that case, there are no licensing issues involved with using the program. The modules include ways to communicate to peripherals such as serial or GPIB ports and calculation modules very similar to Matlab. Using these modules it is possible to automatically capture the thermal measurements and create a PDF report for each test. Overall, the system was able to obtain accurate thermal measurements from each of the package and PCBA combinations. The thermal time constant was also determined to understand the data on more of a transient level as opposed to a steady state response. Although the system was able to obtain accurate results, the model was not able to create accurate simulations. If given the change to reproduce the project, it would be wise to rethink the simulation software, and use Python to automate the experimental processes.

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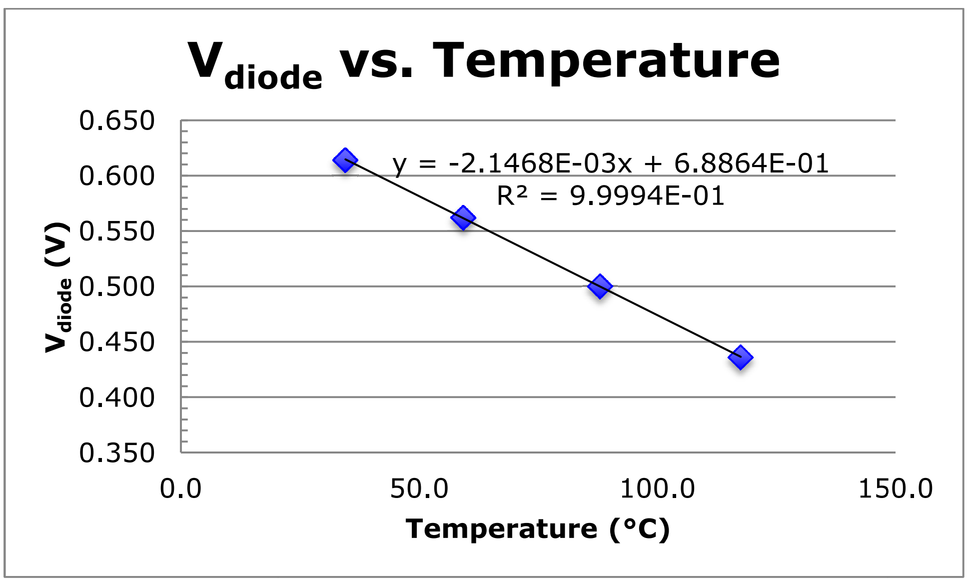

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0.5	58.3	38.5	36.4	28.1	0.591	45.9	35.60
1	58.3	54.2	49.9	34.3	0.542	69.32	35.02

Table 5: Time Constant Results for Board: X_1

SoC Package (sec)	Board with Casting (sec)	Board, Casting and TIM (sec)
0.949	0.529	0.329

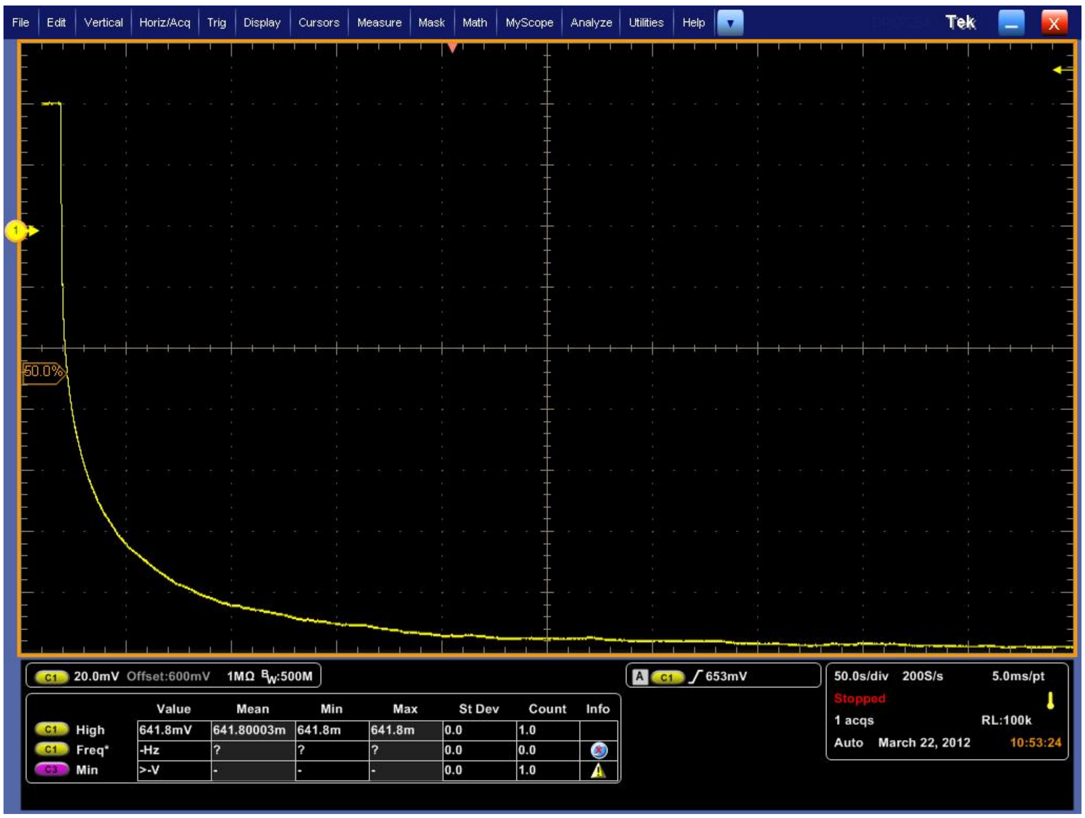

Figure 5: Time Constant Waveform for Board: X_1

Table 6: Calibration results for Board: X_2

Chamber set (°C)	V_Source (V)	i_Diode (uA)	R_Series (Ω)	T1_Top(°C)	T2_Bottom (°C)	T3_Ambient (°C)	V_Diode (V)
30	15	100	58.3	32.3	30.9	33.5	0.62
60	15	100	58.3	60.2	58.6	61.7	0.562
90	15	100	58.3	89.5	87.5	91.8	0.5
120	15	100	58.3	119.8	117.8	123	0.436

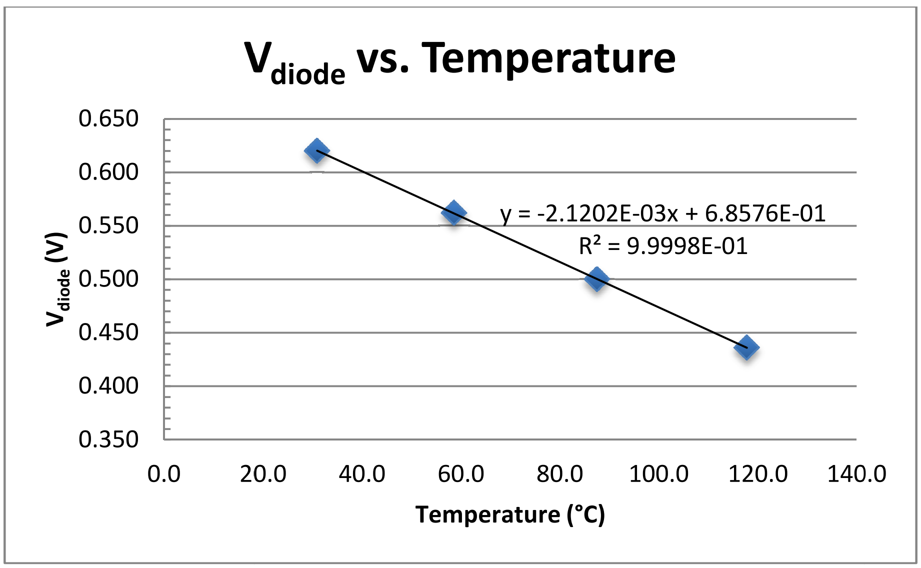

Figure 6: Calibration Plot for Board: X_2

Table 7: Still Air Results for Board: X_2

V_PS (V)	P (W)	Time Elasped (min)	T1_Top (°C)	T2_Bottom (°C)	T3_Casting (°C)	T4_Ambient (°C)	Diode (V)	Junction Temp (°C)	θJA
10.01	1.72	0	73.2	65.1	61.9	60.2	0.478	99.92	23.10
10.01	1.72	2	75.5	73.3	61.6	50	0.469	104.20	31.51
10.01	1.72	4	74.6	72.2	60.4	47.7	0.471	103.25	32.30
10.01	1.72	6	73.7	70.9	59.5	46.1	0.473	102.30	32.67
10.01	1.72	8	72.7	69.9	58.4	44.9	0.475	101.35	32.82
10.01	1.72	10	71.6	68.7	57.5	43.9	0.477	100.40	32.85
10.01	1.72	12	70.6	67.6	56.4	43.3	0.479	99.45	32.64
10.01	1.72	14	69.7	66.7	55.2	41.7	0.481	98.50	33.02
10.01	1.72	16	68.8	65.7	54.4	40.8	0.483	97.55	32.99
10.01	1.72	18	67.7	64.8	53.6	40	0.485	96.60	32.91
10.01	1.72	20	67	64.2	52.7	39.6	0.487	95.65	32.59
10.01	1.72		71.2	68.4	57	43.8	0.478	99.92	32.65

Table 8: Forced Air Results for Board: X_2

V_PS (V)	P (W)	R_Series (Ω)	T1_Top (°C)	T2_Bottom (°C)	T3_Casting (°C)	T4_Ambient (°C)	V_Diode (V)	Junction Temp (°C)	θJA
3.99	0.27	58.3	65.4	64.6	63.3	63.2	0.541	69.985	25.13
8	1.1	58.3	73	69.9	64.6	63.2	0.5	89.469	23.88
11.99	2.47	58.3	85.5	78.5	66.4	63.6	0.432	121.784	23.56

Table 9: Insulated Test Results for Board: X_2

P(W)	R(Ω)	T1_Top (°C)	T2_Bottom (°C)	T3_Ambient (°C)	V_Diode (V)	Junction Temp (°C)	θJA
0.25	58.1	30.1	28.7	24.4	0.618	33.39	35.96
0.5	58.1	38.1	35.2	26.9	0.595	44.32	34.84
1	58.1	53.1	47.1	31.6	0.551	65.23	33.63

Table 10: Time Constant Results for Board: X_2

SoC Package (sec)	Board with Casting (sec)	Board, Casting and TIM (sec)
0.961	0.538	0.339

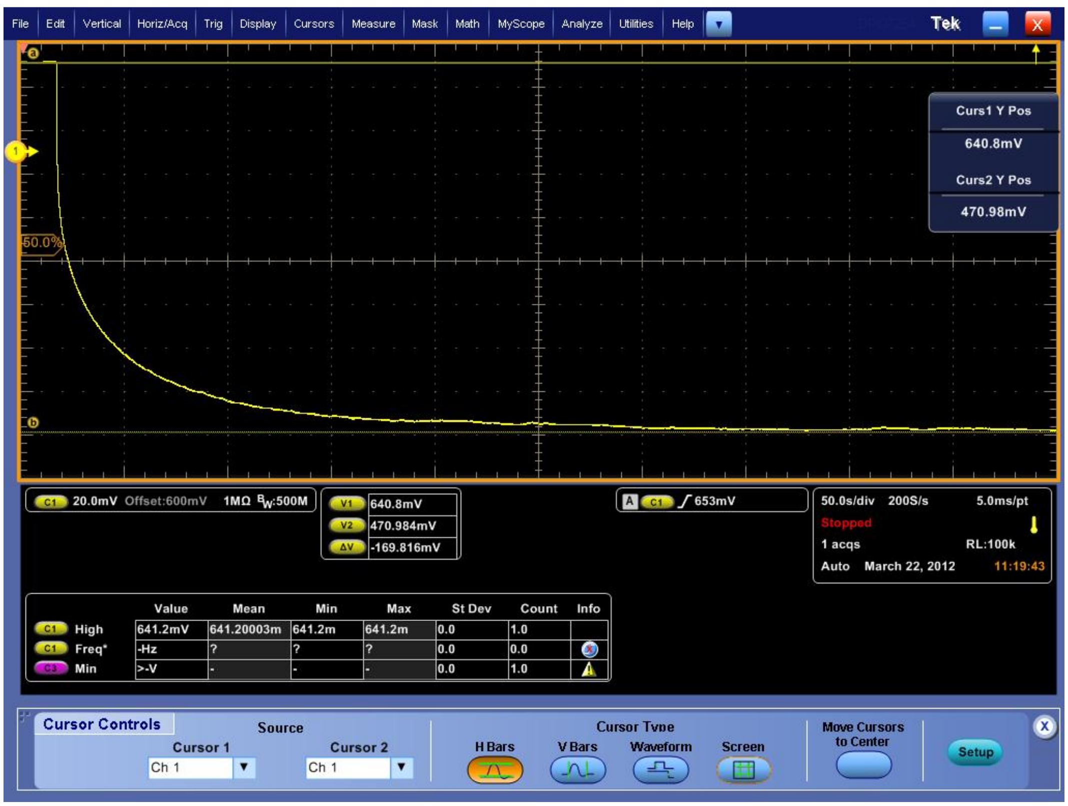

Figure 7: Time Constant Waveform for Board: X_2

Table 11: Calibration results for Board: Y_1

Chamber set (°C)	V_Source (V)	i_Diode (uA)	R_Series (Ω)	T1_Top (°C)	T2_Bottom (°C)	T3_Ambient (°C)	V_Diode (V)
30	15	100	53	29.8	29.8	29.7	0.626
60	15	100	53	61.1	61	62	0.561
90	15	100	53	92.4	92	93.7	0.495
120	15	100	53	123.4	122.9	125.4	0.428

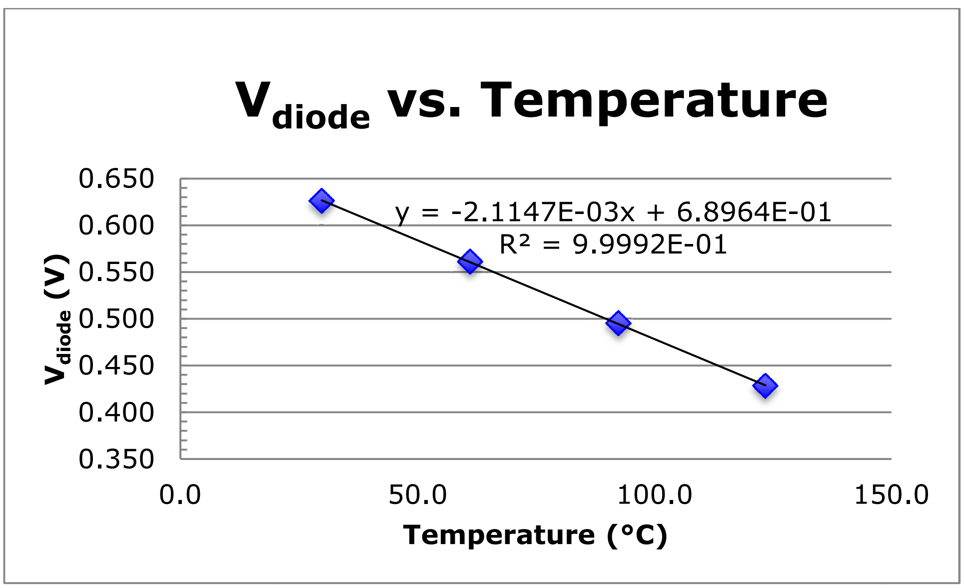

Figure 8: Calibration Plot for Board: Y_1

Table 11: Still Air Results for Board: Y_1

V_PS (V)	P (W)	Time Elasped (min)	T1_Top (°C)	T2_Bottom (°C)	T3_Casting (°C)	T4_Ambient (°C)	V_Diode (V)	Junction Temp. (°C)	θJA
10	1.89	0	70.3	69.2	63.9	63.2	0.511	84.48	11.26
10	1.89	2	73.2	73.2	63.5	51.7	0.506	86.84	18.59
10	1.89	4	72.9	72.8	62.8	49.8	0.506	86.84	19.60
10	1.89	6	72.2	72.1	62.5	49.4	0.508	85.89	19.31
10	1.89	8	71.7	71.5	61.7	48.7	0.509	85.42	19.43
10	1.89	10	71	71	61.2	47.5	0.511	84.48	19.56
10	1.89	12	70.3	70.5	60.4	46.4	0.512	84.00	19.90
10	1.89	14	69.6	69.5	59.8	45.5	0.514	83.06	19.87
10	1.89	16	68.9	69	59	44.8	0.515	82.58	19.99
10	1.89	18	68.4	68.2	58.3	43.8	0.516	82.11	20.27
10	1.89	20	67.8	67.6	57.6	43.1	0.518	81.17	20.14
10	1.89		70.6	70.5	60.7	47.1	0.512	84.00	19.53

Table 12: Forced Air Results for Board: Y_1

V_PS (V)	P (W)	R_series (Ω)	T1_Top (°C)	T2_Bottom (°C)	T3_Casting (°C)	T4_Ambient (°C)	V_Diode (V)	Junction Temp. (°C)	θJA
4	0.3	53	64.5	64.4	63.4	63.4	0.548	66.98	11.93
8	1.21	53	68.1	67.4	64	63.7	0.527	76.91	10.92
11.99	2.71	53	73.8	72	64.7	63.7	0.492	93.46	10.98

Table 13: Insulated Test Results for Board: Y_1

P(W)	R(Ω)	T1_Top (°C)	T2_Bottom (°C)	T3_Ambient (°C)	V_Diode (V)	Junction Temp (°C)	θJA
0.25	53	27.5	29.1	24.2	0.627	29.6	21.6
0.5	53	32.8	32.3	26.5	0.612	36.7	20.4
1	53	43.5	42.1	31.4	0.583	50.4	19

Table 14: Time Constant Results for Board: Y_1

SoC Package (sec)	Board with Casting (sec)	Board, Casting and TIM (sec)
3.124	1.275	0.769

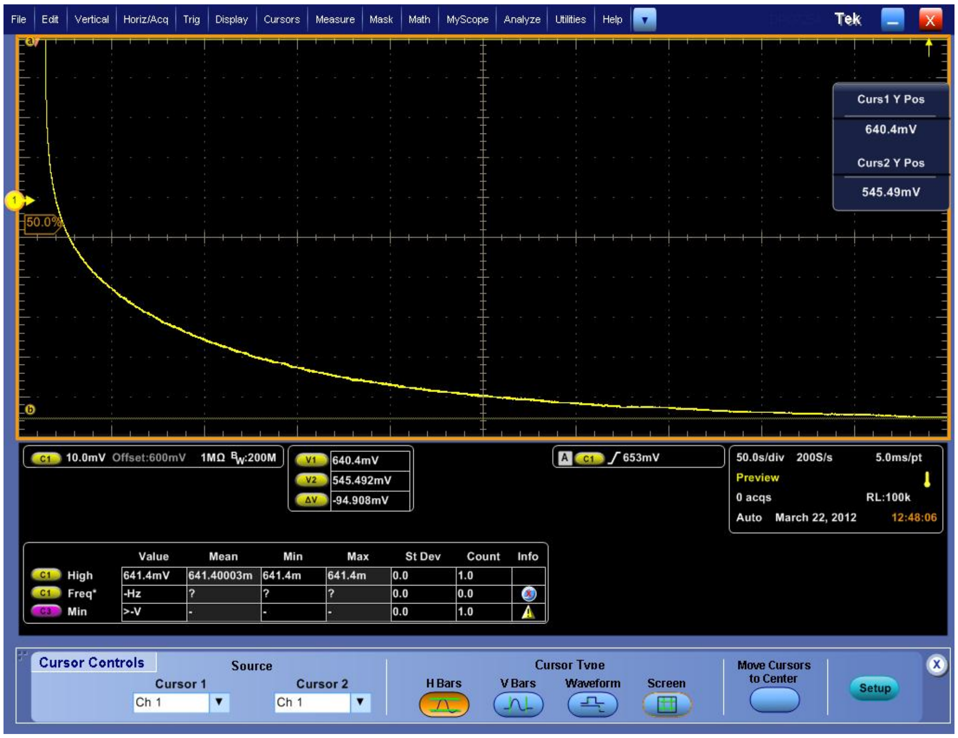

Figure 9: Time Constant Waveform for Board: Y_1

Table 15: Calibration results for Board: Z_1

Chamber set (°C)	V_Source (V)	i_Diode(μA)	R_Series (Ω)	T1_Top(°C)	T2_Bottom (°C)	V_Diode (V)
30°C	15	100	25.4	29.7	29.5	0.692
60°C	15	100	25.4	62.5	61	0.632
90°C	15	100	25.4	90.1	87	0.581
120°C	15	100	25.4	121.1	111.8	0.525

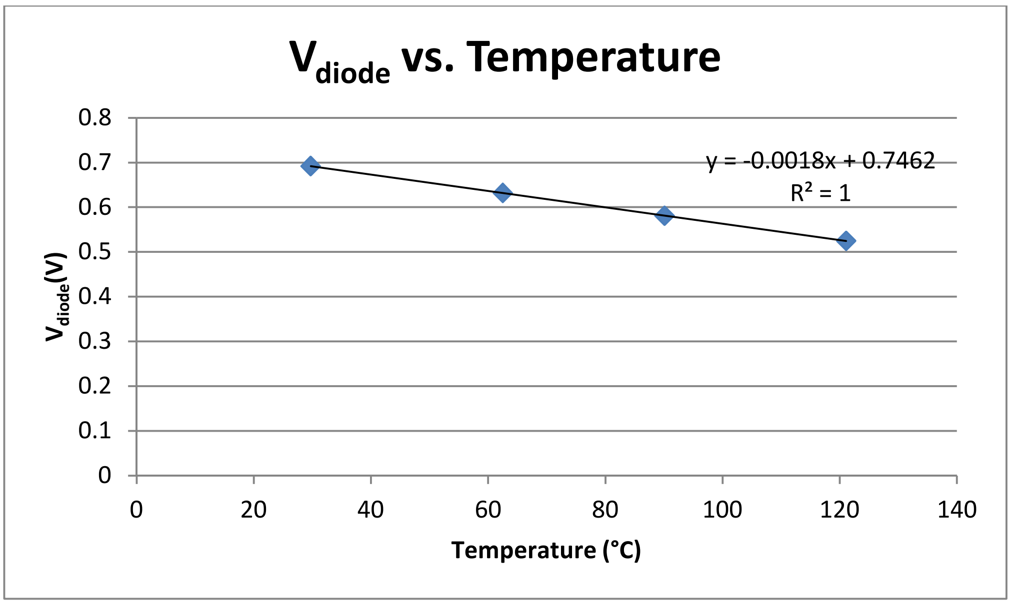

Figure 10: Calibration Plot for Board: Z_1

Table 16: Still Air Results for Board: Z_1

V_PS (V)	P (W)	Time Elasped (min)	T1_Top (°C)	T2_Bottom (°C)	T3_Casting (°C)	T4_Chamber (°C)	V_Diode (V)	Junction Temp. (°C)	θJA
7.13	2.00	0	61.1	67.5	59.7	62.9	0.566	100.11	18.61
7.13	2.00	2	63.6	71.0	58.7	49.9	0.560	103.44	26.77
7.13	2.00	4	63.0	70.2	58.6	48.0	0.561	102.89	27.44
7.13	2.00	6	62.5	69.5	57.7	45.9	0.562	102.33	28.22
7.13	2.00	8	61.9	68.9	57.4	44.7	0.563	101.78	28.54
7.13	2.00	10	61.3	68.0	56.7	41.0	0.564	101.22	30.11
7.13	2.00	12	60.7	67.8	56.3	42.5	0.565	100.67	29.08
7.13	2.00	14	60.2	67.0	55.9	41.3	0.566	100.11	29.41
7.13	2.00	16	59.8	66.5	54.9	40.7	0.567	99.56	29.43
7.13	2.00	18	59.1	65.7	54.2	40.0	0.568	99.00	29.50
7.13	2.00	20	58.5	65.4	53.9	39.1	0.569	98.44	29.67
7.13	2.00		61.1	68.0	56.4	43.3	0.565	100.944	28.82

Table 17: Forced Air Results for Board: Z_1

V_PS (V)	P (W)	R_series (Ω)	T1_Top (°C)	T2_Bottom (°C)	T3_Casting (°C)	T4_Ambient (°C)	V_Diode (V)	Junction Temp. (°C)	θJA
2.00	0.16	25.4	63.8	64.4	63.5	64.1	0.622	69.00	31.11
4.00	0.63	25.4	64.5	66.1	64.1	64.2	0.604	79.00	23.50
6.00	1.42	25.4	65.7	68.9	64.5	64.2	0.577	94.00	21.03
8.00	2.52	25.4	66.9	72.6	65.3	64.2	0.542	113.44	19.54

Table 18: Insulated Test Results for Board: Z_1

P(W)	R(Ω)	T1_Top (°C)	T2_Bottom (°C)	T3_Ambient (°C)	V_Diode (V)	Junction Temp (°C)	θJA
0.25	25.4	28.1	28.2	22.8	0.688	32.33	38.1
0.5	25.4	33.9	34.3	24.2	0.67	42.33	36.3
1	25.4	44.3	45.3	27	0.639	59.56	32.6

Table 19: Time Constant Results for Board: Z_1

SoC Package (sec)	Board with Casting (sec)
1.824	0.974

Figure 11: Time Constant Waveform for Board: Z_1

Table 20: Calibration results for Board: Z_2

Chamber Set (°C)	V_Source (V)	i_Diode (μA)	R_Series (Ω)	T1_Top(°C)	T2_Bottom (°C)	V_Diode (V)
30°C	15	100	24.7	29.8	29.6	0.691
60°C	15	100	24.7	61.1	60.4	0.633
90°C	15	100	24.7	90.1	89.3	0.579
120°C	15	100	24.7	121.5	120.5	0.519

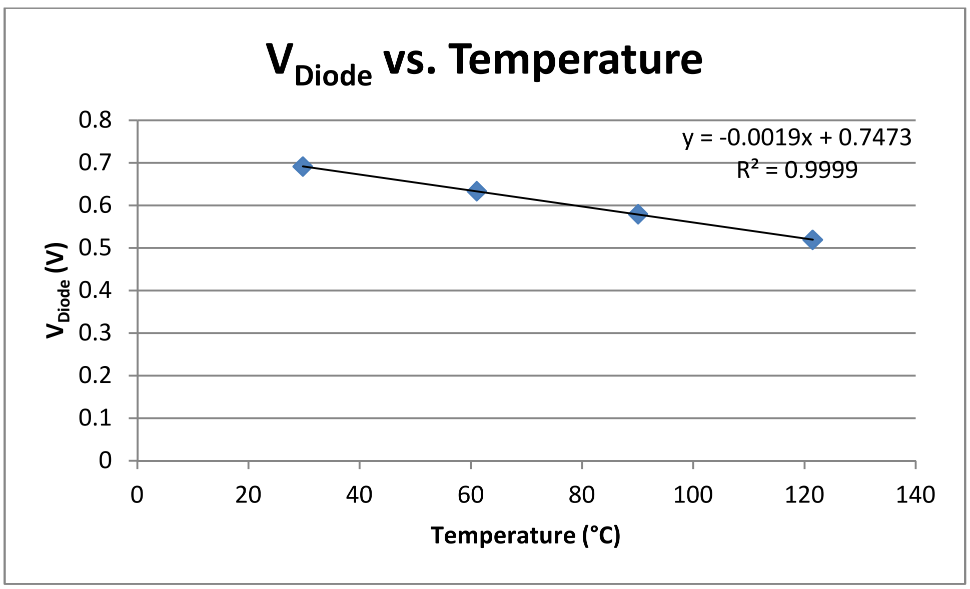

Figure 12: Calibration Plot for Board: Z_2

Table 21: Still Air Results for Board: Z_2

V_PS (V)	P (W)	Time Elasped (min)	T1_Top (°C)	T2_Bottom (°C)	T3_Casting (°C)	T4_Ambient (°C)	V_Diode (V)	Junction Temp. (°C)	θJA
7.10	2.00	0	70.0	68.9	61.3	61.5	0.558	100.37	19.43
7.10	2.00	2	73.3	73.1	60.6	51.9	0.551	104.05	26.08
7.10	2.00	4	73.1	72.9	59.9	49.1	0.552	103.53	27.21
7.10	2.00	6	72.5	71.8	59.1	48.1	0.553	103.00	27.45
7.10	2.00	8	71.9	71.4	58.7	46.6	0.554	102.47	27.94
7.10	2.00	10	71.2	70.9	58.2	46.3	0.555	101.95	27.82
7.10	2.00	12	70.7	70.1	57.5	46.0	0.556	101.42	27.71
7.10	2.00	14	70.1	69.5	56.8	45.2	0.557	100.89	27.85
7.10	2.00	16	69.6	68.9	56.4	43.6	0.558	100.37	28.38
7.10	2.00	18	69.0	68.8	55.8	43.1	0.559	99.84	28.37
7.10	2.00	20	68.5	67.8	55.2	41.9	0.560	99.32	28.71
7.10	2.00		71.0	70.5	57.8	46.2	0.556	101.68	27.75

Table 22: Forced Air Results for Board: Z_2

V_PS (V)	P (W)	R_Series (Ω)	T1_Top (°C)	T2_Bottom (°C)	T3_Casting (°C)	T4_Ambient (°C)	V_Diode (V)	Junction Temp. (°C)	θJA
2.00	0.16	24.7	62.8	63.6	62.6	63.6	0.622	66.68	19.05
4.00	0.65	24.7	64.1	65.5	63.6	63.8	0.603	76.68	19.89
6.00	1.46	24.7	65.1	68.1	64.3	63.9	0.573	92.47	19.60
8.00	2.59	24.7	66.7	71.3	65	64	0.534	113.00	18.91

Table 23: Insulated Test Results for Board: Z_2

P(W)	R(Ω)	V	T1_Top (°C)	T2_Bottom (°C)	T3_Ambient (°C)	V_Diode (V)	Junction Temp (°C)	θJA
0.25	24.7	2.51	28	27.5	23.8	0.686	33.00	36.80
0.5	24.7	3.55	33.1	32.7	25.9	0.667	43.00	34.20
1	24.7	5.02	42	42.1	29.5	0.633	60.89	31.39

Table 14: Time Constant Results for Board: Z_2

SoC Package (sec)	Board with Casting (sec)
1.290	0.874

Figure 13: Time Constant Waveform for Board: Z_2

References:

Heo, Seongmoo, K. Barr, and K. Asanovic. Proc. of Proceedings of the 2003 International Symposium on Low Power Electronics and Design. Print.

Maynard, Jason. *Design of an 8-Channel Data Acquisition System for Measuring Diode Junction Temperature*. Thesis. California Polytechnic State University - San Luis Obispo, 2009. Print.

Galbraith, Richard, and Travis Oenning. "Iterative Detection Read Channel Technology in Hard Disk Drives." *Hitachi Inspire the Next*. Hitachi Global Storage Technologies, 2008. Web.

Galbraith, Richard, and Travis Oenning. "Iterative Detection Read Channel Technology in Hard Disk Drives." *Hitachi Inspire the Next*. Hitachi Global Storage Technologies, 2008. Web.

Viswanath, Ram, Vijay Wakharkar, Abhay Watwe, and Vassou Lebonheur. *Thermal Performance Challenges from Silicon to Systems*. Tech. Intel Technology, 2000. Print.

Gurumurthi, Sudhanva, Anand Sivasubramaniam, and Vivek Nataranjan. *Disk Drive Roadmap from the Thermal Perspective: A Case for Dynamic Thermal Management*. Tech. University Park: Computer System Labs, 2005. Print.

Jaeger, Richard C., and Travis N. Blalock. *Microelectronic Circuit Design*. New York: McGraw-Hill, 2011. Print.

Farrance, Rex. "Timeline: 50 Years of Hard Drives." *PC World* 13 Sept. 2006. Web.

Elerath, Jon G., and Sandeep Shah. *Disk Drive Reliability Case Study*. Tech. IEEE, 2003. Print.

Chung, D.D.L. *Journal of Materials Engineering and Performance*. ASM International, 2000. Prin