Riley the Cat

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Purpose:

To create a toy that is a cross between a stuffed animal and a robot.

Figure 1: Riley the Cat completed

Introduction:

There are many toys that exist that are comfort objects. Generally these are toys that are soft such as blankets, stuffed animals, and pillows. Robotic toys also exist such as games, interactive books, and instruments. There exists a crossover market that includes Furbys, Tomagachi pets, and Fur Real Friends. While being very popular, I believe that this crossover isn't perfect, and that there is a lot of room for improvement. Riley (Figure 1) was created to make something that is both completely a robot and a comfort object.

Design:

Cat: Riley is a stuffed animal filled with an Arduino Mega 2560 and several sensors. Via several communication protocols (Table 1) through the Arduino's various digital and analog inputs, Riley does a variety of activities including detecting objects, moving eyes and speaking. Connections to each of the sensors can be seen can be seen in figure 3. Riley functions as a state machine. The data flow is in figure 2.

Development:

Arduino Software: Development was done within the open source Arduino software available at http://arduino.cc/en/Main/Software.

Breadboard: The electronic circuits were first built on a broad board to ensure functionality. They were then moved and soldered to a PC board.

List of features:

- Oled eyes (x2)
- Photoresistors (x6)
- RFID reader
- Accelerometer
- Microphone
- Speaker
- Vibration motor
- Arduino Mega
- Servo

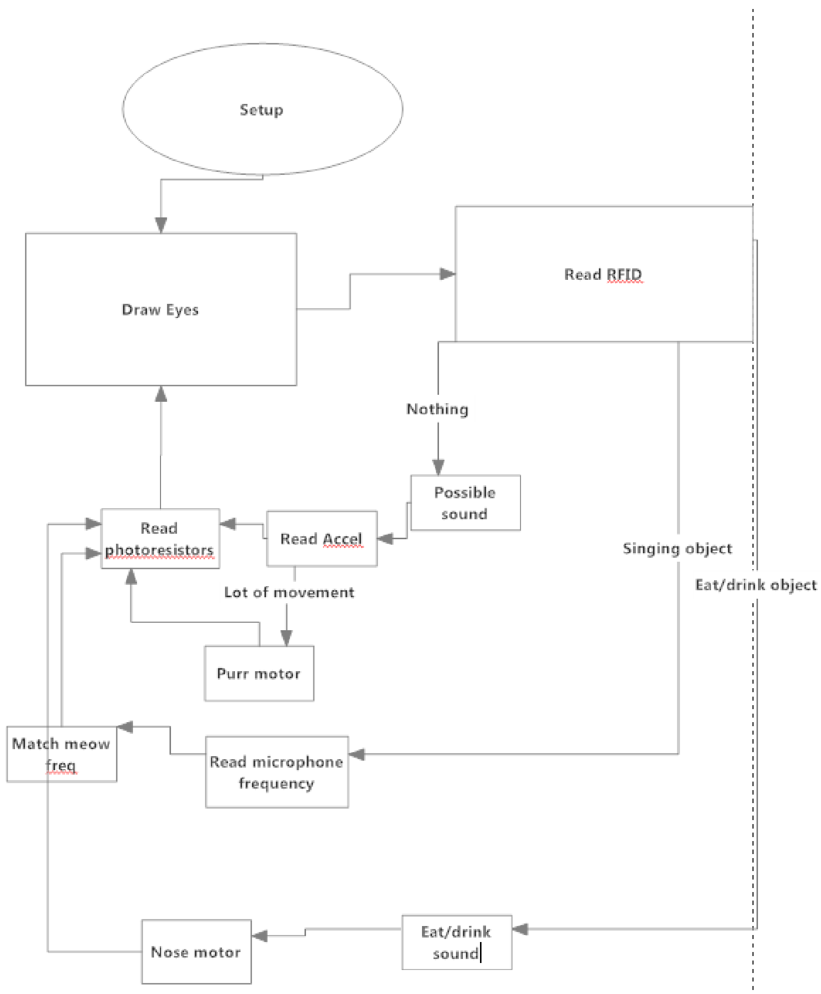


Figure 2: Data Flow Diagram

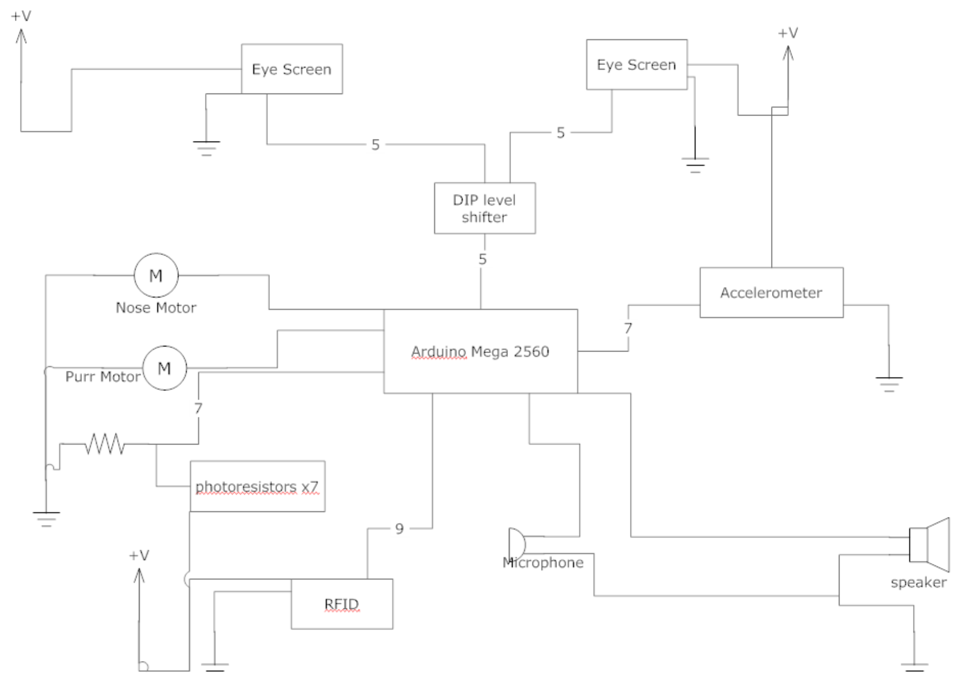


Figure 3: Overall Connections

Sensor	**Ports** *ports correspond to the numbers on the Arduino schematic	**Communication protocol**
Photoresistors	0-5 in Analog in ports(I may multiplex these instead, but this gives the fastest feedback)	ADC
Microphone	7 Analog in port	ADC
Speaker	10	PWM
Purr Motor	24	signal
Tail Servo	5	PWM
DIP Level shifter (connects to screens)	22, 23, 51(Mosi), 52 (SCK), 53(CS)	spi
RFID	0 (RX)	ttl
Accelerometer	Analog in ports 8-10	ADC built into MEGA 2560

Table 1: Connection Protocols

Parts Description:

The following is a list and descriptions of all the features in Riley. Each will include name, simulated part, location in body, and part site.

Part Name: Arduino Mega

Simulated Part: Brain

Location: Torso

Part Site: http://www.sparkfun.com/products/11061

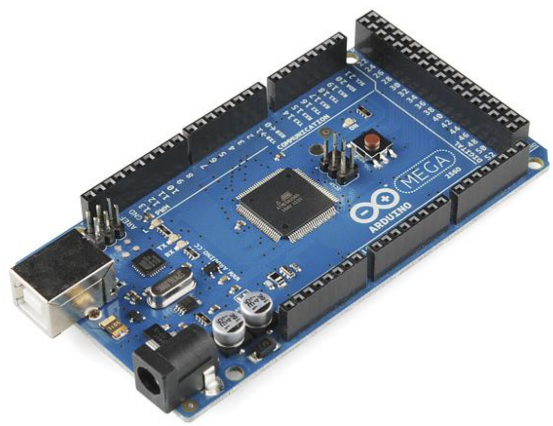


Figure 4: Arduino Mega

The Arduino Mega (figure 4) uses a C++ code that includes the image and sound libraries. The code is a state machine that takes the different inputs and moves into other states. The idle state detects ambient light, RFID tags and accelerometer input.

Part Name: Handmade Sock Cat

Simulated Part: Skin

Location: All

Part Site: http://www.etsy.com/listing/93816729/handmade-sock-cat-kitty-stuffed-animal?ref=pr_shop

Figure 5: Stuffed Sock Cat

The body of Riley, a sock kitty (figure5) found on Etsy, was selected for its adorable looks to ensure Riley would serve as a comfort object. Although the body did fit all of the electronics, a larger stuffed animal may have been preferred for ease of assembly.

Part Name: Oled Screens

Simulated Part: Eyes (visual)

Location: Head

Part Site: http://www.adafruit.com/products/326

Figure 6: OLED Screens

The screens that act as Riley's eyes, are Monochrome 128x64 oled screens (figure 6). The supplied libraries were extremely slow (2 frames per second) as they were meant for displaying static data vs animation. I found an update on a forum that addressed this using hardware acceleration. I had to edit it to work with my board which was different than the specified code. After the update the refresh rate was closer to 10 frames per second. Since the screens were LEDs, no flicker from the slower frame rate was experienced. The frame rate was directly affected by how much I was writing to the screens and did other things in the background.

The Screens are connected in parallel to a level shifter chip which is connected to the board. The chip changes the 5V outputs of the Arduino into the 3V ones the screens require.

The information displayed on the screen was created in different ways. For the images I converted an image into a 128x64 monochrome bitmap. This essentially turned each pixel into a 1 or 0. Then I used a program called LCD assistant (http://en.radzio.dxp.pl/bitmap_converter/) to turn the image into an array of chars that could be copy and pasted over to my program. For the eye animation I first drew an image of a white oval. Then I used the screen libraries to draw a rectangle over them. The width and location of the rectangle depended on the photoresistor input.

Part Name: Photoresistors

Simulated Part: Eye (sensing)

Location: Front Paws

Part Site: http://www.adafruit.com/products/161

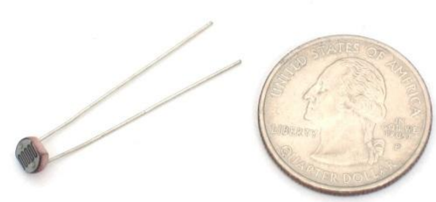


Figure 7: Photoresistors

The photoresistor (figure 7) circuit consisted of a photoresistor tied to high and an output/ resistor tied to ground. The photoresistor increases it resistance under light. The brighter the light, the lower the output voltage. There are 6 photoresistors spread in an array on Riley's paws

and the output voltage of each photoresistor is connected to an analog input on the Arduino. If an object were to go in front of one of the photoresistors, the Arduino would sense the voltage change and cause Riley's eyes to react. The choice of resistance was important because the light sensitivity changed based on the value. The input of light vs the resistance of the photoresistor was not linear, so a value that reflected a natural light value was necessary. Based on a chart of sensitivities found on http://www.ladyada.net/learn/sensors/cds.html I made a chart of expected sensitivities at different light ambiance.

The equation for solving the different pupil sizes was 1000/(darkest resistor) * 30 + 20. The typical analog value from the resistors was approximately 200 – 800. The 1000 *30 coefficient was used to give an appropriate scaling. The offset, 20, was included to ensure the pupils never got smaller than 20 pixels. A check was also done to ensure that the size was never over 50 pixels.

Ambient light	Ambient light (lux)	Photocell resistance (Ω)	LDR + R (Ω)	Current thru LDR+R	Pupil Size
Moonlit night	1 lux	70 KΩ	0.07 mA	0.1 V	50 pixels
Dark Room	10 lux	10 KΩ	0.45 mA	0.5 V	49 pixels
Dark overcast day / Bright room	100 lux	1.5 KΩ	2 mA	2.0 V	30 pixels
Overcast day	1000 lux	300 Ω	3.8 mA	3.8 V	23 pixels
Full daylight	10,000 lux	100 Ω	4.5 mA	4.5 V	20 pixels

Table 2: Light inputs compared to pupil size

Part Name: Speaker

Simulated Part: Voice

Location: Torso

Part Site: http://www.sparkfun.com/products/9151

Figure 8: Speaker

A speaker (figure 8) output sound was output using interrupts. I edited a library from http://www.arduino.cc/playground/Code/PCMAudio to take multiple sounds (the original only took one). The interrupts ensure that the playback is accurately timed.

To create sounds output by the speakers

1. I converted the sound into a PCM (pulse code modulation) unsigned 8 bit mono output. PCM is a digital representation of analog signals. I used GoldWave for this step http://www.goldwave.com/. This took the mp3 image and output it into char data.
2. Since the library only takes input chars in the form of numbers delimited by commas, I wrote a c program script to format the data appropriately.
3. I then copied the output over to my program. The array is stored in the SRAM on startup.

Part Name: Accelerometer
Simulated Part: Balance

Location: Torso

Part Site: http://www.sparkfun.com/products/9652

Figure 9: Accelerometer

The accelerometer (figure 9) senses a difference by reading a value, then comparing it to the previous value. Based on the current tilt, the accelerometer output different analog values from its x, y, and z ports. These outs are wired to the analog ins on the Arduino. The analog reader on the Arduino does an internal 5V comparison. The values are gauged from 0 – 1024, 1024 being 5V. On each iteration of the purr function each of the current directions is compared to the previous value of the direction. If the difference large enough, the purr motor will begin. For Riley, the difference chosen (though experimentation) was 300. Even at rest the analog values of the accelerometer fluxuate wildly. Differences smaller than 300 would cause the check to go off

randomly even when Riley wasn't being handled. Differences greater than 300 wouldn't be detected.

Part Name: RFID Reader

Simulated Part: Object detection

Location: Head

Part Site: http://www.sparkfun.com/products/8419

Figure 10: ID-12 RFID reader

The RFID reader is ID-12 (125 kHz) (figure 10). The reader does not include an antenna so I designed my own using copper wire. The range of the reader with the antenna was 2-3 cms. Initially I used tags http://www.sparkfun.com/products/10169 but they were too large to fit inside the cloth toys envisioned for Riley so I used smaller, button RFID tags https://www.adafruit.com/products/363 instead. Unfortunately, these tags provided even more reduced range (1cm).

Part Name: Vibration Motor

Simulated Part: Purr

Location: Torso

Part Site: http://www.radioshack.com/product/index.jsp?productId=2914700

Figure 11: Vibration Motor

The vibration motor (figure 11) needed a small enough current that a signal alone from the Arduino could power it. The problem was that the Arduino only outputs 5V and the limit of the motor was 3V. I had to use a voltage regulator circuit (figure 12) in order to output a safe 3V to it. The voltage regulator was a variable voltage regulator that required me to change its values via a pair of resistors. The equation was V = 1.25(1+(R2/R1)). I made the values of the resistors 220 for R1 and 165 for R2.

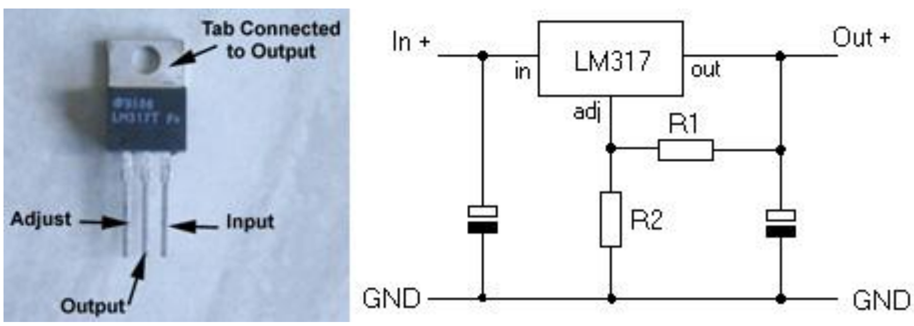


Figure 12: Vibration Motor connection

Part Name: Microphone

Simulated Part: Ears

Location: Torso

Part Site: http://www.sparkfun.com/products/8635

Figure 13: Microphone

The microphone (figure 13) used a standard analog input. I then mapped the input to a Fourier Transform algorithm I found at http://www.arduino.cc/cgi-bin/yabb2/YaBB.pl?num=1286718155. To prove that the data was detecting frequencies I mapped them to different points on the screen to make a kind of audio analyzer.

Part Name: Servo

Simulated Part: Tail

Location: Torso/back

Part Site: http://www.radioshack.com/product/index.jsp?productId=12296088

Figure 14: Servo (servo used was slightly different model)

A servo (figure 14) controlled Riley's tail. Tail operation was simple. The high and ground were connected to the Arduino. The direction was controlled by pulse width modulation. The equation for the tail direction was 255 minus desired angle. 255 is the largest value that can

be written to an 8 bit PWM and maps to the signal being on continuously. The range of the servo was 0 – 179 so the lowest value was 76 (255 – 179). To make the tail move randomly I used the Arduino's random function to find a random angle, and then wrote the value to the servo.

Part Name: Battery

Simulated Part: Energy

Location: Back Left foot

Part Site: http://www.radioshack.com/product/index.jsp?productId=2062219 (connector) http://www.radioshack.com/product/index.jsp?productId=3897297 (battery)

Figure 15: Battery and connector

Riley can be powered via the Arduino's usb port or through a 9V battery (figure 15) . With all of Riley's sensors connected the battery only lasts approximately 17 minutes. To reduce power requirements turn off the servo.

Part Name: On/Off Switch

Simulated Part: Sleep

Location: Back Right foot

Part Site: http://www.radioshack.com/product/index.jsp?productId=12688419

Figure 16: On/Off switch

This switch (figure 16) was included to easily short or open the battery input. It will not affect Riley if the USB is plugged in.

Future improvements:

Cost:

Arduino:

To lower the cost, this board could potentially be replaced with an Uno or smaller board. However to maintain functionality, the analog inputs would have to be multiplexed as there are fewer analog inputs on the Uno bard. Also EEPROM or external memory may have to be used in order to support Riley's eye images and purring sounds.

Screens:

The oled screens are beautifully crisp, but could be taken out for a much cheaper alternative. Examples include a SPI TFT screen (http://www.adafruit.com/products/618) that would provide color support or a Nokia 5110 screen (http://www.adafruit.com/products/338) would give a larger screen. Both are half the price of the OLEDs.

Performance:

Speaker:

If the speaker were to be amplified, it would have had a much higher volume. The tone function was loud enough but the PCM sound image was very quiet.

Battery:

Recharable batteries would be the most desirable for a toy so they won't have to be switched out so often. They may also give a longer life. The servo's moving arm also drained the battery. If the tail wasn't moving the life would be much longer.

Photoresitors:

While the lower power usage of the photoresistors was good on battery life, another form of object detection would probably be more effective. Possible alternatives would include a web cam with vision code or arrayed sound sensor.

Microphone:

The input was very weak and even pounding on the microphone gave very little change. In the future for an effective output, there should be an amplified circuit with a good filter.

RFID:

In the future I would use a more expensive version of the reader (either the ID2 or ID20) which have built in antennas. These would have given a much better range.

Wiring:

What may have been easier and more stable way of wiring would be to make an Arduino shield and solder everything into it. It would make for much less wiring and have more reliability

Conclusion:

With some more work Riley could be a functional toy that could be enjoyed by children. If a PC board was specialized the wiring would be much more solid and Riley could be cheaper. With some market research, liked features could be improved and added while unwanted ones could be dropped. Robotics are becoming much more prevalent today, especially in toys. Riley could potentially share some of that market.

Appendix A: Arduino Code

```
#define OLED_DC 23
#define OLED_CS 53
#define OLED_CLK 52
#define OLED_MOSI 51
#define OLED_RESET 22
#define PHOTO0 0
#define PHOTO1 1
#define PHOTO2 2
#define PHOTO4 3
#define PHOTO5 4
#define PHOTO6 5
#define MICRO 7
#define ACCX 8
#define ACCY 9
#define ACCZ 10
#define SPEAKER 10
#define RFIDResetPin 50
#define PURM 24
#define FOLLOWLEN 3000
#define SERV 5

#define READCARD 15  //how often card is read.  1 is every time, more is less times

//blinkrand must be devisable by blinkdec
//how often blink
#define BLINKRAND 200
//increase of chance they will blink in future
#define BLINKDEC 2
//Speed eye will move to follow object
#define EYESPEED 5
//Eye sensitiy to change (If eye is twitching increase)
#define EYETWITCH 10
#define IRISCHANGE 1

#define MAXPURLEN 5

#include <SSD1306.h>
#include <SPI.h>
#include <stdint.h>
#include <avr/interrupt.h>
#include <avr/io.h>
#include <avr/pgmspace.h>
#include <fix_fft.h>

#define SAMPLE_RATE 8000

SSD1306 oled(OLED_MOSI, OLED_CLK, OLED_DC, OLED_RESET, OLED_CS);
```

```
int sounddata_length=5000;

static unsigned int pc = 0;

int curBl = 0;
int curRand = BLINKRAND;
int eyeDir = 0;
int irisSize = 16;
char tagString[13];
int purLen = 0; //length of purr

char tag1[13] = "8400338D3C06";
char tag2[13] = "84003364D102";
char tag3[13] = "8400336635E4";
char tag4[13] = "8400338A93AE";
char tag5[13] = "4E0004467D71";


void setup()   {
  Serial.begin(9600);
  Serial1.begin(9600);
  pinMode(PURM, OUTPUT);
  digitalWrite(PURM, HIGH);
  pinMode(RFIDResetPin, OUTPUT);
  digitalWrite(RFIDResetPin, HIGH);
  SPI.begin ();
  oled.ssd1306_init(SSD1306_SWITCHCAPVCC);
  oled.display();
  oled.clear();

  pinMode(SERV, OUTPUT);
  pinMode(29, INPUT);
  pinMode(28, OUTPUT);
  pinMode(31, OUTPUT);
  digitalWrite(31, LOW);
  digitalWrite(28, HIGH);
}

//int DEBUG = 0;

char serv = 0;
int tailcur;
void loop() {
  eyeControl();
  oled.display();
  pc++;
  if (!(pc%READCARD)) {
```

```
    readTag();
  }
  if (!(purLen)) {
     purr();
  }  else {
     purLen--;
  }

  if (!(pc%30)){
    tailcur = tail();
  } else if (!(pc%10)){
    analogWrite(SERV, tailcur + 10 - random(10));
  }
}

int tail() {
   int temp = 250 - random(170);
   analogWrite(SERV, temp);
   Serial.println(temp);
   return temp;
}

char servoSafe[] = {};

void tailTest(){
   for(int i = 0; i < 170; i++){
      int temp = 250 - i;
      analogWrite(SERV, temp);
      Serial.println(temp);
      delay(3000);
    }
}

char im[128];
char data[128];
void tapFollow(){
  int static i = 0;
  if (i < 128){
    data[i] = analogRead(MICRO) / 4;
    im[i] = 0;
    i++;
  }
  else{
    fix_fft(data,im,7,0);
    oled.clear();
    for (i=0; i< 64;i++){
      oled.setpixel(i, data[i] + 20, WHITE);
    }
```

```
    oled.display();
  }
}

void lineAnimate(unsigned  char  pic[], int times) {
   int i, offset;
   for (i = 0; i < times; i ++){
     oled.clear();
     offset = i%4;
     offset*= 4;
     lines(offset);
     oled.drawbitmap(0, 0, pic, 128, 64, WHITE);
     oled.display();
   }
   oled.clear();
}

int xpos = 200 , ypos = 200 , zpos = 200;
void purr(){
  boolean mOn = false;

  int temp = xpos;

  digitalWrite(PURM, HIGH);

  xpos = analogRead(ACCX);
  mOn = (abs(temp - xpos) > 300);
  temp = ypos;
  ypos = analogRead(ACCY);
  if (!mOn) {

    mOn = (abs(temp - ypos) > 300);
  }

  temp = zpos;
  zpos = analogRead(ACCZ);
  if (!mOn) {

    mOn = (abs(temp - zpos) > 300);
  }
  if (mOn) {
    startPlayback(meow, 5000);
    purLen = MAXPURLEN;
    digitalWrite(PURM, LOW);
  }
}
```

```
void drawCircle(int xMidPoint, int  yMidPoint, int radius){
   int f = 1 - radius;
   int ddF_x = 1;
   int ddF_y = -2 * radius;
   int x = 0;
   int y = radius;
   //Top Middle
   oled.setpixel(xMidPoint, yMidPoint - radius, WHITE);
   while( x < y )
   {
      if(f >= 0)
      {
         y--;
         ddF_y += 2;
         f += ddF_y;
      }
      x++;
      ddF_x += 2;
      f += ddF_x;
      for( int i = 0; i < 5; i++) {
        //Top Right
        oled.setpixel(xMidPoint + x, yMidPoint - y - i, WHITE);
        oled.setpixel(xMidPoint + y, yMidPoint - x - i, WHITE);


        //Top Left
        oled.setpixel(xMidPoint - x, yMidPoint - y - i, WHITE);
        oled.setpixel(xMidPoint - y, yMidPoint - x - i, WHITE);
      }
   }
}

void testAccel(){
  char str[10];
  int temp, i;
  oled.clear();
  for (i = 300; i > 0; i--) {
   temp = analogRead(ACCX);
   itoa(temp, str, 10);
   oled.drawstring(0, 0, str);

   temp =  analogRead(ACCY);
   itoa(temp, str, 10);
   oled.drawstring(0, 1, str);

   temp = analogRead(ACCZ);
   itoa(temp, str, 10);
   oled.drawstring(0, 2, str);
```

```
    oled.display();
  }
  oled.clear();
}

void love() {
  digitalWrite(PURM, LOW);
  lineAnimate(heart, 90);
  digitalWrite(PURM, HIGH);
}


int eyeMove = 8;
void food() {
  digitalWrite(PURM, LOW);
  lineAnimate(fish, 30);
  startPlayback(munch, 20000);
  for (int i = 0; i < 150; i++) {
    oled.clear();
    drawCircle(65,70 + eyeMove++, 60);
    eyeMove%=15;
    oled.display();
  }
  oled.clear();
  digitalWrite(PURM, HIGH);
}

void microphone(){
  int tot = 0;
  for (int i = 0; i < 10; i++) {
    tot += analogRead(MICRO);
  }
  tot/=10;
  Serial.println(tot);
}

void water() {
  digitalWrite(PURM, LOW);
   lineAnimate(drop, 100);
   digitalWrite(PURM, HIGH);
}

void readTag(){
  int index = 0, readByte;
  boolean reading = false;

  while(Serial1.available()){
```

```
    readByte = Serial1.read(); //read next available byte

    if(readByte == 2) reading = true; //begining of tag
    if(readByte == 3) reading = false; //end of tag

    if(reading && readByte != 2 && readByte != 10 && readByte != 13){
      tagString[index++] = readByte;
    }
  }
  if(index) {
     checkTag(tagString); //Check if it is a match
     clearTag(tagString); //Clear the char of all value
     resetReader(); //eset the RFID reader
  }
}

void checkTag(char tag[]){
  tone(SPEAKER, 2000, 100);
  if(compareTag(tag, tag1)){ // if matched tag1, do this
    water();
  } else if(compareTag(tag, tag2)){ //if matched tag2, do this
    food();
  }else if(compareTag(tag, tag3)){
    for (int i = 0; i < 4000; i++) {
       tapFollow();
    }
  }else if(compareTag(tag, tag4)){
     love();
  }else if(compareTag(tag, tag5)){
    water();
  } else{
    Serial.println(tag); //read out any unknown tag
  }
}

void resetReader(){
  digitalWrite(RFIDResetPin, LOW);
  digitalWrite(RFIDResetPin, HIGH);
  delay(150);
}

void clearTag(char one[]){
  for(int i = 0; i < 12; i++){
    one[i] = 0;
  }
}

boolean compareTag(char one[], char two[]){
```

```
  for(int i = 0; i < 12; i++){
    if(one[i] != two[i]) {
      return false;
    }
  }
  return true; //no mismatches
}

void lines(int offset){
  int LINETHICK = 1;
  int LINEEND = 128 - LINETHICK;

  oled.fillrect(offset     , 0, LINETHICK, 64, WHITE);
  if ((offset += 16) > LINEEND) {
    offset %= 122;
  }
  oled.fillrect(offset, 0, LINETHICK, 64, WHITE);
  if ((offset += 16) > LINEEND) {
    offset %= 122;
  }
  oled.fillrect(offset, 0, LINETHICK, 64, WHITE);
  if ((offset += 16) > LINEEND) {
    offset %= 122;
  }
  oled.fillrect(offset, 0, LINETHICK, 64, WHITE);
  if ((offset += 16) > LINEEND) {
    offset %= 122;
  }
  oled.fillrect(offset, 0, LINETHICK, 64, WHITE);
  if ((offset += 16) > LINEEND) {
    offset %= 122;
  }
  oled.fillrect(offset, 0, LINETHICK, 64, WHITE);
  if ((offset += 16) > LINEEND) {
    offset %= 122;
  }
  oled.fillrect(offset, 0, LINETHICK, 64, WHITE);
  if ((offset += 16) > LINEEND) {
    offset %= 122;
  }
  oled.fillrect(offset, 0, LINETHICK, 64, WHITE);
}

void draweye(int dir, int blin, int thick) {
   //blin is 0 - 32 where 0 is no blink and 32 is closed eye
   //dir is direction of eye where 0 is center and +- 128 is where the iris is
   //think is the width of the iris 0-64
```

```
  //eyeball
  oled.drawbitmap(0, 0, eye, 128, 64, WHITE);
  //iris
  oled.fillrect(62 + dir, 0, thick, 64, BLACK);
  //top eye lid
  oled.fillrect(0, 0, 128, blin, BLACK);
  //bottom eye lid
  oled.fillrect(0, 64 - blin, 128, blin, BLACK);
}

volatile uint16_t sample;
byte lastSample;
unsigned char *sounddata_data = meow;

ISR(TIMER1_COMPA_vect) {
  if (sample >= sounddata_length) {
     if (sample == sounddata_length + lastSample) {
        stopPlayback();
     }
     else {
       OCR2A = sounddata_length + lastSample - sample;
    }
  }
  else {
    OCR2A = pgm_read_byte(&sounddata_data[sample]);
  }
  ++sample;
}


void startPlayback(unsigned char sound[], int length)
{
   sounddata_data = sound;
   sounddata_length = length;
   pinMode(SPEAKER, OUTPUT);
   // Set up Timer 2 to do pulse width modulation on the speaker
   // pin.
   // Use internal clock (datasheet p.160)
   ASSR &= ~(_BV(EXCLK) | _BV(AS2));

   // Set fast PWM mode
   TCCR2A |= _BV(WGM21) | _BV(WGM20);
   TCCR2B &= ~_BV(WGM22);

   // Do non-inverting PWM on pin OC2A
   // On the Arduino this is pin 11.
   TCCR2A = (TCCR2A | _BV(COM2A1)) & ~_BV(COM2A0);
   TCCR2A &= ~(_BV(COM2B1) | _BV(COM2B0));
```

```
  // No prescaler (p.158)
  TCCR2B = (TCCR2B & ~(_BV(CS12) | _BV(CS11))) | _BV(CS10);

  // Set initial pulse width to the first sample.
  OCR2A = pgm_read_byte(&sounddata_data[0]);

  // Set up Timer 1 to send a sample every interrupt.

  cli();
  // Set CTC mode (Clear Timer on Compare Match)
  // Have to set OCR1A *after*, otherwise it gets reset to 0!
  TCCR1B = (TCCR1B & ~_BV(WGM13)) | _BV(WGM12);
  TCCR1A = TCCR1A & ~(_BV(WGM11) | _BV(WGM10));

  // No prescaler (p.134)
  TCCR1B = (TCCR1B & ~(_BV(CS12) | _BV(CS11))) | _BV(CS10);

  // Set the compare register (OCR1A).
  // OCR1A is a 16-bit register, so we have to do this with
  // interrupts disabled to be safe.
  OCR1A = F_CPU / SAMPLE_RATE;    // 16e6 / 8000 = 2000

  // Enable interrupt when TCNT1 == OCR1A (p.136)
  TIMSK1 |= _BV(OCIE1A);

  lastSample = pgm_read_byte(&sounddata_data[sounddata_length-1]);
  sample = 0;
  sei();
}

void stopPlayback()
{
  // Disable playback per-sample interrupt.
  TIMSK1 &= ~_BV(OCIE1A);

  // Disable the per-sample timer completely.
  TCCR1B &= ~_BV(CS10);

  // Disable the PWM timer.
  TCCR2B &= ~_BV(CS10);

  digitalWrite(SPEAKER, LOW);
}

void testEyeSens() {
 char str[10];
 int temp = analogRead(PHOTO0);
```

```
  itoa(temp, str, 10);
  oled.drawstring(0, 0, str);

  temp =  analogRead(PHOTO1);
  itoa(temp, str, 10);
  oled.drawstring(0, 1, str);

  temp = analogRead(PHOTO2);
  itoa(temp, str, 10);
  oled.drawstring(0, 2, str);

  temp = analogRead(PHOTO4);
  itoa(temp, str, 10);
  oled.drawstring(0, 4, str);

  temp = analogRead(PHOTO5);
  itoa(temp, str, 10);
  oled.drawstring(0, 5, str);

  temp = analogRead(PHOTO6);
  itoa(temp, str, 10);
  oled.drawstring(0, 6, str);

  temp = pulseIn(8, 0);
  //temp = analogRead(8);
  itoa(temp, str, 10);
  oled.drawstring(0, 7, str);
}

void eyeControl() {
  int newDir = getDir();
  if (newDir - EYETWITCH > eyeDir){
    eyeDir += EYESPEED;
  } else if (newDir +  EYETWITCH < eyeDir) {
    eyeDir -= EYESPEED;
  }
  if (!curBl) { //see if want to blink

    if (!random(curRand)) {
      curBl = 1;
      curRand = BLINKRAND;
    }
    curRand -= BLINKDEC;
    draweye(eyeDir, curBl, irisSize);
  } else if (curBl >= 64) {
    curBl = 0;
  } else if (curBl < 32 && curBl > 0)  { //opening
     draweye(eyeDir, curBl, irisSize);
```

```
    curBl += 8;
  } else if (curBl >= 32){ //closing
     draweye(eyeDir, 64 - curBl, irisSize);
     curBl += 8;
  }
}

int getDir(){
  //set largest value to
  //if largest value > current Current += IRISCHANGE
  //else current -= irisChange
  //may want to put in sensitivity

  int bottomPin = 0;
  int tempIris = analogRead(PHOTO0);
  int piny = analogRead(PHOTO1) + 40;
  if (piny < tempIris) {
   bottomPin = 1;
   tempIris = piny;
  }
  piny = analogRead(PHOTO2);
  if (piny < tempIris) {
   bottomPin = 2;
   tempIris = piny;
  }
  piny = analogRead(PHOTO4);
  if (piny < tempIris) {
   bottomPin = 4;
   tempIris = piny;
  }
  piny = analogRead(PHOTO5);
  if (piny < tempIris) {
   bottomPin = 5;
   tempIris = piny;
  }
  piny = analogRead(PHOTO6);
  if (piny < tempIris) {
   bottomPin = 6;
   tempIris = piny;
  }
  tempIris = 1000/tempIris * 3 + 20;
  tempIris = (tempIris < 50) ? tempIris : 50;

  if (tempIris < irisSize + 10) {
    irisSize--;
  } else if (tempIris > irisSize + 10){
   irisSize++;
  }
```

```
  return bottomPin * 10 - 35; //7 * num - num/2 * 7
}
```

Appendix B: Senior Project analysis

• **Summary of Functional Requirements**

Describe the overall capabilities of functions of your project or design. Describe what your project does. (Do *not* describe how you designed it.)

Riley is a stuffed animal cat that uses an Arduino to interface to many sensors. Features include, light detection, object following, tone recognition, sound output, tilt sensing, and RFID reading.

• **Primary Constraints**

Describe significant challenges or difficulties associated with your project or implementation. For example, what were limiting factors or other issues that impacted your approach? What made your project difficult? What parameters or specifications limited your options or directed your approach?

Each of the sensors took time to implement. Combining all of their functionality to the overall software was also a challenge. Fitting everything in the final stuffed animal also proved to be a challenge. Memory limits and sensor sensitivity were the largest limiting factors of the project.

• **Economic**

- Original estimated cost of component parts (as of the start of your project) - approximately $150
- Original estimated development time (as of the start of your project) - approximately 70 hours
- Actual development time (at the end of your project) - about 100 hours.

• **If manufactured on a commercial basis:**

- Estimated number of devices to be sold per year - 10,000
- Estimated manufacturing cost for each device - (depending on parts) $50
- Estimated purchase price for each device - $100
- Estimated profit per year - $500,000
- Estimated cost for user to operate device, per unit time (specify time interval) - n/a

• **Environmental**

Describe any environmental impact associated with manufacturing or use.

- *Proper recycling of electronic parts and battery*

• **Manufacturability**

Describe any issues or challenges associated with manufacturing.

- *Instead of an Arduino, a dedicated IC chip should be used to minimize expense/ resources*

• **Sustainability**

- Describe any issues or challenges associated with maintaining the completed device or system.

The wirered connections are sensitive and physical shock or distress to the project may cause some of the wires to short/ open

- Describe how the project impacts the sustainable use of resources. -

- *Oled screens use less energy than standard screens. Nothing within the project is using rare materials, and production would minimally effect the use of sustainable resources*

- Describe any upgrades that would improve the design of the project.

- *see senior project report. Improvements include different object detection, filters and amplifiers on the microphone and speaker.*

- Describe any issues or challenges associated with upgrading the design.

- *see senior project report. Expenses or power consumption could increase depending on the upgrade*

• **Ethical**

Describe ethical implications relating to the design, manufacture, use or misuse of the project.

The sock animal was purchased in China. Factory conditions should be checked before full scale manufacturing.

• **Health and Safety**

Describe any health and safety concerns associated with design, manufacture or use.

Any standard health and safety concerns with the development of electronic parts should be considered. Nothing in particular would be dangerous while producing Riley.

• **Social and Political**

Describe any social and political concerns associated with design, manufacture or use.

As a comfort object Riley could help during developmental stages. As a robot, Riley could potentially interest children in engineering at a young age. Riley is also gender neutral and could appeal to girls as much as boy.

• **Development**

Describe any new tools or techniques used for either development or analysis that you learned independently during the course of your project.

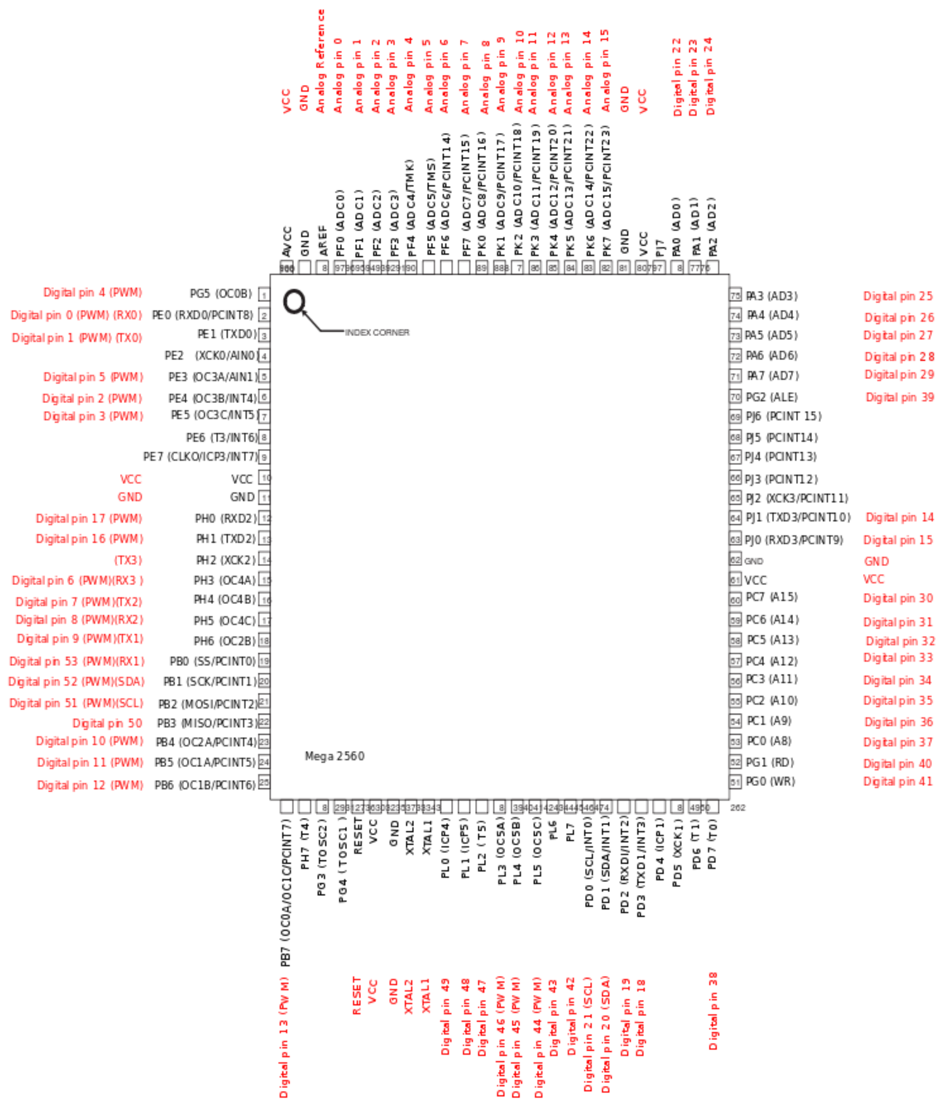
Arduino IDE, how to interface any of my sensors, communication protocols through Arduino

Apendix C: Pin Mapping for Arduino

ATmega2560-Arduino Pin Mapping

Below is the pin mapping for the Atmega2560. The chip used in Arduino 2560. There are pin mappings to Atmega8 andAtmega 168/328 as well.

Arduino Mega 2560 PIN diagram



The source SVG file is also available for download:

PinMapping2560.zip

Arduino Mega 2560 PIN mapping table

Pin Number	Pin Name	Mapped Pin Name
1	PG5 (OC0B)	Digital pin 4 (PWM)
2	PE0 (RXD0/PCINT8)	Digital pin 0 (PWM) (RX0)
3	PE1 (TXD0)	Digital pin 1 (PWM) (TX0)
4	PE2 (XCK0/AIN0)	
5	PE3 (OC3A/AIN1)	Digital pin 5 (PWM)
6	PE4 (OC3B/INT4)	Digital pin 2 (PWM)
7	PE5 (OC3C/INT5)	Digital pin 3 (PWM)
8	PE6 (T3/INT6)	
9	PE7 (CLKO/ICP3/INT7)	
10	VCC	VCC
11	GND	GND
12	PH0 (RXD2)	Digital pin 17 (PWM)
13	PH1 (TXD2)	Digital pin 16 (PWM)
14	PH2 (XCK2)	(TX3)
15	PH3 (OC4A)	Digital pin 6 (PWM)(RX3)
16	PH4 (OC4B)	Digital pin 7 (PWM)(TX2)
17	PH5 (OC4C)	Digital pin 8 (PWM)(RX2)

18	PH6 (OC2B)	Digital pin 9 (PWM)(TX1)
19	PB0 (SS/PCINT0)	Digital pin 53 (PWM)(RX1)
20	PB1 (SCK/PCINT1)	Digital pin 52 (PWM)(SDA)
21	PB2 (MOSI/PCINT2)	Digital pin 51 (PWM)(SCL)
22	PB3 (MISO/PCINT3)	Digital pin 50
23	PB4 (OC2A/PCINT4)	Digital pin 10 (PWM)
24	PB5 (OC1A/PCINT5)	Digital pin 11 (PWM)
25	PB6 (OC1B/PCINT6)	Digital pin 12 (PWM)
26	PB7 (OC0A/OC1C/PCINT7)	Digital pin 13 (PWM)
27	PH7 (T4)	
28	PG3 (TOSC2)	
29	PG4 (TOSC1)	
30	RESET	RESET
31	VCC	VCC
32	GND	GND
33	XTAL2	XTAL2
34	XTAL1	XTAL1
35	PL0 (ICP4)	Digital pin 49
36	PL1 (ICP5)	Digital pin 48
37	PL2 (T5)	Digital pin 47

38	PL3 (OC5A)	Digital pin 46 (PWM)
39	PL4 (OC5B)	Digital pin 45 (PWM)
40	PL5 (OC5C)	Digital pin 44 (PWM)
41	PL6	Digital pin 43
42	PL7	Digital pin 42
43	PD0 (SCL/INT0)	Digital pin 21 (SCL)
44	PD1 (SDA/INT1)	Digital pin 20 (SDA)
45	PD2 (RXDI/INT2)	Digital pin 19
46	PD3 (TXD1/INT3)	Digital pin 18
47	PD4 (ICP1)	
48	PD5 (XCK1)	
49	PD6 (T1)	
50	PD7 (T0)	Digital pin 38
51	PG0 (WR)	Digital pin 41
52	PG1 (RD)	Digital pin 40
53	PC0 (A8)	Digital pin 37
54	PC1 (A9)	Digital pin 36
55	PC2 (A10)	Digital pin 35
56	PC3 (A11)	Digital pin 34
57	PC4 (A12)	Digital pin 33

58	PC5 (A13)	Digital pin 32
59	PC6 (A14)	Digital pin 31
60	PC7 (A15)	Digital pin 30
61	VCC	VCC
62	GND	GND
63	PJ0 (RXD3/PCINT9)	Digital pin 15
64	PJ1 (TXD3/PCINT10)	Digital pin 14
65	PJ2 (XCK3/PCINT11)	
66	PJ3 (PCINT12)	
67	PJ4 (PCINT13)	
68	PJ5 (PCINT14)	
69	PJ6 (PCINT 15)	
70	PG2 (ALE)	Digital pin 39
71	PA7 (AD7)	Digital pin 29
72	PA6 (AD6)	Digital pin 28
73	PA5 (AD5)	Digital pin 27
74	PA4 (AD4)	Digital pin 26
75	PA3 (AD3)	Digital pin 25
76	PA2 (AD2)	Digital pin 24
77	PA1 (AD1)	Digital pin 23

78	PA0 (AD0)	Digital pin 22
79	PJ7	
80	VCC	VCC
81	GND	GND
82	PK7 (ADC15/PCINT23)	Analog pin 15
83	PK6 (ADC14/PCINT22)	Analog pin 14
84	PK5 (ADC13/PCINT21)	Analog pin 13
85	PK4 (ADC12/PCINT20)	Analog pin 12
86	PK3 (ADC11/PCINT19)	Analog pin 11
87	PK2 (ADC10/PCINT18)	Analog pin 10
88	PK1 (ADC9/PCINT17)	Analog pin 9
89	PK0 (ADC8/PCINT16)	Analog pin 8
90	PF7 (ADC7/PCINT15)	Analog pin 7
91	PF6 (ADC6/PCINT14)	Analog pin 6
92	PF5 (ADC5/TMS)	Analog pin 5
93	PF4 (ADC4/TMK)	Analog pin 4
94	PF3 (ADC3)	Analog pin 3
95	PF2 (ADC2)	Analog pin 2
96	PF1 (ADC1)	Analog pin 1
97	PF0 (ADC0)	Analog pin 0

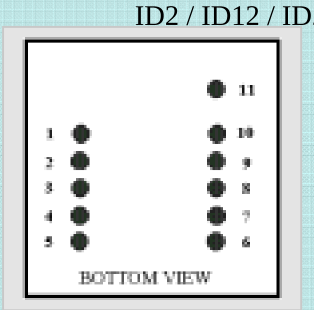
98	AREF	Analog Reference
99	GND	GND
100	AVCC	VCC

ID SERIES DATASHEET Mar 01, 2005

ID-2/ID-12 Brief Data

The ID2. ID12 and ID20 are similar to the obsolete ID0, ID10 and ID15 MK(ii) series devices, but they have extra pins that allow Magnetic Emulation output to be included in the functionality. The ID-12 and ID-20 come with internal antennas, and have read ranges of 12+ cm and 16+ cm, respectively. With an external antenna, the ID-2 can deliver read ranges of up to 25 cm. All three readers support ASCII, Wiegand26 and Magnetic ABA Track2 data formats.

ID2 / ID12 / ID20 PIN-OUT



1. GND
2. RES (Reset Bar)
3. ANT (Antenna)
4. ANT (Antenna)
5. CP
6. Future
7. +/- (Format Selector)
8. D1 (Data Pin 1)
9. D0 (Data Pin 0)
10. LED (LED / Beeper)
11. +5V

Operational and Physical Characteristics

Parameters	ID-2	ID-12	ID-20
Read Range	N/A (no internal antenna)	12+ cm	16+ cm
Dimensions	21 mm x 19 mm x 6 mm	26 mm x 25 mm x 7 mm	40 mm x 40 mm x 9 mm
Frequency	125 kHz	125 kHz	125 kHz
Card Format	EM 4001 or compatible	EM 4001 or compatible	EM 4001 or compatible
Encoding	Manchester 64-bit, modulus 64	Manchester 64-bit, modulus 64	Manchester 64-bit, modulus 64
Power Requirement	5 VDC @ 13mA nominal	5 VDC @ 30mA nominal	5 VDC @ 65mA nominal
I/O Output Current	+/-200mA PK	-	-
Voltage Supply Range	+4.6V through +5.4V	+4.6V through +5.4V	+4.6V through +5.4V

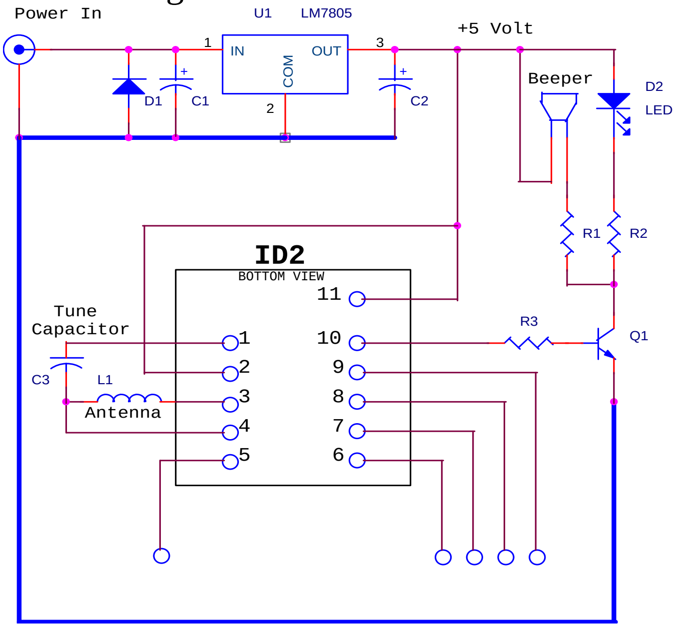
Pin Description & Output Data Formats

Pin No.	Description	ASCII	Magnet Emulation	Wiegand26
Pin 1	Zero Volts and Tuning Capacitor Ground	GND 0V	GND 0V	GND 0V
Pin 2	Strap to +5V	Reset Bar	Reset Bar	Reset Bar
Pin 3	To External Antenna and Tuning Capacitor	Antenna	Antenna	Antenna
Pin 4	To External Antenna	Antenna	Antenna	Antenna
Pin 5	Card Present	No function	Card Present *	No function

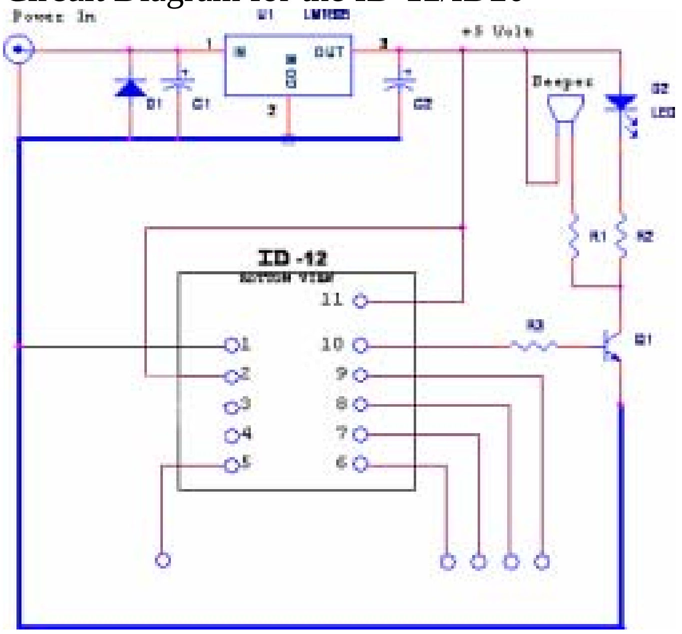
Pin 6	Future	Future	Future	Future
Pin 7	Format Selector (+/-)	Strap to GND	Strap to Pin 10	Strap to +5V
Pin 8	Data 1	CMOS	Clock *	One Output *
Pin 9	Data 0	TTL Data (inverted)	Data *	Zero Output *
Pin 10	3.1 kHz Logic	Beeper / LED	Beeper / LED	Beeper / LED
Pin 11	DC Voltage Supply	+5V	+5V	+5V

* Requires 4K7 Pull-up resistor to +5V

Circuit Diagram for the ID2

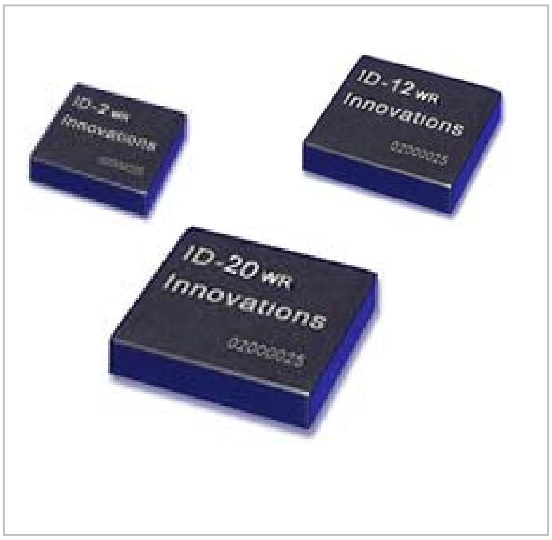


Circuit Diagram for the ID-12/ID20

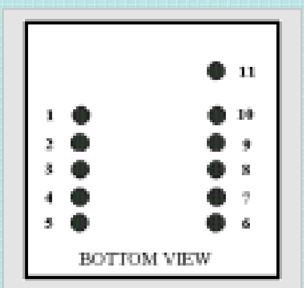


ID-2RW/ID-12RW Brief Data

The ID2-RW, ID12-RW and ID15-RW are a new series of Read/Write modules for the Temec Q5 tag. It has full functionality including password. They contain built-in algorithms to assist customers programming the popular Sokymat Unique type tag. Password protection is allowed. Control is via a host computer using a simple terminal program such as hyper terminal or Qmodem.



ID2 / ID12 / ID20 PIN-OUT



1 GND
2 RES (Reset Bar)
3 ANT (Antenna)
4 ANT (Antenna)
5 Future
6 Program LED
7 ASCII in
8 Future
9 ASCII Out
10 Read (LED / Beeper)
11 +5V

Operational and Physical Characteristics

Parameters	ID-2RW	ID-12RW	ID-20RW
Read Range	N/A (no internal antenna)	12+ cm (Unique Format)	15+ cm (Unique Format)
Dimensions	21 mm x 19 mm x 6 mm	26 mm x 25 mm x 7 mm	40 mm x 40 mm x 9 mm
Frequency	125 kHz	125 kHz	125 kHz
Card Format	Temec Q5555	Temec Q5555	Temec Q5555
Read Encoding	Manchester modulus 64	Manchester modulus 64	Manchester modulus 64
Power Requirement	5 VDC @ 13mA nominal	5 VDC @ 30mA nominal	5 VDC @ 50mA nominal
I/O Output Current	+/-200mA PK	-	-
Voltage Supply Range	+4.6V through +5.4V	+4.6V through +5.4V	+4.6V through +5.4V
Coil Detail	L = 0.6mH - 1.5mH, Q = 15-30	-	-

Description

A simple terminal program such as Qmodem or Hyper-terminal can be used to send commands to the module. The blocks are individually programmable. The command interface is simple to use and easily understood. The programmer also has two types of internal reader. One of these is provided to read Sokymat 'Unique' type tag configuration. The module does not require a MAX232 type chip interface. The module does **not** need an RS232 interface such as a MAX232 IC. The input pin7 goes to the computer through a 4k7 resistor and the output goes to the computer through a 100R resistor.

DATA FORMATS

Output Data Structure – ASCII

STX (02h)	DATA (10 ASCII)	CHECK SUM (2 ASCII)	CR	LF	ETX (03h)

[The 1byte (2 ASCII characters) Check sum is the “Exclusive OR” of the 5 hex bytes (10 ASCII) Data characters.]

Output Data Structure – Wiegand26

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
P	E	E	E	E	E	E	E	E	E	E	E	E	O	O	O	O	O	O	O	O	O	O	O	O	P
Even parity (E)													Odd parity (O)												

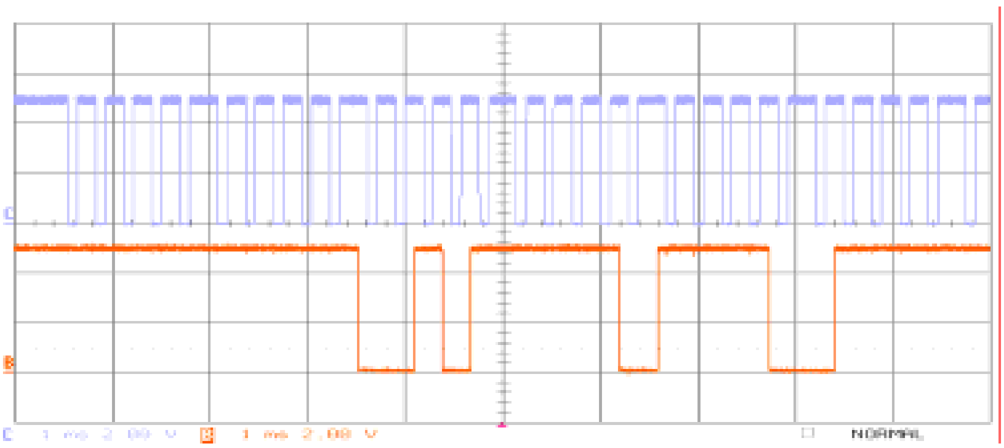
P = Parity start bit and stop bit

Output Data Magnetic ABA Track2

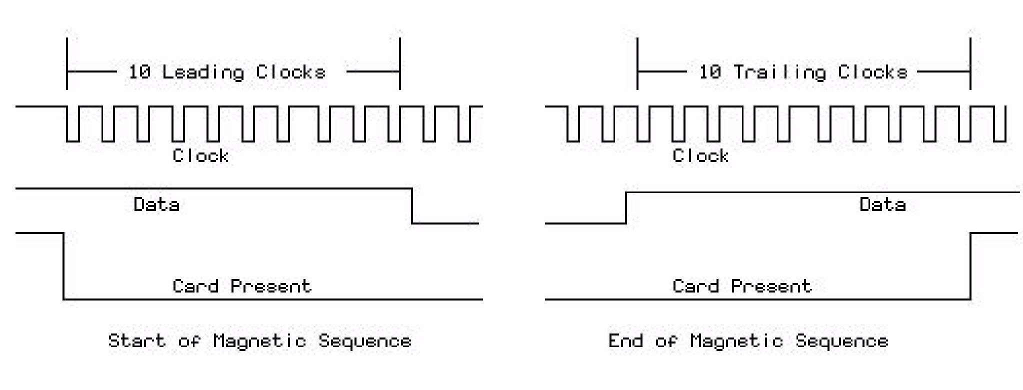
10 Leading Zeros	SS	Data	ES	LCR	10 Ending Zeros

[SS is the Start Character of 11010, ES is the end character of 11111, LRC is the Longitudinal Redundancy Check.]

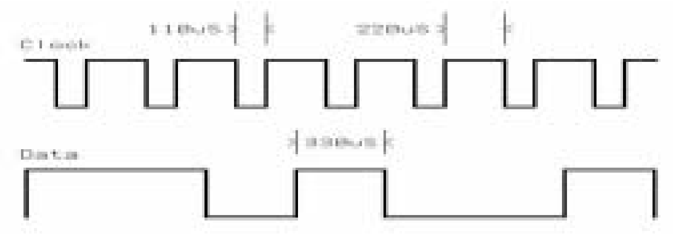
Magnetic Emulation Waveforms



Start and End Sequences For Magnetic Timing

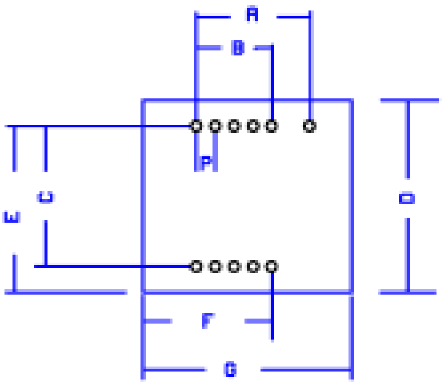


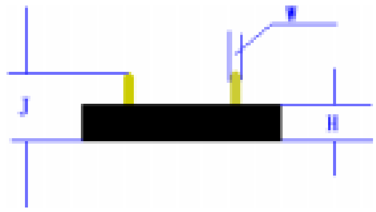
DATA TIMINGS FOR MAGNETIC EMULATION



The magnetic Emulation Sequence starts with the Card Present Line going active (down). There next follows 10 clocks with Zero ‘0’ data. At the end of the 10 leading clocks the start character (11010) is sent and this is followed by the data. At the end of the data the end character is sent followed by the LCR. Finally 10 trailing clocks are sent and the card present line is raised.
The data bit duration is approximately 330uS. The approximate clock duration is 110uS. Because of the symmetry data can be clocked off either the rising or falling edge of the clock.

Dimensions (Top View) (mm)





	ID-0/ID-2wr			ID-10/ID-12wr			ID-15/ID-20wr		
	Nom.	Min.	Max.	Nom.	Min.	Max.	Nom.	Min.	Max
A	12.0	11.6	12.4	12.0	11.6	12.4	12.0	11.6	12.4
B	8.0	7.6	8.4	8.0	7.6	8.4	8.0	7.6	8.4
C	15.0	14.6	15.4	15.0	14.6	15.4	15.0	14.6	15.4
D	20.5	20.0	21.5	25.3	24.9	25.9	40.3	40.0	41.0
E	18.5	18.0	19.2	20.3	19.8	20.9	27.8	27.5	28.5
F	14.0	13.0	14.8	16.3	15.8	16.9	22.2	21.9	23.1
G	22.0	21.6	22.4	26.4	26.1	27.1	38.5	38.2	39.2
P	2.0	1.8	2.2	2.0	1.8	2.2	2.0	1.8	2.2
H	5.92	5.85	6.6	6.0	5.8	6.6	6.8	6.7	7.0
J	9.85	9.0	10.5	9.9	9.40	10.5	9.85	9.4	10.6
W	0.66	0.62	0.67	0.66	0.62	0.67	0.66	0.62	0.67

Note – measurements do not include any burring of edges.
NOTICE - Innovated Devices reserve the right to change these specifications without prior notice.

Designing Coils for ID2

The recommended Inductance is 1.08mH to be used with an internal tuning capacitor of 1n5. In general the bigger the antenna the better, provided the reader is generating enough field strength to excite the tag. The ID-2 is relatively low power so a maximum coil size of 15x15cm is recommended if it is intended to read ISO cards. If the reader is intended to read glass tags the maximum coil size should be smaller, say 10x10cm.

There is a science to determine the exact size of an antenna but there are so many variables that in general it is best to get a general idea after which a degree of 'Try it and see' is unavoidable.

If the reader is located in a position where there is a lot of heavy interference then less range cannot be avoided. In this situation the coil should be made smaller to increase the field strength and coupling.

It is difficult to give actual examples of coils for hand wounding because the closeness and tightness of the winding will significantly change the inductance. A professionally wound coil will have much more inductance than a similar hand wound coil.

For those who want a starting point into practical antenna winding it was found that 63 turns on a 120mm diameter former gave an inductance of 1.08mH. For those contemplating adding an additional tuning capacitor it was found that 50 turns on a 120mm diameter former gave 700uH. The wire diameter is not important.
Anybody who wishes to be more theoretical we recommend a trip to the Microchip Website where we found an application sheet for Loop Antennas.
http://ww1.microchip.com/downloads/en/AppNotes/00831b.pdf

The Tuning Capacitor

It is recommended that the internal 1n% capacitor is used for tuning, however a capacitor may be also be added externally. The combined capacitance should not exceed 2n7. Do not forget that the choice of tuning capacitor can also substantially affect the quality of your system. The Id12 is basically an ID2 with an internal antenna. The loss in an ID12 series antenna is required to be fairly high to limit the series current. A low Q will hide a lot of the shortcomings of the capacitor, but for quality and reliability and repeatability the following capacitors are recommend.

Polypropylene	Good Readily available. Ensure AC voltage at 125kHz is sufficient.
COG/NPO	Excellent. Best Choice
Silver Mica	Excellent but expensive
Polycarbonate	Good Readily available. Ensure AC voltage at 125kHz is sufficient.

Voltage Working.

A capacitor capable of withstanding the RMS voltage at 125KHz MUST be chosen. The working voltage will depend on the coil design. I suggest the designer start with rugged 1n5 Polypropylene 630v capacitor to do his experiments and the come down to a suitable size/value. The capacitor manufacturer will supply information on their capacitors. Do not simply go by the DC voltage. This means little. A tolerance of 2% is preferable. A tolerance of 5% is acceptable.

Fine Tuning

We recommend using an oscilloscope for fine-tuning. Connect the oscilloscope to observe the 125KHz AC voltage across the coil. Get a sizeable piece of ferrite and bring it up to the antenna loop. If the voltage increases then you need more inductance (or more capacitance). If the voltage decreases as you bring the ferrite up to the antenna then the inductance is too great. If you have no ferrite then a piece of aluminum

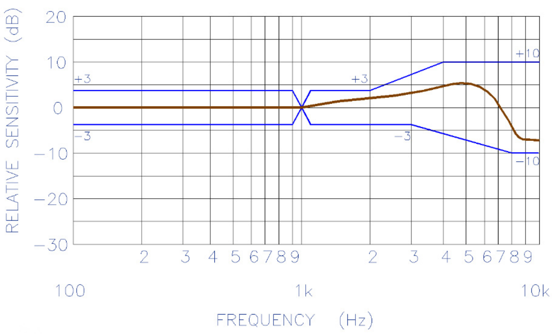
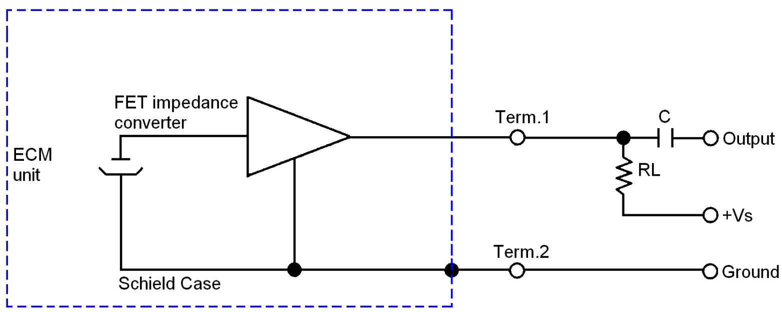
sheet may be used for testing in a slightly different way. Opposing currents will flow in the aluminum and it will act as a negative inductance. If the 125kH AC voltage increases as the aluminum sheet approaches the antenna then the inductance is too high. Note it may be possible that the voltage will first maximize then decrease. This simply means that you are near optimum tuning. If you are using ferrite then the coil is a little under value and if you are using an aluminum sheet then the coil is a over under value.

ID Innovations
Advanced Digital Reader Technology
----*Better by Design*

This specification applies to the electret condenser microphone outlined within this document.

Model Number: **MD9745APZ-F**

I. Electrical Characteristics Test Condition (Vs= 2.0 V, RL= 2.2 k ohm, Ta=20°C, RH=65%)

ITEM	SYMBOL	TEST CONDITION	MINIMUM	STANDARD	MAXIMUM	UNITS
Sensitivity	S	f=1kHz, Pin=1Pa	-46	-44	-42	dB 0dB=1V/Pa
Impedance	Zout	f=1kHz, Pin=1Pa			2.2	kΩ
Directivity			OMNI-DIRECTIONAL			
Current Consumption	I				0.5	mA
S/N Ratio	S/N (A)	f=1kHz, Pin=1Pa A Curve	55			dB
Sensitivity Reduction	ΔS	f=1kHz, Pin=1Pa Vs= 2.0 - 1.5			-3	dB
Frequency Range			100-10,000			Hz
Frequency Response						
Schematic Diagram of Circuit						

II. Mechanical Characteristics

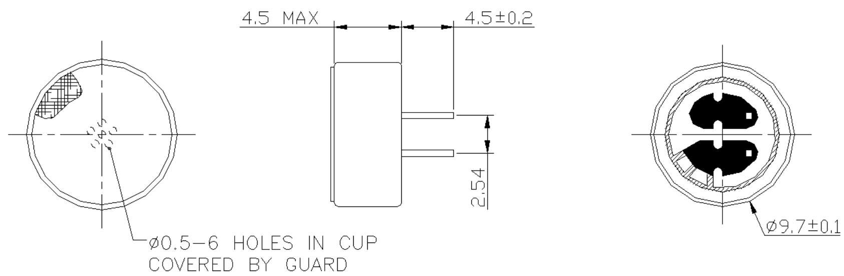
Dimensions	∅ 9.7 x 4.5	See Drawing in Section IV		
Weight	Less than 1.0g			
Soldering Heat Shock	To be no interferance in operation after soldering temperature exposure at 260°C +/-5°C for 2 +/- 0.5 seconds.			
Terminal Mechanical Strength	Not Applicable			
Absolute Maximum Ratings	Operating Voltage	Storage Temperature Range	Operation Temperature Range	
	Vs (V)	Tstg °C	Tope °C	
	10	-25°C to +60°C	-25°C to +55°C	

III. Reliability Tests

Note: After any of the following tests performed, the sensitivity of the microphone unit shall not deviate more than ±3dB from its initial value. The microphone shall maintain its initial operation and appearance. Measurements for tests with thermal requirements are to be done after 2hrs of condistioning at 20°C.

Vibration Test	The microphone to have no interferance in operation after vibrations, 10Hz to 55Hz for 1 minute full amplitude 1.52mm, for 2 hours at three axises.	
Drop Test	The microphone unit must operate when dropped three times once on each axis from a height of 1m onto a metal plate.	
Temperature Test	High	The microphone unit must operate within its sensitivity specifications after subjected to the following conditions: +60°C for 240 hrs, and exposed to room temperature for 2 hrs.
	Low	The microphone unit must operate within its sensitivity specifications after subjected to the following conditions: -25°C for 240 hrs, and exposed to room temperature for 2 hrs.
Humidity Test	+40°C at 95%RH for 240 hrs	
Temperature Cycle Test	After exposure at -25°C for 30 minutes, at+20°C for 10 minutes, at +60°C for 30 minutes, at +20°C for 10 minutes, 5 cycles. (The measurement to be done after 2 hrs of conditioning at +20°C.)	

IV. Dimensional Drawing



V. Other

Freescale Semiconductor
Technical Data

Document Number: MMA7361L
Rev 0, 04/2008

RoHS

±1.5g, ±6g Three Axis Low-g Micromachined Accelerometer

The MMA7361L is a low power, low profile capacitive micromachined accelerometer featuring signal conditioning, a 1-pole low pass filter, temperature compensation, self test, 0g-Detect which detects linear freefall, and g-Select which allows for the selection between 2 sensitivities. Zero-g offset and sensitivity are factory set and require no external devices. The MMA7361L includes a Sleep Mode that makes it ideal for handheld battery powered electronics.

Features

- 3mm x 5mm x 1.0mm LGA-14 Package
- Low Current Consumption: 400 μA
- Sleep Mode: 3 μA
- Low Voltage Operation: 2.2 V – 3.6 V
- High Sensitivity (800 mV/g @ 1.5g)
- Selectable Sensitivity (±1.5g, ±6g)
- Fast Turn On Time (0.5 ms Enable Response Time)
- Self Test for Freefall Detect Diagnosis
- 0g-Detect for Freefall Protection
- Signal Conditioning with Low Pass Filter
- Robust Design, High Shocks Survivability
- RoHS Compliant
- Environmentally Preferred Product
- Low Cost

Typical Applications

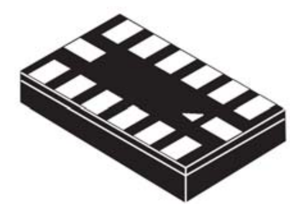
- 3D Gaming: Tilt and Motion Sensing, Event Recorder
- HDD MP3 Player: Freefall Detection
- Laptop PC: Freefall Detection, Anti-Theft
- Cell Phone: Image Stability, Text Scroll, Motion Dialing, E-Compass
- Pedometer: Motion Sensing
- PDA: Text Scroll
- Navigation and Dead Reckoning: E-Compass Tilt Compensation
- Robotics: Motion Sensing

ORDERING INFORMATION				
Part Number	**Temperature Range**	**Package Drawing**	**Package**	**Shipping**
MMA7361LT	–40 to +85°C	1977-01	LGA-14	Tray
MMA7361LR1	–40 to +85°C	1977-01	LGA-14	7” Tape & Reel
MMA7361LR2	–40 to +85°C	1977-01	LGA-14	13” Tape & Reel

MMA7361L

MMA7361L: XYZ AXIS ACCELEROMETER
±1.5g, ±6g

Bottom View



14 LEAD
LGA
CASE 1977-01

Top View

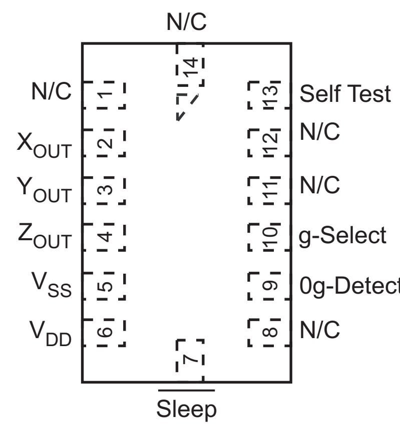


Figure 1. Pin Connections

freescale™ semiconductor

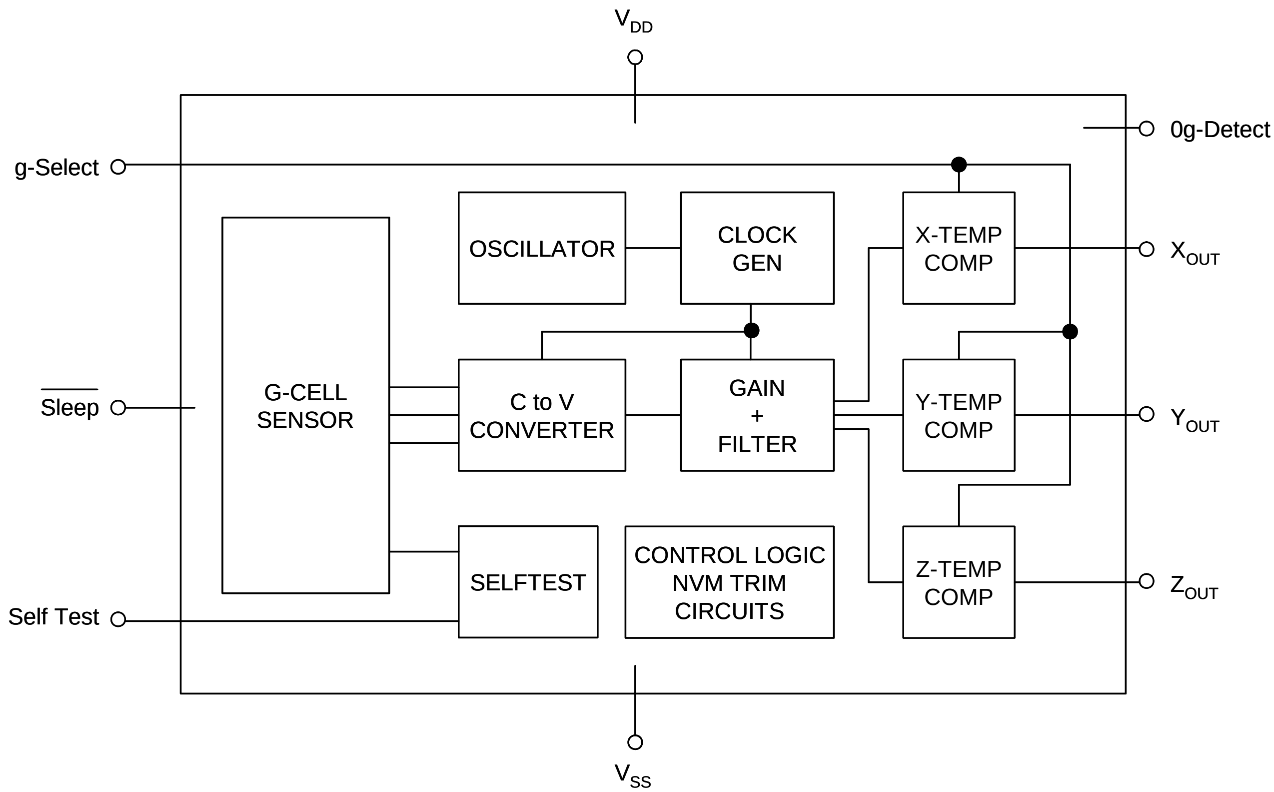


Figure 2. Simplified Accelerometer Functional Block Diagram

Table 1. Maximum Ratings
(Maximum ratings are the limits to which the device can be exposed without causing permanent damage.)

Rating	Symbol	Value	Unit
Maximum Acceleration (all axis)	g_{max}	±5000	g
Supply Voltage	V_{DD}	–0.3 to +3.6	V
Drop Test[1]	D_{drop}	1.8	m
Storage Temperature Range	T_{stg}	–40 to +125	°C

1. Dropped onto concrete surface from any axis.

ELECTRO STATIC DISCHARGE (ESD)

WARNING: This device is sensitive to electrostatic discharge.

Although the Freescale accelerometer contains internal 2000 V ESD protection circuitry, extra precaution must be taken by the user to protect the chip from ESD. A charge of over 2000 volts can accumulate on the human body or associated test equipment. A charge of this magnitude can alter the performance or cause failure of the chip. When handling the accelerometer, proper ESD precautions should be followed to avoid exposing the device to discharges which may be detrimental to its performance.

Table 2. Operating Characteristics
Unless otherwise noted: -40°C ≤ T_A ≤ 85°C, 2.2 V ≤ V_{DD} ≤ 3.6 V, Acceleration = 0g, Loaded output**(1)**

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Range(2)					
Supply Voltage(3)	V_{DD}	2.2	3.3	3.6	V
Supply Current(4)	I_{DD}	—	400	600	μA
Supply Current at Sleep Mode(4)	I_{DD}	—	3	10	μA
Operating Temperature Range	T_A	-40	—	+85	°C
Acceleration Range, X-Axis, Y-Axis, Z-Axis					
g-Select: 0	g_{FS}	—	±1.5	—	g
g-Select: 1	g_{FS}	—	±6.0	—	g
Output Signal					
Zero-g (T_A = 25°C, V_{DD} = 3.3 V)(5), (6)	V_{OFF}	1.485	1.65	1.815	V
Zero-g(4)	V_{OFF}, T_A	-2.0	±0.5	+2.0	mg/°C
Sensitivity (T_A = 25°C, V_{DD} = 3.3 V)					
1.5g	$S_{1.5g}$	740	800	860	mV/g
6g	S_{6g}	190.6	206	221.5	mV/g
Sensitivity(4)	S,T_A	-0.0075	±0.002	+0.0075	%/°C
Bandwidth Response					
XY	f_{-3dBXY}	—	400	—	Hz
Z	f_{-3dBZ}	—	300	—	Hz
Output Impedance	Z_O	—	32	—	kΩ
0g-Detect	$0g_{detect}$	-0.4	0	+0.4	g
Self Test					
Output Response					
X_{OUT}, Y_{OUT}	Δg_{STXY}	+0.05	-0.1	—	g
Z_{OUT}	Δg_{STZ}	+0.8	+1.0	+1.2	g
Input Low	V_{IL}	V_{SS}	—	0.3 V_{DD}	V
Input High	V_{IH}	0.7 V_{DD}	—	V_{DD}	V
Noise					
Power Spectral Density RMS (0.1 Hz – 1 kHz)(4)	n_{PSD}	—	350	—	$\mu g/\sqrt{Hz}$
Control Timing					
Power-Up Response Time(7)	$t_{RESPONSE}$	—	1.0	2.0	ms
Enable Response Time(8)	t_{ENABLE}	—	0.5	2.0	ms
Self Test Response Time(9)	t_{ST}	—	2.0	5.0	ms
Sensing Element Resonant Frequency					
XY	$f_{GCELLXY}$	—	6.0	—	kHz
Z	f_{GCELLZ}	—	3.4	—	kHz
Internal Sampling Frequency	f_{CLK}	—	11	—	kHz
Output Stage Performance					
Full-Scale Output Range (I_{OUT} = 3 μA)	V_{FSO}	V_{SS}+0.1	—	V_{DD}–0.1	V
Nonlinearity, X_{OUT}, Y_{OUT}, Z_{OUT}	NL_{OUT}	-1.0	—	+1.0	%FSO
Cross-Axis Sensitivity(10)	$V_{XY, XZ, YZ}$	-5.0	—	+5.0	%

1. For a loaded output, the measurements are observed after an RC filter consisting of an internal 32kΩ resistor and an external 3.3nF capacitor (recommended as a minimum to filter clock noise) on the analog output for each axis and a 0.1μF capacitor on V_{DD} - GND. The output sensor bandwidth is determined by the Capacitor added on the output. f = 1/2π * (32 x 10^3) * C. C = 3.3 nF corresponds to BW = 1507HZ, which is the minimum to filter out internal clock noise.
2. These limits define the range of operation for which the part will meet specification.
3. Within the supply range of 2.2 and 3.6 V, the device operates as a fully calibrated linear accelerometer. Beyond these supply limits the device may operate as a linear device but is not guaranteed to be in calibration.
4. This value is measured with g-Select in 1.5g mode.
5. The device can measure both + and – acceleration. With no input acceleration the output is at midsupply. For positive acceleration the output will increase above V_{DD}/2. For negative acceleration, the output will decrease below V_{DD}/2.
6. For optimal 0g offset performance, adhere to AN3484 and AN3447
7. The response time between 10% of full scale V_{DD} input voltage and 90% of the final operating output voltage.
8. The response time between 10% of full scale Sleep Mode input voltage and 90% of the final operating output voltage.
9. The response time between 10% of the full scale self test input voltage and 90% of the self test output voltage.
10. A measure of the device's ability to reject an acceleration applied 90° from the true axis of sensitivity.

PRINCIPLE OF OPERATION

The Freescale accelerometer is a surface-micromachined integrated-circuit accelerometer.

The device consists of a surface micromachined capacitive sensing cell (g-cell) and a signal conditioning ASIC contained in a single package. The sensing element is sealed hermetically at the wafer level using a bulk micromachined cap wafer.

The g-cell is a mechanical structure formed from semiconductor materials (polysilicon) using semiconductor processes (masking and etching). It can be modeled as a set of beams attached to a movable central mass that move between fixed beams. The movable beams can be deflected from their rest position by subjecting the system to an acceleration (Figure 3).

As the beams attached to the central mass move, the distance from them to the fixed beams on one side will increase by the same amount that the distance to the fixed beams on the other side decreases. The change in distance is a measure of acceleration.

The g-cell beams form two back-to-back capacitors (Figure 3). As the center beam moves with acceleration, the distance between the beams changes and each capacitor's value will change, ($C = A\varepsilon/D$). Where A is the area of the beam, ε is the dielectric constant, and D is the distance between the beams.

The ASIC uses switched capacitor techniques to measure the g-cell capacitors and extract the acceleration data from the difference between the two capacitors. The ASIC also signal conditions and filters (switched capacitor) the signal, providing a high level output voltage that is ratiometric and proportional to acceleration.

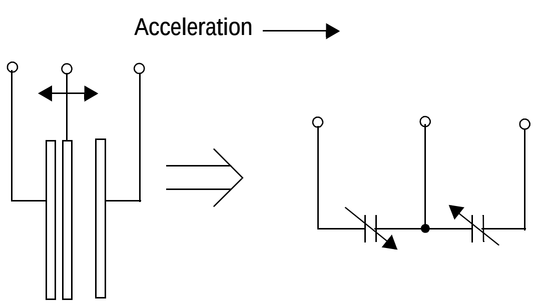


Figure 3. Simplified Transducer Physical Model

SPECIAL FEATURES

0g-Detect

The sensor offers a 0g-Detect feature that provides a logic high signal when all three axes are at 0g. This feature enables the application of Linear Freefall protection if the signal is connected to an interrupt pin or a poled I/O pin on a microcontroller.

Self Test

The sensor provides a self test feature that allows the verification of the mechanical and electrical integrity of the accelerometer at any time before or after installation. This feature is critical in applications such as hard disk drive protection where system integrity must be ensured over the life of the product. Customers can use self test to verify the solderability to confirm that the part was mounted to the PCB correctly. To use this feature to verify the 0g-Detect function, the accelerometer should be held upside down so that the z-axis experiences -1g. When the self test function is initiated, an electrostatic force is applied to each axis to cause it to deflect. The x- and y-axis are deflected slightly while the z-axis is trimmed to deflect 1g. This procedure assures that both the mechanical (g-cell) and electronic sections of the accelerometer are functioning.

g-Select

The g-Select feature allows for the selection between two sensitivities. Depending on the logic input placed on pin 10, the device internal gain will be changed allowing it to function with a 1.5g or 6g sensitivity (Table 3). This feature is ideal when a product has applications requiring two different sensitivities for optimum performance. The sensitivity can be changed at anytime during the operation of the product. The g-Select pin can be left unconnected for applications requiring only a 1.5g sensitivity as the device has an internal pull-down to keep it at that sensitivity (800mV/g)).

Table 3. g-Select Pin Description

g-Select	g-Range	Sensitivity
0	1.5g	800 mV/g
1	6g	206 mV/g

Sleep Mode

The 3 axis accelerometer provides a Sleep Mode that is ideal for battery operated products. When Sleep Mode is active, the device outputs are turned off, providing significant reduction of operating current. A low input signal on pin 7 (Sleep Mode) will place the device in this mode and reduce the current to 3 μA typ. For lower power consumption, it is recommended to set g-Select to 1.5g mode. By placing a high input signal on pin 7, the device will resume to normal mode of operation.

Filtering

The 3 axis accelerometer contains an onboard single-pole switched capacitor filter. Because the filter is realized using switched capacitor techniques, there is no requirement for external passive components (resistors and capacitors) to set the cut-off frequency.

Ratiometricity

Ratiometricity simply means the output offset voltage and sensitivity will scale linearly with applied supply voltage. That is, as supply voltage is increased, the sensitivity and offset increase linearly; as supply voltage decreases, offset and sensitivity decrease linearly. This is a key feature when interfacing to a microcontroller or an A/D converter because it provides system level cancellation of supply induced errors in the analog to digital conversion process.

BASIC CONNECTIONS

Pin Descriptions

Top View

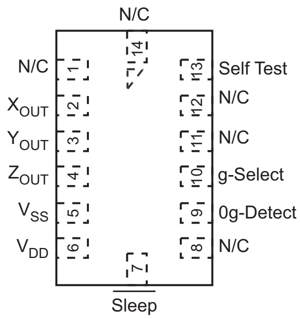


Figure 4. Pinout Description

Table 4. Pin Descriptions

Pin No.	Pin Name	Description
1	N/C	No internal connection Leave unconnected
2	X_{OUT}	X direction output voltage
3	Y_{OUT}	Y direction output voltage
4	Z_{OUT}	Z direction output voltage
5	V_{SS}	Power Supply Ground
6	V_{DD}	Power Supply Input
7	$\overline{\text{Sleep}}$	Logic input pin to enable product or Sleep Mode
8	NC	No internal connection Leave unconnected
9	0g-Detect	Linear Freefall digital logic output signal
10	g-Select	Logic input pin to select g level
11	N/C	Unused for factory trim Leave unconnected
12	N/C	Unused for factory trim Leave unconnected
13	Self Test	Input pin to initiate Self Test
14	N/C	Unused for factory trim Leave unconnected

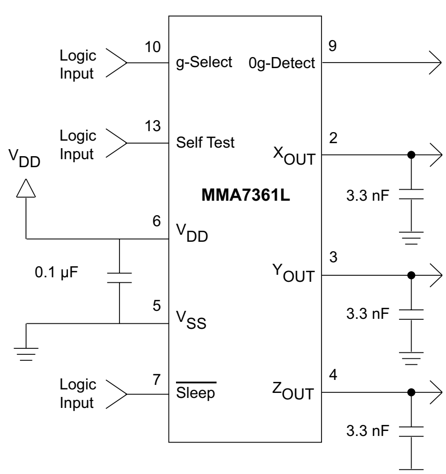


Figure 5. Accelerometer with Recommended Connection Diagram

PCB Layout

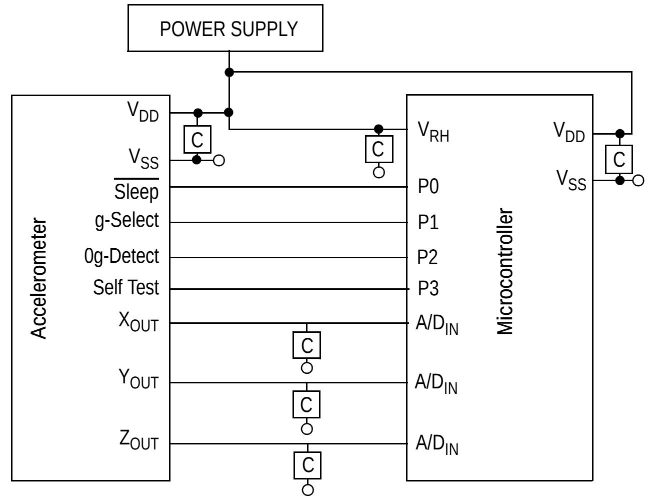
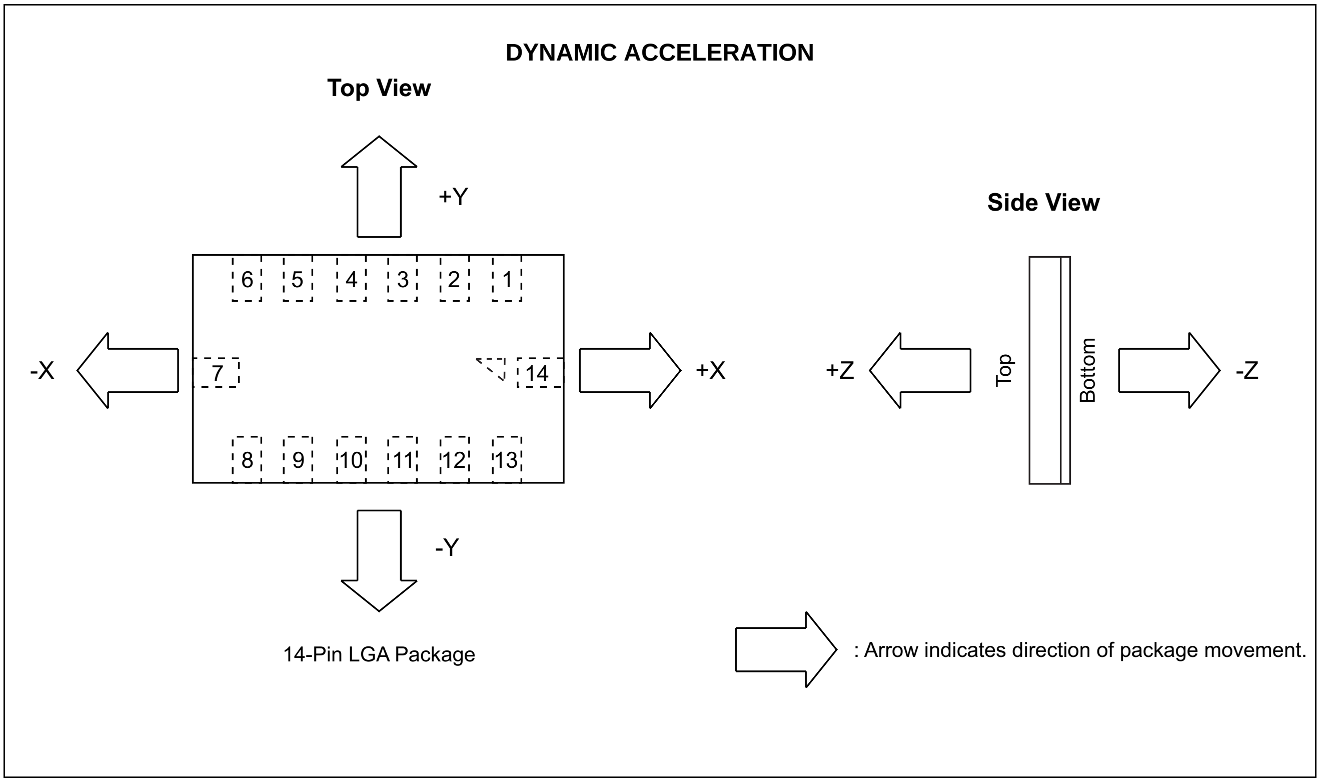
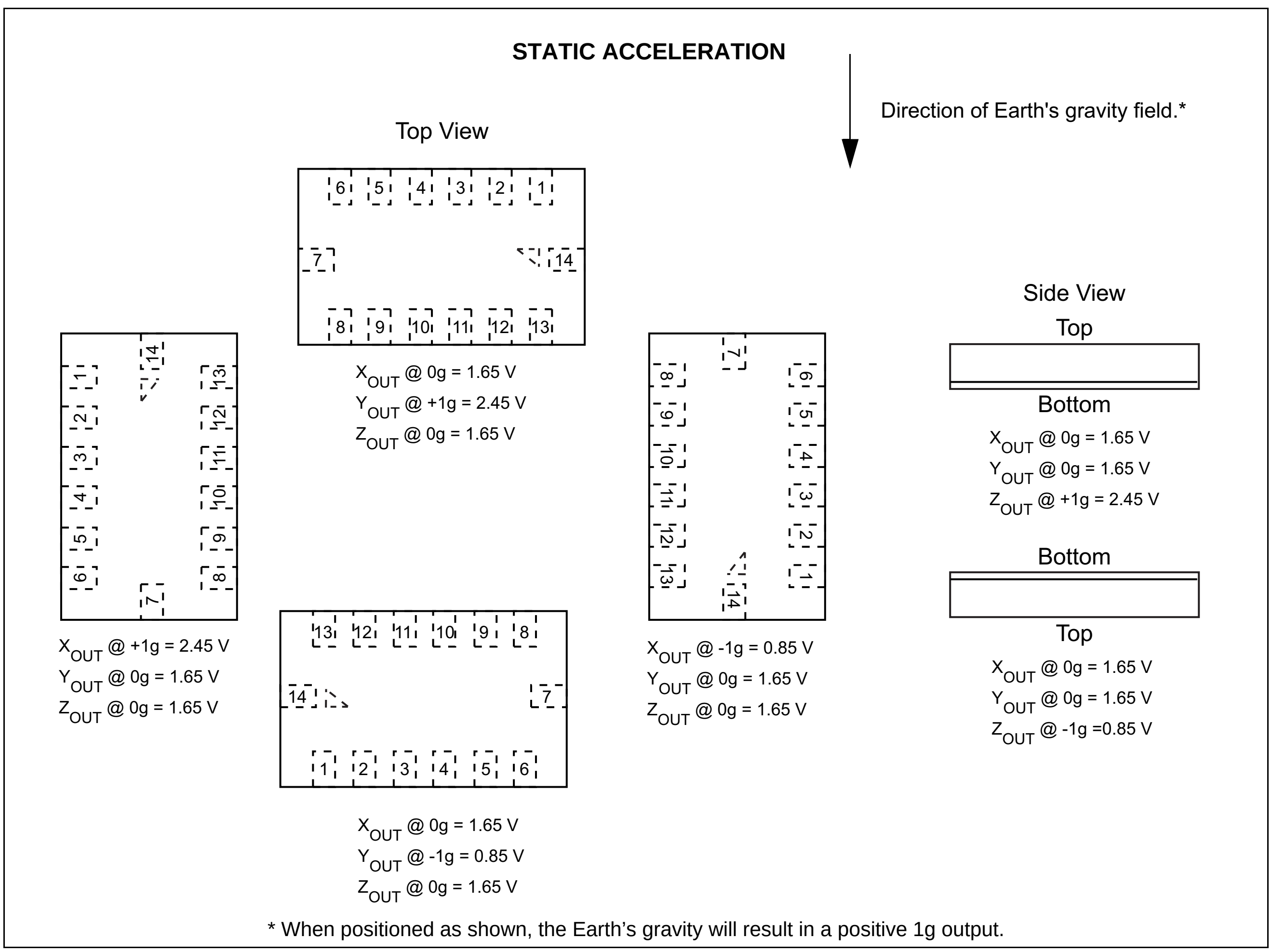


Figure 6. Recommended PCB Layout for Interfacing Accelerometer to Microcontroller

NOTES:

1. Use 0.1 µF capacitor on V_{DD} to decouple the power source.
2. Physical coupling distance of the accelerometer to the microcontroller should be minimal.
3. Place a ground plane beneath the accelerometer to reduce noise, the ground plane should be attached to all of the open ended terminals shown in Figure 6.
4. Use a 3.3nF capacitor on the outputs of the accelerometer to minimize clock noise (from the switched capacitor filter circuit).
5. PCB layout of power and ground should not couple power supply noise.
6. Accelerometer and microcontroller should not be a high current path.
7. A/D sampling rate and any external power supply switching frequency should be selected such that they do not interfere with the internal accelerometer sampling frequency (11 kHz for the sampling frequency). This will prevent aliasing errors.
8. 10MΩ or higher is recommended on X_{OUT}, Y_{OUT} and Z_{OUT} to prevent loss due to the voltage divider relationship between the internal 32 kΩ resistor and the measurement input impedance.


DYNAMIC ACCELERATION
Top View
+Y
-X
+X
-Y
14-Pin LGA Package
Side View
+Z
Top
Bottom
-Z
: Arrow indicates direction of package movement.


STATIC ACCELERATION
Direction of Earth's gravity field.*
Top View
X_{OUT} @ 0g = 1.65 V
Y_{OUT} @ +1g = 2.45 V
Z_{OUT} @ 0g = 1.65 V
X_{OUT} @ +1g = 2.45 V
Y_{OUT} @ 0g = 1.65 V
Z_{OUT} @ 0g = 1.65 V
X_{OUT} @ 0g = 1.65 V
Y_{OUT} @ -1g = 0.85 V
Z_{OUT} @ 0g = 1.65 V
X_{OUT} @ -1g = 0.85 V
Y_{OUT} @ 0g = 1.65 V
Z_{OUT} @ 0g = 1.65 V
Side View
Top
Bottom
X_{OUT} @ 0g = 1.65 V
Y_{OUT} @ 0g = 1.65 V
Z_{OUT} @ +1g = 2.45 V
Bottom
Top
X_{OUT} @ 0g = 1.65 V
Y_{OUT} @ 0g = 1.65 V
Z_{OUT} @ -1g =0.85 V
* When positioned as shown, the Earth's gravity will result in a positive 1g output.

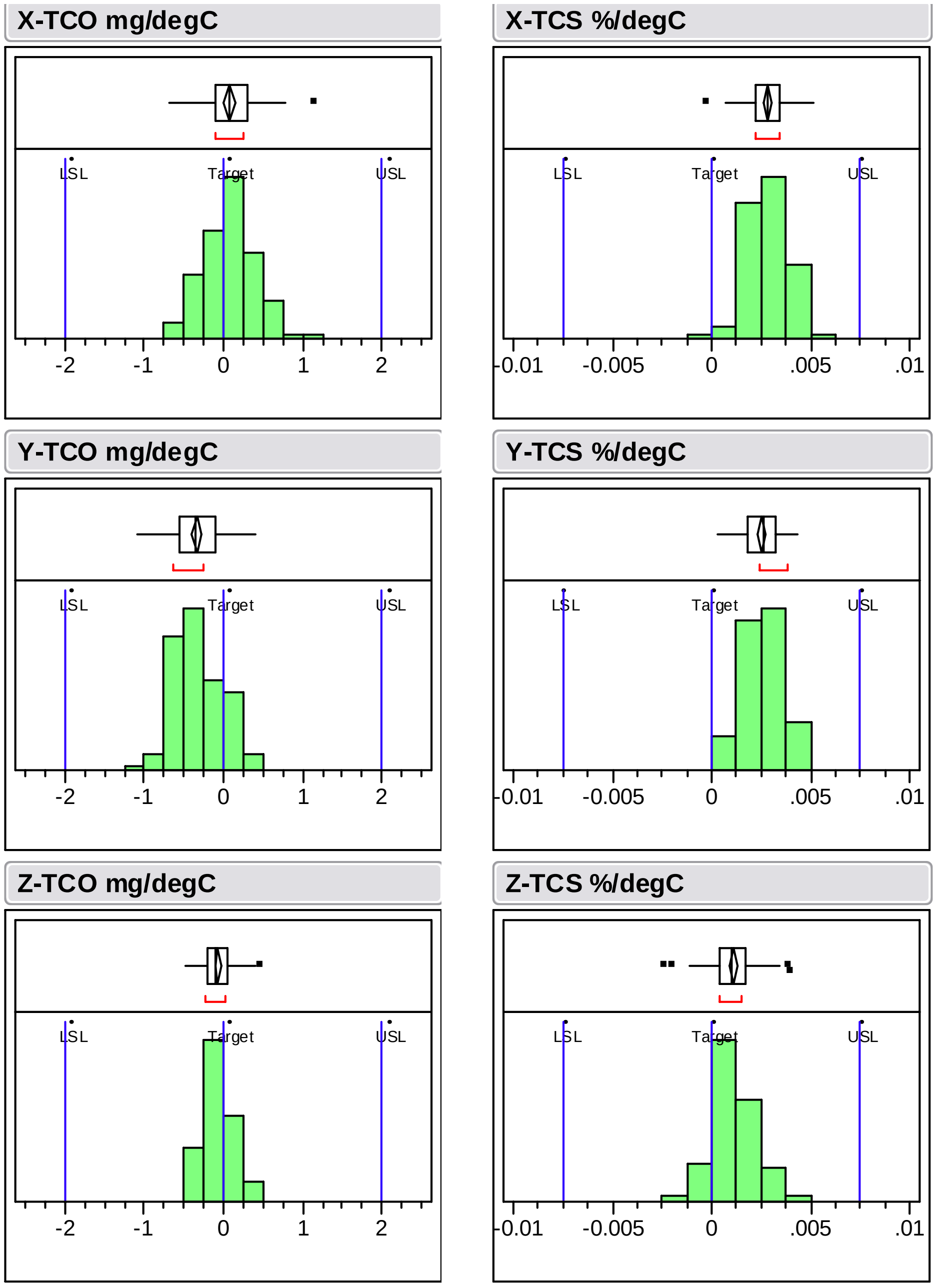


Figure 7. MMA7361L Temperature Coefficient of Offset (TCO) and Temperature Coefficient of Sensitivity (TCS) Distribution Charts

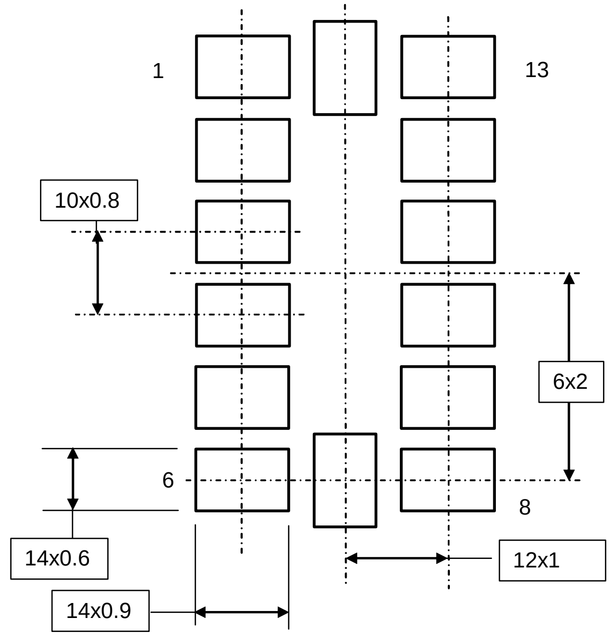
MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

PCB Mounting Recommendations

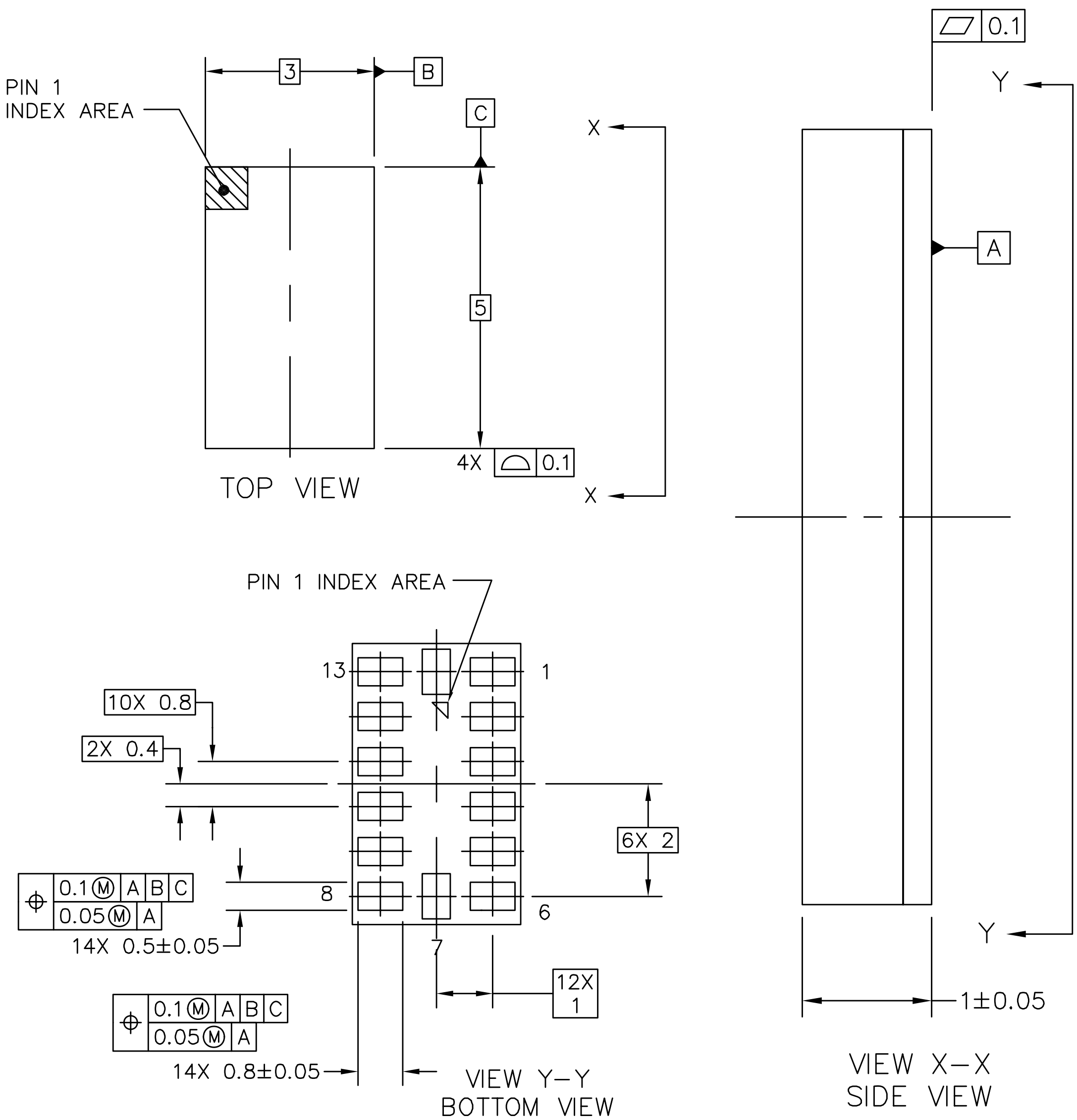
MEMS based sensors are sensitive to Printed Circuit Board (PCB) reflow processes. For optimal zero-g offset after PCB mounting, care must be taken to PCB layout and reflow conditions. Reference application note AN3484 for best practices to minimize the zero-g offset shift after PCB mounting.

Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the board and the package.

With the correct footprint, the packages will self-align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder pads.



PACKAGE DIMENSIONS



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	CASE NUMBER: 1977–01	09 JAN 2008
	STANDARD: NON–JEDEC	

CASE 1977-01
ISSUE A
14-LEAD LGA

PACKAGE DIMENSIONS

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M—1994.

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CASE 1977-01
ISSUE A
14-LEAD LGA

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MMA7361L
Rev. 0
04/2008

SSD1306

Advance Information

128 x 64 Dot Matrix
OLED/PLED Segment/Common Driver with Controller

CONTENTS

TABLES

FIGURES

1 GENERAL DESCRIPTION

SSD1306 is a single-chip CMOS OLED/PLED driver with controller for organic / polymer light emitting diode dot-matrix graphic display system. It consists of 128 segments and 64commons. This IC is designed for Common Cathode type OLED panel.

The SSD1306 embeds with contrast control, display RAM and oscillator, which reduces the number of external components and power consumption. It has 256-step brightness control. Data/Commands are sent from general MCU through the hardware selectable 6800/8000 series compatible Parallel Interface, I^2C interface or Serial Peripheral Interface. It is suitable for many compact portable applications, such as mobile phone sub-display, MP3 player and calculator, etc.

2 FEATURES

- Resolution: 128 x 64 dot matrix panel
- Power supply
  - V_{DD} = 1.65V to 3.3V for IC logic
  - V_{CC} = 7V to 15V for Panel driving
- For matrix display
  - OLED driving output voltage, 15V maximum
  - Segment maximum source current: 100uA
  - Common maximum sink current: 15mA
  - 256 step contrast brightness current control
- Embedded 128 x 64 bit SRAM display buffer
- Pin selectable MCU Interfaces:
  - 8-bit 6800/8080-series parallel interface
  - 3 /4 wire Serial Peripheral Interface
  - I^2C Interface
- Screen saving continuous scrolling function in both horizontal and vertical direction
- RAM write synchronization signal
- Programmable Frame Rate and Multiplexing Ratio
- Row Re-mapping and Column Re-mapping
- On-Chip Oscillator
- Chip layout for COG & COF
- Wide range of operating temperature: -40°C to 85°C

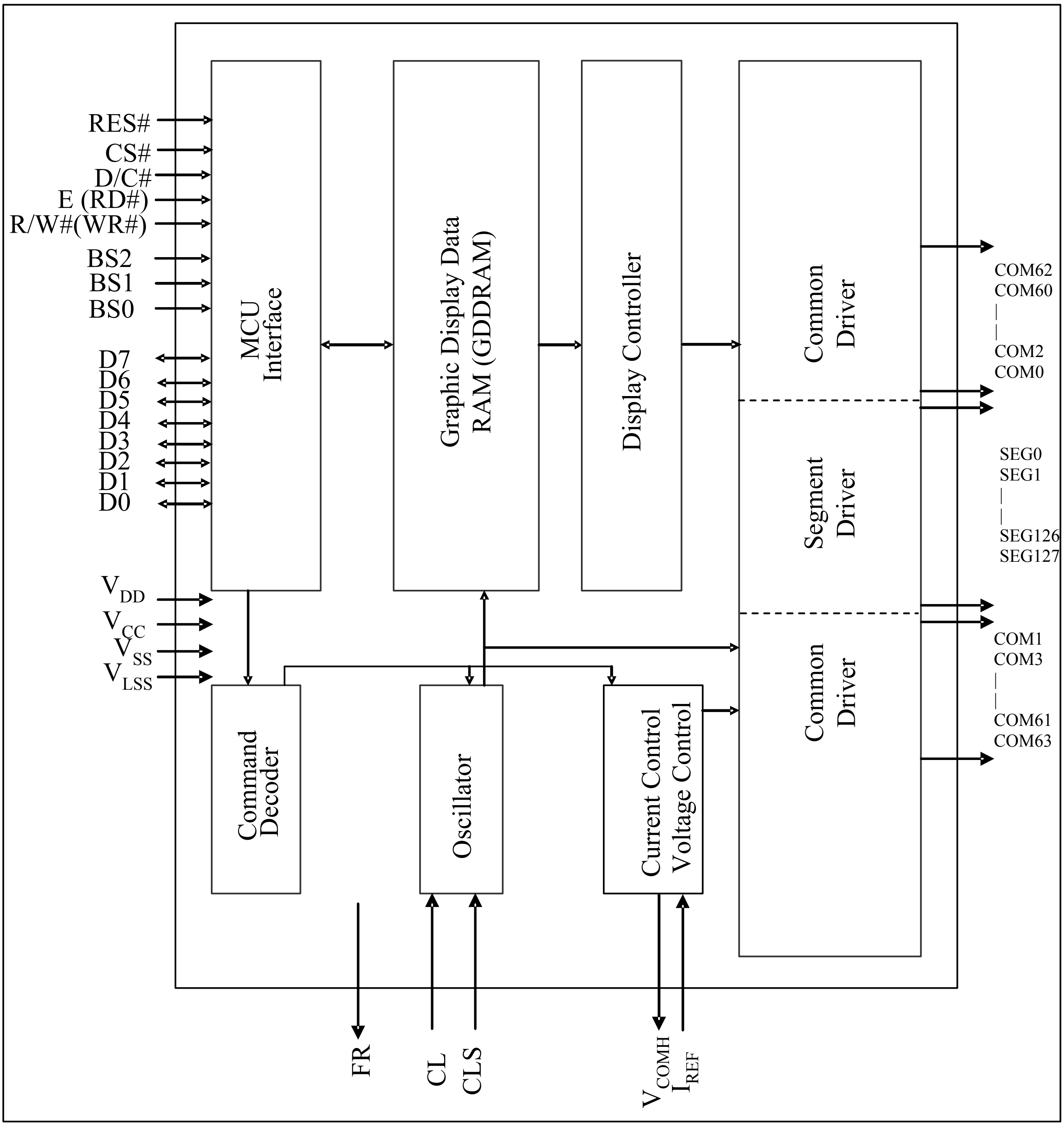
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1306Z	128	64	COG	8	o Min SEG pad pitch : 47um o Min COM pad pitch : 40um o Die thickness: 300 +/- 25um
SSD1306TR1	104	48	TAB	11, 56	o 35mm film, 4 sprocket hole, Folding TAB o 8-bit 80 / 8-bit 68 / SPI / I^2C interface o SEG, COM lead pitch 0.1mm x 0.997 =0.0997mm o Die thickness: 457 +/- 25um

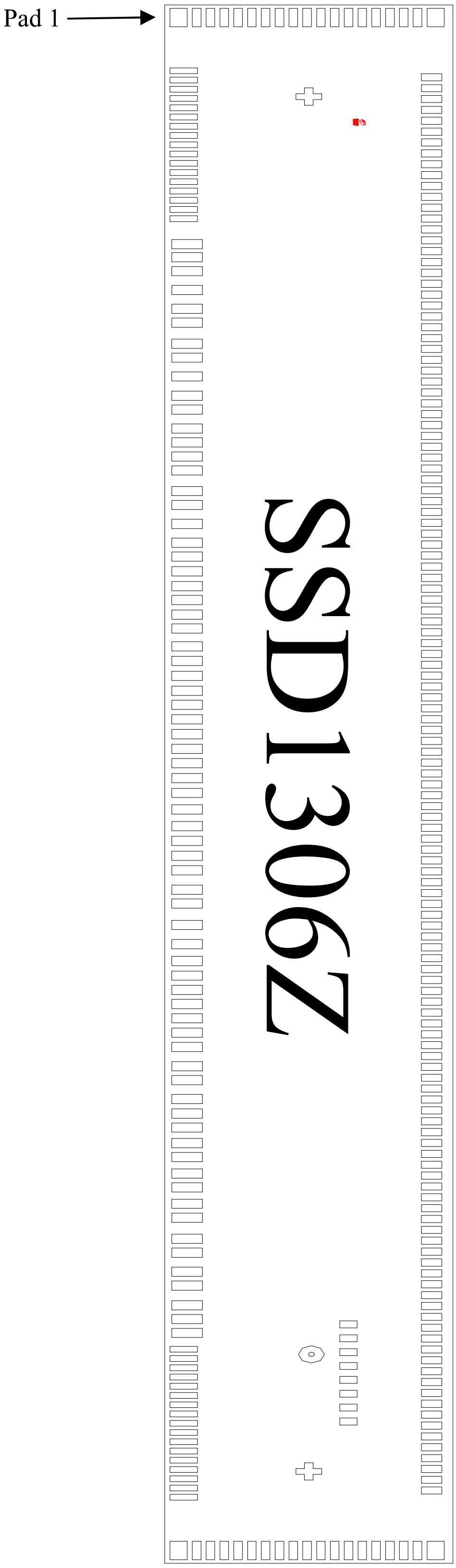
4 BLOCK DIAGRAM

Figure 4-1 SSD1306 Block Diagram



5 DIE PAD FLOOR PLAN

Figure 5-1 : SSD1306Z Die Drawing



Die size	6.76mm x 0.86mm
Die thickness	300 +/- 25um
Min I/O pad pitch	60um
Min SEG pad pitch	47um
Min COM pad pitch	40um
Bump height	Nominal 15um

Bump size	
Pad 1, 106, 124, 256	80um x 50um
Pad 2-18, 89-105, 107-123, 257-273	25ium x 80um
Pad 19-88	40um x 89um
Pad 125-255	31um x 59um
Pad 274-281 (TR pads)	30um x 50um

Alignment mark	Position	Size
+ shape	(-2973, 0)	75um x 75um
+ shape	(2973, 0)	75um x 75um
Circle	(2466.665, 7.575)	R37.5um, inner 18um
SSL Logo	(-2862.35, 144.82)	-

(For details dimension please see p.9)

Note

(1) Diagram showing the Gold bumps face up.
(2) Coordinates are referenced to center of the chip.
(3) Coordinate units and size of all alignment marks are in um.
(4) All alignment keys do not contain gold

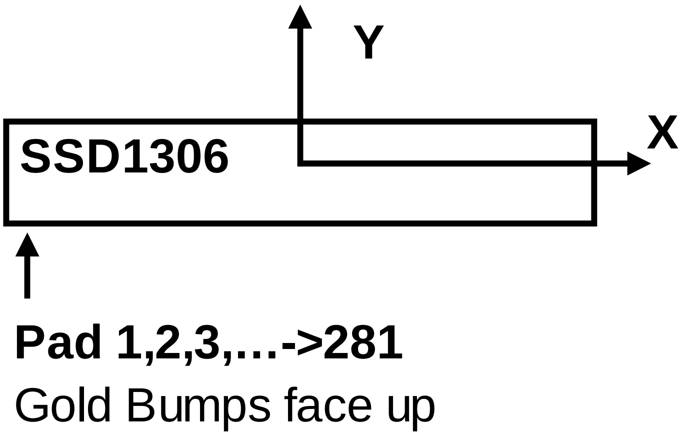
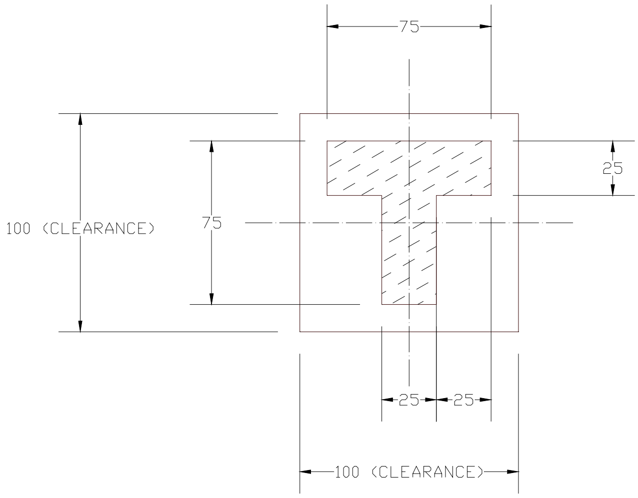
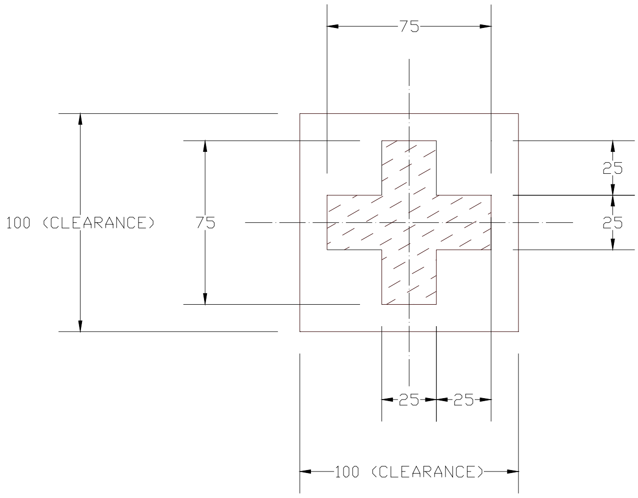


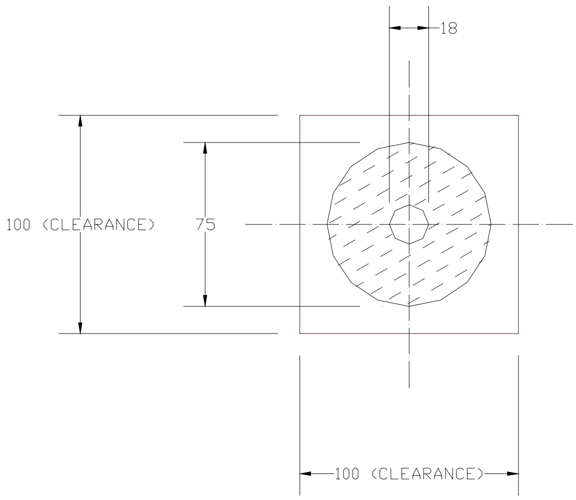
Figure 5-2 : SSD1306Z alignment mark dimensions



T shape



+ shape



Circle

*All units are in um

Table 5-1 : SSD1306Z Bump Die Pad Coordinates

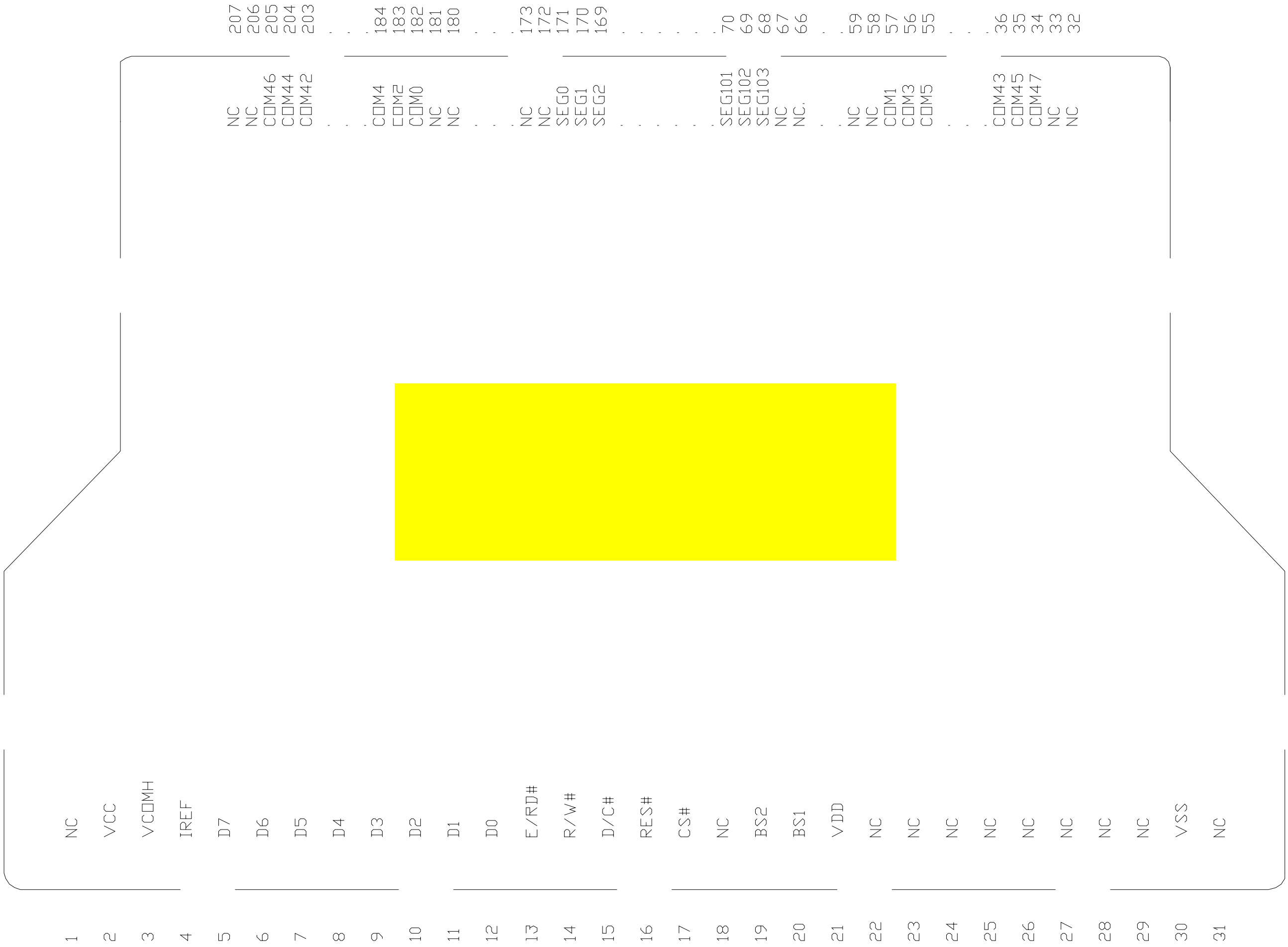
Pad no.	Pad Name	X-pos	Y-pos
1	NC	-3315	-377.5
2	VSS	-3084.77	-362.5
3	COM49	-3044.77	-362.5
4	COM50	-3004.77	-362.5
5	COM51	-2964.77	-362.5
6	COM52	-2924.77	-362.5
7	COM53	-2884.77	-362.5
8	COM54	-2844.77	-362.5
9	COM55	-2804.77	-362.5
10	COM56	-2764.77	-362.5
11	COM57	-2724.77	-362.5
12	COM58	-2684.77	-362.5
13	COM59	-2644.77	-362.5
14	COM60	-2604.77	-362.5
15	COM61	-2564.77	-362.5
16	COM62	-2524.77	-362.5
17	COM63	-2484.77	-362.5
18	VCOMH	-2444.77	-362.5
19	NC	-2334.965	-352.83
20	C2P	-2278.265	-352.83
21	C2P	-2218.265	-352.83
22	C2N	-2136.715	-352.83
23	C2N	-2055.465	-352.83
24	C1P	-1995.465	-352.83
25	C1P	-1904.115	-352.83
26	C1N	-1844.115	-352.83
27	C1N	-1762.865	-352.83
28	VBAT	-1679.31	-352.83
29	VBAT	-1619.31	-352.83
30	VBREF	-1537.51	-352.83
31	BGGND	-1477.51	-352.83
32	VCC	-1416.01	-352.83
33	VCC	-1356.01	-352.83
34	VCOMH	-1266.955	-352.83
35	VCOMH	-1206.955	-352.83
36	VLSS	-1125.155	-352.83
37	VLSS	-1043.355	-352.83
38	VLSS	-983.355	-352.83
39	VSS	-920	-352.83
40	VSS	-856	-352.83
41	VSS	-796	-352.83
42	VDD	-732.645	-352.83
43	VDD	-672.645	-352.83
44	BS0	-595.655	-352.83
45	VSS	-531.955	-352.83
46	BS1	-467.655	-352.83
47	VDD	-403.155	-352.83
48	VDD	-342.555	-352.83
49	BS2	-279.705	-352.83
50	VSS	-215.705	-352.83
51	FR	-151.955	-352.83
52	CL	-89.815	-352.83
53	VSS	-25.665	-352.83
54	CS#	38.635	-352.83
55	RES#	109.835	-352.83
56	D/C#	182.425	-352.83
57	VSS	246.125	-352.83
58	R/W#	310.425	-352.83
59	E	373.125	-352.83
60	VDD	457.175	-352.83
61	VDD	517.175	-352.83
62	D0	609.275	-352.83
63	D1	692.475	-352.83
64	D2	765.675	-352.83
65	D3	828.875	-352.83
66	VSS	890.325	-352.83
67	D4	951.275	-352.83
68	D5	1013.315	-352.83
69	D6	1075.355	-352.83
70	D7	1137.395	-352.83
71	VSS	1220.735	-352.83
72	VSS	1280.735	-352.83
73	CLS	1362.585	-352.83
74	VDD	1425.285	-352.83
75	VDD	1485.885	-352.83
76	VDD	1553.185	-352.83
77	VDD	1613.185	-352.83
78	IREF	1684.585	-352.83
79	IREF	1744.585	-352.83
80	VCOMH	1815.585	-352.83
81	VCOMH	1875.585	-352.83
82	VCC	1967.185	-352.83
83	VCC	2027.185	-352.83
84	VLSS	2109.185	-352.83
85	VLSS	2169.185	-352.83
86	VLSS	2254.185	-352.83
87	NC	2314.185	-352.83
88	NC	2374.185	-352.83
89	VSS	2444.77	-362.5
90	COM31	2484.77	-362.5
91	COM30	2524.77	-362.5
92	COM29	2564.77	-362.5
93	COM28	2604.77	-362.5
94	COM27	2644.77	-362.5
95	COM26	2684.77	-362.5
96	COM25	2724.77	-362.5
97	COM24	2764.77	-362.5
98	COM23	2804.77	-362.5
99	COM22	2844.77	-362.5
100	COM21	2884.77	-362.5
101	COM20	2924.77	-362.5
102	COM19	2964.77	-362.5
103	COM18	3004.77	-362.5
104	COM17	3044.77	-362.5
105	VSS	3084.77	-362.5
106	NC	3315	-377.5
107	COM16	3315	-325
108	COM15	3315	-285
109	COM14	3315	-245
110	COM13	3315	-205
111	COM12	3315	-165
112	COM11	3315	-125
113	COM10	3315	-85
114	COM9	3315	-45
115	COM8	3315	-5
116	COM7	3315	35
117	COM6	3315	75
118	COM5	3315	115
119	COM4	3315	155
120	COM3	3315	195
121	COM2	3315	235
122	COM1	3315	275
123	COM0	3315	315
124	NC	3315	367.5
125	NC	3055.5	356
126	SEG0	3009.5	356
127	SEG1	2962.5	356
128	SEG2	2915.5	356
129	SEG3	2868.5	356
130	SEG4	2821.5	356
131	SEG5	2774.5	356
132	SEG6	2727.5	356
133	SEG7	2680.5	356
134	SEG8	2633.5	356
135	SEG9	2586.5	356
136	SEG10	2539.5	356
137	SEG11	2492.5	356
138	SEG12	2445.5	356
139	SEG13	2398.5	356
140	SEG14	2351.5	356
141	SEG15	2304.5	356
142	SEG16	2257.5	356
143	SEG17	2210.5	356
144	SEG18	2163.5	356
145	SEG19	2116.5	356
146	SEG20	2069.5	356
147	SEG21	2022.5	356
148	SEG22	1975.5	356
149	SEG23	1928.5	356
150	SEG24	1881.5	356
151	SEG25	1834.5	356
152	SEG26	1787.5	356
153	SEG27	1740.5	356
154	SEG28	1693.5	356
155	SEG29	1646.5	356
156	SEG30	1599.5	356
157	SEG31	1552.5	356
158	SEG32	1505.5	356
159	SEG33	1458.5	356
160	SEG34	1411.5	356
161	SEG35	1364.5	356
162	SEG36	1317.5	356
163	SEG37	1270.5	356
164	SEG38	1223.5	356
165	SEG39	1176.5	356
166	SEG40	1129.5	356
167	SEG41	1082.5	356
168	SEG42	1035.5	356
169	SEG43	988.5	356
170	SEG44	941.5	356
171	SEG45	894.5	356
172	SEG46	847.5	356
173	SEG47	800.5	356
174	SEG48	753.5	356
175	SEG49	706.5	356
176	SEG50	659.5	356
177	SEG51	612.5	356
178	SEG52	565.5	356
179	SEG53	518.5	356
180	SEG54	471.5	356
181	SEG55	424.5	356
182	SEG56	377.5	356
183	SEG57	330.5	356
184	SEG58	283.5	356
185	SEG59	236.5	356
186	SEG60	189.5	356
187	SEG61	142.5	356
188	SEG62	95.5	356
189	SEG63	48.5	356
190	SEG64	1.5	356
191	SEG65	-45.5	356
192	SEG66	-92.5	356
193	SEG67	-139.5	356
194	SEG68	-186.5	356
195	SEG69	-233.5	356
196	SEG70	-280.5	356
197	SEG71	-327.5	356
198	SEG72	-374.5	356
199	SEG73	-421.5	356
200	SEG74	-468.5	356
201	SEG75	-515.5	356
202	SEG76	-562.5	356
203	SEG77	-609.5	356
204	SEG78	-656.5	356
205	SEG79	-703.5	356
206	SEG80	-750.5	356
207	SEG81	-797.5	356
208	SEG82	-844.5	356
209	SEG83	-891.5	356
210	NC	-940	356
211	SEG84	-988.5	356
212	SEG85	-1035.5	356
213	SEG86	-1082.5	356
214	SEG87	-1129.5	356
215	SEG88	-1176.5	356
216	SEG89	-1223.5	356
217	SEG90	-1270.5	356
218	SEG91	-1317.5	356
219	SEG92	-1364.5	356
220	SEG93	-1411.5	356
221	SEG94	-1458.5	356
222	SEG95	-1505.5	356
223	SEG96	-1552.5	356
224	SEG97	-1599.5	356
225	SEG98	-1646.5	356
226	SEG99	-1693.5	356
227	SEG100	-1740.5	356
228	SEG101	-1787.5	356
229	SEG102	-1834.5	356
230	SEG103	-1881.5	356
231	SEG104	-1928.5	356
232	SEG105	-1975.5	356
233	SEG106	-2022.5	356
234	SEG107	-2069.5	356
235	SEG108	-2116.5	356
236	SEG109	-2163.5	356
237	SEG110	-2210.5	356
238	SEG111	-2257.5	356
239	SEG112	-2304.5	356
240	SEG113	-2351.5	356
241	SEG114	-2398.5	356
242	SEG115	-2445.5	356
243	SEG116	-2492.5	356
244	SEG117	-2539.5	356
245	SEG118	-2586.5	356
246	SEG119	-2633.5	356
247	SEG120	-2680.5	356
248	SEG121	-2727.5	356
249	SEG122	-2774.5	356
250	SEG123	-2821.5	356
251	SEG124	-2868.5	356
252	SEG125	-2915.5	356
253	SEG126	-2962.5	356
254	SEG127	-3009.5	356
255	NC	-3056.5	356
256	NC	-3315	367.5
257	COM32	-3315	315
258	COM33	-3315	275
259	COM34	-3315	235
260	COM35	-3315	195
261	COM36	-3315	155
262	COM37	-3315	115
263	COM38	-3315	75
264	COM39	-3315	35
265	COM40	-3315	-5
266	COM41	-3315	-45
267	COM42	-3315	-85
268	COM43	-3315	-125
269	COM44	-3315	-165
270	COM45	-3315	-205
271	COM46	-3315	-245
272	COM47	-3315	-285
273	COM48	-3315	-325

Pad no.	Pad Name	X-pos	Y-pos
Pin#	Pin name	X-dir	Y-dir
274	TR0	2757.05	114.8
275	TR1	2697.05	114.8
276	TR2	2637.05	114.8
277	TR3	2577.05	114.8
278	VSS	2517.05	114.8
279	TR4	2457.05	114.8
280	TR5	2397.05	114.8
281	TR6	2337.05	114.8

6 PIN ARRANGEMENT

6.1 SSD1306TR1 pin assignment

Figure 6-1 : SSD1306TR1 Pin Assignment



Note:
(1) COM sequence (Split) is under command setting: DAh, 12h

Table 6-1 : SSD1306TR1 Pin Assignment Table

Pin no.	Pin Name	Pin no.	Pin Name	Pin no.	Pin Name
1	NC	81	SEG90	161	SEG10
2	VCC	82	SEG89	162	SEG9
3	VCOMH	83	SEG88	163	SEG8
4	IREF	84	SEG87	164	SEG7
5	D7	85	SEG86	165	SEG6
6	D6	86	SEG85	166	SEG5
7	D5	87	SEG84	167	SEG4
8	D4	88	SEG83	168	SEG3
9	D3	89	SEG82	169	SEG2
10	D2	90	SEG81	170	SEG1
11	D1	91	SEG80	171	SEG0
12	D0	92	SEG79	172	NC
13	E/RD#	93	SEG78	173	NC
14	R/W#	94	SEG77	174	NC
15	D/C#	95	SEG76	175	NC
16	RES#	96	SEG75	176	NC
17	CS#	97	SEG74	177	NC
18	NC	98	SEG73	178	NC
19	BS2	99	SEG72	179	NC
20	BS1	100	SEG71	180	NC
21	VDD	101	SEG70	181	NC
22	NC	102	SEG69	182	COM0
23	NC	103	SEG68	183	COM2
24	NC	104	SEG67	184	COM4
25	NC	105	SEG66	185	COM6
26	NC	106	SEG65	186	COM8
27	NC	107	SEG64	187	COM10
28	NC	108	SEG63	188	COM12
29	NC	109	SEG62	189	COM14
30	VSS	110	SEG61	190	COM16
31	NC	111	SEG60	191	COM18
32	NC	112	SEG59	192	COM20
33	NC	113	SEG58	193	COM22
34	COM47	114	SEG57	194	COM24
35	COM45	115	SEG56	195	COM26
36	COM43	116	SEG55	196	COM28
37	COM41	117	SEG54	197	COM30
38	COM39	118	SEG53	198	COM32
39	COM37	119	SEG52	199	COM34
40	COM35	120	SEG51	200	COM36
41	COM33	121	SEG50	201	COM38
42	COM31	122	SEG49	202	COM40
43	COM29	123	SEG48	203	COM42
44	COM27	124	SEG47	204	COM44
45	COM25	125	SEG46	205	COM46
46	COM23	126	SEG45	206	NC
47	COM21	127	SEG44	207	NC
48	COM19	128	SEG43		
49	COM17	129	SEG42		
50	COM15	130	SEG41		
51	COM13	131	SEG40		
52	COM11	132	SEG39		
53	COM9	133	SEG38		
54	COM7	134	SEG37		
55	COM5	135	SEG36		
56	COM3	136	SEG35		
57	COM1	137	SEG34		
58	NC	138	SEG33		
59	NC	139	SEG32		
60	NC	140	SEG31		
61	NC	141	SEG30		
62	NC	142	SEG29		
63	NC	143	SEG28		
64	NC	144	SEG27		
65	NC	145	SEG26		
66	NC	146	SEG25		
67	NC	147	SEG24		
68	SEG103	148	SEG23		
69	SEG102	149	SEG22		
70	SEG101	150	SEG21		
71	SEG100	151	SEG20		
72	SEG99	152	SEG19		
73	SEG98	153	SEG18		
74	SEG97	154	SEG17		
75	SEG96	155	SEG16		
76	SEG95	156	SEG15		
77	SEG94	157	SEG14		
78	SEG93	158	SEG13		
79	SEG92	159	SEG12		
80	SEG91	160	SEG11		

7 PIN DESCRIPTION

Key:

I = Input	NC = Not Connected
O =Output	Pull LOW= connect to Ground
I/O = Bi-directional (input/output)	Pull HIGH= connect to V_{DD}
P = Power pin	

Figure 7-1 Pin Description

Pin Name	**Type**	**Description**
V_{DD}	P	Power supply pin for core logic operation.
V_{CC}	P	Power supply for panel driving voltage. This is also the most positive power voltage supply pin.
V_{SS}	P	This is a ground pin.
V_{LSS}	P	This is an analog ground pin. It should be connected to V_{SS} externally.
V_{COMH}	O	The pin for COM signal deselected voltage level. A capacitor should be connected between this pin and V_{SS}.
V_{BAT}	P	Reserved pin. It should be connected to $V_{DD.}$
BGGND	P	Reserved pin. It should be connected to ground.
C1P/C1N C2P/C2N	I	Reserved pin. It should be kept NC.
V_{BREF}	P	Reserved pin. It should be kept NC.
BS[2:0]	I	MCU bus interface selection pins. Please refer to **Table 7-1** for the details of setting.
I_{REF}	I	This is segment output current reference pin. A resistor should be connected between this pin and V_{SS} to maintain the I_{REF} current at 12.5 uA. Please refer to **Figure 8-15** for the details of resistor value.
FR	O	This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect. It should be kept NC if it is not used. Please refer to Section **8.4** for details usage.
CL	I	This is external clock input pin. When internal clock is enabled (i.e. HIGH in CLS pin), this pin is not used and should be connected to V_{SS}. When internal clock is disabled (i.e. LOW in CLS pin), this pin is the external clock source input pin.
CLS	I	This is internal clock enable pin. When it is pulled HIGH (i.e. connect to V_{DD}), internal clock is enabled. When it is pulled LOW, the internal clock is disabled; an external clock source must be connected to the CL pin for normal operation.
RES#	I	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin HIGH (i.e. connect to V_{DD}) during normal operation.
CS#	I	This pin is the chip select input. (active LOW).

Pin Name	Type	Description
D/C#	I	This is Data/Command control pin. When it is pulled HIGH (i.e. connect to V_{DD}), the data at D[7:0] is treated as data. When it is pulled LOW, the data at D[7:0] will be transferred to the command register. In I^2C mode, this pin acts as SA0 for slave address selection. When 3-wire serial interface is selected, this pin must be connected to V_{SS}. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams: **Figure 13-1** to **Figure 13-5**.
E (RD#)	I	When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH (i.e. connect to V_{DD}) and the chip is selected. When connecting to an 8080-series microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS}.
R/W#(WR#)	I	This is read / write control input pin connecting to the MCU interface. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH (i.e. connect to V_{DD}) and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS}.
D[7:0]	IO	These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC. When I^2C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.
TR0-TR6	-	Testing reserved pins. It should be kept NC.
SEG0 ~ SEG127	O	These pins provide Segment switch signals to OLED panel. These pins are V_{SS} state when display is OFF.
COM0 ~ COM63	O	These pins provide Common switch signals to OLED panel. They are in high impedance state when display is OFF.
NC	-	This is dummy pin. Do not group or short NC pins together.

Table 7-1 : MCU Bus Interface Pin Selection

SSD1306 Pin Name	I^2C Interface	6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	4-wire Serial interface	3-wire Serial interface
BS0	0	0	0	0	1
BS1	1	0	1	0	0
BS2	0	1	1	0	0

Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DD}

8 FUNCTIONAL BLOCK DESCRIPTIONS

8.1 MCU Interface selection

SSD1306 MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 8-1. Different MCU mode can be set by hardware selection on BS[2:0] pins (please refer to Table 7-1 for BS[2:0] setting).

Table 8-1 : MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**E**	**R/W#**	**CS#**	**D/C#**	**RES#**
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
3-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	Tie LOW	RES#
4-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	D/C#	RES#
I^2C	Tie LOW					SDA_{OUT}	SDA_{IN}	SCL	Tie LOW			SA0	RES#

8.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

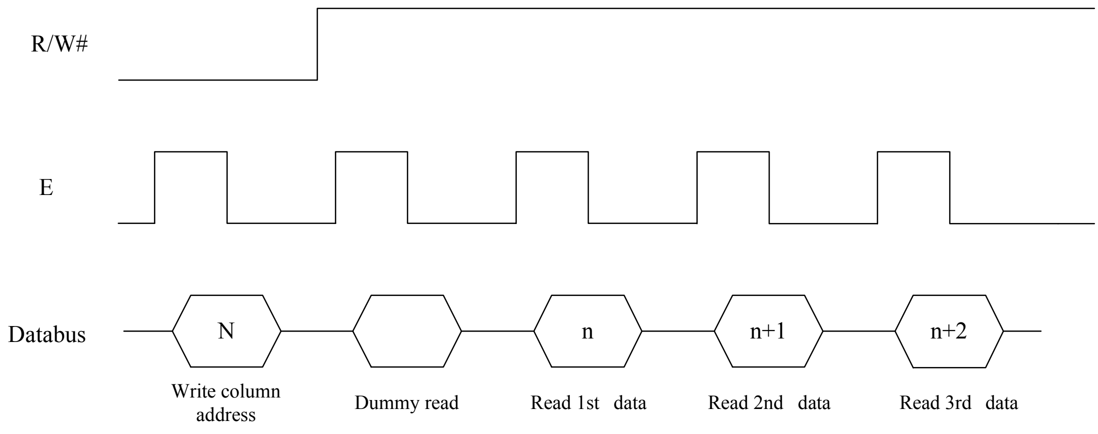
Table 8-2 : Control pins of 6800 interface

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note
(1) ↓ stands for falling edge of signal
H stands for HIGH in signal
L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-1.

Figure 8-1 : Data read back procedure - insertion of dummy read



8.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 8-2 : Example of Write procedure in 8080 parallel interface mode

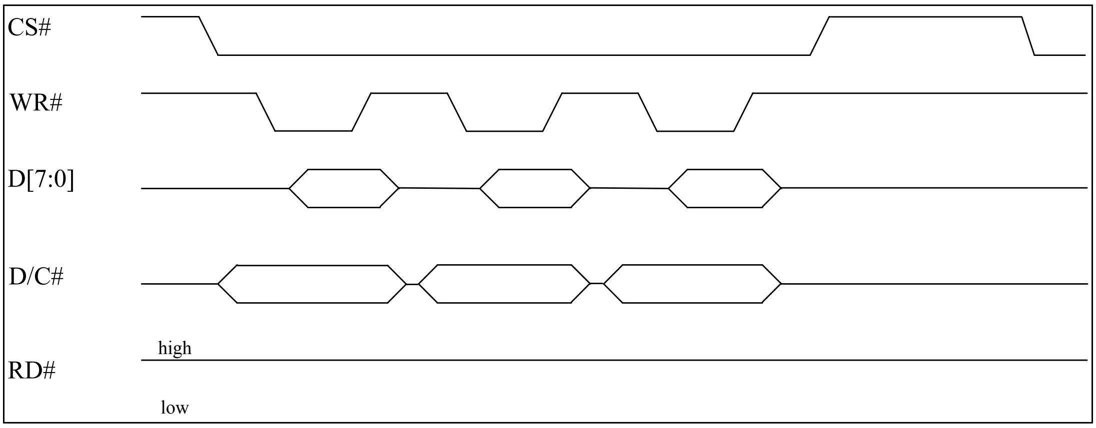


Figure 8-3 : Example of Read procedure in 8080 parallel interface mode

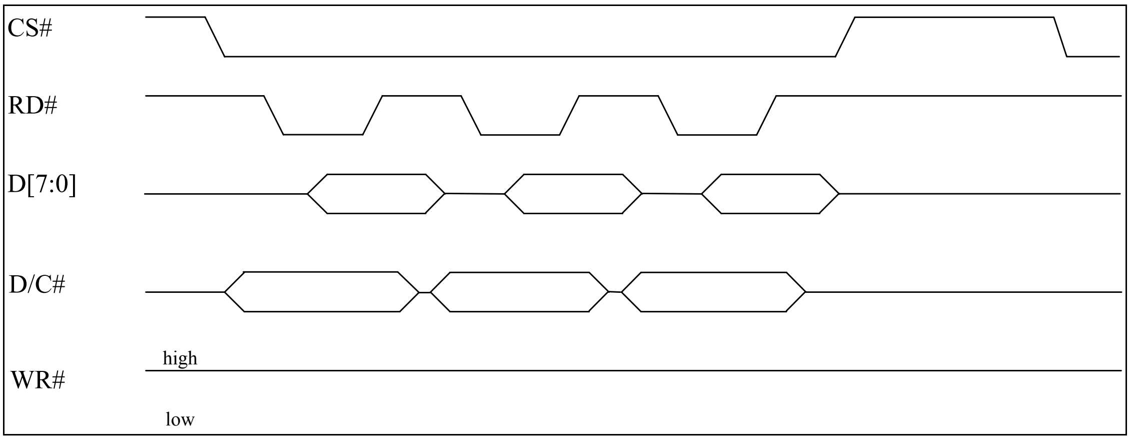


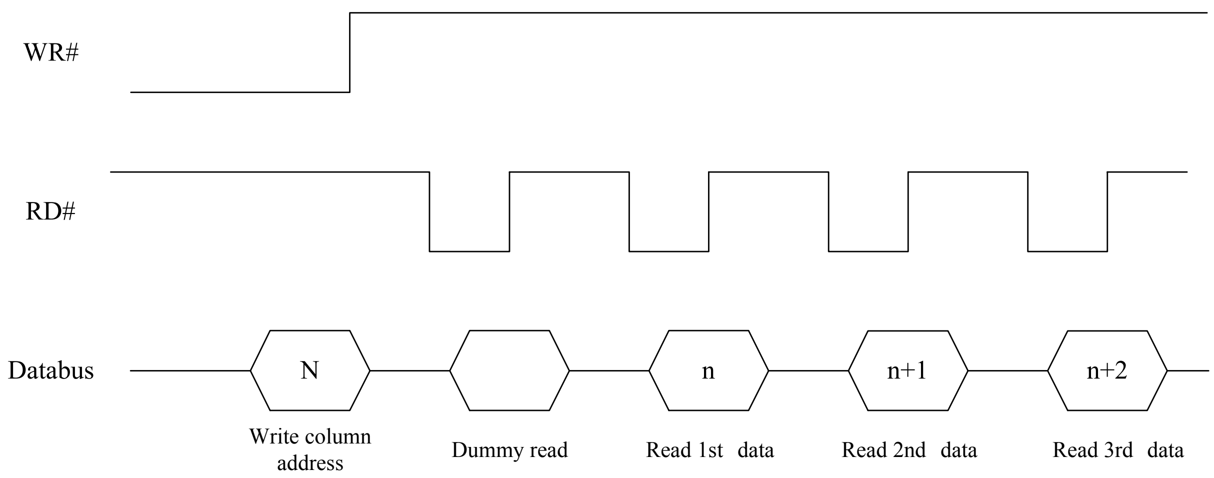
Table 8-3 : Control pins of 8080 interface

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-4.

Figure 8-4 : Display data read back procedure - insertion of dummy read



8.1.3 MCU Serial Interface (4-wire SPI)

The 4-wire serial interface consists of serial clock: SCLK, serial data: SDIN, D/C#, CS#. In 4-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W# (WR#)# can be connected to an external ground.

Table 8-4 : Control pins of 4-wire Serial interface

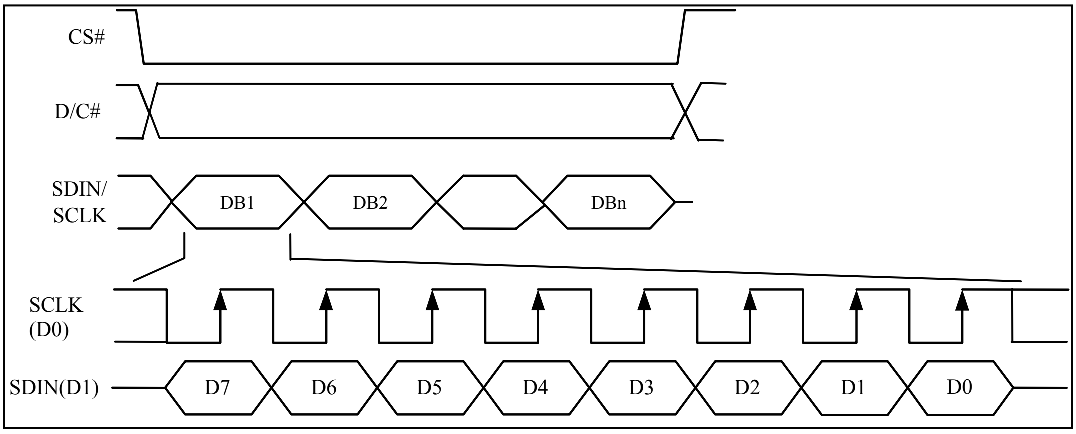
Function	E(RD#)	R/W#(WR#)	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	L	↑
Write data	Tie LOW	Tie LOW	L	H	↑

Note
(1) H stands for HIGH in signal
(2) L stands for LOW in signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 8-5 : Write procedure in 4-wire Serial interface mode



8.1.4 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.
In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, R/W# (WR#)#, E and D/C# can be connected to an external ground.

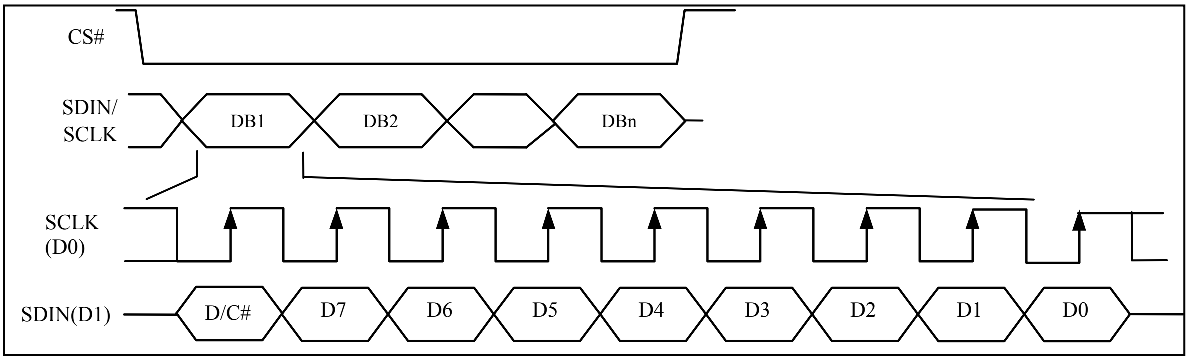
The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Table 8-5 : Control pins of 3-wire Serial interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	Tie LOW	↑
Write data	Tie LOW	Tie LOW	L	Tie LOW	↑

Note
(1) L stands for LOW in signal

Figure 8-6 : Write procedure in 3-wire Serial interface mode



8.1.5 MCU I^2C Interface

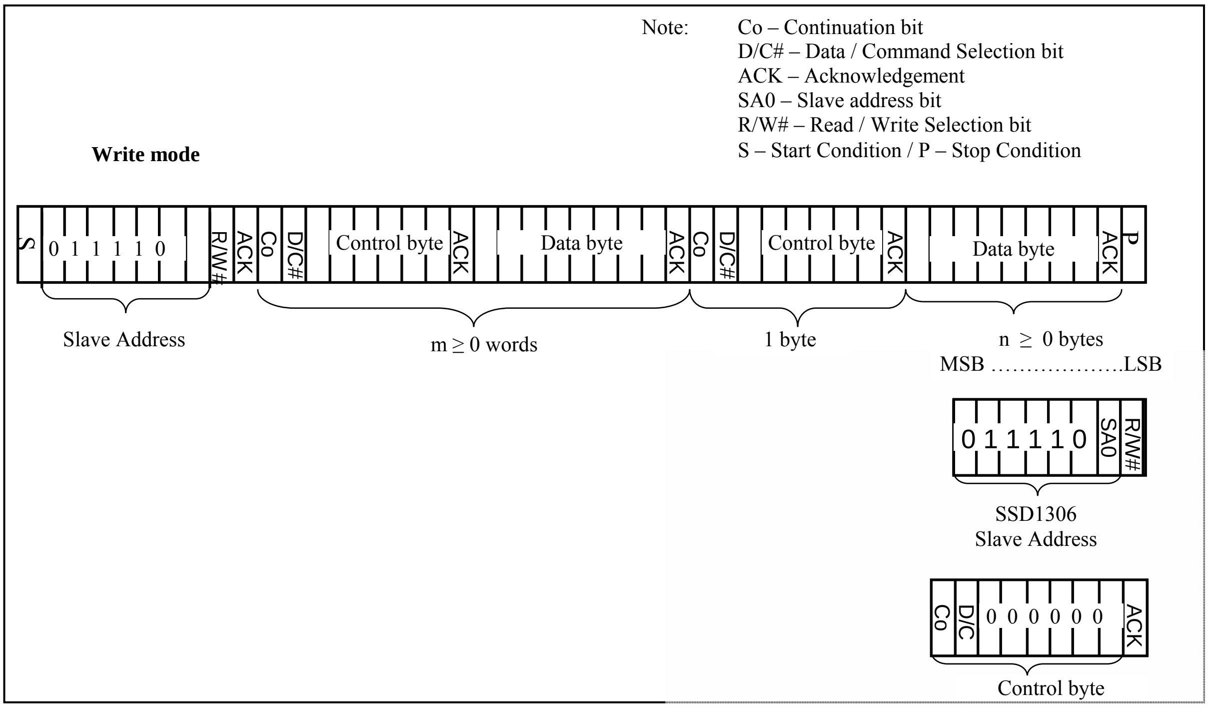
The I^2C communication interface consists of slave address bit SA0, I^2C-bus data signal SDA (SDA_{OUT}/D_2 for output and SDA_{IN}/D_1 for input) and I^2C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)
   SSD1306 has to recognize the slave address before transmitting or receiving any information by the I^2C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,
   b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0
   0 1 1 1 1 0 SA0 R/W#
   "SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1306. D/C# pin acts as SA0 for slave address selection.
   "R/W#" bit is used to determine the operation mode of the I^2C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.
b) I^2C-bus data signal (SDA)
   SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.
   It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".
   "SDA_{IN}" and "SDA_{OUT}" are tied together and serve as SDA. The "SDA_{IN}" pin must be connected to act as SDA. The "SDA_{OUT}" pin may be disconnected. When "SDA_{OUT}" pin is disconnected, the acknowledgement signal will be ignored in the I^2C-bus.
c) I^2C-bus clock signal (SCL)
   The transmission of information in the I^2C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

8.1.5.1 I²C-bus Write data

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 8-7 for the write mode of I²C-bus in chronological order.

Figure 8-7 : I²C-bus data format



8.1.5.2 Write mode for I²C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 8-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD1306, the slave address is either “b0111100” or “b0111101” by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
3) The write mode is established by setting the R/W# bit to logic “0”.
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 8-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six “0” ‘s.
   a. If the Co bit is set as logic “0”, the transmission of the following information will contain data bytes only.
   b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic “0”, it defines the following data byte as a command. If the D/C# bit is set to logic “1”, it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 8-8. The stop condition is established by pulling the “SDA in” from LOW to HIGH while the “SCL” stays HIGH.

Figure 8-8 : Definition of the Start and Stop Condition

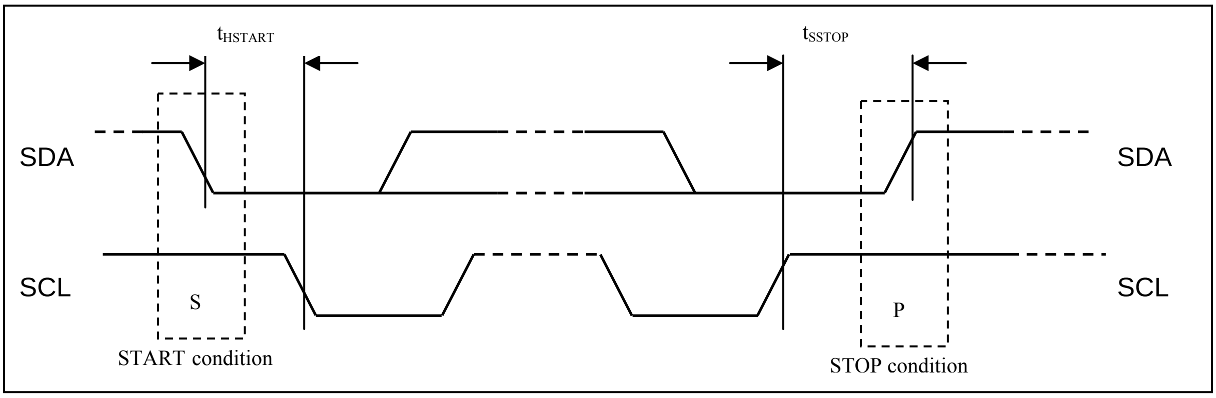
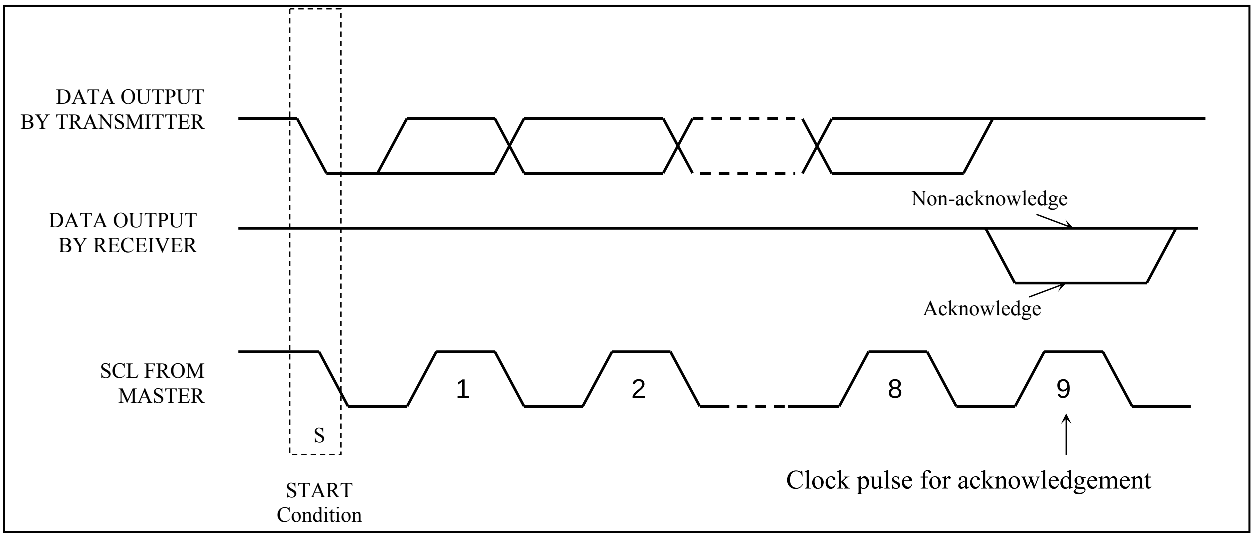


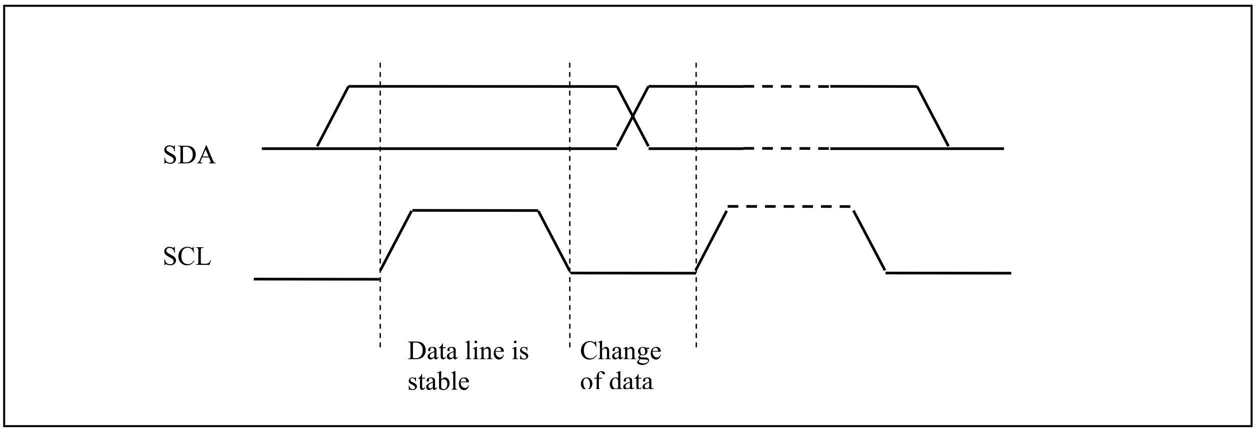
Figure 8-9 : Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 8-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 8-10 : Definition of the data transfer condition



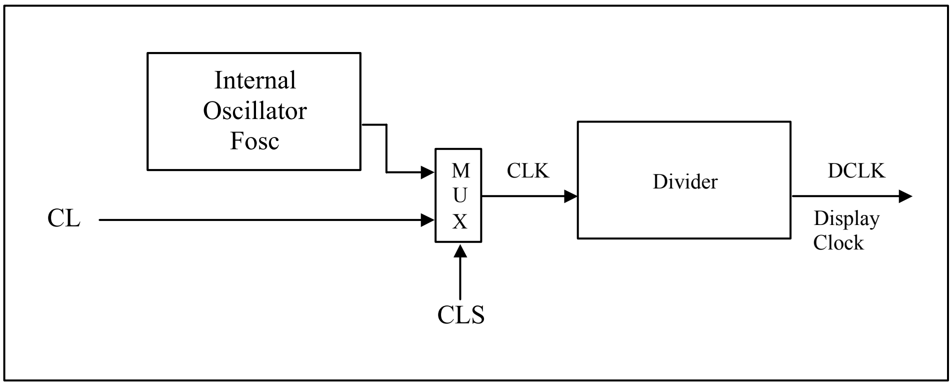
8.2 Command Decoder

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, D[7:0] is interpreted as display data written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D[7:0] is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

8.3 Oscillator Circuit and Display Time Generator

Figure 8-11 : Oscillator Circuit and Display Time Generator



This module is an on-chip LOW power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be left open. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency Fosc can be changed by command D5h A[7:4].

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 16 by command D5h

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula.

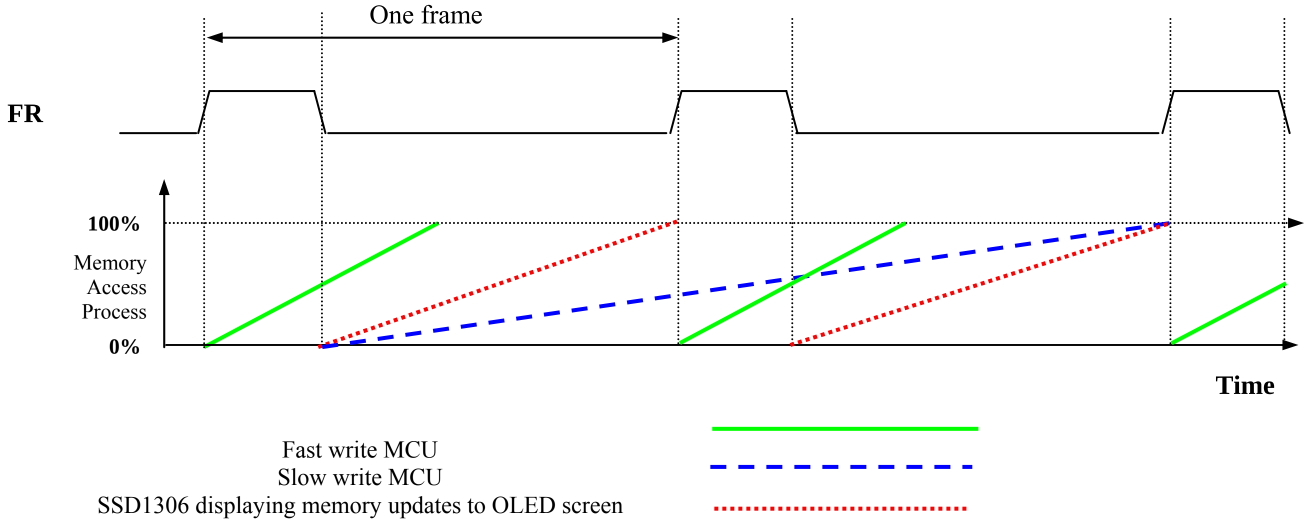
$$F_{FRM} = \frac{F_{osc}}{D \times K \times \text{No. of Mux}}$$

where

- D stands for clock divide ratio. It is set by command D5h A[3:0]. The divide ratio has the range from 1 to 16.
- K is the number of display clocks per row. The value is derived by
  K = Phase 1 period + Phase 2 period + BANK0 pulse width
  = 2 + 2 + 50 = 54 at power on reset
  (Please refer to Section 8.6 "Segment Drivers / Common Drivers" for the details of the "Phase")
- Number of multiplex ratio is set by command A8h. The power on reset value is 63 (i.e. 64MUX).
- F_{OSC} is the oscillator frequency. It can be changed by command D5h A[7:4]. The higher the register setting results in higher frequency.

8.4 FR synchronization

FR synchronization signal can be used to prevent tearing effect.



The starting time to write a new image to OLED driver is depended on the MCU writing speed. If MCU can finish writing a frame image within one frame period, it is classified as fast write MCU. For MCU needs longer writing time to complete (more than one frame but within two frames), it is a slow write one.

For fast write MCU: MCU should start to write new frame of ram data just after rising edge of FR pulse and should be finished well before the rising edge of the next FR pulse.

For slow write MCU: MCU should start to write new frame ram data after the falling edge of the 1st FR pulse and must be finished before the rising edge of the 3rd FR pulse.

8.5 Reset Circuit

When RES# input is LOW, the chip is initialized with the following status:

1. Display is OFF
2. 128 x 64 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

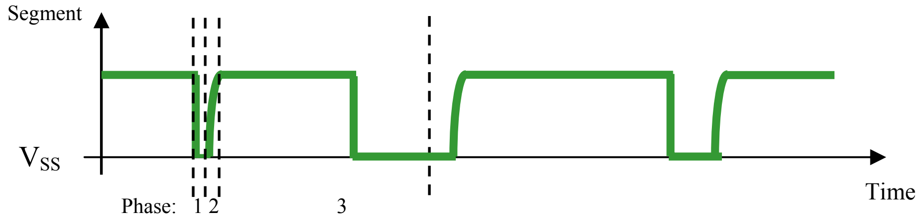
8.6 Segment Drivers / Common Drivers

Segment drivers deliver 128 current sources to drive the OLED panel. The driving current can be adjusted from 0 to 100uA with 256 steps. Common drivers generate voltage-scanning pulses.

The segment driving waveform is divided into three phases:

1. In phase 1, the OLED pixel charges of previous image are discharged in order to prepare for next image content display.
2. In phase 2, the OLED pixel is driven to the targeted voltage. The pixel is driven to attain the corresponding voltage level from V_{SS}. The period of phase 2 can be programmed in length from 1 to 15 DCLKs. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.
3. In phase 3, the OLED driver switches to use current source to drive the OLED pixels and this is the current drive stage.

Figure 8-12 : Segment Output Waveform in three phases



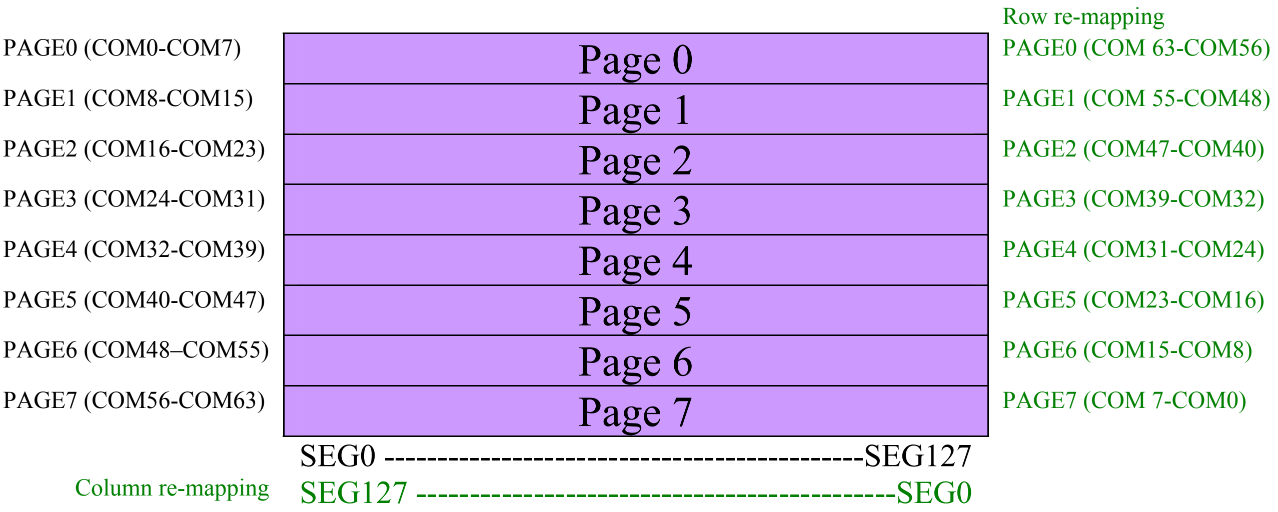
After finishing phase 3, the driver IC will go back to phase 1 to display the next row image data. This three-step cycle is run continuously to refresh image display on OLED panel.

In phase 3, if the length of current drive pulse width is set to 50, after finishing 50 DCLKs in current drive phase, the driver IC will go back to phase 1 for next row display.

8.7 Graphic Display Data RAM (GDDRAM)

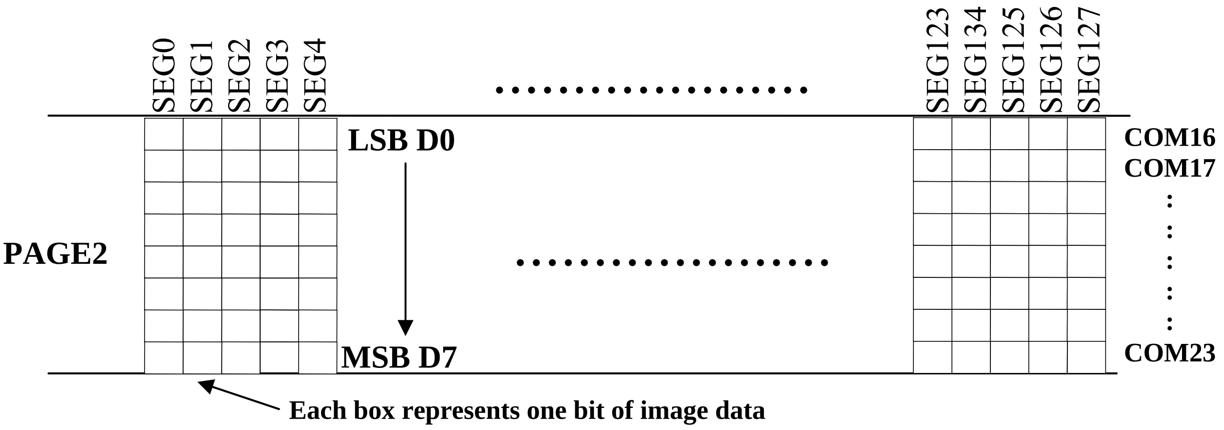
The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 64 bits and the RAM is divided into eight pages, from PAGE0 to PAGE7, which are used for monochrome 128x64 dot matrix display, as shown in Figure 8-13.

Figure 8-13 : GDDRAM pages structure of SSD1306



When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in Figure 8-14.

Figure 8-14 : Enlargement of GDDRAM (No row re-mapping and column-remapping)



For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software as shown in Figure 8-13.

For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

8.8 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current of a color is:

I_{SEG} = Contrast / 256 x I_{REF} x scale factor

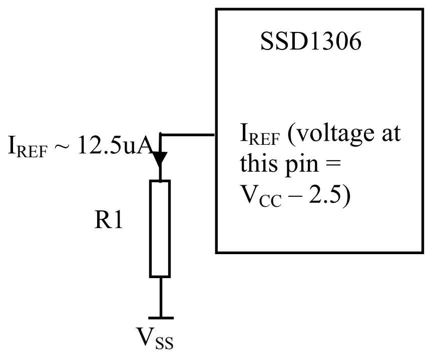
in which

the contrast (0~255) is set by Set Contrast command 81h; and

the scale factor is 8 by default.

The magnitude of I_{REF} is controlled by the value of resistor, which is connected between I_{REF} pin and V_{SS} as shown in Figure 8-15. It is recommended to set I_{REF} to 12.5 ± 2uA so as to achieve I_{SEG} = 100uA at maximum contrast 255.

Figure 8-15 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is V_{CC} – 2.5V, the value of resistor R1 can be found as below:

For I_{REF} = 12.5uA, V_{CC} =12V:

R1 = (Voltage at I_{REF} – V_{SS}) / I_{REF}
= (12 – 2.5) / 12.5uA
= 760KΩ

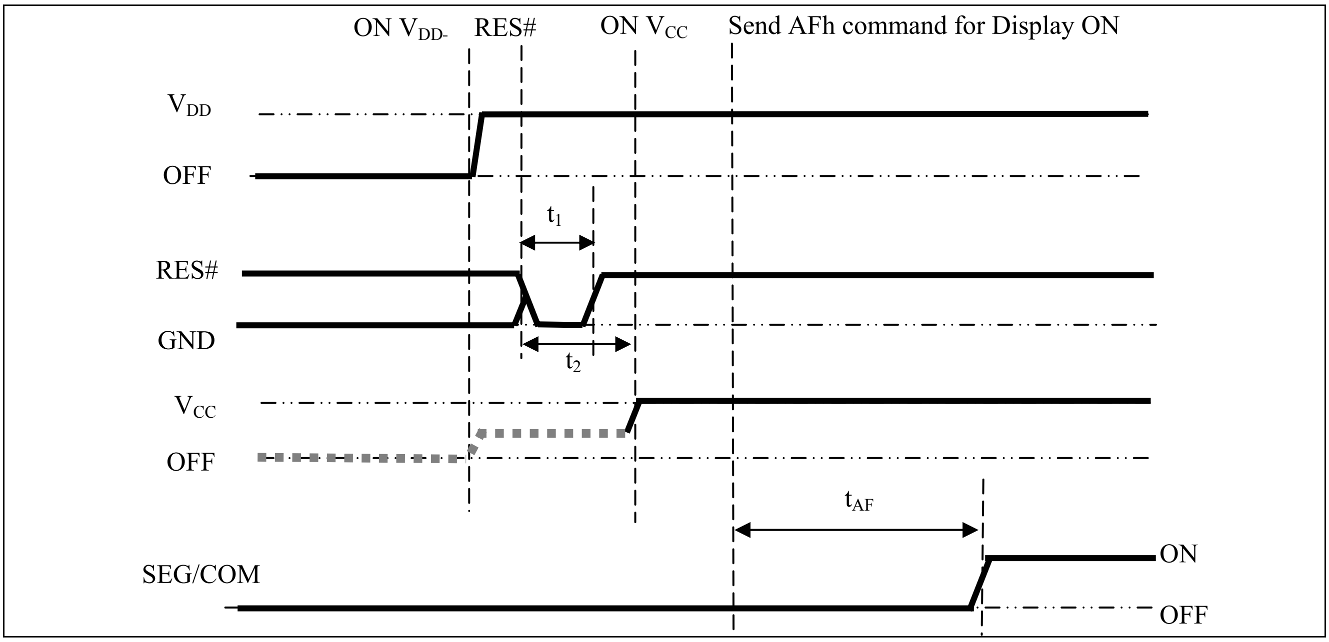
8.9 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1306

Power ON sequence:

1. Power ON V_{DD}
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}. [1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

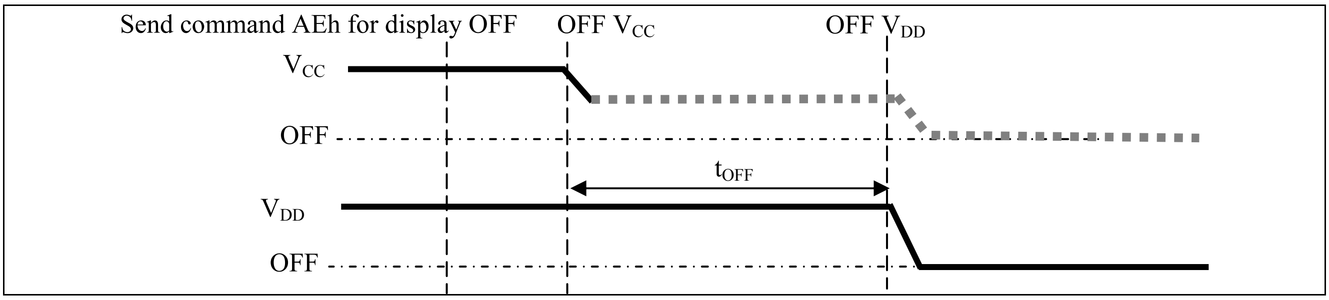
Figure 8-16 : The Power ON sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}. [1], [2], [3]
3. Power OFF V_{DD} after t_{OFF}. [5] (Typical t_{OFF}=100ms)

Figure 8-17 : The Power OFF sequence



Note:

[1] Since an ESD protection circuit is connected between V_{DD} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 8-16 and Figure 8-17.

[2] V_{CC} should be kept float (i.e. disable) when it is OFF.

[3] Power Pins (V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.

[4] The register values are reset after t_1.

[5] V_{DD} should not be Power OFF before V_{CC} Power OFF.

9 COMMAND TABLE

Table 9-1: Command Table

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

1. Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Control	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 7Fh)
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	A4h, X_0=0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X_0=1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0	AE AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF	AEh, X[0]=0b:Display OFF (sleep mode) (RESET) AFh X[0]=1b:Display ON in normal mode

2. Scrolling Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0 0 0 0 0 0	26/27 A[7:0] B[2:0] C[2:0] D[2:0] E[7:0] F[7:0]	0 0 * * * 0 1	0 0 * * * 0 1	1 0 * * * 0 1	0 0 * * * 0 1	0 0 * * * 0 1	1 0 B_2 C_2 D_2 0 1	1 0 B_1 C_1 D_1 0 1	X_0 0 B_0 C_0 D_0 0 1	Continuous Horizontal Scroll Setup	26h, X[0]=0, Right Horizontal Scroll 27h, X[0]=1, Left Horizontal Scroll (Horizontal scroll by 1 column) A[7:0] : Dummy byte (Set as 00h) B[2:0] : Define start page address 000b – PAGE0 / 011b – PAGE3 / 110b – PAGE6 001b – PAGE1 / 100b – PAGE4 / 111b – PAGE7 010b – PAGE2 / 101b – PAGE5 C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 5 frames / 100b – 3 frames 001b – 64 frames / 101b – 4 frames 010b – 128 frames / 110b – 25 frame 011b – 256 frames / 111b – 2 frame D[2:0] : Define end page address 000b – PAGE0 / 011b – PAGE3 / 110b – PAGE6 001b – PAGE1 / 100b – PAGE4 / 111b – PAGE7 010b – PAGE2 / 101b – PAGE5 The value of D[2:0] must be larger or equal to B[2:0] E[7:0] : Dummy byte (Set as 00h) F[7:0] : Dummy byte (Set as FFh)

<table>
<tr><th colspan="12">2. Scrolling Command Table</th></tr>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0
0
0
0
0
0</td><td>29/2A
A[2:0]
B[2:0]
C[2:0]
D[2:0]
E[5:0]</td><td>0
0
*
*
*
*</td><td>0
0
*
*
*
*</td><td>1
0
*
*
*
E_5</td><td>0
0
*
*
*
E_4</td><td>1
0
*
*
*
E_3</td><td>0
0
B_2
C_2
D_2
E_2</td><td>X_1
0
B_1
C_1
D_1
E_1</td><td>X_0
0
B_0
C_0
D_0
E_0</td><td>Continuous Vertical and Horizontal Scroll Setup</td><td>29h, X_1X_0=01b : Vertical and Right Horizontal Scroll
2Ah, X_1X_0=10b : Vertical and Left Horizontal Scroll
(Horizontal scroll by 1 column)
A[7:0] : Dummy byte

B[2:0] : Define start page address
<table>
<tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr>
<tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr>
<tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr>
</table>
C[2:0] : Set time interval between each scroll step in terms of frame frequency
<table>
<tr><td>000b – 5 frames</td><td>100b – 3 frames</td></tr>
<tr><td>001b – 64 frames</td><td>101b – 4 frames</td></tr>
<tr><td>010b – 128 frames</td><td>110b – 25 frame</td></tr>
<tr><td>011b – 256 frames</td><td>111b – 2 frame</td></tr>
</table>
D[2:0] : Define end page address
<table>
<tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr>
<tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr>
<tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr>
</table>
The value of D[2:0] must be larger or equal to B[2:0]

E[5:0] : Vertical scrolling offset
e.g. E[5:0]= 01h refer to offset =1 row
E[5:0] =3Fh refer to offset =63 rows
Note
(1) No continuous vertical scrolling is available.</td></tr>
<tr><td>0</td><td>2E</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>Deactivate scroll</td><td>Stop scrolling that is configured by command 26h/27h/29h/2Ah.

Note
(1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.</td></tr>
<tr><td>0</td><td>2F</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>Activate scroll</td><td>Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences:

Valid command sequence 1: 26h ;2Fh.
Valid command sequence 2: 27h ;2Fh.
Valid command sequence 3: 29h ;2Fh.
Valid command sequence 4: 2Ah ;2Fh.

For example, if “26h; 2Ah; 2Fh.” commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.</td></tr>
</table>

2. Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0 0	A3 A[5:0] B[6:0]	1 * *	0 * B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	1 A_1 B_1	1 A_0 B_0	Set Vertical Scroll Area	A[5:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0).[RESET = 0] B[6:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 64] **Note** (1) A[5:0]+B[6:0] <= MUX ratio (2) B[6:0] <= MUX ratio (3a) Vertical scrolling offset (E[5:0] in 29h/2Ah) < B[6:0] (3b) Set Display Start Line ($X_5X_4X_3X_2X_1X_0$ of 40h~7Fh) < B[6:0] (4) The last row of the scroll area shifts to the first row of the scroll area. (5) For 64d MUX display A[5:0] = 0, B[6:0]=64 : whole area scrolls A[5:0]= 0, B[6:0] < 64 : top area scrolls A[5:0] + B[6:0] < 64 : central area scrolls A[5:0] + B[6:0] = 64 : bottom area scrolls

3. Addressing Setting Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X_3	X_2	X_1	X_0	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. **Note** (1) This command is only for page addressing mode
0	10~1F	0	0	0	1	X_3	X_2	X_1	X_0	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. **Note** (1) This command is only for page addressing mode
0 0	20 A[1:0]	0 *	0 *	1 *	0 *	0 *	0 *	0 A_1	0 A_0	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0 0 0	21 A[6:0] B[6:0]	0 * *	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Setup column start and end address A[6:0] : Column start address, range : 0-127d, (RESET=0d) B[6:0]: Column end address, range : 0-127d, (RESET =127d) **Note** (1) This command is only for horizontal or vertical addressing mode.

3. Addressing Setting Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0 0	22 A[2:0] B[2:0]	0 * *	0 * *	1 * *	0 * *	0 * *	0 A_2 B_2	1 A_1 B_1	0 A_0 B_0	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-7d, (RESET = 0d) B[2:0] : Page end Address, range : 0-7d, (RESET = 7d) **Note** (1) This command is only for horizontal or vertical addressing mode.
0	B0~B7	1	0	1	1	0	X_2	X_1	X_0	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0]. **Note** (1) This command is only for page addressing mode

4. **Hardware Configuration (Panel resolution & layout related) Command Table**											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	40~7F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_3X_2X_1X_0$. Display start line register is reset to 000000b during RESET.
0	A0/A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 127 is mapped to SEG0
0 0	A8 A[5:0]	1 *	0 *	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 64MUX, RESET= 111111b (i.e. 63d, 64MUX) A[5:0] from 0 to 14 are invalid entry.
0	C0/C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N –1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0 0	D3 A[5:0]	1 *	1 *	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Display Offset	Set vertical shift by COM from 0d~63d The value is reset to 00h after RESET.
0 0	DA A[5:4]	1 0	1 0	0 A_5	1 A_4	1 0	0 0	1 1	0 0	Set COM Pins Hardware Configuration	A[4]=0b, Sequential COM pin configuration A[4]=1b(RESET), Alternative COM pin configuration A[5]=0b(RESET), Disable COM Left/Right remap A[5]=1b, Enable COM Left/Right remap

5. Timing & Driving Scheme Setting Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	D5 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1) A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 1000b Range:0000b~1111b Frequency increases as setting value increases.
0 0	D9 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	1 A_3	0 A_2	0 A_1	1 A_0	Set Pre-charge Period	A[3:0] : Phase 1 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h) A[7:4] : Phase 2 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h)
0 0	DB A[6:4]	1 0	1 A_6	0 A_5	1 A_4	1 0	0 0	1 0	1 0	Set V_{COMH} Deselect Level	(see sub-table below)
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation

A[6:4]	Hex code	V_{COMH} deselect level
000b	00h	~ 0.65 x V_{CC}
010b	20h	~ 0.77 x V_{CC} (RESET)
011b	30h	~ 0.83 x V_{CC}

Note

(1) "*" stands for "Don't care".

Table 9-2 : Read Command Table

Bit Pattern	Command	Description
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read	D[7] : Reserved D[6] : “1” for display OFF / “0” for display ON D[5] : Reserved D[4] : Reserved D[3] : Reserved D[2] : Reserved D[1] : Reserved D[0] : Reserved

Note

(1) Patterns other than those given in the Command Table are prohibited to enter the chip as a command; as unexpected results can occur.

9.1 Data Read / Write

To read data from the GDDRAM, select HIGH for both the R/W# (WR#) pin and the D/C# pin for 6800-series parallel mode and select LOW for the E (RD#) pin and HIGH for the D/C# pin for 8080-series parallel mode. No data read is provided in serial mode operation.

In normal data read mode the GDDRAM column address pointer will be increased automatically by one after each data read.

Also, a dummy read is required before the first data read.

To write data to the GDDRAM, select LOW for the R/W# (WR#) pin and HIGH for the D/C# pin for both 6800-series parallel mode and 8080-series parallel mode. The serial interface mode is always in write mode. The GDDRAM column address pointer will be increased automatically by one after each data write.

Table 9-3 : Address increment table (Automatic)

D/C#	R/W# (WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

10 COMMAND DESCRIPTIONS

10.1 Fundamental Command

10.1.1 Set Lower Column Start Address for Page Addressing Mode (00h~0Fh)

This command specifies the lower nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Please refer to Section Table 9-1 and Section 10.1.3 for details.

10.1.2 Set Higher Column Start Address for Page Addressing Mode (10h~1Fh)

This command specifies the higher nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Please refer to Section Table 9-1 and Section 10.1.3 for details.

10.1.3 Set Memory Addressing Mode (20h)

There are 3 different memory addressing mode in SSD1306: page addressing mode, horizontal addressing mode and vertical addressing mode. This command sets the way of memory addressing into one of the above three modes. In there, “COL” means the graphic display data RAM column.

<u>Page addressing mode (A[1:0]=10xb)</u>

In page addressing mode, after the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and page address pointer is not changed. Users have to set the new page and column addresses in order to access the next page RAM content. The sequence of movement of the PAGE and column address point for page addressing mode is shown in Figure 10-1.

Figure 10-1 : Address Pointer Movement of Page addressing mode

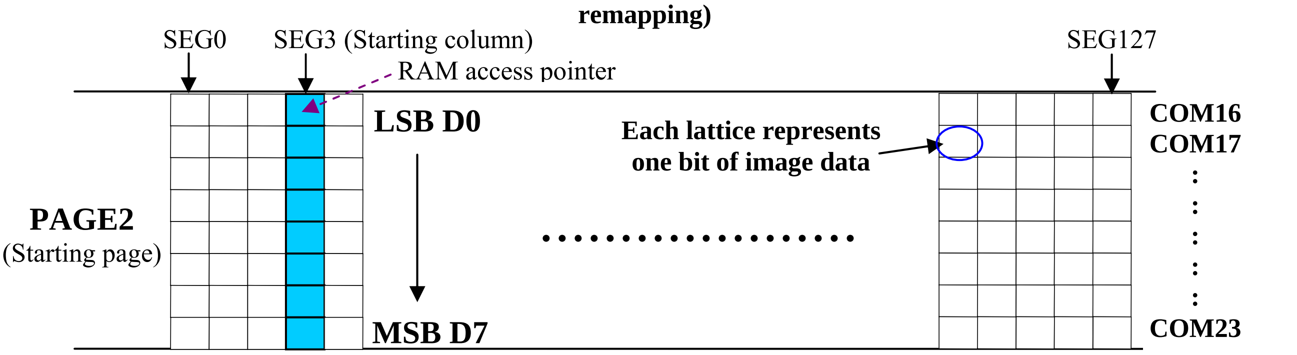
	COL0	COL 1	…..	COL 126	COL 127
PAGE0					
PAGE1					
:	:	:	:	:	:
PAGE6					
PAGE7					

In normal display data RAM read or write and page addressing mode, the following steps are required to define the starting RAM access pointer location:

- Set the page start address of the target display location by command B0h to B7h.
- Set the lower start column address of pointer by command 00h~0Fh.
- Set the upper start column address of pointer by command 10h~1Fh.

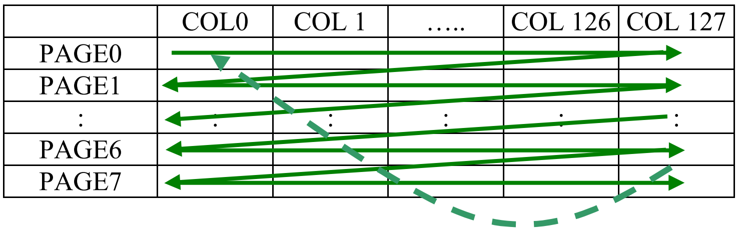
For example, if the page address is set to B2h, lower column address is 03h and upper column address is 10h, then that means the starting column is SEG3 of PAGE2. The RAM access pointer is located as shown in Figure 10-2. The input data byte will be written into RAM position of column 3.

Figure 10-2 : Example of GDDRAM access pointer setting in Page Addressing Mode (No row and column-remapping)



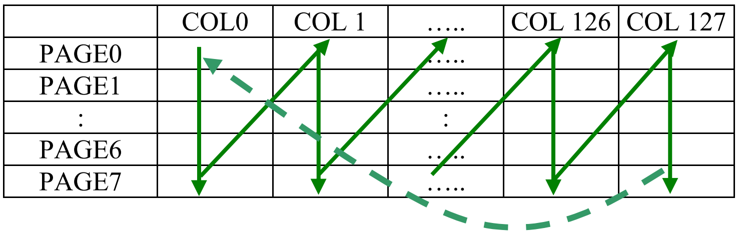
Horizontal addressing mode (A[1:0]=00b)
In horizontal addressing mode, after the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and page address pointer is increased by 1. The sequence of movement of the page and column address point for horizontal addressing mode is shown in Figure 10-3. When both column and page address pointers reach the end address, the pointers are reset to column start address and page start address (Dotted line in Figure 10-3.)

Figure 10-3 : Address Pointer Movement of Horizontal addressing mode



Vertical addressing mode: (A[1:0]=01b)
In vertical addressing mode, after the display RAM is read/written, the page address pointer is increased automatically by 1. If the page address pointer reaches the page end address, the page address pointer is reset to page start address and column address pointer is increased by 1. The sequence of movement of the page and column address point for vertical addressing mode is shown in Figure 10-4. When both column and page address pointers reach the end address, the pointers are reset to column start address and page start address (Dotted line in Figure 10-4.)

Figure 10-4 : Address Pointer Movement of Vertical addressing mode



In normal display data RAM read or write and horizontal / vertical addressing mode, the following steps are required to define the RAM access pointer location:

- Set the column start and end address of the target display location by command 21h.
- Set the page start and end address of the target display location by command 22h.

Example is shown in Figure 10-5.

10.1.4 Set Column Address (21h)

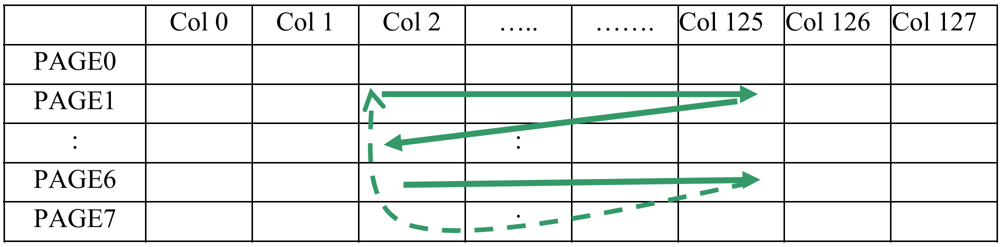
This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command 20h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

10.1.5 Set Page Address (22h)

This triple byte command specifies page start address and end address of the display data RAM. This command also sets the page address pointer to page start address. This pointer is used to define the current read/write page address in graphic display data RAM. If vertical address increment mode is enabled by command 20h, after finishing read/write one page data, it is incremented automatically to the next page address. Whenever the page address pointer finishes accessing the end page address, it is reset back to start page address.

The figure below shows the way of column and page address pointer movement through the example: column start address is set to 2 and column end address is set to 125, page start address is set to 1 and page end address is set to 6; Horizontal address increment mode is enabled by command 20h. In this case, the graphic display data RAM column accessible range is from column 2 to column 125 and from page 1 to page 6 only. In addition, the column address pointer is set to 2 and page address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation (*solid line in Figure 10-5*). Whenever the column address pointer finishes accessing the end column 125, it is reset back to column 2 and page address is automatically increased by 1 (*solid line in Figure 10-5*). While the end page 6 and end column 125 RAM location is accessed, the page address is reset back to 1 and the column address is reset back to 2 (*dotted line in Figure 10-5*). .

Figure 10-5 : Example of Column and Row Address Pointer Movement



10.1.6 Set Display Start Line (40h~7Fh)

This command sets the Display Start Line register to determine starting address of display RAM, by selecting a value from 0 to 63. With value equal to 0, RAM row 0 is mapped to COM0. With value equal to 1, RAM row 1 is mapped to COM0 and so on.

Refer to Table 10-1 for more illustrations.

10.1.7 Set Contrast Control for BANK0 (81h)

This command sets the Contrast Setting of the display. The chip has 256 contrast steps from 00h to FFh. The segment output current increases as the contrast step value increases.

10.1.8 Set Segment Re-map (A0h/A1h)

This command changes the mapping between the display data column address and the segment driver. It allows flexibility in OLED module design. Please refer to Table 9-1.

This command only affects subsequent data input. Data already stored in GDDRAM will have no changes.

10.1.9 Entire Display ON (A4h/A5h)

A4h command enable display outputs according to the GDDRAM contents.
If A5h command is issued, then by using A4h command, the display will resume to the GDDRAM contents.
In other words, A4h command resumes the display from entire display “ON” stage.
A5h command forces the entire display to be “ON”, regardless of the contents of the display data RAM.

10.1.10 Set Normal/Inverse Display (A6h/A7h)

This command sets the display to be either normal or inverse. In normal display a RAM data of 1 indicates an “ON” pixel while in inverse display a RAM data of 0 indicates an “ON” pixel.

10.1.11 Set Multiplex Ratio (A8h)

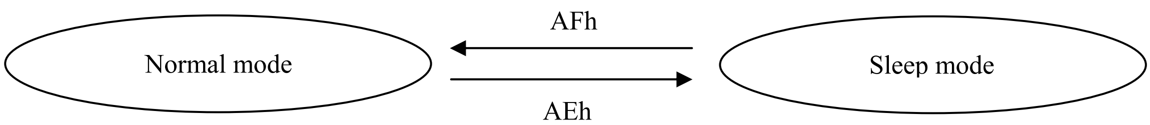
This command switches the default 63 multiplex mode to any multiplex ratio, ranging from 16 to 63. The output pads COM0~COM63 will be switched to the corresponding COM signal.

10.1.12 Set Display ON/OFF (AEh/AFh)

These single byte commands are used to turn the OLED panel display ON or OFF.
When the display is ON, the selected circuits by Set Master Configuration command will be turned ON.
When the display is OFF, those circuits will be turned OFF and the segment and common output are in V_{SS} state and high impedance state, respectively. These commands set the display to one of the two states:

- AEh : Display OFF
- AFh : Display ON

Figure 10-6 :Transition between different modes



10.1.13 Set Page Start Address for Page Addressing Mode (B0h~B7h)

This command positions the page start address from 0 to 7 in GDDRAM under Page Addressing Mode. Please refer to Table 9-1 and Section 10.1.3 for details.

10.1.14 Set COM Output Scan Direction (C0h/C8h)

This command sets the scan direction of the COM output, allowing layout flexibility in the OLED module design. Additionally, the display will show once this command is issued. For example, if this command is sent during normal display then the graphic display will be vertically flipped immediately. Please refer to Table 10-3 for details.

10.1.15 Set Display Offset (D3h)

This is a double byte command. The second command specifies the mapping of the display start line to one of COM0~COM63 (assuming that COM0 is the display start line then the display start line register is equal to 0).

For example, to move the COM16 towards the COM0 direction by 16 lines the 6-bit data in the second byte should be given as 010000b. To move in the opposite direction by 16 lines the 6-bit data should be given by 64 – 16, so the second byte would be 100000b. The following two tables (Table 10-1, Table 10-2) show the example of setting the command C0h/C8h and D3h.

Table 10-1 : Example of Set Display Offset and Display Start Line with no Remap

Hardware pin name	Output												
	64		64		64		56		56		56		Set MUX ratio(A8h)
	Normal		Normal		Normal		Normal		Normal		Normal		COM Normal / Remapped (C0h / C8h)
	0		8		0		0		8		0		Display offset (D3h)
	0		0		8		0		0		8		Display start line (40h - 7Fh)
COM0	Row0	RAM0	Row8	RAM8	Row0	RAM8	Row0	RAM0	Row8	RAM8	Row0	RAM8	
COM1	Row1	RAM1	Row9	RAM9	Row1	RAM9	Row1	RAM1	Row9	RAM9	Row1	RAM9	
COM2	Row2	RAM2	Row10	RAM10	Row2	RAM10	Row2	RAM2	Row10	RAM10	Row2	RAM10	
COM3	Row3	RAM3	Row11	RAM11	Row3	RAM11	Row3	RAM3	Row11	RAM11	Row3	RAM11	
COM4	Row4	RAM4	Row12	RAM12	Row4	RAM12	Row4	RAM4	Row12	RAM12	Row4	RAM12	
COM5	Row5	RAM5	Row13	RAM13	Row5	RAM13	Row5	RAM5	Row13	RAM13	Row5	RAM13	
COM6	Row6	RAM6	Row14	RAM14	Row6	RAM14	Row6	RAM6	Row14	RAM14	Row6	RAM14	
COM7	Row7	RAM7	Row15	RAM15	Row7	RAM15	Row7	RAM7	Row15	RAM15	Row7	RAM15	
COM8	Row8	RAM8	Row16	RAM16	Row8	RAM16	Row8	RAM8	Row16	RAM16	Row8	RAM16	
COM9	Row9	RAM9	Row17	RAM17	Row9	RAM17	Row9	RAM9	Row17	RAM17	Row9	RAM17	
COM10	Row10	RAM10	Row18	RAM18	Row10	RAM18	Row10	RAM10	Row18	RAM18	Row10	RAM18	
COM11	Row11	RAM11	Row19	RAM19	Row11	RAM19	Row11	RAM11	Row19	RAM19	Row11	RAM19	
COM12	Row12	RAM12	Row20	RAM20	Row12	RAM20	Row12	RAM12	Row20	RAM20	Row12	RAM20	
COM13	Row13	RAM13	Row21	RAM21	Row13	RAM21	Row13	RAM13	Row21	RAM21	Row13	RAM21	
COM14	Row14	RAM14	Row22	RAM22	Row14	RAM22	Row14	RAM14	Row22	RAM22	Row14	RAM22	
COM15	Row15	RAM15	Row23	RAM23	Row15	RAM23	Row15	RAM15	Row23	RAM23	Row15	RAM23	
COM16	Row16	RAM16	Row24	RAM24	Row16	RAM24	Row16	RAM16	Row24	RAM24	Row16	RAM24	
COM17	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row17	RAM17	Row25	RAM25	Row17	RAM25	
COM18	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row18	RAM18	Row26	RAM26	Row18	RAM26	
COM19	Row19	RAM19	Row27	RAM27	Row19	RAM27	Row19	RAM19	Row27	RAM27	Row19	RAM27	
COM20	Row20	RAM20	Row28	RAM28	Row20	RAM28	Row20	RAM20	Row28	RAM28	Row20	RAM28	
COM21	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row21	RAM21	Row29	RAM29	Row21	RAM29	
COM22	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row22	RAM22	Row30	RAM30	Row22	RAM30	
COM23	Row23	RAM23	Row31	RAM31	Row23	RAM31	Row23	RAM23	Row31	RAM31	Row23	RAM31	
COM24	Row24	RAM24	Row32	RAM32	Row24	RAM32	Row24	RAM24	Row32	RAM32	Row24	RAM32	
COM25	Row25	RAM25	Row33	RAM33	Row25	RAM33	Row25	RAM25	Row33	RAM33	Row25	RAM33	
COM26	Row26	RAM26	Row34	RAM34	Row26	RAM34	Row26	RAM26	Row34	RAM34	Row26	RAM34	
COM27	Row27	RAM27	Row35	RAM35	Row27	RAM35	Row27	RAM27	Row35	RAM35	Row27	RAM35	
COM28	Row28	RAM28	Row36	RAM36	Row28	RAM36	Row28	RAM28	Row36	RAM36	Row28	RAM36	
COM29	Row29	RAM29	Row37	RAM37	Row29	RAM37	Row29	RAM29	Row37	RAM37	Row29	RAM37	
COM30	Row30	RAM30	Row38	RAM38	Row30	RAM38	Row30	RAM30	Row38	RAM38	Row30	RAM38	
COM31	Row31	RAM31	Row39	RAM39	Row31	RAM39	Row31	RAM31	Row39	RAM39	Row31	RAM39	
COM32	Row32	RAM32	Row40	RAM40	Row32	RAM40	Row32	RAM32	Row40	RAM40	Row32	RAM40	
COM33	Row33	RAM33	Row41	RAM41	Row33	RAM41	Row33	RAM33	Row41	RAM41	Row33	RAM41	
COM34	Row34	RAM34	Row42	RAM42	Row34	RAM42	Row34	RAM34	Row42	RAM42	Row34	RAM42	
COM35	Row35	RAM35	Row43	RAM43	Row35	RAM43	Row35	RAM35	Row43	RAM43	Row35	RAM43	
COM36	Row36	RAM36	Row44	RAM44	Row36	RAM44	Row36	RAM36	Row44	RAM44	Row36	RAM44	
COM37	Row37	RAM37	Row45	RAM45	Row37	RAM45	Row37	RAM37	Row45	RAM45	Row37	RAM45	
COM38	Row38	RAM38	Row46	RAM46	Row38	RAM46	Row38	RAM38	Row46	RAM46	Row38	RAM46	
COM39	Row39	RAM39	Row47	RAM47	Row39	RAM47	Row39	RAM39	Row47	RAM47	Row39	RAM47	
COM40	Row40	RAM40	Row48	RAM48	Row40	RAM48	Row40	RAM40	Row48	RAM48	Row40	RAM48	
COM41	Row41	RAM41	Row49	RAM49	Row41	RAM49	Row41	RAM41	Row49	RAM49	Row41	RAM49	
COM42	Row42	RAM42	Row50	RAM50	Row42	RAM50	Row42	RAM42	Row50	RAM50	Row42	RAM50	
COM43	Row43	RAM43	Row51	RAM51	Row43	RAM51	Row43	RAM43	Row51	RAM51	Row43	RAM51	
COM44	Row44	RAM44	Row52	RAM52	Row44	RAM52	Row44	RAM44	Row52	RAM52	Row44	RAM52	
COM45	Row45	RAM45	Row53	RAM53	Row45	RAM53	Row45	RAM45	Row53	RAM53	Row45	RAM53	
COM46	Row46	RAM46	Row54	RAM54	Row46	RAM54	Row46	RAM46	Row54	RAM54	Row46	RAM54	
COM47	Row47	RAM47	Row55	RAM55	Row47	RAM55	Row47	RAM47	Row55	RAM55	Row47	RAM55	
COM48	Row48	RAM48	Row56	RAM56	Row48	RAM56	Row48	RAM48	-	-	Row48	RAM56	
COM49	Row49	RAM49	Row57	RAM57	Row49	RAM57	Row49	RAM49	-	-	Row49	RAM57	
COM50	Row50	RAM50	Row58	RAM58	Row50	RAM58	Row50	RAM50	-	-	Row50	RAM58	
COM51	Row51	RAM51	Row59	RAM59	Row51	RAM59	Row51	RAM51	-	-	Row51	RAM59	
COM52	Row52	RAM52	Row60	RAM60	Row52	RAM60	Row52	RAM52	-	-	Row52	RAM60	
COM53	Row53	RAM53	Row61	RAM61	Row53	RAM61	Row53	RAM53	-	-	Row53	RAM61	
COM54	Row54	RAM54	Row62	RAM62	Row54	RAM62	Row54	RAM54	-	-	Row54	RAM62	
COM55	Row55	RAM55	Row63	RAM63	Row55	RAM63	Row55	RAM55	-	-	Row55	RAM63	
COM56	Row56	RAM56	Row0	RAM0	Row56	RAM0	-	-	Row0	RAM0	-	-	
COM57	Row57	RAM57	Row1	RAM1	Row57	RAM1	-	-	Row1	RAM1	-	-	
COM58	Row58	RAM58	Row2	RAM2	Row58	RAM2	-	-	Row2	RAM2	-	-	
COM59	Row59	RAM59	Row3	RAM3	Row59	RAM3	-	-	Row3	RAM3	-	-	
COM60	Row60	RAM60	Row4	RAM4	Row60	RAM4	-	-	Row4	RAM4	-	-	
COM61	Row61	RAM61	Row5	RAM5	Row61	RAM5	-	-	Row5	RAM5	-	-	
COM62	Row62	RAM62	Row6	RAM6	Row62	RAM6	-	-	Row6	RAM6	-	-	
COM63	Row63	RAM63	Row7	RAM7	Row63	RAM7	-	-	Row7	RAM7	-	-	
Display examples	(a)		(b)		(c)		(d)		(e)		(f)		

(a)

(b)

(c)

(d)

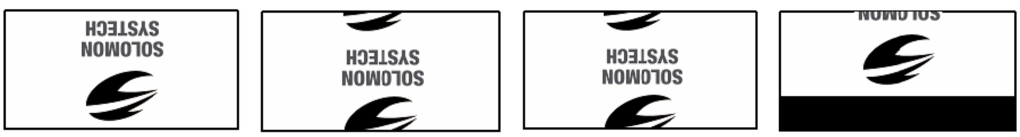
(e)

(f)

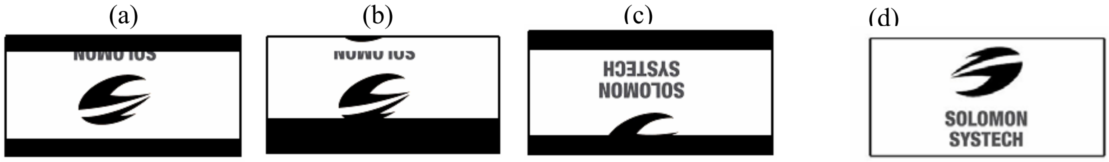
(RAM)

Table 10-2 :Example of Set Display Offset and Display Start Line with Remap

Hardware pin name	Output														
	64		64		64		48		48		48		48		Set MUX ratio(A8h)
	Remap		Remap		Remap		Remap		Remap		Remap		Remap		COM Normal / Remapped (C0h / C8h)
	0		8		0		0		8		0		8		Display offset (D3h)
	0		0		8		0		0		8		16		Display start line (40h - 7Fh)
COM0	Row63	RAM63	Row7	RAM7	Row63	RAM7	Row47	RAM47	-	-	Row47	RAM55	-	-	
COM1	Row62	RAM62	Row6	RAM6	Row62	RAM6	Row46	RAM46	-	-	Row46	RAM54	-	-	
COM2	Row61	RAM61	Row5	RAM5	Row61	RAM5	Row45	RAM45	-	-	Row45	RAM53	-	-	
COM3	Row60	RAM60	Row4	RAM4	Row60	RAM4	Row44	RAM44	-	-	Row44	RAM52	-	-	
COM4	Row59	RAM59	Row3	RAM3	Row59	RAM3	Row43	RAM43	-	-	Row43	RAM51	-	-	
COM5	Row58	RAM58	Row2	RAM2	Row58	RAM2	Row42	RAM42	-	-	Row42	RAM50	-	-	
COM6	Row57	RAM57	Row1	RAM1	Row57	RAM1	Row41	RAM41	-	-	Row41	RAM49	-	-	
COM7	Row56	RAM56	Row0	RAM0	Row56	RAM0	Row40	RAM40	-	-	Row40	RAM48	-	-	
COM8	Row55	RAM55	Row63	RAM63	Row55	RAM63	Row39	RAM39	Row47	RAM47	Row39	RAM47	Row47	RAM63	
COM9	Row54	RAM54	Row62	RAM62	Row54	RAM62	Row38	RAM38	Row46	RAM46	Row38	RAM46	Row46	RAM62	
COM10	Row53	RAM53	Row61	RAM61	Row53	RAM61	Row37	RAM37	Row45	RAM45	Row37	RAM45	Row45	RAM61	
COM11	Row52	RAM52	Row60	RAM60	Row52	RAM60	Row36	RAM36	Row44	RAM44	Row36	RAM44	Row44	RAM60	
COM12	Row51	RAM51	Row59	RAM59	Row51	RAM59	Row35	RAM35	Row43	RAM43	Row35	RAM43	Row43	RAM59	
COM13	Row50	RAM50	Row58	RAM58	Row50	RAM58	Row34	RAM34	Row42	RAM42	Row34	RAM42	Row42	RAM58	
COM14	Row49	RAM49	Row57	RAM57	Row49	RAM57	Row33	RAM33	Row41	RAM41	Row33	RAM41	Row41	RAM57	
COM15	Row48	RAM48	Row56	RAM56	Row48	RAM56	Row32	RAM32	Row40	RAM40	Row32	RAM40	Row40	RAM56	
COM16	Row47	RAM47	Row55	RAM55	Row47	RAM55	Row31	RAM31	Row39	RAM39	Row31	RAM39	Row39	RAM55	
COM17	Row46	RAM46	Row54	RAM54	Row46	RAM54	Row30	RAM30	Row38	RAM38	Row30	RAM38	Row38	RAM54	
COM18	Row45	RAM45	Row53	RAM53	Row45	RAM53	Row29	RAM29	Row37	RAM37	Row29	RAM37	Row37	RAM53	
COM19	Row44	RAM44	Row52	RAM52	Row44	RAM52	Row28	RAM28	Row36	RAM36	Row28	RAM36	Row36	RAM52	
COM20	Row43	RAM43	Row51	RAM51	Row43	RAM51	Row27	RAM27	Row35	RAM35	Row27	RAM35	Row35	RAM51	
COM21	Row42	RAM42	Row50	RAM50	Row42	RAM50	Row26	RAM26	Row34	RAM34	Row26	RAM34	Row34	RAM50	
COM22	Row41	RAM41	Row49	RAM49	Row41	RAM49	Row25	RAM25	Row33	RAM33	Row25	RAM33	Row33	RAM49	
COM23	Row40	RAM40	Row48	RAM48	Row40	RAM48	Row24	RAM24	Row32	RAM32	Row24	RAM32	Row32	RAM48	
COM24	Row39	RAM39	Row47	RAM47	Row39	RAM47	Row23	RAM23	Row31	RAM31	Row23	RAM31	Row31	RAM47	
COM25	Row38	RAM38	Row46	RAM46	Row38	RAM46	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row30	RAM46	
COM26	Row37	RAM37	Row45	RAM45	Row37	RAM45	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row29	RAM45	
COM27	Row36	RAM36	Row44	RAM44	Row36	RAM44	Row20	RAM20	Row28	RAM28	Row20	RAM28	Row28	RAM44	
COM28	Row35	RAM35	Row43	RAM43	Row35	RAM43	Row19	RAM19	Row27	RAM27	Row19	RAM27	Row27	RAM43	
COM29	Row34	RAM34	Row42	RAM42	Row34	RAM42	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row26	RAM42	
COM30	Row33	RAM33	Row41	RAM41	Row33	RAM41	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row25	RAM41	
COM31	Row32	RAM32	Row40	RAM40	Row32	RAM40	Row16	RAM16	Row24	RAM24	Row16	RAM24	Row24	RAM40	
COM32	Row31	RAM31	Row39	RAM39	Row31	RAM39	Row15	RAM15	Row23	RAM23	Row15	RAM23	Row23	RAM39	
COM33	Row30	RAM30	Row38	RAM38	Row30	RAM38	Row14	RAM14	Row22	RAM22	Row14	RAM22	Row22	RAM38	
COM34	Row29	RAM29	Row37	RAM37	Row29	RAM37	Row13	RAM13	Row21	RAM21	Row13	RAM21	Row21	RAM37	
COM35	Row28	RAM28	Row36	RAM36	Row28	RAM36	Row12	RAM12	Row20	RAM20	Row12	RAM20	Row20	RAM36	
COM36	Row27	RAM27	Row35	RAM35	Row27	RAM35	Row11	RAM11	Row19	RAM19	Row11	RAM19	Row19	RAM35	
COM37	Row26	RAM26	Row34	RAM34	Row26	RAM34	Row10	RAM10	Row18	RAM18	Row10	RAM18	Row18	RAM34	
COM38	Row25	RAM25	Row33	RAM33	Row25	RAM33	Row9	RAM9	Row17	RAM17	Row9	RAM17	Row17	RAM33	
COM39	Row24	RAM24	Row32	RAM32	Row24	RAM32	Row8	RAM8	Row16	RAM16	Row8	RAM16	Row16	RAM32	
COM40	Row23	RAM23	Row31	RAM31	Row23	RAM31	Row7	RAM7	Row15	RAM15	Row7	RAM15	Row15	RAM31	
COM41	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row6	RAM6	Row14	RAM14	Row6	RAM14	Row14	RAM30	
COM42	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row5	RAM5	Row13	RAM13	Row5	RAM13	Row13	RAM29	
COM43	Row20	RAM20	Row28	RAM28	Row20	RAM28	Row4	RAM4	Row12	RAM12	Row4	RAM12	Row12	RAM28	
COM44	Row19	RAM19	Row27	RAM27	Row19	RAM27	Row3	RAM3	Row11	RAM11	Row3	RAM11	Row11	RAM27	
COM45	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row2	RAM2	Row10	RAM10	Row2	RAM10	Row10	RAM26	
COM46	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row1	RAM1	Row9	RAM9	Row1	RAM9	Row9	RAM25	
COM47	Row16	RAM16	Row24	RAM24	Row16	RAM24	Row0	RAM0	Row8	RAM8	Row0	RAM8	Row8	RAM24	
COM48	Row15	RAM15	Row23	RAM23	Row15	RAM23	-	-	Row7	RAM7	-	-	Row7	RAM23	
COM49	Row14	RAM14	Row22	RAM22	Row14	RAM22	-	-	Row6	RAM6	-	-	Row6	RAM22	
COM50	Row13	RAM13	Row21	RAM21	Row13	RAM21	-	-	Row5	RAM5	-	-	Row5	RAM21	
COM51	Row12	RAM12	Row20	RAM20	Row12	RAM20	-	-	Row4	RAM4	-	-	Row4	RAM20	
COM52	Row11	RAM11	Row19	RAM19	Row11	RAM19	-	-	Row3	RAM3	-	-	Row3	RAM19	
COM53	Row10	RAM10	Row18	RAM18	Row10	RAM18	-	-	Row2	RAM2	-	-	Row2	RAM18	
COM54	Row9	RAM9	Row17	RAM17	Row9	RAM17	-	-	Row1	RAM1	-	-	Row1	RAM17	
COM55	Row8	RAM8	Row16	RAM16	Row8	RAM16	-	-	Row0	RAM0	-	-	Row0	RAM16	
COM56	Row7	RAM7	Row15	RAM15	Row7	RAM15	-	-	-	-	-	-	-	-	
COM57	Row6	RAM6	Row14	RAM14	Row6	RAM14	-	-	-	-	-	-	-	-	
COM58	Row5	RAM5	Row13	RAM13	Row5	RAM13	-	-	-	-	-	-	-	-	
COM59	Row4	RAM4	Row12	RAM12	Row4	RAM12	-	-	-	-	-	-	-	-	
COM60	Row3	RAM3	Row11	RAM11	Row3	RAM11	-	-	-	-	-	-	-	-	
COM61	Row2	RAM2	Row10	RAM10	Row2	RAM10	-	-	-	-	-	-	-	-	
COM62	Row1	RAM1	Row9	RAM9	Row1	RAM9	-	-	-	-	-	-	-	-	
COM63	Row0	RAM0	Row8	RAM8	Row0	RAM8	-	-	-	-	-	-	-	-	
Display examples	(a)		(b)		(c)		(d)		(e)		(f)		(g)		



(a) (b) (c) (d)



(e) (f) (g) (RAM)

10.1.16 Set Display Clock Divide Ratio/ Oscillator Frequency (D5h)

This command consists of two functions:

- Display Clock Divide Ratio (D)(A[3:0])
  Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with reset value = 1. Please refer to section 8.3 for the details relationship of DCLK and CLK.

- Oscillator Frequency (A[7:4])
  Program the oscillator frequency Fosc that is the source of CLK if CLS pin is pulled high. The 4-bit value results in 16 different frequency settings available as shown below. The default setting is 1000b.

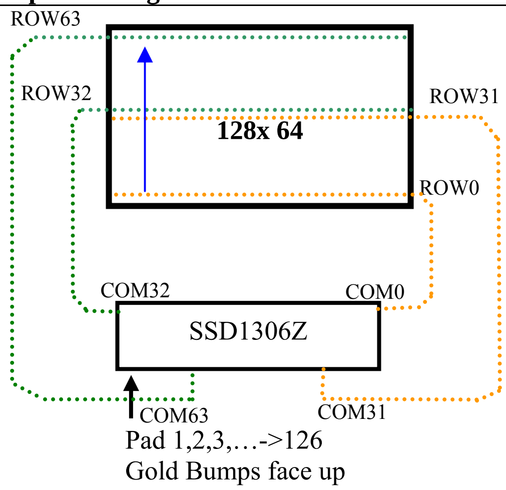
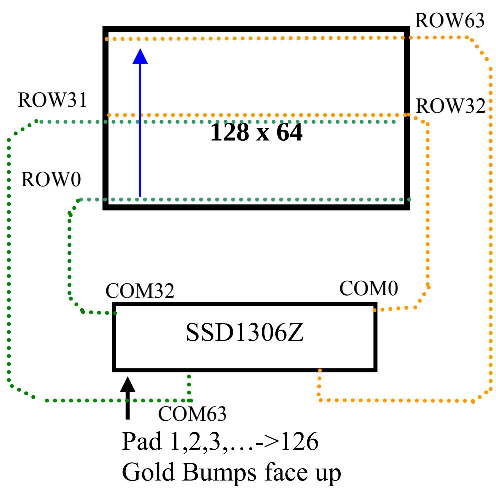
10.1.17 Set Pre-charge Period (D9h)

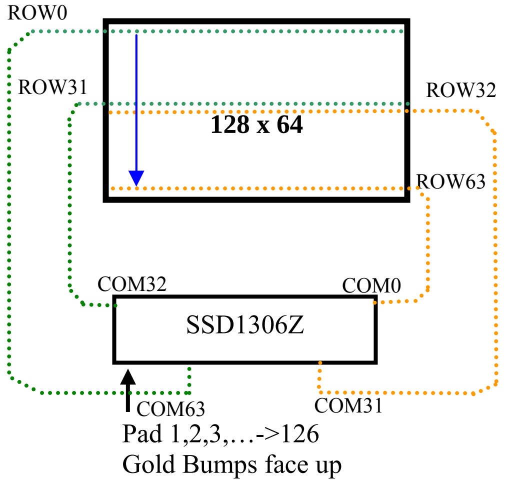
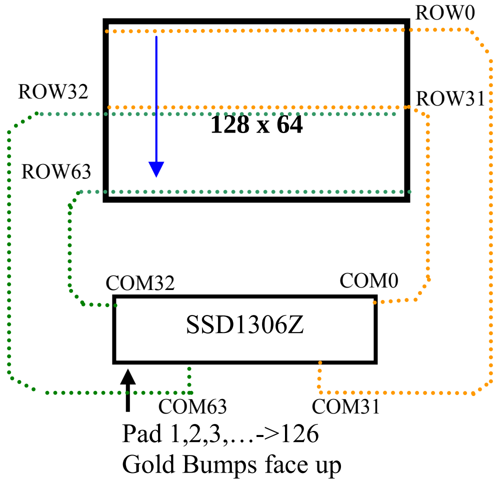
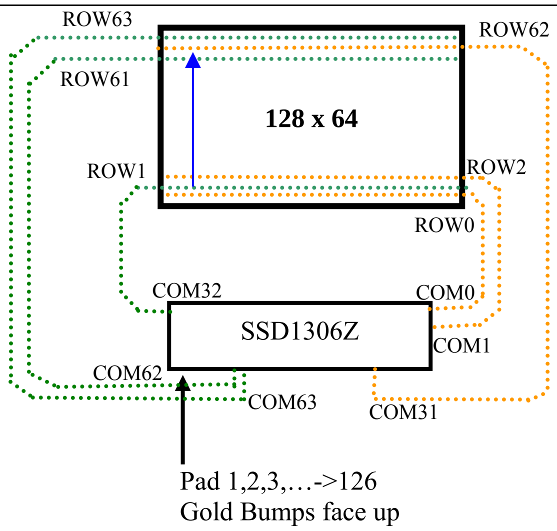
This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK, where RESET equals 2 DCLKs.

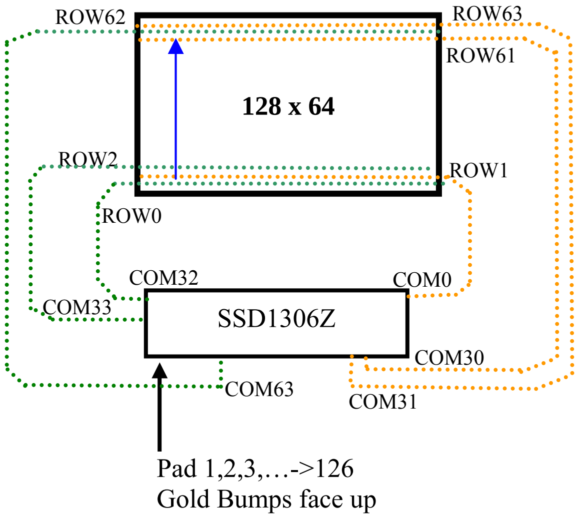
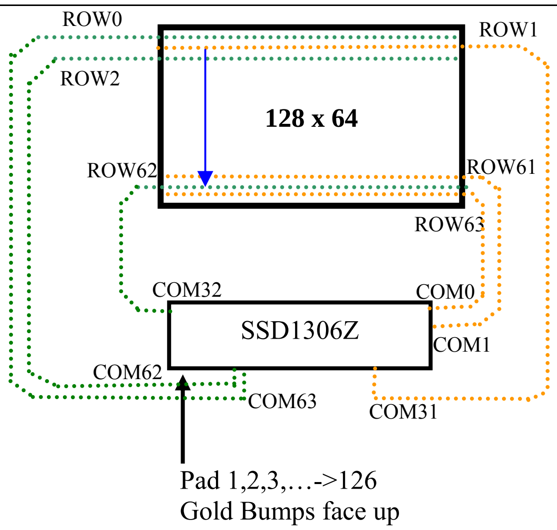
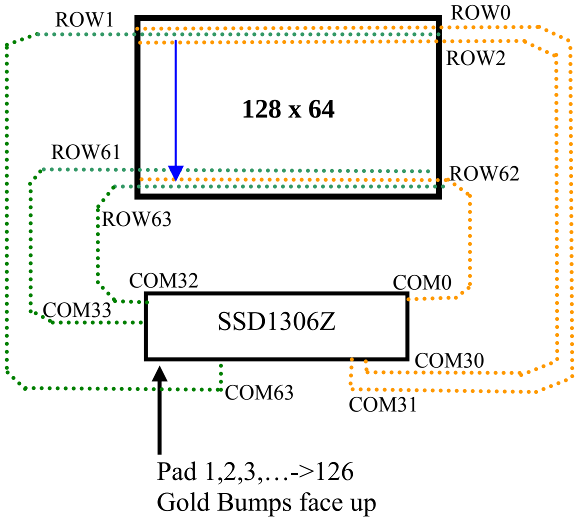
10.1.18 Set COM Pins Hardware Configuration (DAh)

This command sets the COM signals pin configuration to match the OLED panel hardware layout. The table below shows the COM pin configuration under different conditions (for MUX ratio =64):

Table 10-3 : COM Pins Hardware Configuration

Conditions	COM pins Configurations
1 Sequential COM pin configuration (DAh A[4] =0) COM output Scan direction: from COM0 to COM63 (C0h) Disable COM Left/Right remap (DAh A[5] =0)	
2 Sequential COM pin configuration (DAh A[4] =0) COM output Scan direction: from COM0 to COM63 (C0h) Enable COM Left/Right remap (DAh A[5] =1)	

<table>
<tr><th>Conditions</th><th>COM pins Configurations</th></tr>
<tr><td>3 Sequential COM pin configuration (DAh A[4] =0)
COM output Scan direction: from COM63 to COM0 (C8h)
Disable COM Left/Right remap (DAh A[5] =0)</td><td>
</td></tr>
<tr><td>4 Sequential COM pin configuration (DAh A[4] =0)
COM output Scan direction: from COM63 to COM0 (C8h)
Enable COM Left/Right remap (DAh A[5] =1)</td><td>
</td></tr>
<tr><td>5 Alternative COM pin configuration (DAh A[4] =1)
COM output Scan direction: from COM0 to COM63 (C0h)
Disable COM Left/Right remap (DAh A[5] =0)</td><td>
</td></tr>
</table>

<table>
<tr><th>Conditions</th><th>COM pins Configurations</th></tr>
<tr><td>6 Alternative COM pin configuration (DAh A[4] =1)
COM output Scan direction: from COM0 to COM63 (C0h)
Enable COM Left/Right remap (DAh A[5] =1)</td><td>
</td></tr>
<tr><td>7 Alternative COM pin configuration (DAh A[4] =1)
COM output Scan direction: from COM63 to COM0(C8h)
Disable COM Left/Right remap (DAh A[5] =0)</td><td>
</td></tr>
<tr><td>8 Alternative COM pin configuration (DAh A[4] =1)
COM output Scan direction: from COM63 to COM0(C8h)
Enable COM Left/Right remap (DAh A[5] =1)</td><td>
</td></tr>
</table>

10.1.19 Set V_{COMH} Deselect Level (DBh)

This command adjusts the V_{COMH} regulator output.

10.1.20 NOP (E3h)

No Operation Command

10.1.21 Status register Read

This command is issued by setting D/C# ON LOW during a data read (See Figure 13-1 to Figure 13-2 for parallel interface waveform). It allows the MCU to monitor the internal status of the chip. No status read is provided for serial mode.

10.2 Graphic Acceleration Command

10.2.1 Horizontal Scroll Setup (26h/27h)

This command consists of consecutive bytes to set up the horizontal scroll parameters and determines the scrolling start page, end page and scrolling speed.

Before issuing this command the horizontal scroll must be deactivated (2Eh). Otherwise, RAM content may be corrupted.

The SSD1306 horizontal scroll is designed for 128 columns scrolling. The following two figures (Figure 10-7, Figure 10-8, Figure 10-9) show the examples of using the horizontal scroll:

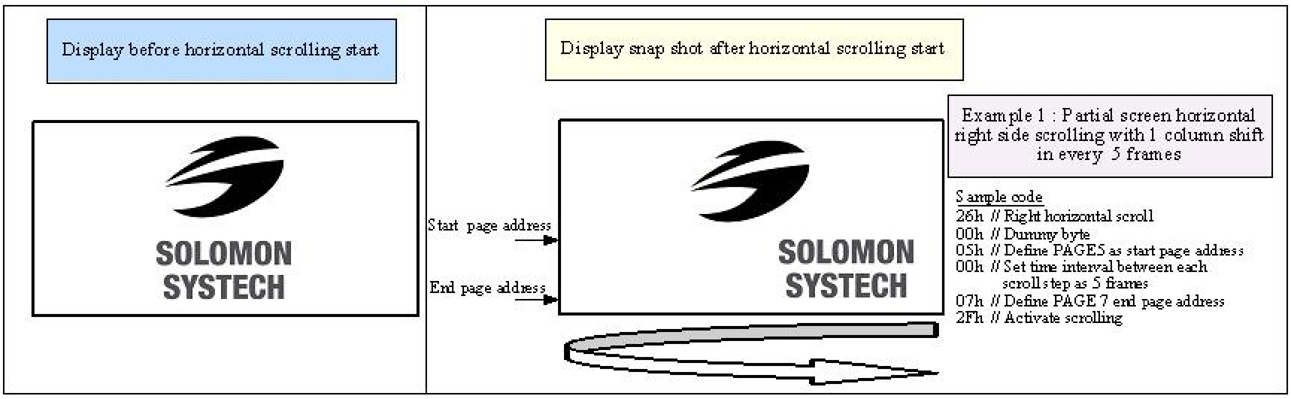
Figure 10-7 : Horizontal scroll example: Scroll RIGHT by 1 column

Original Setting	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	:	:	:	SEG122	SEG123	SEG124	SEG125	SEG126	SEG127
After one scroll step	SEG127	SEG0	SEG1	SEG2	SEG3	SEG4	:	:	:	SEG121	SEG122	SEG123	SEG124	SEG125	SEG126

Figure 10-8 : Horizontal scroll example: Scroll LEFT by 1 column

Original Setting	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	:	:	:	SEG122	SEG123	SEG124	SEG125	SEG126	SEG127
After one scroll step	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	:	:	:	SEG123	SEG124	SEG125	SEG126	SEG127	SEG0

Figure 10-9 : Horizontal scrolling setup example



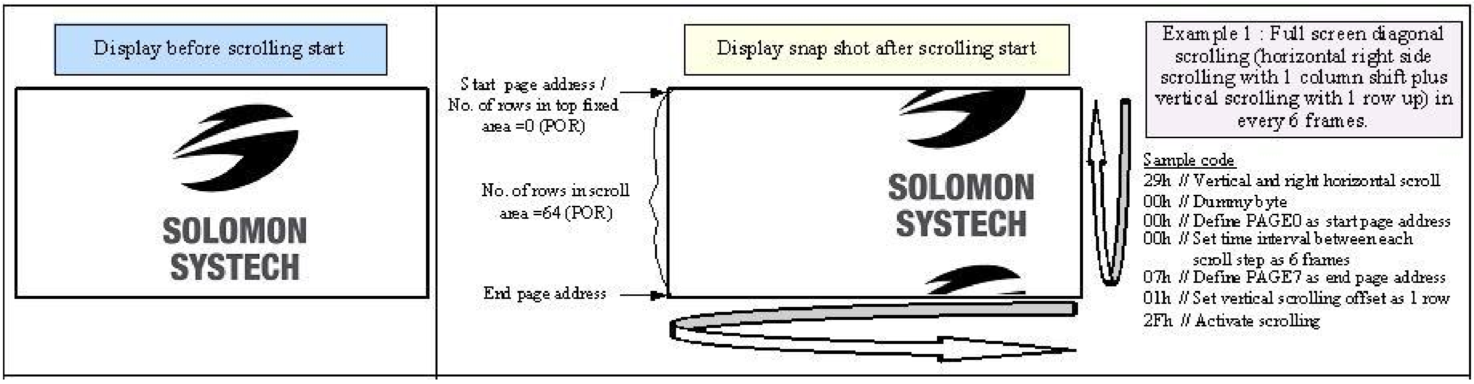
10.2.2 Continuous Vertical and Horizontal Scroll Setup (29h/2Ah)

This command consists of 6 consecutive bytes to set up the continuous vertical scroll parameters and determines the scrolling start page, end page, scrolling speed and vertical scrolling offset.

The bytes B[2:0], C[2:0] and D[2:0] of command 29h/2Ah are for the setting of the continuous horizontal scrolling. The byte E[5:0] is for the setting of the continuous vertical scrolling offset. All these bytes together are for the setting of continuous diagonal (horizontal + vertical) scrolling. If the vertical scrolling offset byte E[5:0] is set to zero, then only horizontal scrolling is performed (like command 26/27h).

Before issuing this command the scroll must be deactivated (2Eh). Otherwise, RAM content may be corrupted. The following figure (Figure 10-10) show the example of using the continuous vertical and horizontal scroll:

Figure 10-10 : Continuous Vertical and Horizontal scrolling setup example



10.2.3 Deactivate Scroll (2Eh)

This command stops the motion of scrolling. After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

10.2.4 Activate Scroll (2Fh)

This command starts the motion of scrolling and should only be issued after the scroll setup parameters have been defined by the scrolling setup commands :26h/27h/29h/2Ah . The setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.

The following actions are prohibited after the scrolling is activated

1. RAM access (Data write or read)
2. Changing the horizontal scroll setup parameters

10.2.5 Set Vertical Scroll Area(A3h)

This command consists of 3 consecutive bytes to set up the vertical scroll area. For the continuous vertical scroll function (command 29/2Ah), the number of rows that in vertical scrolling can be set smaller or equal to the MUX ratio.

11 MAXIMUM RATINGS

Table 11-1 : Maximum Ratings (Voltage Referenced to VSS)

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4	V
V_{CC}		0 to 16	V
V_{SEG}	SEG output voltage	0 to V_{CC}	V
V_{COM}	COM output voltage	0 to 0.9*V_{CC}	V
V_{in}	Input voltage	V_{SS}-0.3 to V_{DD}+0.3	V
T_A	Operating Temperature	-40 to +85	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

12 DC CHARACTERISTICS

Condition (Unless otherwise specified):

Voltage referenced to V_{SS}

V_{DD} = 1.65 to 3.3V

T_A = 25°C

Table 12-1 : DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-	7	-	15	V
V_{DD}	Logic Supply Voltage	-	1.65	-	3.3	V
V_{OH}	High Logic Output Level	I_{OUT} = 100uA, 3.3MHz	0.9 x V_{DD}	-	-	V
V_{OL}	Low Logic Output Level	I_{OUT} = 100uA, 3.3MHz	-	-	0.1 x V_{DD}	V
V_{IH}	High Logic Input Level	-	0.8 x V_{DD}	-	-	V
V_{IL}	Low Logic Input Level	-	-	-	0.2 x V_{DD}	V
$I_{CC, SLEEP}$	$I_{CC,}$ Sleep mode Current	V_{DD} = 1.65V~3.3V, V_{CC} = 7V~15V Display OFF, No panel attached	-	-	10	uA
$I_{DD, SLEEP}$	$I_{DD,}$ Sleep mode Current	V_{DD} = 1.65V~3.3V, V_{CC} = 7V~15V Display OFF, No panel attached	-	-	10	uA
I_{CC}	V_{CC} Supply Current V_{DD} = 2.8V, V_{CC} = 12V, I_{REF} = 12.5uA No loading, Display ON, All ON	Contrast = FFh	-	430	780	uA
I_{DD}	V_{DD} Supply Current V_{DD} = 2.8V, V_{CC} = 12V, I_{REF} = 12.5uA No loading, Display ON, All ON		-	50	150	uA
I_{SEG}	Segment Output Current V_{DD}=2.8V, V_{CC}=12V, I_{REF}=12.5uA, Display ON.	Contrast=FFh	-	100	-	uA
		Contrast=AFh	-	69	-	
		Contrast=3Fh	-	25	-	
Dev	Segment output current uniformity	Dev = $(I_{SEG} – I_{MID})/I_{MID}$ $I_{MID} = (I_{MAX} + I_{MIN})/2$ I_{SEG}[0:131] = Segment current at contrast = FFh	-3	-	+3	%
Adj. Dev	Adjacent pin output current uniformity (contrast = FF)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-2	-	+2	%

13 AC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}
V_{DD}=1.65 to3.3V
T_A = 25°C

Table 13-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC} (1)	Oscillation Frequency of Display Timing Generator	V_{DD} = 2.8V	333	370	407	kHz
F_{FRM}	Frame Frequency for 64 MUX Mode	128x64 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} x 1/(DxKx64) (2)	-	Hz
RES#	Reset low pulse width		3	-	-	us

Note

(1) F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when command D5h A[7:4] is in default value.

(2) D: divide ratio (default value = 1)
K: number of display clocks (default value = 54)
Please refer to Table 9-1 (Set Display Clock Divide Ratio/Oscillator Frequency, D5h) for detailed description

Table 13-2 : 6800-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 13-1 : 6800-series MCU parallel interface characteristics

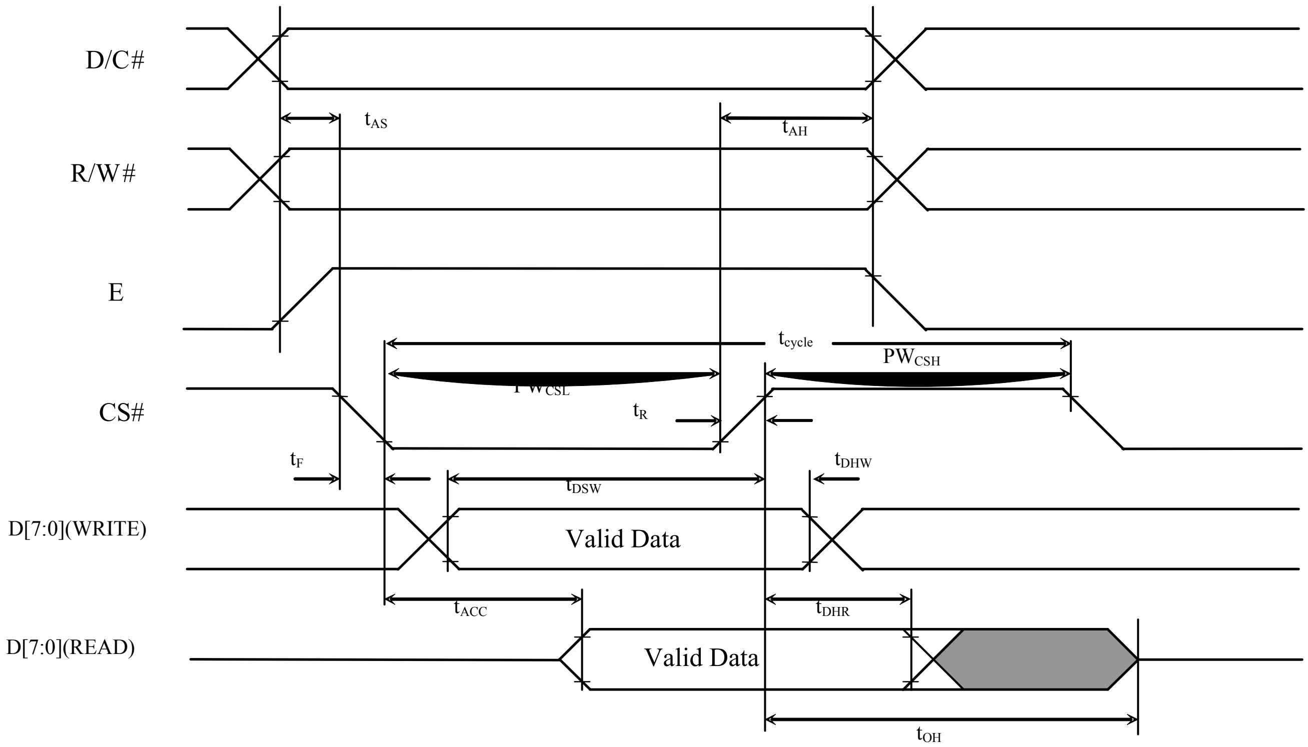


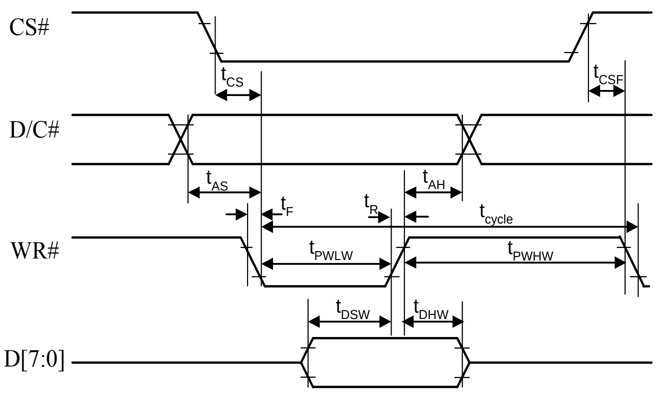
Table 13-3 : 8080-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 13-2 : 8080-series parallel interface characteristics

Write Cycle



Read cycle

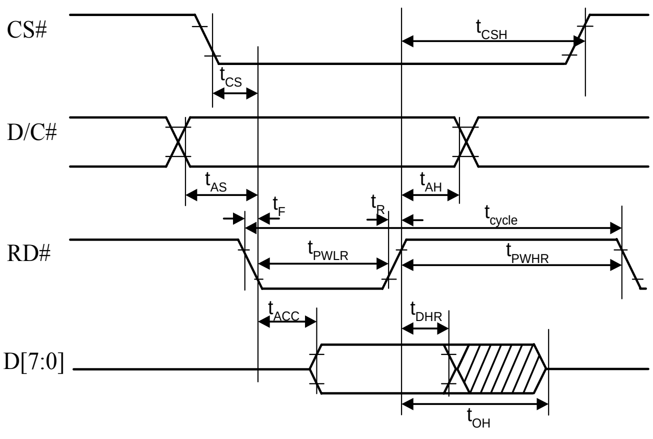
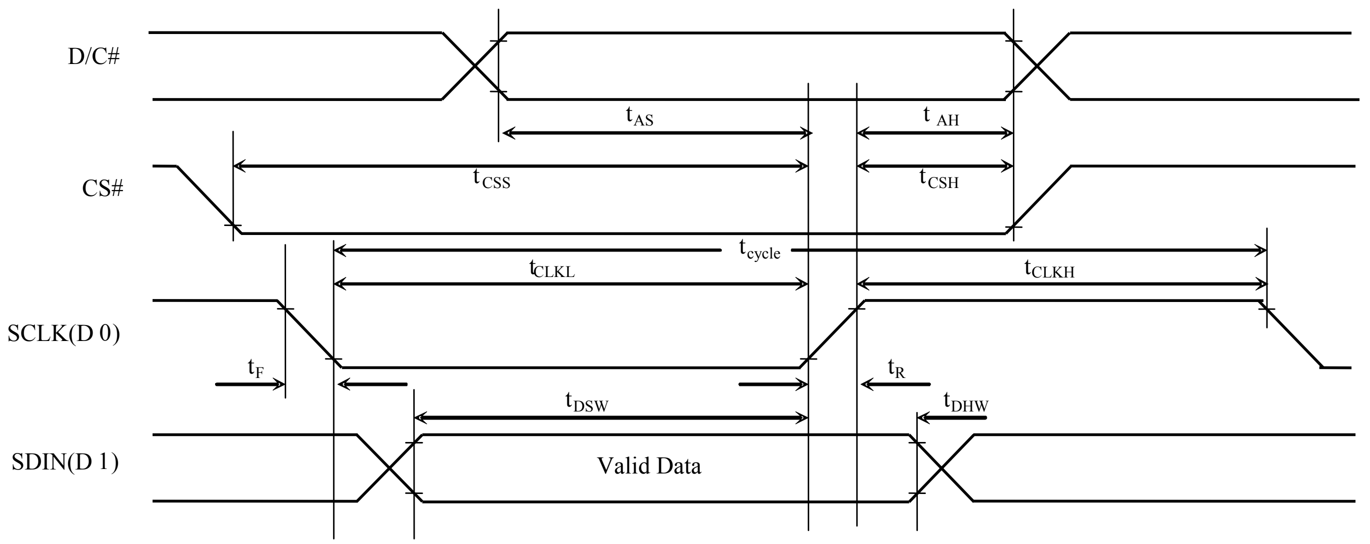


Table 13-4 : 4-wire Serial Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 13-3 : 4-wire Serial interface characteristics



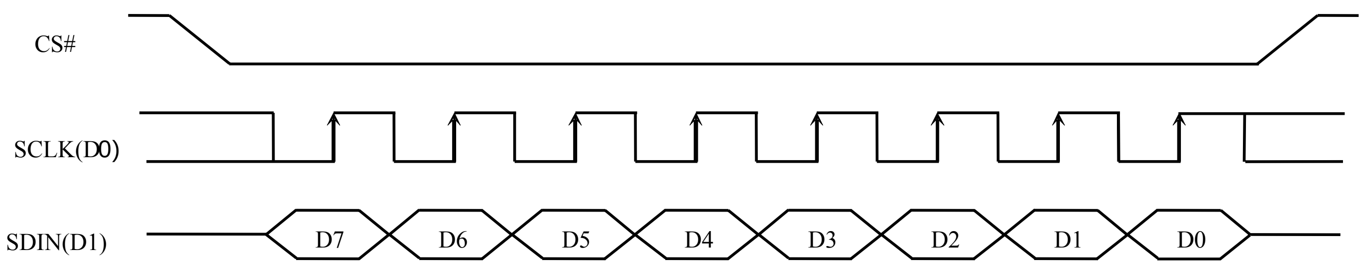
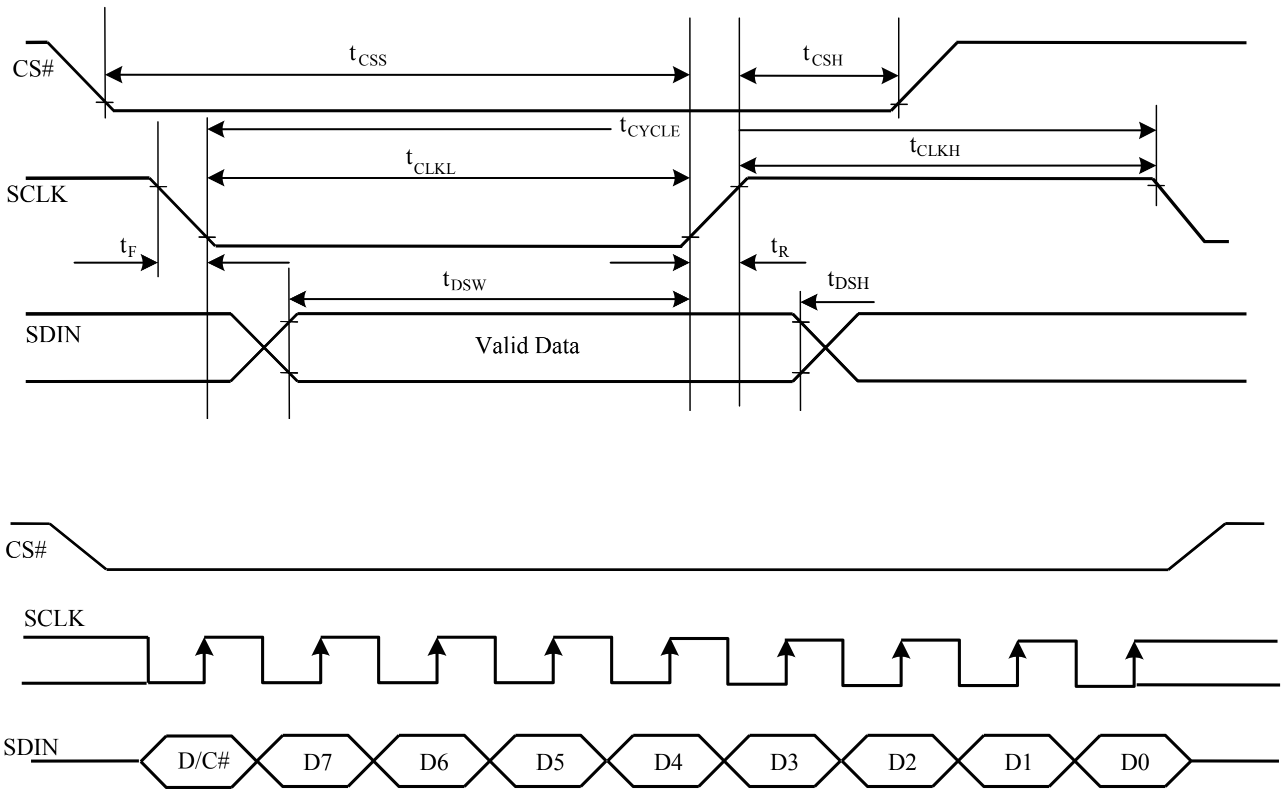


Table 13-5 : 3-wire Serial Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 13-4 : 3-wire Serial interface characteristics



Conditions:

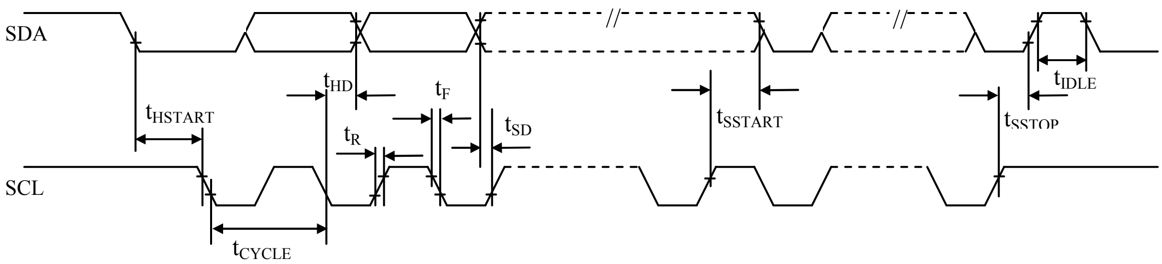
$V_{DD} - V_{SS} = V_{DD} - V_{SS} = 1.65V$ to $3.3V$

$T_A = 25°C$

Table 13-6 :I²C Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

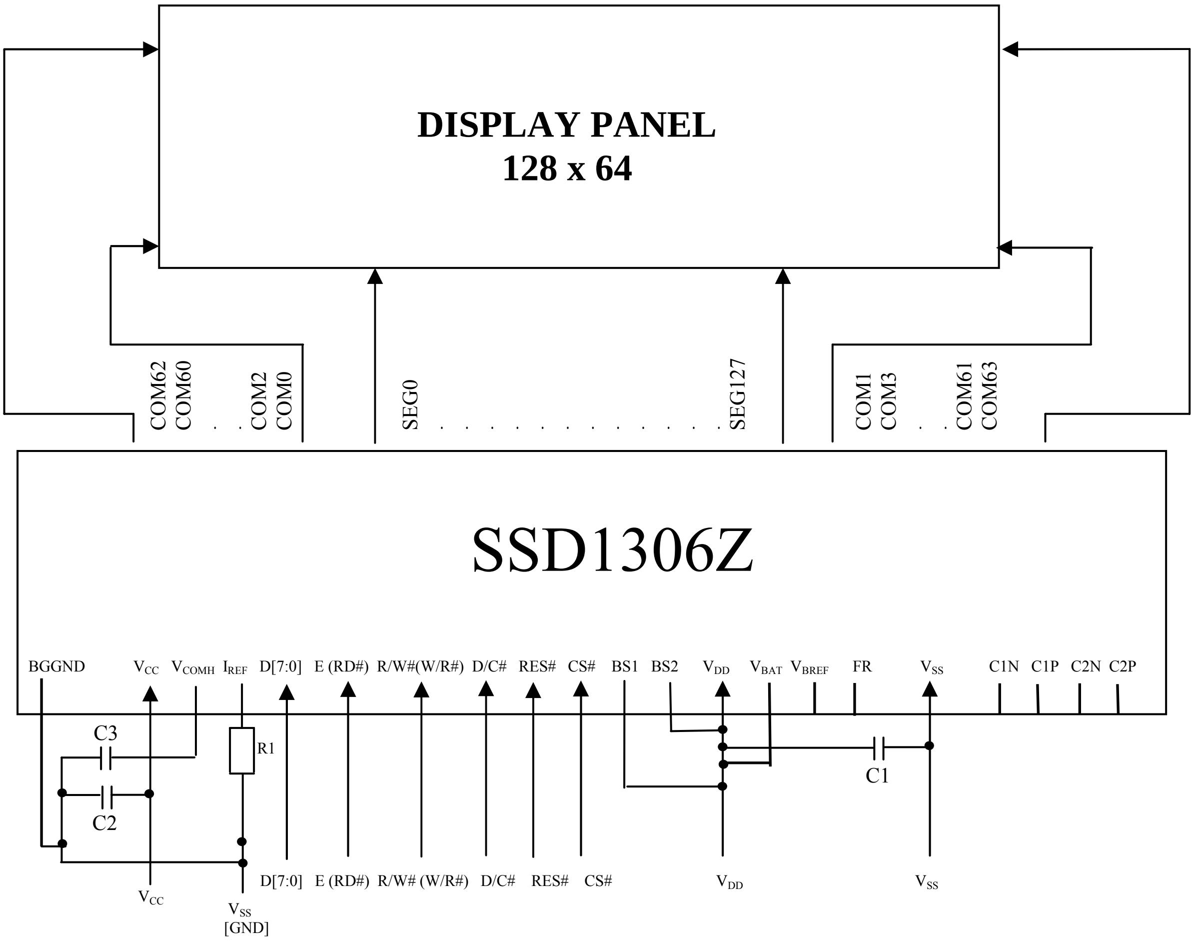
Figure 13-5 : I²C interface Timing characteristics



14 Application Example

Figure 14-1 : Application Example of SSD1306Z

The configuration for 8080-parallel interface mode is shown in the following diagram:
(V_{DD}=2.8V, V_{CC} =12V, I_{REF}=12.5uA)



Pin connected to MCU interface: D[7:0], E, R/W#, D/C#, CS#, RES#
Pin internally connected to V_{SS}: BS0, CL
Pin internally connected to V_{DD}: CLS
C2P, C2N, C1P, C1N, V_{BREF}, FB should be left open.

C1: 1.0uF [(1)]
C2: 2.2uF [(1)]
C3: 2.2uF [(1)]

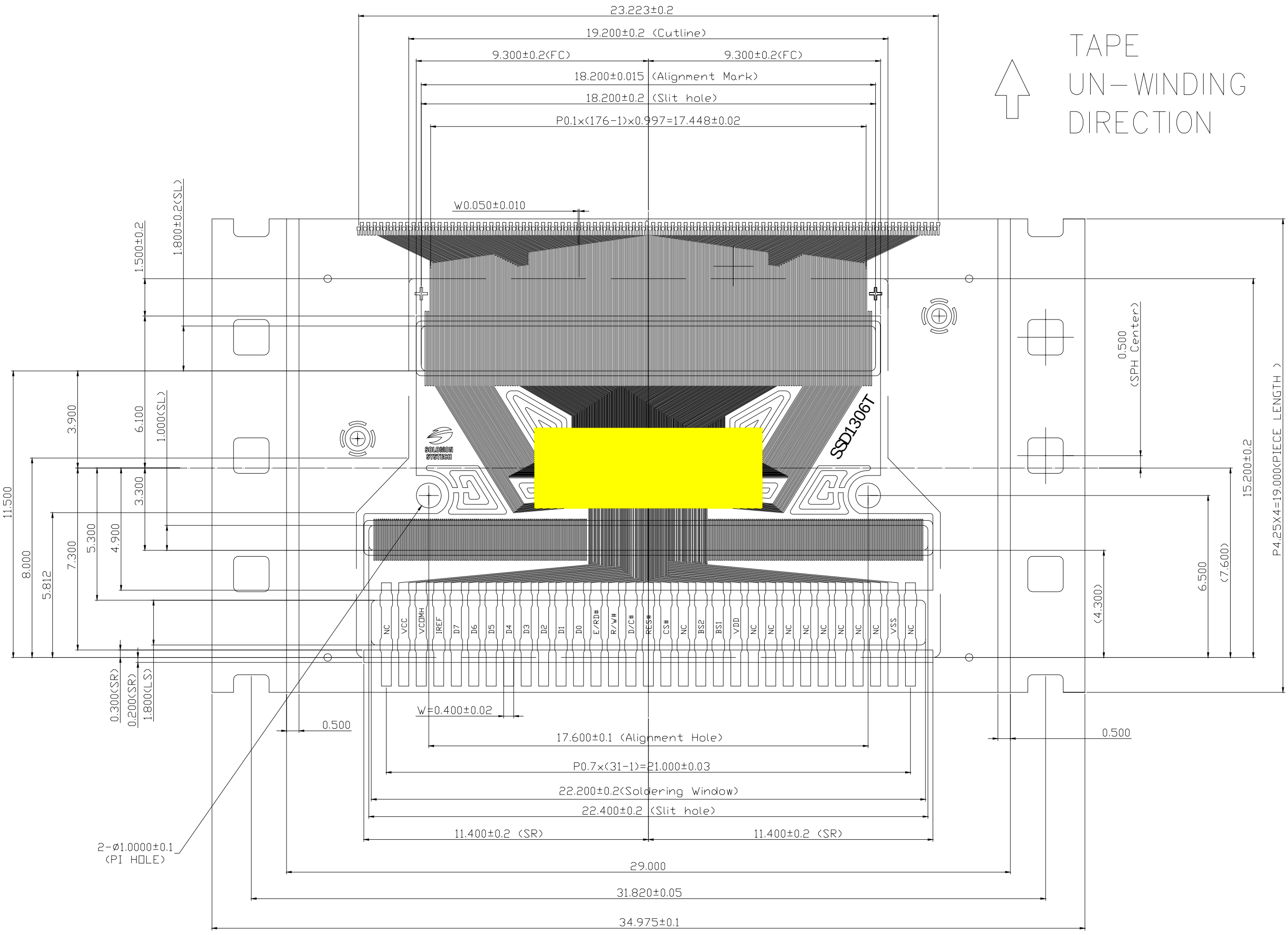
Voltage at I_{REF} = V_{CC} – 2.5V. For V_{CC} = 12V, I_{REF} = 12.5uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
= (12-2.5) / 12.5u
=760KΩ

Note
[(1)] The capacitor value is recommended value. Select appropriate value against module application.

15 PACKAGE INFORMATION

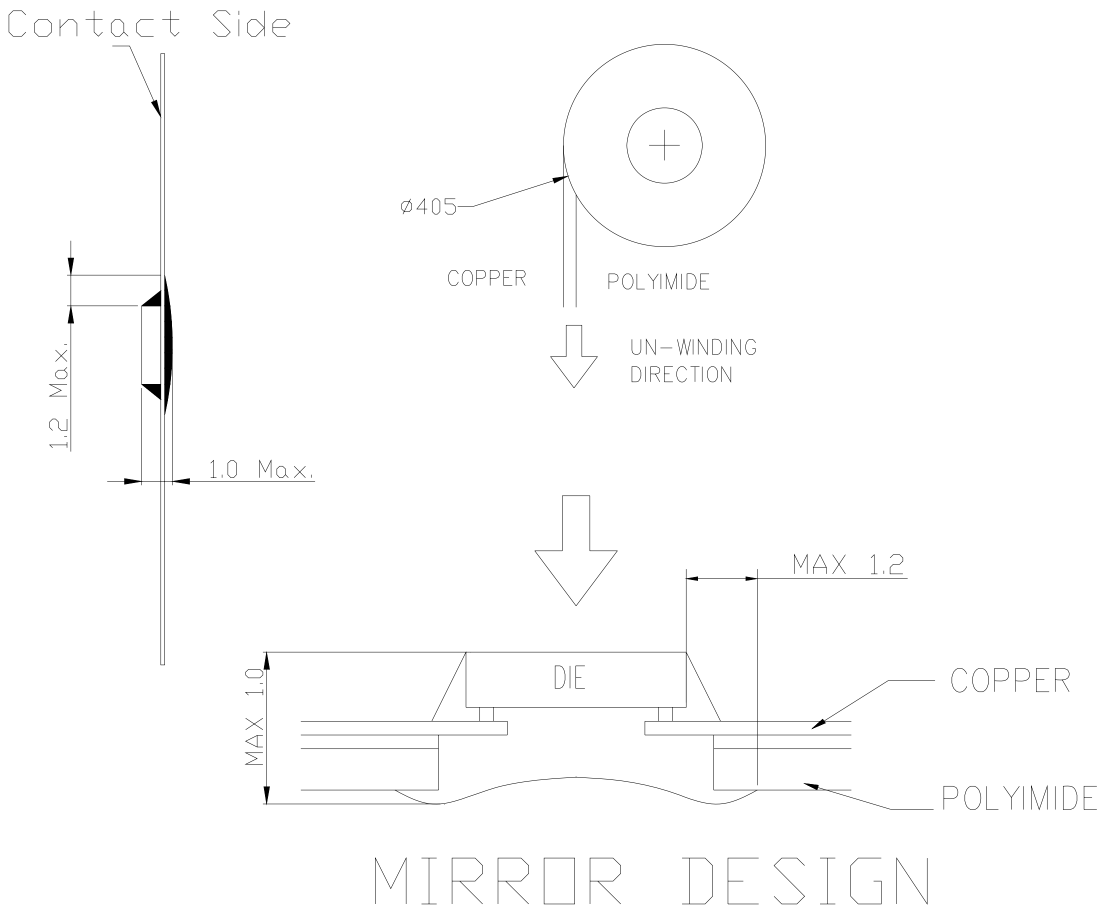
15.1 SSD1306TR1 Detail Dimension

Figure 15-1 SSD1306TR1 Detail Dimension



Specification:

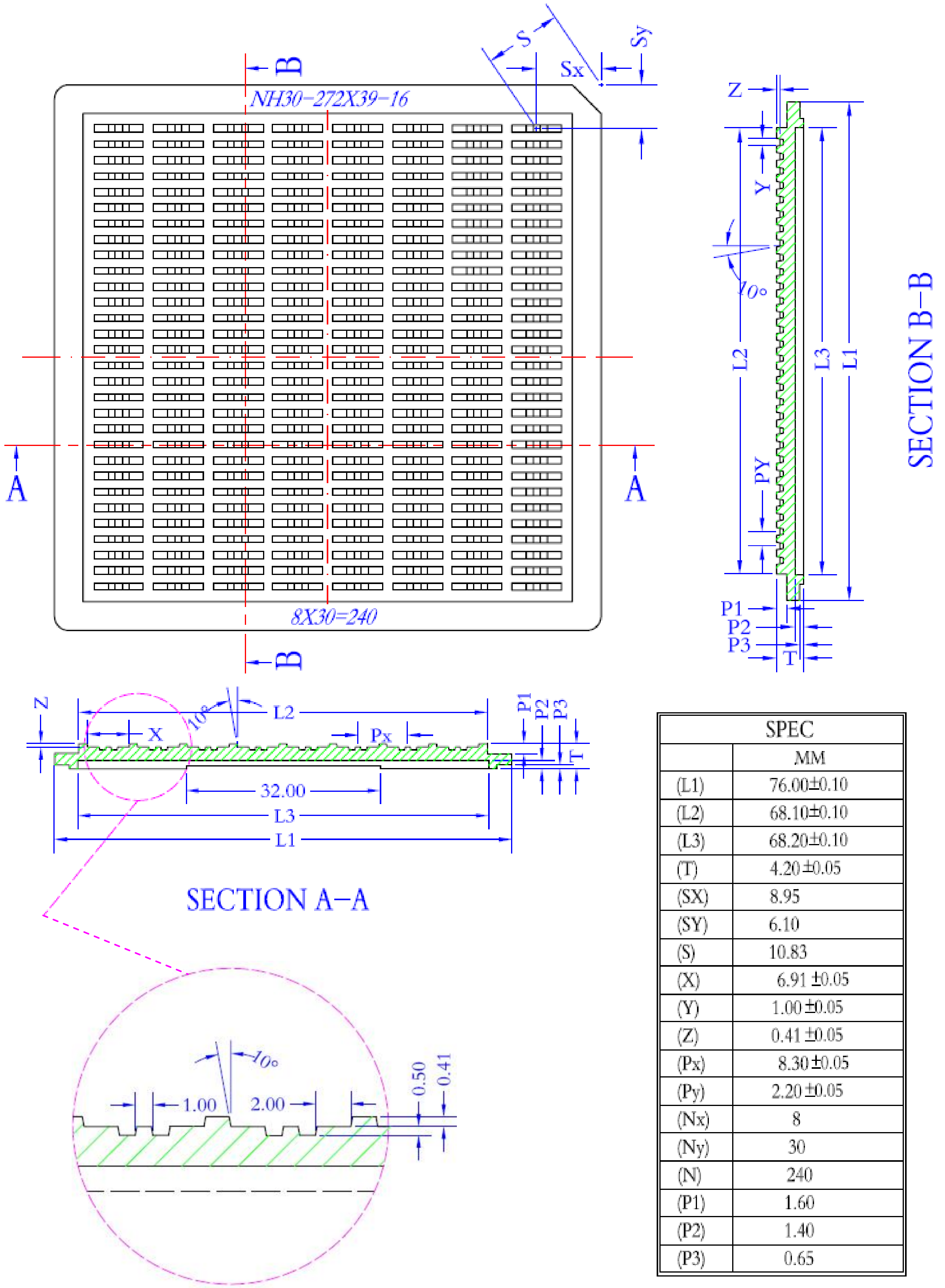
1. GENERAL TOLERANCE: ±0.05 mm
2. MATERIAL
   PI: 75 ± 8 um
   CU: 15 ± 3 um
   ADHESIVE: 12 ± 3um
   SR: 26 ± 14 um
   TOLERANCE ± 0.200 mm
   FLEX COATING: Min10 um
3. Plating : Sn 0.20 ±0.05 um
4. TAPESITE: 4 SPH,19 mm



Contact Side
1.2 Max.
1.0 Max.
ø405
COPPER
POLYIMIDE
UN-WINDING
DIRECTION
MAX 1.2
DIE
MAX 1.0
COPPER
POLYIMIDE
MIRROR DESIGN

15.2 SSD1306Z Die Tray Information

Figure 15-2 : SSD1306Z die tray information



SPEC	
	MM
(L1)	76.00±0.10
(L2)	68.10±0.10
(L3)	68.20±0.10
(T)	4.20 ±0.05
(SX)	8.95
(SY)	6.10
(S)	10.83
(X)	6.91 ±0.05
(Y)	1.00 ±0.05
(Z)	0.41 ±0.05
(Px)	8.30±0.05
(Py)	2.20 ±0.05
(Nx)	8
(Ny)	30
(N)	240
(P1)	1.60
(P2)	1.40
(P3)	0.65

All Solomon Systech Products complied with six (6) hazardous substances limitation requirement per European Union (EU) "Restriction of Hazardous Substance (RoHS) Directive (2002/95/EC)" and China standard "电子信息产品污染控制标识要求 (SJ/T11364-2006)" with control Marking Symbol . Hazardous Substances test report is available upon requested.

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SSD1306

Application Note

128 x 64 Dot Matrix
OLED/PLED Segment/Common Driver with Controller

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TABLE OF CONTENTS

TABLE OF FIGURES

1 Introduction

This application note of SSD1306 is written to explain the charge pump regulator function of SSD1306. SSD1306 is a single-chip CMOS OLED/PLED driver with controller for organic / polymer light emitting diode dot-matrix graphic display system. It consists of 128 segments and 64 commons. This IC is designed for Common Cathode type OLED panel.

For the detailed characteristics of the driver IC, please refer to SSD1306 datasheet.

2 Charge Pump Regulator

The internal regulator circuit in SSD1306 accompanying only 2 external capacitors can generate a 7.5V voltage supply, $V_{CC,}$ from a low voltage supply input, V_{BAT}. The V_{CC} is the voltage supply to the OLED driver block. This is a switching capacitor regulator circuit, designed for handheld applications. This regulator can be turned on/off by software command setting.

- Power supply
  - V_{DD} = 1.65V to 3.3V,<V_{BAT} for IC logic
  - V_{BAT} = 3.3V to 4.2V for charge pump regulator circuit

- Pins description for related pins of the charge pump regulator
  - V_{BAT} – Power supply for charge pump regulator circuit.

Status	V_{BAT}	V_{DD}	V_{CC}
Enable charge pump	Connect to external V_{BAT} source	Connect to external V_{DD} source	A capacitor should be connected between this pin and V_{SS}
Disable charge pump	Connect with V_{DD} pin	Connect to external V_{DD} source	Connect to external V_{CC} source

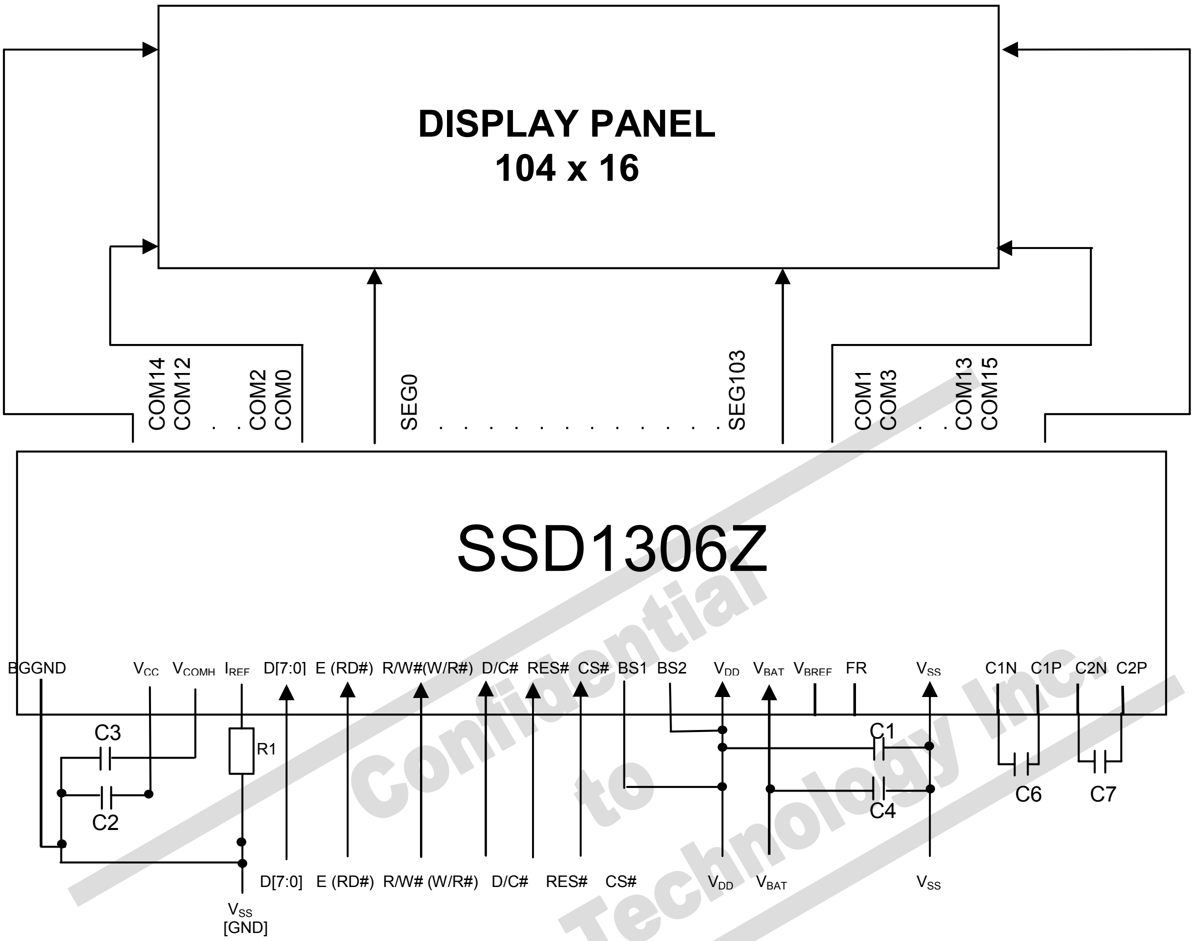
  - C1P/C1N – Pin for charge pump capacitor; Connect to each other with a capacitor
  - C2P/C2N – Pin for charge pump capacitor; Connect to each other with a capacitor

2.1 Command Table for Charge Bump Setting

1. Charge Pump Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	8D	1	0	0	0	1	1	0	1	Charge Pump Setting	A[2] = 0b, Disable charge pump(RESET) A[2] = 1b, Enable charge pump during display on **Note** (1) The Charge Pump must be enabled by the following command: 8Dh ; Charge Pump Setting 14h ; Enable Charge Pump AFh; Display ON
0	A[7:0]	*	*	0	1	0	A_2	0	0		

Figure 1 : Application Example of SSD1306Z with charge bump

The configuration for 8080-parallel interface mode is shown in the following diagram:
(V_{DD}= 1.65V ~ 3.3V, < V_{BAT} , V_{BAT}=3.3V~4.2V, I_{REF}=12.5uA)



Pin connected to MCU interface: D[7:0], E, R/W#, D/C#, CS#, RES#
Pin internally connected to V_{SS}: BS0, CL
Pin internally connected to V_{DD}: CLS
VBREF, FR should be left open.

C1, C4, C6, C7: 1.0uF (1)
C2, C3: 2.2uF (1)

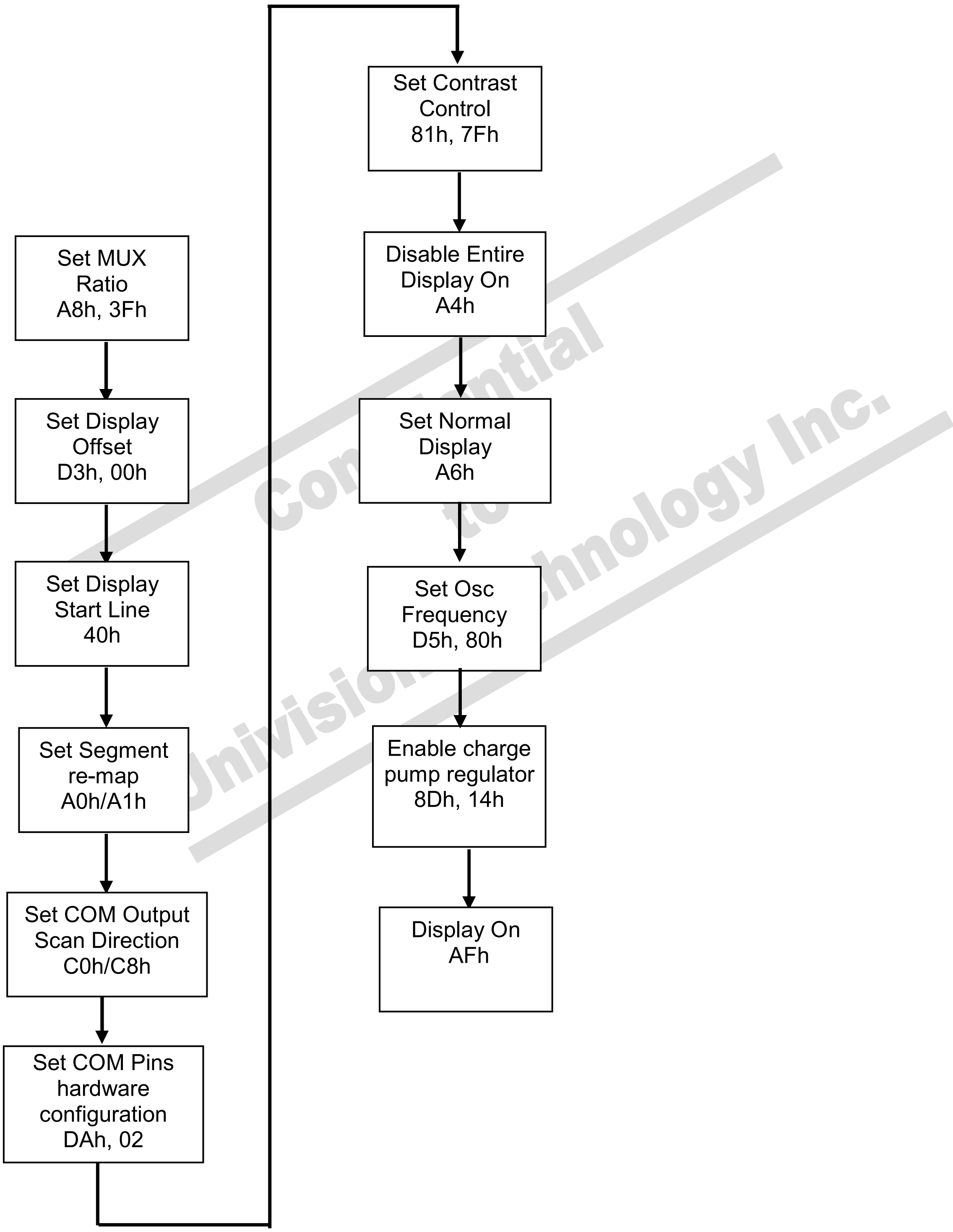
Voltage at I_{REF} = V_{CC} – 2.5V. For V_{CC} = 7.5V, I_{REF} = 12.5uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
= (7.5-2.5) / 12.5u
=400KΩ

Note
(1) The capacitor value is recommended value. Select appropriate value against module application.

3 Software Configuration

SSD1306 has internal command registers that are used to configure the operations of the driver IC. After reset, the registers should be set with appropriate values in order to function well. The registers can be accessed by MPU interface in either 6800, 8080, SPI type with D/C# pin pull low or using I^2C interface. Below is an example of initialization flow of SSD1306. The values of registers depend on different condition and application.

Figure 2 : Software Initialization Flow Chart



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Product Specification

Part Name: OEL Display Module
Part ID: UG-2864HSWEG01
Doc No.: SAS1-9046-B

Customer:
Approved by

From: Univision Technology Inc.
Approved by

Univision Technology Inc.
8, Kebei RD 2, Science Park, Chu-Nan, Taiwan 350, R.O.C.

Notes:
1. Please contact Univision Technology Inc. before assigning your product based on this module specification
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by Univision Technology Inc. for any intellectual property claims or other problems that may result from application based on the module described herein.

Revised History

Part Number	Revision	Revision Content	Revised on
UG-2864HSWEG01	A	New	February 17, 2009
UG-2864HSWEG01	B	Page 5~6 *Section 1.6* Update Application Circuit Page 7 *Section 2* Update Absolute Maximum Ratings Page 8 *Section 3.1 & 3.2* Modify Brightness V_{CC} Supplied Externally (Min/Typ) 80/100→100/120 *V_{CC} Generated by Internal DC/DC* *(Min/Typ) 50/60→70/90* Update DC Characteristics Page 15 *Section 4.4* Update Initialization	June 5, 2009

Notice:

Contents

1. Basic Specifications

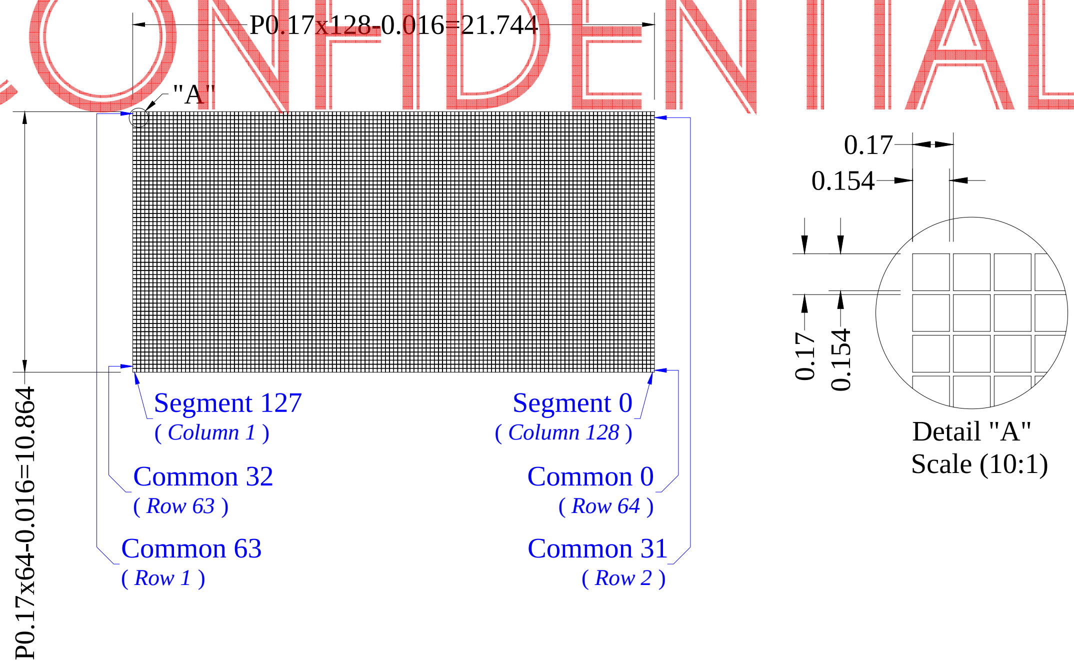
1.1 Display Specifications

1) Display Mode: Passive Matrix
2) Display Color: Monochrome (White)
3) Drive Duty: 1/64 Duty

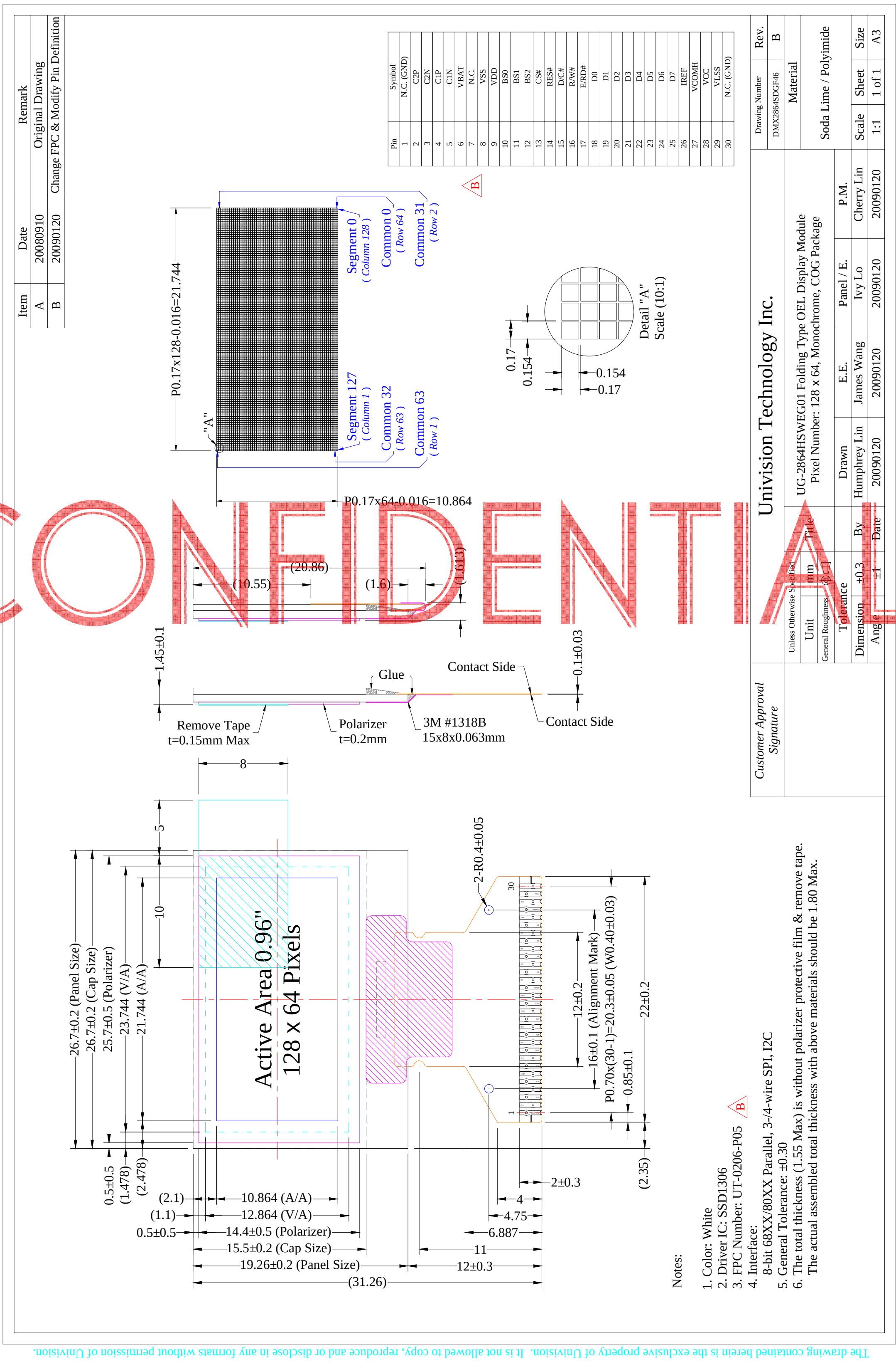
1.2 Mechanical Specifications

1) Outline Drawing: According to the annexed outline drawing
2) Number of Pixels: 128 × 64
3) Panel Size: 26.70 × 19.26 × 1.45 (mm)
4) Active Area: 21.744 × 10.864 (mm)
5) Pixel Pitch: 0.17 × 0.17 (mm)
6) Pixel Size: 0.154 × 0.154 (mm)
7) Weight: 1.54 (g)

1.3 Active Area & Pixel Construction



1.4 Mechanical Drawing



1.5 Pin Definition

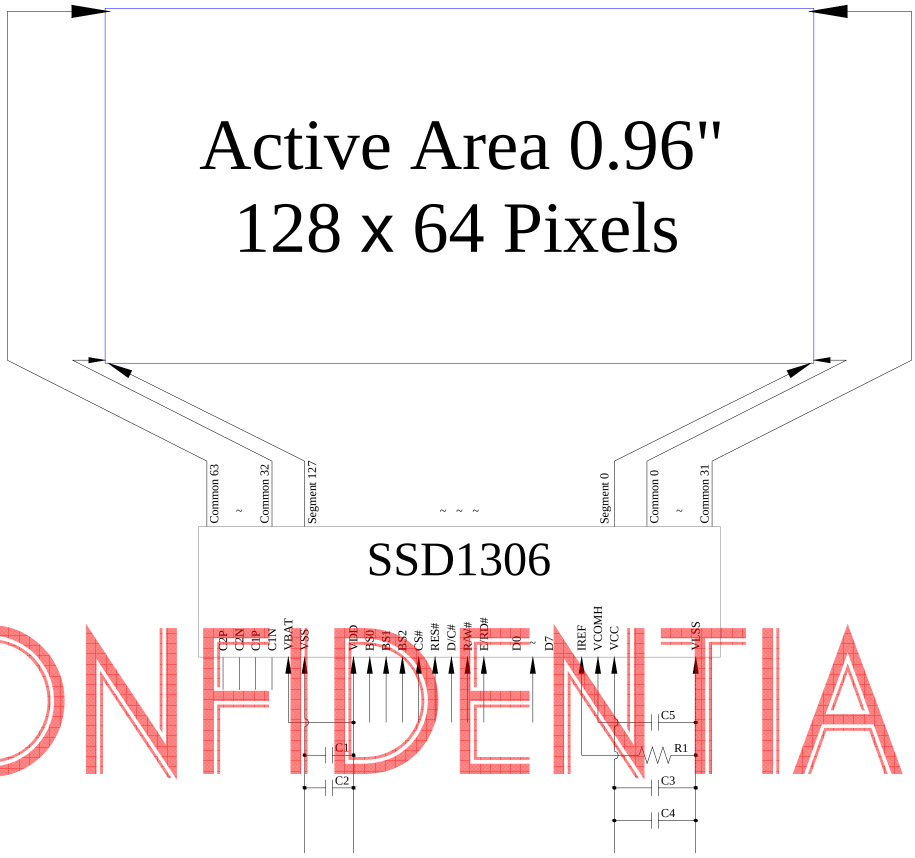
<table>
<tr><th>Pin Number</th><th>Symbol</th><th>Type</th><th>Function</th></tr>
<tr><td colspan="4">Power Supply</td></tr>
<tr><td>9</td><td>VDD</td><td>P</td><td>Power Supply for Logic
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>8</td><td>VSS</td><td>P</td><td>Ground of Logic Circuit
This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>28</td><td>VCC</td><td>P</td><td>Power Supply for OEL Panel
This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and VSS when the converter is used. It must be connected to external source when the converter is not used.</td></tr>
<tr><td>29</td><td>VLSS</td><td>P</td><td>Ground of Analog Circuit
This is an analog ground pin. It should be connected to VSS externally.</td></tr>
<tr><td colspan="4">Driver</td></tr>
<tr><td>26</td><td>IREF</td><td>I</td><td>Current Reference for Brightness Adjustment
This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 12.5μA.</td></tr>
<tr><td>27</td><td>VCOMH</td><td>O</td><td>Voltage Output High Level for COM Signal
This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.</td></tr>
<tr><td colspan="4">DC/DC Converter</td></tr>
<tr><td>6</td><td>VBAT</td><td>P</td><td>Power Supply for DC/DC Converter Circuit
This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to VDD when the converter is not used.</td></tr>
<tr><td>4 / 5
2 / 3</td><td>C1P / C1N
C2P / C2N</td><td>I</td><td>Positive Terminal of the Flying Inverting Capacitor
Negative Terminal of the Flying Boost Capacitor
The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.</td></tr>
<tr><td colspan="4">Interface</td></tr>
<tr><td>10
11
12</td><td>BS0
BS1
BS2</td><td>I</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><th></th><th>BS0</th><th>BS1</th><th>BS2</th></tr>
<tr><td>I2C</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>3-wire SPI</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>4-wire SPI</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>8-bit 68XX Parallel</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>8-bit 80XX Parallel</td><td>0</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>14</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
</table>

1.5 Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
Interface (Continued)			
13	CS#	I	*Chip Select* This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.
15	D/C#	I	*Data/Command Control* This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams. When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection.
17	E/RD#	I	*Read/Write Enable or Read* This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.
16	R/W#	I	*Read/Write Select or Write* This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
18~25	D0~D7	I/O	*Host Data Input/Output Bus* These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2C mode is selected, D2 & D1 should be tired together and serve as SDAout & SDAin in application and D0 is the serial clock input SCL.
Reserve			
7	N.C.	-	*Reserved Pin* The N.C. pins between function pins are reserved for compatible and flexible design.
1, 30	N.C. (GND)	-	*Reserved Pin (Supporting Pin)* The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.

1.6 Block Diagram

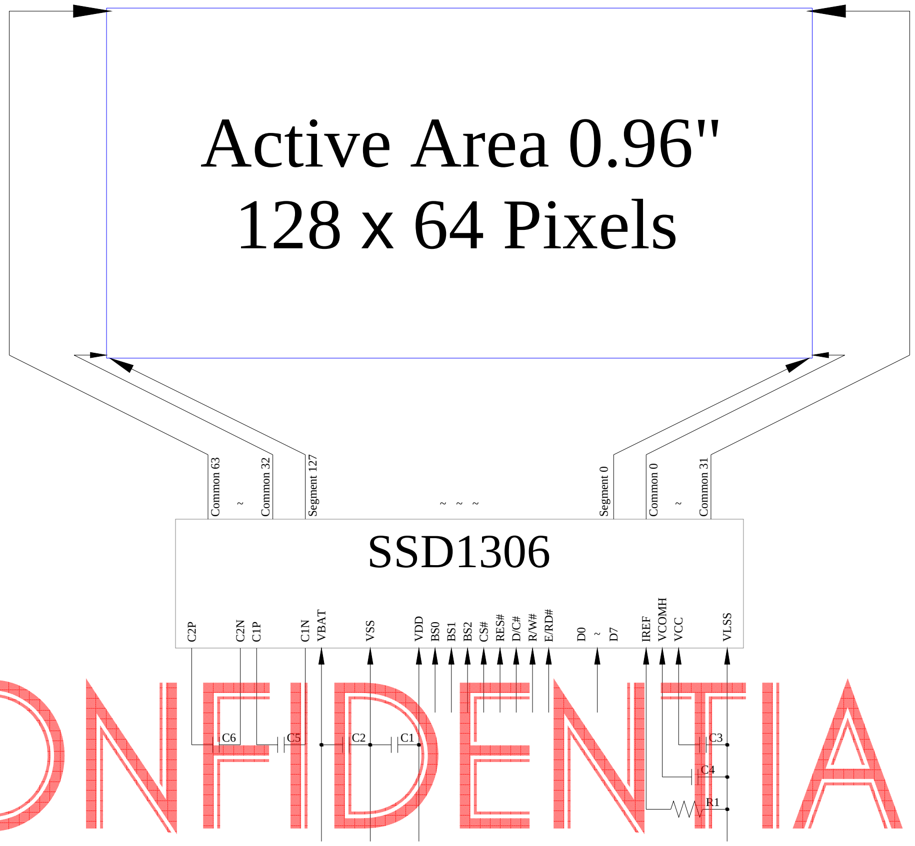
1.6.1 V_{CC} Supplied Externally



MCU Interface Selection: BS0, BS1 and BS2
Pins connected to MCU interface: CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7

C1, C3: 0.1µF
C2: 2.2µF
C4, C5: 4.7µF / 16V, X7R
R1: 560kΩ, R1 = (Voltage at IREF – VSS) / IREF

1.6.2 V_{CC} Generated by Internal DC/DC Circuit



MCU Interface Selection: BS0, BS1 and BS2
Pins connected to MCU interface: CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7

C1, C2, C5, C6: 1μF
C3: 2.2μF
C4: 4.7μF / 16V, X7R
R1: 390kΩ, R1 = (Voltage at IREF – VSS) / IREF

2. *Absolute Maximum Ratings*

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	4	V	1, 2
Supply Voltage for Display	V_{CC}	0	11	V	1, 2
Supply Voltage for DC/DC	V_{BAT}	*-0.3*	*5*	*V*	*1, 2*
Operating Temperature	T_{OP}	-30	70	°C	-
Storage Temperature	T_{STG}	-40	80	°C	-

Note 1: All the above voltages are on the basis of “VSS = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. “Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (V_{CC} Supplied Externally)	L_{br}	With Polarizer (Note 3)	100	120	-	cd/m^2
Brightness (V_{CC} Generated by Internal DC/DC)	L_{br}	*With Polarizer (Note 4)*	70	90	-	cd/m^2
C.I.E. (White)	(x) (y)	Without Polarizer	0.28 0.29	0.32 0.33	0.36 0.37	
Dark Room Contrast	CR		-	>2000:1	-	
View Angle			>160	-	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 9V & 7.25V.
Software configuration follows Section 4.4 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}	-	1.65	2.8	3.3	V
Supply Voltage for Display (Supplied Externally)	V_{CC}	Note 3	8.5	9	9.5	V
Supply Voltage for DC/DC	V_{BAT}	*Internal DC/DC Enable*	3.5	-	4.2	V
Supply Voltage for Display (Generated by Internal DC/DC)	V_{CC}	*Note 4*	7	7.25	7.5	V
High Level Input	V_{IH}	-	$0.8\times V_{DD}$	-	V_{DD}	V
Low Level Input	V_{IL}	-	0	-	$0.2\times V_{DD}$	V
High Level Output	V_{OH}	I_{OUT} = 100μA, 3.3MHz	$0.9\times V_{DD}$	-	V_{DD}	V
Low Level Output	V_{OL}	I_{OUT} = 100μA, 3.3MHz	0	-	$0.1\times V_{DD}$	V
Operating Current for V_{DD}	I_{DD}	-	-	180	300	μA
Operating Current for V_{CC} (V_{CC} Supplied Externally)	I_{CC}	Note 5	-	7.3	9.1	mA
		Note 6	-	12.3	15.4	mA
Operating Current for V_{BAT} (V_{CC} Generated by Internal DC/DC)	I_{BAT}	*Note 7*	-	17.3	21.6	mA
		Note 8	-	23.1	28.9	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$	-	-	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$	-	-	1	5	μA

Note 3 & 4: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.
Note 5: V_{DD} = 2.8V, V_{CC} = 9V, 50% Display Area Turn on.
Note 6: V_{DD} = 2.8V, V_{CC} = 9V, 100% Display Area Turn on.
Note 7: V_{DD} = 2.8V, V_{CC} = 7.25V, 50% Display Area Turn on.
Note 8: V_{DD} = 2.8V, V_{CC} = 7.25V, 100% Display Area Turn on.

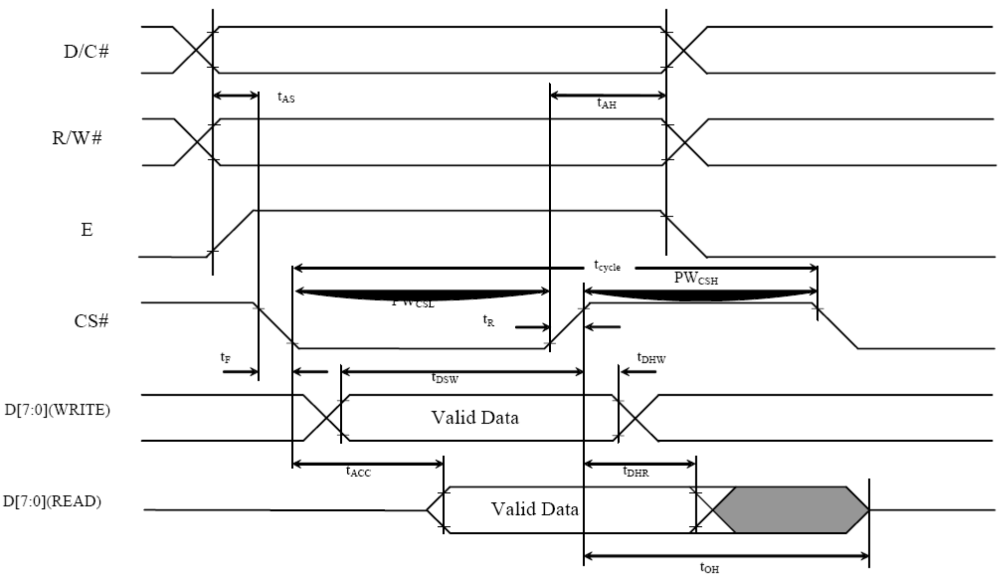
* Software configuration follows Section 4.4 Initialization.

3.3 AC Characteristics

3.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	0	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

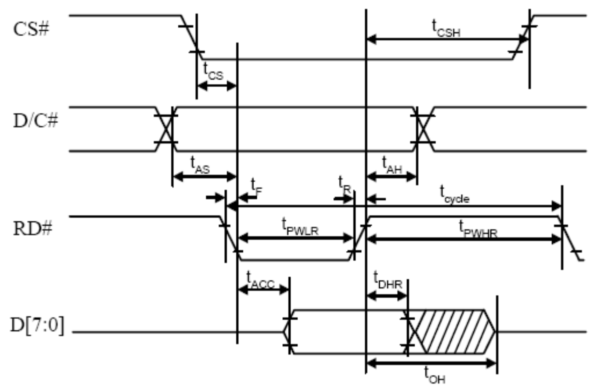
* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



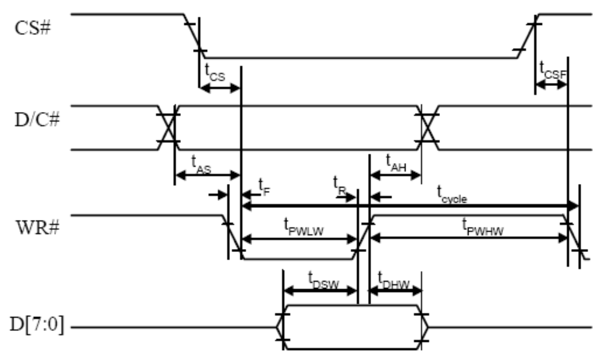
3.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	120	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



(Read Timing)

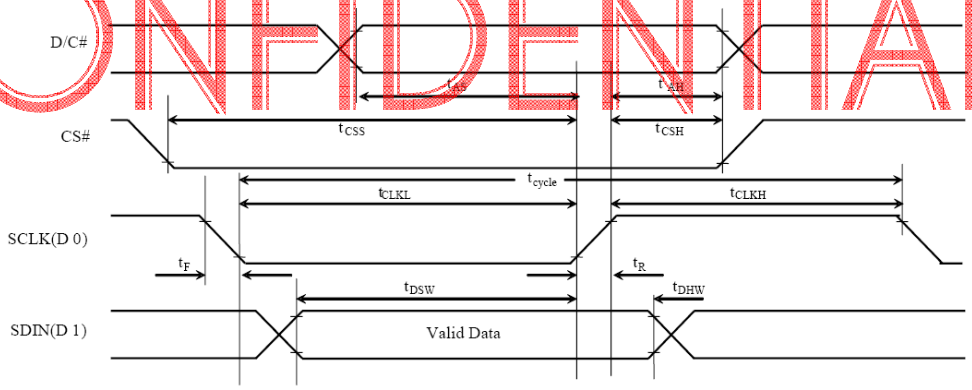


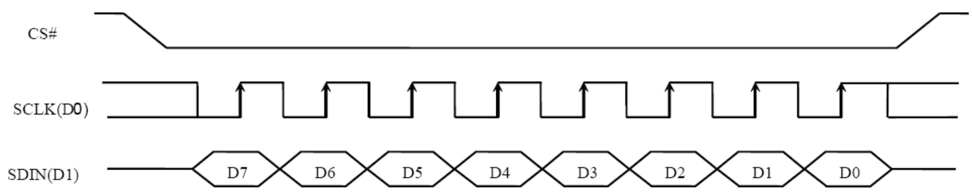
(Write Timing)

3.3.3 Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)

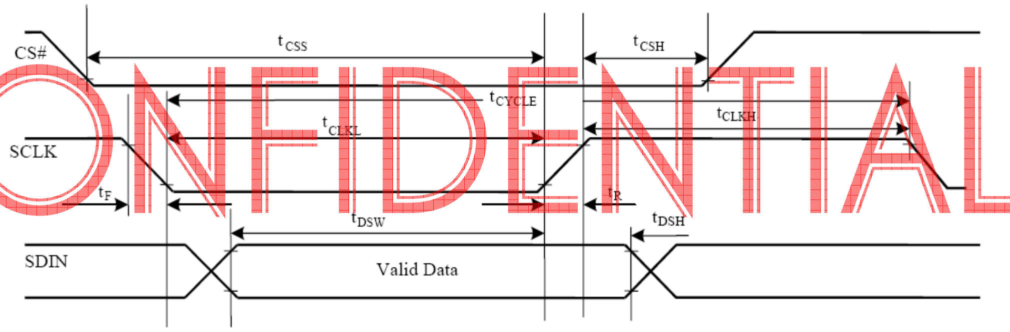


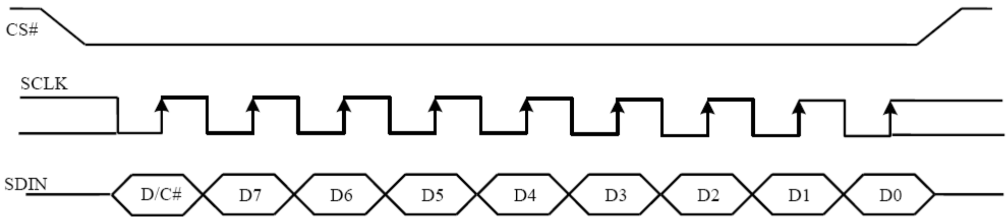


3.3.4 Serial Interface Timing Characteristics: (3-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)

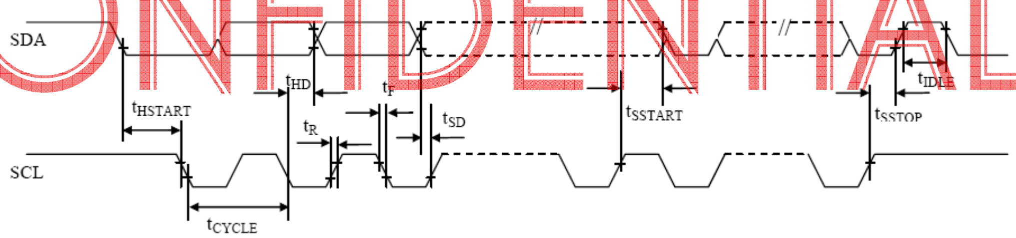




3.3.5 I²C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	us
t_{HSTART}	Start Condition Hold Time	0.6	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" Pin)	0	-	ns
	Data Hold Time (for "SDA_{IN}" Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	us
t_{SSTOP}	Stop Condition Setup Time	0.6	-	us
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	us

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



4. Functional Specification

4.1. Commands

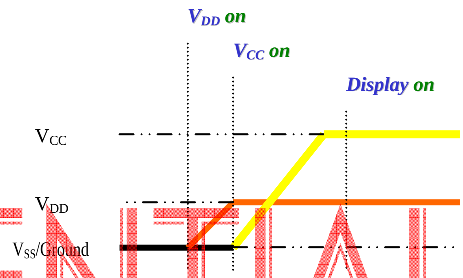
Refer to the Technical Manual for the SSD1306

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

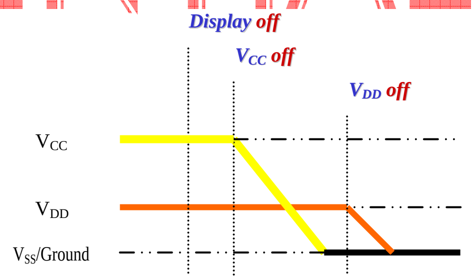
4.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



4.3 Reset Circuit

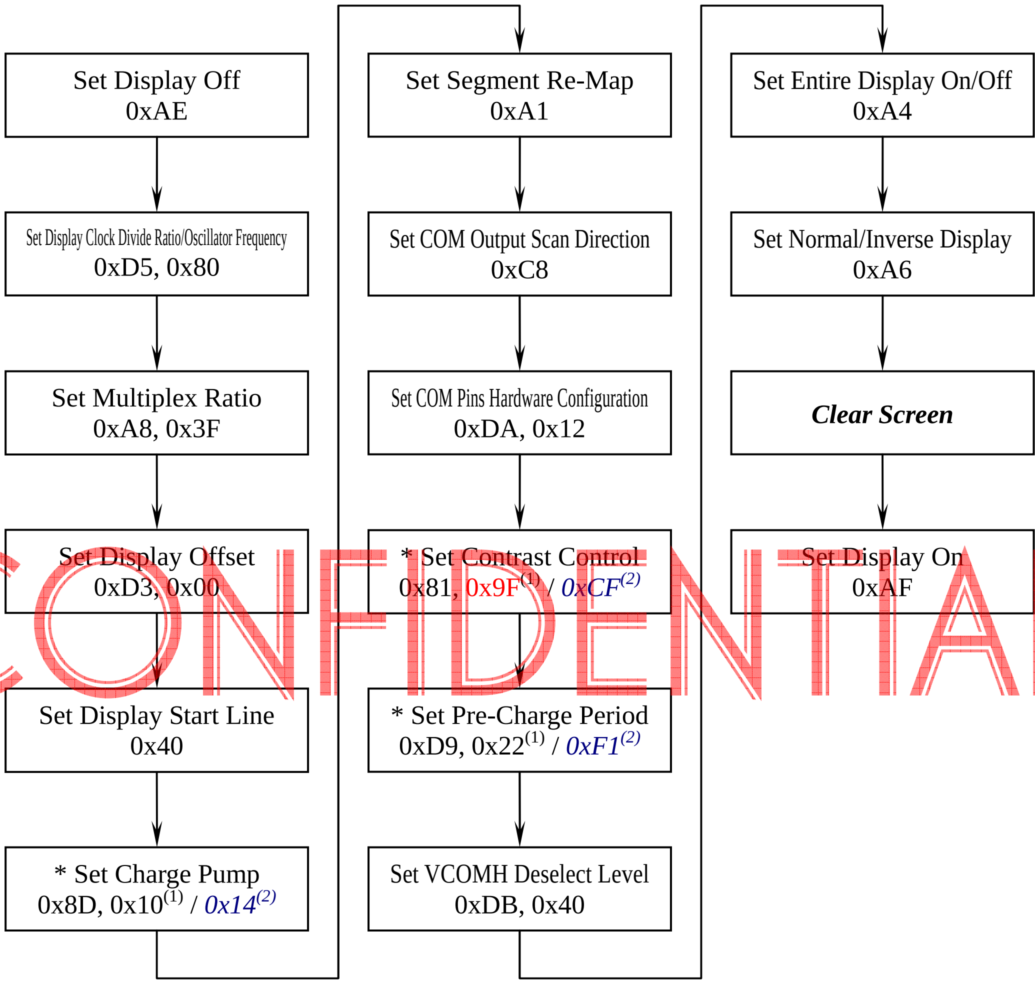
When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

4.4 Actual Application Example

Command usage and explanation of an actual example

<Initialization>



* Written Value for Parameters

(1) ➔ V_{CC} Supplied Externally

(2) ➔ V_{CC} Generated by Internal DC/DC Circuit

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

5. *Reliability*

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-30°C, 240 hrs	
High Temperature Storage	80°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Lifetime

End of lifetime is specified as 50% of initial brightness reached.

Parameter	Min	Max	Unit	Condition	Notes
Operating Life Time	10,000	-	hr	100 cd/m^2, 50% Checkerboard	6
Storage Life Time	20,000	-	hr	T_a = 25°C, 50% RH	-

Note 6: The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

5.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

6. *Outgoing Quality Control Specifications*

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15 %RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50 cm
Distance between the Panel & Eyes of the Inspector:	≥ 30 cm

Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic.

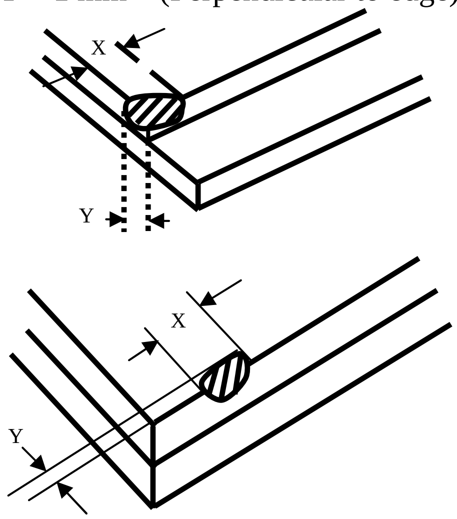
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

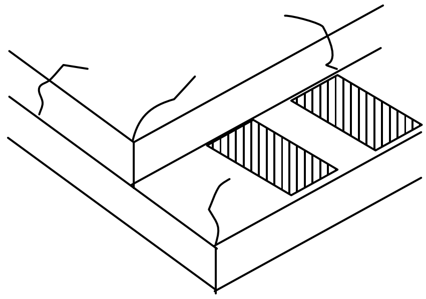
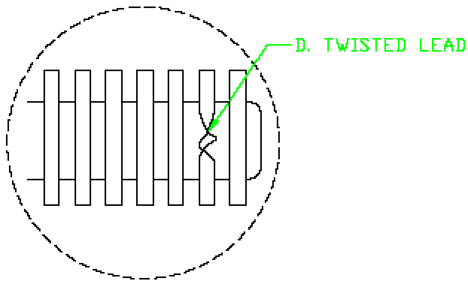
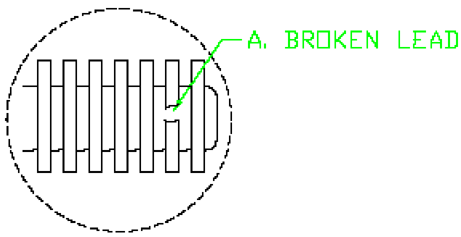
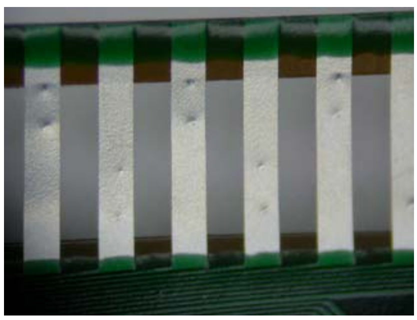
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

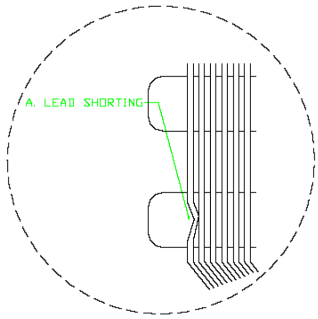
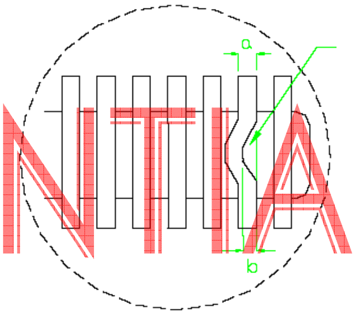
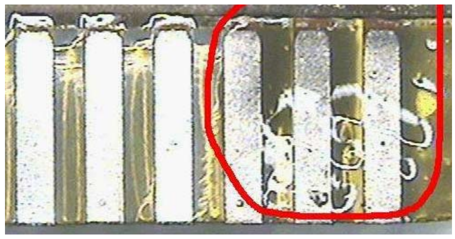
6.3.1 Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 

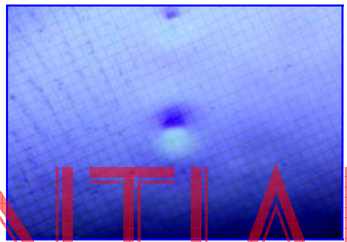
6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Cupper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Twist	Minor	Not Allowable 
Terminal Lead Broken	Minor	Not Allowable 
Terminal Lead Prober Mark	Acceptable	

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

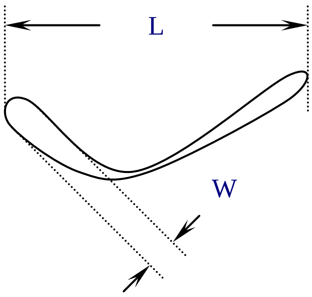
Check Item	Classification	Criteria
Terminal Lead Bent (Not Twist or Broken)	Minor	NG if any bent lead cause lead shorting. 
	Minor	NG for horizontally bent lead more than 50% of its width. 
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

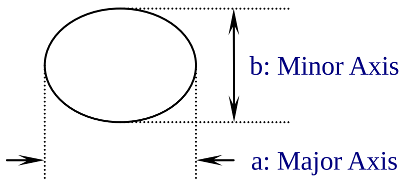
6.3.2 Cosmetic Check (Display Off) in Active Area

Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	W ≤ 0.1 Ignore W > 0.1, L ≤ 2 n ≤ 1 L > 2 n = 0
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 <Φ ≤ 0.25 n ≤ 1 0.25 <Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 ➔ Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

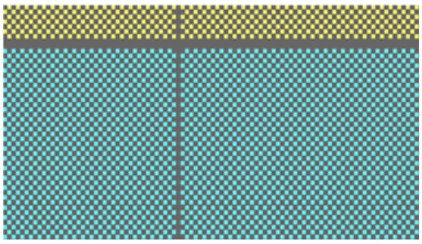
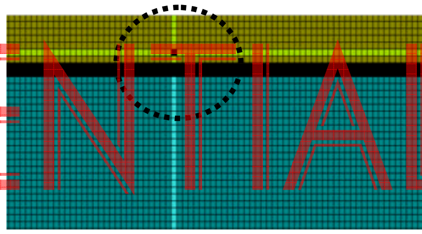
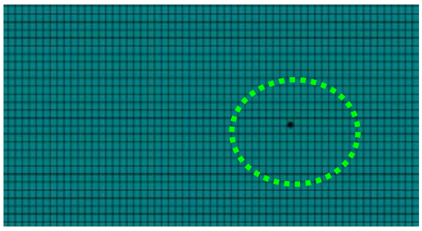
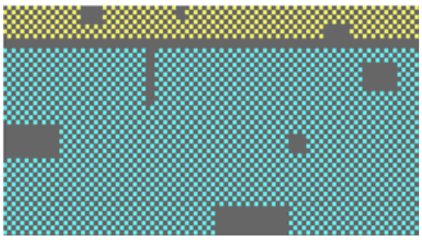
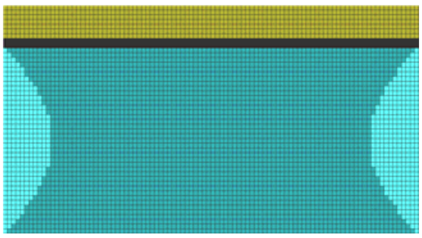
* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2

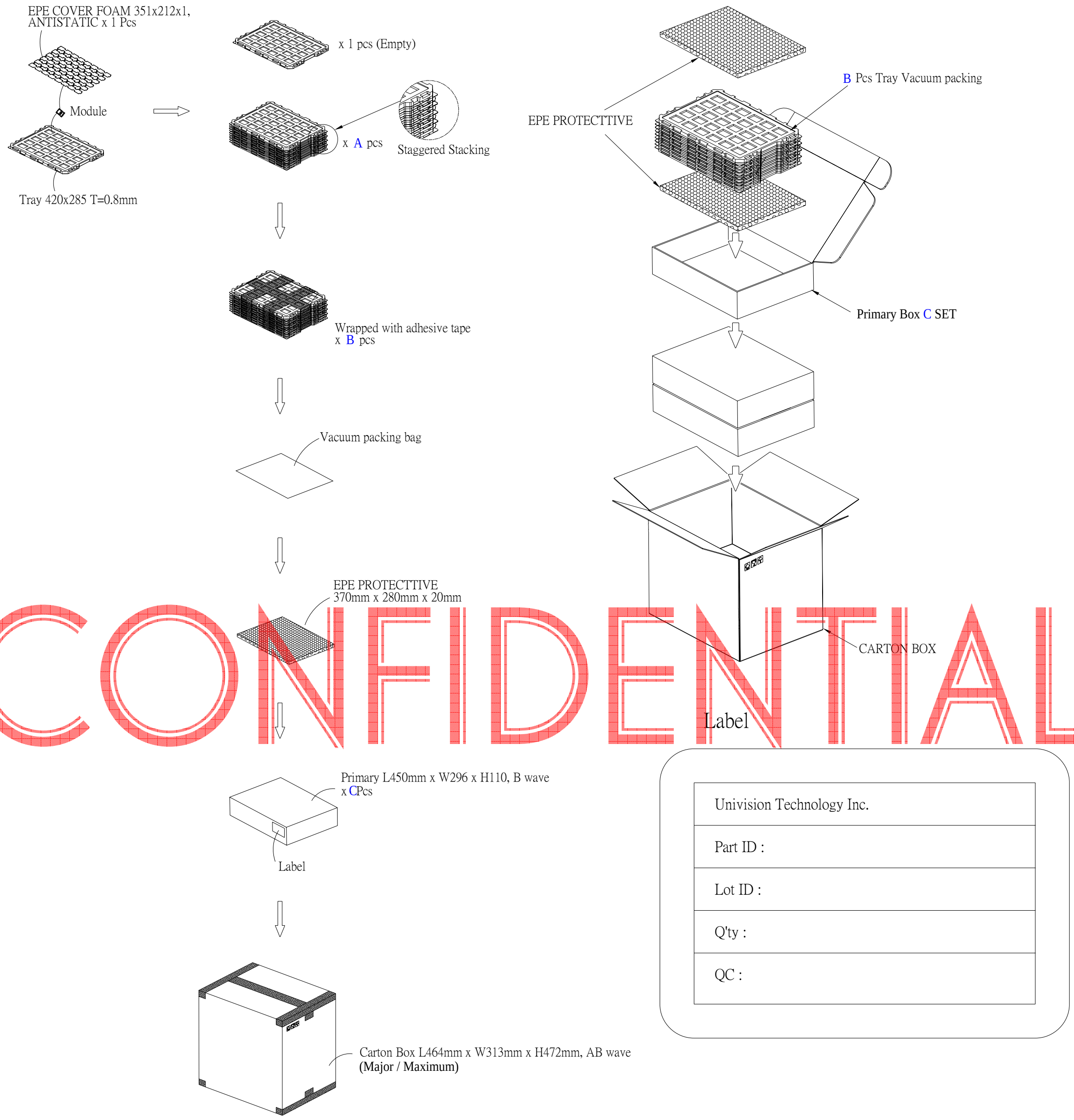




6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Flicker	Major	Not Allowable
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

7. Package Specifications



Item		Quantity	
Holding Trays	(A)	15	per Primary Box
Total Trays	(B)	16	per Primary Box (Including 1 Empty Tray)
Primary Box	(C)	1~4	per Carton (4 as Major / Maximum)

8. *Precautions When Using These OEL Display Modules*

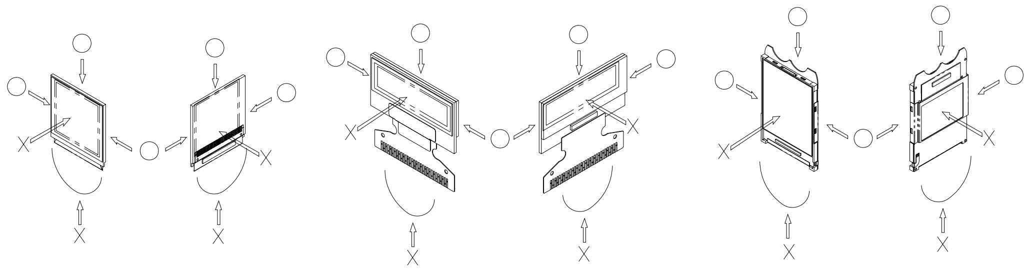
8.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.

   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents

6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.

11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).

12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

8.2 Storage Precautions

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Univision Technology Inc.)
   At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.

2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

8.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: SSD1306
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

8.4 Precautions when disposing of the OEL display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

8.5 Other Precautions

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
   Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.