

**DESIGN AND FABRICATION OF SERPENTINE-HINGED SILICON MICRO-  
MIRROR DEVICES**

BY

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# Approval Page

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## **Abstract**

Seven different actuating micro-mirror designs were created and verified via finite element analysis. Two were straight torsion beam hinge designs representative of previous work at Cal Poly; the remaining five were new designs incorporating serpentine hinges. The surface area of these mirror devices ranged from 0.5 square millimeters to 12.5 square millimeters. Geometric patterns representing the device profiles were created and used to obtain photolithographic masks. Beginning with a 400 $\mu$ m thick, 100mm diameter silicon on insulator wafer, a silicon dioxide layer was thermally grown on the surface at 1050 degrees Celsius. Positive photoresist was then spun onto the wafer at 4000 RPM for 20 seconds. Using an exposure dose of 180 millijoules per square centimeter, this photoresist was exposed through the photomask and developed, then used to transfer the geometry into the oxide. The wafer was placed in a reactive ion etcher for 5 minutes at a power throughput of 300 watts and a mixture of 300mTorr of 80% sulfur hexafluoride and 20% oxygen to create a device thickness of 10 microns. After producing the top-side geometry, additional photoresist was spun onto the bottom side of the wafer and a different photo mask was used to expose geometries for “windows” through the wafer to allow mirror rotation. Using 25% tetramethylammonium hydroxide solution, these “windows” were etched through the entire wafer substrate. A turntable arm counterweighted with a micrometer was used to apply extremely accurate forces to the devices with a resolution of 40 micronewtons. Using a laser and a position sensitive detector, the displacements corresponding to various applied forces

were measured, but electronic noise prevented effective comparison between designs.

**Keywords:** Materials Engineering, MEMS, Micromirror, Serpentine, Silicon, Silicon on Insulator, SOI, Digital Mirror Device, Digital Light Projection

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## **Introduction**

### **The Digital Micromirror**

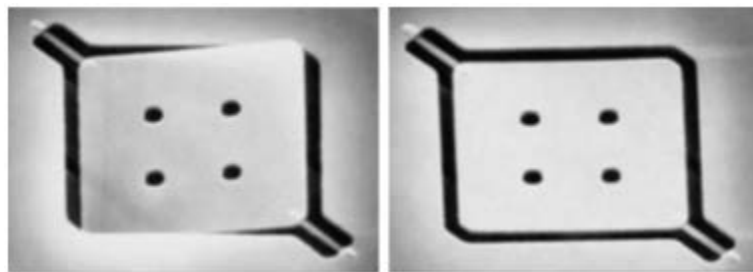
In 1987, Dr. Larry Hornbeck, a staff scientist at Texas Instruments, developed the first practical digital micromirror<sup>1</sup>. At the time, the field of Microelectromechanical Systems – or MEMS – was in its infancy, and efforts to create micromirror arrays were little more than yet another Department of Defense-funded science experiment<sup>2,3</sup>. Yet following Hornbeck's 1987 success, Texas Instruments began to aggressively pursue commercialization options for the digital micromirror device (DMD), integrating hundreds of thousands of the mirrors on a single chip. By the early 1990s, the first digital light projection (DLP) chips had reached the market and enabled the first cheap, lightweight, digital, full-color projectors. By the end of the decade, most of the initial problems with the DLP chips – particularly with overheating – had been overcome, and DLP-powered technology became affordable and commonplace. Today, almost all digital projectors contain a DLP chip. Moreover, digital micromirrors have found many other applications, including fiber optic switches and 3D imaging.

The functional heart of a modern DLP chip is an array of millions of digital micromirrors. These mirrors are “digital” because they have two states – they can be tilted completely to one side or the other depending on the applied voltage. Typically, in commercial devices, these tilt angles are about 10 degrees in either direction, and are well-defined because the mirror will usually encounter a mechanical stop<sup>4</sup>. Because of their extremely small size, digital micromirrors are also capable of switching between these “on” and “off” states extremely rapidly,



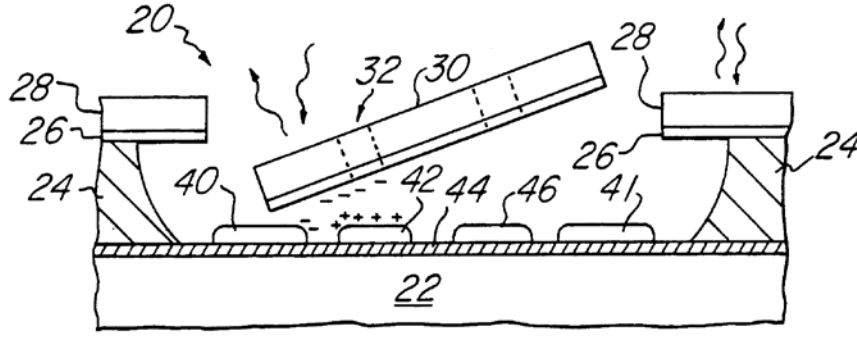
generally as much as 100,000 times a second<sup>5</sup>. This extreme switching speed is critical – although most video projection applications require switching between successive image frames only every 16 milliseconds, the micromirrors create color greyscales by switching on and off about 100 times per frame, far faster than is visible to the eye<sup>5</sup>. In this way, a mirror may flip over 6,000 times per second in typical operation. This would normally lead to concerns about fatigue of the mirror hinges, but again the small size of the mirrors produce unusual material properties, and a typical mirror may survive 5 trillion cycles – equating to over 200,000 operating hours<sup>6</sup>.

Micromirrors have changed dramatically since their invention in 1987. The initial design, as submitted in the 1988 patent, consisted of a square metal mirror fabricated on top of a silicon wafer. The mirror was suspended from microscopic metal beams to permit torsion.



**Figure 1: Primitive micromirrors: 10 degree tilt with applied voltage from hidden electrode (left), and neutral position with no voltage (right).**

The key to the success of the digital micromirror is the fact that its tilt is controlled entirely by the voltage applied; if voltage is applied on an electrode, the mirror will rotate toward it. The face of the mirror itself effectively forms a pair of parallel-plate capacitors with the two electrodes below.



**Figure 2: Cross-section of the original micromirror<sup>1</sup>.**

In Figure 2, the layer labeled 22 is the silicon wafer. 42 and 46 are the electrodes that pull the wafer down in either direction, and 40 and 41 are stops to keep the mirror from touching the electrode and discharging<sup>1</sup>.

By placing voltage on only one electrode (“42” in Figure 2), the attractive force on the mirror can be estimated with the parallel-plate capacitor equation<sup>7,8</sup>.

$$F_d = -\frac{\frac{1}{2}(\epsilon_r \epsilon_0 W L V^2)}{d^2} \quad (\text{Equation 1})$$

Here,  $\epsilon_r \epsilon_0 = 8.85 * 10^{-12} \text{ F/m}$  for air, W and L are the sides of the mirror, given in the patent as  $W = L = 19 \mu\text{m}$ , d is the separation of the mirror from the electrode, given in the patent as  $d = 2.3 \mu\text{m}$ , and V is the voltage applied. The patent suggests that a voltage of 50V is sufficient to achieve 10 degrees of rotation, so

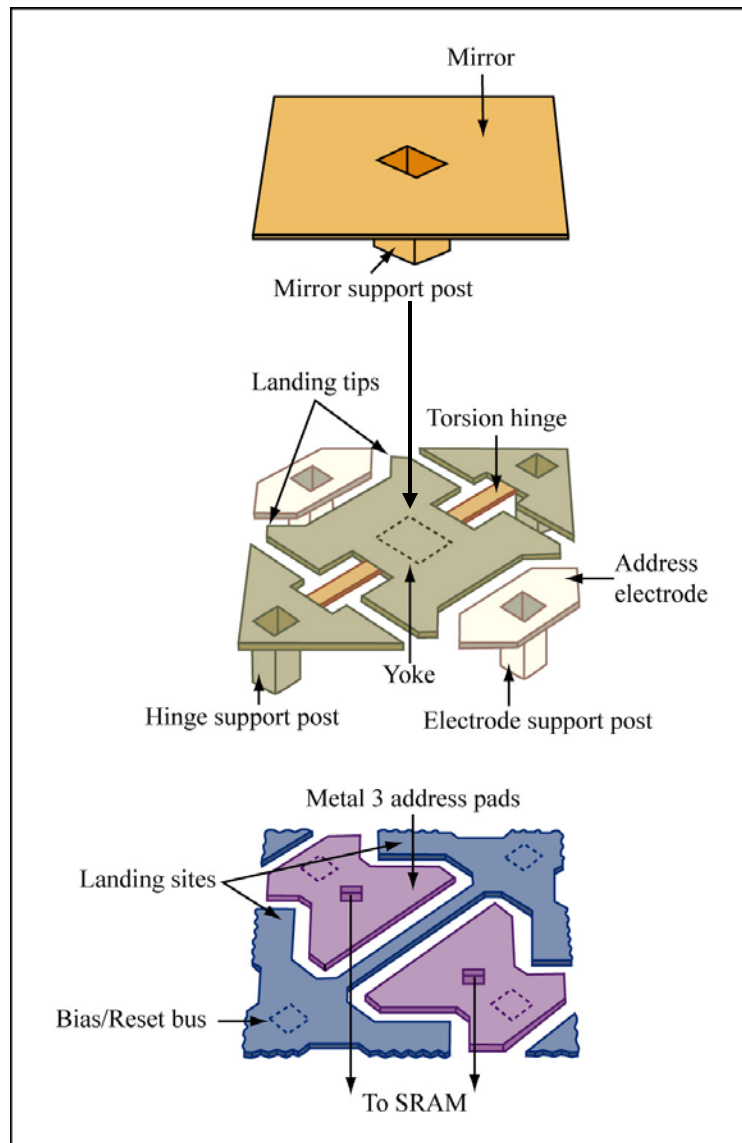
$$F_d = -\frac{\frac{1}{2} * \left(8.85 * 10^{-12} \frac{\text{F}}{\text{m}}\right) * (19 \mu\text{m})^2 * (50 \text{ V})^2}{(2.3 \mu\text{m})^2} = -0.755 \mu\text{N}$$

This implies that a single micromirror (as described in Hornbeck’s original 1988 patent) requires only  $0.755 \mu\text{N}$  of attractive force to achieve 10 degrees of rotation, and that this is achievable with a capacitive electrode. Of course, the

torsion elastic modulus, or “rotational spring constant”, of the hinges which oppose the pull of the electrode – and thus determine the degree of tilt achieved by any applied force - can be controlled by varying their thickness, length, and width. Another way to influence the torsion elastic modulus is by using a hinge geometry other than a straight beam<sup>7</sup>.

Despite the ability to tilt the mirror 10 degrees in either direction in a fraction of a second, the first digital micromirror had limitations for projection applications – particularly because the spacing between each mirror due to the hinges was large, and this contributed to gaps between projected pixels

Ultimately, the solution to this issue was the three-level design present in modern DMDs: electrodes and circuitry on the bottom layer, the hinges and capacitor plate on the second layer, and the actual mirror on the third layer, joined with a post to the second layer. This permits the mirror to completely cover the hinges.

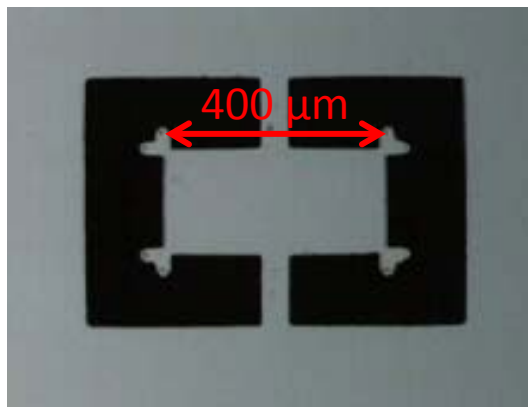


**Figure 3: Modern DMD with three-level design. (Courtesy MIT Open Courseware)**

### **Micromirrors at Cal Poly**

In 2007, graduate student Steven Meredith began exploring the visco-elastic response of aluminum layers on silicon micromirrors, and in so doing created the first micromirror structures at Cal Poly. Rather than being made entirely of aluminum, these devices were micromachined from silicon and then were covered with an aluminum layer. Furthermore, instead of resting on supports

deposited above the surface of silicon wafers, they were made by etching deep pits directly into the silicon wafers over which the thin micromirror could rotate. Many of these design decisions were made to match the capabilities of the Cal Poly Microfabrication Lab. Similar work was undertaken by graduate student Dylan Chesbro. Both Steven Meredith and Dylan Chesbro used identical straight-beam hinged mirrors, and neither reported electrostatic tilt angles much in excess of 0.3 degrees<sup>9,10</sup>. Furthermore, Dylan Chesbro reported that this 0.3 degree angle was not stable over time, which would be unacceptable for DLP applications.



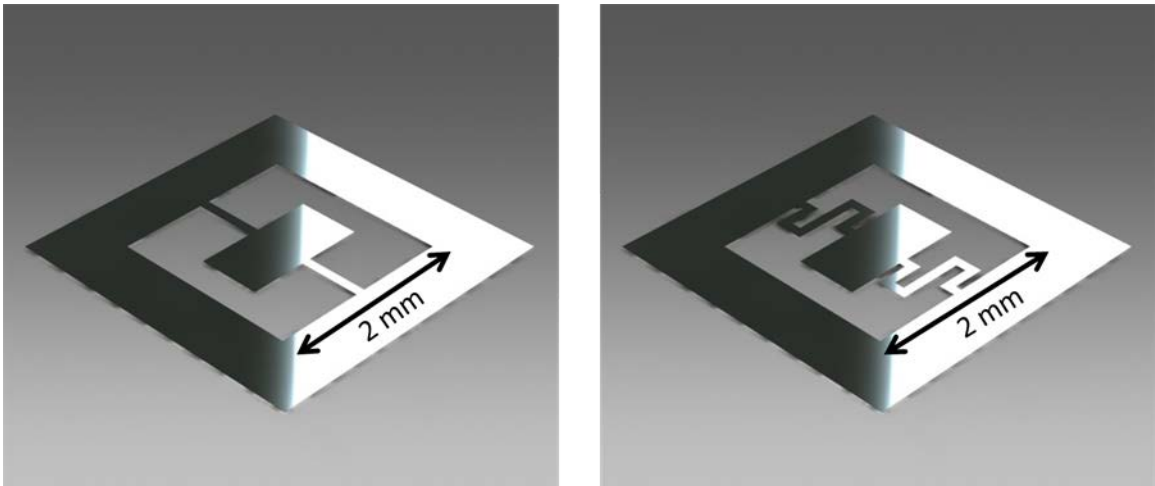
**Figure 4: Prior design of micromirrors at Cal Poly<sup>9</sup>.**

These devices had other issues besides the limited deflection angle. These difficulties included a very poorly controlled device thickness resulting from a problematic etch step, and a large amount of wasted space on each wafer resulting from a need to suction a large part of the wafer that would otherwise have been covered with 10-micron thick device membranes.

## Motivations and Constraints

In order to address the issues encountered in the past with Cal Poly micromirrors, a number of very significant changes were made to the device fabrication process. The goals of these changes included fabricating devices capable of 10 degree tilt, ensuring a well-defined device thickness of 10 microns, and utilizing the full surface of the silicon wafer to create devices.

The most significant change made in order to address the issue of limited tilt was the introduction of serpentine hinge structures. A serpentine hinge performs the same function as a straight torsion beam hinge, but will have a much lower torsion elastic modulus for the same hinge length<sup>7</sup>.

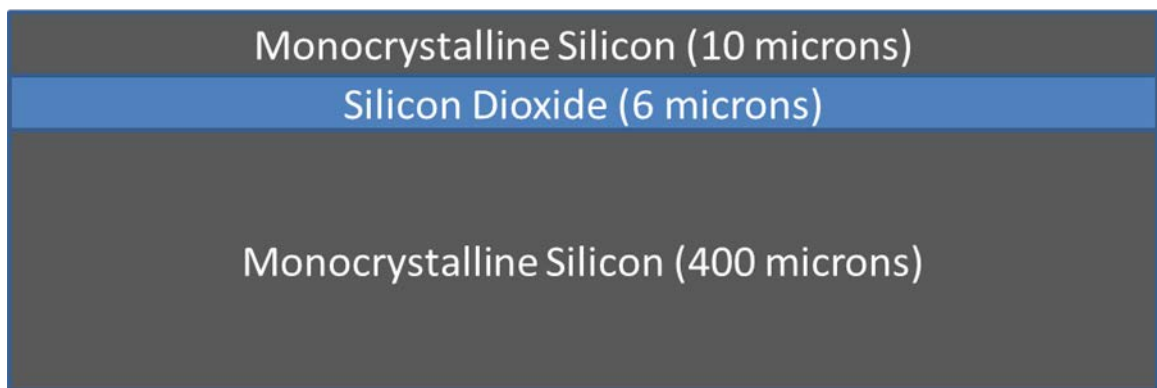


**Figure 5: A straight-beam hinge CAD render (left) and serpentine-hinge CAD render (right).**

Although these serpentine hinge structures promise very significant tilt even with 10 microns of device thickness, serpentine hinge structures increase the potential for the phenomenon of “pistoning”, where actuation of the micromirror can cause undesired oscillation out of the plane of the silicon mirror<sup>7</sup>. In commercial mirrors, this “pistoning” is not an issue because the mirror snaps

down onto mechanical stops that prevent any oscillations and define the “on”-state tilt angle, but without the use of these stops, the “pistoning” could become a concern.

The most significant change to address the poorly controlled device thickness was the use of silicon on insulator (SOI) wafers. These SOI wafers have an embedded oxide layer 10 microns below the top surface, and 400 microns above the bottom surface; as a result, any etch operation started from the top will be halted by a silicon dioxide layer after exactly 10 microns of etch, and any etch operation started from the bottom will be halted after 400 microns of etch, preventing it from cutting into the thickness of the 10 micron devices.



**Figure 6: Cross-section of specific SOI wafers used for processing.**

The use of SOI wafers, while a convenient method to guarantee a controlled thickness for the devices, is extremely expensive, at a cost of approximately \$180 per wafer. Although this cost was accepted with the understanding that no alternative approach would be as effective, the expense made it even more imperative that the entire surface of the wafer be useful for devices, unlike the previous device fabrication process that did not use most of the center.

Ultimately, standardizing the thickness of the devices permits direct comparison of the mechanical properties – particularly the torsion elastic modulus – of one fabricated device to another. As a result, the use of an SOI wafer made it possible to make direct comparisons between straight-beam and serpentine-hinged devices, as well as devices of different hinge width and overall size.

The objectives were therefore clear: to design several new devices utilizing both straight-beam and serpentine hinges, of various hinge width and overall size; to design a workable process to create the devices as designed; to use the new process to create functional devices; and to characterize the mechanical behavior of these devices in order to study the impact of hinge type, hinge width, and overall size on performance.

Furthermore, the process had to address a number of practical constraints.

Manufacturability is a constant constraint; Dylan Chesbro reported a wafer scrap rate in excess of 75% in his thesis<sup>10</sup>. A wafer scrap rate this high is a drain on funds and resources, and represents an enormously larger time investment to create a functional device wafer. Anything that will decrease the difficulty of manufacture or increase the yield per wafer is of enormous benefit. Furthermore, if processes are not available in the Cal Poly Microfabrication Lab, they cannot be used to produce devices, no matter how effective they might otherwise be.

Economic concerns – particularly with regard to the expense of the wafer and the materials required to process it – were the other major constraint. For example, there are several methods of silicon etching available in the Microfabrication Lab. Reactive Ion Etching through a silicon wafer is faster, more controlled, and more



anisotropic than wet etching through the wafer with tetramethyl ammonium hydroxide (TMAH) – but it is also vastly more expensive. Decisions to use TMAH in the process at all were therefore entirely cost-conscious.

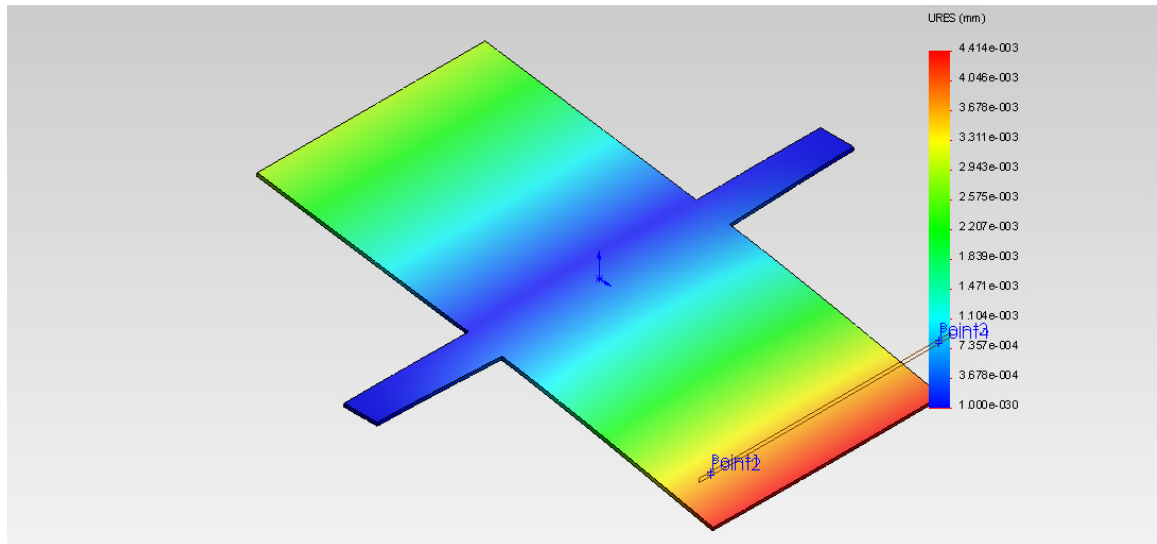
Once the objectives and constraints of the project were clear, the project roadmap was also clear: the complete project would involve design not only of the micromirror devices, but also of the process used to create them. Once the process steps were determined, process engineering would be necessary in order to find the correct parameters required to create the devices. Finally, the devices were to be characterized by building an appropriate test apparatus and then using it to obtain mechanical data.

## **Design**

### **Mechanical Design of Micromirror Devices**

In order to enable more informed design of the micromirror devices, Finite Element Analysis (FEA) software was employed to study their mechanical response to applied force. Using the COSMOSWorks FEA extension to SolidWorks, several iterations of designs featuring different beam widths, lengths, and mirror sizes were simulated to judge their relative ability to tilt a sufficient amount – specifically 10 degrees. The applied force used to create a response angle in the FEA package was nominally 100 micronewtons, as a similar force was reported in Steve Meredith's thesis during mirror actuation<sup>9</sup>. Although actual deflection angles for serpentine designs were significantly higher than for straight beam designs, the limitations of the COSMOSWorks FEA software – particularly the assumption of isotropy for single-crystalline silicon and

mesh sizes that are too large for a small device like a micromirror – meant that deflection reported by the software was more useful for design purposes than for characterization.

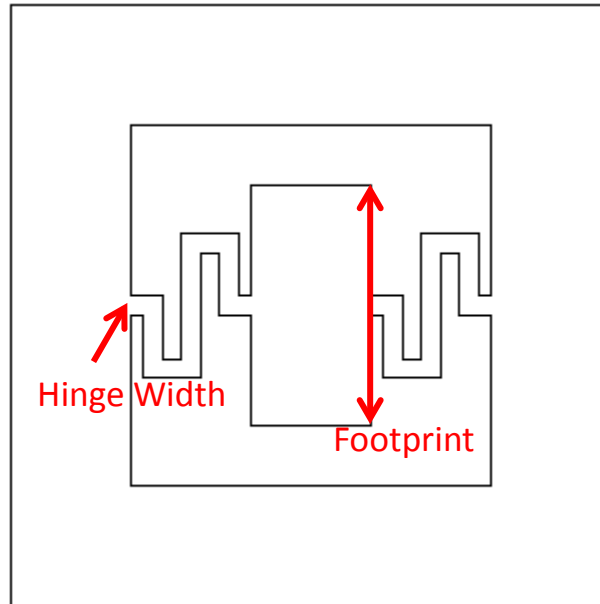


**Figure 7: FEA of straight-beam micromirror**

Eventually, one serpentine-hinge design was settled upon that appeared capable of achieving the desired tilt angle while also surviving any harsh processing steps. Because the overall objective was to study the relative efficacy of straight hinges and serpentine hinges, the same design footprint was used for both serpentine and straight-beam micromirrors. The final result of the modeling was seven devices of varying hinge type, hinge width, and mirror size, but with a common footprint, hinge length, and device thickness.

**Table I: Matrix of Fabricated Micromirror Dimensions**

Design #	Footprint	Hinge Type	Hinge Width
1	1 mm	Serpentine	80 $\mu\text{m}$
2	2 mm	Beam	160 $\mu\text{m}$
3	2 mm	Serpentine	160 $\mu\text{m}$
4	2 mm	Beam	240 $\mu\text{m}$
5	2 mm	Serpentine	240 $\mu\text{m}$
6	5 mm	Serpentine	400 $\mu\text{m}$
7	5 mm	Serpentine	600 $\mu\text{m}$



**Figure 8: CAD Top View of Final Device Design #2.**

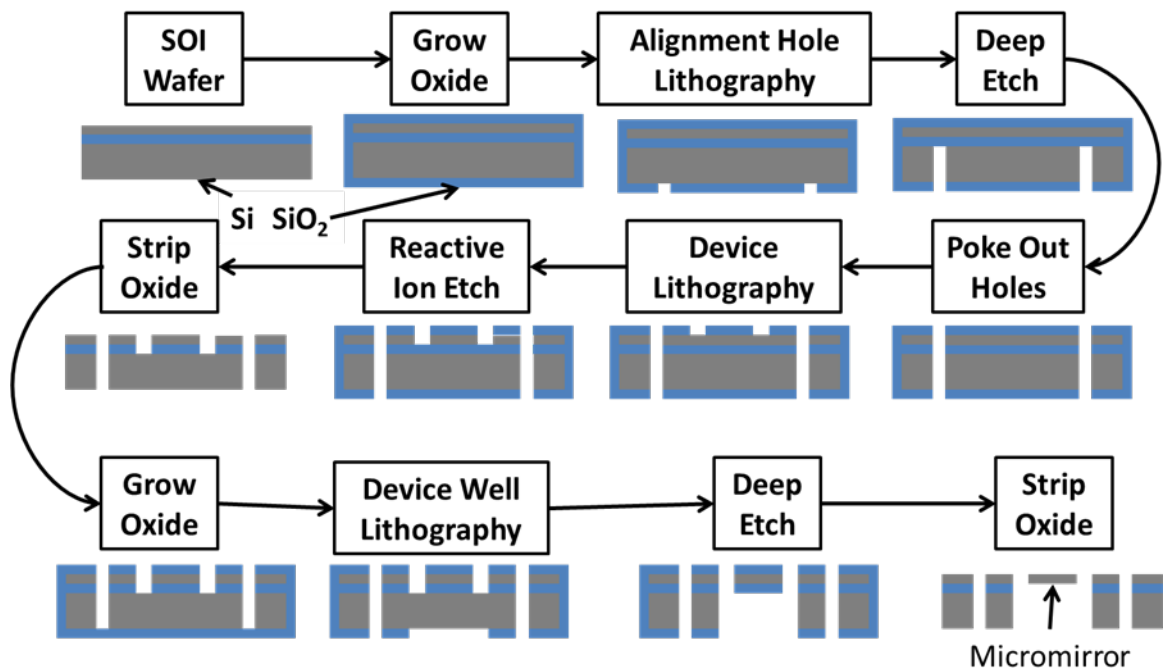
It should be noted that all of these devices are extremely large in comparison to previous micromirrors. This was a conscious decision made for two reasons. The first was simple: larger devices are easier to fabricate. The second was to make them easier to test: although small sizes are beneficial for electrostatically actuated micromirrors, electrostatic actuation makes the applied force very

difficult to determine experimentally and therefore makes comparisons between different designs troublesome. In light of this, these mirrors were designed to be actuated mechanically, not electrostatically, and their size reflects this. Future serpentine-hinged devices may have mirror sizes significantly smaller than one millimeter.

### **Overall Process Design**

The fabrication process used by previous students, although similar to the final process used to create serpentine devices, was unsuitable because it used a vacuum chuck to suction the center of the device wafer after creating membranes 10 microns thick. In the past, the entire center of the wafer was free of devices, permitting this to be accomplished without shattering the membranes. However, because of the expense of SOI wafers, it was desirable to use the entire surface area of the wafer, and so the process had to be changed in order to avoid needing to suction the center of the wafer after creating devices.

The process step that required the suction was photoresist spin coating, where a photoactive polymer solution is coated onto the wafer. This photoresist is part of photolithography and is critical for creating geometries on the wafer; therefore, the last photolithography step was changed to create the geometries for the device wells, creating the final devices rather than silicon membranes.



**Figure 9: General overview of processing steps to create micromirror devices.**

Figure 9 illustrates a simplified process flow for creating devices. The cross-sections are not to scale, and show only one device between the two alignment holes rather than dozens. However, the two general types of process steps are shown: the etch steps, where the portions of the wafer not covered with silicon dioxide are removed, and the patterning steps, in which oxide is grown or shaped by lithography to create an etch mask. The oxide growth was accomplished by placing the wafers in a furnace, and the lithography was accomplished first by spin-coating the wafers with photoactive photoresist, then exposing certain portions of the photoresist, determined by the photomask, to ultraviolet light. This caused a chemical reaction in the exposed portions of photoresist that rendered it soluble, so it could be removed with a developing agent. The exposed oxide regions could then be removed with hydrofluoric acid. The etch steps, reactive

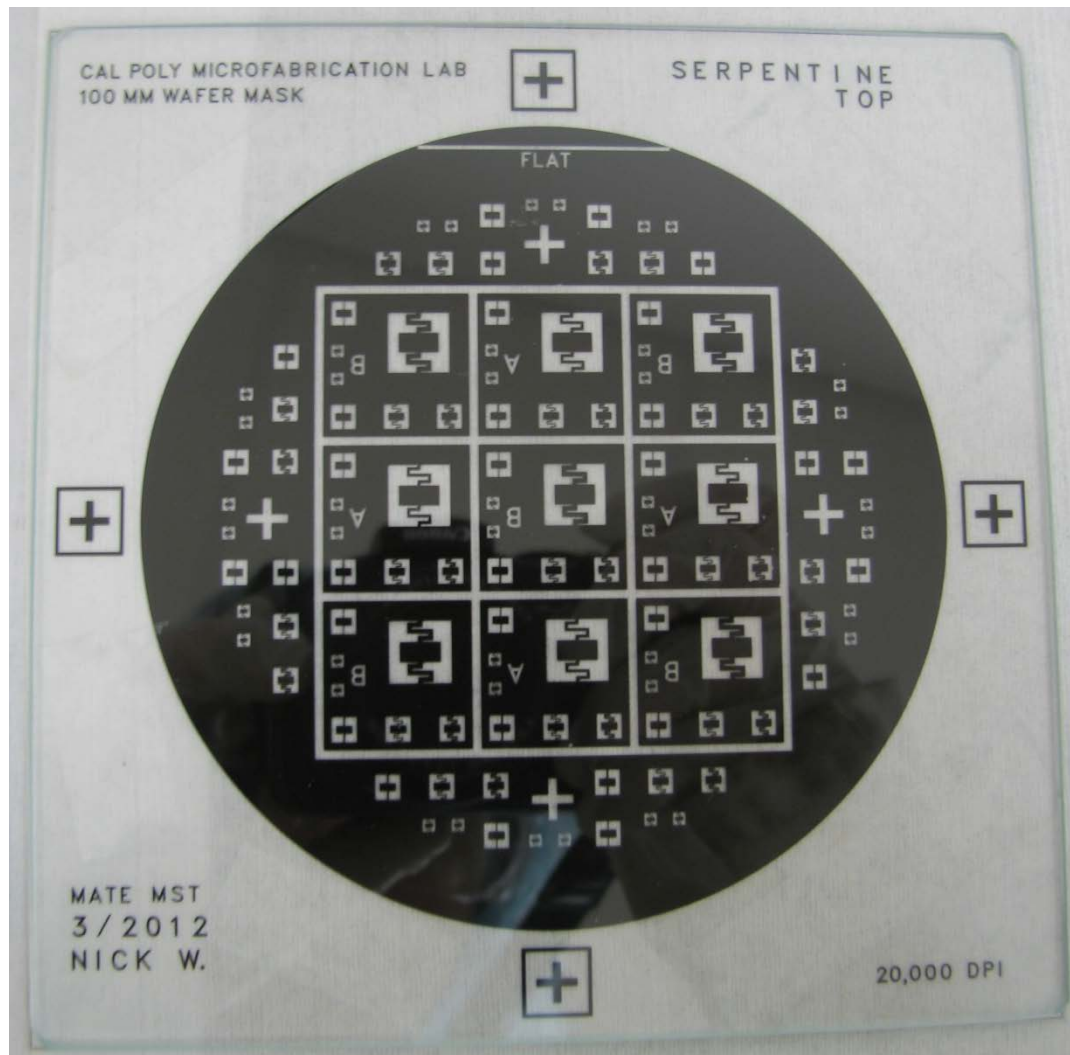
ion etching (RIE) and deep etching, were similar in their removal roles, except RIE produced much better uniformity and anisotropy, but was more expensive than the TMAH deep etch. Because of the expense, TMAH was used for the bulk etch through the 400 microns of silicon wafer, and the RIE was limited to creating the actual device geometries.

Beyond the fact that the device geometries were created on the top of the wafer prior to creating the pits for them to be suspended over, it is worth noting that an entire deep etch step was necessary simply to create alignment holes. The topside photomask could not be used without first creating alignment holes, since alignment would have then been impossible to the bottom photomask. This was previously not the case: the device wells and alignment holes were created simultaneously during the first etch step.

### **Design and Creation of Micromirror Photolithography Masks**

Using the geometries of the seven devices, a top-side photomask was created to enable lithographic patterning onto the wafer and ultimately fabrication of the micromirror devices. At the time of the creation of the photomask, it was believed that testing would be possible using an existing microhardness tester. This microhardness tester was capable of extremely fine force resolution, but required test devices to be mounted onto a SEM stage. The square outlines on the top mask delineate squares that would fit onto a large SEM stage, and would be used to help guide cutting of the wafer into test coupons. Unfortunately this microhardness tester was not made available, and so these test coupons are of

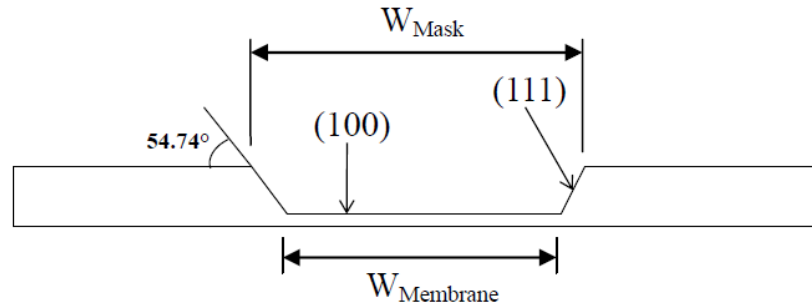
no significance; however, all test coupons include design numbers 1-5, but the coupons labeled “A” feature design number 6, while the coupons labeled “B” feature design number 7 instead (note that “A” and “B” are inverted on the mask). An additional feature on the photomask was plus-sign shaped alignment marks intended to enable accurate alignment to the mask used for the bottom side of the wafer. These alignment marks were made very large (5 mm) because they would eventually need to become actual holes passing through the wafer. After the design was completed, the plastic photomask was printed off-campus using a very high-resolution printer (20,000 DPI) and attached to a glass plate for use in a lithographic aligner.



**Figure 10: Topside photomask used to create devices attached to glass plate.**

The bottom side of the wafer required an additional photomask in order to create deep through-hole “wells” that the micromirror devices could be suspended above and rotate into. However, because these holes were to be fabricated using deep tetramethyl ammonium hydroxide (TMAH) through-hole etching, it was necessary to compensate for the anisotropy of the etch so that the profile of the holes would match the profile of the devices once the etch reached the top side of the wafer.

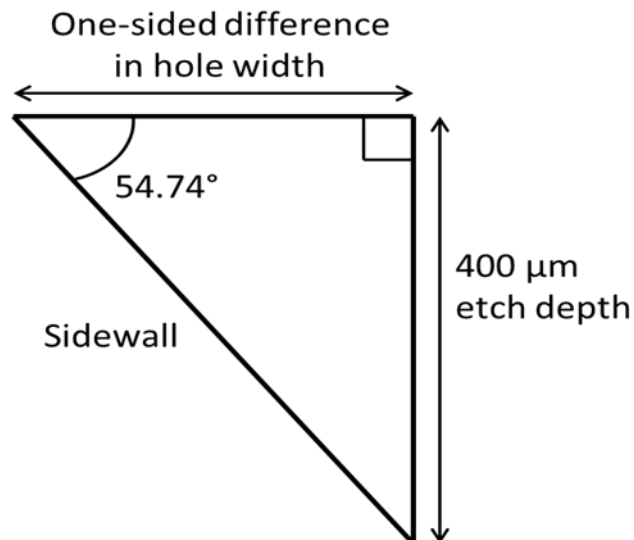




**Figure 11: TMAH etches the different planes of monocrystalline silicon wafers at different rates, producing a 54.74 degree sidewall slope.**

The (100) plane of silicon is attacked much more readily by TMAH than the (111) plane, which has atomic smoothness and closer atomic packing<sup>11,12</sup>. The result of this etch-rate mismatch is flat, sloping walls through the wafer. The slope of these walls is a characteristic 54.74 degrees.

Because the depth of etch is approximately 400 microns (to the oxide etch stop of the SOI wafer), the difference in size of the resulting topside hole was approximated.

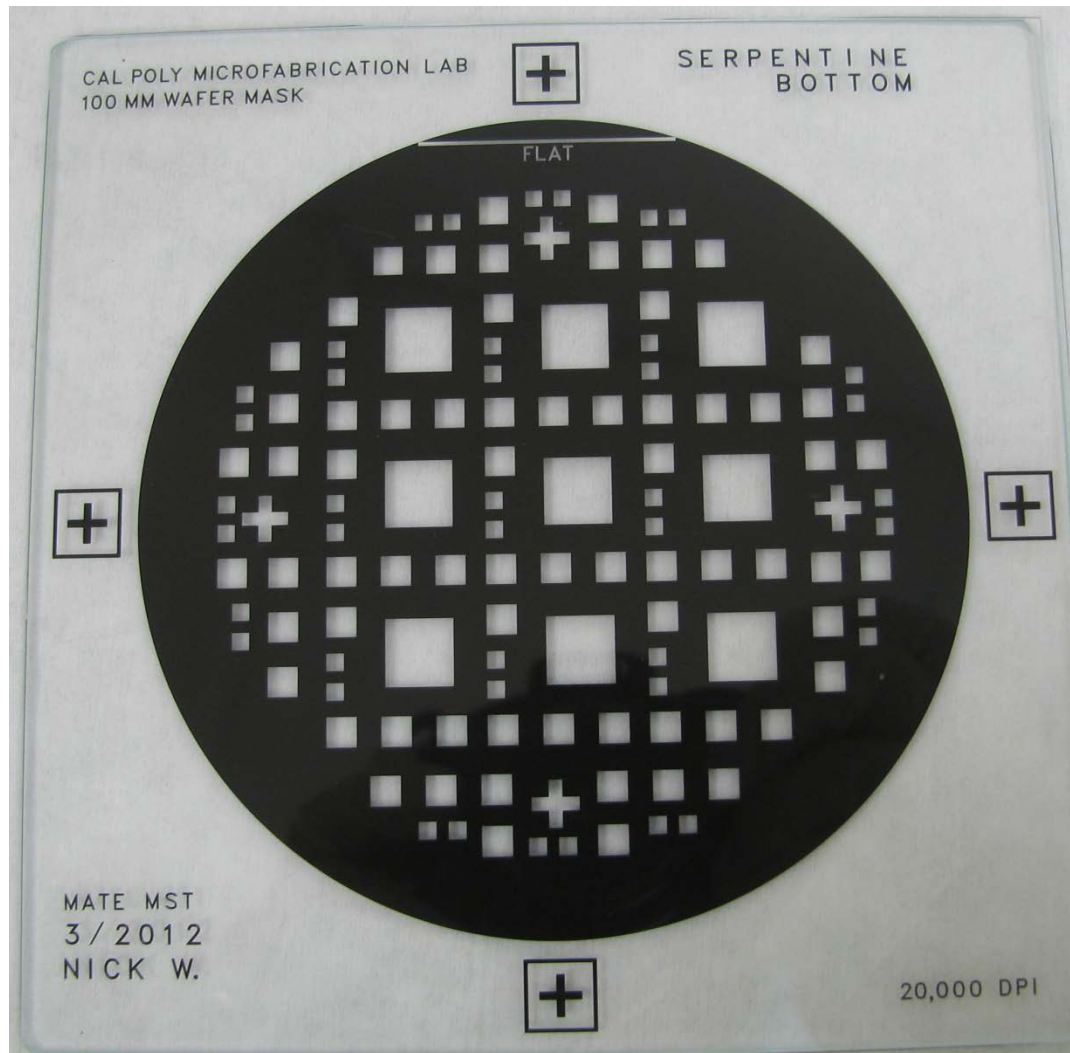


**Figure 12: Geometry of etch compensation (not to scale).**

Based on this geometry, the one-sided difference in hole width is

$$d = 400 \mu\text{m} * \tan(54.74^\circ) \quad (\text{Equation 2})$$

This provides a one-sided difference of 566  $\mu\text{m}$ . By expanding each side of the top mask windows and alignment marks by this amount, the bottom-side mask was created.



**Figure 13: Bottom photomask used to create device wells attached to glass plate.**

With the photomasks complete, actual fabrication of the devices could be attempted.

## Processing

### Silicon Dioxide Growth

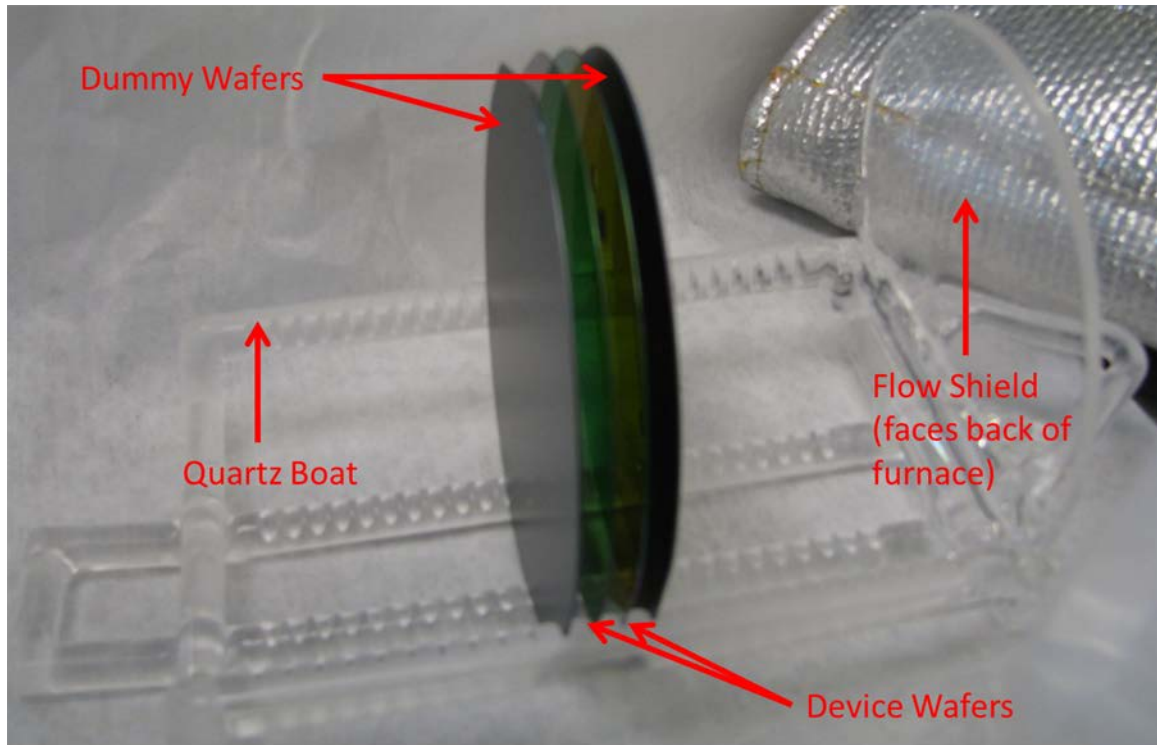
Although silicon oxide layers are not a part of the final micromirror device, they are instrumental as etch masks that define the actual geometries of the devices.

One of the benefits of using silicon as a substrate is its stable, unreactive, thermally grown oxide. However, temperatures in excess of 900 degrees Celsius are required to produce oxide layers of any appreciable thickness. A tube furnace with built-in gas flow control and capable of maximum temperatures potentially as high as 1400 Celsius was used for oxide growth.



**Figure 14: Thermal oxidation furnace in Cal Poly Microfabrication Lab.**

When the furnace was hot, wafers were placed slowly into the tube (approximately 1 centimeter per second) to avoid thermal warping from rapid temperature change. The device wafers themselves were loaded into a quartz boat and surrounded with a dummy wafer on either side. These dummy wafers served to deflect the turbulent flow of gas through the furnace away from the device wafers and ensure an even oxide layer.

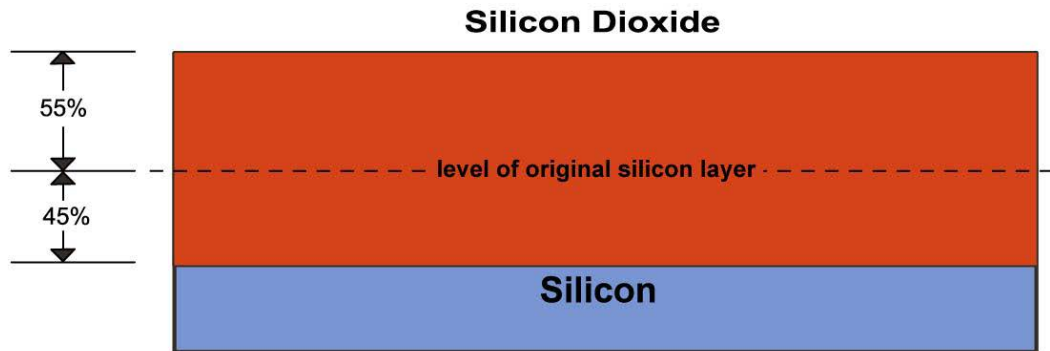


**Figure 15: Oxidation boat with wafers loaded.**

When the wafers were loaded into the furnace and the desired temperature was reached, the gas flowing into the furnace was changed from pure nitrogen to pure oxygen combined with water vapor. This allowed the oxidation process to begin. Once the desired time had elapsed, the flow gas was switched back to nitrogen to purge the furnace atmosphere and stop the oxide growth.

Part of the challenge with the oxidation furnace was determining what thickness of oxide was appropriate, and which process parameters would create an oxide of that thickness. It was desirable to use the thinnest oxide permissible, because each time an oxide is grown in a furnace, some of the silicon layer that it grew upon is consumed: typically, for every micron of oxide that is created, 450 nanometers of silicon are lost<sup>13</sup>. Since the SOI wafers being used had a well-

defined 10 micron device layer before oxidation, it was of interest to restrict oxidation as much as possible, so that the device layer did not become significantly smaller than 10 microns.



**Figure 16: Relationship between oxide growth and consumption of the silicon substrate.**

Because the only role of the silicon dioxide layer was to protect areas of silicon from etchants, the required thickness of oxide was determined entirely by the relative etch rate of silicon to silicon dioxide, known as the selectivity. The selectivity was used to ensure that the etch process would complete before the oxide layer was etched away.

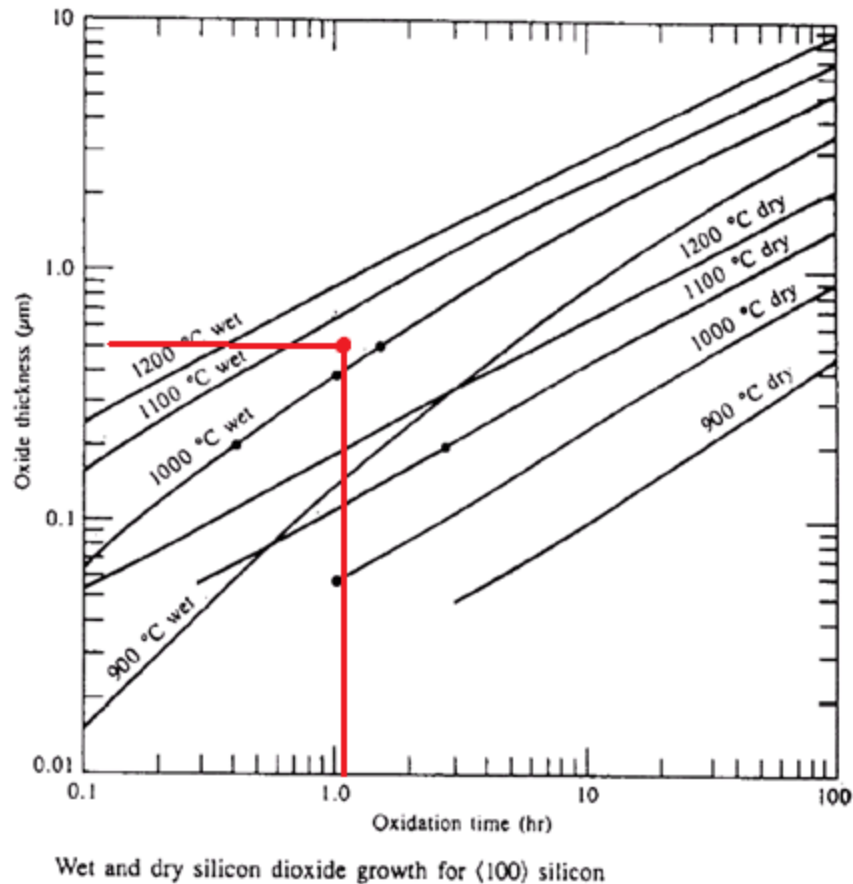
Only two etch processes were used:  $\text{SF}_6/\text{O}_2$  reactive ion etching (RIE), and tetramethyl ammonium hydroxide (TMAH) deep etch. The selectivity of silicon to silicon dioxide of the RIE etch was approximately 100:1, and the selectivity of silicon to silicon dioxide of the TMAH deep etch was in excess of 1000:1<sup>14,15</sup>.

The depth of the RIE etch was 10 microns. A selectivity of 100:1 implies that the required oxide thickness was 0.1 micron, or 1000 angstroms. Similarly, the depth of the TMAH etch was 400 microns, so a selectivity of 1000:1 implies a required

oxide thickness of 0.4 microns, or 4000 angstroms. In order to cover both situations, the target oxide thickness was arbitrarily set to be 5000 angstroms. In order to create an oxide with the desired 5000 angstroms of thickness, the Deal-Grove model, a theoretical framework relating the thickness of oxide to the temperature, process time, and presence of water vapor in the atmosphere, was used. The equation models the two processes which create oxide on a wafer: surface interaction and diffusion-limited transport. The relationship is<sup>16</sup>

$$t = \frac{X_o^2}{B} + \frac{X_o}{\frac{B}{A}} \quad (\text{Equation 3})$$

Here, t is the required time to create an oxide of thickness  $X_o$ . B and A are rate constants associated with the temperature of the furnace and the presence of water vapor. Since the temperature most commonly used in the Microfabrication Lab is 1050 degrees Celsius, and the presence of water vapor significantly speeds oxide growth, the exact time required can be computed. For the case of 5000 angstroms and 1050 degrees Celsius, the required time is 1 hour 7 minutes. This is demonstrated by the curves in Figure 17.

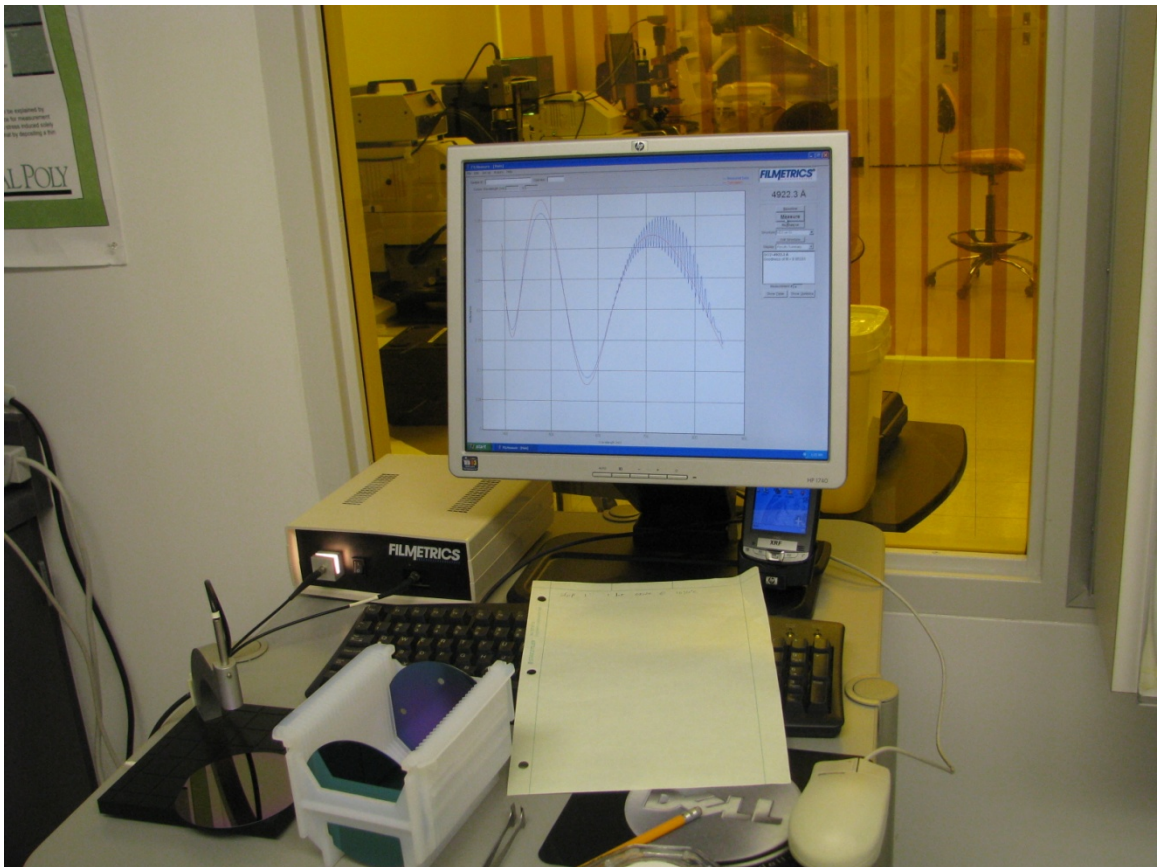


**Figure 17: Deal-Grove curves. The required process time for a 5000 angstrom oxide using wet oxidation at 1050°C is approximately one hour.**

Once a wafer was run in the furnace for 1 hour and 7 minutes at 1050 degrees Celsius, the final step was to verify that the oxide thickness was approximately 5000 angstroms. Oxide thickness measurements accurate to within a few angstroms could be obtained with a Filmetrics reflectometer, which uses spectral reflectance to mathematically determine the thickness of the oxide. Typically, a thin film will have strong thin-film interference at certain wavelengths and weak interference at others, depending on the thickness of the film. By analyzing the wavelength-based response, the Filmetrics device could determine the oxide thickness by comparison with a mathematical model. Generally, wafers had a



measured oxide thickness within a range of a few hundred angstroms from the target of 5000 angstroms.



**Figure 18: Filmetrics device measuring an oxide thickness of 4922 Å on an SOI wafer.**

### **Photolithography**

Photolithography was used to shape the oxide layer. The shaping of the oxide layer ultimately allowed transfer of the oxide pattern into the silicon substrate using etch processes to remove silicon not protected by an oxide layer. Several unit steps are involved in the photolithography used to shape the oxide. In order of execution, these steps are: the deposition and spin-coating of photoresist,



exposure of the photoresist, development of the photoresist, etching of the oxide, and finally the removal of the photoresist.

Photoresist spin-coating is a process that has been well-established by previous projects in the Microfabrication Lab. There are two types of photoresist for processing purposes: positive photoresist and negative photoresist. Positive photoresist becomes soluble in developing solution when exposed to light.

Negative photoresist becomes insoluble when exposed. Because positive resist is easier to remove from the surface of the wafer after photolithography, it was selected for use. Consequently, the photomask was designed to expose the regions that should become soluble.

In order to spin-coat photoresist onto the wafer, approximately 2.5 mL of MicroChem MCC primer was dispensed onto the wafer, then spun for at 300 RPM for 30 seconds and 3000 RPM for 20 seconds. This caused the primer to evaporate and leave a better adhesion surface for the photoresist. Approximately 4 mL of Rohm-Haas Microposit S1813 positive photoresist was then dispensed onto the wafer, and spun using the following program.

**Table II: Photoresist Spin-Coat Program**

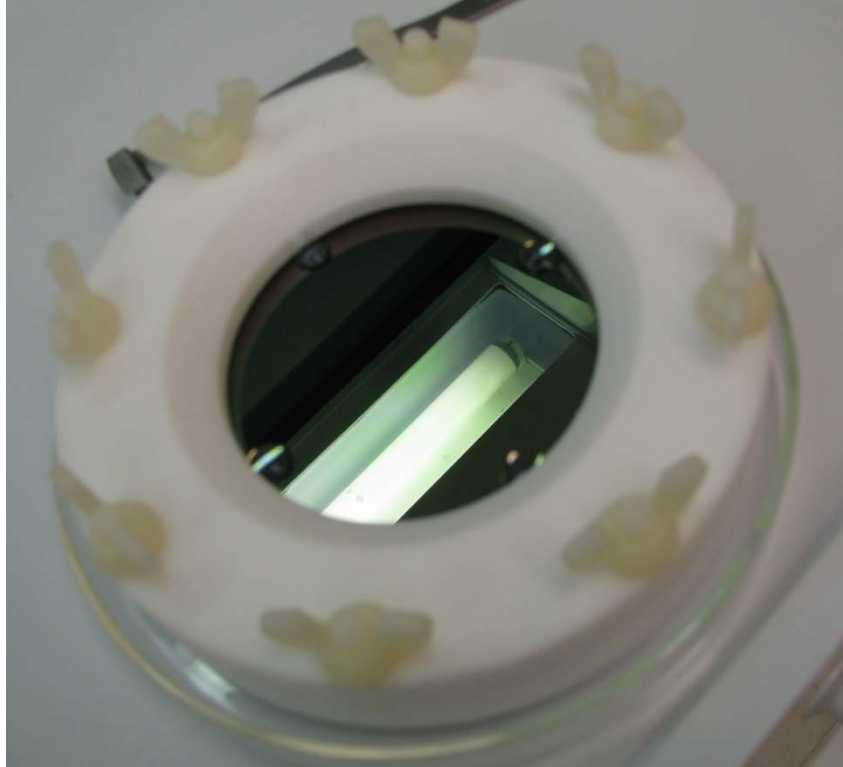
Step	Spin Speed (RPM)	Duration
1	200	20
2	500	10
3	4000	20
4	300	5

Once photoresist covered the wafer, it was soft-baked at 90°C for 60 seconds to remove excess solvent. After the soft-bake, the wafer was exposed in the aligner. In order to create the alignment marks for the first deep etch step, aluminum foil was used to cover all of the features on the bottom photomask except the

alignment marks. Because the alignment marks created this way were very large, successive lithography steps required alignment by hand rather than with the aligner microscope. This was accomplished through use of a small magnifying glass. Once the wafer was aligned and ready for exposure, the light integral was set to 4.5, corresponding to a dose time of 16.7 seconds, or 108 mJ/cm<sup>2</sup> of light energy. After being exposed, the wafer was ready for development.

In order to develop the wafer, it was submerged and agitated in Microposit CD-26 developer for 2 minutes. This removed the parts of the photoresist that had been exposed through the photomask, exposing the oxide. Before moving on to the oxide etch step, the wafer was hard-baked at 150°C for 60 seconds to ensure that it would withstand the etching. At this point, the quality and “sharpness” of the features in the photoresist were verified with an optical microscope.

In order to remove the newly exposed oxide, the wafer was submerged in buffered oxide etchant (BOE). The active chemical in BOE is hydrofluoric acid, which attacks silicon dioxide but not photoresist. Because the oxide layer was 5000 angstroms thick, and BOE has a well-established etch rate of 800 angstroms per minute, wafers were left submerged for about 7 minutes to ensure the oxide was completely removed. For those steps that required the oxide on the back side of the wafer to be left intact during the etch, the wafer was mounted in a Teflon fixture exposing only the top side of the wafer, and BOE was very carefully deposited onto the surface.



**Figure 19: Creating alignment holes in oxide with BOE and Teflon fixture.**

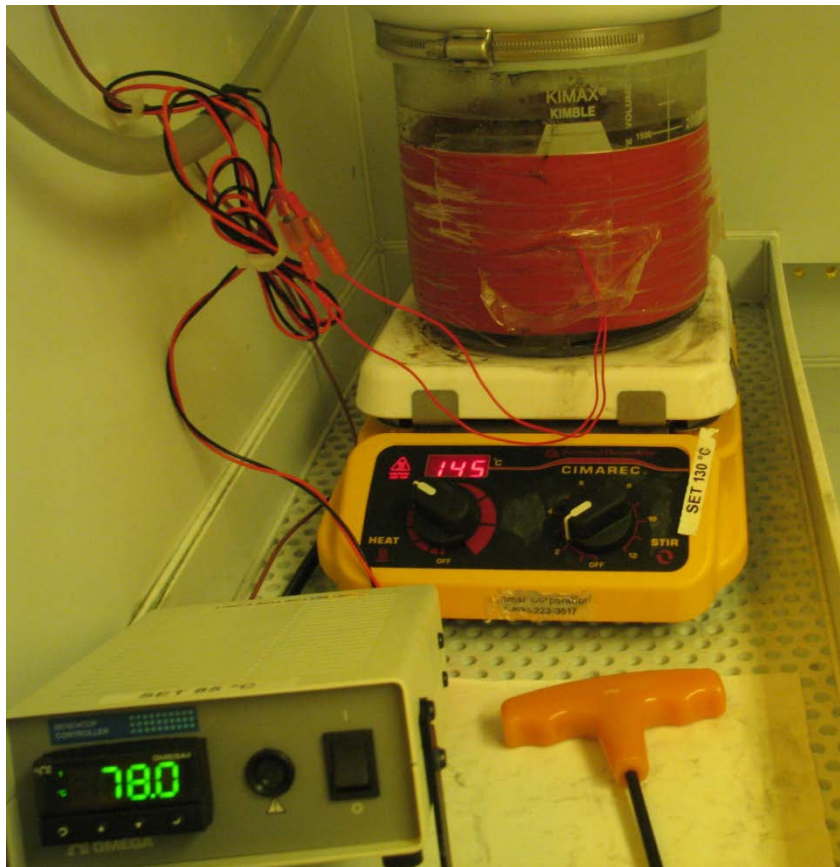
Finally, once the desired oxide pattern had been created, the wafer was submerged in Shipley photoresist stripper at 60°C for 2 minutes to ensure removal of the photoresist.

### **Deep Etch**

The deep etch step was used for two purposes: to create alignment holes which travel all the way through the wafer and enable the patterns on each side to be aligned, and to dramatically thin the silicon wafer below the device layer, enabling them to flex into the pit below.

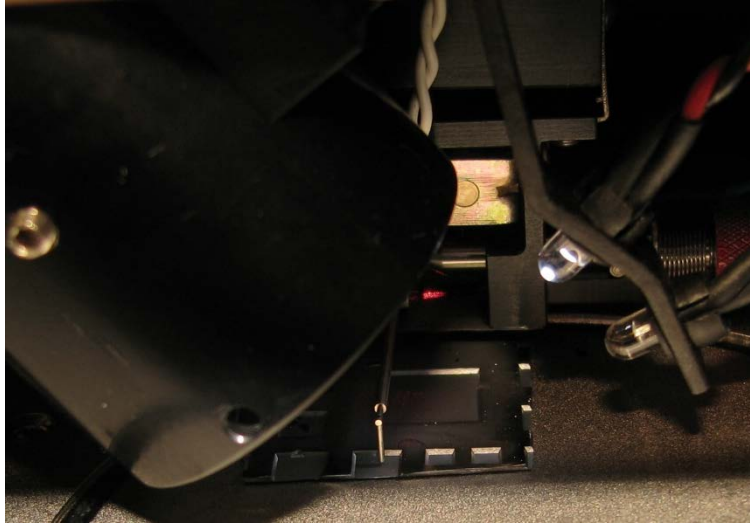
The deep etch process used 25% tetramethyl ammonium hydroxide (TMAH) solution at 85°C to remove silicon. Unfortunately, TMAH etch rates are extremely sensitive to both temperature and TMAH concentration<sup>12,14</sup>. In order to keep concentration constant, the TMAH solution was held in a reflux condenser

chamber intended to condense evaporated liquid. Furthermore, to control temperature, a coil heater was installed on the condenser chamber, and connected to an Omega temperature controller. This controller monitored temperature from a thermocouple inside the chamber and would set a duty cycle for the heater to maintain temperature at 85°C. Unfortunately, it would often permit temperature swings of as much as a few degrees Celsius.



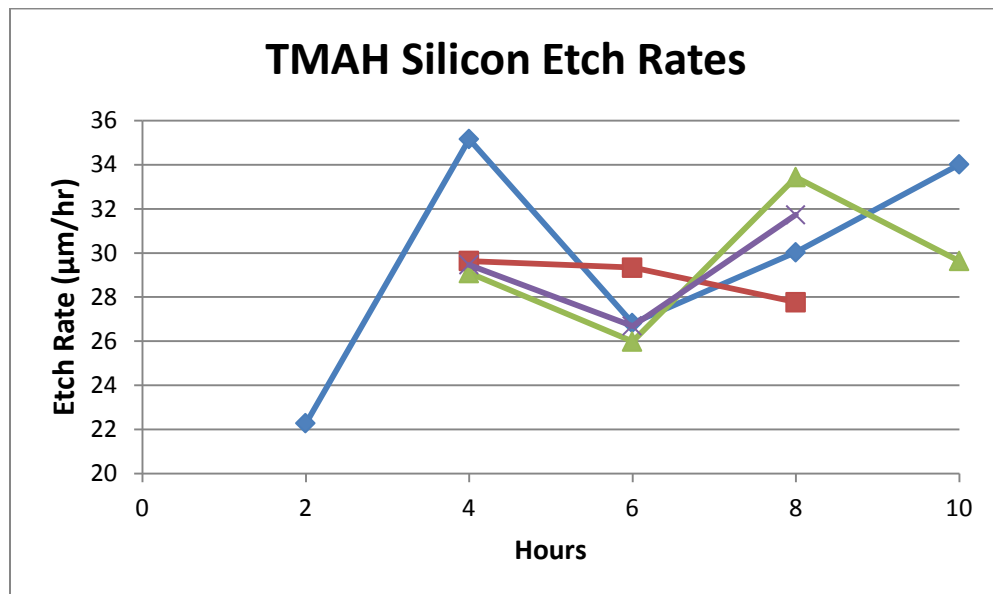
**Figure 20: Condenser chamber with coil heater warming up to 85°C.**

In order to determine etch rates for the TMAH, wafers were placed into the solution for a two hour period, then removed and placed in a profilometer. A profilometer can measure the depth of geometries on a surface by dragging a stylus along its surface.



**Figure 21: Profilometer measuring etch depth on a chunk of silicon.**

By measuring the change in depth of the exposed features for every two hours of TMAH exposure, etch rates were established for four different test wafers.



**Figure 22: Etch rate measurements of TMAH deep etch over 2 hour intervals.**

The etch rate was highly unpredictable, ranging from 22.3  $\mu\text{m/hr}$  to 35.1  $\mu\text{m/hr}$ .

This unpredictability was likely due to poor temperature control. The best method to compensate for this variation was simply to get close to the desired etch

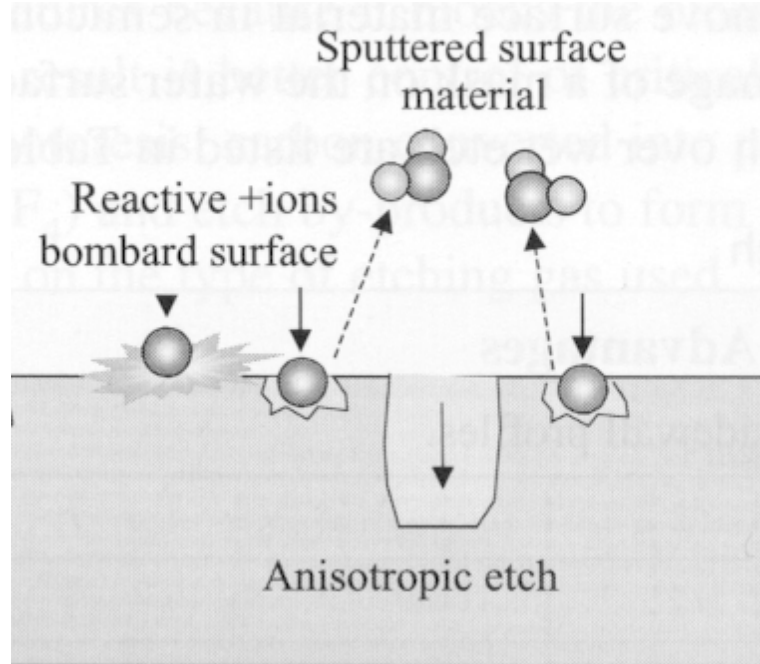
depth, and then begin making frequent measurements with the profilometer until the desired etch depth was achieved. Typical etch times to achieve 400 microns of depth were about 15 hours.

Unpredictable etch depth was not the only difficulty with the deep etch – imperfections and scratches in the oxide could lead to deep trenches over the course of 15 hours of etching. This was very harsh on the wafers, especially since two 15-hour deep etches were required to create devices, and this 30 hours of exposure to TMAH could make the wafers brittle, leading to breakage and wafer scrapping.

### **Reactive Ion Etch**

A Reactive Ion Etcher was used in order to create the device geometries. Deep etching was undesirable because it creates sloping sidewalls that would not have been appropriate for the sides of the devices, and also because it has a tendency to undercut and etch beneath oxide masks, which could have seriously interfered with the structure of the mirror hinges.

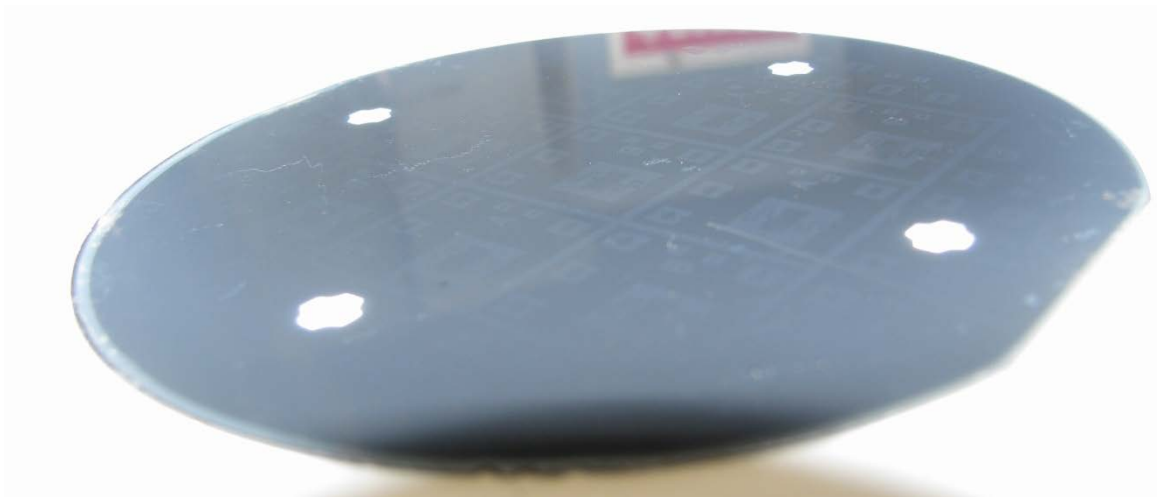
In reactive ion etching, a plasma of reactive ions is created, and then these ions are accelerated toward the charged substrate. By accelerating these ions downward, a straight etch profile is ensured. Once the ions reach the surface, they tend to react with it and remove surface material.



**Figure 23: Reactive ion etching.**

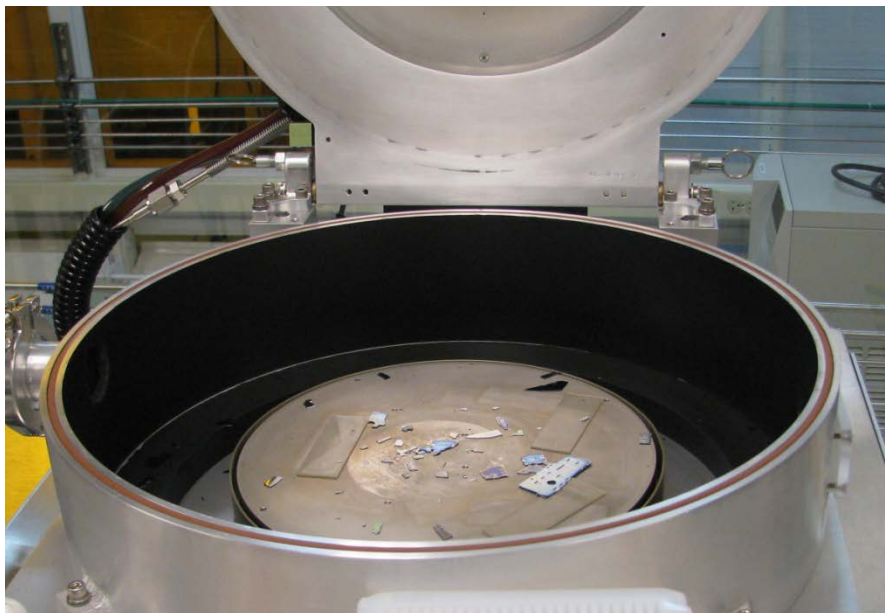
In the case of the RIE tool in the Microfabrication Lab, the process gases available for use were oxygen ( $O_2$ ) and sulfur hexafluoride ( $SF_6$ ). In the plasma, the  $SF_6$  breaks apart into sulfur and fluorine ions. The sulfur tends to combine with oxygen ions, producing  $SO_2$ , and leaving the remaining fluorine ions to react with the silicon, forming  $SF_2$  and  $SF_4$ <sup>17</sup>. These gases are vented out of the chamber.

One of the potential downsides to RIE is the sensitivity of the results to the process parameters. However, careful experimentation and control permits repeatable results. A gas mixture of 60%  $SF_6$  and 40%  $O_2$  at a power setpoint of 500 watts and pressure setpoint of 300 millitorr produced a black silicon wafer, which effectively destroyed any devices on the wafer.



**Figure 24: Black silicon wafer produced by RIE. The alignment holes and some device outlines are visible.**

Similarly, a gas mixture of 70%  $\text{SF}_6$  and 30%  $\text{O}_2$  at a power setpoint of 300 watts and pressure setpoint of 300 millitorr caused the process wafer to inexplicably explode inside the chamber. The cause for this could not be determined, but the process parameters were considered unsuitable.



**Figure 25: Wafer debris produced by RIE recipe.**



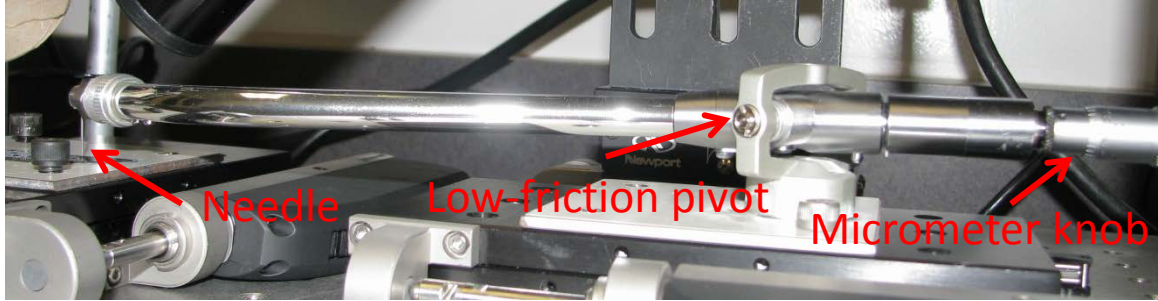
The process identified as suitable for etching purposes was a mixture of 80% SF<sub>6</sub> and 20% O<sub>2</sub> at a power setpoint of 300 watts and pressure setpoint of 300 millitorr. The etch rate measured with the profilometer for this recipe was approximately 2.2 μm/min. In order to ensure the RIE would etch through the 10 microns of topside silicon and reach the oxide etch stop, a process time of 5 minutes was used.

## **Testing**

### **Test Apparatus**

After obtaining devices, the next step was mechanical testing to characterize the device behavior and enable effective comparisons between the seven different designs. The necessary test apparatus would apply forces on the order of tens of micronewtons to an extremely small area on the edge of the micromirror. It would then need to measure either the displacement of the edge of the mirror, permitting calculation of the angle using the known mirror length, or simply measure the angular deflection directly.

After attempts to obtain a microhardness tester to use for this purpose and a number of design iterations, the final design for a micro-force applicator was a turntable arm with an extremely fine needle mounted on one end, and a depth micrometer mounted on the other.

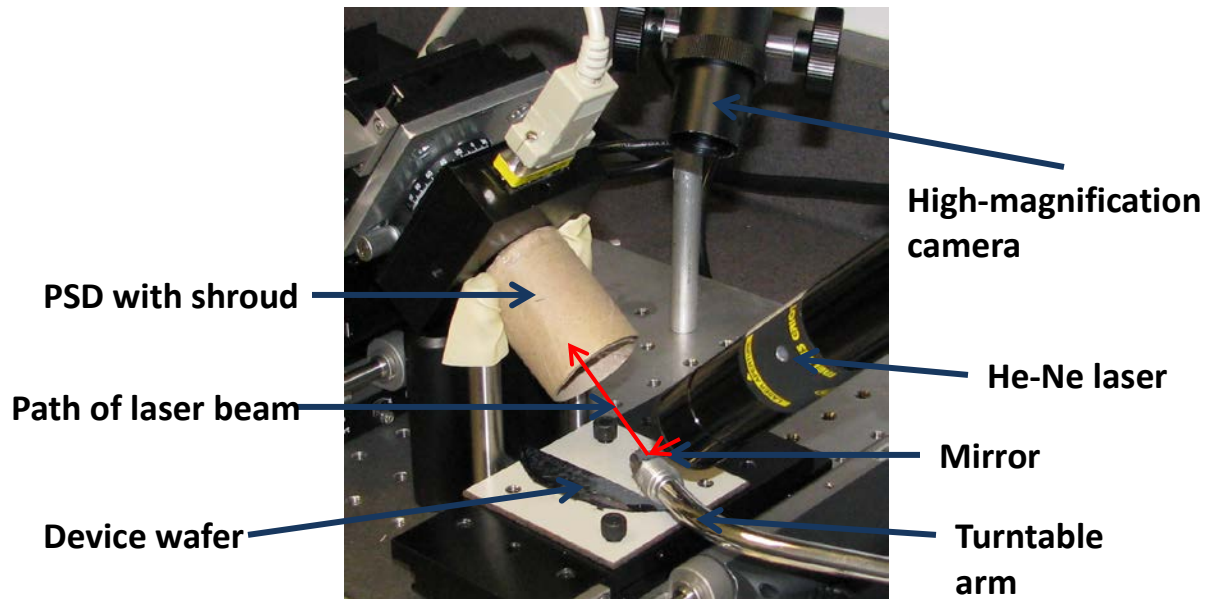


**Figure 26: Turntable arm used to apply micro-forces.**

The motion of the micrometer barrel causes the micrometer to extend and retract. This extremely fine motion along the neutral axis of the turntable arm creates a small change in the moment at the pivot. To compensate for this moment, a small force is applied at the needle, which can be used to actuate the mirror devices.

To calibrate the turntable arm, the needle was placed on a very sensitive scale. One division on the micrometer (corresponding to 1 micron of travel of the micrometer) produced approximately 38 micronewtons of force at the needle, permitting 38 micronewtons of force resolution applied to the device.

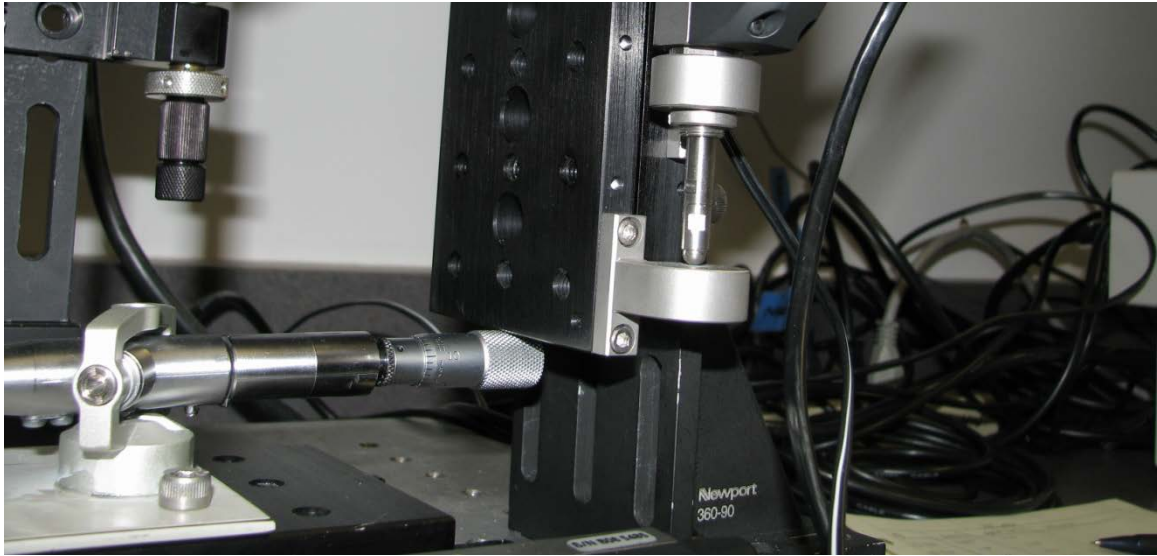
The turntable arm was positioned such that the top of the arm would be parallel to the floor when resting on the surface of a flat silicon wafer. A small mirror was mounted on the arm above the needle; when the force from the needle caused torsion in a micromirror device, this mirror would sink down toward the wafer a distance equal to the deflection of the micromirror device. By bouncing a laser beam off of this mirror and into a position sensitive detector (PSD), the deflection resulting from a known applied force could be recorded as a change in voltage.



**Figure 27: Optics of test apparatus.**

### **Test Methods**

In order to enable the accurate placement of the force needle on the edge of the micromirrors, a high-magnification video camera was focused at the landing point of the force needle, and stepper motors were used to position the device wafer beneath the needle. Once alignment was satisfactory, the turntable arm was set to the desired force using the micrometer, and lowered onto the device by slowly raising a vertically-positioned stepper motor and allowing the arm to rotate to contact the micromirror. This kept the arm from oscillating and ensured an accurate application of force.



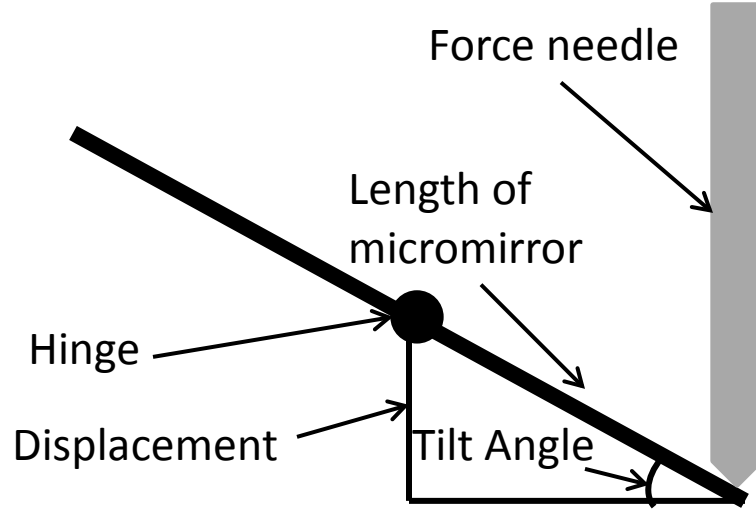
**Figure 28: Stepper motor being used to slowly raise and lower the turntable arm and force application needle.**

Once the needle was in full contact with the test device, the deflection of the device could be recorded as an output voltage from the position-sensitive detector. The change in voltage from the undeflected neutral point would correspond to a linear displacement on the face of the position-sensitive detector. Unfortunately, noise created by the electronic amplifier and ambient lighting striking the position-sensitive detector overwhelmed the true change in voltage, which would have been on the order of millivolts. This noise prevented the test apparatus from yielding any useful force versus displacement data.

Had the electronic noise not been present, however, the tilt angle could have been computed from the voltage. Because the laser mirror mounted on the turntable arm was mostly undergoing linear displacement equal to the linear displacement of the micromirror, the linear displacement of the laser beam on the position-sensitive detector would have been equal to the deflection of the micromirror. Because the position-sensitive detector had a correspondence of 1

millivolt to 1 micron vertically on the detector, the change in voltage, measured in milliamps, due to the applied force was approximately equal to the displacement of the mirror, measured in microns.

If the tip of the force needle was placed approximately at the edge of the device, the length of the mirror could then be used to find the deflection angle.

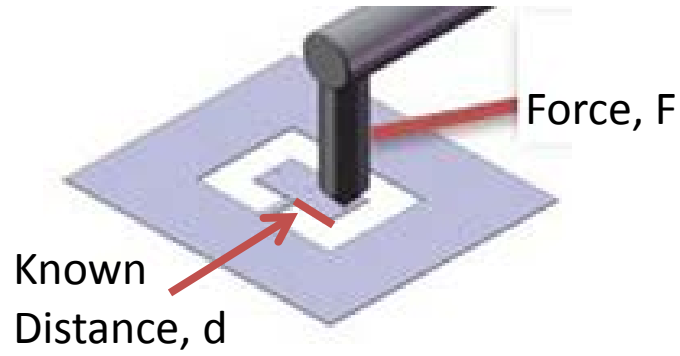


**Figure 29: Relationship between tilt and displacement.**

Assuming the case of a micromirror with a 2 mm footprint (i.e. a 1mm length from the pivot to the edge of the mirror), and a displacement of 5 microns (5 mV from the photosensitive detector), the angle would be

$$\theta = \sin^{-1} \frac{\text{Displacement}}{\text{Length}} = \sin^{-1} \frac{5 \mu\text{m}}{1\text{mm}} = 0.3^\circ \quad (\text{Equation 4})$$

Since the applied force is known from the micrometer, it is then possible to calculate the elastic torsion modulus,  $\kappa = \frac{\tau^{18}}{\theta}$ . First, however, the torque must be found, again assuming the applied force is at the edge of the device.



**Figure 30: Calculating torque on a micromirror.**

The torque is then  $\tau = Fd$ , and the elastic torsion modulus can be written as

$$\kappa = \frac{Fd}{\theta} \quad (\text{Equation 5})$$

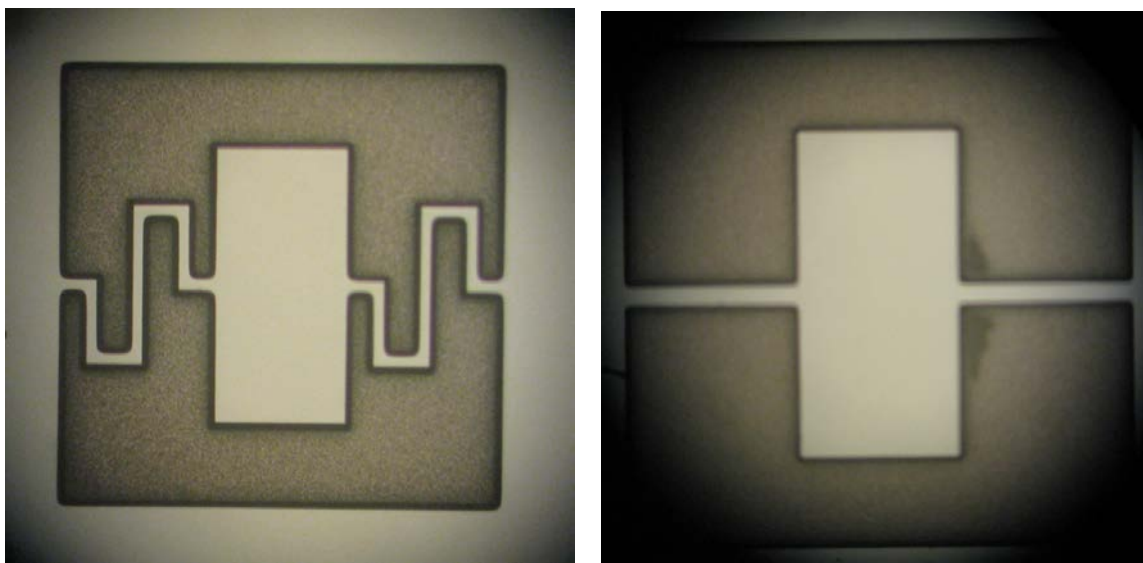
Where  $F$  is the force applied with the needle and set with the micrometer,  $d$  is half the device “footprint” (Table I), and  $\theta$  is the tilt angle calculated with Equation 4.

## Results

### Overview

Although all 7 device types were successfully fabricated, the only SOI wafer used for processing snapped before completion of the devices. As a result, no etch stop layer was used in the fabrication of any of the devices, which are of questionable thickness.

Furthermore, despite the demonstration of the viability of the process to create serpentine-hinged devices, the relative mechanical properties of straight-hinged and serpentine-hinged devices could not be established due to limitations in the testing equipment.



**Figure 31: Optical microscope images of completed devices of design #1 (left) and design #2 (right).**

### **Fabrication Difficulties**

The SOI wafer was not the only wafer to snap: over 80% of the process wafers ended up snapping before yielding devices. This extremely high scrap rate is unsurprising for two reasons: a total process time in excess of 50 hours per wafer, providing ample opportunities for mishandling, and two 15-hour deep etches, both of which are extremely harsh on the wafer due to pitting around defects and scratches in the oxide. By the end of the second deep etch, the wafers tended to be very brittle, and keeping them intact was a challenge.

## **Conclusions and Recommendations**

### **Process Feasibility**

In the sense that the process described is capable of producing functional devices, it is successful – however, it is not a practical, repeatable method. The wafers used in the process become excessively fragile, and while the devices seem easily capable of surviving the processing, the wafers do not. Furthermore,

the wafers required to create the devices cost \$180 each – this is not a cost-effective way to produce test devices, especially considering that the scrap rate is very high.

There are some potential solutions to this problem. One is using a boron etch stop in a normal silicon wafer, as was done by previous students, to replace the silicon dioxide etch stop of the SOI wafer<sup>19,20</sup>. This would greatly reduce costs while still providing the benefit of an etch stop, although the device thicknesses would be more difficult to control. Another option would be to cut deep etching out of the process entirely, and use deep RIE (DRIE) instead; however, this would be associated with significant cost, since  $\text{SF}_6$  is a very expensive gas, and RIE components can wear quickly. Still, DRIE is a very feasible method used in many fabrication processes, and with the correct process parameters, etch rates significantly higher than 2.2 microns per minute may be obtainable<sup>17</sup>. A boron etch stop could still be used with DRIE through the use of optical emission spectroscopy.

Even if DRIE is not an option, placing the wafer in a deep etch for approximately 15 hours simply to create alignment holes does not seem appropriate, and so either alternative methods of alignment that do not require through holes or non-chemical alignment hole creation methods should be investigated.

### **Suggestions for Future Work**

It should be understood that this project is not intended to represent a final result; it is expected that work will continue on these micromirror devices as part of a graduate thesis. Because no mechanical data was collected from the devices,



the most obvious objective for continuing work on the project is enabling the test apparatus to produce useful data, and to use that data to study the benefit of using a serpentine hinge device rather than a straight-beam hinge device.

Potential methods to improve the signal to noise ratio of the test apparatus include the use of a more sensitive detector and amplifier, or alternatively the placement of the reflecting mirror above the pivot of the turntable arm rather than at the end, so that angular deflection rather than linear deflection occurs when force is applied to the micromirror device. If the laser beam changes angle slightly rather than displacing downward, the PSD can be placed much further away from the mirror, creating a larger linear displacement on the PSD for the same displacement of the mirror.

Alternatively, the initial plans to use a microhardness tester to obtain force versus displacement curves could be realized; this ultimately depends on access to a microhardness tester.

Additionally, new methods of creating alignment holes without need for the deep etch could be explored. Silicon cannot easily be mechanically drilled because it has a propensity to shatter<sup>21</sup>. Rather than using a drill to create fine holes, electrostatic discharge could be used create small holes in a silicon wafer<sup>21,22</sup>.

Using a rotating tungsten electrode and about 200 volts of bias, it is possible to use sparking to bore a hole 50 microns or less in diameter through a 400 micron-thick wafer in less than two minutes<sup>23,24</sup>. This would not only enable alignment without the need for an initial 15-hour deep etch step, it would create holes small

enough to permit alignment using the alignment microscope instead of a magnifying lens.

Finally, free-standing micromirrors that rise up from the silicon substrate, rather than being formed by etching into the silicon, can easily be electrostatically actuated with simple circuits in the wafer below. Most micromirrors have been created this way, and it may be possible to use SU-8 to create these 3-dimensional structures at Cal Poly based on other sacrificial photoresist processes<sup>25</sup>. The greatest hurdle to creating these free-standing devices would be identifying a method to deposit sufficient metal on top of the SU-8 using Cal Poly's existing tools.

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