ANALYSIS AND DESIGN OF CONTINUOUS INPUT
CURRENT MULTIPHASE INTERLEAVED BUCK
CONVERTER

A Thesis

presented to

the Faculty of the College of Engineering

California Polytechnic State University

In Partial Fulfillment

of the Requirements for the Degree

Master of Science in Electrical Engineering

by

Sean Michael Zich

January 2009

© 2009

Sean Michael Zich

ALL RIGHTS RESERVED

APPROVAL PAGE

**TITLE: ANALYSIS AND DESIGN OF CONTINUOUS INPUT
CURRENT MULTIPHASE INTERLEAVED BUCK
CONVERTER**

AUTHOR: Sean Michael Zich

DATE SUBMITTED: January 2009

**COMMITTEE CHAIR: Dr. Taufik, Associate Professor of Electrical
Engineering**

**COMMITTEE MEMBER: Dr. James G. Harris, Professor of Electrical
Engineering**

**COMMITTEE MEMBER: Dr. John A. Saghri, Associate Professor of
Electrical Engineering**

ABSTRACT

ANALYSIS AND DESIGN OF CONTINUOUS INPUT CURRENT MULTIPHASE INTERLEAVED BUCK CONVERTER

Sean Michael Zich

The power requirements for microprocessors have been increasing per Moore's Law. According to International Technology Roadmap (ITRS), Voltage Regulator Module (VRM) for microprocessors will be about 200 W at 1 V output in 2010. With the VRM's topology of synchronous buck, serious technical challenges such as small duty cycle, high switching frequencies, and higher current demands, contribute to decreased power density and increased cost.

This thesis proposes a Continuous Input Current Multiphase Interleaved Buck topology to solve the technical challenges of powering future microprocessors. This new topology is aimed to improve past topologies by providing continuous input current and improved efficiency. An open loop system of the proposed new topology is simulated using OrCAD PSpice to evaluate the performance criteria of the VRM. A hardware prototype of a four-phase Continuous Input Current Multiphase Interleaved Buck Converter is constructed and tested to assess the targeted improvements.

ACKNOWLEDGEMENT

I would like to thank my parents, my brothers, my grandparents, and my girlfriend for all their love and support. Their love showed no bound or distance, and I am grateful to them for being there for me. In particular, I would like to thank Gran Gran everything he has done for me. Thanks and Gig 'Em.

I would also like thank Dr. Taufik for taking me under his wing and mentoring me. Not only has been a great mentor but a good friend. Thank you to Dr. Harris and Dr. Saghri for being on my committee. Your support means a lot to me. Finally, I would like to thank Arief and Furqan for all the help they have given me this past year.

TABLE OF CONTENTS

LIST OF TABLES.....	vi
LIST OF FIGURES.....	vii
CHAPTER 1 INTRODUCTION: POWER ELECTRONICS AND DC-DC CONVERTERS	1
1.1 Power Electronics	1
1.1.1 Types of Power Electronics Devices	1
1.2 DC to DC Converter Basic Topologies	4
1.2.1 Isolated Topologies.....	5
1.2.2 Non-Isolated Topologies.....	12
1.3 Thesis Objective.....	14
1.4 Document Overview	14
CHAPTER 2 BACKGROUND: VOLTAGE REGULATOR MODULES AND MULTIPHASE BUCK CONVERTERS	16
2.1 Moore's Law	16
2.2 VRM	18
2.3 Synchronous Buck Converter	19
2.4 Multiphase Buck Converter	20
2.4.1 Timing of Multiphase Buck Converter	21
2.4.2 Current Sharing.....	27
2.4.3 Current Sensing.....	28
2.5 Improving Duty Cycle in the Multiphase Buck Converter.....	29
2.5.1 Multiphase Tapped-Inductor Buck Converter	31
2.5.2 Multiphase Coupled-Buck Converter	32
2.6 Cal Poly's Multiphase Buck Converter	33
CHAPTER 3 PROPOSED TOPOLOGY: ANALYSIS AND DESIGN	35
3.1 Continuous Input Current Multiphase Interleaved Buck Converter	35
3.1.1 Input Inductors	36
3.1.2 Interleaved Switching	37
3.2 Design	40
3.2.1 Inductors	41
3.2.2 Capacitors	44
3.2.3 MOSFETs	47
3.2.4 Controller	49
3.2.5 MOSFET Drivers.....	50
3.3 Power Loss Calculations.....	53
3.3.1 Parameters.....	53
3.3.2 Inductor Losses	55
3.3.3 Capacitor Losses	56
3.3.4 MOSFET Losses	57
3.3.5 Total Power Loss and Efficiency.....	59
CHAPTER 4 SIMULATION: PROPOSED LAYOUT	61
4.1 Simulation Background	61
4.2 Output Voltage and Current.....	63
4.3 Input Current.....	65

4.4 Affect of the Input Current on the Output Current	66
4.5 Simulated Efficiency.....	69
4.6 Review of Specifications	71
CHAPTER 5 HARDWARE IMPLEMENTATION OF PROPOSED TOPOLOGY	72
5.1 Hardware Setup.....	72
5.1.1 Test Equipment	73
5.2 Chip Operation.....	75
5.3 Efficiency	77
5.4 Load and Line Regulations	79
5.5 Input Current.....	81
5.6 Output Voltage Ripple	82
5.7 Current Sharing.....	83
5.8 Transient Response	84
5.9 Frequency Response	86
5.10 Review of Specifications	88
CHAPTER 6 CONCLUSION: SUMMARY AND FUTURE WORK	90
6.1 Summary	90
6.2 Future Work	92
BIBLIOGRAPHY.....	95
APPENDIX I.....	97
APPENDIX II.....	100
APPENDIX III.....	106
APPENDIX IV	107

LIST OF TABLES

Table 3.1	Proposed Topology Specifications	40
Table 4.1	Review of Simulation Specifications.....	71
Table 5.1	List of Test Equipment	73
Table 5.2	Voltage and Current Data for Efficiency Measurement	77
Table 5.3	Experimental Efficiency Data.....	78
Table 5.4	Review of Experimental Specifications.....	89
Table 6.1	Review of Simulation/Experimental Specifications	90

LIST OF FIGURES

Figure 1.1 AC Voltage Controller	2
Figure 1.2 Full Bridge Rectifier	3
Figure 1.3 Full Bridge Inverter	3
Figure 1.4 Forward Converter.....	6
Figure 1.5 Flyback Converter	7
Figure 1.6 Push-Pull Converter.....	9
Figure 1.7 Half Bridge Converter	10
Figure 1.8 Full Bridge Converter	11
Figure 1.9 Buck Converter.....	12
Figure 1.10 Boost Converter.....	13
Figure 1.11 Buck-Boost Converter	14
Figure 2.1 Moore's Law	16
Figure 2.2 Current and Voltage Requirements	17
Figure 2.3 Synchronous Buck Converter.....	20
Figure 2.4 Multiphase Buck Converter.....	22
Figure 2.5 Multiphase Buck Converter Timing Signals	23
Figure 2.6 Time Period t_0 to t_1	24
Figure 2.7 Time Period t_1 to t_2	25
Figure 2.8 Time Period t_2 to t_3	26
Figure 2.9 Phase Inductor Currents and Output Current	27
Figure 2.10 Lossless Current Sensing using DCR of Inductor.....	29
Figure 2.11 Output Current Ripple versus Duty Cycle.....	30
Figure 2.12 Multiphase Tapped-Inductor Buck Converter [7]	31
Figure 2.13 Multiphase Coupled Buck Converter [7]	32
Figure 2.14 Cal Poly's Multiphase Buck Converter.....	34
Figure 3.1 Continuous Input Current Multiphase Interleaved Buck Converter.....	35
Figure 3.2 LC Resonant Tank.....	36
Figure 3.3 Current through Inductor in Resonant Tank.....	37
Figure 3.4 Buck Input Current	37
Figure 3.5 Cell Current Using Interleaved Switching	38
Figure 3.6 Cell Current Using Non-Interleaved Switching	39
Figure 3.7 Current through Output Capacitors	45
Figure 3.8 TPS40090 Block Diagram.....	49
Figure 3.9 PWM Controller Outputs	50
Figure 3.10 TPS2833 Block Diagram.....	51
Figure 3.11 Dead Time Between Top and Synchronous Switches.....	52
Figure 3.12 Input Power Supply Short to Ground	52
Figure 3.13 Calculated Efficiency vs. Percent Load.....	60
Figure 4.1 Circuit Layout in OrCAD PSpice.....	61
Figure 4.2 Top and Synchronous MOSFET Gate Pulse	62
Figure 4.3 Average Output Voltage and Ripple	63
Figure 4.4 Average Output Current and Ripple.....	64
Figure 4.5 RMS Input Current and Ripple.....	65
Figure 4.6 Bypass Capacitor Currents	66

Figure 4.7 Cell Output Currents.....	67
Figure 4.8 Phase Inductor Currents	68
Figure 4.9 Input/Output Power and Efficiency at Full Load	69
Figure 4.10 Simulated Efficiency	70
Figure 5.1 Picture Final Board of Proposed Topology	72
Figure 5.2 Picture of Lab Setup	74
Figure 5.3 PWM Signals from TPS40090	76
Figure 5.4 Experimental Efficiency	79
Figure 5.5 Input Current and Input Inductor Currents	81
Figure 5.6 Output Voltage Ripple.....	82
Figure 5.7 Phase Inductor Currents	83
Figure 5.8 Positive Load Step Response.....	84
Figure 5.9 Negative Load Step Response	85
Figure 5.10 Schematic for Frequency Response Measurement.....	86
Figure 5.11 Frequency Response at No Load	87
Figure 5.12 Frequency Response at Full Load	88
Figure 6.1 Calculated, Simulated, and Experimental Efficiency.....	91
Figure 6.2 Calculated Power Losses Breakdown	92

CHAPTER 1 INTRODUCTION: POWER ELECTRONICS AND DC-DC CONVERTERS

1.1 Power Electronics

Power electronics is the “study of processing and controlling the flow of electric energy by implementing solid state switches to meet requirements set by the users” [1]. There are many different input and output requirements that are set by users such as output power, output frequency, input line, etc. Therefore, different types of power electronics devices are used. Depending on the application of the power electronics device used, different solid state switches are used.

1.1.1 Types of Power Electronics Devices

There are four types of power electronics devices. First, there are AC voltage controllers which convert a fixed RMS AC input voltage to a different RMS AC output voltage. An example of an AC voltage controller can be seen in Figure 1.1. The solid state switches used in an AC voltage controller must be able to allow bidirectional paths for the current. This can be accomplished with thyristors in anti-parallel or TRIACs. Use of these switches allows for the RMS AC output voltage to be different from the input while keeping the average output voltage at zero. Another example of an AC voltage controller is a cycloconverter. Cycloconverters may be used to adjust RMS of output voltage as well as its frequency to somewhere lower than that of the input. Hence,

cycloconverters are typically used to control the speed of AC motors, such as a traction motor.

Figure 1.1 AC Voltage Controller

Second, there are rectifiers which convert an input AC voltage to an output DC voltage. Rectifiers are commonly used in off-line power supplies to convert AC voltage from a wall outlet to a usable DC voltage. Uncontrolled rectifiers, which use diodes as switches, do not control the output voltage level. The full bridge rectifier seen in Figure 1.2 is an example of a circuit used for uncontrolled rectifiers. On the other hand, controlled rectifiers, which use the same circuit but utilize thyristors as switches, control the output voltage level. Hence, controlled rectifiers become useful for applications that require adjustable DC voltage, such as for DC motor speed control. Uncontrolled rectifiers are much cheaper since no control is needed to operate the switches. However, their output is unregulated and therefore the output relies heavily on how regulated the input voltage is. In the United States, since the input typically comes from the utility, then the input AC voltage is typically regulated within 3 to 5 % of its nominal value.

Figure 1.2 Full Bridge Rectifier

Third, there are inverters which convert an input DC voltage to an output AC voltage. Inverters use MOSFETs with an anti-parallel body diode as the switches. Inverters are used in wide range of applications, such as variable frequency AC drives, renewable energy conversion, and uninterruptible power supplies. An example of a circuit used for an inverter can be seen below in Figure 1.3. The circuit is called the Full Bridge, which employs four switches to perform the conversion. There is another circuit called the Half Bridge in which the two switches on the “left leg” are replaced by equal capacitors.

Figure 1.3 Full Bridge Inverter

Finally, there are DC to DC converters, also called DC choppers, which convert an input DC voltage to a different output DC voltage. DC choppers are typically used in power supplies which make use of a common DC bus to supply the DC voltage required by the applications down the stream. When designing a DC to DC converter, high power density or high efficiency is normally desired. To achieve high power density, high switching frequencies are used to make the component values smaller. The proposed topology presented in this thesis falls into the DC to DC converter category. In particular, the proposed converter aims to achieve continuous input current multiphase interleaved buck which will be explained in detail in later sections. To better understand the proposed converter, different topologies of DC choppers will be explored in more detail next.

1.2 DC to DC Converter Basic Topologies

DC to DC converters can increase (boost) and/or decrease (buck) the input voltage. The simplest form of decreasing a DC voltage is the voltage divider. Voltage dividers are not practical for energy conversion since they do not provide output voltage regulation and have low efficiency, especially when output voltage is much lower than input voltage. Another simple form of decreasing a DC voltage is the linear regulator. Unfortunately, linear regulators work based on voltage division, hence suffers the same drawbacks as that of voltage dividers. A better form of converting a DC voltage to another level is to use a switching mode DC to DC converter.

There are two basic forms of switching mode DC to DC converters: non – isolated and isolated. The isolation refers to whether or not the input and output are electrically isolated from one another. Therefore, the isolated types may be indicated by the use of high frequency transformer in their circuit.

1.2.1 Isolated Topologies

As previously mentioned, isolated topologies use transformers to electrically isolate the input stage and output stage of the converter. The use of transformers also allows flexibility in stepping up and down the input voltage. Some disadvantages of transformers are the space and cost requirements, as well as additional loss in the circuit. There are five widely used isolated topologies. The five topologies are the Forward (Figure 1.4), Flyback (Figure 1.5), Push Pull (Figure 1.6), Half Bridge (Figure 1.7), and Full Bridge (Figure 1.8) converters. Each topology has advantages and disadvantages depending on power and size requirements.

The Forward converter is derived from a Buck converter (explained later) where the energy is delivered from the source to the load when the main switch is turned on. Figure 1.4 shows the basic Forward converter topology. Forward converters are typically used when the required output power is relatively small (less than 150 watts). The two diodes on the secondary side function as a rectifier network, while the one on the primary provides a path for the core to reset itself. An advantage of the Forward converter is that there are not many parts to construct it; hence it is relatively small and cheap to build. A

disadvantage of the Forward converter is there is considerable radio frequency interference and noise spikes on the ground buses.

Figure 1.4 Forward Converter

The DC gain of the Forward converter is:

$$\frac{V_o}{V_{in}} = \left[\frac{N_1}{N_2} \right] D$$

Therefore, the duty cycle of the Forward converter is:

$$D = \frac{V_o}{V_{in}} \left[\frac{N_2}{N_1} \right]$$

The Flyback converter is derived from a Buck-Boost converter (explained later) where the output stage is disconnected from the input stage as the main switch turns on. Figure 1.5 shows the basic configuration of a Flyback converter topology. Like the Forward converter, Flyback converters are typically used when the required output power is relatively small. Since there are fewer components used to construct the Flyback converter compared to the Forward converter, it is smaller and cheaper to build than the

Forward converter. In fact, the Flyback converter is the simplest and most economical among all isolated topologies due to its lowest part count. The disadvantage to using the Flyback converter is that the peak currents are much higher than the Forward converter. Therefore, if the same MOSFET is used, then the Flyback MOSFET is more likely to fail. In addition, since it lacks an output inductor, the Flyback converter is known to yield high output ripple. Consequently, the output capacitor is big and additional filtering may be necessary.

Figure 1.5 Flyback Converter

The DC gain of the Flyback converter is:

$$\frac{V_o}{V_{in}} = \left[\frac{N_2}{N_1} \right] \left[\frac{D}{1-D} \right]$$

Therefore, the duty cycle of the Flyback converter is:

$$D = \frac{1}{\left(1 + \left(\frac{1}{\frac{V_o}{V_{in}} \left[\frac{N_1}{N_2} \right]} \right) \right)}$$

The Push Pull converter is derived from a Buck converter where again the energy is transferred from input to output when either switch is on. Push Pull converters are typically used when the required output power is relatively medium to high (up to 1000 watts). More parts are required to construct the Push Pull converter compared to the Forward and Flyback converters, since it employs two switches on the primary side and a total of four windings for its transformer. Therefore, it is larger and more expensive to build. Another disadvantage of the Push Pull converter is that the currents flowing through the MOSFETs need to be balanced to achieve equal volt-second balance on the transformer windings. However, this was difficult to achieve due to the nature of real world devices, i.e. it is impossible to have two physically identical switches. Hence, Push Pull for a while had the “flux imbalance” issue which is no longer a problem now due to widely used current mode control PWM which forces equal sharing of switch currents. Due to the open switch voltage being twice the input voltage; the Push Pull converter is suitable for low voltage applications such as in the telephone industry. Another advantage of the Push Pull converter is that output switching frequency is twice that of the switches due to the switches being fired 180° out of phase. Figure 1.6 shows the basic configuration of the Push Pull converter topology.

Figure 1.6 Push-Pull Converter

The DC gain of the Push Pull converter is:

$$\frac{V_o}{V_{in}} = \left[\frac{N_3}{N_1} \right] 2 \cdot D, \text{ where } N_1 = N_2 \text{ and } N_3 = N_4$$

Therefore, the duty cycle of the Push Pull converter is:

$$D = \frac{1}{2} \frac{V_o}{V_{in}} \left[\frac{N_1}{N_3} \right], \text{ where } N_1 = N_2 \text{ and } N_3 = N_4$$

The Half Bridge converter is typically used when relatively medium output power is required (up to 500 watts). Furthermore, the Half Bridge converter is derived from the Buck converter where energy flows from input to output when either switch is on. Figure 1.7 shows the basic configuration of the Half Bridge converter topology. An advantage of the Half Bridge converter is the reduced voltage stress on the primary switches. Also, like the Push Pull converter, the output switching frequency is twice that of the switches due to the switches being fired 180° out of phase. The main disadvantage of the Half

Bridge converter is that there is a relatively high part count, which makes the converter relatively more costly and larger to build.

Figure 1.7 Half Bridge Converter

The DC gain of the Half Bridge converter is:

$$\frac{V_o}{V_{in}} = \left[\frac{N_2}{N_1} \right] D, \text{ where } N_2 = N_3$$

Therefore, the duty cycle of the Half Bridge converter is:

$$D = \frac{V_o}{V_{in}} \left[\frac{N_1}{N_2} \right], \text{ where } N_2 = N_3$$

The Full Bridge converter is similar to the Half Bridge converter with two input capacitors replaced by two switches. Full Bridge converters are typically used when the required output power is relatively large (greater than 500 watts). The main advantage of the Full Bridge converter is that the voltage at the primary of the transformer is the input voltage, while the voltage stress of the open MOSFETs are only the input voltage.

Therefore, the Full Bridge converter can deliver twice the amount of power than the Half Bridge converter when using the same MOSFETs. The main disadvantage of the Full

Bridge converter is that four MOSFETs are used since more control is required. This makes the circuit more complex. Also, since there are more parts, the Full Bridge converter is the largest and most expensive converter to build of the isolated converters previously discussed. Figure 1.8 shows the basic configuration of the Full Bridge converter topology.

Figure 1.8 Full Bridge Converter

The DC gain of the Full Bridge converter is:

$$\frac{V_o}{V_{in}} = \left[\frac{N_2}{N_1} \right] 2 \cdot D, \text{ where } N_2 = N_3$$

Therefore, the duty cycle of the Full Bridge converter is:

$$D = \frac{1}{2} \frac{V_o}{V_{in}} \left[\frac{N_1}{N_2} \right], \text{ where } N_2 = N_3$$

1.2.2 Non-Isolated Topologies

Non-isolated DC to DC converters are advantageous since they yield high efficiency and do not require as much space as that of the isolated topologies. There are three widely used non-isolated topologies used for stepping up or down DC voltage. Buck converters (Figure 1.9) step down voltage while Boost converters (Figure 1.10) step up voltage. Buck-Boost converters (Figure 1.11) may be used to either step up or step down voltage. All three topologies cost approximately the same to build and use approximately the same space per given output power. Also, all three topologies are typically used for low to medium output power levels.

Buck converters have the advantage of good output current characteristics since the inductor is connected directly to its output. This implies that less output filtering is required. Figure 1.9 shows the basic configuration of the Buck converter. The main disadvantage of using the Buck converter is that it requires a high side driver to power the MOSFET. The source of the MOSFET is not grounded while it is on but is floating above ground. Hence, complexity is added to the controller. Another disadvantage is that the input current is discontinuous; therefore, more input filtering is required.

Figure 1.9 Buck Converter

Figure 1.10 illustrates the basic configuration of the Boost converter. As shown, the inductor is located at the front end of the input of the Boost converter. This makes the input current of the Boost converter continuous, and hence less input filtering is required. The main disadvantage of the Boost converter is that the output current is discontinuous. This implies that the use of a larger output capacitor to ensure that the load voltage has the minimum ripple voltage possible.

Figure 1.10 Boost Converter

Figure 1.11 depicts the basic Buck-Boost converter. As the name implies, the converter combines the Buck and the Boost topology. More specifically, the input of the Buck-Boost looks like that of the Buck, while its output mimics that of a Boost. Buck-Boost has the advantage of flexibility in how its input voltage relates to output voltage. The converter becomes very useful in applications where the output voltage may drift higher or lower than the input voltage, such as that found in battery charging. There are three disadvantages to the Buck-Boost converter. First, just like the Buck converter, a high side driver is needed to power the MOSFET. Second, the input current is discontinuous, which poses the same problems as the Buck converter. Third, the output

current is discontinuous, just like the Boost converter. Hence, significant filtering is required at its input and output stages.

Figure 1.11 Buck-Boost Converter

1.3 Thesis Objective

The objective of this thesis is to design a DC to DC converter that can efficiently supply power to microprocessors. The next chapter will go into details on the challenges in designing a power supply that can power today's and the future microprocessors, but first, some of the specifications of the proposed converter will be discussed. The proposed converter will be supplied by a 12 volt supply and will output 1 volt at 40 amperes. There is no requirement for isolation. Details of design requirements for the proposed converter will be discussed further in the next chapter.

1.4 Document Overview

Chapter 1 introduced power electronics and went into further detail of the advantages and disadvantages of basic isolated and non-isolated DC to DC converters.

Voltage regulator modules and different multiphase buck converter topologies are discussed in Chapter 2. In Chapter 3, the analysis and design of the proposed Continuous Input Current Multiphase Interleaved Buck Converter topology is presented. Chapter 4 reviews the OrCAD PSpice simulation results from the open loop system of the proposed topology. The experimental results of the proposed topology are presented in Chapter 5. Chapter 6 discusses future work that can be done to improve the multiphase buck converter in general and the proposed topology specifically.

CHAPTER 2 BACKGROUND: VOLTAGE REGULATOR MODULES AND MULTIPHASE BUCK CONVERTERS

2.1 Moore's Law

Intel co-founder Gordon E. Moore stated in 1965 that the number of transistors on a chip would double approximately every two years [2]. This is known as Moore's Law, which is shown for Intel's microprocessor chips in Figure 2.1 [3]. As can be seen, the number of transistors in microprocessor chips is expected to reach one billion transistors in 2010, but Intel's Quad-Core Itanium Tukwila has 2 billion transistors per chip as of 2008.

Figure 2.1 Moore's Law

As the number of transistors increases on a microprocessor chip, more power will need to be supplied to the microprocessor chip. The trend for powering microprocessors

is depicted Figure 2.2 [3]. As shown, the output current requirements for microprocessors are rising while output voltage requirements are falling.

Figure 2.2 Current and Voltage Requirements

The favored solution to powering microprocessors is through a converter known as Voltage Regulator Module (VRM). Presently, VRMs employ Buck converters in parallel to achieve the low output voltage at high output power. The goal of using VRM is to achieve a low cost power supply with high efficiency and high power density. Power density is defined as the volume in which the converter is housed. Also, a fast transient response is important when powering a microprocessor. If the output voltage was to fall too low, then the microprocessor would turn off. On the other hand, if the output voltage is too high, then the microprocessor could be destroyed.

2.2 VRM

As indicated from Figure 2.2, future VRMs will require output voltage lower than one volt. Since, the input voltage to future VRMs will be constant at twelve volts [9]; the duty cycle will consequently reduce in the future following Buck's duty cycle equation

$D = V_o / V_{in}$. There are at least three disadvantages to having a low duty cycle. First, low duty cycle causes higher switching losses, which equate to lower efficiency. Second, low duty cycle causes a drop in the transient response. As discussed before, a slow transient response can destroy the microprocessor or cause undesirable performance from the microprocessor. Finally, lower duty cycle means that the twelve volt supply will be directly supplying energy to the microprocessor for a shorter period of time. Therefore, larger output capacitors need to be used to provide energy support. This in turn means that the VRM would be more costly, have a lower power density, and have a lower efficiency.

Figure 2.2 further shows that in the future, the output current will be higher than 200 amperes. Higher output current will cause higher current ripple and stress on components. To reduce current ripple, larger input and output capacitors will be used, but this may potentially reduce the power density, worsen efficiency, and increase cost. Moreover components that can handle higher current stress need to be selected. This also may be more costly.

A requirement for future VRMs not shown in Figure 2.2 relates to the use of higher switching frequencies. The higher switching frequency operation in VRM allows reduced circuit components which will help in achieving a more compact or higher density converter. However, higher switching frequencies may cause the efficiency to drop due to more switching losses as commonly known in any PWM converter. Also, components will need to be able to handle higher switching frequencies, which may be more costly.

There are many requirements that must be accounted for when building a VRM. A low cost solution must be found to achieve high power density and high efficiency while meeting the requirements of future VRMs. More specific details of VRM will be discussed in a later section.

2.3 Synchronous Buck Converter

Early VRMs use the synchronous Buck topology. As shown in Figure 2.3 below, the synchronous Buck topology replaces the free-wheeling diode in a Buck Converter with a MOSFET. An advantage of using this approach is that the VRM can provide low output voltage and high output current at higher efficiencies compared to the buck topology since MOSFETs have lower forward voltage than diodes at higher currents. A disadvantage of this topology is that there is a chance for both MOSFETs to be on simultaneously. This would cause a short from the twelve volt supply to ground. To avoid this short, a dead time is introduced in the PWM controller such that the MOSFETs

will never be on simultaneously. Another disadvantage of this topology is that the issue of higher switching frequencies is not addressed. Therefore, to meet the requirements of future VRMs, a different topology, the multiphase buck topology is used.

Figure 2.3 Synchronous Buck Converter

2.4 Multiphase Buck Converter

Multiphase Buck topology uses the synchronous Buck topology as a building block. The multiphase buck topology puts N number of buck converters in parallel. Figure 2.4 shows a four phase multiphase buck converter. There are many advantages to using a multiphase buck over the synchronous buck. First, by increasing the number of phases, the multiphase buck can achieve high switching frequencies as seen by the input and the output. This allows for a faster transient response, and less filtering capacitors at both the input and the output [4]. Also, each channel will carry less current due to multiple paths from input to output. This gives a major benefit especially in high current applications since conduction loss is proportional to current squared. This also means that the inductors and MOSFETs do not need to be as large, which allows for greater power density. Furthermore, the temperature of the components will not be as high,

reducing heat sinking requirements. This in turn allows for greater power density of the converter.

It has been known that as the number of phases increases in the multiphase buck, the efficiency will increase and transient response will improve. A study has shown that output ripple values are smaller when the number of phases is between two and six [5]. However, as the number of phases increases, the complexity of the converter and component count increases and hence cost raises. To achieve a good compromise among efficiency, power density, and better dynamics, the study suggests that a four phase multiphase buck topology gives the best case. Hence, the proposed VRM topology described in this thesis also focuses on a four phase configuration.

2.4.1 Timing of Multiphase Buck Converter

The basic timing of the four phase multiphase buck converter is shown in Figure 2.5. From time 0 to time t_1 , the PWM signal to the top MOSFET in phase one is high. Also, the PWM signal to the synchronous MOSFET in phases two, three, and four are high. The energy flow during this time is illustrated in Figure 2.6.

Figure 2.4 Multiphase Buck Converter

Figure 2.5 Multiphase Buck Converter Timing Signals

Figure 2.6 Time Period t_0 to t_1

As shown in Figure 2.6, the input power supply is directly supplying the load during time period t_0 to t_1 while inductors in Phase 2, 3, and 4 are discharging to help supply energy to the load. An important note is that during this time period the inductor current of Phase 1 is being charged and thus is increasing at a steeper slope than the decreasing or discharging slope of inductor currents of Phases 2, 3, and 4. Therefore, when the current from each phase is summed at the common node before the output, the slope of the output current is rising during this time period.

From time t_1 to time t_2 , the PWM signal to the synchronous MOSFET in Phases 1, 2, 3, and 4 are high. This is illustrated in Figure 2.5 and Figure 2.7. The input power supply is not directly supplying the load during this time period. Therefore, the load is

depending upon the stored energy in the four inductors. Furthermore, the inductor currents of all the phases are decreasing. This means that the output current during this time period is also decreasing.

When looking at the timing diagram in Figure 2.5, a slight period in time when both MOSFETs are off in a phase occurs. This is called dead time. Dead time will be further discussed in Chapter 3. However, in essence it is during the dead time the anti-parallel diode of the synchronous MOSFET is conducting. Therefore, the inductor current of each phase during dead time is decreasing.

Figure 2.7 Time Period t1 to t2

The time period from time t2 to time t3 is much like the time period from time t0 to time t1. The PWM signal to the top MOSFET in phase three is high. The PWM signal to the synchronous MOSFET in phases one, two, and four are high. This is illustrated in

Figure 2.5 and Figure 2.8. The input power supply is again directly supplying the load during this time period. As in the first time period, the output current is increasing.

Figure 2.8 Time Period t_2 to t_3

The next time period all phases will have the synchronous MOSFET high. Then, the load will be supplied by the input power supply through Phase 3, followed by all phases having the synchronous MOSFET high. Afterward, the load will be supplied by the input power supply through Phase 4, followed by all phases having the synchronous MOSFET high. Then, the cycle repeats itself. To conclude, the phases are not fired in numerical order (1, 2, 3, 4) but rather in a unique order (1, 3, 2, 4) called interleaving. This will be further discussed in Chapter 3.

2.4.2 Current Sharing

Another important aspect of multiphase Buck topology is current sharing. This means each phase of the multiphase Buck will have the same average inductor current and will fire 90° apart. The advantages are two folds. First, the ripple of each Buck phase will combine to make the output current ripple four times smaller than an individual Buck would give. Therefore, a high current may be obtained with a small ripple. Secondly, the input and output of the converter will see a frequency four times greater than the switching frequency applied to each Buck phase. This again occurs since each phase is 90° apart. The increase in effective frequency at the load allows for smaller output capacitance per given output ripple requirement. In addition, higher frequency means increase bandwidth and hence improved transient response. To the input, the higher frequency means less filtering requirements which may translate to less cost and less board space requirement. Figure 2.9 below shows the inductor current of each phase and the total output current.

Figure 2.9 Phase Inductor Currents and Output Current

2.4.3 Current Sensing

There are three methods that can be used to sense the current in each phase of the multiphase Buck [6]. The first method is to put a current sense resistor in series with the inductor. If a 1% current sense resistor is used, then this method would be very accurate. Unfortunately, current sense resistors are costly, and they are in the power path. Therefore, this would cause additional loss in power and hence a drop in efficiency.

Another method is to sense the current using the on resistance of the top MOSFET. Since power is already lost here, this method would not introduce additional loss to sense the current. Unfortunately, this method suffers from the fact that the on resistance of MOSFETs has a wide variation.

The third method is to use a resistor in series with a capacitor, which are in parallel with inductor. Figure 2.10 below illustrates the method. This method uses the DC resistance (DCR) of the inductor to sense the current. Since power is already lost here, this would be considered a loss-less place to sense the current. The purpose of using the resistor-capacitor network in parallel with the inductor is to measure the voltage of the DC resistance of the inductor across the capacitor. The resistor and capacitor are sized such that $\frac{L}{DCR} = R \cdot C$ which achieves the voltage across the capacitor equaling the voltage across the DC resistance of the inductor. The problem with this method is that a current sense amplifier would need to be used to amplify the sensed current.

Figure 2.10 Lossless Current Sensing using DCR of Inductor

The third method is used in the proposed topology for this thesis. The main reason being the controller selected for the proposed topology, (TPS40090), has current sense amplifiers built into the chip.

2.5 Improving Duty Cycle in the Multiphase Buck Converter

Several multiphase Buck topologies that have been developed and studied will be discussed here. These different multiphase Buck topologies attempt to address duty cycle. As shown in Figure 2.11 [7], certain duty cycles can result in no output current ripple depending on the number of phases in the multiphase Buck.

Figure 2.11 Output Current Ripple versus Duty Cycle

The graph in Figure 2.11 is plotted using the following equation [7]:

$$\Delta I_L = \frac{V_o(1-D)}{L_o F_s} \frac{N \left(D - \frac{m}{N} \right) \left(\frac{m+1}{N} - D \right)}{D(1-D)}$$

L_o and F_s are the inductance per phase and the switching frequency, respectively.

Also, N , D , and m are number of phases, the duty cycle, and the maximum integer less than the value when multiplying N and D . From Figure 2.11, we can see that in general larger duty cycles result in smaller output current ripple than smaller duty cycles.

Output current ripple is important since it greatly affects the efficiency of a converter. Larger current ripples, which results in a larger RMS current, create more conduction and switching losses in MOSFETs. In a Buck, this translates to more losses in the inductors and capacitors. Therefore, smaller current ripples are more desirable.

2.5.1 Multiphase Tapped-Inductor Buck Converter

The multiphase tapped – inductor Buck converter extends the duty cycle by using a tapped – inductor as seen in Figure 2.12 [7]. The free – wheeling path of the Buck converter taps into one turn of the inductor, while the main path of the inductor will see all n – turns of the inductor. This circuit is advantageous since you do not need to add any more components to achieve higher duty cycles.

Figure 2.12 Multiphase Tapped-Inductor Buck Converter [7]

The DC voltage gain of this topology is:

$$\frac{V_o}{V_{in}} = \frac{D}{D + n \cdot (1 - D)}$$

Therefore, the duty cycle of this topology is:

$$D = \frac{n}{\frac{V_{in}}{V_o} + n - 1}$$

Using this equation, the inductor turns can be chosen such that one can achieve no current ripple. The disadvantage of this topology is that there is a large voltage spike across the switches created by the leakage inductance of the tapped – inductor and the output capacitance of the switches. To decrease the voltage spike, one can use a snubber or a clamp circuit. Unfortunately, both methods require more components to solve the voltage spike problem which results in added cost, reliability issues, and board space.

2.5.2 Multiphase Coupled-Buck Converter

The multiphase coupled-Buck converter is another topology that extends the duty cycle, but without the voltage spike problem across the switches. As shown in Figure 2.13 [5], the multiphase coupled-Buck converter also uses a tapped-inductor to extend the duty cycle. The difference is that a third winding is used to clamp the voltage spike across the switches. The third winding is added such that the clamping capacitor appears as a constant voltage, which equals the input voltage minus the output voltage.

Figure 2.13 Multiphase Coupled Buck Converter [7]

The DC voltage gain of this topology is:

$$\frac{V_o}{V_{in}} = \frac{D}{D + n}$$

Therefore, the duty cycle of this topology is:

$$D = \frac{n}{\frac{V_{in}}{V_o} - 1}$$

Using this equation, the number of turns of the inductors can be chosen to achieve a desired duty cycle. There are two disadvantages when using this topology. First, this topology requires more components, making it more complex. Second, the output current is pulsing, which creates a larger output voltage ripple. Therefore, more filtering would be needed, which means more components will need to be used.

2.6 Cal Poly's Multiphase Buck Converter

The topology developed at Cal Poly as shown in Figure 2.14 does address the duty cycle, and attempts to increase efficiency by grouping the different phases into cells [13]. This topology uses more components to filter, but since the phases are different cells, the filtering components can be smaller.

Figure 2.14 Cal Poly's Multiphase Buck Converter

Since the first development of the converter focuses more on the functionality of the converter, the converter was only able to achieve 51.7% efficiency at full load. Hence, with a few modifications, the converter should be able to reach a much higher efficiency at full load. For example, MOSFETs should be selected based on the power that will be lost during operation of the converter. Therefore, the on-resistance and gate charge of the MOSFET must be looked at and then select the appropriate MOSFET based on whether it is the top or synchronous switch. This will be explored more in Section 3.2.3. The proposed topology in this thesis is derived from Cal Poly's converter with particular focus on improving input current characteristics, component selection, and layout to give a much improved converter.

CHAPTER 3 PROPOSED TOPOLOGY: ANALYSIS AND DESIGN

3.1 Continuous Input Current Multiphase Interleaved Buck Converter

The proposed circuit for this thesis is shown in Figure 3.1. There are two new aspects to this topology compared to the previous Cal Poly topology [13]. First, input inductors were added to improve input current characteristics. Second, interleaved switching was used for improved equal current sharing and better heat distribution.

Figure 3.1 Continuous Input Current Multiphase Interleaved Buck Converter

3.1.1 Input Inductors

By placing inductors in series with the input line into the cells, a continuous input current can be achieved without having to implement the widely used input LC filter. This is made possible by taking advantage of the feed forward capacitors which create a resonant tank. Figure 3.2 shows an example of a basic resonant tank circuit.

Figure 3.2 LC Resonant Tank

The advantage of a resonant tank is that it produces a continuous current. As shown in Figure 3.3, a resonant tank creates a sinusoidal current as shown in the following equation [8]:

$$i_L(t) = I_{L0} \cdot \cos w_0 t + \frac{V_{in} - V_{c0}}{Z_0} \sin w_0 t, \text{ where } w_0 = \frac{1}{\sqrt{LC}} \text{ and } Z_0 = \sqrt{\frac{L}{C}}$$

Figure 3.3 Current through Inductor in Resonant Tank

By creating this resonant tank at the input of the multiphase buck, a continuous input current can be achieved. Therefore, there will be a smaller peak to peak input current ripple, which further lessens RMS loss both in the power path and at the input capacitors. The sinusoidal current also has the benefit of having gradual change instead of sharp transitions such as those found in the Buck, shown in Figure 3.4. This in turn reduces the amount of electromagnetic interference noise (di/dt) back to the DC input bus.

Figure 3.4 Buck Input Current

3.1.2 Interleaved Switching

Interleaved switching is mainly used such that the cells in the proposed converter will be better balanced in its energy flow. Interleaved switching is done by modifying the

firing sequence of the individual buck converters. In the proposed topology there are two cells that make up the entire four phases. To interleave, the top buck of the top cell will fire first, and then the top buck of the bottom cell will fire. Next, the bottom buck of the top cell will fire, and finally the bottom buck of the bottom cell will fire. Figure 3.5 shows how each cell's output current is balanced due to the interleaved switching.

Figure 3.5 Cell Current Using Interleaved Switching

Interleaved switching is advantageous since it will yield a smaller current ripple and higher frequency compared to non-interleaved switching. When using cells as in the proposed topology, there is an inductor at the output of each cell. A smaller current ripple means that the RMS current will be less. Therefore, there will be less power losses in the output inductors of the cells when using interleaved switching. Figure 3.6 shows the cell currents in the proposed topology when interleaved switching is not being used.

Figure 3.6 Cell Current Using Non-Interleaved Switching

When comparing Figure 3.5 and Figure 3.6, we can see the difference between the current ripple and frequency of the cells' output currents. However, an important note is that both interleaved and non-interleaved multiphase bucks would have the same output current ripple.

Another problem that occurred with the previous Cal Poly topology was the significant unbalanced current sharing. Therefore, the output current of each cell was unbalanced. This could be problematic since a channel could be carrying more current than its components are rated to carry. This could cause the channel to fail, which would cause the other channels to share more current, resulting most likely in their failures too. Interleaved switching might be able to solve this current unbalanced issue since each cell will be forced to be more balanced.

3.2 Design

This section details how the main components in the proposed topology were chosen. Important factors when choosing components were size, cost, and impact on efficiency of the circuit. All components were chosen to be surface mount to reduce size and hence improve power density from the previous design. More importantly, the components have to be selected such that the proposed circuit meets the following specifications seen in Table 3.1. These requirements are based on Intel's VRM 9.0 DC-DC Converter Design Guidelines [9]. For a quick reference to see the components chosen for the design of the proposed topology, go to Appendix III for the Bill of Materials.

Table 3.1 Proposed Topology Specifications

Parameter	Specification
Input Voltage	12 V
Output Voltage	1 V
Output Voltage Ripple	<50 mV
Output Current	40 A
Efficiency	>80%
Line Regulation	<5%
Load Regulation	<2%
Switching Frequency	500 kHz
Continuous Input Current	Yes

3.2.1 Inductors

To find the value of the output inductor in each phase, L_1, L_2, L_3, L_4 , we will use:

$$V_L = L \cdot \frac{di}{dt}$$

For high switching frequency operation:

$$V_L = L \cdot \frac{\Delta i}{\Delta t} \Rightarrow L = V_L \frac{\Delta t}{\Delta i}$$

There are two states of a buck converter. The first state occurs when the switch is on, (closed), and the second stage occurs when the switch is off, (open). Choosing the switch to be on, we can write the equation as:

$$L = V_{L,on} \cdot \frac{t_{on}}{\Delta i}$$

When the switch is on, the voltage source is connected to the positive end of the inductor. The negative end of the inductor is connected to the output voltage. Therefore, assuming an ideal switch, the voltage across the inductor when the switch is on is equal to:

$$V_{L,on} = V_s - V_o = 12 - 1 = 11 \text{ V}$$

The time the switch is on is equal to:

$$t_{on} = DT$$

The period, T , is equal to the inverse of the switching frequency, which is given by the design requirement to be 500 kHz. Therefore, the period is equal to 2 μ s. Based on Volt-Second Balance concept, the average of the voltage across an inductor is equal to zero [3]. Therefore, we can use volt-second balance to find the duty cycle, D . The equation for volt-second balance is:

$$V_{L,on} \cdot DT + V_{L,off} \cdot (1 - D)T = 0$$

The period will be dropped from this equation. To find the duty cycle, we only need to find the voltage across the inductor when the switch is off. The positive end of the voltage is connected to ground, while the negative end is connected to the output voltage. Therefore, the voltage across the inductor when the switch is off is equal to the negative of the output voltage, which equals -1 volts. The duty cycle will equal:

$$(V_s - V_o)D + (-V_o) \cdot (1 - D) = 0 \Rightarrow D = \frac{V_o}{V_s} = \frac{1}{12}$$

The inductor is chosen to have a ripple of 1 ampere, which is 10% of the desired average current through the inductor. Plugging all the values in, the value of the inductor is equal to:

$$L = V_{L,on} \cdot \frac{t_{on}}{\Delta i} = (V_s - V_o) \frac{DT}{\Delta i} = (12 - 1) \frac{\left(\frac{1}{12}\right) \cdot 2E-6}{1} \Rightarrow L = 1.83 \text{ } \mu H$$

To ensure that the inductor would equal 1.83 micro-henrys while the switch is on, the buck output inductor was chosen to be 1.75 μH while the input and output inductors are 36 nF.

To find the peak current that will pass through the inductor, the ripple of the inductor current must be found at 10% of full load. The average inductor current at 10% of full load is equal to 1 ampere. At 10% of full load, the minimum inductor current will equal zero. Therefore, the ripple of inductor current is equal to:

$$I_{\min} = \bar{I} - \frac{\Delta i}{2} \Rightarrow 0 = 1 - \frac{\Delta i}{2} \Rightarrow \Delta i = 2 \text{ A}$$

Therefore, the inductor must be able to hand a peak current:

$$I_f = \bar{I} + \frac{\Delta i}{2} = 10 + \frac{2}{2} \Rightarrow I_f = 11 \text{ A}$$

The phase inductors chosen were the MLC1260-172ML from CoilCraft. They have an inductance of 1.75 μH and a DCR of 2.84 m Ω . The chosen inductors were a sample and can handle up to 100 A before saturation. The maximum current of the input inductors occurs when one of the top MOSFETs is on. Therefore, the maximum current flowing through the input inductors equals the maximum current flowing through the phase inductors. The maximum current flowing through the output inductors equals twice the maximum current flowing through the phase inductors. The input and output inductors chosen were the SLC7649S-360KL from CoilCraft. They have an inductance

of 36 nH and a maximum DCR of 0.17 mΩ. Also, the inductors can handle up to 100 A before saturation.

3.2.2 Capacitors

To find the output capacitor, C_4 , we will use the charge equation.

$$Q = CV$$

The average of the charge, Q , equals zero. Therefore, the charge when the switch is on is used to find the capacitor value. The voltage across the capacitor while the switch is on is equal to the output voltage ripple.

$$C = \frac{Q_{on}}{\Delta V_o}$$

Since the current through the load is the average inductor current, the inductor current ripple runs through the output capacitor. We know that based on Amp-Second Balance, the average of the capacitor current equals zero [3]. The charge when the switch is on equals the area of capacitor current above zero. Figure 3.7 shows the area of the capacitor current above zero.

Figure 3.7 Current through Output Capacitors

Therefore, the charge while one of the switches is on equals:

$$Q_{on} = \left(\frac{1}{2}\right)bh = \left(\frac{1}{2}\right)\left(\frac{T}{2}\right)\left(\frac{\Delta i}{2}\right) = \left(\frac{1}{2}\right)\left(\frac{0.5E-6}{2}\right)\left(\frac{0.25}{2}\right) \Rightarrow Q_{on} = 15.625 \text{ nC}$$

Therefore, the output capacitor value is equal to:

$$C_o = \frac{Q_{on}}{\Delta V_o} = \frac{T \cdot \Delta i}{8 \cdot \Delta V_o} = \frac{0.5E-6 \cdot 0.25}{8 \cdot 0.05} \Rightarrow C_o = 0.3125 \text{ } \mu F$$

When choosing a capacitor, the capacitor must be rated to meet its peak voltage.

The peak voltage can be found using:

$$V_{o,pk} = V_o + \frac{\Delta V_o}{2} = 1 + \frac{0.05}{2} = 1.025 \text{ V}$$

Yet another rating of capacitors is its RMS current. Since the RMS current is triangular centered on zero as shown in Figure 3.7, the RMS current equals:

$$i_{c,rms} = \frac{I_{pk}}{2} = \frac{0.125}{2} = 62.5 \text{ mA}$$

Therefore, the output capacitors chosen were TPSD227M016R0050 from AVX. They are tantalum capacitors with a capacitance of 220 μF and have an Electric Series Resistance (ESR) of 50 $\text{m}\Omega$. Since, two capacitors are paralleled, the overall output capacitance is 440 micro-farads, and the overall ESR is 25 $\text{m}\Omega$. They also have a voltage rating of 6.3 V and current rating of 1.732 A.

Next, the input capacitors, C_3 , must be chosen. The input voltage ripple level is arbitrarily chosen to be 50 mV. The input switching frequency is 2 MHz. Since the maximum current ripple through the input capacitor is approximately 2 A as shown above, the input capacitance equals:

$$C_{in} = \frac{Q_{on}}{\Delta V_o} = \frac{1.250E-7}{0.05} \Rightarrow C_{in} = 6.25 \mu\text{F}$$

The peak voltage seen through the input occurs at the maximum voltage during line regulation. Therefore, the peak voltage equals approximately 14 V. The RMS input current, taken from the Power Loss Section 3.3, is approximately 5.776 A. Assuming the efficiency is at worst case of 80%, the average input current is approximately 4.1667 A. This was found by dividing full power by the input voltage. Therefore, the RMS AC ripple seen through the input capacitor equals:

$$i_{c,rms} = \sqrt{i_{rms}^2 - i_{dc}^2} = \sqrt{5.776^2 - 4.1667^2} = 4 \text{ A}$$

Therefore, the input capacitors chosen were UCD1E221MNL1GS from Nichicon. These capacitors are \$0.31. They are aluminum electrolytic capacitors with a capacitance

of 220 μF and an unspecified ESR. ESR was arbitrarily chosen high at 1 Ω . They are rated for 25 V but only 1 A. Two of these capacitors were paralleled with two tantalum capacitors (594D107X0016D2T) from Vishay/Sprague. These capacitors are \$1.84. They are 100 μF and have an ESR of 75 m Ω . Therefore, the overall input capacitance is approximately 640 μF while the ESR is approximately 36 m Ω . The rated voltage for the tantalum capacitors is 16 V while the rated current is 1.41 A. Therefore, the input capacitors can handle 4.8 A.

3.2.3 MOSFETs

Both the main and synchronous MOSFETs are N-type MOSFETS. When selecting the main and synchronous MOSFETs, we must ensure that the MOSFETs can handle the 500 kHz switching frequency. Also, the MOSFETs must be able to handle the peak current of 11 amperes, which is the same as the phase inductors. By meeting these two parameters, the proposed topology should work. To meet the 80% efficiency specification, more care must be taken in selecting the MOSFETs. First, the top MOSFET will be chosen.

The top MOSFET is closed only one-twelfth of the period. This means that less power will be lost from the on resistance of the MOSFET compared to the power lost from the capacitance of the MOSFET. Therefore, the gate charge of the MOSFET must be low, while the on resistance does not need to be kept as low. A MOSFET that meets this requirement is FDS8690 from Fairchild. The component costs \$1.10. The on

resistance is 11.4 m Ω while the total gate charge is 27 nC. To see the power lost from the top MOSFETs, refer to the Power Losses Section 3.3.

The synchronous MOSFET is closed for eleven-twelfths of the period. That means that more power will be lost from the on resistance of the MOSFET than from its capacitance. Therefore, the on resistance must be kept as low as possible while the total gate charge does need to be kept as low. Another important factor when choosing the synchronous MOSFET is the body diode, which is usually a PN junction diode. During dead time, the body diode of the synchronous MOSFET will conduct. Typically, a Schottky diode would be placed in anti-parallel to the synchronous MOSFET. This is done for two reasons. First, a Schottky diode has a lower forward voltage drop (0.15V~0.45V) than a PN junction diode (0.7V~1.7V), which equates to less power lost while the diode is conducting. Second, a Schottky diode has a much faster reverse recovery time (~100ps) than a PN junction diode (~100ns or more), which equates to less power lost due to switching. A MOSFET that meets this requirement is FDS6299S from Fairchild. The component costs \$1.85. The on resistance is 5.1 m Ω while total gate charge is 81 nC. Furthermore, a Schottky diode is built into the chip as the body diode, negating the need to place a Schottky diode in anti-parallel with the synchronous MOSFET. To see the power lost from the synchronous MOSFETs, refer to the Power Losses Section 3.3.

3.2.4 Controller

The first component selected when designing the proposed multiphase buck was the PWM controller. When selecting the controller, it was important to make sure the controller could output four PWM signals that are 90 degrees out of phase from each other. The PWM controller selected was the TPS40090 from Texas Instruments [10]. The block diagram of the TPS40090 is shown in Figure 3.8.

Figure 3.8 TPS40090 Block Diagram

The controller uses two main types of control loops. The first loop is the voltage feedback. The output voltage is sensed at the VOUT and GNDS pins, which is run into a differential amplifier. The output of the differential amplifier is the true output voltage

and is outputted at pin 11. From there, a voltage divider is used to reach a voltage of 700 mV which is run into the feedback pin. When the output voltage is too high, the PWM signals are held low. Otherwise, the PWM signals will operate normally as shown in Figure 3.9.

Figure 3.9 PWM Controller Outputs

The second loop is the current feedback. There is a current feedback loop for each buck stage. The voltage seen across the DCR of the buck inductor from each stage is compared to the voltage seen at the comp pin. Once the voltage seen across the DCR of the buck inductor goes above the voltage seen at the comp pin, the PWM signal for that buck stage will be terminated.

3.2.5 MOSFET Drivers

Each PWM signal needs to be used to control the top and synchronous MOSFETs of each stage. This is done with a MOSFET driver. The MOSFET driver selected for this converter was the TPS2832 from Texas Instruments [11]. The block diagram of the TPS2832 is shown in Figure 3.10.

Figure 3.10 TPS2833 Block Diagram

The importance of using the MOSFET driver is to enable us to precisely control and drive both low side and high side switches. A low side switch is where the source of the MOSFET is connected to ground, while a high side switch is where the source is connected to a point at a higher voltage than ground. To drive a MOSFET, the gate voltage must be higher than the source voltage. The MOSFET driver uses an externally placed capacitor as a charge pump between the Boot and Bootlo pins to achieve a gate voltage higher than the source voltage for the high side switch.

The MOSFET driver is also important in that it allows for dead time between when the top and synchronous switches are on. Figure 3.11 illustrates this. The dead time is required since a MOSFET's turn-on and turn-off times are not infinitely small.

Figure 3.11 Dead Time Between Top and Synchronous Switches

If both the top and synchronous switch were on simultaneously, then the input voltage source would be shorted to ground as illustrated in Figure 3.12. This would cause a large current spike, most likely resulting in the failure of components especially the switches.

Figure 3.12 Input Power Supply Short to Ground

3.3 Power Loss Calculations

The following power loss calculations are calculated for the proposed topology at full load for worst case scenario. A well-known industry computation software called MathCAD was used to perform the calculations.

3.3.1 Parameters

This section shows all the given, component, and calculated parameters.

Given Parameters

Output Voltage: $V_o := 1V$

Input Voltage: $V_{in} := 12V$

Output Current: $I_o := 40A$

Frequency: $f_s := 500kHz$

Component Parameters

Input Inductor DCR:	$DCR_{in} := 0.0001 \Omega$
Buck Inductor DCR:	$DCR_{buck} := 0.00284 \Omega$
Output Inductor DCR:	$DCR_{out} := 0.0001 \Omega$
Input Capacitor ESR:	$ESR_{in} := 0.036 \Omega$
Bypass Capacitor ESR:	$ESR_{by} := 0.075 \Omega$
Output Capacitor ESR:	$ESR_{out} := 0.025 \Omega$
Main Switch Q_g :	$Q_{sw} := 27 \cdot 10^{-9} C$
Synchronous Switch Q_g :	$Q_{synch} := 81 \cdot 10^{-9} C$
Main Switch R_{dson} :	$R_{sw} := 0.0114 \Omega$
Synchronous Switch R_{dson} :	$R_{synch} := 0.0051 \Omega$
Main Switch Rise Time:	$t_{rmain} := 10 \cdot 10^{-9} s$
Main Switch Fall Time:	$t_{fmain} := 35 \cdot 10^{-9} s$
Reverse Recovery Charge:	$Q_{rr} := 34 \cdot 10^{-9} C$
Body Diode Forward Volatage:	$V_{bd} := 0.7V$

The component parameters come from the typical values listed in the component data sheets. Next, some calculated parameters will be shown, where D is the duty cycle, T_s is the switching period, I_{buck} is the average current through each phase, and ΔI_{buck} is the current ripple through each phase.

Calculated Parameters

$$D := \frac{V_o}{V_{in}} \quad D = 0.083$$

$$T_s := \frac{1}{f_s} \quad T_s = 2 \times 10^{-6} \text{ s}$$

$$I_{\text{buck}} := \frac{I_o}{4} \quad I_{\text{buck}} = 10 \text{ A}$$

$$\Delta i_{\text{buck}} := 0.1 \cdot I_{\text{buck}} \quad \Delta i_{\text{buck}} = 1 \text{ A}$$

3.3.2 Inductor Losses

This section shows the power losses in the input, phase, and output inductors.

First, the power loss in the input inductors will be calculated. The calculation assumes that core losses are negligible and thus only copper loss is being considered.

Input Inductor Losses

$$D_{\text{in}} := 4 \cdot D \quad D_{\text{in}} = 0.333$$

$$I_{\text{rms}_{\text{in}}} := I_{\text{buck}} \cdot \sqrt{D_{\text{in}} \cdot \left[1 + \frac{\left(\frac{\Delta i_{\text{buck}}}{2} \right)^2}{I_{\text{buck}}^2} \right]} \quad I_{\text{rms}_{\text{in}}} = 5.776 \text{ A}$$

$$P_{\text{Lin}} := 2 I_{\text{rms}_{\text{in}}}^2 \cdot \text{DCR}_{\text{in}} \quad P_{\text{Lin}} = 0.011 \text{ W}$$

Next, the power loss from the inductor in each buck stage is calculated. Again, only copper loss is taken into consideration.

Phase Inductor Losses

$$I_{rms_buck} := I_{buck} \cdot \sqrt{1 + \frac{\left(\frac{\Delta i_{buck}}{2}\right)^2}{I_{buck}^2}} \quad I_{rms_buck} = 10.004A$$

$$P_{Lbuck} := 4 \cdot I_{rms_buck}^2 \cdot DCR_{buck} \quad P_{Lbuck} = 1.137W$$

Next, the power loss from the output inductor after each cell is calculated.

Output Inductor Losses

$$I_{obuck} := \frac{I_o}{2} \quad I_{obuck} = 20A$$

$$\Delta i_{obuck} := \frac{\Delta i_{buck}}{2} \quad \Delta i_{obuck} = 0.5A$$

$$I_{rms_obuck} := I_{obuck} \cdot \sqrt{1 + \frac{\left(\frac{\Delta i_{obuck}}{2}\right)^2}{I_{obuck}^2}} \quad I_{rms_obuck} = 20.001A$$

$$P_{Lobuck} := 2 \cdot I_{rms_obuck}^2 \cdot DCR_{out} \quad P_{Lobuck} = 0.136W$$

Finally, the total power loss from all inductors is calculated whose value is expected to be 1.284 W.

Total Inductor Losses

$$P_L := P_{Lobuck} + P_{Lin} + P_{Lbuck} \quad P_L = 1.284W$$

3.3.3 Capacitor Losses

This section shows the power loss from the input, output, and bypass capacitors.

First, the power losses from the bypass capacitors are calculated.

Bypass Capacitor Losses

$$I_{rms_{by}} := .001A$$

$$P_{C_{by}} := 2 \cdot I_{rms_{by}}^2 \cdot ESR_{by} \quad P_{C_{by}} = 1.5 \times 10^{-7} W$$

Next, the power losses from the input capacitors are calculated.

Input Capacitor Losses

$$P_{C_{in}} := I_{rms_{in}}^2 \cdot ESR_{in} \quad P_{C_{in}} = 1.201W$$

Next, the power losses from the output capacitors are calculated.

Output Capacitor Losses

$$\Delta i_o := \frac{\Delta i_{obuck}}{2} \quad \Delta i_o = 0.25A$$
$$P_{C_o} := \Delta i_o^2 \cdot ESR_{out} \quad P_{C_o} = 1.563 \times 10^{-3} W$$

Finally, the total power loss from all capacitors is calculated whose value is expected to be 1.203 W.

Total Capacitor Losses

$$P_C := P_{C_o} + P_{C_{in}} + P_{C_{by}} \quad P_C = 1.203W$$

3.3.4 MOSFET Losses

This section calculates the power losses in the main and synchronous MOSFETs.

First, the power loss from the main MOSFET is calculated. As shown, the total power loss in the main MOSFET comes from conduction, gate charge, and switching losses.

Main MOSFET Losses

$$I_{rms_{sw}} := I_{buck} \cdot \sqrt{D \cdot \left[1 + \frac{\left(\frac{\Delta i_{buck}}{2} \right)^2}{I_{buck}^2} \right]} \quad I_{rms_{sw}} = 2.888A$$

Conduction Loss

$$P_{on_{sw}} := 4 I_{rms_{sw}}^2 R_{sw} \quad P_{on_{sw}} = 0.38W$$

Switching Loss

$$P_{sw_{sw}} := 4 \cdot 0.5 I_{buck} \cdot V_{in} \cdot (t_{rmain} + t_{fmain}) \cdot f_s \quad P_{sw_{sw}} = 5.4W$$

Gate Charge Loss

$$P_{off_{sw}} := 4 Q_{sw} \cdot V_{in} \cdot f_s \quad P_{off_{sw}} = 0.648W$$

Total Main MOSFET Loss

$$P_{sw} := P_{on_{sw}} + P_{sw_{sw}} + P_{off_{sw}} \quad P_{sw} = 6.428W$$

Next, the power loss from the synchronous MOSFET is calculated. Unlike the main MOSFET, the synchronous MOSFET body diode will conduct during dead time. Therefore, there will be negligible switching loss but body diode loss must be considered. The minimum required dead time is t_{dt} .

Synchronous MOSFET Losses

$$I_{rms_synch} := I_{buck} \cdot \sqrt{(1-D) \cdot \left[1 + \frac{\left(\frac{\Delta i_{buck}}{2} \right)^2}{I_{buck}^2} \right]}$$
$$I_{rms_synch} = 9.578A$$

Conduction Loss

$$P_{on_synch} := 4 I_{rms_synch}^2 R_{synch} \quad P_{on_synch} = 1.872W$$

Gate Charge Loss

$$P_{off_synch} := 4 Q_{synch} \cdot V_{in} \cdot f_s \quad P_{off_synch} = 1.944W$$

$$t_{dt} := t_{rmain} + t_{fmain} \quad t_{dt} = 4.5 \times 10^{-8} s$$

Body Diode Loss

$$P_{sw_bd} := 4 \cdot (t_{dt} \cdot V_{bd} \cdot I_{buck} \cdot f_s + Q_{rr} \cdot V_{in} \cdot f_s) \quad P_{sw_bd} = 1.446W$$

Total Synchronous MOSFET Loss

$$P_{synch} := P_{on_synch} + P_{off_synch} + P_{sw_bd} \quad P_{synch} = 5.262W$$

Finally, the total power loss from all MOSFETs is calculated.

Total MOSFET Losses

$$P_{fets} := P_{sw} + P_{synch} \quad P_{fets} = 11.69W$$

3.3.5 Total Power Loss and Efficiency

Finally, the total power loss and efficiency at full load can now be calculated.

Total Power Lost/Efficiency

$$P_{total} := P_{fets} + P_C + P_L \quad P_{total} = 14.177W$$

$$\eta := \frac{40W \cdot 100}{40W + P_{total}} \quad \eta = 73.832$$

As shown, the expected efficiency at full load is 73.832%. Next, the same procedure was repeated over the full range of loads and graphed the result in Figure 3.13.

Figure 3.13 Calculated Efficiency vs. Percent Load

Now that all the components have been selected and the efficiency has been calculated, we can proceed with simulation to test the proposed topology before a hardware prototype is built.

CHAPTER 4 SIMULATION: PROPOSED LAYOUT

4.1 Simulation Background

The proposed topology was simulated using OrCAD PSpice to run an open loop system. Therefore, tests such as line and load regulation cannot be done due to the absence of a feedback mechanism. Figure 4.1 shows the OrCAD schematic layout of the proposed topology.

Figure 4.1 Circuit Layout in OrCAD PSpice

It is important to note that components used in the schematic were modeled to be similar to the components purchased for the hardware prototype. The FDS8690 and FDS6299S MOSFET models were downloaded from Fairchild's website. The inductors and capacitors had resistors put in series with them to model DC resistance of the inductors and Equivalent Series Resistance of the capacitors. Another important note is that the duty cycle was adjusted manually to obtain an output voltage close to the value of one volt. This must be done due to the voltage drops in the circuit. If this was a closed loop system, then the duty cycle would be adjusted automatically by the controller. Furthermore, with a closed loop system, voltage pulses would not need to be used to control the MOSFETs. Figure 4.2 shows the voltage pulse used to turn the MOSFETs on and off to simulate a PWM signal.

Figure 4.2 Top and Synchronous MOSFET Gate Pulse

As shown in Figure 4.2, there are four pulses; each pulse is separated by 500 nano-seconds and the period of any pulse is 2 micro-seconds corresponding to the 500 kHz switching frequency. Furthermore, the pulses are shown to interleave, meaning pulses in one cell are 180° apart. Also, whenever one of the pulses to a main MOSFET is high, the pulse to the corresponding synchronous MOSFET is low and vice versa. Dead time was also provided such that pulses of corresponding main and synchronous MOSFET pair never overlaps; therefore, preventing a short from the input power supply to ground.

4.2 Output Voltage and Current

As stated earlier, the duty cycle was adjusted such that the output voltage value would be close to one volt. Figure 4.3 shows the average output voltage and the output voltage ripple.

Figure 4.3 Average Output Voltage and Ripple

The average output voltage is 1.0117 V. The output voltage ripple equals 80.6 mV. This value does not fall below the desired specification of 50 mV. Also, note that the switching frequency of the output voltage is measured at 2 MHz. Therefore, the interleaved switching is working as desired.

Figure 4.4 Average Output Current and Ripple

Figure 4.4 shows the output current ripple, and as expected, the waveform follows the output voltage waveform. This is due the load being resistive. Also, its average value 40.469 A as the load resistor is set at 0.025 Ω . The peak to peak output current ripple equals 3.265 A. Looking at the phase peak to peak current ripple of 1.2 A discussed later in Section 4.4, we can conclude that the output current ripple is increased. Therefore, the current ripple cancellation does not seem to be fully occurring. On further

analysis, the bypass capacitor current affects the output current as also discussed later in Section 4.4.

4.3 Input Current

The input current waveform of Figure 4.5 is depicted below. This waveform is desirable since it is continuous. Therefore, the goal of achieving continuous input current was achieved in the proposed topology.

Figure 4.5 RMS Input Current and Ripple

The equation from Section 3.2.2 to find the RMS AC ripple current is used to find that 2.911 A would flow through the input capacitors. Therefore, less power will be consumed by the input capacitors. Also note that the frequency of the input current is

measured to be 2 MHz, which corresponds to 4 times the switching frequency. This emphasizes the frequency multiplication advantage of the multiphase Buck converter.

4.4 Affect of the Input Current on the Output Current

To achieve continuous input current, the bypass capacitors must store energy while the main MOSFETs are off. While the main MOSFETs are on, the bypass capacitors release energy through the main MOSFET that is on. This causes the current waveform as shown in Figure 4.6.

Figure 4.6 Bypass Capacitor Currents

Notice that the bypass capacitor currents are 180° apart, which is expected. The frequency of the bypass capacitor current is 1 MHz, which is also expected.

Unfortunately, the bypass current affects the cell output currents as shown in Figure 4.7.

Ideally, the cell output currents would have a frequency of 1 MHz with a rising slope for one-third of the period and falling slope for two-thirds of the period. Also, the average cell output current would equal 20 A. The waveform would ideally be triangular just like the summation of the cell's phase currents seen in Figure 4.8. Furthermore, its current ripple would be half that of the phase current ripple.

Figure 4.7 Cell Output Currents

By observing Figure 4.7, we can see that the cell output currents have a frequency of 1 MHz and a decline slope for two-thirds of the period. The ringing from switching noise seen when the slope changes are expected. However, during the one-third of the period where the current is expected to rise, the cell output current loses current through the bypass capacitor. This adversely affects the ripple cancellation at the output current, since the two cell output currents are added together to create the total output current. The negative current spike seen in the cell output current while a main MOSFET is on

(~8 A) is much greater than when all main MOSFETs are off (~1 A). Therefore, the large negative current spike is not effectively cancelled. This results in the larger than desired output current ripple.

The large negative current spike further has a negative impact since it decreases the average cell output current to less than 20 A. Therefore, to sustain an average cell output current at 20 A, more power will need to be supplied by the input source. This means there will be a drop in efficiency. The phase inductor currents can be seen in Figure 4.8 below.

Figure 4.8 Phase Inductor Currents

From Figure 4.8, we can see that the switching frequency of each current is 500 kHz while the peak to peak current ripple is approximately 1.2 A. The average current is approximately 10 A as expected. Also, each phase inductor current is 90° apart from

each other, while the phase inductor currents from a cell are 180° apart. Therefore, the phase inductor currents are acting as expected. An important note is the spike in the downward slope of each phase current. This spike corresponds to the other phase current from their cell switching on. The spike lasts for as long as the other phase current is switched on. This is important since the energy from the phase inductors in a cell supplies power to one another through the bypass capacitor. The power stored in the phase inductors is desired to only provide power to the output load. Therefore, this may reduce the overall efficiency of the converter.

4.5 Simulated Efficiency

Figure 4.9 shows the input and output average power and efficiency of the proposed topology at full load.

Figure 4.9 Input/Output Power and Efficiency at Full Load

The average output power in the simulation was 37.251 W while the input was 52.367 W. Therefore, the simulated efficiency at full load was 71.136%. This is well below the desired value of 80% efficiency. Next, the simulation was run across varying loads to determine the efficiency of the proposed topology versus percent load. Figure 4.10 shows this.

Figure 4.10 Simulated Efficiency

As shown in Figure 4.10, the worst case efficiency obtained from the simulation occurs at full load. The lower than desirable efficiency at full load is likely due to the affect of the input inductors on the proposed topology. The input inductors along with the bypass capacitors create a continuous input current that reduces power loss in the input capacitors. Unfortunately, this also creates the positive spike in the phase currents during the falling slope of the phase currents. The falling slope occurs while the

synchronous MOSFET is on. Therefore, more current through the synchronous MOSFET causes increased power losses.

4.6 Review of Specifications

Table 4.1 below shows how the simulations met the specifications set out in Chapter 3.

Table 4.1 Review of Simulation Specifications

Parameter	Specification	Simulation Results
Input Voltage	12 V	12 V
Output Voltage	1 V	1.0117 V
Output Voltage Ripple	<50 mV	80.4 mV
Output Current	40 A	40.469 A
Efficiency	>80%	71.136%
Line Regulation	<5%	N/A
Load Regulation	<2%	N/A
Switching Frequency	500 kHz	500 kHz
Continuous Input Current	Yes	Yes

As summarized in Table 4.1, the only specifications the simulations did not meet were the efficiency and output voltage ripple. Also, notice that line and load regulations were not included due the simulation being tested as an open loop system. An important note that is not mentioned in the specifications is that a continuous input current was desired and was achieved by the proposed topology simulations.

CHAPTER 5 HARDWARE IMPLEMENTATION OF PROPOSED TOPOLOGY

5.1 Hardware Setup

Once simulations were completed, a hardware prototype of the proposed topology was designed and built. Using ExpressPCB's software [12], the schematics and board layout were created. Appendix I shows the schematics while Appendix II shows the board layout of the proposed topology. Moreover, Appendix III shows the Bill of Materials for the proposed topology. After soldering the components, the Continuous Input Current Multiphase Interleaved Buck topology was ready to be tested. Figure 5.1 shows the final board of the proposed topology. As shown, the final board can hold two power supplies.

Figure 5.1 Picture Final Board of Proposed Topology

Note from Figure 5.1 that the board was not laid out optimally. A jumper was eventually needed to power the controller. Also, the MOSFETs' connections needed to be adjusted such that the circuit would run properly. Unfortunately, these adjustments done on the board layout would hurt the overall efficiency of the hardware prototype.

5.1.1 Test Equipment

The hardware prototype was tested to qualify against the specifications laid out in Chapter 3. The list of the testing equipment is shown in Table 5.1.

Table 5.1 List of Test Equipment

Manufacturer	Manufacture Part Number	Description
Hewlett Packard	6574A	DC Power Supply
Hewlett Packard	6060B	System DC Electronic Load
GWInstek	GDS-2204	Digital Storage Oscilloscope
GWInstek	GPR-6060D	Laboratory DC Power Supply
GWInstek	GDM-8245	Dual Display Digital Multimeter
Agilent	DSO3203A	Digital Storage Oscilloscope
RSR	M9803R	True RMS Multimeter
Tektronix	TM502A	AM 503 Current Probe Amplifier
Tektronix	A6302	Current Probe
Execute Engineer	EE30140A	Electronic Load
Venable Instruments	3120	Frequency Response Analyzer
Texas	TX22	50 Ω /1 W Probe End
Fluke	87	True RMS Multimeter
Dell	-	Computer

Figure 5.2 shows a picture of the lab set up used for testing. Testing was done entirely in the Power Electronics Lab Building 20 Engineering East, Room 104. An

important note while taking data is that the input power supply did not give an accurate reading of input voltage, nor did the voltage display on the electronic load for the output voltage. Therefore, multimeters were utilized to measure the correct input voltage and current and the correct output voltage.

Figure 5.2 Picture of Lab Setup

The Hewlett Packard 6574A DC Power Supply was used to separately power the controller (TPS40090) and the MOSFET drivers (TPS2832). The voltage was set to 5 V. The GWInstek GPR-6060D Laboratory DC Power Supply was used as the 12 V main input power supply. Two electronic loads (Hewlett Packard 6060B and Executive Engineering EE30140A) were utilized in parallel such that the hardware prototype could give out full load at 40 A. The main reason of using two electronic loads is that the HP

electronic load could only source approximate 37 amperes due to low voltage sensed at the electronic load. The Executive Engineering electronic load could only source approximately 30 amperes but its operation was limited due to lack of an electronic display to determine how much current was being sourced. Hence, a multimeter was used to sense the total output current sourced by the electronic load.

Two digital storage oscilloscopes (Agilent DSO3203A and GWInstek GDS-2204) were used to capture waveforms from the lab test. The Agilent oscilloscope could capture images to a computer and capture crisper images, but the oscilloscope only has two channels. Therefore, the GWInstek oscilloscope was used for any waveform display requiring more than two channels. To capture current images, Tektronix A6302 current probes were used in conjunction with Tektronix TM502A AM 503 Current Probe Amplifier. In the instance where the 4 phase inductor currents were captured, 4 current probe amplifiers and current probes were used.

5.2 Chip Operation

The first test was to ensure that the controller was outputting the desired PWM signals with correct phasing, and that the MOSFET drivers were properly receiving the PWM signals. Figure 5.3 shows the PWM signals outputted by the controller.

Figure 5.3 PWM Signals from TPS40090

As shown, the PWM signals are at approximately 490 kHz and are interleaved as desired. The switching frequency is not exactly 500 kHz because the timing resistor used was not the exact value calculated to achieve 500 kHz. To achieve the exact value at 500 kHz, the resistor used would be a common resistor value; therefore, the only common value closest to the exact resistor was used. Notice that the duty cycle of the PWM signals are fully open at approximately 87.5%. This maximum duty cycle value is produced since no current is following through the channels.

5.3 Efficiency

After running the unit through line and load regulations to ensure that no major problems were encountered, the efficiency of the hardware prototype was taken. Table 5.2 shows the data taken from the efficiency measurement. Chip current and voltage refers to the power required to operate the PWM controller and MOSFET drivers.

Table 5.2 Voltage and Current Data for Efficiency Measurement

Percent Load (%)	Output Current (A)	Output Voltage (V)	Input Current (A)	Input Voltage (V)	Chip Current (A)	Chip Voltage (V)
0	0	1.0068	0.27	12.01	0.078	4.99
10	4	1.0075	0.79	11.92	0.078	4.99
20	8	1.0079	1.19	12.05	0.078	4.99
30	12	1.0088	1.59	12.04	0.078	4.99
40	16	1.0088	1.98	12	0.078	4.99
50	20	1.01	2.37	12.06	0.078	4.99
60	24	1.0094	2.84	12.02	0.078	4.99
70	28	1.0108	3.3	11.98	0.078	4.99
80	32	1.011	3.77	12.01	0.078	4.99
90	36	1.0114	4.28	11.96	0.078	4.99
100	40	1.013	4.82	11.91	0.078	4.99

To calculate the efficiency, the following equations were used:

$$\eta = \frac{P_o}{P_{in}}(100\%), \text{ where}$$

$$P_o = \bar{I}_o \cdot \bar{V}_o$$

$$P_{in} = \bar{I}_{in} \cdot \bar{V}_{in} + \bar{I}_{in \text{ pwm}} \cdot \bar{V}_{in \text{ pwm}}$$

Using these equations, Table 5.3 was populated.

Table 5.3 Experimental Efficiency Data

Percent Load (%)	Output Power (W)	Input Power (W)	Efficiency (%)
0	0	3.63	0
10	4.03	9.81	41.1
20	8.06	15.93	50.6
30	12.11	19.53	61.98
40	16.14	24.15	66.84
50	20.2	28.97	69.72
60	24.23	34.53	70.17
70	28.3	39.92	70.89
80	32.35	45.67	70.84
90	36.41	51.58	70.59
100	40.52	57.8	70.11

Figure 5.4 shows the overall efficiency of the converter plotted against percent load. Also shown is the efficiency of the previous Cal Poly converter [13].

Figure 5.4 Experimental Efficiency

As shown in Figure 5.4, the proposed topology achieves higher efficiency than the previous Cal Poly topology. In this sense, the proposed topology has accomplished the goal of improving efficiency from the previous topology. However, the desired efficiency of 80% at full load was not met. As stated earlier, the efficiency should improve if the board is laid out optimally.

5.4 Load and Line Regulations

Using the data taken when finding the efficiency, the load regulation can be calculated as follows:

$$\% \text{Load Regulation} = \frac{V_{\text{out(min load)}} - V_{\text{out(full load)}}}{V_{\text{out(nominal)}}} (100\%)$$

The minimum load was measured at 0 A, while full load was chosen to be at 40 A. The nominal output voltage is 1 V. Therefore, the load regulation for the proposed topology equals:

$$\% \text{Load Regulation} = \frac{1.0068 - 1.013}{1} (100\%) = -0.62\%$$

As a result, the load regulation of the proposed topology meets the specification for load regulation of less than 2%.

Next, the line regulation of the hardware prototype was calculated as follows:

$$\% \text{Line Regulation} = \frac{V_{\text{out(highest input)}} - V_{\text{out(lowest input)}}}{V_{\text{out(nominal)}}} (100\%)$$

The highest input voltage is given at 14 V, while the lowest input voltage is 10 V. The output voltage at 14 V is measured at 1.0115 V, while the output voltage at 10 V is measured at 1.0118 V. As before, the nominal output voltage is 1 V. Therefore, the line regulation for the proposed topology equals:

$$\% \text{Line Regulation} = \frac{1.0115 - 1.0118}{1} (100\%) = -0.03\%$$

This shows that the line regulation of the proposed topology meets the line regulation specification of less than 5%.

5.5 Input Current

As the name of proposed topology suggests, a continuous input current is desired. In fact, a continuous input current was indeed achieved with a small ripple. This is shown in Figure 5.5 for the input inductor currents. Also, by means of the Math function of the oscilloscope, the sum of the input inductor currents was obtained to show the input current from the input power supply.

Figure 5.5 Input Current and Input Inductor Currents

The data taken for Figure 5.5 occurred while the current sense amplifier was set to 1 A per 10mV/division. The inductor currents are Channels 1 ($I_{L\ cell\ 1}$) and 2 ($I_{L\ cell\ 2}$), while the summation of both inductor currents ($I_{in\ total}$). Both input inductor currents are found to be continuous; hence, the input current is also continuous. The average input inductor current is approximately 3.5 A with a peak to peak ripple of approximately 2 A. Therefore, the proposed topology was successful in producing a continuous input current. Nevertheless, an input current with less peak to peak ripple would be more desirable since the RMS input current would be less, which in turn equates to a higher efficiency.

5.6 Output Voltage Ripple

Figure 5.7 shows the output voltage ripple of the proposed topology.

Figure 5.6 Output Voltage Ripple

As shown in Figure 5.6, the peak to peak output voltage ripple is approximately 44.8 mV. Hence, the output voltage ripple of the proposed topology meets the specification of being less than 50 mV. Figure 5.7 also shows the switching frequency of the output voltage which is measured at approximately 1.96 MHz due to the frequency multiplication effect of the proposed converter. This is close to the expected value of 2 MH.

5.7 Current Sharing

Figure 5.7 shows the inductor current of each phase.

Figure 5.7 Phase Inductor Currents

The data taken in Figure 5.7 occurred while the current sense amplifier was set to 5 A per 10mV/division. As shown, the inductor currents are interleaved. An important note is that each inductor current rises for approximately 1/12 of the period. This is desirable since the duty cycle of the proposed topology is 1/12.

Figure 5.7 further illustrates that the phases do not equally share the output current since their levels are not exactly equal to one another. Figure 5.7 shows that Phases 3 (I_{L3}) and 4 (I_{L4}) have more current compared to those in Phases 1 (I_{L1}) and 2 (I_{L2}). Unfortunately, this would mean the components in Phases 3 and 4 are more stressed than those in the other two phases, which could lead to potential problems. The

unbalanced current sharing is most likely due to poor layout of the board or the variations in actual DC resistance of inductors used in the current sensing scheme.

5.8 Transient Response

As stated in earlier chapters, a fast transient response is desired. The transient is measured using a load step response imposed by the electronic load. Figure 5.8 shows a positive load step response from zero to 25 A, while Figure 5.9 shows a negative load step response from 25 to 0 A.

Figure 5.8 Positive Load Step Response

The data taken for the positive load step in Figure 5.8 occurred while the current sense amplifier was set to 5 A per 10mV/division. The positive load step response was

captured by triggering off the rising edge of the positive load step. As can be seen in Figure 5.8, the response is under damped with sufficient damping ratio. The fast transient response is measured at an approximate value of $100.25\ \mu\text{s}$.

Figure 5.9 Negative Load Step Response

For the negative load step in Figure 5.9, the data was measured while the current sense amplifier was set to 5 A per 10mV/division. The negative load step response was captured by triggering off the falling edge of the negative load step. As can be seen in Figure 5.9, the response is under damped with better damping than that found in the step up response. This step down transient response is measured at an approximate value of $80.9\ \mu\text{s}$.

5.9 Frequency Response

Using the Venable frequency response analyzer, one can look at the stability of the proposed topology. Figure 5.10 shows how the Venable frequency response analyzer was connected to the circuit [14].

Figure 5.10 Schematic for Frequency Response Measurement

The injection resistor used was a 49.9 ohm resistor instead of a 100 ohm resistor shown in Figure 5.10. The injection point chosen in the proposed topology was before the voltage divider in the voltage feedback loop. The injection point is placed in the loop such that the signal is confined to that single path. Also, the input impedance looking into the input of the feedback loop must be high, while the output impedance looking into the output of the feedback loop must be low. The injection point meets this requirement. The input of the feedback loop is connected to the input of the operational amplifier, which has high impedance. The output of the feedback loop is connected to the output capacitance, which has low impedance. Therefore, accurate frequency response data was

able to be obtained. Figure 5.11 shows the frequency response of the proposed topology at no load.

Figure 5.11 Frequency Response at No Load

To achieve a stable system, the phase margin of the system must be above zero. A desirable amount of phase margin is between 45° and 60° . This amount of phase margin is desirable since the transient response of the system is close to being critically damped in this region. If the phase margin is lower, the system will be more under damped. If the phase margin is higher, the system will be more over damped. The phase margin of the proposed topology at no load is 57.29° . The crossover frequency is approximately 20.14 kHz. Figure 5.12 shows the frequency response of the proposed topology at full load.

Figure 5.12 Frequency Response at Full Load

The phase margin of the proposed topology at full load is 24.34° . This is less than desirable since the low phase margin corresponds to an under damped response. However, the system is stable since the phase margin is above zero. Also, the crossover frequency is approximately 19.71 kilo-Hertz, which is close to the crossover frequency at no load. Therefore, the load does not affect the crossover frequency of the unit.

5.10 Review of Specifications

Table 5.4 shows the results of the hardware implementation of the proposed topology compared to the specifications laid out in Chapter 3.

Table 5.4 Review of Experimental Specifications

Parameter	Specification	Experimental Results
Input Voltage	12 V	12 V
Output Voltage	1 V	1.013 V
Output Voltage Ripple	<50 mV	44.8 mV
Output Current	40 A	40 A
Efficiency	>80%	70.11%
Line Regulation	<5%	-0.03%
Load Regulation	<2%	-0.62%
Switching Frequency	500 kHz	490 kHz
Positive Load Step Response	-	100.25 μ s
Negative Load Step Response	-	80.9 μ s
Phase Margin	-	24.34°
Continuous Input Current	Yes	Yes

As can be seen in Table 5.4, all specifications were met including the continuous input current except for efficiency. Furthermore, the unit was properly interleaved. Overall, the proposed topology achieved all goals set out in Chapter 3 except for efficiency.

CHAPTER 6 CONCLUSION: SUMMARY AND FUTURE WORK

6.1 Summary

In conclusion, the proposed topology was derived from the previous Cal Poly topology, and then, the design and power equations were derived such that components could be chosen [13]. Next, an open loop system simulated in OrCAD PSpice was used to test the design. After simulation, a circuit was built to test the design. Table 6.1 compares the simulation and experimental results to the specifications laid out in Chapter 3.

Table 6.1 Review of Simulation/Experimental Specifications

Parameter	Specification	Simulation Results	Experimental Results
Input Voltage	12 V	12 V	12 V
Output Voltage	1 V	1.0117 V	1.013 V
Output Voltage Ripple	<50 mV	80.4 mV	44.8 mV
Output Current	40 A	40.469 A	40 A
Efficiency	>80%	71.136%	70.11%
Line Regulation	<5%	-	-0.03%
Load Regulation	<2%	-	-0.62%
Switching Frequency	500 kHz	500 kHz	490 kHz
Positive Load Step Response	-	-	100.25 μ s
Negative Load Step Response	-	-	80.9 μ s
Phase Margin	-	-	24.34°
Continuous Input Current	Yes	Yes	Yes

All specifications were met during the simulation and experimentation of the proposed topology except for efficiency. However, the efficiency was an improvement upon that of the previous Cal Poly topology, which had an efficiency of 52.985% [13]. Figure 6.1 shows a comparison of the calculated, simulated, and experimental efficiency of the proposed topology.

Figure 6.1 Calculated, Simulated, and Experimental Efficiency

As can be seen in Figure 6.1, the experimental efficiency follows the calculated efficiency by approximately 3~10% lower efficiency. Also, the simulated efficiency and experimental efficiency are basically the same at full load. Since only conduction losses are accounted for in the MOSFETs during simulation, the simulated efficiency would likely be more similar to the experimental data.

Besides meeting the specifications laid out in Chapter 3, the proposed topology also met the design goals of a continuous input current and interleaved switching.

However it was observed that the method in achieving continuous input current seems to have hurt the efficiency of the circuit. Overall, the proposed topology was successful.

6.2 Future Work

There are a few improvements to the proposed topology that could improve efficiency. First, the calculated total losses were broken down and put into Figure 6.2.

Figure 6.2 Calculated Power Losses Breakdown

Notice that the largest contributor to power loss is the main MOSFETs' switching losses. Therefore, a MOSFET with shorter rise and fall times should be used to improve switching losses. When the main MOSFET rise and fall times are shorter, the required dead time is shorter which improves the synchronous MOSFET body diode losses. The synchronous MOSFET must also be improved. First, a synchronous MOSFET with lower on resistance should be found to improve conduction losses. Another way to

improve conduction losses is to parallel the synchronous MOSFETs. This will lessen conduction losses by halving (if two MOSFETs are paralleled) the current that flows through each MOSFET. Second, a synchronous MOSFET with lower gate charge should be found to improve gate charge losses.

Another place to improve efficiency is at the input capacitors. First, capacitors with lower ESR should be found. Organic polymer capacitors provide high capacitance at low ESR; though, they are more costly than tantalum or electrolytic capacitors. Another way to improve efficiency at the input capacitors is to decrease the RMS input current. This could be done by reducing the AC ripple of the input current. The proposed topology provides a continuous input current but has a large ripple. If capacitors were to be connected to ground between the input inductors and the cells, then a resonant tank would be formed. This would likely create a continuous input current with a smaller AC ripple. Since the input current would be using this capacitor for added energy support, the bypass capacitor current spikes would not be so large. Therefore, the phase inductors would be providing more energy to the output inductors. This in turn means that the output inductor current ripple would be smaller which makes the RMS output current ripple smaller. Therefore, by adding these capacitors, the efficiency would most likely increase.

A problem noticed using the controller TPS40090 is that a phase current unbalance occurs. Therefore, another interesting thing to look into is a controller that could sense the phase currents and automatically change the phase separation to properly

balance the phase currents. Furthermore, this new controller would be able to change the phase separation if a phase were to cease to operate. For the controller currently used in this thesis, the phase separation is pre-determined by what is connected to the pin BP5. The new controller would keep the currents of each phase always balanced. This would lead to better ripple cancellation and higher efficiency.

To improve efficiency, a more optimal board layout could be implemented. First, the main input could be placed closer to the main MOSFETs to lessen copper trace losses. Second, the MOSFET drivers could be placed closer to the controller PWM signals to lessen the likelihood of noise interfering with the PWM signals. Finally, smaller components could be used to decrease board size. This would affect the distance signals would travel along the copper traces which would lessen losses and the likelihood of noise interference.

BIBLIOGRAPHY

- [1] Taufik. “Introduction to Power Electronics”. Lecture Notes. 2007.
- [2] Moore’s Law. Available at: <http://www.intel.com/technology/mooreslaw/>.
- [3] Taufik. “DC-DC Converter Design”. Lecture Notes. 2008.
- [4] Drew, Jim. “Capacitor Ripple Current Improvements”. Power Electronics Technology. August 2004 Pages 33-37.
- [5] A.Simón-Muela, C.Alonso, V.Boitier, B.Estibals, J.L.Chaptal, Freescale Semiconductor and LAAS-CNRS. “Comparative study of the optimal number of phases for interleaved Voltage Regulator Modules”. Available at: <http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=04417266>.
- [6] W. Huang, J. Clarkin, P. Cheng, G. Schuellein, ON Semiconductor, E. Greenwich, R.I. “Inductors Allow Loss-Less Current Sensing in Multiphase DC-DC Converters”. PCIM. June 2001 Pages 58-67.
- [7] P. Xu, J. Wei, and F. C. Lee, “Multiphase Coupled-Buck Converter—A Novel High Efficient 12V Voltage Regulator Module,” in *transactions on Power Electronics*, Volume 18, Issue 1, Part 1, Jan. 2003 Page(s):74 – 82
- [8] Taufik. “Advanced Power Electronics”. Lecture Notes. 2008.
- [9] Intel. “VRM 9.0 DC-DC Converter Design Guidelines”. April 2002.
- [10] TPS40090 Datasheet, Texas Instruments, May 2006.
- [11] TPS2832 Datasheet, Texas Instruments, January 2001.
- [12] ExpressPCB, ExpressSCH software. Available at: <http://www.expresspcb.com>.
- [13] Waters, Ian. “Design and Analysis of a Multiphase DC-DC Converter Prototype”. Senior Project. 2007.

- [14] “Testing Power Supplies for Stability”. Venable Technical Paper #1. Venable Industries.
- [15] Ohn, Kay. “Analysis and Design of Multiphase DC-DC Converter with Input-Output Bypass Capacitors”. Master’s Thesis. May 2007.
- [16] “Overall roadmap technology characteristics,” *International Technology Roadmap for Semiconductors*, 2006 Update.
- [17] Rashid, Muhammad. Power Electronics: Circuits, Devices, and Applications 3rd Ed. Pearson Prentice Hall: Upper Saddle River, 2003.

APPENDIX I

Notes:

1. All resistor are 1% tolerance and values are in ohms
2. All capacitor values are in μF unless otherwise noted
3. All inductor values are in μH unless otherwise noted

Company Name		
Schematic Name		
Designer's name	Rev 1.0 11/5/08	Page # or name

Controller Schematic

Company Name	
Schematic Name	
Designer's name	Rev 1.0
	Page # or name
	11/5/08

MOSFET Drivers and MOSFETs Schematic

Output Schematic

APPENDIX II

Silkscreen

Overall

Top Layer

Inner Power Layer

Inner Ground Layer

Bottom Layer

APPENDIX III

Bill of Materials

Reference Designator	#	Description	Manufacturer	Part Number	Price/unit	Price
C1,C2,C19,C20	5	Capacitor, Tantalum, SMT 7543, 100uF	Vishay/Sprague	594D107X0016D2T	1.84	9.2
C39	1	Capacitor, Aluminum organic, 100uF,10V	Nichicon	PCJ1A121MCL1GS	1.35	1.35
C3 - C6	4	Capacitor, ceramic, SMT 1206, 0.022uF	Kemet	C1206C223K5RACTU	0.15	0.6
C7, C13 - C20	7	Capacitor, ceramic, SMT 1206, 1.0uF	Kemet	C1206C105K3RACTU	0.18	1.26
C8	1	Capacitor, ceramic, SMT 1206, 5600pF	Kemet	C1206C562K5RACTU	0.33	0.33
C9	1	Capacitor, ceramic, SMT 1206, 1000pF	Kemet	C1206C102K1RACTU	0.13	0.13
C10 -C11	1	Capacitor, ceramic, SMT 1206, 4.7uF	Kemet	C1206C475K3RACTU	0.38	0.38
C12, C38	1	Capacitor, ceramic, SMT 1206, 0.01uF	Kemet	C1206C103K1RACTU	0.11	0.11
C21 - C28	8	Capacitor, ceramic, SMT 1206, 10uF	Kemet	C1206C106K3PACTU	0.63	5.04
C33-C37	6	Capacitor, Electrolytic, 3217, 220uF	Nichicon	F950G227MAAAM1Q2	0.83	4.98
L1 - L4	4	Inductor, SMT, 1.75uH	Coilcraft	MLC1260-172ML		
L5 - L7, L10	3	Inductor, SMT, 36 nH	Coilcraft	SLC7649S-300KL		
Q1 ,Q3,Q5, Q7	4	MOSFet, N-Channel, V, A	Fair Child	FDS8690	1.1	4.4
Q2,Q4,Q6,Q8	8	MOSFet, N-Channel, V, A	Fair Child	FDS6299S	1.58	12.64
R	4	Resistor, SMT 1206, 1 Meg , 1%	KOA Speer	RK73H2BTTD1004F	0.1	0.4
R1, R5, R31	3	Resistor, SMT 1206, 10k , 1%	KOA Speer	RK73H2BTTD1002F	0.1	0.3
R2, R21, R23, R25, R27	5	Resistor, SMT 1206, 25.5k , 1%	KOA Speer	RK73H2BTTD2552F	0.1	0.5
R3, R9, R12, R17, R20 R22, R24, R26, R28 - R30	11	Resistor, SMT 1206, 10 , 1%	KOA Speer	RK73H2BTTD10R0F	0.1	1.1
R4	1	Resistor, SMT 1206, 4.32k , 1%	KOA Speer	RK73H2BTTD4321F	0.1	0.1
R6	1	Resistor, SMT 1206, 49.9 , 1%	KOA Speer	RK73H2BTTD49R9F	0.1	0.1
R7	1	Resistor, SMT 1206, 45.3k , 1%	KOA Speer	RK73H2BTTD4532F	0.1	0.1
R8	1	Resistor, SMT 1206, 274k , 1%	KOA Speer	RK73H2BTTD2743F	0.1	0.1
R10, R11, R13 - R16, R18, R19	8	Resistor, SMT 1206, 0 , 1%	Vishay/Dale	CRCW12060000Z0EA	0.1	0.8
R32 - R35	4	Resistor, SMT 1206, 1k , 1%	KOA Speer	RK73H2BTTD1001F	0.1	0.4
U1	1	IC, high-frequency, multiphase controller	Texas Instruments	TPS40090		
U2 - U5	4	IC, MOSFET driver, fast synchronous buck with DTC	Texas Instruments	TPS2832		

Total = 44.32

APPENDIX IV

Efficiency Results

Percent Load	Calculated Results	Simulated Results	Experimental Results
0	0	0	0
10	49.463	87.88	41.1
20	62.451	88.78	50.6
30	67.989	89.97	61.98
40	70.796	85.78	66.84
50	72.359	82.78	69.72
60	73.238	79.69	70.17
70	73.684	76.3	70.89
80	73.903	74.42	70.84
90	73.77	73.59	70.59
100	73.665	71.136	70.11