Creating a Solar Cell Array from a Single Silicon Wafer

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Approval Page

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Abstract

Two different processes to create multi-celled solar panels from single wafers were made and implemented. To do this, the cells must not have a common ground, and both designs use different approaches to solve this problem. One utilizes a 2.9 µm deep n-type well within a 10.74 µm deep p-type well in an n-type wafer. There are two cells in series, which has a theoretical voltage of 1 V. The cells are connected in series with 1.9 µm thick gold traces. Any area that the gold is not in contact with the silicon has a .5 µm layer silicon dioxide layer in order to keep them separate. The other is made from a p-type silicon on insulator wafer with 2.9 µm deep n-type wells. There are ten cells, which gives a theoretical voltage of 5 V. Each solar cell was separated by etching through the silicon down to the buried oxide layer. This left each cell completely unconnected electrically. The traces were deposited on a glass wafer that attaches to the cells by use of a conductive epoxy. A layer of titanium was deposited first to promote adhesion to the glass, and a 1.9 µm gold layer was deposited on top of that to carry the current. Each panel is tested by measuring the short circuit current, the open circuit voltage, and intermediate points in order to create a graph of the current density versus voltage.

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Introduction

Importance of solar cells

Unlike most other forms of energy, solar cells have no emissions and don't require anything harmful to make them work. They also last for a long time without becoming significantly less efficient. Solar technology also can save money over time, as there are no upkeep costs. Because of this, they are becoming increasingly popular in both the private and public sector. In fact, over the last 20 years, market demand for solar energy has grown an average of 30% due to decline in costs in manufacturing along with increasing efficiencies in solar cells. Photovoltaic installations are predicted to be 15.4-37 GW by 2014, which is five times the market size in 2009, proving that photovoltaic energy sources are in high demand[1].

Science

P-n junction

Solar cells utilize a p-n junction in semiconductor materials, such as silicon, to create a voltage and current. The p-type material has a deficiency of electrons (thus a positive charge), while the n-type material has an excess of electrons (thus a negative charge). These charges are created by doping (or diffusing small amounts of impurity into) the silicon with different impurities. The p-type regions are doped with boron or gallium, which has three valence electrons and leaves a hole when bonded into a silicon crystal. Conversely, the n-type regions are doped with phosphorus or arsenic, which have five valence electrons and have an extra electron when replacing a silicon atom in a silicon crystal. The border between the two types of silicon is called the junction. At the junction, some of the holes in the p-type silicon combine with some of the holes in the n-type silicon. This creates an electric field that neither electrons nor holes can drift across normally. Voltage and current are created when sunlight hits the silicon and excites the electrons and holes. This excitation causes them to have more available energy and give them the ability to drift towards opposite ends of the cell (p-type for holes, n-type for electrons). Assuming there is a circuit that the charges can travel through, they will end up on the opposite side that they started in. Using the extra energy absorbed from the photons, they cross the junction and return to their ground state. The movement of the charges through the circuit creates useable energy[2].

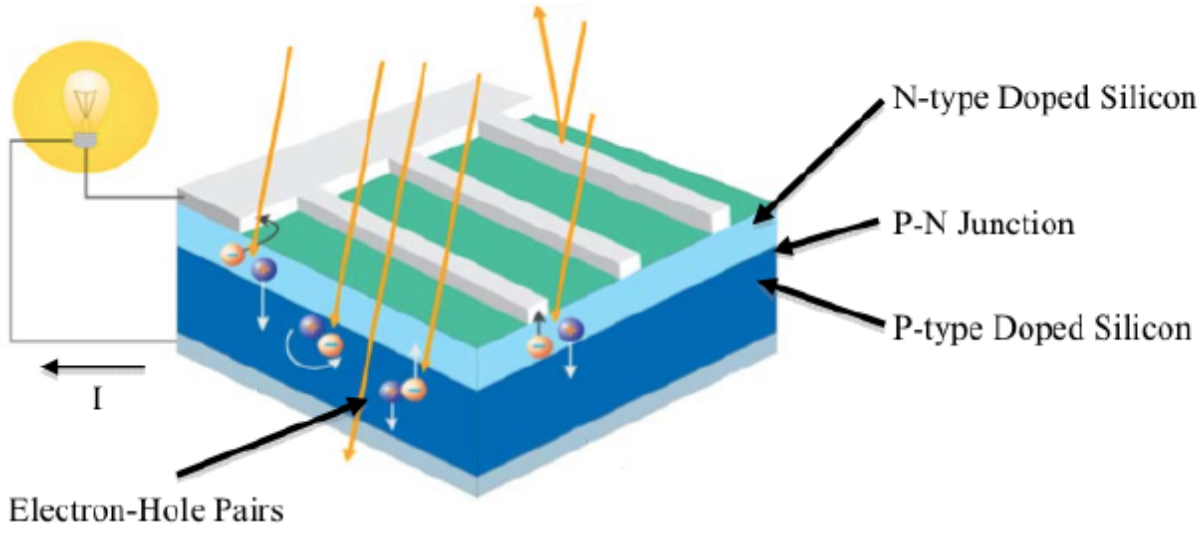


Figure 1: Typical solar cell diagram with labeled parts[1]

To create the electron-hole pairs in the solar cell, the silicon must have absorbed at least the band-gap's worth of energy from the sun. When placed in series, the voltages from the solar cells add and a solar panel, or array, is created. Typically, solar cells are not used for their voltage and current directly, rather for charging a battery that is in turn used for useful applications. Many rechargeable batteries, such as Li-Ion, NiMH, and SLA, require a constant current to recharge, which is exactly what solar cells produce. Many batteries, without special charging circuitry, require a charge rate of 10% of their total capacity per hour[3].

Series and shunt

There are two measures of resistance that are important in solar panel technology; series resistance (R_s) and shunt resistance (R_p, also called parallel resistance). Series resistance is the measure of the resistance between each cell in a solar panel. Since the whole point of this project is to connect solar cells in series, this is an important concern. It is undesirable as it limits the current through the solar panels and reduces efficiency. The metal contact pads on the cell are very thin, which contributes to resistance. P-type silicon has about 10^5 times as much conductivity as n-type silicon, which means that the array will have less resistance than it could. Connecting solar cells in series does, however, result in additive series resistance. Series resistance is equal to the nearly horizontal portion of the current versus voltage curve, next to the short circuit current. Shunt resistance is the resistance through parts of the solar cell where current is not supposed to be. If the shunt resistance is low, some current will travel across the solar cell and will not travel through the load that is connected to the cell. Typically, shunt resistance is much lower in polycrystalline materials. Shunt resistance is equal to the

slope of the current versus voltage curve at the nearly vertical portion of the graph next to the open circuit voltage.[4]

Testing terminology

Measuring Current and Voltage

Typically, a solar cell is characterized by using a Source Measurement Unit (SMU). The SMU can either provide a known voltage and measure the current or provide a known current and measure the voltage. The most common characterization method is by SMUs are stepped through a range of currents while the voltage is measured. Solar cells can be further characterized by applying a reverse bias voltage and measuring the current.

Fill factor

Fill factor is the ratio of maximum power to the product of open circuit voltage and short circuit current. It can be visually represented as the ratios of the area of the blue square to the area of the yellow square in the figure below. Commercial grade solar cells have a fill factor of 0.8 or greater while lower grade solar cells have a fill factor of 0.4 -0.7.

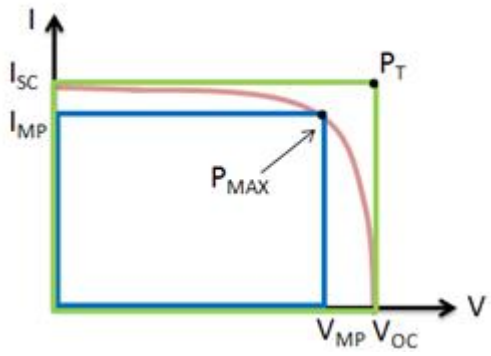


Figure 2: Graph of solar cell current versus voltage curve (red), the ideal power (green), and maximum solar cell power (blue).

Efficiency

The maximum efficiency of a solar cell is calculated as the ratio of the maximum power output by the solar cell to the power input. Power input is determined by multiplying the irradiance of the light source with the surface area of solar cell. The incident solar power is approximately $1mW/mm^2$. [5]

Existing Fabrication Process

Typically, solar cells are made from p-type silicon wafers. An oxide, SiO_2, is grown on the silicon to use as a diffusion mask. Photoresist is spun on the oxide layer and patterned in the design that is to be doped. When the resist is developed, the wafer is submerged in an oxide etchant, usually primarily HF. When the oxide is etched through to the silicon, the resist is stripped off, and the dopant is added. For a p-type wafer, the dopant must result in an n-type doped region, and therefore must be phosphorus, or an element from the phosphorus group. This dopant is baked onto the wafer in the "pre deposition" step. The resulting dopant oxide is then stripped off the wafer, again leaving bare silicon. Another oxide layer is then grown on the wafer, which serves two functions. First, the furnace process serves to drive the dopant in further, resulting in the final junction depth. The oxide also serves to mitigate electron-hole recombination along the surface of the solar cell. As before, the oxide is patterned and etched to allow the metal traces to make contact with the silicon. The metal is put on the solar cell by physical vapor deposition, patterned, and etched in the same fashion as the oxide layers. Each region of the wafer that can act as an individual solar cell is separated from the rest of the wafer. They must be mounted into the final array configuration and connected together. To do this, there is typically some sort of metal lead, either a wire or piece of conductive foil, which is attached with an electrically conductive epoxy. Leads are then attached to the array on the positive side and the negative side, which allows it to provide electricity.[6]

Design

Needs statement/ benefit to society

The solar panels that we are designing for our senior project are going to be fabricated from a single wafer and will not require separation of the wafer with subsequent connecting. For solar cells that only require a low current output but high voltage, these steps cost extra money and would be more easily accomplished with clean-room processes.

The biggest obstacle holding back solar power is its cost-competitiveness with conventional sources of power. In order for solar power to become a viable source of energy, the cost per kilowatt-hour of solar energy must be lower than the cost per kilowatt-hour of electricity from fossil fuel. Currently, the cost of conventional sources of power ranges from 3-15 cents per kilowatt-hour while the cost of solar power is approaching 25 cents per kilowatt-hour.[7][1] Although costs of solar power have reduced significantly within the last five years and continue to decrease, solar power is still much more expensive than current power sources. By

integrating multiple solar cells into one wafer we will be reducing production costs and therefore will be bridging the gap between solar energy and energy derived from fossil fuels.

There are numerous patents that have the goal of reducing post-fabrication assembly steps of solar panels.[8] Low current and high voltage cells, for example, can be made with a smaller form factor than the original wafer that they are processed from. These panels would be easier to make from a single wafer without macro-scale machining, since it would be easier to process wafers for a few extra steps instead of sending them to a different plant for connection. Large solar panels that are made to power a house or office building do not have this problem since space concerns are minimal and the individual wafers are less than a foot in diameter. Smaller panels can be made such that the finished wafer is the finished panel. This scenario uses fewer processing steps and is easier to fabricate once the process is developed.

Specifications/ goals for this project

To create a design and a process to manufacture an array of solar cells on a silicon wafer that are isolated from each other and connected in series. A proof of concept was created to verify the designs. The end goal of the project is to create an array to produce enough current (0.1 mA) and voltage (3.5 V) to power an LED.

Previous projects

The 2010 team's project created four different solar cell design. Design 1 and 2 were created to determine if the microfabrication lab in Cal Poly was capable of creating a solar cell using a single crystalline silicon wafer. Design 3 and 4 were multi-cell designs created on a SOI wafer. Each cell was physically separated by channels and grounded on the bottom by the buried oxide layer. The 2010 team attempted to sputter on metal interconnects, however they were unsuccessful, and created electrical shorts. This occurred because the channels that separated the cells were too deep and sputtered aluminum was not able to coat the sides of the channels. To solve this problem, the 2011 team spun on SU-8 in between the individual cells to serve as an insulating layer and then sputtered the aluminum across the top. The 2011 team was able to create a working design with sufficient voltage however, problems with the interconnects caused low current. The high resistance between cells could be caused by the metal traces being too thin, and the aluminum forming junction spikes.

Design Development

Multi-Well Design

The design involves diffusing a p-type well and a shallower n-type well into an n-type wafer. Rather than having the solar cells physically separate from each other, the cells would be separated by the n-type substrate. This would create a much flatter surface to sputter on interconnects and is much easier to manufacture than the previous designs. The interconnects would also be made with gold instead of aluminum to improve conductivity.

Figure 3: Cross-section of multi-well design

Before designing the final wafers a preliminary test must be conducted to determine the optimum distance the cells must be separated in order not to produce cross-talk. The masks for the preliminary test were designed to create four pairs of cells that were connected in series and were 50 mm, 35 mm, 20 mm, and 5 mm apart. The composite AutoCAD drawing is shown in Figure 3.

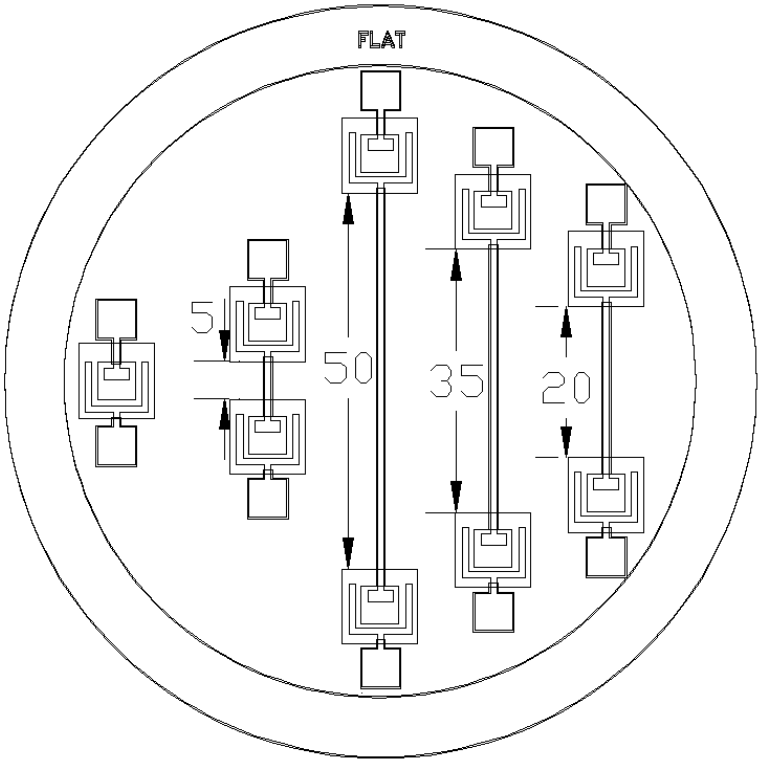


Figure 4: Composite drawing of the preliminary test structures

The cells were then physically separated from the other pairs and tested to check for open circuit voltage and short circuit current. In addition to the four pairs of cells, one individual cell was also created and checked for open circuit voltage and short circuit current. The individual cell served as a control so that the measurements from the individual cell could be compared to the pairs to determine the optimum distance between cells. The results for the preliminary test are shown in Figure 4 below.

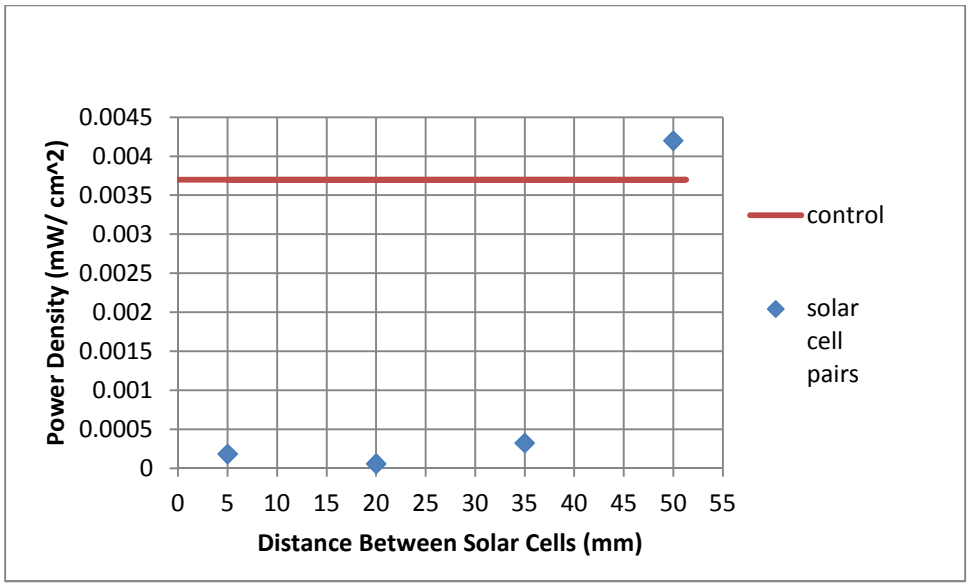


Figure 5: power density vs. distance between solar cells plot for the preliminary tests

Figure 4 shows that the optimum distance between solar cell pairs is somewhere between 35 mm and 50 mm. A pair of solar cells is an improvement on a single solar cell only when the power of the pair is above the red line depicting current in the Figure 4. Using these results, a new two-cell design was created that was a distance of 45 mm apart. A distance of 45 mm was chosen in order to create solar cells with the largest area while keeping the distance between the cells as far as possible.

Since the preliminary test results had a low short circuit current, the 2-cell design was created to have a finger-like p-n junction much like the 2010 team's design. The finger-like design would create interlocking p- and n-type regions so that the gold interconnects deposited on top would be able to theoretically collect more current.

Silicon Island Design

The second design that was fabricated and tested utilized a Silicon On Insulator (SOI) wafer. SOI wafers have a SiO_2 layer that is 10 µm below the surface of the wafer[5]. Unlike the Multi-Well design, the functional solar cells were connected in a similar way to most commercial solar cells. The theory is that ten regions could be doped into the top of the SOI wafer that would eventually be ten separate solar cells. Once that was completed, the wafer would go into a tetramethyl ammonium hydroxide (TMAH) solution, which would etch through the top of the silicon all the way to the buried oxide layer. The etch rate of TMAH is approximately 30 µm per

hour through the (100) plane of silicon, but around 1 nm per hour through SiO_2. This means that the buried oxide layer makes a great etch stop and allows some leeway in terms of over etching. Since the area between the cells is the only place that would be etched, there would only be ten distinct silicon islands left that would be connected by insulator material. This would leave them electrically unconnected, which eliminates the problem of the common ground. So far, this is a similar design to the previous solar cell array processes. The biggest difference, aside from the number of cells, is the method of interconnection. Instead of trying to fill in the gaps and plate the traces onto the wafer itself, an entirely different wafer was used to keep the traces in contact with the cells. As per the recommendations of the previous projects, gold was used as the trace material, as it has a much better conductivity than aluminum. Since the separate wafer would be on top of the device wafer, it had to be transparent. Therefore, it was chosen to be a glass wafer, which would have a small attenuation. Unfortunately, gold does not adhere to glass very well, so a layer of titanium was used, as it would adhere to both the glass and the gold.

Initially, the wafer with the metal layers (henceforth referred to as the traces wafer) was to be connected to the solar cell wafer through eutectic bonding. The gold-silicon solid solubility system has a eutectic point at 363˚C. The traces wafer and the solar cell wafer would be held together with a small pressure and heated up just past the eutectic point. This should cause the silicon and gold to dissolve into each other, creating a good electrical connection. This was tested and found to be less reliable than initially theorized. Instead, a silver filled epoxy was thought to be more reliable, easier to utilize, and able to produce a similar result.

Procedures

Multi-well design process

The process began with an n-type wafer. After cleaning it with a H_2SO_4 + H_2O_2 solution to remove organic contaminants and a HF solution to remove any native oxide layer, an 800 nm oxide layer was grown on the wafer. This was accomplished in an oxygen rich atmosphere with the presence of water vapor at 1050˚C for 2.5 hours.

oxide

n-type

After the wafer was removed from the furnace, it was coated with a layer of Photoresist, soft baked, and exposed to UV light through a mask that only allows exposure of regions where the oxide layer will be etched.The resist was then developed in order to wash away the exposed regions of Photoresist and hard baked in order to complete the cross-linking of molecules in the Photoresist. The wafer was then submerged in an HF solution in order to etch through the oxide layer. At an etch rate of around 100 nm per minute, plus 10% in order to make sure that all of the oxide is gone where it should be. Afterwards, the resist was stripped off. This step created the diffusion mask needed to create p-type wells.

oxide

n-type

Boron dopant was then spun onto the wafer and placed onto a hot plate for 5 min at 200℃ to drive off solvents. The wafers were then placed into the furnace at 1050℃ for 3 hours in an oxygen-rich, dry atmosphere to allow for the boron to diffuse into the wafer.

oxide

p-type p-type

n-type

The dopant layer and diffusion mask was then stripped off and another thick 8000 Å oxide layer was grown. It was patterned and etched the same way that the previous oxide layer was. When this oxide layer was done with processing, it was used as a diffusion mask for the n-type wells.

oxide

p-type p-type

n-type

Phosphorous dopant was spun on and the wafer was baked for five minutes at 200℃ to drive off solvents. It was then placed in the furnace at 1050℃ for 90 min to create the n-type wells.

oxide

n-type n-type
p-type p-type

n-type

The dopant layer and diffusion mask were again stripped off and a final 5000 Å thick oxide layer was grown by placing the wafer in the furnace at 1050℃ for 1hr 7min. When this oxide layer was done with processing, it was used as an insulator for metal contacts.

oxide

n-type n-type
p-type p-type

n-type

For the traces, the wafer was sputtered with gold for 10 min to create a 150 nm gold layer. It was then patterned and etched in gold etchant for 1 min.

gold
oxide

n-type n-type
p-type p-type

n-type

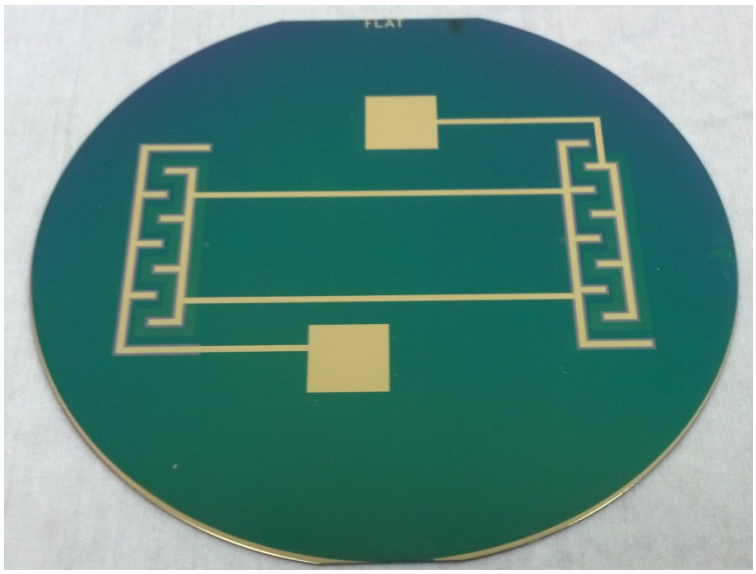
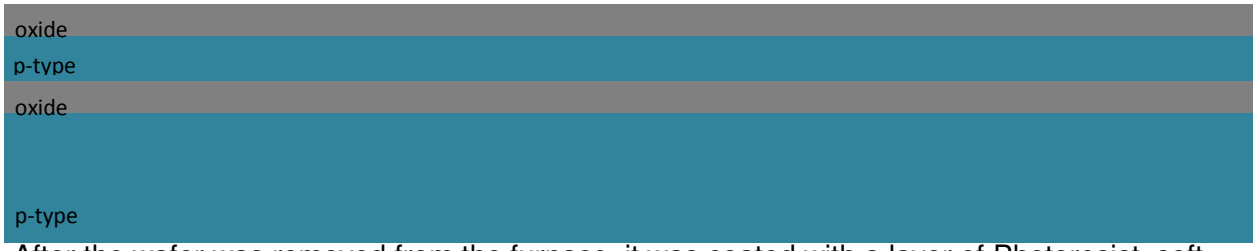


Figure 6: Final Multi-Well Design

Silicon Island Design Process

The process began with an SOI wafer. After cleaning it with a H_2SO_4 + H_2O_2 solution to remove organic contaminants and a HF solution to remove any native oxide layer, a 600 nm oxide layer was grown on the wafer. This was accomplished in an oxygen rich atmosphere with the presence of water vapor at 1050˚C for 1.5 hours.

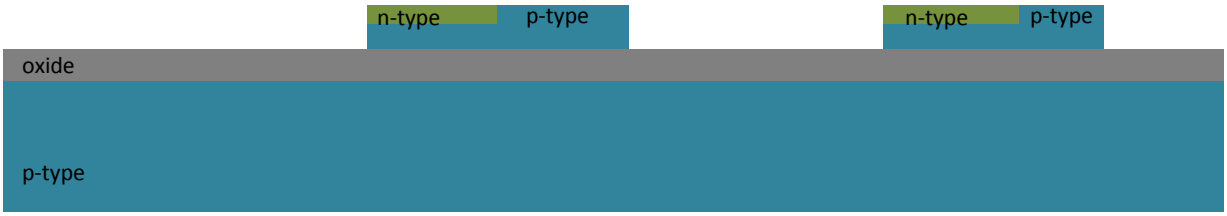


After the wafer was removed from the furnace, it was coated with a layer of Photoresist, soft baked, and exposed to UV light through a mask that only allows exposure of regions where the oxide layer will be etched. The resist was then developed in order to wash away the exposed regions of Photoresist and hard baked in order to complete the cross-linking of molecules in the Photoresist. The wafer was then submerged in an HF solution in order to etch through the oxide layer. At an etch rate of around 100 nm per minute, plus 10% in order to make sure that all of the oxide is gone where it should be. Afterwards, the resist was stripped off.

Since the wafer used was p-type, and n-type wells needed to be created, a phosphorus solution was spun on the top of the wafer. The dopant was then diffused into the wafer for 1.5 hours.

The dopant layer and diffusion mask was then stripped off and another 500 nm thick oxide layer was grown. It was patterned and etched the same way that the previous oxide layer was. When this oxide layer was done with processing, it was used as an etch mask for the deep silicon etching.

The wafer was submerged in a solution of TMAH, which etches through the silicon at a rate of approximately one 30 µm per hour. The etch rate through glass is nearly negligible, so it acts as an etch stop. This leaves silicon islands in the wafer, each with an n- and p-type region. Once the silicon is etched through to the oxide, the oxide on the surface was etched off and the SOI wafer was complete.



For the traces, a glass wafer was cleaned and coated with a layer of titanium, which adheres to glass. On top of the titanium, a layer of gold was deposited, which connects to the silicon and carries the current in the array.

A layer of Photoresist was spun on top of the gold layer, exposed, and developed in the shape of the traces to connect the solar cells together. The wafer was then immersed in a solution to etch through the gold, then in another solution to etch the titanium. Once the metal layers were etched, the resist was removed.

To bond the wafers together, a conductive, silver-filled epoxy was used. It was applied to the metal contacts and cured with the wafers together. After curing, copper wire leads were connected to the contact pads on the traces wafer using more conductive epoxy.

Now the solar cell is ready for bonding and testing (Figure 6)

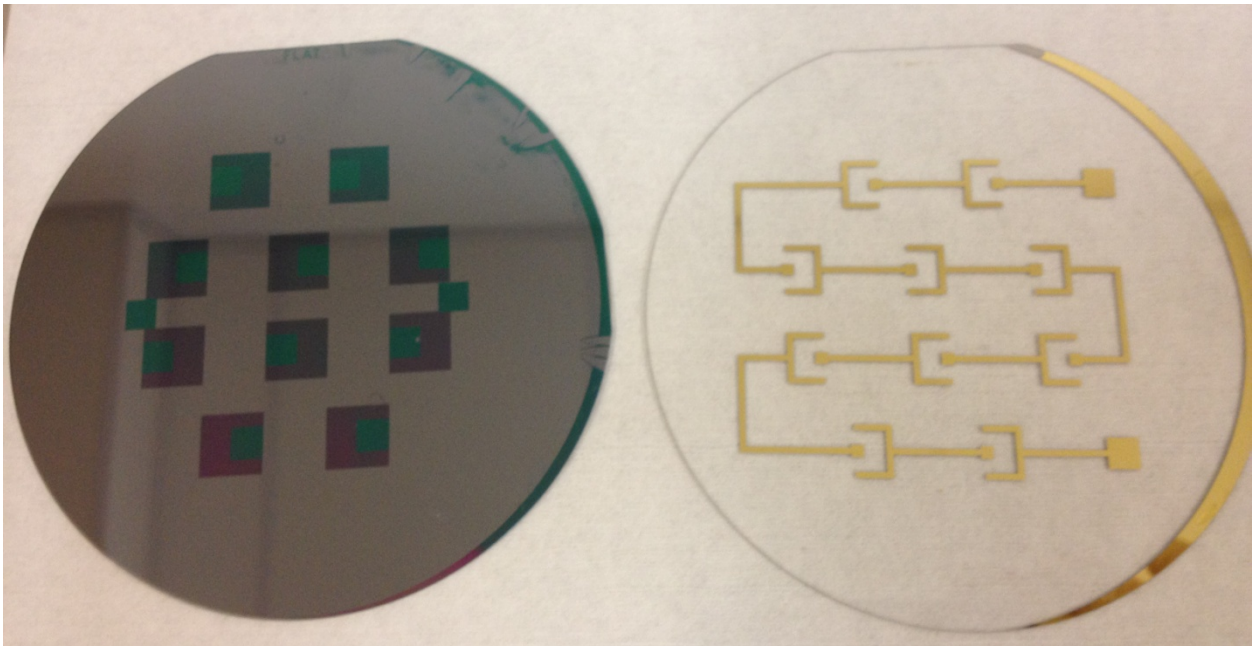


Figure 7: Both halves of the silicon island design. The solar cell wafer is on the left, while the traces wafer is on the right. Each large square on the solar cell wafer is 1 cm x 1 cm.

Testing Procedure

The wafers were tested to determine open circuit voltage and short circuit current and the data was used to calculate power and fill factor of the solar cell. In order, to test the wafers probes were placed on both the positive and negative electrodes and connected to a Kiethley source meter. The wafers were placed under a Cole Parmer Model 41500-50 fiber optic illuminator for about an hour to get to an equilibrium temperature. The Keithely was programmed to step through a series of voltages with a step size of .01 every 250 ms and corresponding current reading were measured. This data was then recorded and graphed in LabView.

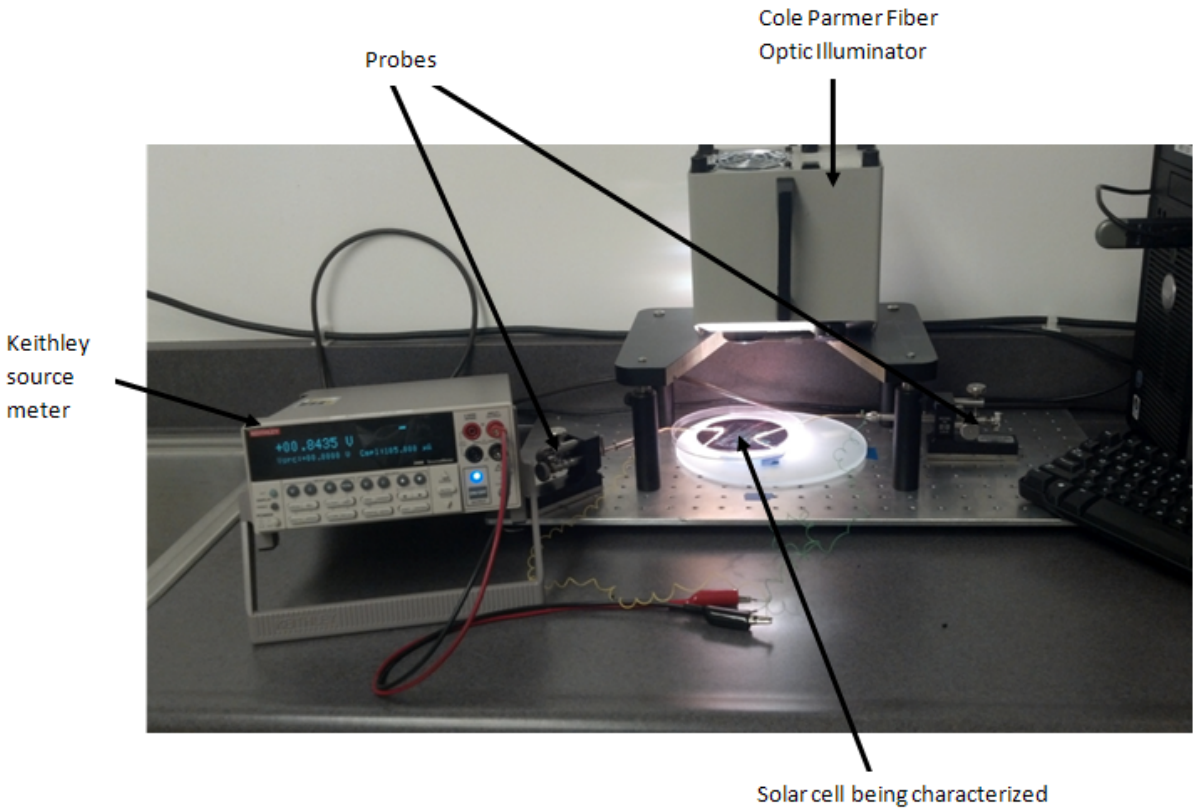


Figure 8: Solar cell testing setup

Results Analysis

Multi-well design

Three 2-cell devices were fabricated and tested to create current-voltage curves in both sun light and lab light. Additionally, each individual cell was tested to investigate series resistance. The individual cells were only tested in the lab light. The sun light measurements were taken at 1 pm on a sunny day with light intensity of 108,000 lux. The intensity of the lab light was around 100,000 lux. Figures 7-9 shows the open circuit voltage for the 2-cells ranged from 0.73 V - 0.85 V and for the individual cells ranged from 0.35 V - 0.43 V.

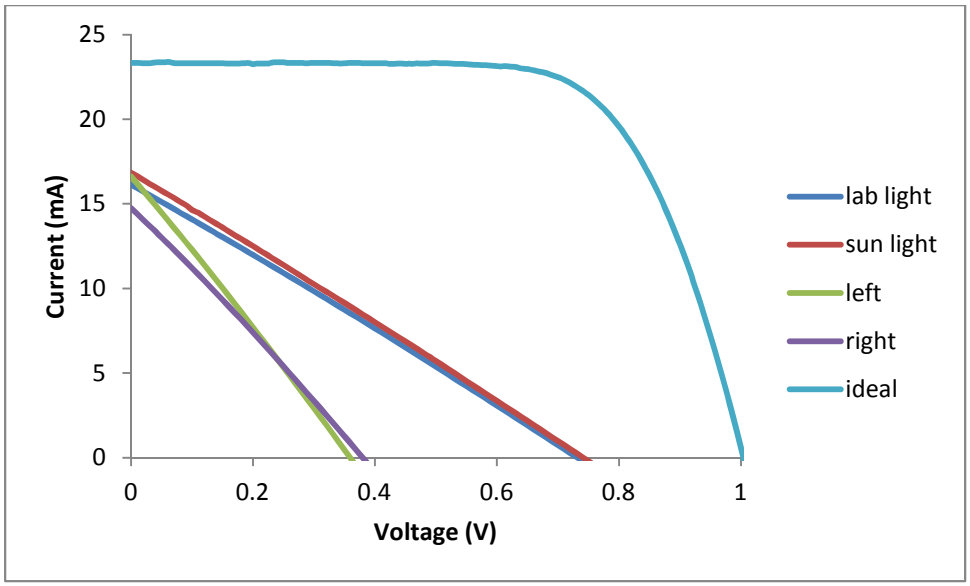


Figure 9: Current and voltage curves for wafer 1 in lab light, sunlight, and ideal

Table I: Critical Measurements for Wafer 1

	Voc	Isc (mA)	Power (mW)	FF
lab light	0 .7313	16.12	3.07	0.2603
sun light	0.7412	16.85	3.22	0.2575
left	0.3590	16.60	1.55	0.2605
right	0.3798	14.74	0.48	0.2640

The highest power produced from all three wafers was 3.8 mW (sunlight) by wafer 2. Although, wafer 2 had the highest power it had a lower fill factors (0.2582).

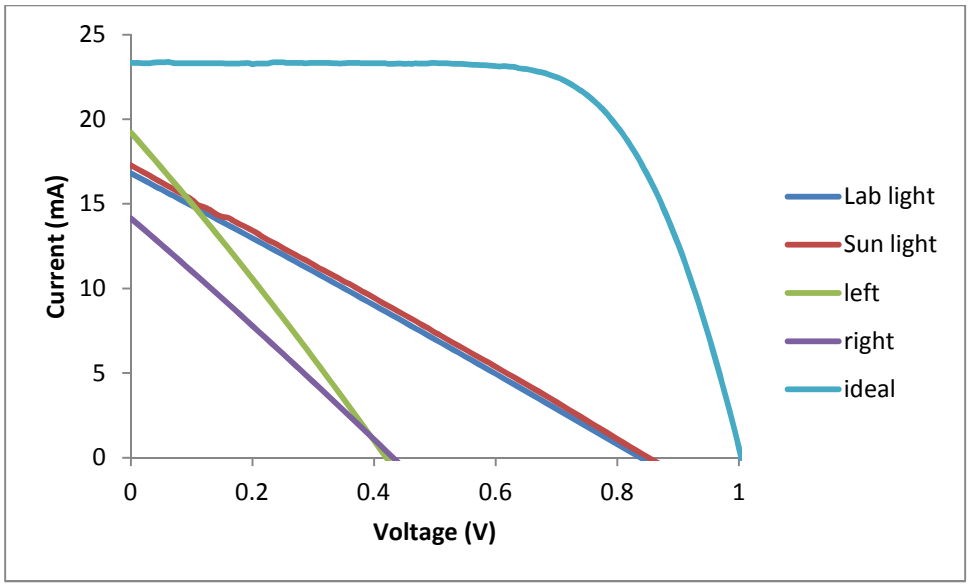


Figure 10: Current and voltage curves for wafer 2 in lab light, sunlight, and ideal

Table II: Critical Measurements for Wafer 2

	Voc	Isc (mA)	Power(mW)	FF
lab light	0.8382	16.80	3.617	0.2569
sun light	0.8519	17.27	3.799	0.2582
left	0.4197	19.20	2.123	0.2634
right	0.4311	14.14	1.567	0.2572

Wafer 3 was only sputtered with gold for 5 min rather than 10 min compared to the other wafers. The data below shows no evidence of the thickness of the traces having an effect on the current and voltage of the cells.

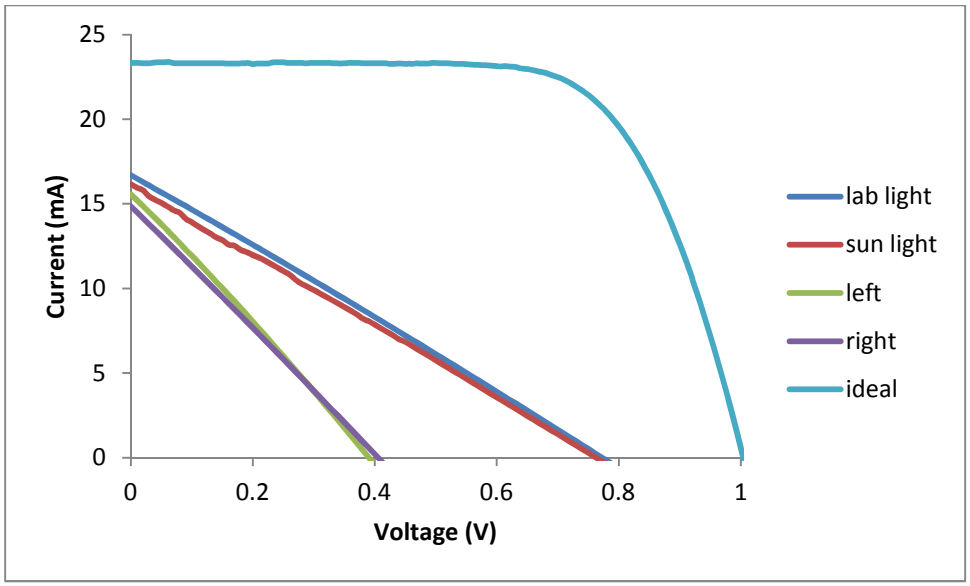


Figure 11: Current and voltage curves for wafer 3 in lab light, sunlight, and ideal

Table III: Critical Measurements for Wafer 3

	Voc (V)	Isc (mA)	Power (mW)	FF
lab light	0.7727	16.68	3.32	0.2578
sun light	0.7626	16.15	3.14	0.2550
left	0.3903	15.56	1.61	0.2647
right	0.4052	14.85	1.53	0.2544

Voltage and current did not vary a significant amount between the cells. The fill factor for all of the cells was around 0.25.

Silicon Island Design

There were some complications with the processing of the silicon island array. The TMAH did not etch in a uniform or consistent fashion. A test was done to ensure the etch rate of TMAH, and it was found to be very low, almost 10% of what it should be. Knowing this, the wafer was left in for much longer than it ended up needing. During this etching process though, the TMAH performed as it should, which resulted in more wafer being etched than was supposed to. Specifically, the back side of the wafer was etched far more than expected. This means that the top of the wafer etched all the way to the buried oxide layer, as it was supposed to, but so did the handle of the wafer. This left the wafer extremely brittle and broken in a few places. These

breaks resulted in the loss of one of the ten cells. However, as the topside ended up as intended, the array should have still worked properly.

Even though it was connected properly, there was no output voltage or current when tested as described in the previous section. At first, it seemed as if there was a disconnection between the traces wafer and the device wafer. However, it was discovered later that the wafer that was used only had a p-type bulk wafer, but an n-type top layer. This means an n-type dopant was used on an n-type wafer, which results in no junction and no band gap.

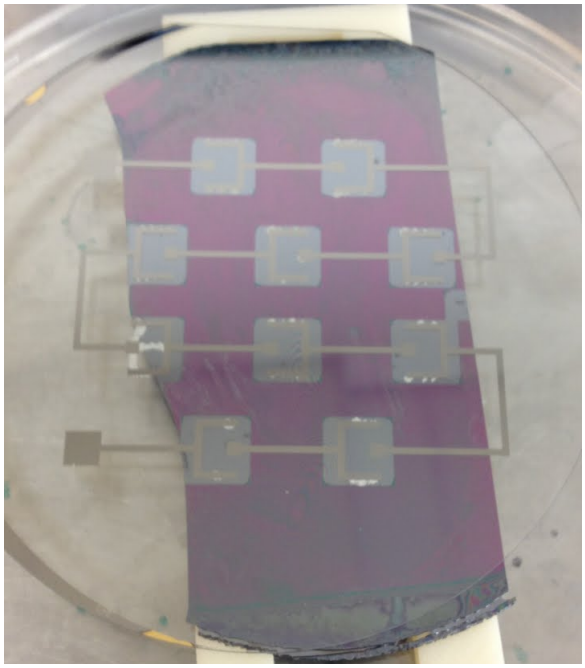


Figure 12: Final silicon island solar cell array

Discussion

Multi-Well Design

The data shows that the power output of the solar cells in the sun light was very similar to that in the lab. Wafer 3 was the only wafer in which the lab light was better than the sun light however, this can be attributed to the fact that wafer 3 was tested last and the position of the sun could have changed enough to cause these differences in measurements. In every single wafer the right side cell had a smaller short circuit. A possible explanation for the smaller short circuit current is that the mask for the interconnects has one of the “fingers” of the right cell 5.5 mm shorter than the rest.

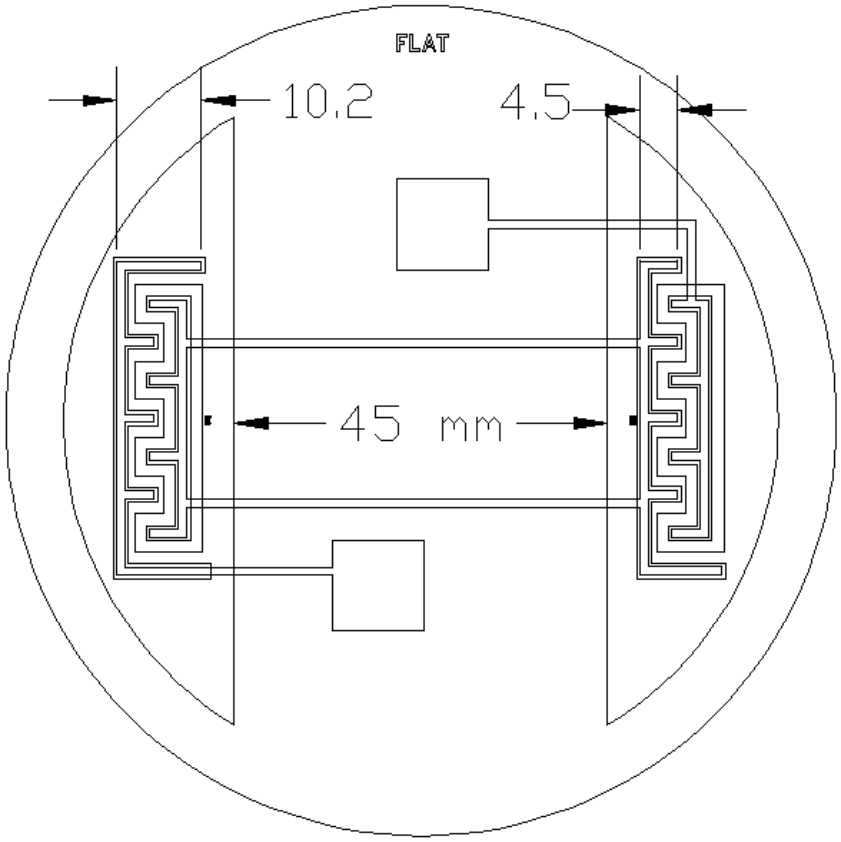


Figure 13: Final composite mask for 2-cell multi-well design

If this is the case, design of the interconnects, including number, length and thickness of the fingers, need to carefully planned in future iterations of the project.

Another concern is that the IV curve of the solar cell is not acting ideal. The IV curve has completely flatten out which is indicative of high series resistance and low shunt resistance. Since there is no nose of the curve we cannot calculate how much of the flattening is caused by low shunt resistance and how much is caused by high series resistance. Although it may seem that the low shunt resistance is inherent in this particular design because of the multiple wells, the same problem has been occurring in the previous projects. Even the single cell on a wafer design had problems with shunt resistance. One theory that could explain the leakage of current is the depletion region thickness might be too large. The larger the thickness of the depletion region of the p-n junction the more leakage can occur[5]. A thinner depletion region would allow for closer solar cell placing and therefore produce a higher total voltage.

Silicon Island Design

As mentioned in the results section, the process portion of the wafer was not severely affected and should have worked as intended, aside from the dopant discrepancy. Obviously, the correct dopant and wafer combination must be used in the future, regardless of which is which. Though a p-type wafer is preferable due to its lower resistivity, doping n-type wells with a p-type dopant will still create usable solar cells.

The TMAH deep etch step is another aspect that needs fine-tuning. There are a few ways that the islands can be left distinct while ensuring a sturdy solar cell. First, if the etch rate is properly characterized, the wafer can be etched for a short time and only etch through 10 µm on either side. This will leave the silicon islands exactly as they should be, while taking off only a small percent of the bulk wafer. Another option is to leave an oxide layer on the back half of the wafer that will protect it from the TMAH. This way, the wafer can be left in a longer time to ensure that the top is etched all the way through but that the bottom is not. Finally, a plasma etching process could be used in place of the wet etch process. Though plasma etching is usually used for small depths, proper parameters may be available to etch deeper with a high directional selectivity and while ignoring the back side of the SOI wafer.

While the connection of the traces wafer to the solar cells wafer was solid, it was a manual process done by hand and therefore prone to misalignment. It is prudent to note that great care must be taken in ensuring that the two wafers are correctly aligned when placing them together.

Conclusion

Multi-Well Design

As a proof of concept, this design was successful. Since the current design only allows for two solar cells on a wafer only a maximum voltage of 1 V can be theoretically achieved which is not sufficient to power an LED. However, the microfabrication lab at Cal Poly can only support processes on four inch wafers. In industry, twelve inch wafers are more commonly used. A twelve inch wafer would be able to hold twelve multi-well solar cells in series and be able to generate a voltage of 4.8 V.

The next step in this design is to add more solar cells onto a wafer to increase voltage and to investigate more efficient ways of collecting current. Some modeling of the design in software such as COMSOL would be helpful in understanding the sources of the possible high series and

low shunt resistance. A more reliable test for detecting the actual junction depth would be helpful in optimizing the depth for the current output.

Silicon Island Design

Few conclusions can be made from the silicon island design. The next step of this project is to fabricate it again while ensuring the proper dopant and wafer combination. The TMAH deep etch step also needs to change or be characterized in order to ensure that the bulk of the wafer does not end up needlessly fragile.

Appendix A: References

[1] Solarbuzz Website. *Solarbuzz| Portal to the World of Solar Energy*. Web. May 2012. <http://www.solarbuzz.com/moduleprices.htm>.

[2] “All About Chargers.” *Battery University*. Web. May 2012. <http://batteryuniversity.com/learn/article/all_about_chargers>.

[3] Kasap, Safa O. *Principles of Electronic Materials and Devices.* Boston: McGraw-Hill, 2006. Print. 420-553

[4] “Series Resistance” and “Shunt Resistance.” *Photovoltaic Education Network*. Web. May 2012. <http://pveducation.org/pvcdrom/solar-cell-operation/series-resistance> and <http://pveducation.org/pvcdrom/solar-cell-operation/shunt-resistance>.

[5]“Solar Cell Voltage-Current Characterization.” *California Scientific, Inc.* Web. May 2012. http://www.californiascientific.com/resource/Solar%20Cell.pdf.

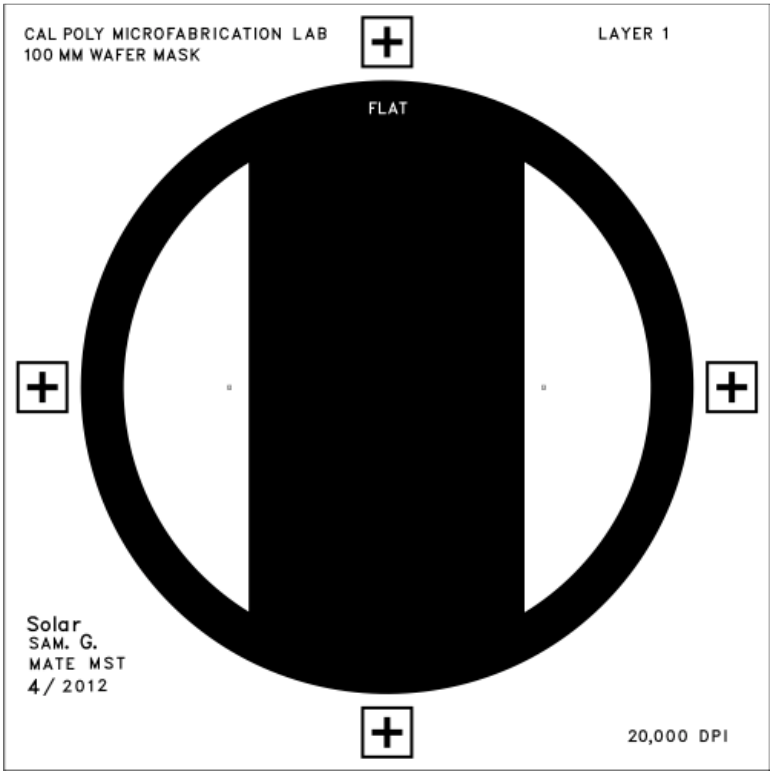
[6] Campbell, Stephen A. *Fabrication Engineering at the Micro and Nanoscale*. New York: Oxford UP, 2008. 40-440. Print.

[7] "NEI: Nuclear Energy Institute." *Nuclear Energy Institute*. Web. 08 Apr. 2012. <http://www.nei.org/resourcesandstats/documentlibrary/reliableandaffordableenergy/graphicsandcharts/uselectricityproductioncostsandcomponets/>

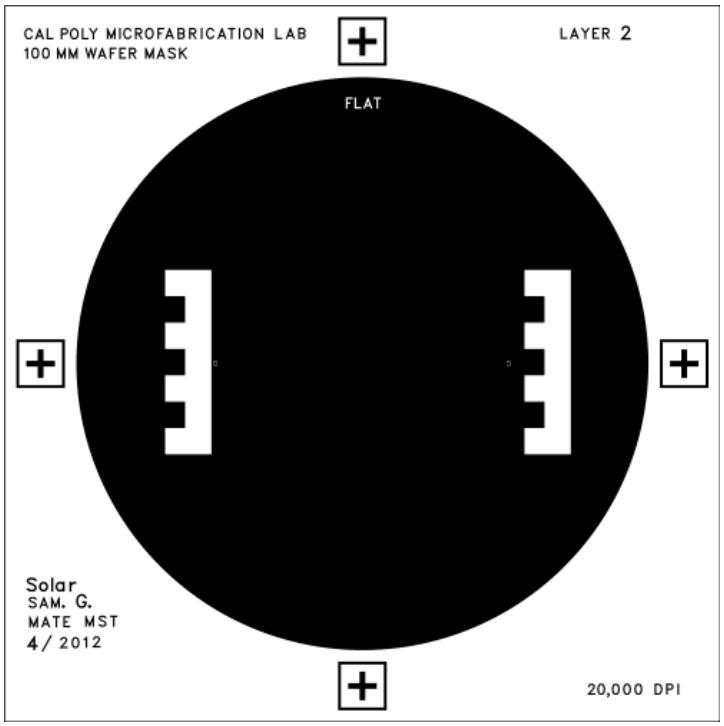
[8] Keller, S. et al. (2002) *U.S. Patent No. 6,441,297*. Washington, D.C: U.S.

Appendix B: Multi-Well Masks

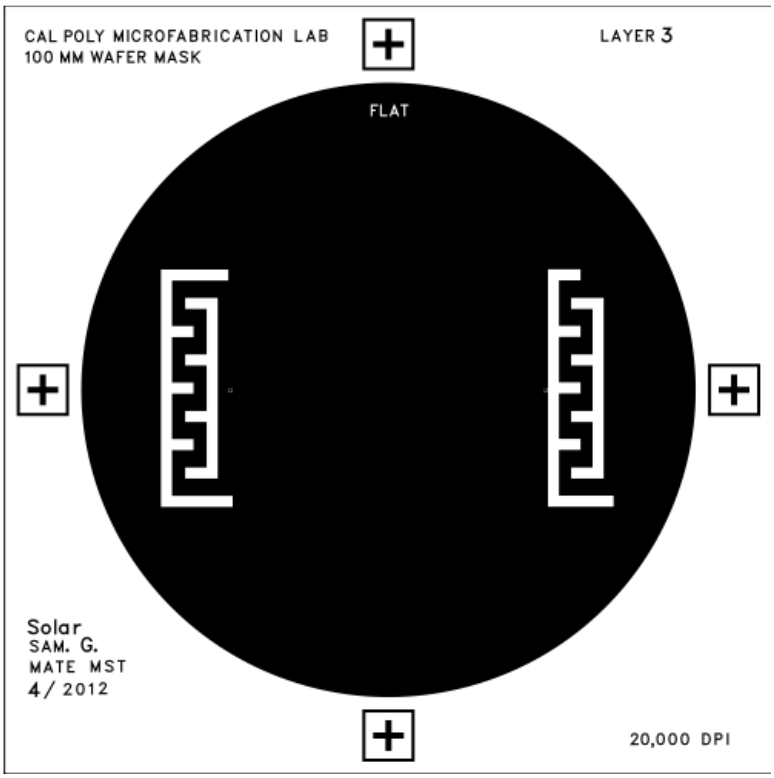
Diffusion Mask 1:



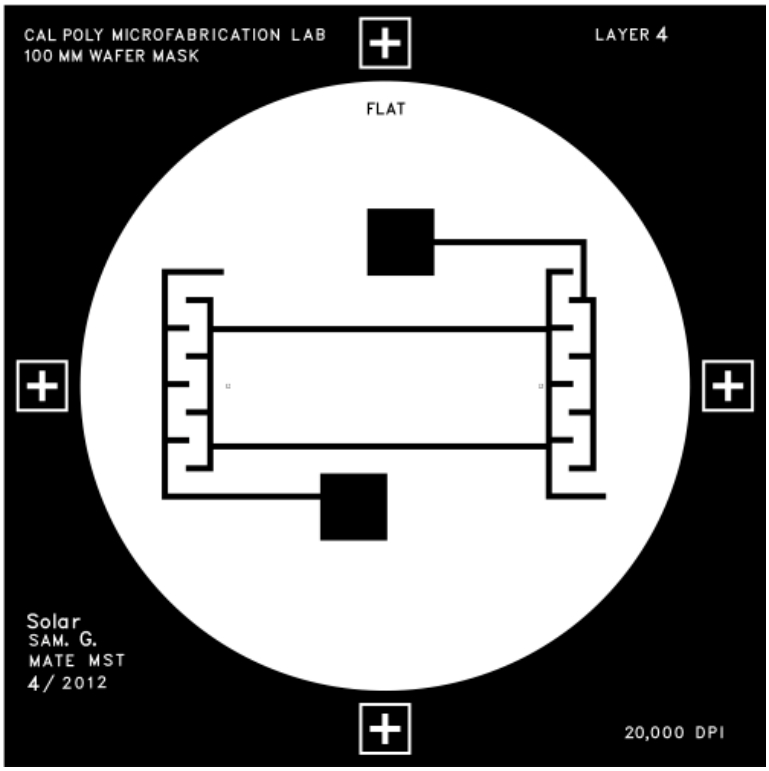
Diffusion Mask 2:



Oxide Mask:

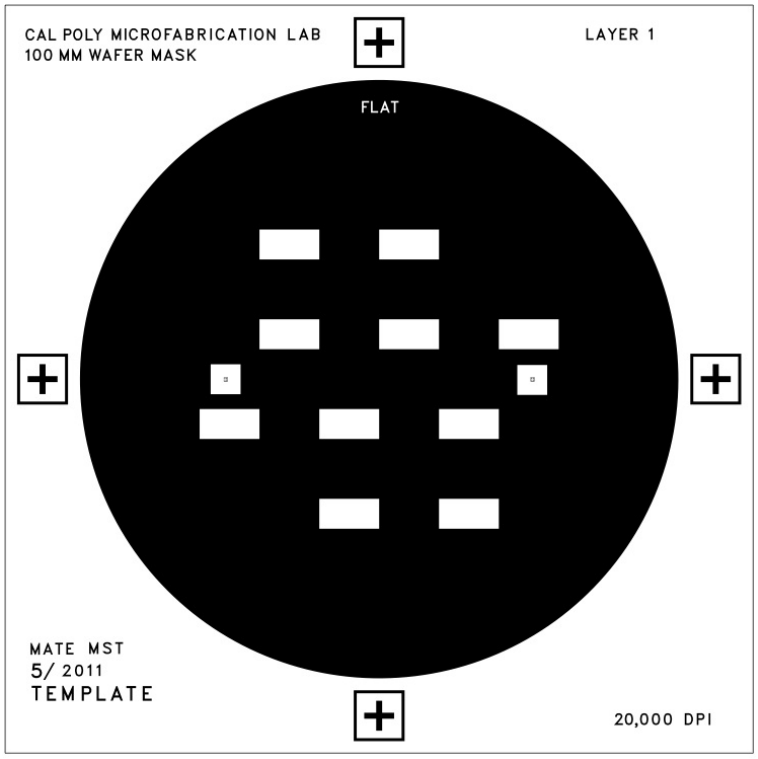


Traces Mask:

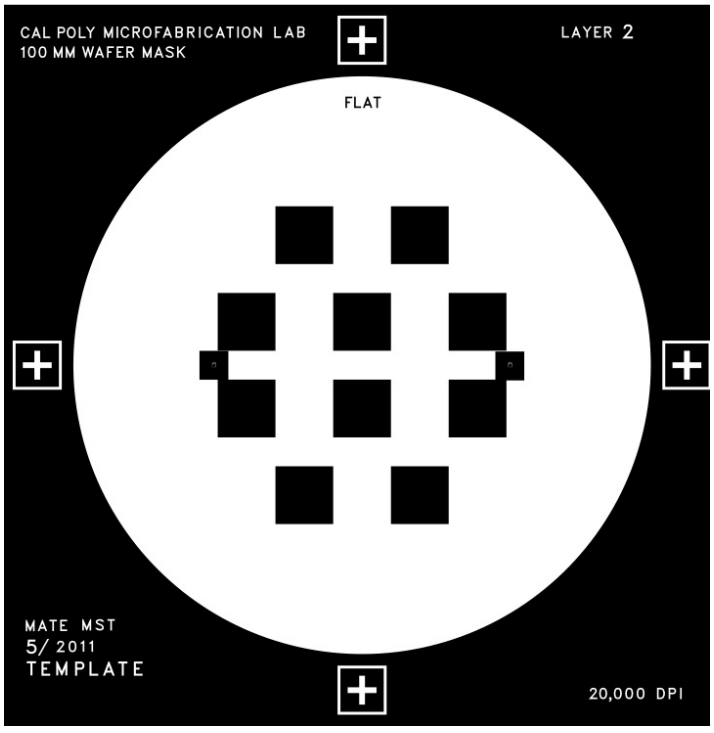


Appendix C: SILICON ISLAND Masks

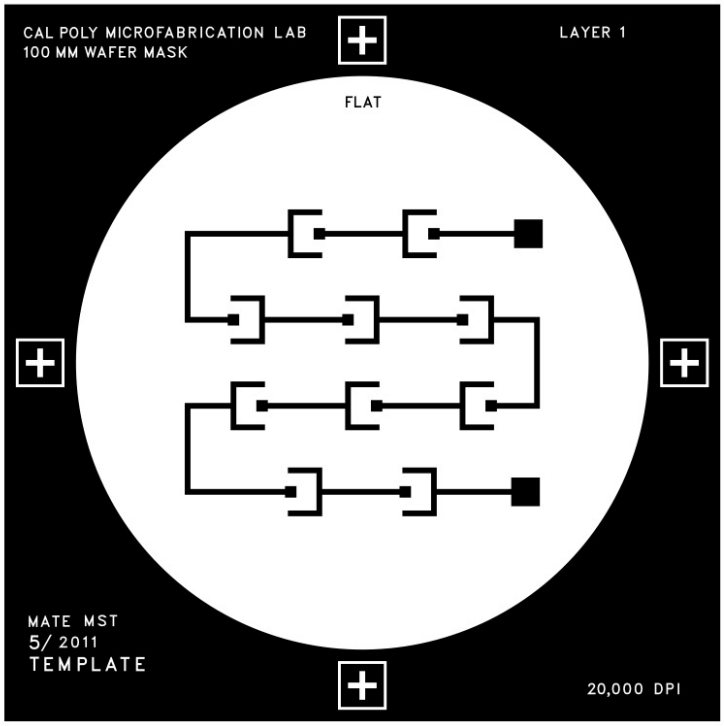
Diffusion Mask:



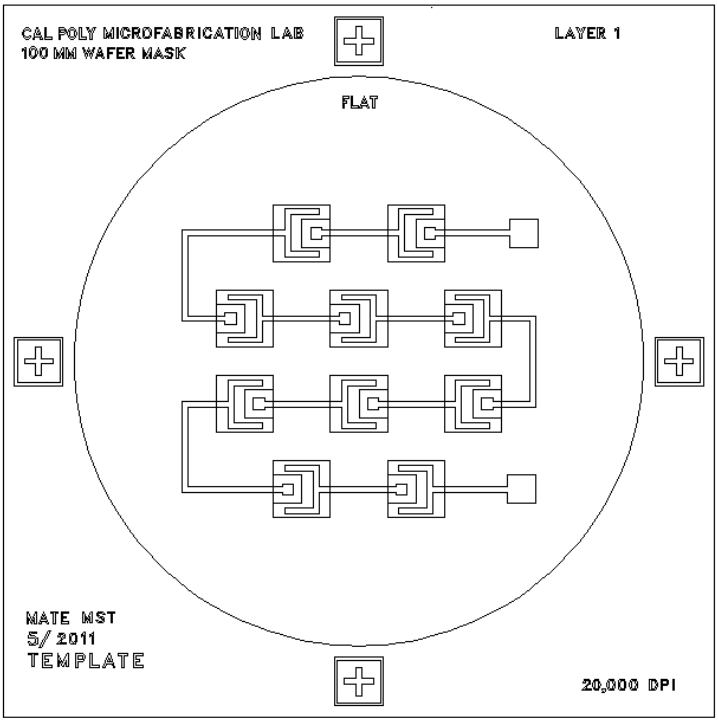
Etch Mask:



Metal Mask:



Composite of Finished Solar Array:



Appendix D: Multi-Well Processing Steps

1. Start with n-type wafer

   n-type

2. Grow an 800 nm oxide layer on wafer using the wet oxidation process at 1050°C for 2.5 hours.

   oxide

3. Pre-treat surface with Microchem MCC Primer. Spin coat with 5 ml photoresist up to 4000 RPM for 20 sec. Soft bake for 60 sec to drive off solvents

   Photoresist

4. Expose using mask 1- n-type diffusion mask with a light integral of 2.00 and developed for 2 min in Microposit MF-CD-26 developer

5. Etch oxide layer in BOE solution for 10 minutes at room temperature

6. Strip off photoresist layer with Shipley Microposit remover 1165 at 60°C for 5 min

7. Warm dopant to room temperature for 24 hours before use and spin on 4 mL of boron dopant (B_2O_3) up to 3000RPM for 20 sec.Diffuse Boron in furnace using dry oxygen atmosphere at 1050°C for 3 hours

p-type p-type

8. Etch off dopant oxide for 45 min in BOE at room temperature.

9. Grow another 800nm oxide layer using the wet oxidation process at 1050°C for 2.5 hours.

10. Pre-treat surface with Microchem MCC Primer. Spin coat with 5 ml photoresist up to 4000 RPM for 20 sec. Soft bake for 60 sec to drive off solvents

11. Expose using mask 2- p-type diffusion mask with a light integral of 2.00 and developed for 2 min in Microposit CD-26 developer

12. Etch oxide layer in BOE solution for 10 minutes at room temperature

13. Strip off photoresist layer with Shipley Microposit Remover 1165 at 60°C for 5 min

14. Warm dopant to room temperature for 24 hours before use and spin on 4 mL of phosphorous dopant up to 3000RPM for 20 sec. Diffuse Phosphorus in furnace using dry oxygen atmosphere at 1050°C for 1.5 hours

n-type n-type

15. Etch off dopant oxide for 45 min in BOE at room temperature.

16. Grow final 500nm oxide layer using the wet oxidation process at 1050°C for 1 hr. 7min.

17. Pre-treat surface with Microchem MCC Primer. Spin coat with 5 ml photoresist up to 4000 RPM for 20 sec. Soft bake for 60 sec to drive off solvents

18. Expose using mask 2- p-type diffusion mask with a light integral of 2.00 and developed for 2 min in Microposit CD-26 developer

19. Etch oxide layer in BOE solution for 10 minutes at room temperature

20. Strip off photoresist layer with Shipley Microposit Remover 1165 at 60°C for 5 min

21. Sputter gold using Denton Desk V sputter coater for 10min at 50 mA
    gold

22. Spin coat with 5 ml photoresist up to 4000 RPM for 20 sec. Soft bake for 60 sec to drive off solvents

23. Expose using mask 2- p-type diffusion mask with a light integral of 2.00 and developed for 2 min in Microposit CD-26 developer

24. Etch Gold for 1 min in gold etchant

25. Strip off photoresist layer with Shipley Microposit Remover 1165 at 60°C for 5 min
    gold
    oxide
    n-type
    n-type
    p-type
    p-type

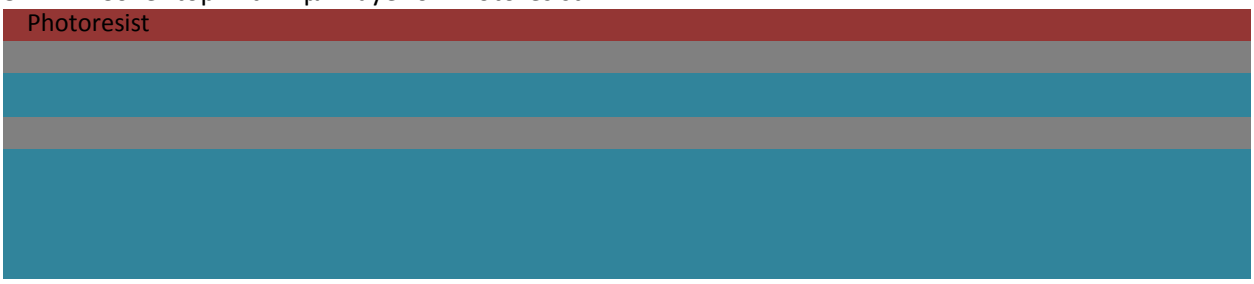
    n-type

Appendix E: Silicon Island Processing Steps

1. Start with a SOI wafer with a buried oxide layer 10 µm deep.

2. Grow a 6000 µm oxide layer on wafer. This is done in with a wet oxide growth process in a 1050˚C furnace for 1.5 hours.

3. Cover top with 1 µm layer of Photoresist.



4. Expose using Diffusion Mask with a light integral of 2.00 and develop for 2.5 minutes in a CD-26 developer solution.

5. Etch oxide layer in BOE solution for 8 minutes at room temperature.

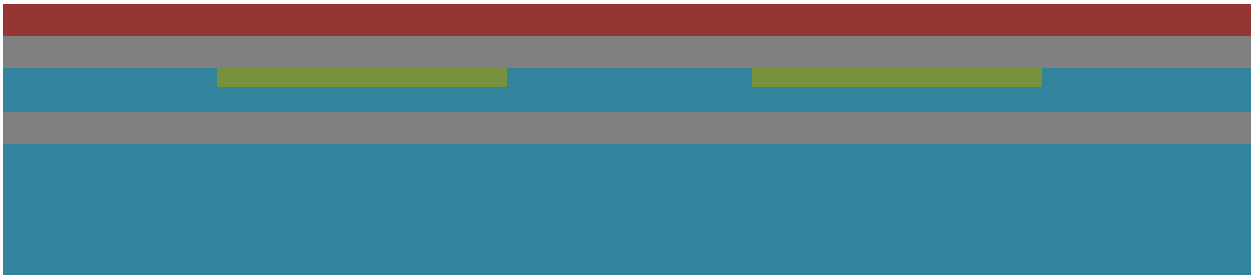
6. Strip off Photoresist layer with Microposit Remover 1165 at 50˚C for 10 minutes.

7. Spin on phosphorus dopant. Carry out pre-deposition in nitrogen rich atmosphere at 1050˚C for 1.5 hours.

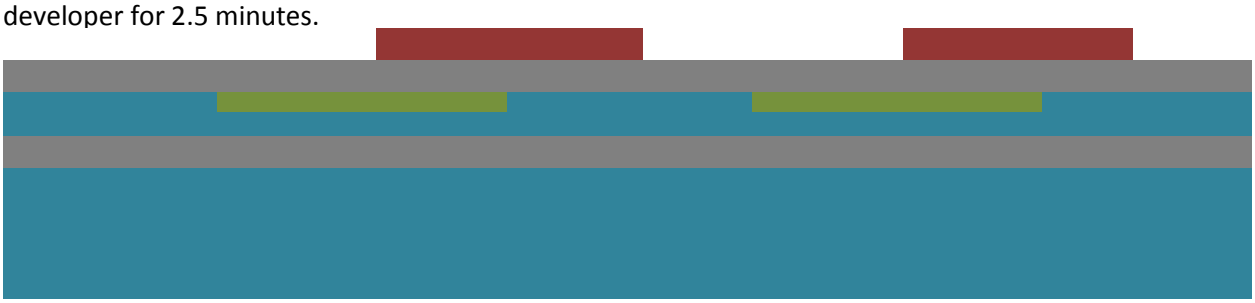
8. Etch off dopant oxide from wafer in BOE. Since there is no danger of over etching, leave in solution for 1.5 hours at room temperature.

9. Grow another 6000 µm oxide layer using a wet oxide process at 1050˚C for 1.5 hours.

10. Spin on another 1 µm layer of Photoresist.



11. Expose Photoresist layer to the Etch Mask with a light integral of 2.00 and develop in CD-26 developer for 2.5 minutes.



12. Etch through oxide layer with room temperature BOE for 8 minutes.

13. Strip off Photoresist with Microposit Remover 1156 at 50˚C for 10 minutes.

14. Deep etch silicon in 25% TMAH for 40 minutes.

15. Strip off oxide layer in room temperature BOE for 8 minutes.

16. For traces wafer, start with a SiO_2 wafer.

17. Deposit titanium thin film adhesion layer on glass wafer.

18. Deposit 1.9 µm gold thin film on the titanium layer.

19. Spin 1 µm layer of Photoresist on top of the gold layer.

20. Expose the Photoresist to Trace Mask with a light integral of 2.00 and develop for 2.5 minutes in CD-26 developer.

21. Etch through the gold film using a gold etchant solution, immediately followed by etching the titanium layer in a titanium etchant solution.

22. Strip off Photoresist in Microposit Remover 1156 at 50˚C for 10 minutes.

23. Finally, connect traces wafer to solar cell wafer using silver filled epoxy.