Cal Poly SuPER System Photovoltaic Array
Universal DC-DC Step Down Converter

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Presented to the Faculty of
California Polytechnic State University,
San Luis Obispo

In Partial Fulfillment
of the Requirements for the Degree of
Master of Science in Electrical Engineering

by
Joseph Witts
June 2008

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Abstract

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Standard converter topologies are usually presented with a voltage source as the input supply to the converters. However, a photovoltaic (PV) array has the I-V characteristics of a current source not a voltage source. This thesis details the design process of modifying the standard Buck and synchronous Buck converter topologies to function with either a voltage or current source input, making them universal DC-DC step down converters. This is accomplished by placing a capacitor at the converter's input to supply the pulsating current required for the Buck topologies to function properly. The equations for determining the capacitor's size and RMS current rating are derived, and a prototype of each topology was constructed and analyzed. Also, the issues that arose during the integration of the converter's into the SuPER system are discussed.

The Cal Poly Sustainable Power for Electrical Resources (SuPER) project seeks to build a stand alone photovoltaic (PV) unit that can supply the energy needs of a single family home. Before the start of this thesis the SuPER project was using an off-the-shelf DC-DC converter to step down the PV array's voltage, perform maximum power point tracking, and act as a charge controller for the battery. One goal of the project is to have a Cal Poly built DC-DC converter that can perform all the functions of the off-the-shelf DC-DC converter currently being used.

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Table of Contents

List of Figures	ix
List of Tables	xiii
Chapter 1: Introduction	1
1.1 The SuPER Project	1
1.2 Personal Involvement.....	1
1.3 Photovoltaic Array I-V Characteristics.....	1
1.5 Thesis Objectives	2
1.6 Document Overview	3
Chapter 2: Buck Converter	5
2.1 Buck Converter Current Voltage Relationship	5
2.1.1 Switch Turned On	6
2.1.2 Switch Turned Off	7
2.1.3 Critical Component Values.....	8
2.2 Ideal Buck Converter Design.....	11
2.2.1 Parameters.....	11
2.2.2 Inductor Calculation.....	12
2.2.3 Capacitor Calculation.....	13
2.2.4 Diode and Switch.....	13
2.3 Ideal PSpice Simulation.....	13
2.3.1 Simulation at Ten Percent Load.....	14
2.3.2 Theoretical and Simulation Comparison	16
2.4 Standard Topology Limitations	16
2.4.1 Voltage Source Input	17
2.4.2 Current Source Input.....	17
Chapter 3: Universal Buck Converter.....	18
3.1 Input Capacitor Derivation	18
3.2 Ideal Universal Buck Converter Design	20
3.2.1 Inductor Current Values at Full Load	21
3.2.2 Input Capacitor.....	21
3.3 Ideal PSpice Simulation.....	22
3.3.1 Simulation at Full Load	22
3.3.2 Theoretical and Simulation Comparison	25
3.4 Component Selection for Actual Design	25
3.4.1 MOSFET.....	25
3.4.2 Gate Driver.....	26
3.4.3 PIC to Gate Driver Interface	27
3.4.4 Inductor	28
3.4.5 Capacitors	28
3.4.6 Freewheeling Diode	29
3.5 Theoretical Efficiency.....	31
3.5.1 MOSFET Switching Losses.....	31
3.5.2 MOSFET Conduction Losses	32
3.5.3 MOSFET Gate Losses	32
3.5.4 Diode Conduction Losses	33

3.5.4 Inductor Losses	33
3.5.5 Theoretical Efficiency Calculation	34
3.6 Heat Sink Calculation	35
3.6.1 MOSFET	35
3.6.2 Diode	37
3.7 Modification for Battery Load	38
3.8 Universal Buck Converter Prototype Testing	39
3.8.1 Test Setup	40
3.8.2 Different Converter Configuration Noise Results	41
3.8.3 Efficiency	42
Chapter 4: Universal Synchronous Buck Converter	44
4.1 Component Selection	44
4.1.1 Gate Driver	45
4.1.2 Inductor	47
4.1.3 Input Capacitor	48
4.2 Modification for Battery Load	48
4.3 Theoretical Efficiency	49
4.3.1 High Side MOSFET Switching Losses	49
4.3.2 High Side MOSFET Conduction Losses	50
4.3.3 Low Side MOSFET Switching Losses	50
4.3.4 Low Side MOSFET Conduction Losses	50
4.3.5 MOSFET Gate Losses	50
4.3.6 Freewheeling Diode Conduction Losses	50
4.3.7 Inductor Losses	51
4.3.8 Output Diode Conduction Losses	51
4.3.9 Theoretical Efficiency Calculation	52
4.4 Heat Sink Calculations	53
4.4.1 High Side MOSFET	53
4.4.2 Output Diode	54
4.5 Universal Synchronous Buck Converter Prototype Testing	54
4.5.1 Test Setup	55
4.5.2 Different Converter Configuration Noise Results	55
4.5.3 Efficiency	56
4.5.4 Efficiency Comparison with Universal Buck Converter	58
Chapter 5: Converter Implementation into SuPER	59
5.1 SuPER Control System as Found	59
5.2 Simulink Simulation Control Code	60
5.2.1 Implementation	60
5.2.2 Results	62
5.3 Improved Control Algorithm	63
5.3.1 Improvements	63
5.3.2 Results	64
5.3.3 Converter Control Code Difference	65
Chapter 6: Conclusion	66
6.1 Achievements	66
6.2 Future Recommendations	67

Bibliography	70
Appendix A: Universal Buck Converter Testing Configuration 1	73
A.1 No Load Waveforms.....	73
A.2 Full Load Waveforms	75
Appendix B: Universal Buck Converter Testing Configuration 2.....	81
B.1 Full Load Waveforms.....	81
Appendix C: Universal Buck Converter Testing Configuration 3.....	87
C.1 No Load Waveforms	87
C.2 Full Load Waveforms.....	89
Appendix D: Universal Buck Converter Testing Configuration 4	94
D.1 Full Load Waveforms	94
Appendix E: Universal Buck Converter Testing Configuration 5.....	98
E.1 No Load Waveforms	98
E.2 Full Load Conditions.....	98
Appendix F: Universal Buck Converter Testing Configuration 6.....	103
F.1 No Load Waveforms.....	103
F.2 Full Load Condition.....	104
Appendix G: Universal Buck Converter Testing Configuration 7	108
G.1 No Load Waveforms.....	108
G.2 Full Load Waveforms	109
G.3 Battery Load Waveforms	112
Appendix H: Universal Synchronous Buck Converter Testing Configuration 1	114
H.1 No Load Waveforms.....	114
H.2 Full Load Waveforms	118
Appendix I: Universal Synchronous Buck Converter Testing Configuration 2	125
I.1 No Load Waveforms	125
I.2 Full Load Waveforms.....	130
Appendix J: Universal Synchronous Buck Converter Testing Configuration 3.....	137
J.1 No Load Waveform.....	137
J.2 Full Load Waveforms.....	138
Appendix K: Universal Synchronous Buck Converter Testing Configuration 4	146
K.1 Full Load Waveforms	146
Appendix L: Analysis of Senior Project Design.....	150
L.1 Summary of Functional Requirements.....	150
L.2 Primary Constraints	150
L.3 Economics	151
L.4 Manufacturing on a Commercial Basis	153
L.5 Environmental	154
L.6 Manufacturability	154
L.7 Sustainability	154
L.8 Ethical.....	155
L.9 Health and Safety	155
L.10 Social and Political	155
L.11 Development.....	155

List of Figures

Figure 1.1 – BP SX 150 I-V Characteristics [2]	2
Figure 2.1 – Buck Converter Topology	5
Figure 2.2 – Buck Converter Circuit when Switch is On	7
Figure 2.3 – Buck Converter Circuit when Switch is Off.....	8
Figure 2.4 – 10% Load Simulation with Voltage Source Input.....	14
Figure 2.5 – Output Voltage Ripple and Average Value.....	14
Figure 2.6 – Current in S2 Representing Diode Current	15
Figure 2.7 – Current in S1 Representing Input Current.....	15
Figure 2.8 – Average Current Values	15
Figure 2.9 – Inductor and Capacitor Current.....	16
Figure 3.1 – Universal Buck Converter	18
Figure 3.2 – Universal Buck Converter Circuit when Switch is On.....	19
Figure 3.3 – Universal Buck Converter Circuit when Switch is Off.....	19
Figure 3.4 – Ideal Universal Buck Converter at Full Load.....	22
Figure 3.5 – Average Output Voltage and Ripple at Full Load.....	23
Figure 3.6 – Inductor and Capacitor Ripple Current at Full Load.....	23
Figure 3.7 – Average Current Values	23
Figure 3.8 – Input Capacitor, Switch, and Current Source Current.....	24
Figure 3.9 – Input Capacitor RMS Current	24
Figure 3.10 – Average Input Capacitor Voltage and Ripple	24
Figure 3.11 – IRS2117 High Side Gate Driver [8]	27
Figure 3.12 – MM74C906N Open Drain Buffer [9].....	28
Figure 3.13 – MBR2045CT Pin Connections [11]	30
Figure 3.14 – MBR2045CT Diode Current Voltage Characteristics Per Leg [11]	30
Figure 3.15 – MOSFET's V_{GS} vs. Q_G Curve [13]	33
Figure 3.16 – MOSFET Thermal Model without Heatsink.....	36
Figure 3.17 – MOSFET Thermal Model with Heatsink	37
Figure 3.18 – Diode Thermal Model with Heatsink.....	38
Figure 3.19 – Modification for Battery Load [20].....	39
Figure 3.20 – Universal Buck Converter Prototype Schematic.....	40
Figure 3.21 – Universal Buck Converter Efficiency Comparison.....	43
Figure 4.1 – Universal Synchronous Buck Converter	44
Figure 4.2 – IRS2003 Gate Driver [22]	46
Figure 4.3 – IRS2004 Gate Driver [23]	46
Figure 4.5 – Universal Synchronous Buck Converter Prototype Schematic.....	55
Figure 4.6 - Universal Synchronous Buck Converter Efficiency Comparison.....	57
Figure 4.7 – Converter Prototypes Efficiency Comparison.....	58
Figure 5.1 – Simulink Control Code Flowchart.....	62
Figure 5.2 – Improved Control Code Flowchart.....	64
Figure A.1 – V_{gate} Rise Time (Ch 1) and V_{out} (Ch 2).....	73
Figure A.2 – V_{gate} Fall Time (Ch 1) and V_{out} (Ch 2)	74
Figure A.3 – V_{gate} (Ch1) and V_{out} (Ch 2) During MOSFET Turn On	74

Figure A.4 – V_{gate} (Ch1) and V_{out} (Ch 2) During MOSFET Turn Off.....	75
Figure A.5 – V_{gate} Measurement (Ch 1) and V_{out} (Ch 2)	76
Figure A.6 – V_{gate} (Ch 1) and V_{out} Measurement (Ch 2)	76
Figure A.7 – V_{gate} (Ch 1) and Zoomed in V_{out} (Ch 2).....	77
Figure A.8 – V_{gate} (Ch 1) and Gate Driver PWM Input (Ch 2)	77
Figure A.9 – V_{gate} (Ch 1) and V_{diode} Undershoot (Ch 2).....	78
Figure A.10 – V_{gate} (Ch 1) and V_{diode} Overshoot (Ch 2).....	78
Figure A.11 – MOSFET Drain Voltage (Ch 1) and MOSFET Source Voltage (Ch 2)....	79
Figure A.12 – V_{DS} Turn On Undershoot.....	79
Figure A.13 – V_{DS} Turn Off Overshoot.....	80
Figure B.1 – V_{gate} Measurements (Ch1) and V_{out} (Ch 2).....	82
Figure B.2 – V_{gate} (Ch1) and V_{out} Measurements (Ch 2) with Snubber.....	82
Figure B.3 – V_{gate} (Ch1) and V_{out} Zoomed In (Ch 2).....	83
Figure B.4 – V_{gate} (Ch1) and V_{diode} Turn On Undershoot (Ch 2).....	83
Figure B.5 – V_{gate} (Ch1) and V_{diode} Turn Off Overshoot (Ch 2).....	84
Figure B.6 – MOSFET Drain Voltage (Ch 1) and MOSFET Source Voltage (Ch 2).....	84
Figure B.7 – MOSFET Drain Voltage (Ch 1) and.....	85
Figure B.8 – V_{DS} Turn On Undershoot.....	85
Figure B.9 – V_{DS} Turn Off Overshoot	86
Figure C.1 – V_{gate} Rise Time (Ch 1) and V_{out} (Ch 2).....	87
Figure C.2 – V_{gate} Fall Time (Ch 1) and V_{out} (Ch 2).....	88
Figure C.3 – V_{gate} (Ch1) and V_{out} Noise (Ch 2) During MOSFET Turn On	88
Figure C.4 – V_{gate} (Ch1) and V_{out} Noise (Ch 2) During MOSFET Turn Off.....	89
Figure C.5 – V_{gate} Measurements (Ch1) and V_{out} (Ch 2).....	90
Figure C.6 – V_{gate} (Ch1) and V_{out} Measurements (Ch 2).....	90
Figure C.7 – V_{gate} (Ch1) and V_{out} Zoomed In (Ch 2).....	91
Figure C.8 – V_{gate} (Ch 1) and Gate Driver PWM Input (Ch 2).....	91
Figure C.9 – V_{gate} (Ch1) and V_{diode} (Ch 2).....	92
Figure C.10 – MOSFET Drain Voltage (Ch 1) and MOSFET Source Voltage (Ch 2)....	92
Figure C.11 – V_{DS} Turn On Undershoot.....	93
Figure C.12 – V_{DS} Turn Off Overshoot	93
Figure D.1 – V_{gate} (Ch1) and V_{out} Measurements (Ch 2).....	95
Figure D.2 – V_{gate} (Ch1) and V_{out} Zoomed In (Ch 2)	95
Figure D.3 – V_{gate} (Ch1) and V_{diode} Turn Off Overshoot (Ch 2).....	96
Figure D.4 – MOSFET Drain Voltage (Ch 1) and MOSFET Source Voltage (Ch 2).....	96
Figure D.5 – V_{DS} Turn On Undershoot.....	97
Figure D.6 – V_{DS} Turn Off Overshoot.....	97
Figure E.1 – V_{gate} (Ch1) and V_{out} (Ch 2) No Load	98
Figure E.2 – V_{gate} (Ch1) and V_{out} Measurements (Ch 2)	99
Figure E.3 – V_{gate} (Ch1) and V_{out} Zoomed In (Ch 2).....	100
Figure E.4 – V_{gate} (Ch1) and V_{diode} Turn Off Overshoot (Ch 2).....	100
Figure E.5 – MOSFET Drain Voltage (Ch 1) and MOSFET Source Voltage (Ch 2)....	101
Figure E.6 – V_{DS} Turn On Undershoot.....	101
Figure E.7 – V_{DS} Turn Off Overshoot	102
Figure F.1 – V_{gate} (Ch1) and V_{out} Measurements (Ch 2)	103
Figure F.3 – V_{gate} (Ch1) and V_{out} Zoomed In (Ch 2)	105

Figure F.4 – V_{gate} (Ch1) and V_{diode} Turn Off Overshoot (Ch 2)	105
Figure F.5 – MOSFET Drain Voltage (Ch 1) and MOSFET Source Voltage (Ch 2)	106
Figure F.6 – V_{DS} Turn On Undershoot	106
Figure F.7 – V_{DS} Turn Off Overshoot.....	107
Figure G.1 – V_{gate} (Ch1) and V_{out} (Ch 2) No Load	108
Figure G.2 – V_{gate} (Ch1) and V_{out} (Ch 2)	109
Figure G.3 – V_{gate} (Ch1) and V_{diode} Turn Off Overshoot (Ch 2).....	110
Figure G.4 – MOSFET Drain Voltage (Ch 1) and MOSFET Source Voltage (Ch 2)....	110
Figure G.5 – V_{DS} Turn On Undershoot.....	111
Figure G.6 – V_{DS} Turn Off Overshoot.....	111
Figure G.7 – Bootstrap Capacitor Voltage (Ch 1) and V_{out} (Ch 2).....	113
Figure G.8 – Bootstrap Capacitor Voltage (Ch 1) and V_{out} (Ch 2).....	113
Figure H.1 – V_{gate} High Side Noise (Ch 1) and V_{gate} Low Side (Ch 2)	115
Figure H.2 – V_{gate} High Side (Ch 1) and V_{gate} Low Side Noise (Ch 2)	115
Figure H.3 – V_{gate} High Side (Ch 1) and V_{gate} Low Side (Ch 2) During PWM High.....	116
Figure H.4 – V_{gate} High Side (Ch 1) and V_{gate} Low Side (Ch 2) During PWM Low	116
Figure H.5 – V_{gate} High Side (Ch 1) and V_{out} Peak Oscillation (Ch 2).....	117
Figure H.6 – V_{gate} High Side (Ch 1) and V_{out} Oscillation Frequency (Ch 2).....	117
Figure H.7 – V_{gate} High Side Rise Time (Ch 1) and V_{out} (Ch 2)	118
Figure H.8 – V_{gate} High Side Fall Time (Ch 1) and V_{out} (Ch 2)	118
Figure H.9 – V_{gate} High Side Measurements (Ch 1) and V_{out} (Ch 2).....	119
Figure H.10 – V_{gate} High Side (Ch 1) and V_{out} Measurements (Ch 2).....	120
Figure H.11 – V_{gate} High Side (Ch 1) and V_{out} Measurements (Ch 2).....	120
Figure H.12 – V_{gate} High Side (Ch 1) and Gate Driver PWM Input (Ch 2)	121
Figure H.13 – V_{gate} Low Side (Ch 1) and Gate Driver PWM Input (Ch 2).....	121
Figure H.14 – V_{gate} High Side (Ch 1) and V_{diode} (Ch 2)	122
Figure H.15 – V_{gate} Low Side (Ch 1) and V_{diode} (Ch 2).....	122
Figure H.16 – High Side Drain Voltage (Ch 1) and High Side Source Voltage (Ch 2). ..	123
Figure H.17 – High Side V_{ds} Turn On Undershoot	123
Figure H.18 – High Side V_{ds} Turn Off Overshoot.....	124
Figure I.1 – V_{gate} High Side Turn Off Noise (Ch 1) and V_{gate} Low Side (Ch 2)	126
Figure I.2 – V_{gate} High Side (Ch 1) and V_{gate} Low Side Turn On Noise (Ch 2)	126
Figure I.3 – V_{gate} High Side (Ch 1) and V_{gate} Low Side (Ch 2) During PWM High	127
Figure I.4 – V_{gate} High Side (Ch 1) and V_{gate} Low Side (Ch 2) During PWM Low	127
Figure I.5 – V_{gate} High Side (Ch 1) and V_{out} Peak Oscillation (Ch 2)	128
Figure I.6 – V_{gate} High Side (Ch 1) and V_{out} Peak Oscillation Frequency (Ch 2)	128
Figure I.7 – V_{gate} High Side Rise Time(Ch 1) and V_{out} (Ch 2)	129
Figure I.8 – V_{gate} High Side Fall Time (Ch 1) and V_{out} (Ch 2).....	129
Figure I.9 – V_{gate} High Side Measurements (Ch 1) and V_{out} (Ch 2)	131
Figure I.10 – V_{gate} High Side (Ch 1) and V_{out} Measurements (Ch 2)	131
Figure I.11 – V_{gate} High Side (Ch 1) and Gate Driver PWM Input (Ch 2).....	132
Figure I.12 – V_{gate} Low Side (Ch 1) and Gate Driver PWM Input (Ch 2).....	132
Figure I.13 – V_{gate} High Side Measurements (Ch 1) and V_{diode} Undershoot (Ch 2)	133
Figure I.14 – V_{gate} High Side Measurements (Ch 1) and V_{diode} Overshoot (Ch 2)	133
Figure I.15 – Low Side Gate Voltage Undershoot (Ch 1) and V_{diode} (Ch 2)	134
Figure I.16 – V_{gate} Low Side Noise (Ch 1) and V_{diode} (Ch 2)	134

Figure I.17 – High Side Drain Voltage (Ch 1) and High Side Source Voltage (Ch 2)...	135
Figure I.18 – High Side V_{ds} Turn On Undershoot	135
Figure I.19 – High Side V_{ds} Turn Off Overshoot	136
Figure J.1 – V_{gate} High Side (Ch 1) and V_{out} Oscillation (Ch 2).....	137
Figure J.2 – V_{gate} High Side (Ch 1) and V_{out} Peak Noise (Ch 2)	138
Figure J.3 – V_{gate} High Side (Ch 1) and V_{out} (Ch 2)	139
Figure J.4 – V_{gate} High Side (Ch 1) and V_{out} Zoomed In (Ch 2) During PWM High.....	140
Figure J.5 – V_{gate} High Side (Ch 1) and V_{out} (Ch 2) High Side Gate Turn Off Noise	140
Figure J.6 – V_{gate} High Side (Ch 1) and Gate Driver PWM Input (Ch 2).....	141
Figure J.7 – V_{gate} Low Side (Ch 1) and Gate Driver PWM Input (Ch 2)	141
Figure J.8 – V_{gate} High Side (Ch 1) and V_{diode} Turn On Undershoot (Ch 2)	142
Figure J.9 – V_{gate} High Side (Ch 1) and V_{diode} Turn Off Overshoot (Ch 2).....	142
Figure J.10 – V_{gate} Low Side Noise (Ch 1) and V_{diode} (Ch 2) During Diode Turn Off...	143
Figure J.11 – V_{gate} Low Side Noise (Ch 1) and V_{diode} (Ch 2) During Diode Turn On ...	143
Figure J.12 – High Side Drain Voltage (Ch 1) and High Side Source Voltage (Ch 2) ..	144
Figure J.13 – High Side V_{ds} Turn On Undershoot.....	144
Figure J.14 – High Side V_{ds} Turn Off Overshoot	145
Figure K.1 – V_{gate} High Side Undershoot (Ch 1) and V_{out} (Ch 2)	147
Figure K.2 – V_{gate} High Side (Ch 1) and V_{out} Noise (Ch 2) During PWM High.....	147
Figure K.3 – V_{gate} High Side (Ch 1) and V_{out} Noise (Ch 2) During PWM Low	148
Figure K.4 – V_{gate} High Side (Ch 1) and V_{diode} Turn On Undershoot (Ch 2)	148
Figure K.5 – V_{gate} High Side (Ch 1) and V_{diode} Turn Off Overshoot (Ch 2)	149
Figure K.6 – V_{out} (Ch 1) and V_{diode} (Ch 2).....	149

List of Tables

Table 1.1 – Initial DC-DC Converter Specifications [3]	3
Table 1.2 – Modified DC-DC Converter Specifications	3
Table 2.1 – Buck Converter Data Comparison	16
Table 3.1 – Universal Buck Converter Data Comparison	25
Table 3.2 – Universal Buck Converter Theoretical Efficiency.....	34
Table 3.3 – Thermal Elements and Analogous Electrical Element [10].....	35
Table 3.4 – Universal Buck Noise Data Table	42
Table 3.5 – Universal Buck Testing Configurations	42
Table 3.6 – Universal Buck Converter Prototype Efficiency Data.....	43
Table 4.1 – Universal Synchronous Buck Converter Theoretical Efficiency.....	53
Table 4.2 – Universal Synchronous Buck Noise Data Table.....	56
Table 4.3 – Universal Synchronous Buck Testing Configurations.....	56
Table 4.4 – Actual Universal Synchronous Buck Converter Efficiency Data.....	57
Table A.1 – Full Load Conditions for Configuration 1	76
Table B.1 – Full Load Conditions for Configuration 2	81
Table C.1 – Full Load Condition for Configuration 3	90
Table D.1 – Full Load Conditions for Configuration 4	94
Table E.1 – Full Load Conditions for Configuration 5.....	99
Table F.1 – Full Load Conditions for Configuration 6.....	104
Table G.1 – Full Load Conditions for Configuration 7	109
Table G.2 – Condition for Charging Motorcycle Battery.....	112
Table H.1 – Full Load Conditions for Configuration 1	119
Table I.1 – Full Load Conditions for Configuration 2.....	130
Table J.1 – Full Load Conditions for Configuration 3.....	139
Table K.1 – Full Load Conditions for Configuration 4	146
Table L.1 – Universal Buck Converter Component List	152
Table L.2 – Miscellaneous Universal Buck Converter Components.....	152
Table L.3 – Universal Synchronous Buck Converter Components.....	153
Table L.4 – Miscellaneous Universal Synchronous Buck Converter Components.....	153

Chapter 1: Introduction

1.1 The SuPER Project

In 2005 the idea of the Sustainable Power for Electrical Resources (SuPER) project was introduced by Dr. James Harris's white paper [1], with the goal to develop a low cost sustainable source of electrical power to families in underdeveloped countries. It consists of a photovoltaic (PV) array for electricity generation, battery for energy storage, digital control system to perform maximum power point tracking (MPPT) and battery charge control, and various DC loads.

1.2 Personal Involvement

In fall of 2006 I was first introduced to the SuPER project while trying to determine what I was going to do for my senior project. I was initially tasked with attaching an ultra-capacitor across battery, but also took on the task of developing a model of the DC motor to be used for computer simulations. While working on the project several groups attempted to develop a DC-DC converter to step down the PV array's voltage to the battery's bus voltage, but none were successful. In fall of 2007 I decided to take on the challenge of developing the DC-DC converter and implementing it into the SuPER system for my master's thesis.

1.3 Photovoltaic Array I-V Characteristics

Figure 1.1 shows the current and voltage (I-V) characteristics of the BP SX 150 PV array used for the SuPER projects solar energy source. These characteristics show the PV array behaving as a current source, in the sense that the current remains constant as the voltage varies. The standard Buck topology would have limited performance with

a current source for its electrical power input, since the output current of the converter could never be higher than the maximum input current.

Figure 1.1 – BP SX 150 I-V Characteristics [2]

1.5 Thesis Objectives

The objective of this thesis is to modify the standard Buck converter topology to work with a current source input, and make the converter capable of supplying a higher output current than the source current. This will be accomplished by making the PV array appear to the converter as a voltage source, by placing a capacitor across the input of the converter. By accomplishing this the converter will behave as the standard Buck converter, and the same pulse width modulation (PWM) control algorithm can be used. The original DC-DC converter specifications can be seen in table 1.1, but the DC-DC converters in this thesis were designed to meet the modified specifications seen in table 1.2. These modifications and additions to the specifications were made to aid in the design process.

To accomplish this thesis, two converter topologies were investigated. A universal Buck and universal synchronous Buck converter were designed, prototyped, and analyzed. Multiple versions of each converter were tested to improve the overall performance, and after individual testing was completed, the best performing configuration of each converter was selected for integrations into the SuPER system prototype. Now that the converters could be connected to the actual system, the PWM control code was tested and modified to increase the converter's overall performance.

Table 1.1 – Initial DC-DC Converter Specifications [3]

Parameter	Value
Input voltage	wide range, 0 to 40V
Input current	4.75A max
Max power	150W, 80% efficiency target
Output voltage	11.5V-14V
Output current	13A max
Switching frequency	500kHz

Table 1.2 – Modified DC-DC Converter Specifications

Parameter	Value
Input voltage	wide range, 0 to 40V
Input current	4.75A max
Max power	150W, 80% efficiency target
Output voltage	11.5V-14V
Output current	13A max
Switching frequency	any practical value
Continuous conduction mode	down to 10% of full load
Output voltage ripple	240mV
Input voltage ripple	100mV

1.6 Document Overview

A review of a Buck converters current and voltage relationships are given in Chapter 2, and the equations needed for proper component selection for designing the

converter are derived. A simulation of the designed ideal converter is conducted using PSpice, and the results are compared with the theoretical values. The limitations of a Buck converter are then discussed for both voltage and current source inputs. A solution is then presented in Chapter 3 that will overcome the converter's limitations with a current source input, and the necessary equations needed to design a universal Buck converter are derived. An ideal universal Buck converter is then simulated using PSpice, and the results are compared with the theoretical calculations. An actual universal Buck converter is then designed and tested in the lab, using a static PWM signal and power supplies. Chapter 4 goes through the design of a universal synchronous Buck converter, in the hopes of improving the converters overall efficiency. Chapter 5 discusses how the PWM signal is controlled to implement MPPT, battery charge control, and PV array voltage step down for both the universal Buck and synchronous Buck converters. The achievements of this thesis are discussed in Chapter 6, as well as future recommendations for the SuPER project. Appendices A through G show the voltage waveforms obtained during the testing of seven different universal Buck converter configurations, and appendices H through K show the waveforms for four different universal synchronous Buck converter configurations. And finally the senior project analysis form is presented in appendix L.

Chapter 2: Buck Converter

A Buck converter, which is also known as a step down converter, acts as a DC transformer in the sense that it allows the ability to step down the input voltage and increase the output current much like an AC step down transformer. Figure 2.1 shows the Buck converter topology, where the ideal switch can be realized with a MOSFET. The Buck converter uses passive energy storage elements to transfer energy from the source to the load. When the switch is on, the input charges the inductor L to the output current necessary to produce the desired output voltage V_{out} across the load R . Once the output voltage is obtained the switch disconnects and the diode D provides an alternate path for the inductor current, which then begins to decay. The output capacitor C helps reduce the output voltage ripple caused by switching. The cycle repeats at the switching frequency and the duty cycle, which is ratio of time the switch is on compared to the switching period, determines the output voltage [4].

Figure 2.1 – Buck Converter Topology

2.1 Buck Converter Current Voltage Relationship

DC-DC converters can be difficult to analyze because they are nonlinear circuits. By using average values the nonlinear circuits can be analyzed using a linear model. The following sections derive the equations necessary to design an ideal Buck converter

similar to Taufik [5], to familiarize the reader with how average values can be used to predict the converter's performance. The Buck converter can be represented by two circuits. One circuit represents the converter when the switch is turned on, and the second circuit represents the converter when the switch is turned off. Before the derivation can occur, some variables need to be defined and some assumptions made. For this derivation all components will be assumed lossless, and the converter will operate in constant current mode (CCM). CCM means that the inductor current will never go below zero in steady state operation. Also, average voltage and current values are represented by upper case letters, while time varying values are represented by lower case letters.

Variables

f = switching frequency
 T = switching period
 D = duty cycle
 R = load
 v_L = inductor voltage
 i_L = inductor current
 Δi_L = inductor ripple current
 ΔV_{out} = output ripple voltage
 Q = charge

2.1.1 Switch Turned On

When the switch is turned on the diode becomes reversed biased (figure 2.2), and energy is transferred from the source to the inductor, capacitor, and load.

Using Kirchhoff's voltage law (KVL) the voltage across the inductor can be found by:

$$v_L = V_{in} - V_{out} \quad (2.1)$$

And the voltage across the inductor also equals:

$$v_L = L \frac{di_L}{dt} \quad (2.2)$$

Setting equations (2.1) and (2.2) equal, and rearranging variables yields:

$$\frac{di_L}{dt} = \frac{V_{in} - V_{out}}{L} \quad (2.3)$$

Realizing that di_L equals the change of inductor current (ripple) while the switch is closed, and dt equals the time the switch is closed, the following conclusion can be made:

$$\frac{di_L}{dt} = \frac{\Delta i_{L,closed}}{\Delta t} = \frac{\Delta i_{L,closed}}{D \cdot T} = \frac{V_{in} - V_{out}}{L} \Rightarrow \Delta i_{L,closed} = \frac{V_{in} - V_{out}}{L} \cdot D \cdot T \quad (2.4)$$

Figure 2.2 – Buck Converter Circuit when Switch is On

2.1.2 Switch Turned Off

When the switch is turned off the inductor transfers energy to the load, and the diode becomes forward biased as seen in figure 2.3. This occurs because the current through an inductor can not change instantaneously, so the cathode of the diode is forced below ground by the inductor to insure a current path.

Using KVL the voltage across the inductor can be found:

$$v_L = -V_{out} \quad (2.5)$$

And the voltage across the inductor also equals:

$$v_L = L \frac{di_L}{dt} \quad (2.6)$$

Setting equations (2.5) and (2.6) equal, and rearranging variables yields:

$$\frac{di_L}{dt} = -\frac{V_{out}}{L} \quad (2.7)$$

Realizing that di_L equals the change of inductor current (ripple) while the switch is open, and dt equals the time the switch is open, the following conclusion can be made:

$$\frac{di_L}{dt} = \frac{\Delta i_{L,open}}{\Delta t} = \frac{\Delta i_{L,open}}{T - D \cdot T} = \frac{\Delta i_{L,open}}{(1 - D) \cdot T} = -\frac{V_{out}}{L} \Rightarrow \Delta i_{L,open} = -\frac{V_{out}}{L} \cdot (1 - D) \cdot T \quad (2.8)$$

Figure 2.3 – Buck Converter Circuit when Switch is Off

2.1.3 Critical Component Values

Since the inductor current magnitude at the end of the switching period must equal the inductor current magnitude at the beginning of the next period at steady state, the change in current over the switching period must equal zero. Using this knowledge yields the following:

$$\Delta i_{L,period} = \Delta i_{L,closed} + \Delta i_{L,open} = 0 \quad (2.9)$$

Substituting equations (2.4) and (2.8) into (2.9) and solving for D yields:

$$D = \frac{V_{out}}{V_{in}} \quad (2.10)$$

Now the average inductor current equals the average of the minimum and maximum inductor current values, so the maximum inductor can be found using equation (2.11) noting that either $\Delta i_{L,closed}$ or $\Delta i_{L,open}$ can be used.

$$i_{L\max} = I_L + \frac{|\Delta i_L|}{2} \quad (2.11)$$

Using the rule known as amp-second balance, which states the average current through a capacitor at steady state must equal zero, the average inductor current must equal the average output current.

$$I_L = I_{out} = \frac{V_{out}}{R} \quad (2.12)$$

Substituting equations (2.8) and (2.12) into (2.11) and simplifying yields:

$$i_{L\max} = V_{out} \cdot \left[\frac{1}{R} + \frac{(1-D)}{2 \cdot L \cdot f} \right] \quad (2.13)$$

The minimum inductor current can be found in the same manner as the maximum inductor current:

$$i_{L\min} = I_L - \frac{|\Delta i_L|}{2} \quad (2.14)$$

Substituting equations (2.8) and (2.12) into (2.14) and simplifying yields:

$$i_{L\min} = V_{out} \cdot \left[\frac{1}{R} - \frac{(1-D)}{2 \cdot L \cdot f} \right] \quad (2.15)$$

The minimum inductor current is an important value, because as mentioned previously, it determines the mode of conduction. Since all previous equations were derived using the assumption of CCM, for them to remain valid $i_{L\min}$ can never go below

zero. So by setting equation (2.15) equal to zero and rearranging to solve for L , the minimum inductor value can be found to keep the converter in CCM as seen below.

$$L_{\min} = \frac{(1-D) \cdot R}{2 \cdot f} \quad (2.16)$$

Once the inductor value is determined, the minimum capacitance to maintain the desired output ripple voltage can be found. This can be done by finding how much charge is supplied by the capacitor when the switch is on or off. By using amp-second balance the average current through a capacitor must equal zero if the circuit is in steady state. Then by calculating the area under the current wave form either when the switch is on or off will yield the change in charge. Since the current wave form is triangular the area can be found by using the formula one half times the triangle's base times the triangles height. Where the height equals the change in current divided by two, and the base is the switching period divided by two.

$$\Delta Q = \frac{1}{2} \cdot \frac{|\Delta i_L|}{2} \cdot \frac{T}{2} \quad (2.17)$$

In this case the change of charge (ΔQ) is easier to calculate using the change in current when the switch is off ($\Delta i_{L,open}$). Substituting equation (2.8) into (2.17) and simplifying yields:

$$\Delta Q = \frac{V_{out} \cdot (1-D)}{8 \cdot L \cdot f^2} \quad (2.18)$$

Noting that:

$$C = \frac{\Delta Q}{\Delta V_{out}} \quad (2.19)$$

Substituting equation (2.18) into equation (2.19) yields the equation for selecting the minimum output capacitor for the desired output ripple voltage.

$$C_{\min} = \frac{1-D}{8 \cdot L \cdot \Delta V_{out} \cdot f^2} \cdot V_{out} \quad (2.20)$$

2.2 Ideal Buck Converter Design

This section goes through the process of designing an ideal Buck converter, by using the previously derived equations to size the inductor and capacitor. These values will later be used to simulate the ideal Buck converter.

2.2.1 Parameters

The rated current and voltage values of the PV array at maximum power point (MPP), were used to describe the converter input parameters. A switching frequency of 100kHz was used, since it produced reasonably sized inductor and capacitor values. Also since the converter's output voltage is specified as a range in table 2.2, 12V was chosen for the output voltage. By assuming ideal components the following converter parameters were calculated.

$$f = 100kHz$$

$$V_{in} = 34.5V$$

$$V_{out} = 12V$$

$$P_{in} = P_{out} = 150W$$

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{150W}{12V} = 12.5A$$

$$D = \frac{V_{out}}{V_{in}} = \frac{12V}{34.5V} = 0.348$$

$$I_{in} = \frac{P_{in}}{V_{in}} = \frac{150W}{34.5V} = 4.348A$$

2.2.2 Inductor Calculation

The minimum inductor value to keep the converter operating in continuous conduction mode down to 10% of full load is calculated by finding the output resistance that represents this load and inserting into equation (2.16).

$$P_{10\%} = 0.10 \cdot P_{out} = 0.10 \cdot 150W = 15W$$

$$R_{10\%} = \frac{V_{out}^2}{P_{10\%}} = \frac{(12V)^2}{15W} = 9.6\Omega$$

$$L_{min} = \frac{(1-D) \cdot R}{2 \cdot f} = \frac{(1-0.348) \cdot 9.6\Omega}{2 \cdot 100kHz} = 31.3\mu H$$

Now that the minimum inductor value is known to keep the converter operating in continuous conduction mode, a slightly larger inductor is selected to maintain a performance margin. A 56 μ H inductor was selected for L , since it is a standard value and 1.8 times larger than the calculated L_{min} value. By substituting L and $R_{10\%}$ into equations (2.13) and (2.15) the minimum and maximum inductor current values are calculated.

$$i_{Lmin} = 12V \cdot \left[\frac{1}{9.6\Omega} - \frac{(1-0.348)}{2 \cdot 56\mu H \cdot 100kHz} \right] = 0.551A$$

$$i_{Lmax} = 12V \cdot \left[\frac{1}{9.6\Omega} + \frac{(1-0.348)}{2 \cdot 56\mu H \cdot 100kHz} \right] = 1.949A$$

The difference between the maximum and minimum inductor current equals the inductor's ripple current.

$$\Delta i_L = i_{Lmax} - i_{Lmin} \quad (2.21)$$

Inserting the maximum and minimum inductor current values into equation (2.21) yields:

$$\Delta i_L = 1.949A - 0.551A = 1.398A$$

2.2.3 Capacitor Calculation

Using the output ripple voltage found in table 1.2, and the value of the inductor found in section 2.2.2, the minimum output capacitance can be found using equation (2.20).

$$C_{\min} = \frac{1 - 0.348}{8 \cdot 56 \mu H \cdot (100 kHz)^2} \cdot \left(\frac{12V}{0.24V} \right) = 7.3 \mu F$$

2.2.4 Diode and Switch

Although MOSFETs are typically used as the switch, all MOSFET models used for simulations have losses. Instead of a MOSFET, a switch was used in its place for the simulation. Also, due to the fact that all diodes in the PSpice libraries have losses as well, the diode was also modeled with a switch. Switches called SBreak can be found in the PSpice BREAKOUT library and modified to be virtually lossless. By reviewing the help files included with the program, the process of how to modify the component was learned. To modify the SBreak model, place the switch on the schematic and right click on it. Next choose edit PSpice model and change the Ron value (on resistance) to 0.0000001. Any value of resistance could have been selected, but 0.1Ω was used to decrease the voltage drop across the switch to a negligible value.

2.3 Ideal PSpice Simulation

To prove the previous derived equations work, a PSpice simulation was used to make a comparison of simulated and theoretical values. The simulation was also used to generate different current and voltage wave forms, to develop a better understanding of

what is physically happening in the circuit. The simulation schematic can be seen in figure 2.4.

Figure 2.4 – 10% Load Simulation with Voltage Source Input

2.3.1 Simulation at Ten Percent Load

Figure 2.5 shows the output voltage ripple compared to the average output voltage calculated from the output ripple voltage. The current through switch two, which represents the diode, can be seen in figure 2.6. This current added to the input switch current seen in figure 2.7 make up the inductor current seen in figure 2.9. Notice that none of these currents are DC, and their average values are shown in figure 2.8.

Figure 2.5 – Output Voltage Ripple and Average Value

Figure 2.6 – Current in S2 Representing Diode Current

Figure 2.7 – Current in S1 representing Input Current

Figure 2.8 – Average Current Values

Figure 2.9 – Inductor and Capacitor Current

2.3.2 Theoretical and Simulation Comparison

After reviewing the data in table 2.1 obtained from both the theoretical calculations and simulated results, the simulation generates very accurate values when compared to the theoretical calculations.

Table 2.1 – Buck Converter Data Comparison

Parameter	Theoretical	Simulation
Output voltage ripple	0.240V	0.240V
Minimum inductor current	0.551A	0.554A
Maximum inductor current	1.949A	1.950A
Inductor current ripple	1.398A	1.396A

2.4 Standard Topology Limitations

Figure 2.1 shows the standard Buck converter topology, and figure 2.8 shows how the average output current can be higher than the average input current with a voltage source input. Also note that the average input current added to the average diode current equals the average output current. However, the actual input current is not DC at all, but rather a pulse with a constant rate of rise and duration associated with how long the

switch is turned on as seen in figure 2.7. So the maximum input current value is always greater than the average output current.

2.4.1 Voltage Source Input

When an ideal voltage source is connected to the input of the converter, the input voltage stays constant while the input current varies. Meaning the voltage stays constant while the current varies with load. So there are no output current limitations for the converter. The only limitation is the maximum output voltage can not be greater than the input, coincides with a duty cycle of one.

2.4.2 Current Source Input

When an ideal current source is connected to the input of the converter, the input current stays constant while the input voltage varies. Meaning the current stays constant while the voltage varies with load, so there are no output voltage limitations for the converter. The only output limitation is the maximum output current cannot be greater than the maximum input current. This is where the problem lies with the standard Buck topology that uses an inductor as the main energy storage element in the circuit.

Chapter 3: Universal Buck Converter

In order to solve the Buck converter's output current limitation when a current source is connected to the input, the standard Buck topology seen in figure 2.1 needed to be modified. A buck converter requires pulsating current, so a capacitor is needed at the input of the converter to store the energy generated by the PV array when the switch is off [6]. Also by taking advantage of the capacitor's property that the voltage across a capacitor can not change instantaneously, the PV array can be viewed as a voltage source if a large enough capacitor is placed in parallel with it. This capacitor will be referred to as the input capacitor of the universal Buck converter, and can be seen in figure 3.1. The input capacitor creates a reservoir for energy to be stored when the switch is off, and if the switch is off long enough the capacitor will be charged to the open circuit voltage (V_{OC}) of PV array.

Figure 3.1 – Universal Buck Converter

3.1 Input Capacitor Derivation

To design the universal Buck converter the equation for properly sizing the input capacitor needed to be derived, since the equation was not found in any literature reviewed. Since the PV array can now be viewed as a voltage source the equations derived in chapter 2 are still valid, since they were derived using the average input

voltage value. The input capacitor will transfer the most charge when the converter is operating under full load. By using amp-second balance, the average current of the capacitor must equal zero at steady state. This means the charge transferred when the switch is on (figure 3.2) must equal the charge transferred when the switch is off (figure 3.3).

Figure 3.2 – Universal Buck Converter Circuit when Switch is On

Figure 3.3 – Universal Buck Converter Circuit when Switch is Off

The change in charge when the switch is turned off, can be solved easier than when the switch is on. At full load and steady state, the capacitor current will equal that of the current source when the switch is turned off.

$$\Delta Q = I_{in} \cdot (1 - D) \cdot T \quad (3.1)$$

Noting that:

$$C_{in} = \frac{\Delta Q}{\Delta V_{in}} \quad (3.2)$$

Substituting equation (3.1) into equation (3.2) yields the equation for selecting the minimum input capacitor for the desired input ripple voltage.

$$C_{in,min} = \frac{I_{in} \cdot (1-D)}{\Delta V_{in} \cdot f} \quad (3.3)$$

Since the input capacitor will supply a fair amount of charge, the capacitor RMS current needs to be known to properly design the converter. Once again this equation was not found in any literature that was reviewed, so it needs to be derived. The equation defining the RMS current was derived as follows:

$$I_{Crms} = \sqrt{\frac{1}{T} \left[\int_0^{t_{on}} \left(i_{L,min} + \frac{\Delta i_L}{t_{on}} \cdot t - I_{in} \right)^2 dt + \int_0^{t_{off}} (-I_{in})^2 dt \right]} \quad (3.4)$$

After integrating and simplifying equation (3.4), equation (3.5) defines the input capacitor's RMS current.

$$I_{Crms} = \sqrt{\frac{1}{T} \left\{ \left[i_{L,min}^2 - 2 \cdot I_{L,min} \cdot I_{in} + I_{in}^2 \right] \cdot t_{on} + (I_{L,min} - I_{in}) \cdot \Delta i_L + \frac{\Delta i_L^2}{3} \cdot t_{on} + I_{in}^2 \cdot t_{off} \right\}} \quad (3.5)$$

3.2 Ideal Universal Buck Converter Design

This section goes through the process of designing an ideal universal Buck converter, by using the previously derived equations to size the input capacitor. The same inductor used for the Buck converter in chapter 2 can be used for this converter, since the same parameters defined in section 2.2.1 are going to be used for this converter. This capacitor value will later be used to simulate the ideal universal Buck converter.

3.2.1 Inductor Current Values at Full Load

The inductor current values at ten percent load were already calculated and compared to simulated results in chapter 2. This time the simulation was conducted at full load, so the minimum, maximum, and ripple current of the inductor are calculated below to compare with the simulation. The inductor value from section 2.2.2 and the resistance value representing full load, calculated below, were substituted into equations (2.13) and (2.15).

$$R = \frac{V_{out}^2}{P_{out}} = \frac{(12V)^2}{150W} = 0.96\Omega$$

$$i_{L\min} = 12V \cdot \left[\frac{1}{0.96\Omega} - \frac{(1-0.348)}{2 \cdot 56\mu H \cdot 100kHz} \right] = 11.801A$$

$$i_{L\max} = 12V \cdot \left[\frac{1}{0.96\Omega} + \frac{(1-0.348)}{2 \cdot 56\mu H \cdot 100kHz} \right] = 13.199A$$

Inserting the maximum and minimum inductor current values into equation (2.21) yields:

$$\Delta i_L = 13.199A - 11.801A = 1.398A$$

3.2.2 Input Capacitor

The minimum value for the input capacitor can be calculated by substituting the values found in section 2.2.1 and table 1.2 into equation (3.3).

$$C_{in(\min)} = \frac{I_{in} \cdot (1-D)}{\Delta V_{in} \cdot f} = \frac{4.35A \cdot (1-0.348)}{100mV \cdot 100kHz} = 283.6\mu F$$

The input capacitor's RMS current (I_{Crms}) was also calculated below, using equation (3.5) and the values from sections 2.2.1 and 3.2.1.

$$\sqrt{\frac{1}{10\mu s} \left\{ \left[\left((11.8A)^2 - 2 \cdot 11.8A \cdot 4.4A + (4.4A)^2 \right) + (11.8A - 4.4A) \cdot 1.4A + \frac{(1.4A)^2}{3} \right] \cdot 3.48\mu s + (4.4A)^2 \cdot 6.52\mu s \right\}} = 5.959A$$

Figure 3.5 – Average Output Voltage and Ripple at Full Load

Figure 3.6 – Inductor and Capacitor Ripple Current at Full Load

Figure 3.7 – Average Current Values

Figure 3.8 – Input Capacitor, Switch, and Current Source Current

Figure 3.9 – Input Capacitor RMS Current

Figure 3.10 – Average Input Capacitor Voltage and Ripple

3.3.2 Theoretical and Simulation Comparison

After reviewing the data in table 3.1 obtained from both the theoretical calculations and simulated results, the simulation generates very accurate values when compared to the theoretical calculations.

Table 3.1 – Universal Buck Converter Data Comparison

Parameter	Theoretical	Simulation
Output voltage ripple	0.240V	0.227V
Input voltage ripple	0.100V	0.100V
Minimum inductor current	11.801A	11.794A
Maximum inductor current	13.199A	13.190A
Inductor current ripple	1.398A	1.396A
Input capacitor's RMS current	5.959A	5.960A

3.4 Component Selection for Actual Design

When the universal Buck converter was simulated, ideal components were used. Since no components are actually ideal in real world applications, the following section discusses the methodology of how components were selected for the universal Buck converter design.

3.4.1 MOSFET

When selecting a MOSFET there are several important parameters to review on the MOSFET's datasheet.

$V_{(BR)DSS}$ – maximum drain to source voltage.

I_D – maximum continuous drain current.

V_{GS} – maximum gate to source voltage.

$R_{DS(on)}$ – drain to source on resistance.

Q_G – total gate charge.

t_r – rise time.

t_f – fall time.
 C_{OSS} – output capacitance
 T_J – maximum junction temperature.
 R_{JC} – junction to case thermal resistance.

The maximum voltage the PV array can output is 43.5V [2] at open circuit voltage, and the maximum current through the switch from section 2.2.1 is 4.348A. Once the maximum voltage and current of the converter are known, the $V_{(BR)DSS}$ and I_D values will determine if the MOSFET can withstand normal operating conditions. The maximum voltage output of the gate driver will determine if the V_{GS} rating is adequate. While t_r , t_f , and C_{OSS} will be used to determine the switching losses of the MOSFET in section 3.5.1. The conduction losses of the MOSFET in section 3.5.2 are calculated using $R_{DS(on)}$. Q_G is used to determine the gate driver's losses in section 3.5.3. T_J and R_{JC} will be used to determine if a heatsink is required to dissipate heat from the MOSFET in section 3.6.1. After all of these parameters were reviewed, an International Rectifier IRF3205Z automotive MOSFET was selected, which has a minimum 55V $V_{(BR)DSS}$ and 75A I_D rating. A MOSFET from International Rectifiers switching mode power supply line would have been a better choice, but none were available for purchase through online vendors.

3.4.2 Gate Driver

Figure 3.1 shows the switch in between the source and the load, which is know as high side switch. When the MOSFET turns on the drain and source terminals are at the same voltage. In order to turn the MOSFET on, and keep it turned on, the gate to source voltage must be between 10V-15V. This requires the gate voltage to be 10V-15V greater than the MOSFET's drain voltage [7]. One method to accomplish this is to use a high side gate driver with a bootstrap capacitor (IRS2117), which can be seen in figure 3.11.

The bootstrap capacitor is connected between the V_B and V_S pin of the gate driver. Initially the output capacitor has 0V across it, so the V_S pin voltage is 0V as well. This causes the bootstrap diode, connected between pins V_{CC} and V_B , to become forward biased and charge the bootstrap capacitor to the V_{CC} voltage level. When the PWM signal at the IN pin is high, V_B is connected to the HO pin. This turns the MOSFET on and the V_S pin is now at the MOSFET's drain voltage. But since the bootstrap capacitor is connected between V_B and V_S , the MOSFET's gate to source voltage remains constant at the V_{CC} voltage.

Figure 3.11 – IRS2117 High Side Gate Driver [8]

3.4.3 PIC to Gate Driver Interface

International Rectifiers did not have a large selection of high side gate drivers to choose from, which created a problem when it came to interfacing the PIC's PWM signal with the gate driver. Since the IRS2117 gate driver is 15V input logic compatible, this meant the 0V to 5V PWM signal coming from the PIC needed to be increased to interface with the gate driver. This was accomplished by using a MM74C906N open drain buffer. The buffer's V_{CC} must be powered by a 5V source to make it compatible with the PIC's

5V output. With a 5V V_{CC} the logic high threshold is 3.5V [9]. A $\mu A7805$ CKCS 5V linear voltage regulator was used to supply the 5V V_{CC} of the buffer. The output of the buffer was connected to the battery bus with a 1.2k Ω pull up resistor.

Figure 3.12 – MM74C906N Open Drain Buffer [9]

3.4.4 Inductor

According to section 2.2.2 a 56 μ H inductor will keep the converter operating in continuous conduction mode down to 10% of full load. A Bourns 1140-560K-RC 56 μ H 14.4A inductor was selected since it was the only inductor available through Newark Electronics that could be used.

3.4.5 Capacitors

When it came to selecting an input capacitor, it was very difficult finding capacitors that could handle the large RMS current, calculated in section 3.2.2, to be used for the input capacitor. Instead of using a single input capacitor three Rubycon ZLH series 1000 μ F 50V capacitors, each rated for 3.01 Arms, were connected in parallel to make up the input capacitor. These three capacitors produce 3000 μ F of input capacitance, which is much larger than the 283.6 μ F calculated in section 3.2.2, and were selected for their high current rating not capacitance value.

The output capacitance was calculated in section 2.2.3, but this equation only works for ideal capacitors. Since the actual capacitors will have an equivalent series

resistance (ESR), the actual output capacitance required to meet the ripple voltage criteria will be much larger than what was calculated in section 2.2.3. It was discovered that with electrolytic capacitor the product of ESR and capacitance is constant, and a more conservative approach for calculating the output capacitance is given by equation (3.6) [10].

$$C_{out} = (65\mu\Omega \cdot F) \cdot \left(\frac{0.2 \cdot I_{out}}{\Delta V_{out}} \right) \quad (3.6)$$

Substituting the values from table 1.2 and section 2.2.1 into equation (3.6) yields a conservative output capacitance value seen below. A Rubycon ZLH series 1000 μ F 50V capacitor will also be used for the output capacitor.

$$C_{out} = (65\mu\Omega \cdot F) \cdot \left(\frac{0.2 \cdot 12.5A}{240mV} \right) = 677\mu F$$

3.4.6 Freewheeling Diode

The main requirements for selecting the diode were current rating, reverse blocking voltage, and forward voltage during conduction. Since the maximum output current of the converter is 12.5A, this value can be used as the diode's current rating. Since the maximum voltage across the diode occurs when the MOSFET is on, the reverse blocking voltage of the diode must be rated for at least V_{OC} . Using these two requirements to narrow the options of diodes to a lower number, the forward voltage of the remaining diodes can then be considered. The forward voltage will determine the power consumption of the diode during conduction, so a small forward voltage is desired. An International Rectifier MBR2045CT Schottky diode was selected, and the forward voltage at maximum current was found as follows. Since the MBR2045CT contains two

diodes per package, see figure 3.13, they will be connected in parallel. The current per leg through the diode to determine the forward voltage can be found below.

$$I_{diode(per_leg)} = \frac{I_{out}}{2} = \frac{12.5A}{2} = 6.25A$$

From figure 3.14 the forward voltage (V_f) at 6.25A, using the 25°C curve, is approximately 0.61V. This forward voltage value will later be used in the converter's theoretical efficiency calculations in section 3.5.4.

Figure 3.13 – MBR2045CT Pin Connections [11]

Figure 3.14 – MBR2045CT Diode Current Voltage Characteristics Per Leg [11]

3.5 Theoretical Efficiency

Since the actual Buck converter will not use ideal components, losses will occur as energy is transmitted from the input to the output. In order to predict the converter's efficiency at various loads, component losses need to be calculated. These losses include MOSFET switching, MOSFET conduction, MOSFET gate, inductor losses, and diode conduction. Note that the MOSFET gate losses are constant, where as the other four losses are dependent on the output current. All sample calculations in the following sections are at maximum load.

3.5.1 MOSFET Switching Losses

Due to the fact that a MOSFET does not turn on and off instantaneously, power is consumed during the transition of turning the switch off and on. These losses are known as switching losses and Shen et al [12] references an approximate way of calculating these losses. The second term of equation (3.7) takes into account the energy stored in the MOSFET's output capacitance that is internally dissipated during turn off. Now the first term of equation (3.7) makes the assumption that the drain to source voltage and current change linearly, and calculates the switching losses as the triangular area under the drain to source voltage and current transition periods.

$$P_{sw} = \frac{1}{2} \cdot V_{in} \cdot I_{out} \cdot (t_r + t_f) \cdot f + \frac{1}{2} \cdot C_{OSS} \cdot V_{in}^2 \cdot f \quad (3.7)$$

Substituting the values from sections 2.2.1 and the datasheet [13] into equation (3.7) yield the switching losses seen below. The assumption is being made that t_r and t_f equals the values in the datasheet [13], even though the actual gate resistor value does not equal that used in datasheet.

$$P_{sw} = \frac{1}{2} \cdot 34.5V \cdot 12.5A \cdot (95ns + 67ns) \cdot 100kHz + \frac{1}{2} \cdot 430pF \cdot 34.5V^2 \cdot 100kHz = 3.52W$$

3.5.2 MOSFET Conduction Losses

This loss is due to the MOSFET's internal resistance between the drain and source terminals. Since no curve of $R_{ds(on)}$ vs. V_{GS} was supplied with the MOSFET's datasheet [13], the maximum specified $R_{ds(on)}$ was used. Mappus [14] calculates the MOSFET conduction losses as follows:

$$P_{cond} = I_{out}^2 \cdot R_{ds(on)} \cdot D \quad (3.8)$$

Substituting the values from sections 2.2.1 and the datasheet [13] into equation (3.8) yield the MOSFET's conduction losses.

$$P_{cond} = (12.5A)^2 \cdot 6.5m\Omega \cdot 0.348 = 353mW$$

3.5.3 MOSFET Gate Losses

This loss is not load dependent and is directly related to the MOSFET's total gate charge, and gate to source voltage which equals the gate drivers V_{CC} voltage. By using the graph in figure 3.15 from the MOSFET's datasheet and the $V_{DS} = 44V$ curve, Q_G equals approximately 90nC at V_{GS} equal to 12V. Now the power dissipated by charging and discharging the gate is supplied by V_{CC} of the gate driver, which is connected to the battery. But when the battery is being charged by the converter, the converter is supplying the V_{CC} voltage of the gate driver. The application note [7] calculates the gate losses as follows:

$$P_{gate} = V_{GS} \cdot Q_G \cdot f \quad (3.9)$$

Substituting the appropriate values into equation (3.9) yields the MOSFET's gate losses.

$$P_{gate} = 12V \cdot 90nC \cdot 100kHz = 108mW$$

Figure 3.15 – MOSFET's V_{GS} vs. Q_G Curve [13]

3.5.4 Diode Conduction Losses

This loss is only present when the MOSFET is turned off and the diode is freewheeling. The forward voltage V_f was found in section 3.4.6, and for worst case scenario it will be held constant for all loads.

$$P_{diode} = (1 - D) \cdot I_o \cdot V_f \quad (3.10)$$

Substituting the values found in sections 2.2.1 and 3.4.6 into equation (3.10) yields the diode conduction losses.

$$P_{diode} = (1 - 0.348) \cdot 12.5A \cdot 0.61V = 4.972W$$

3.5.4 Inductor Losses

The inductor losses are caused by the DC resistance (DCR) of the copper.

According to Bournes [15] the maximum DCR of the 1140-560K-RC inductor is $19m\Omega$.

$$P_{inductor} = I_{out}^2 \cdot DCR \quad (3.11)$$

Substituting the appropriate values into equation (3.11) yields the inductor's losses.

$$P_{inductor} = (12.5A)^2 \cdot 19m\Omega = 2.969W$$

3.5.5 Theoretical Efficiency Calculation

The theoretical efficiency is the ratio of the output power over the input power, and the calculation is determined by the equation below. The results from 10% load to full load can be seen in table 3.2. These values will later be compared to the actual results in figure 3.21.

$$\eta = \frac{P_{out}}{P_{total}} = \frac{P_{out}}{P_{out} + P_{sw} + P_{cond} + P_{diode} + P_{gate} + P_{inductor}} \quad (3.12)$$

Substituting the appropriate values found in section 3.5.1 through 3.5.4 into equation (3.12) yields the theoretical efficiency of the converter at full load.

$$\eta = \frac{150W}{150W + 3.519W + 0.353W + 4.972W + 0.108W + 2.969W} = \frac{150W}{161.92W} = 92.64\%$$

Table 3.2 – Universal Buck Converter Theoretical Efficiency

Percent Load	P _{out} (W)	P _{sw} (W)	P _{cond} (W)	P _{diode} (W)	P _{gate} (W)	P _{inductor} (W)	P _{total} (W)	η (%)
10	15.0	0.375	0.004	0.497	0.108	0.030	16.01	93.67
20	30.0	0.724	0.014	0.995	0.108	0.119	31.96	93.87
30	45.0	1.074	0.032	1.492	0.108	0.267	47.97	93.80
40	60.0	1.423	0.057	1.989	0.108	0.475	64.05	93.67
50	75.0	1.772	0.088	2.486	0.108	0.742	80.20	93.52
60	90.0	2.121	0.127	2.984	0.108	1.069	96.41	93.35
70	105.0	2.471	0.173	3.481	0.108	1.455	112.69	93.18
80	120.0	2.820	0.226	3.978	0.108	1.900	129.03	93.00
90	135.0	3.169	0.286	4.476	0.108	2.405	145.44	92.82
100	150.0	3.519	0.353	4.972	0.108	2.969	161.92	92.64

3.6 Heat Sink Calculation

Since the MOSFET and freewheeling diode have quite large losses, the temperature of each component at full load needs to be calculated to determine if their maximum junction temperature is exceeded. Taufik [10] presents thermal analysis with an electrical analogy, making the design process quite easy to follow. The thermal circuit elements can be represented by their electrical counterparts seen in table 3.3. Once the values of the different elements are known, the thermal circuit can be drawn. Below are definitions of component values obtained from datasheet required to conduct a thermal analysis.

T_J – junction temperature
 T_C – case temperature
 T_S – heatsink surface temperature
 T_A – ambient temperature
 R_{JA} – junction to ambient thermal resistance
 R_{JC} – junction to case thermal resistance
 R_{CS} – case to sink thermal resistance
 R_{SA} – heatsink to ambient thermal resistance

Table 3.3 – Thermal Elements and Analogous Electrical Element [10]

Electrical Element	Thermal Element
Current Source (A)	Heat source (W)
Resistance (Ω)	Thermal Resistance ($^{\circ}\text{C}/\text{W}$)
Node Voltage (V)	Surface Temperature ($^{\circ}\text{C}$)
Current Loop	Thermal Loop
Circuit Ground (V)	Ambient Air Temperature ($^{\circ}\text{C}$)

3.6.1 MOSFET

Figure 3.16 shows the MOSFET's thermal loop if no heat sink is used. Equation (3.13) determines how much heat the MOSFET must dissipate, and equation (3.14) is used to calculate the junction temperature.

$$\text{Heat} = P_{sw} + P_{cond} \quad (3.13)$$

Substituting the values from section 3.5.1 and 3.5.2 into equation (3.13) yields the MOSFET's heat that is directly related to switching and conduction losses.

$$Heat = 3.519W + 0.353W = 3.872W$$

Figure 3.16 shows the thermal loop for the MOSFET without a heatsink. The junction temperature can then be calculated using equation (3.14).

$$T_J = Heat \cdot R_{JA} + T_A \quad (3.14)$$

Using the value of heat calculated above, and the values found in the datasheet [13], the junction temperature without a heat sink can be determined assuming an ambient temperature of 25°C.

$$T_J = 3.872W \cdot 62 \frac{^{\circ}C}{W} + 25^{\circ}C = 265.1^{\circ}C$$

The maximum allowable junction temperature of the MOSFET is 175°C, so a heatsink must be used to keep the junction temperature from exceeding its maximum value.

Figure 3.16 – MOSFET Thermal Model without Heatsink

Figure 3.17 shows the thermal loop for the MOSFET with a heatsink. The junction temperature can then be calculated using equation (3.15).

$$T_J = Heat \cdot (R_{JC} + R_{CS} + R_{SA}) + T_A \quad (3.15)$$

A Comair Rotron 411320B02500 heatsink and a Wakefield Engineering 175-6-210P insulator were selected. Substituting the values from the datasheets [13], [16], and [17] into equation (3.15) yields the junction temperature calculated below, which is well below the maximum allowable junction temperature.

$$T_j = 3.872W \cdot \left(0.9 \frac{^{\circ}C}{W} + 0.4 \frac{^{\circ}C}{W} + 9.1 \frac{^{\circ}C}{W} \right) + 25^{\circ}C = 65.3^{\circ}C$$

Figure 3.17 – MOSFET Thermal Model with Heatsink

3.6.2 Diode

The calculation for the diode is similar to that of the MOSFET, except the thermal resistance from the junction to ambient was not given in the diodes datasheet. So only the calculation to determine the junction temperature with a heatsink is calculated below. Equation (3.16) gives the relationship between the diode's heat and power dissipation.

$$Heat = P_{diode} \quad (3.16)$$

The diode conduction losses can be found in section 3.5.4.

$$Heat = 4.972W$$

Figure 3.18 shows the thermal loop for the diode, and notice that there is a parallel junction to case thermal resistance, since the value given in the datasheet [11] is per diode. The junction temperature can then be calculated using equation (3.17).

$$T_J = \text{Heat} \cdot \left[\left(\frac{R_{JC1} \cdot R_{JC2}}{R_{JC1} + R_{JC2}} \right) + R_{CS} + R_{SA} \right] + T_A \quad (3.17)$$

Substituting the values from the datasheets [11], [16], and [17] into equation (3.17) yields the junction temperature calculated below, which is well below the maximum allowable junction temperature of 150°C for the diode.

$$T_J = 4.972W \cdot \left[\left(\frac{2 \frac{^{\circ}C}{W} \cdot 2 \frac{^{\circ}C}{W}}{2 \frac{^{\circ}C}{W} + 2 \frac{^{\circ}C}{W}} \right) + 0.4 \frac{^{\circ}C}{W} + 9.1 \frac{^{\circ}C}{W} \right] + 25^{\circ}C = 77.2^{\circ}C$$

Figure 3.18 – Diode Thermal Model with Heatsink

3.7 Modification for Battery Load

Since the battery is supplying V_{CC} for the gate driver, the ultra-capacitor that was added to the SuPER cart is a necessity to help regulate the battery voltage when the DC motor is started. If the capacitor is not connected to the circuit, the battery voltage can be pulled down to less than 7V [18]. This becomes a problem because the IRS2117 gate driver has an under voltage lockout (V_{CCUV+}) of 8.6V [8], and if the battery voltage goes below this value the gate driver will turn itself off [19]. The ultra-capacitor must be across the battery to mitigate the voltage sag when the DC motor is turned on.

Another problem associated with having the battery supply V_{CC} to the gate driver is that the bootstrap capacitor cannot be charged initially. Before the gate driver starts to

schematic were tested to determine which one yielded the best noise performance, and actual oscilloscope voltage traces taken during the testing process can be seen in appendices A thru G. C4, C5, C7, and C8 are ceramic capacitors used to filter high frequency transients. C14 is the snubber capacitor used to decrease voltage transients when the diode turns on and off.

Figure 3.20 – Universal Buck Converter Prototype Schematic

3.8.1 Test Setup

The converter was tested using a power supply operating in constant current mode, and an electronic load was connected to the output of the converter. The PWM signal was supplied via a function generator. A separate power supply was used to power the gate driver. Application note [7] recommends separating logic and power ground into two separate paths to help eliminate noise due to the switching of large amounts of current on the power ground. To accomplish this, the grounding scheme of the testing equipment had to be looked at. It turns out that the reference clip on the oscilloscope probe is connected to earth ground, as well as the negative lead of the function generator.

In order to separate power and logic grounds, the function generator's negative lead was used for supplying ground to the gate driver and the gate driver's power supply. The power ground was supplied via the oscilloscope's probe reference clip to the negative terminal of the converter's output.

3.8.2 Different Converter Configuration Noise Results

Table 3.4 summarizes the noise results obtained by testing different configurations of the universal Buck converter, and table 3.5 defines the different configuration numbers seen in table 3.4. In some cases a gate resistor was placed in between the gate driver's output and the MOSFET's gate, which helps reduce noise by decreasing how fast the MOSFET turns on and off. The drain to source voltage (V_{DS}) overshoot occurs when the MOSFET turns off, and the V_{DS} undershoot occurs when the MOSFET turns on. The diode voltage overshoot happens when the diode turns off, and the output voltage transient occurs when the MOSFET turns on.

The best output noise performance was produced by having no gate resistor, and the MBR2045CT Schottky diode snubbed. From table 3.4 the conclusion can be made that the SBR2060CT super barrier diode should not be used as the freewheeling diode due to extremely poor noise performance, even when the diode was snubbed and a 47Ω gate resistor was used. However, application note [21] suggest that the high frequency noise does not really exist on the output of the converter, since the current of the inductor does not produce sharp current steps. The noise doesn't likely exist at the point of measurement, but is phantom noise that the ground lead of the oscilloscope probe produces by picking up EMI. This noise should not pose a problem, unless noise sensitive loads are connected to the output of the converter.

Table 3.4 – Universal Buck Noise Data Table

Configuration	V_{DS} Undershoot (V)	V_{DS} Overshoot (V)	Diode Overshoot (V)	Output Voltage Noise (V_{p-p})
1	-21.75	18.25	20.75	4.25
2	-11.25	18.12	18.12	1.50
3	-7.35	8.25	12.25	2.50
4	-4.44	9.31	3.68	2.50
5	-14.69	7.81	20.31	8.44
6	-16.06	10.19	21.44	10.83
7	-10.19	9.81	14.19	8.55

Table 3.5 – Universal Buck Testing Configurations

Configuration No.	Definition
1	No Gate Resistor and MBR2045CT freewheeling diode
2	No Gate Resistor and 2.2nF snubber across the MBR2045CT freewheeling diode
3	47 Ω Gate Resistor and MBR2045CT freewheeling diode
4	47 Ω Gate Resistor and 2.2nF with 2.2 Ω series resistor snubber across MBR2045CT freewheeling diode
5	47 Ω Gate Resistor and 2.2nF snubber across the SBR2060CT freewheeling diode
6	47 Ω Gate Resistor with 2.2nF snubber across the SBR2060CT freewheeling diode and MOSFET
7	47 Ω Gate Resistor and 2.2nF snubber with 2.2 Ω series resistor across the SBR2060CT freewheeling diode

3.8.3 Efficiency

Configuration number 2 yielded the best output noise performance, so it was selected to be implemented into the SuPER system. The converter's efficiency over a wide range of loads was tested, and the results can be seen in table 3.6. The actual efficiency data, compared to the theoretical efficiency, can be seen in figure 3.21. Notice that the deviation from actual and theoretical values increases as load decreases. One reason for this deviation could be due to the fact that the theoretical calculations used a conservative value for the forward voltage of the freewheeling diode. The forward

voltage was kept constant for all loads, but it actually decreases as load decreases as seen in figure 3.14. At full load the theoretical value efficiency is about 2% lower than the actual measured efficiency.

Table 3.6 – Universal Buck Converter Prototype Efficiency Data

Percent Load	V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Duty Cycle	η (%)
10	34.6	0.45	15.6	11.95	1.26	15.1	33	96.7
20	34.6	0.91	31.5	12.20	2.52	30.7	34	97.6
30	34.6	1.36	47.1	12.15	3.76	45.7	34	97.1
40	34.6	1.80	62.3	12.08	5.00	60.4	34	97.0
50	34.6	2.26	78.2	12.05	6.28	75.7	34	96.8
60	34.7	2.71	94.0	12.00	7.53	90.4	34	96.1
70	34.7	3.16	109.7	11.95	8.78	104.9	34	95.7
80	34.7	3.61	125.3	11.92	10.02	119.4	34	95.3
90	34.7	4.19	145.4	12.23	11.27	137.8	35	94.8
100	34.7	4.66	161.7	12.20	12.53	152.9	35	94.5

Universal Buck Converter Theoretical and Measured Efficiency Comparison

Figure 3.21 – Universal Buck Converter Efficiency Comparison

Chapter 4: Universal Synchronous Buck Converter

By looking at figure 4.1 the only difference between the universal Buck converter and the universal synchronous Buck converter is the addition of a low side switch. The extra switch is to help improve the efficiency of the converter by decreasing the losses associated with the freewheeling diode. Since the conduction losses of a MOSFET are less than that of the diode, the overall efficiency can be improved as long as the MOSFET's switching losses are kept low. The reason why the diode is not removed from the circuit is to allow a path for current to flow during the switching dead time. Switching dead time is added to the circuit because the MOSFETs do not turn off instantaneously. If the high side MOSFET is turned on before the low side MOSFET turns off, the source is essentially shorted to ground which is known as shoot through. If no dead time is added to the circuit shoot through can occur, which only happens during the turn on and off transitions.

Figure 4.1 – Universal Synchronous Buck Converter

4.1 Component Selection

The universal synchronous Buck converter will use several of the same components as the universal Buck converter. The only components that vary from the universal Buck converter are the gate driver and inductor. A gate driver that was capable

of driving both a high and low side switch, and provide a switching deadtime, is required for the universal synchronous Buck converter. Since the universal Buck converter was designed to operate with a switching frequency of 100kHz, the decision was made to design the universal synchronous Buck converter to operate at a lower frequency in the hope of reducing switching losses and increasing the overall efficiency further. The lower frequency will also make the converter more compatible with the gate driver's switching deadtime. A switching frequency of 30kHz was selected in order to cut the MOSFET switching losses to approximately one third of the universal Buck converter. The following parameters were used in the design of the universal synchronous Buck converter.

$$f = 30kHz$$

$$V_{in} = 34.5V$$

$$V_{out} = 12V$$

$$P_{in} = P_{out} = 150W$$

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{150W}{12V} = 12.5A$$

$$D = \frac{V_{out}}{V_{in}} = \frac{12V}{34.5V} = 0.348$$

$$I_{in} = \frac{P_{in}}{V_{in}} = \frac{150W}{34.5V} = 4.348A$$

4.1.1 Gate Driver

Originally an International Rectifier IRS2003 gate driver was going to be used for the universal synchronous Buck converter. As seen in figure 4.2 the IRS2003 has two separate input PWM inputs. The HIN pin controls the high side switch, and the LIN pin controls the low side switch. Instead of using two separate PWM signals to supply HIN and LIN, the two pins were connect together so a single PWM could drive both inputs. However, this created a problem because the LIN pin has about 2.5V on it when it is not grounded by a low input signal. This in turn causes the high side switch to turn on, because the 2.5V is over the input logic high threshold of the HIN pin. If the switch is

turned on, then the PV array is directly connected to the output of the converter. So the HIN and LIN pins cannot be connected together, and the IRS2003 must be driven using two PWM signals.

Figure 4.2 – IRS2003 Gate Driver [22]

To eliminate the need for two PWM signals, another gate driver needed to be selected. An International Rectifier IRS2004 (figure 4.3) was found which uses a single PWM input to drive both high and low side switches. The gate driver also has an input, pin SD, that turns both switches off when a low signal is present. The IRS2004, like the IRS2003, has a deadtime of 520ns to eliminate the possibility of shoot through from occurring.

Figure 4.3 – IRS2004 Gate Driver [23]

4.1.2 Inductor

The minimum inductor value to keep the converter operating in continuous conduction mode down to 10% of full load needs to be calculated. The values from 2.2.2 and 4.1 were substituted into equation (2.16) to determine the minimum inductor value to maintain CCM.

$$L_{\min} = \frac{(1 - 0.348) \cdot 9.6\Omega}{2 \cdot 30kHz} = 104\mu H$$

Now that the minimum inductor value is known to keep the converter operating in continuous conduction mode, a slightly larger inductor is selected to maintain a performance margin. An inductor value around 200 μ H would have been preferred, but a Vishay IHV-15-500 500 μ H 15A inductor was selected since it was the only inductor available through Newark Electronics that could be used. The 500 μ H inductor is 4.8 times larger than the calculated $L_{\min}$ value, and was used in the equations below to determine the inductor current values at 10% full load below. Due to how oversized this inductor is, the switching frequency can be decreased below 30kHz in the future if needed. By substituting the value of L above and $R_{10\%}$ from section 2.2.2 into equations (2.13) and (2.15) the minimum and maximum inductor current values were calculated.

$$I_{\min} = 12V \cdot \left[\frac{1}{9.6\Omega} - \frac{(1 - 0.348)}{2 \cdot 500\mu H \cdot 30kHz} \right] = 0.99A$$

$$I_{\max} = 12V \cdot \left[\frac{1}{9.6\Omega} + \frac{(1 - 0.348)}{2 \cdot 500\mu H \cdot 30kHz} \right] = 1.51A$$

Inserting the maximum and minimum inductor current values into equation (2.21) yields:

$$\Delta i_L = 1.51A - 0.99A = 0.52A$$

4.1.3 Input Capacitor

As a check to make sure the same 3000 μ F of input capacitance used for the universal Buck converter is large enough to produce the input ripple voltage requirement at the lower switching frequency, the input capacitance was calculated. The minimum value for the input capacitor can be calculated by substituting the values found in section 4.1 and table 1.2 into equation (3.3).

$$C_{in(min)} = \frac{4.35A \cdot (1 - 0.348)}{100mV \cdot 30kHz} = 945.4\mu F$$

4.2 Modification for Battery Load

Since the universal synchronous Buck converter has a high and low side switch, there is no need to modify the circuit as was required for the universal Buck converter seen in section 3.7. This is because the low side switch does not use the bootstrap capacitor, so the gate driver can turn on the low side switch even though the high side switch cannot be turned on. Once the low side switch is turned on, the negative terminal of the bootstrap capacitor is grounded and can be charged via the bootstrap diode connected between the V_{CC} and V_B pins of the gate driver. Now that the bootstrap capacitor is charged, the high side switch can be turned on.

One disadvantage of using the NiDAQ's to supply the signal to the SD pin of the gate driver, is that they initialize with a high output when they are first powered up. This will turn the gate driver on since the SD pin has a high signal, and since the PIC is initialized with a duty cycle of zero the low side switch will turn on. With the low side switch turned on, the battery will be connected to ground. To eliminate the possibility of current flowing into the converter from the battery, a diode was placed in between the

converter's output and the battery. This diode will only allow current to flow out of the converter, and block current from flowing into the converter.

The addition of this diode will decrease the overall efficiency of the converter, and should be removed once the problem of the NiDAQs initializing with a high output is solved. A Diodes Incorporated SBR2060CT super barrier rectifier was selected for the output diode, since it has a lower voltage drop than the MBR2045CT being used for the freewheeling diode. The SBR2045CT was not used for the freewheeling diode, because even though it is more efficient it produced very large voltage spikes when the diode would turn on and off. These voltage spikes will not pose a problem when used for the output diode, because in normal operation the diode should always be on.

4.3 Theoretical Efficiency

Since the actual universal synchronous Buck converter will not use ideal components, losses will occur as power is transmitted from the input to the output. In order to predict the converters efficiency at various loads, component losses need to be calculated. These losses include MOSFET switching, MOSFET conduction, MOSFET gate, inductor losses, and diode conduction. Note that the MOSFET gate losses are constant, whereas the other four losses are dependent on the output current. All sample calculations in the following sections are at maximum load.

4.3.1 High Side MOSFET Switching Losses

Substituting the values found in section 4.1 and the datasheet [13] into equation (3.7), the switching losses can be found at full load.

$$P_{sw} = \frac{1}{2} \cdot 34.5V \cdot 12.5A \cdot (95ns + 67ns) \cdot 30kHz + \frac{1}{2} \cdot 430pF \cdot 34.5V^2 \cdot 30kHz = 1.056W$$

4.3.2 High Side MOSFET Conduction Losses

These losses are the same as calculated in section 3.5.2, but will be labeled as

$$P_{cond_high}.$$

4.3.3 Low Side MOSFET Switching Losses

The low side switch should only turn on when the diode is freewheeling during the switching deadtime. Also when the low side switch is trying to turn off the diode will once again freewheel. Due to the fact that the diode will limit the voltage across the MOSFET to its forward voltage, the low side switching losses should be negligible.

4.3.4 Low Side MOSFET Conduction Losses

The conduction losses of the low side MOSFET are calculated using the following formula presented in Mappus [14].

$$P_{cond_low} = I_{out}^2 \cdot R_{ds(on)} \cdot (1 - D) \quad (4.1)$$

Substituting the values from sections 4.1 and the datasheet [13] into equation (4.1) yield the low side MOSFET's conduction losses.

$$P_{cond_low} = (12.5A)^2 \cdot 6.5m\Omega \cdot (1 - 0.348) = 662mW$$

4.3.5 MOSFET Gate Losses

Similar to section 3.5.3, application note [7] calculates the gate losses for two switches as follows:

$$P_{gate} = 2 \cdot V_{GS} \cdot Q_G \cdot f \quad (4.2)$$

Substituting the values from 3.5.3 into equation (4.2) yields the MOSFET's gate losses.

$$P_{gate} = 2 \cdot 12V \cdot 90nC \cdot 30kHz = 65mW$$

4.3.6 Freewheeling Diode Conduction Losses

The diode only conducts during the switching deadtime, and Melito and Belverde [24] calculates the losses if the deadtime occurs only once a period. The IRS2004

produces a switching deadtime twice in one period, so the diode conduction losses would be twice what [24] describes.

$$P_{diode} = 2 \cdot I_o \cdot V_f \cdot t_{deadtime} \cdot f \quad (4.3)$$

Inserting the values from section 3.4.6 into equation (4.3)

$$P_{diode} = 2 \cdot 12.5A \cdot 0.61V \cdot 520ns \cdot 30kHz = 238mW$$

4.3.7 Inductor Losses

According to Vishay [25] the maximum DCR of the IHV-15-500 inductor is $50m\Omega$, and the inductor losses can be calculated using equation (3.11).

$$P_{inductor} = (12.5A)^2 \cdot 50m\Omega = 7.813W$$

4.3.8 Output Diode Conduction Losses

Since the SBR2060CT contains two diodes per package, similar to figure 3.13, they will be connected in parallel. The current per leg through the diode to determine the forward voltage is the same as section 3.4.6. From figure 4.1 the forward voltage (V_f) at 6.25A, using the $25^\circ C$ curve, is approximately 0.43V. The power dissipated by the output diode is calculated using equation (4.4).

$$P_{diode_out} = I_{out} \cdot V_f \quad (4.4)$$

Substituting the output current from 4.4 and the forward voltage found above into equation (4.4) yields:

$$P_{diode_out} = 12.5A \cdot 0.43V = 5.375W$$

Figure 4.4 – SBR2060CT Diode Current Voltage Characteristics Per Leg [26]

4.3.9 Theoretical Efficiency Calculation

The theoretical efficiency is the ratio of the output power over the input power, and the calculation is determined by the equation below. The results from 10% load to full load can be seen in table 4.1. These values will later be compared to the actual results in figure 4.6.

$$\eta = \frac{P_{out}}{P_{total}} = \frac{P_{out}}{P_{out} + P_{sw} + P_{cond_high} + P_{cond_low} + P_{diode} + P_{gate} + P_{inductor} + P_{diode_out}} \quad (4.5)$$

Substituting the appropriate values found in section 4.3.1 through 4.3.8 into equation (4.5) yields the theoretical efficiency of the converter at full load.

$$\eta = \frac{150W}{150W + 1.056W + 0.353W + 0.662W + 0.238W + 0.065W + 7.813W + 5.375W} = \frac{150W}{165.55W} = 90.61\%$$

Table 4.1 – Universal Synchronous Buck Converter Theoretical Efficiency

Percent Load	P _{out} (W)	P _{sw} (W)	P _{cond_high} (W)	P _{cond_low} (W)	P _{diode} (W)	P _{gate} (W)	P _{inductor} (W)	P _{diode_out} (W)	P _{total} (W)	η (%)
10	15.0	0.112	0.004	0.007	0.024	0.065	0.078	0.538	15.83	94.78
20	30.0	0.217	0.014	0.026	0.048	0.065	0.313	1.075	31.76	94.47
30	45.0	0.322	0.032	0.060	0.071	0.065	0.703	1.613	47.87	94.01
40	60.0	0.427	0.057	0.106	0.095	0.065	1.250	2.150	64.15	93.53
50	75.0	0.532	0.088	0.166	0.119	0.065	1.953	2.688	80.61	93.04
60	90.0	0.636	0.127	0.238	0.143	0.065	2.813	3.225	97.25	92.55
70	105.0	0.741	0.173	0.325	0.167	0.065	3.828	3.763	114.06	92.06
80	120.0	0.846	0.226	0.424	0.190	0.065	5.000	4.300	131.05	91.57
90	135.0	0.951	0.286	0.537	0.214	0.065	6.328	4.838	148.22	91.08
100	150.0	1.056	0.353	0.662	0.238	0.065	7.813	5.375	165.55	90.61

4.4 Heat Sink Calculations

Since the freewheeling diode is only dissipating 238mW at full load, a heatsink is not required. The power dissipated by the low side switch should also be quite low, since the conduction losses are only 662mW at full load and the switching losses should be negligible. But to be conservative a heatsink will be added to the low side MOSFET. The same heatsink and insulating pad used for the universal Buck converter will also be used for the universal synchronous Buck converter. Also, an ambient temperature of 25°C will be assumed for the calculations.

4.4.1 High Side MOSFET

Similar to section 3.6.1 the junction temperature can be calculated with and without a heatsink. The amount of heat generated by the MOSFET is calculated by substituting the values from sections 4.3.1 and 4.3.2 into equation (3.13).

$$Heat = 1.056W + 0.353W = 1.409W$$

Using the value of heat calculated above, and the values found in the datasheet [13], the junction temperature without a heat sink can be determined from equation (3.14).

$$T_j = 1.409W \cdot 62 \frac{^{\circ}C}{W} + 25^{\circ}C = 112.4^{\circ}C$$

Although the junction temperature is lower than the maximum allowed temperature, a heatsink will still be used to reduce the junction temperature. Substituting the values from the datasheets [13], [16], and [17] into equation (3.15) yields a more reasonable junction temperature.

$$T_j = 1.409W \cdot \left(0.9 \frac{^{\circ}C}{W} + 0.4 \frac{^{\circ}C}{W} + 9.1 \frac{^{\circ}C}{W} \right) + 25^{\circ}C = 39.7^{\circ}C$$

4.4.2 Output Diode

The amount of heat the output diode will generate is 5.375W at full load.

Substituting the values from [16], [17], [26], and heat into equation (3.17) results in the junction temperature of the diode with a heatsink. The resulting temperature is less than the maximum allowable temperature of 150°C.

$$T_j = 5.375W \cdot \left[\left(\frac{2 \frac{^{\circ}C}{W} \cdot 2 \frac{^{\circ}C}{W}}{2 \frac{^{\circ}C}{W} + 2 \frac{^{\circ}C}{W}} \right) + 0.4 \frac{^{\circ}C}{W} + 9.1 \frac{^{\circ}C}{W} \right] + 25^{\circ}C = 81.4^{\circ}C$$

4.5 Universal Synchronous Buck Converter Prototype Testing

A prototype was built using the previously mentioned components, and tested in a lab using a power supply. Figure 4.5 shows the final universal synchronous Buck converter prototype schematic, used for efficiency testing in section 4.5.3. Several versions of this schematic were tested to determine which one yielded the best noise performance, and actual oscilloscope voltage traces taken during the testing process can

be seen in appendix H thru K. C4, C5, C7, and C8 are ceramic capacitors used to filter high frequency transients. In order to increase the time it takes the MOSFETs to turn on, and decrease their turn off time, D4 and D5 were added in parallel to the gate resistor.

Figure 4.5 – Universal Synchronous Buck Converter Prototype Schematic

4.5.1 Test Setup

The test setup was similar to that of section 3.8.1, except the power supply for the gate driver also supplied the SD pin's logic input to enable the gate driver.

4.5.2 Different Converter Configuration Noise Results

The testing results can be seen in table 4.2, and the configuration number definitions are seen in table 4.3. Once again the SBR2060CT super barrier diode yielded the poorest noise performance of the group. The best performing configuration was number 2, which consisted of a 47Ω Gate Resistor, gate diode, and MBR2045CT freewheeling diode. The V_{DS} overshoot and V_{DS} undershoot data are missing for

configuration 4, because the circuit was damaged while moving the oscilloscope probe from one measurement point to another.

Table 4.2 – Universal Synchronous Buck Noise Data Table

Configuration	V_{DS} Undershoot (V)	V_{DS} Overshoot (V)	Diode Overshoot (V)	Output Voltage Noise (V_{p-p})
1	-6.88	9.375	10.63	1.21
2	-9.63	12.25	8.63	1.00
3	-14.44	15.56	10.13	8.00
4			7.13	7.75

Table 4.3 – Universal Synchronous Buck Testing Configurations

Configuration No.	Definition
1	47 Ω Gate Resistor and MBR2045CT freewheeling diode
2	47 Ω Gate Resistor, gate diode, and MBR2045CT freewheeling diode
3	47 Ω Gate Resistor, gate diode, and SBR2060CT freewheeling diode
4	47 Ω Gate Resistor, gate diode, and 2.2nF snubber across SBR2060CT freewheeling diode

4.5.3 Efficiency

Since configuration number 2 yielded the best output noise performance, it was selected to be implemented into the SuPER system. The converter's efficiency over a wide range of loads was tested, and the results can be seen in table 4.4. The actual efficiency data, compared to the theoretical efficiency, can be seen in figure 4.6. Notice that the deviation from actual and theoretical values increases as load decreases. One reason for this deviation could be due to the fact that the theoretical calculations used a conservative values for the forward voltage of the freewheeling and output diodes. The forward voltage was kept constant for all loads, but it actually decreases as load decreases as seen in figure 4.4. At full load the theoretical value efficiency is about 0.25% lower than the actual measured efficiency.

Table 4.4 – Actual Universal Synchronous Buck Converter Efficiency Data

Percent Load	V _{in} (V)	I _{in} (A)	P _{in} (W)	V _{out} (V)	I _{out} (A)	P _{out} (W)	Duty Cycle	η (%)
10	34.7	0.46	16.0	11.98	1.26	15.1	36	94.6
20	34.7	0.91	31.6	12.03	2.52	30.3	37	96.0
30	34.7	1.35	46.8	11.92	3.76	44.8	37	95.7
40	34.7	1.84	63.8	12.12	5.02	60.8	38	95.3
50	34.7	2.30	79.8	12.02	6.28	75.5	38	94.6
60	34.7	2.76	95.8	11.92	7.53	89.8	38	93.7
70	34.7	3.32	115.2	12.20	8.78	107.1	40	93.0
80	34.7	3.79	131.5	12.10	10.02	121.2	40	92.2
90	34.7	4.26	147.8	12.00	11.27	135.2	40	91.5
100	34.7	4.87	169.0	12.25	12.53	153.5	41	90.8

Universal Synchronous Buck Converter Theoretical and Measured Efficiency Comparison

Figure 4.6 - Universal Synchronous Buck Converter Efficiency Comparison

4.5.4 Efficiency Comparison with Universal Buck Converter

Now that data for both the universal Buck and synchronous Buck converter was obtained, a side by side comparison can be made. Figure 4.7 shows the efficiency plot of each converter from 10% to 100% of full load. The universal Buck converter is slightly more efficient than the synchronous version over the wide range of loads. But remember that the synchronous version has the output diode connected in between the converter and the load. This diode absorbs around 5.375W at full load, but in the future this diode can be removed to enhance the converters efficiency. Also, since the inductor is much larger than required for the 30kHz switching frequency, a smaller replacement inductor with a lower DCR can decrease the copper losses of the converter.

Figure 4.7 – Converter Prototypes Efficiency Comparison

Chapter 5: Converter Implementation into SuPER

Now that a universal Buck and universal synchronous Buck have been tested in a lab and proven to function properly, they now need to be implemented into the SuPER system to test the control algorithm.

5.1 SuPER Control System as Found

Since the PIC has the switching frequency and initial duty cycle hard coded in its memory, it does not need any signal from the laptop to produce a squarewave output. When the PIC was energized it initialized with a static squarewave having a switching frequency of 95kHz and a duty cycle of 57 percent. Since the control code is not running on the laptop the PIC cannot generate a PWM signal. This is a problem because at the PV array's MPP, only a 35 percent duty cycle is required to produce a 12V output. The 57 percent duty cycle will produce almost 20V on the output, and with no control code running to decrease the duty cycle the output voltage will remain high.

The *pnopal.c* control code on the laptop was then looked at and found to only have code written to perform MPPT. However, the code never looked at the battery's voltage, just the power of the PV array. This is a problem because without a battery voltage feedback the output voltage of the converter is never regulated. The program will only try to get the maximum power out of the array, which is bad if there is a small load on the system and the PV array is capable of supplying a large amount of power. If the MPPT algorithm is running, the duty cycle will change to get the maximum power out of the PV array, which will raise the output voltage to increase the power supplied by the converter until MPP is found. This will result in the small load being destroyed, since it is not meant to operate at such a high voltage.

5.2 Simulink Simulation Control Code

It is not known why the PIC was programmed to initialize at a 57 percent duty cycle, but it was reprogrammed to initialize at a zero percent duty cycle. The control algorithm was adjusted to implement the code found in Sheffield [3], used for the simulink SuPER system simulation. The only part of the algorithm found in Sheffield [3] that was changed was the duty cycle step. The code in Sheffield [3] used a 2.5% step in duty cycle, but this step is too large and decreases the chances of operating at the MPP of the array. A 0.25% duty cycle step change was used instead, in order to allow for finer adjustments of the converter. The *pnopal.c* code was then modified so the system could be tested with the new algorithm.

5.2.1 Implementation

Figure 5.1 shows a flow chart that represents the control algorithm. It has two modes of operation, Bulk and Float, and is initialized to start in bulk mode. Bulk mode is used when there is a large load on the system, or the battery is in a low state of charge. Float mode is used when there is a light load on the system, or the battery is in a high state of charge. The algorithm works as follows:

- 1) Sensor data is taken and the algorithm starts to run.
- 2) If the power out of the array is less than 3W, and the converter is in Bulk mode, the duty cycle will increase.
- 3) If the array power is not less than 3W, and the battery voltage is less than 13.7V, the MPPT algorithm is implemented. The counter used to determine if the converter will change to Float mode is also reset to zero.

- 4) If the converter is operating in Bulk mode, and the battery's voltage exceeds 13.7V, the Float mode counter is incremented by one. If the Float mode counter exceeds one, then the duty cycle is decreased and the mode of operation is changed to Float mode. If the counter is not greater than one, then nothing happens. The counter is used so two consecutive readings are required to change the converter to operate in Float mode.
- 5) If the converter is operating in Float mode, and the battery voltage is greater than 13.4V, the duty cycle is decreased.
- 6) Once the battery voltage is less than 13.4V the system does nothing until the battery voltage is less than 12.7V. At that point the mode of operation is changed to Bulk mode.

Figure 5.1 – Simulink Control Code Flowchart

5.2.2 Results

Since the duty cycle is initialized to zero, it takes a long time for the converter to reach a duty cycle close to normal operation. This is because the program updates the PWM once every second, and since very little power is being supplied by the array the MPPT algorithm doesn't work well. When the current supplied by the PV array is close to zero, it can be sensed as negative. This ends up affecting the MPPT algorithm because the change of power can be calculated as negative even though it could be positive. In this case it took almost an hour to reach a 35% duty cycle.

5.3 Improved Control Algorithm

This section discusses improving the Simulink control code to increase the performance of the converter.

5.3.1 Improvements

Since the original system refreshed the duty cycle every second, and these changes were made a quarter of a percent at a time, the code responded very slowly to large changes in load. The duty cycle refresh rate was changed to five times a second, making the response to load variations five times as fast. This also made the converter capable of finding the MPP faster than the original refresh rate. The faster the program can find the MPP, the less time the battery supplies power that could be coming from the PV array.

Also, the original code never addressed severe overvoltage situation, and protecting the system from it. A decision was made that the battery voltage should never exceed 15V if the system is functioning properly. Another mode of operation was added called Safety Off, which changes the duty cycle to zero if the battery voltage is sensed to be above 15V. The zero percent duty cycle stops power from being supplied by the PV array to the battery.

To avoid the long time it took the converter to reach a 35% duty cycle, another mode of operation was added called Initial. This mode will increase the duty cycle in 5% steps until the duty cycle reaches 35%. Once the duty cycle reaches 35% the mode of operation changes to Bulk and the MPPT algorithm can begin. This way the MPPT algorithm is not involved in increasing the duty cycle from 0% to 35%. If the battery voltage is ever sensed to be above 13.7V while in initial mode, the mode of operation will

change to Bulk mode. Once in Bulk mode the converter will switch to float mode if the battery's voltage is above 13.7V for two iterations of the code. The improved algorithm can be seen in figure 5.2.

Figure 5.2 – Improved Control Code Flowchart

5.3.2 Results

The SuPER system was tested with the improved control algorithm which worked quite well. The program was started and the duty cycle increased to 35%. After which it switched to Bulk mode and started to perform MPPT. Once the converter started to charge the battery the Mode of Operation Board was set to Charging, and the ultra-capacitor was charged. After the capacitor was fully charged the Mode of Operation

Board was changed to Normal, and the laptop and refrigerator were added as loads. The program was still running in Bulk mode, and the MPPT algorithm eventually adjusted the duty cycle to 56.4% to supply 120W from the PV array (apparently the most power ever observed being supplied by the PV array with the off the shelf converter was 120W). At this point the converter was supplying both the laptop and fridge, as well as charging the battery. When the laptop and fridge were disconnected from the system, the converter went into Float mode and the duty cycle was decreased.

Under heavy loads if the duty cycle gets too high, the converters output voltage will start to decrease. This is because the PV array does not have enough time to replenish the charge of the input capacitor when the switch is off.

5.3.3 Converter Control Code Difference

The same control code can be used for both the Buck and synchronous Buck converter. The only difference between the two is that the switching frequency of the PIC must be programmed to supply 100kHz for the universal Buck and 30kHz for the universal synchronous Buck converter. Also, the DEV 2 P06 NiDAQ port will supply the universal synchronous Buck converter's gate driver shutdown signal, which turns the driver on and off.

Chapter 6: Conclusion

The goal of having a Cal Poly built DC-DC converter was finally realized this quarter by completing both the universal Buck and universal synchronous Buck converter prototypes. This section concludes the work done on the SuPER project and discusses achievements and recommendations for future improvements.

6.1 Achievements

Both the universal Buck and universal synchronous Buck topologies presented in this thesis were successfully implemented into the SuPER system. Both converters can perform the same functions as the off-the-shelf DC-DC converter that was previously used in the SuPER system. With the future development of the PWM control algorithm, and an increased understanding of the battery, the converters have the possibility of outperforming the off-the-shelf model when it comes to extending the life of the battery.

The limitations of the standard Buck converter topology, with a current source input, were successfully overcome with the addition of the input capacitor used by the universal topologies presented in this thesis. The equations to determine the minimum input capacitor size and the RMS current rating were derived and proven to be valid via PSpice simulation. By adding the input capacitor, the PV array's constant current can be successfully stepped up without the use of a transformer. This makes the converters lighter and cheaper than topologies that use transformers, such as current fed, since capacitors weigh and cost less than a transformer.

Both the universal Buck and universal synchronous Buck converter prototypes have their own strong points and weak points. The universal Buck converter currently has a higher efficiency than the synchronous version, but has a more complicated gate

drive circuit due to the battery load and PIC interface. The synchronous Buck converter has a lower efficiency, but a much simpler gate driver circuit. Since the synchronous version has the potential of becoming more efficient than the universal Buck converter if the recommendation presented in the following section are implemented, it should be the converter used by the SuPER system. This will allow time for the bugs to be worked out with the control scheme using the prototype, while a more efficient version is being developed.

Although there is still room for improvement when it comes to the PWM control algorithm, the current version is a significant improvement over the code that was originally found operating on the system. The original code would have eventually destroyed the loads connected to the converter, and possibly cause thermal degradation of the battery, since the code had no battery voltage feedback. The new algorithm monitors not only the PV array's voltage and current, but the battery's voltage as well. This eliminates the possibility of damaging any of the loads connected to the converter, because the algorithm adjusts the duty cycle accordingly based on the battery's voltage.

6.2 Future Recommendations

The current NiDAQ's should be replaced with ones that output low when they are initialized, since the current ones output high when they first receive power. This causes a problem because the SD pin of the universal synchronous Buck converter will turn on the gate driver, even though it should be off. By replacing the NiDAQ's with an alternate solution that keeps this from occurring, the reliability of the system can be increased. This will also allow the removal of the output diode to take place, since there will no

longer be a possibility of inadvertently grounding the battery through the converters low side switch.

Since the low side MOSFET losses combined with the freewheeling diode conduction losses of the synchronous converter are less than the Buck version's freewheeling diode conduction losses, the synchronous version has the potential of having a higher efficiency. The power dissipated by the inductor in the synchronous version is one reason why a smaller inductor, which should have a lower DCR, is preferred. If a more suitable inductor cannot be found for a switching frequency of 30kHz, increase the switching frequency to 100kHz and use the same inductor as the Buck converter. Or, an alternate inductor with a lower DCR should be selected if at all possible. The synchronous Buck converter should then be more efficient than the Buck version, as long as the output diode can be removed.

Currently the output diode of the synchronous versions is extremely hot with 12.5A running through it. Even though the thermal calculation determined the junction temperature to be within the diodes normal operating range, a different heatsink with a lower thermal resistance should be used to reduce the chances of someone being burned.

Since the control loop of the SuPER system has finally been closed, the necessity of the Mode of Operation Board that was added for the ultra-capacitor should be looked at. Before there was no way of controlling the off the shelf converter when it came to charging the ultra-capacitor. But if a MOSFET is added in between the battery and load bus, it could be used to disconnect the battery from the load bus. If the battery is disconnected, then a 100% duty cycle can be supplied by the PIC, turning the high side switch on. This will draw short circuit current from the PV array, which is less than five

amps, and charge the ultra-capacitor eliminating the need for the charging resistor. Once the load bus voltage is sensed to be within a certain range of the battery's voltage, the duty cycle can be changed to zero which turns off the high side switch and stops the ultra-capacitor from being charged. The MOSFET connecting the battery to the load bus can then be turned on to connect the ultra-capacitor across the battery. However, there still will be a need for a discharging resistor to discharge the capacitor when needed, to remain compliant with NEC according to Baskin [27].

The main reason for including appendices A through K is so the future students working on the converters have a visual record of what the voltage waveforms looked like at different locations on the converters. This way they will have a visual representation of how the converter behaved under different modifications. Also, they might recognize a phenomenon from the images, and know how to fix it. For this reason very little detail discussing the waveforms in the previously mentioned appendixes was included.

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Appendix A: Universal Buck Converter Testing Configuration 1

This section shows the voltage waveforms at various locations on the universal Buck converter, under configuration 1 constraints. The switching frequency was supplied by a function generator and set at 100kHz, and the gate driver was supplied with 13.8V. The converter was constructed with no gate resistor, or snubber across the MBR2045CT freewheeling diode.

A.1 No Load Waveforms

The rise and fall time of the MOSFET's gate voltage at no load can be seen in figure A.1 and A.2. At this point the converter was not connected to the power supply representing the PV array. The rise time equaled 380ns with a fall time of 160ns. By looking at the output voltage on these two figures, noise is present when the gate voltage goes high and low, even with no input or load on the converter. Figures A.3, and A.4, show the noise frequency to be 83MHz during both turn on and off transitions.

Figure A.1 – V_{gate} Rise Time (Ch 1) and V_{out} (Ch 2)

Figure A.2 – V_{gate} Fall Time (Ch 1) and V_{out} (Ch 2)

Figure A.3 – V_{gate} (Ch1) and V_{out} (Ch 2) During MOSFET Turn On

Figure A.4 – V_{gate} (Ch1) and V_{out} (Ch 2) During MOSFET Turn Off

A.2 Full Load Waveforms

The converter was then tested at full load and table A.1 shows the conditions during testing. Figure A.5 shows the maximum and minimum gate voltage value, while Figure A.6 shows the maximum, minimum, and average output voltage. The output voltage was then zoomed in to get a better image of the noise in figure A.7. Figure A.8 shows the input voltage coming out of the buffer and going into the gate driver. The diode's voltage undershoot that occurs when the diode turns on, and the overshoot that occurs when the diode turns off, can be seen in figures A.9 and A.10. To measure the MOSFET's drain to source voltage with the oscilloscope, the drain voltage and source voltage must be measured using two different channels as seen in figure A.11. Using the math function on the oscilloscope, the source voltage can be subtracted from the drain voltage and displayed on the scope. Figures A.12 and A.13 show the MOSFET's drain to source voltage undershoot and overshoot.

Table A.1 – Full Load Conditions for Configuration 1

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Duty Cycle	η (%)
34.6	4.45	154	11.34	12.52	142	35	92.2

Figure A.5 – V_{gate} Measurement (Ch 1) and V_{out} (Ch 2)

Figure A.6 – V_{gate} (Ch 1) and V_{out} Measurement (Ch 2)

Figure A.7 – V_{gate} (Ch 1) and Zoomed in V_{out} (Ch 2)

Figure A.8 – V_{gate} (Ch 1) and Gate Driver PWM Input (Ch 2)

Figure A.9 – V_{gate} (Ch 1) and V_{diode} Undershoot (Ch 2)

Figure A.10 – V_{gate} (Ch 1) and V_{diode} Overshoot (Ch 2)

Figure A.11 – MOSFET Drain Voltage (Ch 1) and MOSFET Source Voltage (Ch 2)

Figure A.12 – V_{DS} Turn On Undershoot

Figure A.13 – V_{DS} Turn Off Overshoot

Appendix B: Universal Buck Converter Testing Configuration 2

This section shows the voltage waveforms at various locations on the universal Buck converter, under configuration 2 constraints. The switching frequency was supplied by a function generator and set at 100kHz. The converter was constructed with no gate resistor, and a 2.2nF snubber across the MBR2045CT freewheeling diode.

B.1 Full Load Waveforms

The converter was tested at full load and table B.1 shows the conditions during testing. Figure B.1 shows the maximum and minimum gate voltage value, while Figure B.2 shows the maximum, minimum, and average output voltage. The output voltage was then zoomed in to get a better image of the noise in figure B.3. The diode voltage undershoot that occurs when the diode turns on, and the overshoot that occurs when the diode turns off, can be seen in figures B.4 and B.5. To measure the MOSFET's drain to source voltage with the oscilloscope, the drain voltage and source voltage must be measured using two different channels as seen in figure B.6. Figures B.6 and B.7 measure the MOSFET's source voltage overshoot and undershoot. By using the math function on the oscilloscope, the source voltage can be subtracted from the drain voltage and displayed on the scope. Figures B.8 and B.9 show the MOSFET's drain to source voltage undershoot and overshoot.

Table B.1 – Full Load Conditions for Configuration 2

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Duty Cycle	η (%)
34.4	4.70	161.7	12.02	12.53	150.6	37	93.1

Figure B.1 – V_{gate} Measurements (Ch1) and V_{out} (Ch 2)

Figure B.2 – V_{gate} (Ch1) and V_{out} Measurements (Ch 2) with Snubber

Figure B.3 – V_{gate} (Ch1) and V_{out} Zoomed In (Ch 2)

Figure B.4 – V_{gate} (Ch1) and V_{diode} Turn On Undershoot (Ch 2)

Figure B.5 – V_{gate} (Ch1) and V_{diode} Turn Off Overshoot (Ch 2)

Figure B.6 – MOSFET Drain Voltage (Ch 1) and MOSFET Source Voltage (Ch 2)

Figure B.7 – MOSFET Drain Voltage (Ch 1) and

Figure B.8 – V_{DS} Turn On Undershoot

Figure B.9 – V_{DS} Turn Off Overshoot

Appendix C: Universal Buck Converter Testing Configuration 3

This section shows the voltage waveforms at various locations on the universal Buck converter, under configuration 3 constraints. The switching frequency was supplied by a function generator and set at 100kHz. The converter was constructed with a 47Ω gate resistor, and no snubber across the MBR2045CT freewheeling diode.

C.1 No Load Waveforms

The rise and fall time of the MOSFET's gate voltage at no load can be seen in figure C.1 and C.2. At this point the converter was not connected to the power supply representing the PV array. The rise time equaled 850ns with a fall time of 660ns. By looking at the output voltage on these two figures, noise is present when the gate voltage goes high and low, even with no input or load on the converter. Figures C.3 and C.4 show the frequency of the noise to be 119MHz during turn on and 15MHz during the turn off transitions.

Figure C.1 – V_{gate} Rise Time (Ch 1) and V_{out} (Ch 2)

Figure C.2 – V_{gate} Fall Time (Ch 1) and V_{out} (Ch 2)

Figure C.3 – V_{gate} (Ch1) and V_{out} Noise (Ch 2) During MOSFET Turn On

Figure C.4 – V_{gate} (Ch1) and V_{out} Noise (Ch 2) During MOSFET Turn Off

C.2 Full Load Waveforms

The converter was then tested at full load and table C.1 shows the conditions during testing. Figure C.5 shows the maximum and minimum gate voltage value, while Figure C.6 shows the maximum, minimum, and average output voltage. The output voltage was then zoomed in to get a better image of the noise in figure C.7. Figure C.8 shows the input voltage coming out of the buffer and going into the gate driver. The diode voltage undershoot that occurs when the diode turns on, and the overshoot that occurs when the diode turns off, can be seen in figure C.9. To measure the MOSFET's drain to source voltage with the oscilloscope, the drain voltage and source voltage must be measured using two different channels as seen in figure C.10. Using the math function on the oscilloscope, the source voltage can be subtracted from the drain voltage and displayed on the scope. Figures C.11 and C.12 show the MOSFET's drain to source voltage undershoot and overshoot.

Table C.1 – Full Load Condition for Configuration 3

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Duty Cycle	η (%)
33.3	4.92	163.8	11.98	12.53	150.1	35	91.6

Figure C.5 – V_{gate} Measurements (Ch1) and V_{out} (Ch 2)

Figure C.6 – V_{gate} (Ch1) and V_{out} Measurements (Ch 2)

Figure C.7 – V_{gate} (Ch1) and V_{out} Zoomed In (Ch 2)

Figure C.8 – V_{gate} (Ch 1) and Gate Driver PWM Input (Ch 2)

Figure C.9 – V_{gate} (Ch1) and V_{diode} (Ch 2)

Figure C.10 – MOSFET Drain Voltage (Ch 1) and MOSFET Source Voltage (Ch 2)

Figure C.11 – V_{DS} Turn On Undershoot

Figure C.12 – V_{DS} Turn Off Overshoot

Appendix D: Universal Buck Converter Testing Configuration 4

This section shows the voltage waveforms at various locations on the universal Buck converter, under configuration 4 constraints. The switching frequency was supplied by a function generator and set at 100kHz. The converter was constructed with a 47Ω gate resistor, and a 2.2nF capacitor with a 2.2Ω series resistor snubber across the MBR2045CT freewheeling diode.

D.1 Full Load Waveforms

The converter was then tested at full load and table D.1 shows the conditions during testing. Figure D.1 shows the maximum, minimum, and average output voltage. The output voltage was then zoomed in to get a better image of the noise in figure D.2. The diode voltage overshoot, that occurs when the diode turns off, can be seen in figure D.3. To measure the MOSFET's drain to source voltage with the oscilloscope, the drain voltage and source voltage must be measured using two different channels as seen in figure D.4. Using the math function on the oscilloscope, the source voltage can be subtracted from the drain voltage and displayed on the scope. Figures D.5 and D.6 show the MOSFET's drain to source voltage undershoot and overshoot.

Table D.1 – Full Load Conditions for Configuration 4

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Duty Cycle	η (%)
33.9	4.91	166.4	11.98	12.53	150.1	34	90.2

Figure D.1 – V_{gate} (Ch1) and V_{out} Measurements (Ch 2)

Figure D.2 – V_{gate} (Ch1) and V_{out} Zoomed In (Ch 2)

Figure D.3 – V_{gate} (Ch1) and V_{diode} Turn Off Overshoot (Ch 2)

Figure D.4 – MOSFET Drain Voltage (Ch 1) and MOSFET Source Voltage (Ch 2)

Figure D.5 – V_{DS} Turn On Undershoot

Figure D.6 – V_{DS} Turn Off Overshoot

Appendix E: Universal Buck Converter Testing Configuration 5

This section shows the voltage waveforms at various locations on the universal Buck converter, under configuration 5 constraints. The switching frequency was supplied by a function generator and set at 100kHz. The converter was constructed with a 47Ω gate resistor, and a 2.2nF snubber across the SBR2060CT freewheeling diode.

E.1 No Load Waveforms

Figure E.1 measures the amplitude of the output noise with no load or input to the converter.

Figure E.1 – V_{gate} (Ch1) and V_{out} (Ch 2) No Load

E.2 Full Load Conditions

The converter was then tested at full load and table E.1 shows the conditions during testing. Figure E.2 shows the output voltage noise measurement. The output

voltage was then zoomed in to get a better image of the noise in figure E.3. The diode voltage overshoot, that occurs when the diode turns off, can be seen in figure E.4. To measure the MOSFET's drain to source voltage with the oscilloscope, the drain voltage and source voltage must be measured using two different channels as seen in figure E.5. Using the math function on the oscilloscope, the source voltage can be subtracted from the drain voltage and displayed on the scope. Figures E.6 and E.7 show the MOSFET's drain to source voltage undershoot and overshoot.

Table E.1 – Full Load Conditions for Configuration 5

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Duty Cycle	η (%)
34.1	4.81	164	11.98	12.53	150.1	35	91.5

Figure E.2 – V_{gate} (Ch1) and V_{out} Measurements (Ch 2)

Figure E.3 – V_{gate} (Ch1) and V_{out} Zoomed In (Ch 2)

Figure E.4 – V_{gate} (Ch1) and V_{diode} Turn Off Overshoot (Ch 2)

Figure E.5 – MOSFET Drain Voltage (Ch 1) and MOSFET Source Voltage (Ch 2)

Figure E.6 – V_{DS} Turn On Undershoot

Figure E.7 – V_{DS} Turn Off Overshoot

Appendix F: Universal Buck Converter Testing Configuration 6

This section shows the voltage waveforms at various locations on the universal Buck converter, under configuration 6 constraints. The switching frequency was supplied by a function generator and set at 100kHz. The converter was constructed with a 47Ω gate resistor, and a 2.2nF snubber across the SBR2060CT freewheeling diode and MOSFET.

F.1 No Load Waveforms

Figure E.1 measures the amplitude of the output noise with no load or input to the converter.

Figure F.1 – V_{gate} (Ch1) and V_{out} Measurements (Ch 2)

F.2 Full Load Condition

The converter was then tested at full load and table F.1 shows the conditions during testing. Figure F.2 shows the maximum, minimum, and average output voltage measurements. The output voltage was then zoomed in to get a better image of the noise in figure F.3. The diode voltage overshoot, that occurs when the diode turns off, can be seen in figure F.4. To measure the MOSFET's drain to source voltage with the oscilloscope, the drain voltage and source voltage must be measured using two different channels as seen in figure F.5. Using the math function on the oscilloscope, the source voltage can be subtracted from the drain voltage and displayed on the scope. Figures F.6 and F.7 show the MOSFET's drain to source voltage undershoot and overshoot.

Table F.1 – Full Load Conditions for Configuration 6

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Duty Cycle	η (%)
33.8	4.81	162.6	11.9	12.53	149.1	35	91.7

Figure F.2 – V_{gate} (Ch1) and V_{out} Measurements (Ch 2)

Figure F.3 – V_{gate} (Ch1) and V_{out} Zoomed In (Ch 2)

Figure F.4 – V_{gate} (Ch1) and V_{diode} Turn Off Overshoot (Ch 2)

Figure F.5 – MOSFET Drain Voltage (Ch 1) and MOSFET Source Voltage (Ch 2)

Figure F.6 – V_{DS} Turn On Undershoot

Figure F.7 – V_{DS} Turn Off Overshoot

Appendix G: Universal Buck Converter Testing Configuration 7

This section shows the voltage waveforms at various locations on the universal Buck converter, under configuration 7 constraints. The switching frequency was supplied by a function generator and set at 100kHz. The converter was constructed with a 47Ω gate resistor, and a 2.2nF capacitor and 2.2Ω series snubber across the SBR2060CT freewheeling diode.

G.1 No Load Waveforms

Figure E.1 measures the amplitude of the output noise with no load or input to the converter.

Figure G.1 – V_{gate} (Ch1) and V_{out} (Ch 2) No Load

G.2 Full Load Waveforms

The converter was then tested at full load and table G.1 shows the conditions during testing. Figure G.2 shows the output voltage noise measurement. The diode voltage overshoot, that occurs when the diode turns off, can be seen in figure G.3. To measure the MOSFET's drain to source voltage with the oscilloscope, the drain voltage and source voltage must be measured using two different channels as seen in figure G.4. Using the math function on the oscilloscope, the source voltage can be subtracted from the drain voltage and displayed on the scope. Figures G.5 and G.6 show the MOSFET's drain to source voltage undershoot and overshoot.

Table G.1 – Full Load Conditions for Configuration 7

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Duty Cycle	η (%)
33.4	4.81	160.7	11.65	12.53	146.0	35	90.9

Figure G.2 – V_{gate} (Ch1) and V_{out} (Ch 2)

Figure G.3 – V_{gate} (Ch1) and V_{diode} Turn Off Overshoot (Ch 2)

Figure G.4 – MOSFET Drain Voltage (Ch 1) and MOSFET Source Voltage (Ch 2)

Figure G.5 – V_{DS} Turn On Undershoot

Figure G.6 – V_{DS} Turn Off Overshoot

G.3 Battery Load Waveforms

While the converter was still setup in configuration 7, a Yuasa NP7-12 12V motorcycle battery was connected to the output of the converter. The battery voltage was then used to supply the gate driver, but the negative node of the battery was not connected to ground via function generator but rather the scope probe reference clip. Table G.2 shows the operating conditions during testing. Figure G.7 shows the bootstrap capacitor's voltage reference to ground. An interesting phenomenon can be seen in figure G.8 when the duty cycle is reduced down to 20%, which looks the inductor is going into discontinuous conduction mode. The bootstrap capacitor's voltage floats on top of diodes cathode voltage. Since the duty cycle is so low, it appears not enough energy is being transferred to the inductor to keep the diode freewheeling during the entire off time of the MOSFET. This would cause the inductor to go into discontinuous conduction mode. The MOSFET's on time is measured in figure G.8, and when it is divided by the switching period produces a 21% duty cycle. So the oscillation are definitely occurring when the switch is off.

Table G.2 – Condition for Charging Motorcycle Battery

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Duty Cycle	η (%)
24.7	0.25	6.18	14.65	0.41	6.01	55	97.2

Figure G.7 – Bootstrap Capacitor Voltage (Ch 1) and V_{out} (Ch 2)

Figure G.8 – Bootstrap Capacitor Voltage (Ch 1) and V_{out} (Ch 2)

Appendix H: Universal Synchronous Buck Converter Testing Configuration 1

This section shows the voltage waveforms at various locations on the universal synchronous Buck converter, under configuration 1 constraints. The switching frequency was supplied by a function generator and set at 30kHz. The converter was constructed with a 47 Ω gate resistor, and no snubber across the MBR2045CT freewheeling diode.

H.1 No Load Waveforms

At this point the converter was not connected to the power supply representing the PV array. Figure H.1 shows noise on the high side gate when the low side gate goes high, and figure H.2 shows noise on the low side gate turns on. The high side switch turn on and off transition deadtime is measured in figure H.3 and H.4. Figures H.5 and H.6 shows the output's peak and oscillating frequency to be 200mV and 323kHz. The rise and fall time of the MOSFET's gate voltage at no load can be seen in figure H.7 and H.9. The rise time equals 820ns with a fall time of 700ns. By looking at the output voltage on these two figures, noise is present when the gate voltage goes high and low, even with no input or load on the converter.

Figure H.1 – V_{gate} High Side Noise (Ch 1) and V_{gate} Low Side (Ch 2)

Figure H.2 – V_{gate} High Side (Ch 1) and V_{gate} Low Side Noise (Ch 2)

Figure H.3 – V_{gate} High Side (Ch 1) and V_{gate} Low Side (Ch 2) During PWM High

Figure H.4 – V_{gate} High Side (Ch 1) and V_{gate} Low Side (Ch 2) During PWM Low

Figure H.5 – V_{gate} High Side (Ch 1) and V_{out} Peak Oscillation (Ch 2)

Figure H.6 – V_{gate} High Side (Ch 1) and V_{out} Oscillation Frequency (Ch 2)

Figure H.7 – V_{gate} High Side Rise Time (Ch 1) and V_{out} (Ch 2)

Figure H.8 – V_{gate} High Side Fall Time (Ch 1) and V_{out} (Ch 2)

H.2 Full Load Waveforms

The converter was then tested at full load and table H.1 shows the conditions during testing. Figure H.9 shows the maximum and minimum gate voltage measurements of the high side switch, while figure H.10 shows the maximum, minimum, and average output voltage. The output voltage was then zoomed in to get a better image

of the noise in figure H.11. Figure H.12 and H.13 shows the PWM signal going into the gate driver, compared to the high side and low side gate voltages. The diode voltage overshoot, that occurs when the diode turns off, can be seen in figures H.14 and H.15 compared to the high side and low side gate voltages. To measure the high side MOSFET's drain to source voltage with the oscilloscope, the drain voltage and source voltage must be measured using two different channels as seen in figure H.16. Using the math function on the oscilloscope, the source voltage can be subtracted from the drain voltage and displayed on the scope. Figures H.17 and H.18 show the high side MOSFET's drain to source voltage undershoot and overshoot.

Table H.1 – Full Load Conditions for Configuration 1

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Duty Cycle	η (%)
34.6	4.78	165.4	12.25	12.53	153.5	35	92.8

Figure H.9 – V_{gate} High Side Measurements (Ch 1) and V_{out} (Ch 2)

Figure H.10 – V_{gate} High Side (Ch 1) and V_{out} Measurements (Ch 2)

Figure H.11 – V_{gate} High Side (Ch 1) and V_{out} Measurements (Ch 2)

Figure H.12 – V_{gate} High Side (Ch 1) and Gate Driver PWM Input (Ch 2)

Figure H.13 – V_{gate} Low Side (Ch 1) and Gate Driver PWM Input (Ch 2)

Figure H.14 – V_{gate} High Side (Ch 1) and V_{diode} (Ch 2)

Figure H.15 – V_{gate} Low Side (Ch 1) and V_{diode} (Ch 2)

Figure H.16 – High Side Drain Voltage (Ch 1) and High Side Source Voltage (Ch 2)

Figure H.17 – High Side Vds Turn On Undershoot

Figure H.18 – High Side Vds Turn Off Overshoot

Appendix I: Universal Synchronous Buck Converter Testing Configuration 2

This section shows the voltage waveforms at various locations on the universal synchronous Buck converter, under configuration 2 constraints. The switching frequency was supplied by a function generator and set at 30kHz. The converter was constructed with a 47 Ω gate resistor with a diode in parallel, and no snubber across the MBR2045CT freewheeling diode.

I.1 No Load Waveforms

At this point the converter was not connected to the power supply representing the PV array. Figure I.1 shows noise on the high side gate when the low side gate goes high, and figure I.2 shows noise on the low side gate turns on. The high side switch turn on and off transition deadtime is measured in figure I.3 and I.4. Figures I.5 and I.6 shows the output's peak and oscillating frequency to be 151mV and 313kHz. The rise and fall time of the MOSFET's gate voltage at no load can be seen in figure I.7 and I.9. The rise time equals 810ns with a fall time of 290ns. By looking at the output voltage on these two figures, noise is present when the gate voltage goes high and low, even with no input or load on the converter.

Figure I.1 – V_{gate} High Side Turn Off Noise (Ch 1) and V_{gate} Low Side (Ch 2)

Figure I.2 – V_{gate} High Side (Ch 1) and V_{gate} Low Side Turn On Noise (Ch 2)

Figure I.3 – V_{gate} High Side (Ch 1) and V_{gate} Low Side (Ch 2) During PWM High

Figure I.4 – V_{gate} High Side (Ch 1) and V_{gate} Low Side (Ch 2) During PWM Low

Figure I.5 – V_{gate} High Side (Ch 1) and V_{out} Peak Oscillation (Ch 2)

Figure I.6 – V_{gate} High Side (Ch 1) and V_{out} Peak Oscillation Frequency (Ch 2)

Figure I.7 – V_{gate} High Side Rise Time(Ch 1) and V_{out} (Ch 2)

Figure I.8 – V_{gate} High Side Fall Time (Ch 1) and V_{out} (Ch 2)

I.2 Full Load Waveforms

The converter was then tested at full load and table I.1 shows the conditions during testing. Figure I.9 shows the maximum and minimum gate voltage measurements of the high side switch. The output voltage was then zoomed in to get a better image of the noise in figure I.10. Figure I.11 and I.12 shows the PWM signal going into the gate driver, compared to the high side and low side gate voltages. The diode's voltage undershoot and overshoot can be seen in figures I.13 and I.14 compared to the high side gate voltages. The diode voltage's undershoot compared to the low side gate voltage can be seen in figures I.15, and the gate voltage noise is measured in I.16. To measure the high side MOSFET's drain to source voltage with the oscilloscope, the drain voltage and source voltage must be measured using two different channels as seen in figure I.17. Using the math function on the oscilloscope, the source voltage can be subtracted from the drain voltage and displayed on the scope. Figures I.18 and I.19 show the high side MOSFET's drain to source voltage undershoot and overshoot.

Table I.1 – Full Load Conditions for Configuration 2

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Duty Cycle	η (%)
34.6	4.76	164.7	12.4	12.53	155.4	37	94.4

Figure I.9 – V_{gate} High Side Measurements (Ch 1) and V_{out} (Ch 2)

Figure I.10 – V_{gate} High Side (Ch 1) and V_{out} Measurements (Ch 2)

Figure I.11 – V_{gate} High Side (Ch 1) and Gate Driver PWM Input (Ch 2)

Figure I.12 – V_{gate} Low Side (Ch 1) and Gate Driver PWM Input (Ch 2)

Figure I.13 – V_{gate} High Side Measurements (Ch 1) and V_{diode} Undershoot (Ch 2)

Figure I.14 – V_{gate} High Side Measurements (Ch 1) and V_{diode} Overshoot (Ch 2)

Figure I.15 – Low Side Gate Voltage Undershoot (Ch 1) and V_{diode} (Ch 2)

Figure I.16 – V_{gate} Low Side Noise (Ch 1) and V_{diode} (Ch 2)

Figure I.17 – High Side Drain Voltage (Ch 1) and High Side Source Voltage (Ch 2)

Figure 1.18 – High Side Vds Turn On Undershoot

Figure I.19 – High Side Vds Turn Off Overshoot

Appendix J: Universal Synchronous Buck Converter Testing Configuration 3

This section shows the voltage waveforms at various locations on the universal synchronous Buck converter, under configuration 3 constraints. The switching frequency was supplied by a function generator and set at 30kHz. The converter was constructed with a 47Ω gate resistor with a diode in parallel, and no snubber across the SBR2060CT freewheeling diode.

J.1 No Load Waveform

At this point the converter was not connected to the power supply representing the PV array., Figure J.1 measures the peak of the output voltage oscillation, while figure J.2 Measure the peak to peak voltage of the output noise.

Figure J.1 – V_{gate} High Side (Ch 1) and V_{out} Oscillation (Ch 2)

Figure J.2 – V_{gate} High Side (Ch 1) and V_{out} Peak Noise (Ch 2)

J.2 Full Load Waveforms

The converter was then tested at full load and table J.1 shows the conditions during testing. Figure J.3 shows the high side gate voltage and output voltage. The output voltage was then zoomed in to get a better image of the noise during high side MOSFET turn on and off, in figure J.4 and J.5. The delta V measurement displays the maximum amplitude of noise seen, which was difficult to capture an image of because of the fast amplitude variations. Figure J.6 and J.7 shows the PWM signal going into the gate driver, compared to the high side and low side gate voltages. The diode's voltage undershoot and overshoot can be seen in figures J.8 and J.9 compared to the high side gate voltages. The noise on the low side gate voltage compared to the diode turning on and off, can be seen in figures J.10 and J.11. To measure the high side MOSFET's drain to source voltage with the oscilloscope, the drain voltage and source voltage must be

measured using two different channels as seen in figure J.12. Using the math function on the oscilloscope, the source voltage can be subtracted from the drain voltage and displayed on the scope. Figures J.13 and J.14 show the high side MOSFET's drain to source voltage undershoot and overshoot.

Table J.1 – Full Load Conditions for Configuration 3

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Duty Cycle	η (%)
35.7	4.46	159.2	11.75	12.53	147.2	35	92.5

Figure J.3 – V_{gate} High Side (Ch 1) and V_{out} (Ch 2)

Figure J.4 – V_{gate} High Side (Ch 1) and V_{out} Zoomed In (Ch 2) During PWM High

Figure J.5 – V_{gate} High Side (Ch 1) and V_{out} (Ch 2) High Side Gate Turn Off Noise

Figure J.6 – V_{gate} High Side (Ch 1) and Gate Driver PWM Input (Ch 2)

Figure J.7 – V_{gate} Low Side (Ch 1) and Gate Driver PWM Input (Ch 2)

Figure J.8 – V_{gate} High Side (Ch 1) and V_{diode} Turn On Undershoot (Ch 2)

Figure J.9 – V_{gate} High Side (Ch 1) and V_{diode} Turn Off Overshoot (Ch 2)

Figure J.12 – High Side Drain Voltage (Ch 1) and High Side Source Voltage (Ch 2)

Figure J.13 – High Side Vds Turn On Undershoot

Figure J.14 – High Side Vds Turn Off Overshoot

Appendix K: Universal Synchronous Buck Converter Testing Configuration 4

This section shows the voltage waveforms at various locations on the universal synchronous Buck converter, under configuration 3 constraints. The switching frequency was supplied by a function generator and set at 30kHz. The converter was constructed with a 47Ω gate resistor with a diode in parallel, and 2.2nF snubber across the SBR2060CT freewheeling diode.

K.1 Full Load Waveforms

The converter was then tested at full load and table K.1 shows the conditions during testing. Figure J.3 measures the high side gate voltage undershoot compared to the output voltage. The output voltage was then zoomed in to get a better image of the noise during high side MOSFET turn on and off, in figure K.2 and K.3. The diode's voltage undershoot and overshoot can be seen in figures K.4 and K.5 compared to the high side gate voltages. Figure K.6 shows the output voltage compared to the diode voltage.

Table K.1 – Full Load Conditions for Configuration 4

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Duty Cycle	η (%)
36.5	4.47	163.2	12.17	12.53	152.5	35	93.4

Figure K.1 – V_{gate} High Side Undershoot (Ch 1) and V_{out} (Ch 2)

Figure K.2 – V_{gate} High Side (Ch 1) and V_{out} Noise (Ch 2) During PWM High

Figure K.3 – V_{gate} High Side (Ch 1) and V_{out} Noise (Ch 2) During PWM Low

Figure K.4 – V_{gate} High Side (Ch 1) and V_{diode} Turn On Undershoot (Ch 2)

Figure K.5 – V_{gate} High Side (Ch 1) and V_{diode} Turn Off Overshoot (Ch 2)

Figure K.6 – V_{out} (Ch 1) and V_{diode} (Ch 2)

Appendix L: Analysis of Senior Project Design

This section is used to fulfill the requirements outlined in appendix C of the Senior Project Handbook.

L.1 Summary of Functional Requirements

The universal Buck and synchronous Buck converters act as DC transformers, and allow for the PV arrays voltage to be stepped down to a lower voltage level. One benefit of these converters over the standard Buck and synchronous Buck topologies, is that they allow for the output current of the converter to be greater than the input current. This is not possible with the standard topologies, because the PV array is a current source. Which means the maximum output current would coincide with a duty cycle of 100%, and the output current would equal the input current. By placing a capacitor at the converter's input, the pulsating current required for the Buck topologies to function properly can be supplied. Allowing for the average output current to be larger than the PV array's current.

The converters that were designed, prototyped, and analyzed, were integrated into a much larger project know as the Cal Poly Sustainable Power for Electrical Resources (SuPER) project. The goal of the SuPER project is to develop a stand alone photovoltaic (PV) unit that can supply the energy needs of a single family home, and decrease the dependency on fossil fuels. A stand alone PV system is one that is not connected to the electrical grid, and uses a battery for energy storage.

L.2 Primary Constraints

Table 1.1 shows the original converter specifications when the project was started. Originally a 500kHz switching frequency was specified for the converters, but

the switching losses at this frequency were quite large. Typically the switching frequency is increased to decrease the inductor and capacitor size, but since size is not an issue the switching frequency was decreased in order to make the converter more efficient.

L.3 Economics

The converter prototype schematics can be seen in figures 3.20 and 4.5. Tables L.1 and L.2 shows the component price breakdown for the universal Buck converter, and the total cost of the prototype came to \$27.86. Tables L.3 and L.4 shows the component price breakdown for the universal synchronous Buck converter, and the total cost of the prototype came to \$37.56. The main difference in cost between the two converters is due to the inductor used in the synchronous version. This price difference can be reduced if a different inductor is selected in the future. Note that not all parts were purchased, but some were obtained as samples or already found in the projects part inventory.

Table L.1 – Universal Buck Converter Component List

Component	Description	Part #	Newark Part #	Mouser Part #	Price (\$)
C1	1000 μ F	50ZLH1000M16X25	38M6924		0.78
C2	1000 μ F	50ZLH1000M16X25	38M6924		0.78
C3	1000 μ F	50ZLH1000M16X25	38M6924		0.78
C4	3.3 μ F	DD-3R3	19F300		0.24
C5	0.1 μ F				
C6	1000 μ F	50ZLH1000M16X25	38M6924		0.78
C7	3.3 μ F	DD-3R3	19F300		0.24
C8	0.1 μ F				
C9	0.47 μ F				
C10	10 μ F	106CKH100M	69K7898		0.12
C11	0.47 μ F				
C12	0.1 μ F				
C13	0.47 μ F				
C14	2.2nF	1C10X7R222K100B	66C6015		0.25
R1	68k Ω				
R2	1.2k Ω				
D1	16V V Zener	1N4745A	18M3510		0.04
D2	Ultra-Fast Diode	1N6622			
D3	Schottky Diode	MBR2045CTPBF	63J7963		1.25
D4	Ultra-Fast Diode	MUR120G		863-MUR120G	0.24
L	56 μ H	1140-560K-RC	63K3399		7.61
M1	MOSFET	IRF3205ZPBF	37J1434		2.06
M2	MOSFET	IRF3205ZPBF	37J1434		2.06
U1	Gate Driver	IRS2117PBF	21M6598		2.20
U2	Buffer	MM74C906N	58K1928		2.37
U3	Linear Regulator	UA7805CKCS	02H5525		0.72

Total 22.52

Table L.2 – Miscellaneous Universal Buck Converter Components

Description	Part #	Newark Part #	Price (\$)	Quantity	Total (\$)
Heatsinks	411320B02500	19M5087	1.19	2	2.38
Insulators	175-6-210P	46F7846	0.68	2	1.36
8 Pin DIP Socket	110-44-308-41-001000	04M0615	0.35	1	0.35
14 Pin DIP Socket	SPC15513	82K7800	1.25	1	1.25

Total 5.34

Table L.3 –Universal Synchronous Buck Converter Components

Component	Description	Part #	Newark Part #	Mouser Part #	Price (\$)
C1	1000 μ F	50ZLH1000M16X25	38M6924		0.78
C2	1000 μ F	50ZLH1000M16X25	38M6924		0.78
C3	1000 μ F	50ZLH1000M16X25	38M6924		0.78
C4	3.3 μ F	DD-3R3	19F300		0.24
C5	0.1 μ F				
C6	1000 μ F	50ZLH1000M16X25	38M6924		0.78
C7	3.3 μ F	DD-3R3	19F300		0.24
C8	0.1 μ F				
C9	0.47 μ F				
C10	10 μ F	106CKH100M	69K7898		0.12
C11	0.47 μ F				
R1	47 Ω				
R2	47 Ω				
D1	Ultra-Fast Diode	MUR120G		863-MUR120G	0.24
D2	Schottky Diode	MBR2045CTPBF	63J7963		1.25
D3	Super Barrier Diode	SBR2060CT			
D4	Ultra-Fast Diode	MUR120-E3/4	76K7747		0.37
D5	Ultra-Fast Diode	MUR120-E3/4	76K7747		0.37
L	500 μ H	IHV15BJ500		70-IHV-15-500	18.58
M1	MOSFET	IRF3205ZPBF	37J1434		2.06
M2	MOSFET	IRF3205ZPBF	37J1434		2.06
U1	Gate Driver	IRS2004PBF	21M6594		1.70
Total					30.35

Table L.4 – Miscellaneous Universal Synchronous Buck Converter Components

Description	Part #	Newark Part #	Price (\$)	Quantity	Total (\$)
Heatsinks	411320B02500	19M5087	1.19	3	3.57
Insulators	175-6-210P	46F7846	0.68	3	2.04
8 Pin DIP Socket	110-44-308-41-001000	04M0615	0.35	1	0.35
14 Pin DIP Socket	SPC15513	82K7800	1.25	1	1.25
Total					7.21

L.4 Manufacturing on a Commercial Basis

Millions of people around the world don't have access to electricity, and some developing countries lack the resource to construct a centralized electrical grid. The SuPER project can be used to supply the energy needs for these people, without increasing the demand for fossil fuels and carbon dioxide emissions. Currently the

system is in the prototyping phase, and a cost competitive version is still years away. But the overall goal is to bring the cost of the system down to \$500, making it an affordable energy solution for millions.

L.5 Environmental

The biggest environmental concerns surrounded around the project involves disposal of the used battery and lead found on the electronic components. There is not much that can be done about the waste generated by the used batteries, but making sure it gets disposed of properly. If the batteries are properly maintained their overall life expectancy can be increased, which will in turn decrease the amount of waste generated. If lead free versions of the electronic components were available, they were used instead of their lead containing counter parts.

L.6 Manufacturability

Since the converters and SuPER system are still in the prototyping phase, manufacturing issues have not been looked at. Once the final version of each are developed, and a decision is made on what components will be kept or added to the system, the manufacturing process can be looked at more closely.

L.7 Sustainability

The only component of the SuPER system that will require attention throughout its proposed 20 year life span is the battery. Currently a Deka absorbed glass mat valve regulated lead acid battery is used in the system, to minimize maintenance issues. The battery should last four to five years if properly used, if a new battery type that can last 20 years is used the mean time between failure can be extended to the life of the entire system. Also, since the energy source is a PV array, no fossil fuels are consumed in the

production of electricity. This will help decrease the demand for fossil fuels, and carbon dioxide emissions. As electronic components evolve over the years, the current system components can be easily upgraded with the latest technology.

L.8 Ethical

There is really no negative ethical implications related to the project. The systems overall goal is to supply affordable electricity, generated by a renewable source, to millions of people around the world.

L.9 Health and Safety

The only real health concern was addressed in L.5, and electrical safety is the only real hazard of the system. As long as the system is properly built, and made weather proof, there should really be no concerns about electrical safety. Since the system runs on low voltage, less than 50V, the likelihood of someone being injured is minimal.

L.10 Social and Political

If the SuPER project can reach its goal of an overall system cost of \$500, it will become an affordable means of electricity production. The SuPER system can be used to supply a water pump, refrigerator, lighting, and any other device that runs on DC voltage. By supplying electricity to those who currently don't have access to it, the quality of life for millions of people can be greatly improve.

L.11 Development

Although several papers were found containing topologies similar to the universal Buck and synchronous Buck converter, none were found that actually explained how to design the converters. During the development of these two converters, the equations for determining the input capacitor's size and RMS current rating were derived. This

allowed for easier component selection since they no longer needed to be selected by trial and error, but the actual values required to meet the specifications could be calculated.