Warren J. Baker Endowment for Excellence in Project-Based Learning
Robert D. Koob Endowment for Student Success

FINAL REPORT

I. Project Title

High Density Inverter for the Little Box Google Challenge

II. Student(s), Department(s), and Major(s)

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III. Faculty Advisor and Department

Taufik, Professor, Electrical Engineering Department

IV. Cooperating Industry, Agency, Non-Profit, or University Organization(s)

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2) Enerpro Inc., 99 Aero Camino, Goleta, CA 93117, USA
3) Maxim Integrated, 160 Rio Robles, San Jose, CA 95134 USA

V. Executive Summary

This project entailed the construction of a High Density Inverter for the competition held by Google called the Little Box Challenge. An inverter is an electrical equipment widely used for roof-top solar panels which enables us to convert solar energy to useful electricity. A Cal Poly team consisting of three electrical engineering students and one electrical engineering professor officially entered the competition in September 2014. In addition to the funding from the Baker-Koob grant, the team also received technical and funding supports from three companies. The high density inverter was built based on the team's new proposed approach consisting of two hardware stages called the Boost stage and the switching inverter+filter stage. The design was also to utilize a new component technology, fully supported by one of the sponsoring companies, which will be crucial in achieving the high efficiency. The project consisted of three phases: Design & Calculation (Phase 1), Computer Simulation and Analysis (Phase 2), and Hardware Development and Testing (Phase 3). Phase 1 resulted in an initial estimation on the overall efficiency of the design. Phase 2 incorporated data obtained from Phase 1 to construct a computer model to simulate the inverter against technical specifications set by Google. Results from Phase 2 demonstrated successful performance of the high density inverter. Finally in Phase 3, the Boost stage was completed and tested successfully to its full functionality. The inverter+filter stage was also built and tested with

commercially available critical components within the inverter called semiconductor switches. However, its full functionality was not realized due to the technical issues in utilizing the new (was not yet commercialized) switches as originally intended for use in the high density inverter. This turned out to be the major obstacle in the project as the team spent significant amount of time getting familiar with the new component and troubleshooting technical issues in using the component. The team at the end was able to achieve most of the goals but did not meet the Google's deadline and was not able to submit the final hardware for the competition due to the aforementioned technical issues. Despite this, the project is successful in demonstrating the proof-of-concept of the team's proposed new method for a high-density inverter. The project is currently still on-going with plans to refine the proposed new design which will further be developed as a master's thesis by one of the student members of the team. A portion of the new method will be submitted for a US patent through Cal Poly. Following these, results obtained from this project will be disseminated as conference papers in technical conferences.

VI. Major Accomplishments

The goal of this project is to design and construct a high-density inverter for the Google's little box challenge using a new method. The level 0 block diagram of the proposed method is shown in Figure 1.

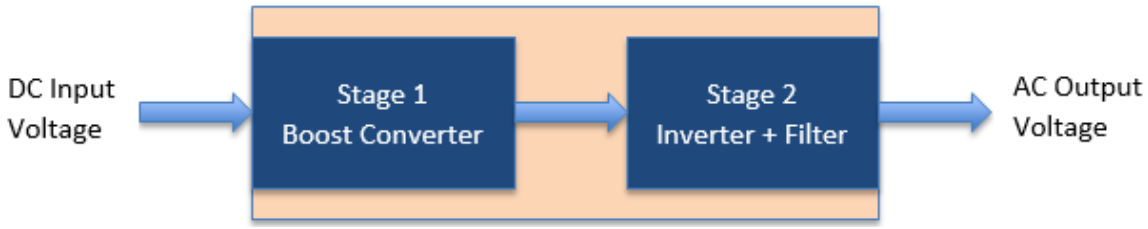

Figure 1. High Density Inverter – Level 0 Block Diagram

The construction and testing of the proposed inverter had to be completed by the middle of July 2015 per Google's deadline for the competition. The following summarizes team's accomplishments.

1. Stage 1 – Boost Converter

Based on the specifications given by Google, an inverter topology was designed and simulated. The topology was divided into three different segments - Input ripple suppressor, Inverter and the controls. The role of input ripple suppressor is to provide constant and stable DC supply to the inverter in order to improve the efficiency of the overall system. The topology used for the input ripple suppressor is a unique and efficient Boost converter which could meet the desired requirements. Initially, simulation and analysis was carried out on the input ripple suppressor. Based on the results obtained, optimization techniques were applied in order to achieve a compact and efficient boost converter. Printed circuit board (PCB) layouts were designed for the asynchronous Boost converter and tested with regular silicon MOSFETS to test the topology. This topology had integrated a hardware controller to implement a closed loop for the boost converter and maintain a constant supply voltage to the inverter. The same topology was later tested with the industry standard, latest technology edge FET's. The topology proved to be very efficient and optimized when tested with silicon MOSFETS and industry cutting edge FET's. In order to improvise the control scheme of the asynchronous Boost converter, PWM algorithm was implemented on an

Arduino microcontroller. For better efficiency, PID control logic was used for the Non-Synchronous Boost and the output voltage was regulated to the desired value. Improvised the existing topology and Implemented synchronous boost using standard FET. It was able to regulate 480-520V output for an input range of 50-200V using a microcontroller. The input ripple suppressor was successfully implemented with all the requirements met. PWM signals for the H-Bridge topology of the Inverter were implemented along with the dead times and also at different frequencies using SPWM Algorithm. The slower clock of the microcontroller and also the memory limitations, did not meet the requirements so switched to a powerful microcontroller. Implemented the PWM signals for the H- Bridge (4 industry standard Switches) with different combinations of the switches for better efficiency.

Figures 2 through 6 show the hardware prototype for the stage 1 boost circuit along with the laboratory setup for measurements and its corresponding critical waveforms. The figures further demonstrate or successful accomplishment in the construction of the stage 1 in our high-density inverter.

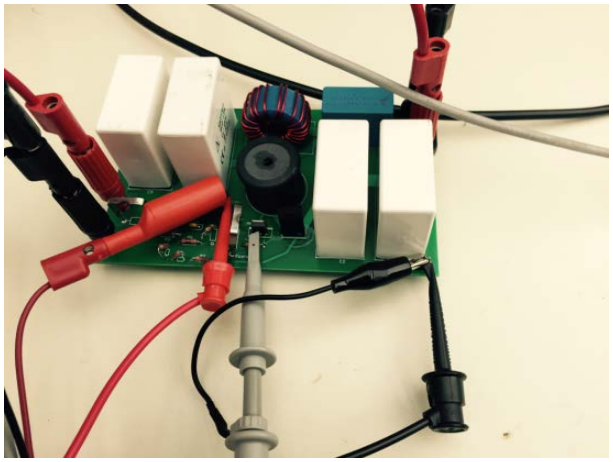

Figure 2. Input ripple suppressor boost circuit

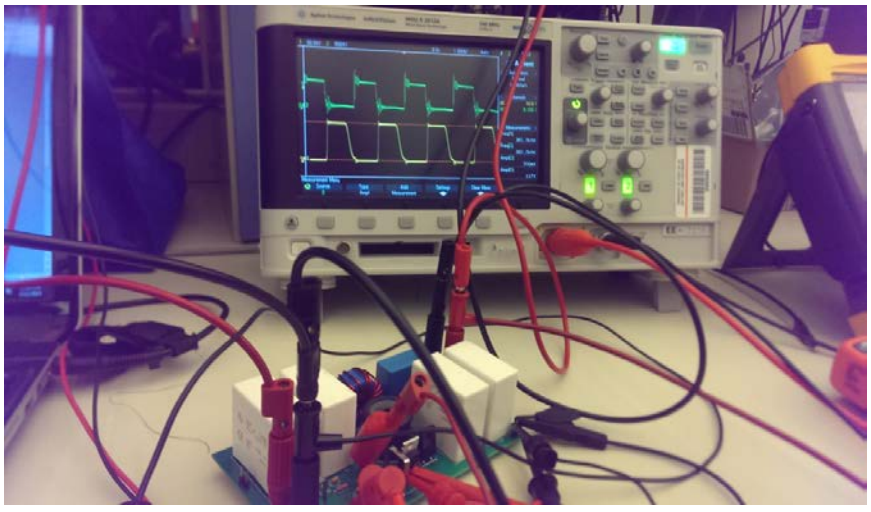

Figure 3. VGS (Green) and VDS (Yellow) waveforms with Vin = 40V and Vout = 500V.

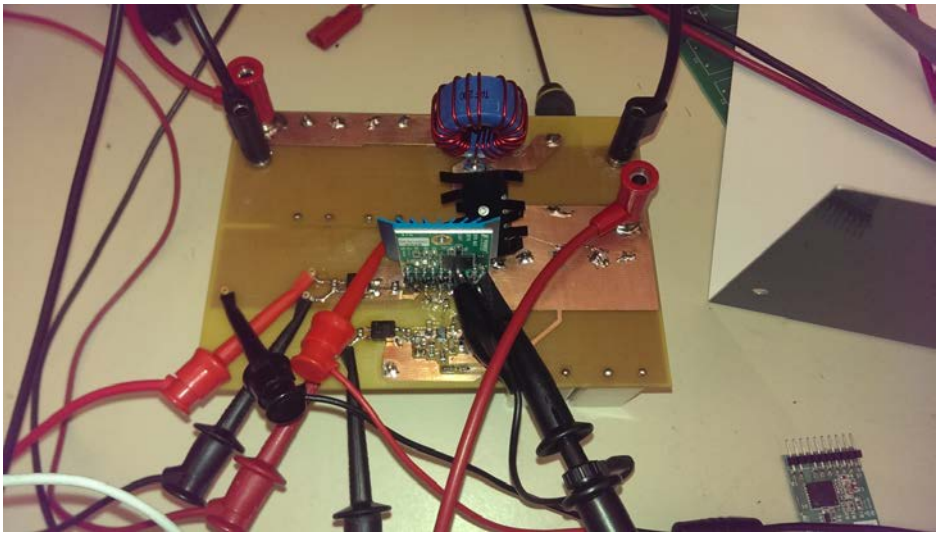

Figure 4. Non synchronous Boost Test Setup

Figure 5. CH1 (yellow) Switch IN signal, CH2 (green) Drain to Source Voltage. Vin=100V, Vout=480V.

Figure 6. The Yellow waveform represents the Gate to Source Signal from the micro-controller
The Green waveform represents the Drain to Source Signal of the Switch

2. Stage 2 – Inverter + Filter

The design and analysis of the inverter power stage include: an input capacitor stage, 8 switch full bridge topology, and an output filtering stage. In conjunction, these three stages take a 500V DC voltage at the input and produce a 120Vrms, 60Hz sinusoid at the output.

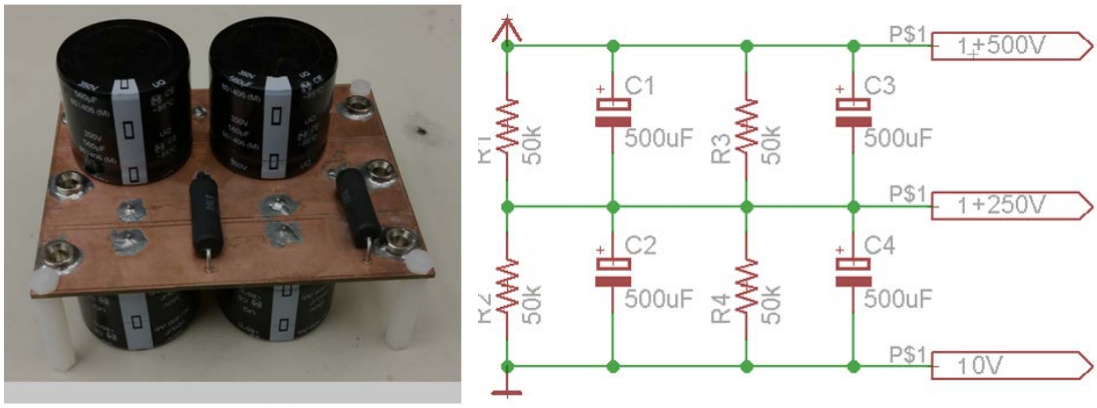

Figure 7. Input Capacitor Stage

An input capacitor stage was successfully designed to support the DC to AC conversion process by means of bulk energy storage. The final design and schematic are shown in Figure 7. The design uses balance resistors to maintain equal charge between two series capacitors. During this project improvements were identified to further increase the efficiency of this circuit by removing these balancing resistors, and incorporating a charge balancing scheme via a micro-controller. This improvement is noted for future developments.

Figure 8. Output Filter

The output filter stage is necessary in order to filter the unwanted frequencies caused by the inverter power stage. A balanced topology makes this power filter unique as shown in Figure 8. By utilizing this balanced topology parasitic in the energy storing components are reduced by a half. In addition, the balanced topology reduces the inductance of each inductor by one half, thus achieving an overall reduction in size.

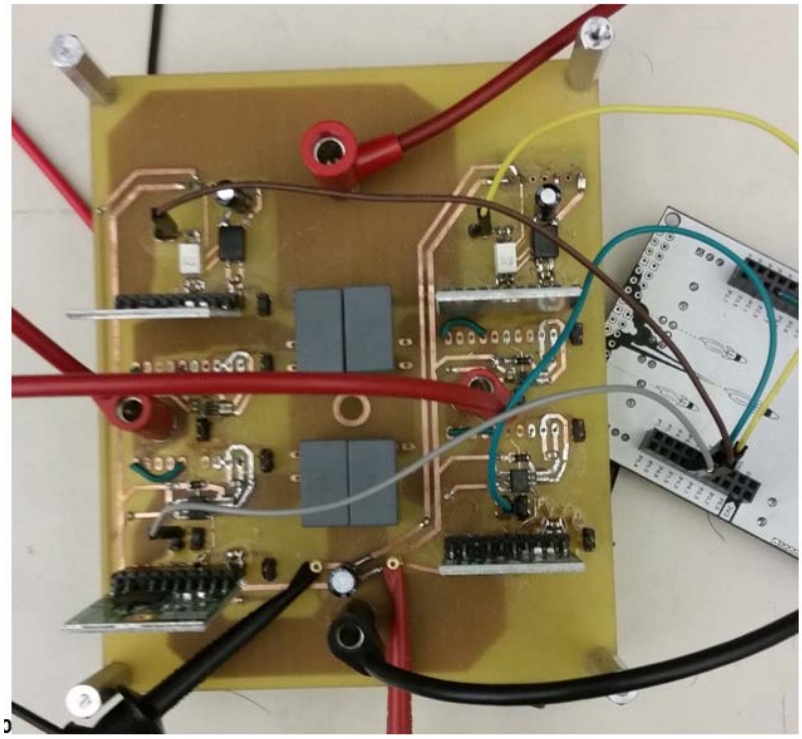

Figure 9. Final Revision of the Power Inverter Stage

The final hardware design for the power inverter stage is shown in Figure 9. The power stage uses 4 switches in an H-bridge topology to effectively produce a bipolar DC voltages at the output. The three possible states for the output are +Vdc, -Vdc, and 0V. Figure 10 demonstrates the output of the inverter power stage prior to the filtering stage. The switching signals are produced using an MSP432 micro-controller.

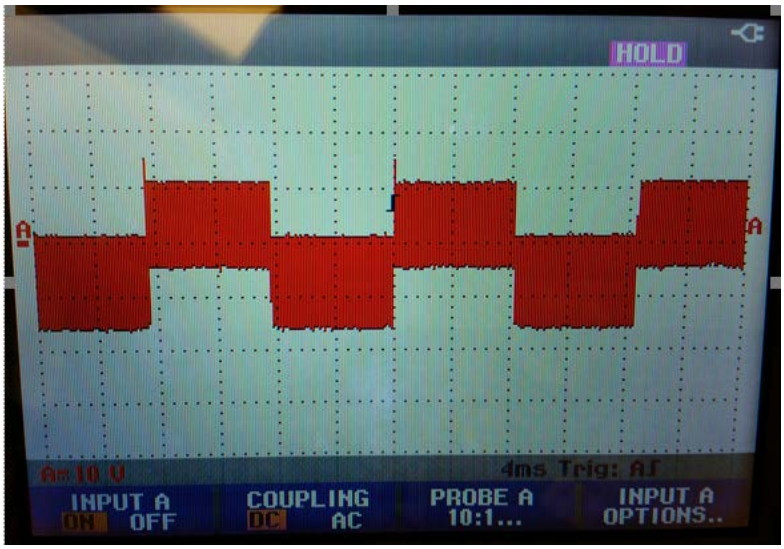

Figure 10. Inverter Stage Output

In summary, the three main stages of the power inverter were prototyped and tested for their functionality. Figure 11 demonstrates the output of the inverter, post filtering. The output is now a 60Hz sinusoid after filtering out the higher frequency components via the power stage filter. As seen in Figures 10 and 11 the functionality of the inverter is in agreement with the simulated

results. Overall this project resulted in a successful prototype build of a potentially highly efficient power inverter.

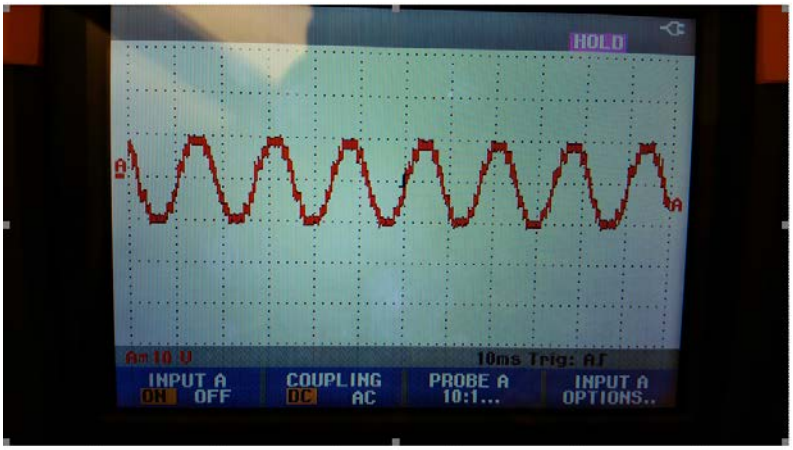

Figure 11. Final Inverter Output

VII. Expenditure of Funds

At the time we are writing this report, we haven't yet used the funding provided by the Baker-Koob grant. As explained in the section below, we encountered technical issues that pushed back our schedule despite our initial success in demonstrating the basic function of the inverter as previously discussed. Per information provided by our advisor, Professor Taufik, we are given the approval to use the fund by January 2016. In general, we plan to use to the majority of the fund we received to purchase parts and components that we will be needing to construct our final version of the proposed inverter.

VIII. Impacts to Student's Learning

One thing that we learned from this project is how we can work as a team. Given the different set of background each one of us has, we learned how to communicate to each other to achieve a common goal. The difficulty of conveying and sharing our ideas at the beginning stage was quite a challenging process and was also observed by the faculty advisor who provided us with some advises. Several meetings later, we were able to overcome this issue and we demonstrated our improved ability to communicate effectively to every member of the team. The same learning experience we also encountered when we presented our data and results to the company sponsor.

Since the proposed high density inverter is new or has not been done before, we were really challenged to apply our technical knowledge to perform analysis and design of the inverter. During system modeling phase of the design, we had to learn how to use industry standard software which is definitely beneficial for us especially in making use more competitive when seeking for job after our graduation.

Another set of skill that we learned from the project relates to management skills. As a group and at the initial stage of the design, we had to come up with and agree on project schedules, deadlines, and milestones. Once this was accomplished, we had to commit ourselves to the schedule to ensure continuing progress toward the completion of the proposed inverter. However, during the course of the project we encountered several issues which forced us to learn the need

for allowing our schedules to anticipate these and later to revisit and modify our schedule.

Last but not least, we feel that our hands-on skill had become better because of our involvement in this project. In particular, our troubleshooting and debugging skills had improved after hours and hours of attempting to fix technical problems on our circuit board. From this project we also learned to use new lab equipment which is again useful especially in making ourselves more marketable when it comes to finding job after our graduation. Board layout skill which is not formally thought in any of our classes was a technical skill that we often had to perform for this project. Overall, we really believe that our hands-on skill has improved to another level due to this project.