THE DESIGN AND FABRICATION OF AN ELECTROSTATICALLY ACTUATED DIAPHRAGM WITH A SILICON-ON-INSULATOR WAFER

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THE DESIGN AND FABRICATION OF AN ELECTROSTATICALLY ACTUATED DIAPHRAGM WITH A SILICON-ON-INSULATOR WAFER

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ABSTRACT

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Electrostatically actuated silicon membranes were designed, modeled, fabricated, and characterized. The intended application was for use in a microspeaker. Fabrication issues necessitated the use of thick diaphragms with a large gap between the electrodes. The devices did not function as speakers but did show actuation with a high DC voltage. Device dimensions were chosen by examining membrane mechanics, testing the processing steps required for device fabrication, and modeling with COMSOL. Several adhesives were researched to fabricate the device sidewalls, including BCB, PMMA, and TRA-Bond F112. A method for patterning PMMA through photolithography was found using a scanning electron microscope. Masks were designed in AutoCAD to create the electrostatically actuated devices and a microfabrication process was developed to produce diaphragms that could be characterized. Twenty micron thick diaphragms were fabricated by etching an SOI wafer in 25% TMAH and the etch depth was measured with a profilometer. Glass slides were coated with gold and patterned with positive photoresist to create counter-electrodes. The diaphragms were bonded to the glass slides using a forty micron thick layer of patterned SU-8 as sidewalls. Bonding was successful in the initial fabrication testing but not successful for the final devices. The final fabrication run resulted in eight devices that were partially bonded. Three devices were chosen to test the membrane actuation and the data analyzed for statistical significance. A DC voltage was applied to the electrodes with a MEMS driver and the change in force measured with a micro-force displacement system. Data analysis showed device actuation at high voltages (300V) for the medium and large devices.
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Keywords

**Electrostatic Force:** a force caused by the interaction between two electrically charged surfaces. The electrostatic force is attractive between oppositely charged surfaces and attractive between positively charged surfaces.

**Silicon-On-Insulator Wafer:** A silicon wafer with three layers: a thin surface layer of silicon (the device layer), a thin insulating layer (the embedded oxide) and a thick support layer of silicon (the handle layer).

**MEMS Actuator:** A device or component on the micro-scale that generates motion through electrostatic, magnetic, piezoelectric, thermal, optical, or chemical means.

**Tetramethylammonium Hydroxide:** (TMAH) A chemical used in microfabrication as a silicon etchant. TMAH is nontoxic, inexpensive, and does not decompose below 130°C. Oxide or nitride layers can be used to mask silicon during etching.

**Potassium Hydroxide:** (KOH) The most popular Si anisotropic etchant. It exhibits poor selectivity between silicon and silicon dioxide, cannot be used for IC fabrication processes, and is toxic.

**SU-8 Resist:** A thick, epoxy-based negative photoresist capable of high resolution and aspect ratios when patterned by lithography. SU-8 becomes insoluble in developer after exposure.

**Poly(methylmethacrylate):** (PMMA) is a positive photoresist that becomes soluble through chain scission under deep UV, x-ray, or E-beam exposure.

**COMSOL Multiphysics:** A modeling program with a finite element analysis solver capable of coupling multiple physics packages.
1. Introduction

1.1 MEMS Devices and Electrostatic Actuation

MEMS, an acronym for “Micro Electro Mechanical Systems,” is a broad category of devices engineered to perform specific functions through electromechanical or electrochemical means. Most MEMS devices fall into three broad categories: microactuators, microsensors, or microfluidics. The term “micro” implies that the device components range from one micron to one millimeter in size and device sizes have been continuously decreasing with the evolution of microfabrication techniques.[1] Device miniaturization has many benefits when considering engineering design:

1. It enables the design of increasingly complex systems without increasing device size.
2. Smaller systems generally move faster than larger systems due to decreased mass and mechanical inertia.
3. Thermal distortion is generally reduced.
4. Smaller masses have much higher resonant frequencies, reducing problems in device vibration. For this reason, miniature condenser microphones have virtually no resonant diaphragm vibration.
5. Device actuation and dimensional stability are highly accurate.
6. Devices can be fabricated with reduced materials and precise dimensions.[1]

A wide range of MEMS devices and components have been designed and produced, including microgears, micromotors, microturbines, and micro-optical components. Devices are finding application in every-day products such as laptops, cell phones, automobiles, biomedical devices, and refrigeration systems.[1]

Electrostatic force is a common driving method for actuators and sensors. It is defined as the attractive or repulsive electrical force between two charged components induced by an electrical field.[1] Electrostatic actuation has a few key advantages: power is consumed only during actuation, fabrication technology is simple compared to electromagnetic actuation, and device
size is relatively small.[2] Electrostatic actuation provides a fast response due to the good charging and discharging time constants of conductors, enabling high frequency applications.[3] Compatibility with basic MEMS fabrication techniques enables batch processing and lower production costs.

Recently, sensing MEMS microphones have been designed for use in advanced hearing aids. A typical MEMS microphone is 1 mm x 1 mm x 0.5 mm and is made from polymers or single-crystalline silicon. Figure 1 shows the basic structure of a silicon based condenser microphone. The diaphragm and back plate are made of conductive materials so that they act as the electrodes of a capacitor. Holes in the back plate and bottom cavity allow for pressure equalization. Incoming pressure waves from sound induce deflection in the diaphragm, which changes the gap between the two electrodes. The capacitance between the plates changes with the changing gap distance, and can be seen as an electrical signal output.[1] In theory, this design can be inversely applied to create a speaker.

![Figure 1.1: Core Components of an electrostatically sensing MEMS Microphone](image)

1.2 Electrostatically Actuated Microspeaker

An electrostatically actuated microspeaker functions in the opposite way as the electrostatically sensing microphone. The microspeaker is essentially a capacitor with an upper conductive diaphragm and lower conductive plate (Figure 1.2). When a voltage is applied to the electrode
plates, an attractive electrostatic force develops. When this force overcomes the mechanical
restoring force of the diaphragm, the diaphragm will deflect (Figure 1.2). The volume change of
the air inside the cavity creates a pressure wave that can be transferred to the ear. An oscillating
differential voltage applied to the electrodes can be controlled to produce varying sound waves.
The electrostatic force is dependent upon the surface area of the electrodes, the distance
between the electrodes, and the applied voltage.[4] Due to the fabrication capabilities of our lab,
my design is limited to larger distances between the parallel plates. To compensate, the device
requires a relatively large surface area and large differential voltage. The maximum voltage was
determined to be 300V because this could be achieved by a MEMS driver available in our lab.

Figure 1.2: Electrostatically Actuated Diaphragm Model. An applied voltage creates an
electrostatic force that induces diaphragm deflection. The deflection creates a pressure
differential inside the cavity. The balance of forces is shown; the mechanical restoring force of the
diaphragm balances the electrostatic force induced by the applied voltage.

1.2.1 Project Scope

The purpose of this project is to improve upon the device design and microfabrication processes
in our lab in order to advance this project. The goal is to create an improved electrostatically
actuated parallel plate device that can be characterized in our lab. The induced pressure caused
by diaphragm deflection and electrostatic force is simply related by:[5]
\[ F_{elec} = Pa^2 \]  
(1.1)

\( P \) is the induced pressure, \( P_{\text{ref}} \) is the reference pressure (20 \( \mu \)Pa) and \( a \) is the side length of a square diaphragm. For the continuation of this project, the change in pressure and sound produced can be related by the equation:[5]

\[ dB = 20 \log_{10} \frac{P}{P_{\text{ref}}} \]  
(1.2)

Average noise levels range from 50 dB to 80 dB.[1] To achieve these levels, 158 nN to 500 nN of electrostatic force is required for a diaphragm with a 5 mm side-length.

1.3 Broader Impact

The World Health Organization estimated in 2001 that 250 million people worldwide have a disabling hearing impairment. Currently, one-tenth of the hearing aids needed globally are in existence; 75% of these are distributed to North America and Europe, 13% to Japan, Australia and New Zealand, and 12% to the rest of the world.[6] Hearing aids are typically too expensive for individuals in less developed countries (LDCs) and require unavailable education and power sources. There is a pressing need for hearing aids that are affordable for individuals in LCDs, with consideration to their resources.

1.3.1 Prevalence of Hearing Loss in Less Developed Countries

Individuals in LDCs are twice as likely to develop hearing impairments as individuals in developed countries due to the living conditions that contribute to hearing loss. Problems during pregnancy and childbirth including birthing conditions, infectious diseases during pregnancy, misuse of ototoxic drugs, and jaundice contribute to hearing impairment in newborn babies. Hearing loss can occur during childhood due to infectious diseases such as meningitis, measles, mumps, and chronic ear infections. Other common risks include wax blockage, head injury, and excessive noise. Most of these risk factors are elevated in LDCs. Low-quality, inaccessible health care contributes to childbirth complications, infectious diseases, and poor health education.
Preventative measures such as immunizations, monitored drug dosages, disease diagnosis, and treatment are less available. Operating machinery without protective gear and noise control can expose individuals to dangerous levels of noise. Exposure to dangerous noise levels from gunfire or explosions are often experienced more in countries with weak government structures.[7]

Along with the increased risk, hearing impairment is stigmatized in LDCs due to poor health care and education. The development of a child’s language and cognitive skills can be delayed due to the inability to hear correctly. Hearing impairment can hinder adults from adequately performing their jobs. Without health care or special education programs, these individuals are often isolated and stigmatized.[7]

1.4 Improving Hearing Aids

A hearing aid has four basic parts: a microphone, amplifier, speaker, and battery (Figure 1.3). The microphone receives sound waves and converts them into electrical signals. The amplifier receives the electrical signals and increases their power. The speaker takes the amplified signal and converts it back into sound waves directed into the ear.[8] The battery powers the microphone, amplifier, and speaker. A microspeaker alone accounts for 50-95% of the power consumption in a hearing aid.[9] Decreasing the power consumption level of the speaker will prolong operation life and decrease the device’s dependence on a power source.
Improvements on Previous Work at Cal Poly

Electrostatically actuated diaphragms have been researched, designed, and fabricated by Brian Stahl at Cal Poly. He attempted to fabricate diaphragms by doping one side of a silicon wafer with boron to create an etch-stop for silicon etching. This led to significant warping in the diaphragms due to internal stresses built during the thermal cycling.[11] To reduce warping, I fabricated diaphragms with a silicon-on-insulator (SOI) wafer. SOI wafers have an embedded oxide that provides an etch stop without doping. His design also suffered poor adhesion of SU-8 in the fabrication of device side walls. I researched other materials to replace SU-8, but eventually found a processing procedure that resulted in complete bonding. The final diaphragm fabrication used the same processing procedure that was previously found successful, but was unsuccessful in creating a completely bonded surface.

Initially I fabricated diaphragms with a mask made by Brian Stahl to produce diaphragms of five different sizes. This showed the effects of warping on diaphragm size for my processing conditions. Once an adhesive was chosen (the side wall thickness was known) the devices were modeled and diaphragms were designed. The final devices were characterized by applying a voltage with a MEMS driver and measuring the change in force with a micro-force displacement system. The deflection of the diaphragm was calculated from the change in force.
Section 2: Design

2.1 Summary

This section outlines the process used to design the device. Initially, diaphragm mechanics was studied to predict the membrane displacement based on the pressure induced by electrostatic actuation. These equations were then modified to consider the increase in electrostatic force that occurs as the distance between the plates decreases as the membrane deflects. Finally, necessary design constraints were added to ensure proper functioning of the device.

2.2 Diaphragm Mechanics

The mechanics of square membranes was examined to estimate the deflection of the diaphragm and ensure that the stresses produced by actuation would not lead to device failure. An ideal membrane can be considered a square plate of uniform thickness clamped on all four edges. Mathematically comparing square, rectangular, and circular plate geometries with the same surface area, thickness, and applied pressure shows that square diaphragms have the highest pressure induced stress.[12] This is favorable for an actuator because the high stresses result in high precision.[12] A square shape also allows for design simplicity and ease of fabrication. The plate is assumed to be in pure bending due to the high aspect ratio of the diaphragm (the plate thickness $h$ is small compared to the side length $a$). The load (electrostatic force) applied to the plate is perpendicular to the plate surface.

Linear elastic theory of thin, isotropic plates with small deflections was investigated to estimate diaphragm mechanics.[13] The plate is considered thin because the side-length $a>5h$ and the deflection $w>h/2$.[14] This implies that membrane stresses induced by deflection are small compared to stresses induced in bending. The following assumptions, known as the Love-Kirchoff hypotheses, apply in this analysis:

1. The device material is operated in the linear elastic regime where Hooke’s law applies.
2. The device material is homogeneous and isotropic.
3. The plate thickness is small compared to the side length so that the transverse normal stresses can be ignored.

4. Points perpendicular to the plate surface remain perpendicular after deflection.

5. The plate deflection is small compared to the plate thickness.

6. Existing membrane stresses are neglected.

7. The applied load is perpendicular to the face of the plate.

2.2.1 Derivation of Stress Components

The assumptions made in the Kirchoff-Love theory allow a two-dimensional mid-plane to represent the three-dimensional plate. No angular distortion occurs, so the strains \( \varepsilon_{zz} = \gamma_{xz} = \varepsilon_{yz} = 0 \). Applying assumption 4, the displacements \( u(x,y,z) \) and \( v(x,y,z) \) of a point (see Figure 2.1) on the center plane of the actuated membrane can be defined as

\[
\begin{align*}
u(x,y,z) &= -z \frac{\partial w}{\partial x}, \\
v(x,y,z) &= -z \frac{\partial w}{\partial y}.
\end{align*}
\]

The corresponding strains are found using the definition of normal strain:

\[
\begin{align*}
\varepsilon_{xx} &= \text{change in displacement} \div \text{original length} = \frac{\partial u_x}{\partial x} = -z \frac{\partial^2 w}{\partial x^2}, \\
\varepsilon_{yy} &= -z \frac{\partial^2 w}{\partial y^2}.
\end{align*}
\]

Engineering shear strain \( \gamma_{xy} \) is defined as the change in angles \( \alpha \) and \( \beta \) between lines AC and AB (Figure 2.1). For small displacements, \( \tan \alpha \approx \alpha \) and \( \tan \beta \approx \beta \), therefore \( \gamma_{xy} \) can be approximated by

\[
\gamma_{xy} = \alpha + \beta = \frac{\partial u_x}{\partial x} + \frac{\partial u_y}{\partial y} = -2z \frac{\partial^2 w}{\partial x \partial y}.
\]
Hooke’s law defines the stress components as:

\[ \varepsilon_{xx} = \frac{1}{E} (\sigma_{xx} - \nu \sigma_{yy}), \]  
\[ \varepsilon_{yy} = \frac{1}{E} (\sigma_{yy} - \nu \sigma_{xx}), \]  
\[ \gamma_{xy} = \frac{2(1+\nu)}{E} \sigma_{xy}. \]

Combining our previously found stress Equations (2.3), and (2.5), with Hooke’s stress components, Equations (2.6), (2.7), and (2.8), gives the following relationships

\[ \sigma_{xx} = \frac{Ez}{1-\nu^2} \left( \frac{\partial^2 w}{\partial x^2} + \nu \frac{\partial^2 w}{\partial y^2} \right), \]  
\[ \sigma_{yy} = \frac{Ez}{1-\nu^2} \left( \frac{\partial^2 w}{\partial y^2} + \nu \frac{\partial^2 w}{\partial x^2} \right), \]  
\[ \sigma_{xy} = \frac{Ez}{1-\nu} \frac{\partial^2 w}{\partial x \partial y}. \]

From these equations, we can calculate the relevant stresses from a given deflection.
2.2.2 Resulting Forces and Moments

It is useful to next define the resulting bending moments \( m_x \) and \( m_y \), twisting moments \( m_{xy} \) and \( m_{yx} \), and transverse forces \( Q_x \) and \( Q_y \) (Figure 2.2).

![Figure 2.2: Bending moments, twisting moments, and transverse forces of the membrane. [15]](image)

The bending moments can be found by integrating the in-plane stresses over the membrane thickness:

\[
m_{xx} = \int_{-h/2}^{h/2} \sigma_x z dz, \quad \text{(2.12)}
\]

\[
m_{yy} = \int_{-h/2}^{h/2} \sigma_y z dz, \quad \text{(2.13)}
\]

\[
m_{xy} = m_{yx} = \int_{-h/2}^{h/2} \sigma_{xy} z dz. \quad \text{(2.14)}
\]

Combining Equation (2.12) with Equation (2.9), gives

\[
m_{xx} = -\frac{EI}{1 - v^2} \left( \frac{\partial^2 w}{\partial x^2} + v \frac{\partial^2 w}{\partial y^2} \right) \quad \text{(2.15)}
\]

Where \( I \) is the moment of inertia of the membrane. For simplicity, the flexural rigidity

\[
D = \frac{EI}{1 - v^2} = \frac{Eh^3}{12(1 - v^2)} \quad \text{(2.16)}
\]

can be substituted into the equation so that
Similarly,

\[ m_{xx} = -D \left( \frac{\partial^2 w}{\partial x^2} + v \frac{\partial^2 w}{\partial y^2} \right). \]  

(2.17)

Similarly,

\[ m_{yy} = -D \frac{\partial^2 w}{\partial y^2} + v \frac{\partial^2 w}{\partial x^2}, \]  

(2.18)

\[ m_{xy} = m_{yx} = -1 - v D \frac{\partial^2 w}{\partial y \partial x}. \]  

(2.19)

Next it is necessary to establish a rotational equilibrium equation about the y-axis of an infinitesimal plate segment \( hdx dy \):

\[ Q_x = \frac{\partial m_{xx}}{\partial x} + \frac{\partial m_{xy}}{\partial y}. \]  

(2.20)

### 2.2.3 Derivation of Deflection and Maximum Stress

Substituting Equations (2.17) and (2.19) into this equilibrium equation and simplifying gives a simple relationship between \( Q_y \) and the deflection \( w \)

\[ Q_x = -D \frac{\partial}{\partial x} \frac{\partial^2 w}{\partial x^2} + \frac{\partial^2 w}{\partial y^2} = -D \frac{\partial^2 w}{\partial x}. \]  

(2.21)

Similarly, considering rotational equilibrium about the x-axis and substituting with Equations (2.18) and (2.19) gives

\[ Q_y = \frac{\partial m_{yy}}{\partial y} + \frac{\partial m_{xy}}{\partial x} = -D \frac{\partial^2 w}{\partial x}. \]  

(2.22)

Applying vertical equilibrium to the system requires that the applied pressure is equal and opposite to the changes in forces, or

\[ -p = \frac{\partial Q_x}{\partial x} + \frac{\partial Q_y}{\partial y}. \]  

(2.23)
Finally, substituting in Equations (2.21) and (2.22) gives us the system’s governing differential equation

\[
\frac{p}{\rho} = w\left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2}\right)\left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2}\right).
\] (2.24)

This equation allows us to compute the deflection of the plate at any point. With a known deflection, we can calculate the stresses and moments from previous equations. This is a fourth order partial differential equation that can be solved by applying appropriate boundary conditions. For a square diaphragm with clamped edges and uniform loading, the maximum deflection occurs at the center of the diaphragm and can be found by the equation \([15]\)

\[
w_{\text{max}} = 0.01303 \frac{pa^4}{\rho h^3}.
\] (2.25)

The maximum stress occurs at the middle of each edge. Applying the same boundary conditions to Equation (2.24) with Equation (2.9) and (2.10) gives the maximum stress:\([16]\)

\[
s_{\text{max}} = \frac{0.308pa^2}{h^2}
\] (2.26)

2.3 Electrostatic Force

The diaphragm deflection is induced by the electrostatic force that develops between the two plates. The electrostatic force forms due to the separation of opposite charges concentrated on opposing plates. If the diaphragm and counterelectrode are treated as parallel plates fixed by two fixed-guided beams, the static capacitance \(C_o\) is given by \([17]\)

\[
C_o = \frac{\varepsilon \varepsilon_o A}{d}
\] (2.27)

where \(\varepsilon\) is the permittivity of the dielectric medium between the two plates, \(\varepsilon_o\) is the permittivity of free space (\(\varepsilon_o = 8.854 \times 10^{-12} \text{ F/m}\)), \(A\) is the overlapping area of the plates, and \(d\) is the distance between the two plates. When a voltage \(V\) is applied to the plates, the attractive electrostatic force \(F_{\text{elec}}\) is estimated by
Combining Equations (2.27) and (2.28) gives an equation for the electrostatic force between parallel plates in terms of membrane material properties and device dimensions:[18]

\[ F_{elec} = \frac{C_d V^2}{2d} \]  \hspace{1cm} (2.28)  

where \( x_0 \) is the gap distance at rest \((V=0)\) and \( x \) is distance of gap deflection distance after actuation.

\[ F = \frac{\varepsilon \varepsilon_0 A V^2}{2(x_0 - x)^2} \]  \hspace{1cm} (2.29)  

2.3.1 Parallel Plate Actuation with Uniform Force

The applied equations assume that the electrostatic force is uniformly applied across the plates and that the plates do not deform. In reality, the diaphragm deforms toward the counterelectrode and the electrostatic force increases toward the center of the diaphragm where the gap distance between the plates is the smallest.

The maximum deflection \( w_{max} \) at the center of the membrane was found (Equation 2.25). Replacing the pressure with \( F/a^2 \) gives the maximum deflection in terms of a constant electrostatic force:

\[ w_{max} = 0.01303 \frac{F_{elec} a^2}{E h^3} \]  \hspace{1cm} (2.30)  

Combining Equation (2.30) with Equation (2.29) gives the maximum deflection in terms of the membrane's material properties, device dimensions, and applied voltage:

\[ w_{max} = 0.01303 \frac{\varepsilon \varepsilon_0 A^4 V^2}{2E(x_0 - x)^2 h^3} \]  \hspace{1cm} (2.31)
2.3.2 Nonlinear Force Response

Equation (2.31) serves as a rough approximation for diaphragm deflection and does not account for the nonlinear electrostatic force response. As the diaphragm deflects closer to the counterelectrode, the electrostatic force increases with decreasing gap distances. As previously stated, the electrostatic force is balanced by the mechanical restoring force of the diaphragm. If the membrane is treated as a simple spring, Hooke’s law gives the mechanical restoring force $F_{\text{res}}$ as:

$$F_{\text{res}} = kx$$  \hspace{1cm} (2.32)

where $k$ is the effective spring constant of the diaphragm and $x$ is the diaphragm displacement. The displacement $x$ was defined as:

$$x = x_o - d$$  \hspace{1cm} (2.33)

where $x_o$ is the gap distance between the plates before actuation and $d$ is the gap distance after actuation. At equilibrium, the mechanical restoring force is equal to the electrostatic force:

$$F = F_{\text{elec}} + F_{\text{res}} = 0$$  \hspace{1cm} (2.34)

The balanced load displacement can be found by combining Equations (2.29), (2.32), (2.33), and (2.34):

$$0 = \frac{\varepsilon \varepsilon_0 AV^2}{2(x_o - x)^2} - k(x_o - d)$$  \hspace{1cm} (2.35)

where $A = a^2$ for the square diaphragm. This equation accounts for the increasing electrostatic force with displacement, but it still assumes a rigid plate with uniform deflection toward the membrane. In reality, the sides of the diaphragm are fixed at the edges, so the deflection varies from little deflection near the sides to the largest deflection at the center. The approximation made for Equation (2.35) becomes less valid as the deformation becomes greater. At small deformations the membrane is closer to plate-like.

The effective spring constant of the membrane, $k$ can be found by using Equation (2.31) and solving for the force divided by the maximum deflection:
Replacing the spring constant in Equation (2.35) with this expression gives the overall system equation:

\[ k = \frac{F_{\text{elec}}}{w_{\text{max}}} = \frac{Eh^3}{0.01303a^2} \]  

(2.36)

From this equation the deflection of the diaphragm \(d\) can be calculated with diaphragm dimensions, applied voltage, and material properties.

2.3.3 Electrostatic Actuation Concerns

2.3.3.1 Pull-In Voltage

The upper limit of applied voltage for electrostatic actuation is the breakdown voltage predicted by Paschen’s Curve (Figure 2.3). As the distance between the two electrodes decreases, the electrostatic force increases nonlinearly. With an increasing applied voltage, the electrostatic force curve increases \((V_d>V_3>V_2>V_1\) on Figure 2.3). At the pull-in voltage, the electrostatic force over-exceeds the mechanical restoring so that that deflection of the membrane cannot balance the forces. The top electrode deflects so far that it hits the bottom electrode and sticks, resulting in snap-down. At the pull-in voltage, the electrostatic force becomes tangential to the mechanical restoring force, indicating that any voltage at or above this voltage will prevent equilibrium between the two forces. Staying below this pull-in voltage will prevent snap-down.
Figure 2.3: Paschan’s Curve. The mechanical restoring force and electrostatic force graphed as a function of the distance between the plates, $x$. At higher voltages, the electrostatic force curve rises. The intersection points between the two curves are equilibrium points (left). The voltage at which the mechanical restoring force lies tangentially to the electrostatic force (right) is the pull-in voltage, $V_4$. Above this voltage, equilibrium does not exist and snap-down occurs.\[3\]

The pull-in voltage $V_p$ can be found by taking the derivative of Equation (2.35) with respect to $x$:

$$0 > \frac{\varepsilon \varepsilon_0 AV^2}{d_o - x^3} - k$$

Equation (2.35) can be further manipulated:

$$0 > x \frac{\varepsilon \varepsilon_0 AV^2}{d_o - x^3} - \frac{\varepsilon \varepsilon_0 AV^2}{2} \frac{d_o}{d_o - x^2}$$

Solving Equation (2.39) for $x$ gives the critical displacement $x_c$:

$$x_c = \frac{d_o}{3}$$

The membrane cannot deflect more than a third of the gap distance otherwise snap-down will occur. This model should provide a generous measurement because the added support of a four-sided diaphragm should increase the mechanical restoring force and allow for a higher pull-in voltage. The pull-in effect can be eliminated with a series capacitor but a much higher operation
voltage is required to support the two capacitors.[4] Substituting the critical displacement for the displacement in Equation (2.36) gives an equation of critical design parameters:

\[
\frac{8}{27} d_0^2 = \frac{0.01303 \varepsilon_0 V^2 a^4}{E h^3}
\]  \hspace{1cm} (2.41)

2.3.3.2 Fringe Effects

Fringe capacitance along the edges of the diaphragm can alter the electrostatic force attraction.[3] For this device, the side lengths of the plates are much larger than the spacing between them, so fringe effects can be ignored.[6]

2.3.3.3 Breakdown Voltage

Paschen's law states the breakdown voltage between parallel plates separated by a gas is a function of operating pressure \( p \), and electrode gap distance, \( d \):[19]

\[
V_b = \frac{A(pd)}{\ln(pd) + B}
\]  \hspace{1cm} (2.42)

Where \( A \) and \( B \) are experimentally obtained constants dependent upon the gas medium. For air, \( A \) is 15 cm\(^{-1}\)Torr\(^{-1}\) and \( B \) is 365 V\(^{-1}\)Torr\(^{-1}\)cm\(^{-1}\). This breakdown voltage needs to be avoided to prevent electron ionization between the electrodes.

2.4 Design Constraints

Design constraints were applied to eliminate variables in determining the geometry of the diaphragm. The range of applied voltages, materials, and dimensions needed to be defined before the design equations could be solved.

2.4.1 Applied Voltage

As previously stated, the gap distance between the plates is constrained to larger distances due to microfabrication processing. To get a deflection high enough to be measured by a micro-force measurement system, a large voltage and large plate area was used for this research. The
maximum voltage that can be achieved by the MEMS driver is 300V. To avoid such high voltages, 200V was chosen as a target voltage.

2.7.2 Material Selection

Materials for different parts of the device were selected based on design requirements and fabrication capabilities (Figure 2.4). Silicon was chosen for the diaphragm material because it can be etched to achieve a small diaphragm thickness. Silicon wafers are compatible with our microfabrication equipment and is the most widely used substrate in MEMS design.[20] Silicon is ideal for the following reasons:

1. It is mechanically stable.
2. Multiple electronics can be integrated and circuited onto a single substrate.
3. It has a high Young’s modulus of 150 GPa, allowing for fast actuation times with an oscillating voltage.
4. It is very light, about the same mass density as aluminum (2.3 g/cm$^3$).
5. It has a high melting temperature of 1400°C. The silicon can easily withstand oxidation processing temperatures of 1050°C.
6. The coefficient of thermal expansion is small compared to comparable materials. This is important because the coefficient of thermal expansion of silicon dioxide is very small. Silicon dioxide is used as a masking layer and etch stop in the fabrication process. If the difference of coefficients of thermal expansion between the silicon and silicon dioxide contributes to stress build-up at the interface between the layers. These stresses may cause warping in the thin membrane of the device.

The bottom of the device will be made of Pyrex, a borosilicate glass. Pyrex was chosen because it is transparent, allowing accurate alignment between the top and bottom structure. Gold has good adhesion to Pyrex; Pyrex can be masked and sputtered to create a conductive counterelectrode. The silicon diaphragm and Pyrex wafer will be bonded together with SU-8, a photo-definable epoxy based polymer. SU-8 can be spin-coated to a 40 micron thickness and
then cured with applied heat and pressure to seal the cavity. This will be the material that forms the side walls of the cavity.

Figure 2.4: Materials Selection for Microspeaker. The diaphragm is silicon, the bottom plate is Pyrex, and the walls are SU-8.

2.4.3 Dimension Constraints

The electrostatic force increases proportional to the plate area (Equation 2.29). To maximize the electrostatic force, the plate area needs to be maximized.

The electrostatic force between electrodes increases with smaller gap distances. The SU-8 used to fabricate the side-walls of the diaphragm can be coated at a 40μm thickness. This will be the maximum gap distance used for design purposes.

2.5 Concerns with Dimension Selection

The calculations performed thus far are simplified estimates. Accurate solutions are complicated problems that can only be solved through Finite Element Analysis. A COMSOL model was produced to provide better conceptual modeling.

Past experiments with bonding SU-8 to Pyrex and silicon have been unsuccessful. Researching alternate bonding methods is necessary to determine the sidewall thickness used in calculations.
SOI wafers have not been etched to create diaphragms in our lab. Diaphragms should be fabricated and examined for warping or pin-hole etching to verify the 10µm thick diaphragm used in calculations.
Section 3: First Fabrication of Diaphragms

3.1 Summary

A silicon-on-insulator (SOI) wafer with a 20 μm thick device layer was chosen to provide an etch stop for silicon etching during diaphragm fabrication. The wafer was oxidized, patterned to create etch windows, and anisotropically etched with 25% tetramethylammonium hydroxide (TMAH), which terminated at the embedded oxide layer. Finally the diaphragms were inspected and the etch depth was measured with a profilometer. Critical device design dimensions (gap thickness and diaphragm thickness) were unknown at this time, so device masks were not created for the initial fabrication run. This fabrication process was done to prove the usability of SOI wafers in the final design and examine the degree of warping or pinholes as a function of size. A mask created by Brian Stahl was used for lithographic patterning to produce sixty diaphragms of five different sizes.[11]

3.2 Wafer Selection

The substrate selection is extremely important in MEMS design because the processing steps are highly dependent upon the particular crystallographic orientation and defect/impurity concentration. The crystallographic geometry especially influences silicon wet etching. The wafer must be polished on both sides with a low thickness variation to etch multiple uniform membranes. If the thickness of the substrate varies, so too will the membrane thicknesses. An SOI wafer was required to provide an etch stop that would allow multiple uniform membranes. Previous research done by Brian Stahl looked at doping a silicon substrate to create an etch-stop. Unfortunately, this created internal stresses in the membranes that caused warping.

SOI wafers are typically used in MEMS design to prevent charge leakage between p-n junctions.[21] I will be using one to fabricate membranes with the embedded oxide layer as an etch-stop. The wafer is a double-side polished, 100 mm (diameter) SOI prime silicon wafer. The crystal orientation is <100> ± 0.5°. This orientation was chosen because it provides a flat bottom parallel to the surface for membrane fabrication (Figure 3.1).
Figure 3.1: Anisotropic Silicon Etching. a) anisotropic silicon etching of a (100) wafer b) anisotropic silicon etching of a (110) wafer.

The SOI wafer used during initial fabrication has three layers; a 400 ± 10 µm thick handle layer, a 2 ± 0.10 µm thick embedded oxide layer, and a 20 ± 1 µm thick device layer (Figure 3.2). I etched through the wafer handle, so the critical tolerance was with the N-type silicon device layer that will be the thin membrane. The thickness variation for the device layer (1 µm) is much less than the overall thickness of the diaphragm (20 µm).

Figure 3.2: Silicon-on-Insulator Wafer Cross Section

3.3 Wet Thermal Oxidation

An oxide layer was grown on both sides of the wafer to provide an etch mask during silicon etching (Figure 3.3). The oxide layer was patterned with lithography on the handle side of the wafer to create etch windows and the device layer remained covered by the oxide until silicon etching was complete. Thermally grown oxides are commonly used as mask materials because they have a very low etch rates in silicon etchants. A thick oxide of 8000 Å was chosen as a target
to provide more than enough protection during etching and processing. Oxides thicker than 1μm can create bowing in the wafer.[20]

Figure 3.3: Wet Thermal Oxidation. Wafer cross section after oxidation (left) and the oxidation tube furnace (right)

3.3.1 Wet Oxidation vs. Dry Oxidation

There are several ways to deposit a silicon dioxide layer on silicon, but the least expensive method is by thermal oxidation. There are two methods of thermal oxidation: dry oxidation and wet oxidation. Both use an electric resistance furnace with a large fuzed quartz tube, as shown in Figure 3.4. Wet oxidation introduces water vapor into the furnace at high temperatures (1050°C). The water reacts with the silicon to create silicon dioxide on the surface of the silicon and dihydrogen gas.

\[ Si_{(solid)} + 2H_2O_{(gas)} \rightarrow SiO_2(solid) + 2H_2(gas) \]

The thermally grown oxidation layer has a different molecular volume and coefficient of thermal expansion than the silicon substrate. When the wafer is cooled the oxide layer is under compression, causing significant stress between the oxide layer and the substrate. Wet oxidation reduces these compressive stresses and speeds up the oxide growth. Oxidation takes less time with wet oxidation because a water molecule is much smaller than an O₂ molecule, so diffusion occurs much faster. Water also loosens the SiO₂ structure during oxidation, making it easier for a diffusing species.[20]

Dry oxidation introduces oxygen gas into the furnace instead of water. The oxygen reacts with the silicon to create silicon dioxide on the surface:
Dry oxidation takes longer and has higher stresses, but provides a better quality oxide layer.[20] 

\[ Si_{(solid)} + O_{2(gas)} = SiO_{2(solid)} \]

Figure 3.4: Oxidation Furnace Cross Section. [22]

Due to the membranes’ tendency to warp, I used wet oxidation thermally grown in an oxidation furnace. The oxide layer is used as a masking material, so an oxide grown by wet oxidation should be of sufficient quality.

It is important to note that silicon is consumed during oxide growth. The ratio of the oxide thickness grown into the wafer \( X_{si} \) to the total oxide thickness \( X_{ox} \) depends on the molecular densities of the two materials (Figure 3.5): [23]

\[
X_{si} = X_{ox} \times \frac{N_{ox}}{N_{Si}} = X_{ox} \times \frac{2.3 \times 10^{22} \text{molecules/cm}^3}{5 \times 10^{22} \text{atoms/cm}^3} = 0.46 X_{ox}
\]  

(3)
3.3.2 Estimating Oxidation Time

The Deal-Grove model predicts the oxide thickness $x_0$ based on the oxidation environment:[24]

$$\frac{x_0}{A} = 1 + \frac{t + \tau}{\frac{A^2}{4B}} - 1$$  \hspace{1cm} (3.2)

where $A$ for wet oxidation at 1050°C is 0.292μm and $B$ is 0.35μm$^2$/hr, $t$ is the oxidation time in hours, and $\tau$ is a factor that accounts for silicon's native oxide. At relatively long times, $t >> \frac{A^2}{4B}$, $t >> \tau$ and the equation can be reduced to:

$$x_0 \approx \frac{Bt}{A^2}$$  \hspace{1cm} (3.3)

With Equation (3.3) it is predicted that a two hour oxidation period at 1050°C will produce an 8000Å oxide thin film. [23]

3.3.3. Oxidation Process

Before thermal oxidation, the device wafer, two N-type control wafers, and two “dummy wafers” (previously used wafers that had been cleaned) were cleaned in Piranha at 70°C to remove
organics and dipped in a buffered oxide etchant (BOE) for 5 minutes to remove any existing oxides. Two N-type dummy wafers were placed on either side of the SOI wafer and control wafers. The dummy wafers are used to minimize turbulent gas flow around the SOI wafer. The doping type matches the device side of the wafer, preventing unwanted doping of the device layer that could later contribute to wafer bowing. The oxidation tube furnace was preheated to 900°C. Once 900°C was reached, ultra-high-purity (UHP) nitrogen (N₂) was turned on at a 5 L/min flow rate. The SOI wafer surrounded by the dummy wafers were placed in a quartz boat and loaded into the furnace at about 0.5 cm/second to prevent thermal shock. The temperature was then increased to 1050°C while the UHP N₂ prevented oxidation. Once the desired oxidation temperature (1050°C) was reached, the UHP N₂ was stopped and UHP oxygen (O₂) was turned on at a 5 L/min flow rate. The UHP O₂ was bubbled through boiling water to produce a water vapor for wet oxidation. The wet oxidation was carried out for two hours. After two hours, the furnace and UHP O₂ were turned off, and UHP N₂ was switched back on at 5 L/min to prevent further oxidation during cooling. When the furnace reached 900°C, the UHP N₂ was turned off and the furnace was allowed to cool overnight. Once at room temperature (RT), the quartz boat was removed from the furnace. The oxidation process is summarized in Table (3.1).

Table 3.1: Oxidation Process Steps for an 8000Å Oxide Film

<table>
<thead>
<tr>
<th>Process Step</th>
<th>Temperature</th>
<th>Gas</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre-heat furnace</td>
<td>RT to 900°C</td>
<td>None</td>
</tr>
<tr>
<td>Insert Wafers</td>
<td>900°C</td>
<td>UHP N₂ at 5 L/min</td>
</tr>
<tr>
<td>Warm-up</td>
<td>900°C to 1050°C</td>
<td>UHP N₂ at 5 L/min</td>
</tr>
<tr>
<td>Oxidation for 2 hours</td>
<td>1050°C</td>
<td>Wet UHP O₂ at 5 L/min</td>
</tr>
<tr>
<td>Cool-down</td>
<td>1050°C to 900°C</td>
<td>UHP N₂ at 5 L/min</td>
</tr>
<tr>
<td>Cool-down</td>
<td>900°C to RT</td>
<td>None</td>
</tr>
<tr>
<td>Remove Wafers</td>
<td>RT</td>
<td>None</td>
</tr>
</tbody>
</table>

3.3.4 Measuring the Oxide

After the wafers were removed from the furnace, a Filmetrics F20 thin-film measurement system was used to measure the oxide thickness on both sides of the SOI wafer. Each side was measured in six different places (Figure 3.6).
Figure 3.6: (a) The oxide grown on the SOI wafer measured in 6 places with a (b) Filmetrics F20 thin-film measurement system.

The average oxide thickness was 842 nm on the device side and 850 nm on the handle (Table 3.2). This is considerably more than predicted by the Deal-Groove model. The thermally grown SiO$_2$ layer is in compression due to the difference of molecular volume and thermal expansion between SiO$_2$ and Si. The compressive stress is dependent upon the oxide thickness; SiO$_2$ films thicker than 1 μm can cause significant wafer bowing. An oxide thickness less than 850 nm would be favorable to reduce the potential for membrane warping.

Table 3.2: SOI Oxide Measurements at Locations Indicated on Figure 3.4(a)

<table>
<thead>
<tr>
<th>Location</th>
<th>Device Side Oxide Thickness(Å)</th>
<th>Handle Side Oxide Thickness(Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>8389.9</td>
<td>8472.6</td>
</tr>
<tr>
<td>2</td>
<td>8404.6</td>
<td>8473.8</td>
</tr>
<tr>
<td>3</td>
<td>8422.9</td>
<td>8550.0</td>
</tr>
<tr>
<td>4</td>
<td>8417.7</td>
<td>8494.0</td>
</tr>
<tr>
<td>5</td>
<td>8482.0</td>
<td>8494.1</td>
</tr>
<tr>
<td>6</td>
<td>8414.2</td>
<td>8493.8</td>
</tr>
<tr>
<td><strong>Average</strong></td>
<td><strong>8421.9</strong></td>
<td><strong>8496.4</strong></td>
</tr>
</tbody>
</table>

As previously discussed, the oxide grows into the silicon as well as out of the silicon. Using Equation 3.1, the oxide growth into the silicon $X_{Si}$ is calculated to be 437 nm, leaving a device side thickness of approximately 19.5 μm.
3.4 Lithography

Following oxide measurements, the SOI wafer was cleaned in 70°C Piranha for 10 minutes, 25°C buffered oxide etchant (BOE) for 5 minutes, and spin-rinsed and dried with low-purity (LP) nitrogen using a spin-rinse-drier (SRD).

The SOI wafer was first baked on a hot plate at 150°C for 5 minutes to remove any solvents or water left over from the cleaning process. The wafer was placed in a Laurell Technologies WS-400B-6NPP spin-coater with the handle side facing up and held with a vacuum chuck. 2.5mL of Microchem MCC Primer 80/40 was applied to the wafer to promote adhesion between the resist and wafer. The wafer was spun at 300RPM for 30 seconds and 3000 RPM for 30 seconds. Next, 5 mL of Rohm-Haas Microposit s1813 positive photoresist was dispensed into the center of the wafer in a continuous stream. It is important to prevent bubble formation during the photoresist application process. Bubbles will prevent areas of the wafer from being coated and the spin-coating procedure will have to be repeated. The wafer was spun at 500RPM for 10 sec, 4000RPM for 20 sec, and 300RPM for 5 sec. The first spin step spread the photoresist over the wafer surface, the second planarized the photoresist, and the last step brought the wafer to a gradual stop (Table 3.3). The wafer was removed from the spin-coater and soft-baked on a hot-plate at 90°C for 1 minute to drive off solvents, reduce stresses, and promote adhesion between the resist and wafer.[20]

Table 3.3: Spin coating steps used for positive photoresist application

<table>
<thead>
<tr>
<th>Step #</th>
<th>Speed (RPM)</th>
<th>Time (s)</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>300</td>
<td>30</td>
<td>Spread primer over wafer surface</td>
</tr>
<tr>
<td>2</td>
<td>3000</td>
<td>30</td>
<td>Planarized primer</td>
</tr>
<tr>
<td>3</td>
<td>3000 to 200</td>
<td>20</td>
<td>Slow wafer, pause during this step to apply resist</td>
</tr>
<tr>
<td>4</td>
<td>200 to 500</td>
<td>10</td>
<td>Spread resist over wafer surface</td>
</tr>
<tr>
<td>5</td>
<td>4000</td>
<td>20</td>
<td>Planarized resist</td>
</tr>
<tr>
<td>6</td>
<td>4000 to 300</td>
<td>5</td>
<td>Slow to stop</td>
</tr>
</tbody>
</table>

The wafer was then placed in a Canon PLA-501FA aligner for mask alignment and exposure. A control wafer was exposed to 16 light integrals between 3.5 and 5 to determine the optimum light integral. A light integral of 4 was chosen (Figure 3.7), corresponding to a 15 second exposure.
time with a 150mJ/cm² exposure dose. A diaphragm mask created by Brian Stahl was aligned to the wafer and the wafer coated with resist was exposed by the aligner with a mercury arc lamp. The exposed positive photoresist was weakened by rupture or scission of the main and side polymer chains, making exposed areas soluble in developer.[20] The wafer was placed in Rohm Hass CD-26 positive resist developer for 2 minutes at room temperature to remove the soluble regions. This left the unexposed photoresist in the pattern of the mask. The wafer was then inspected to ensure proper pattern transfer (Figure 3.8 (b)).

Figure 3.7: Control wafer tested with various light integrals showed the optimum light integral of 4. (a) shows a square geometry created on the test wafer and (b) shows ten micron thick channels.

Finally the wafer was hard baked for one minute at 150°C to drive off any remaining solvents and ensure that the reactions initiated by exposure had run to completion. A cross section of the device at this point is shown in Figure 3.8.
3.5 Mask Oxide Etch

The exposed oxide was etched in a buffered oxide etchant (BOE) containing hydrofluoric acid (HF) and a buffering agent (NH₄F). The buffering agent stabilizes the pH under the oxide ledge to prevent lateral undercutting of the oxide. This improves pattern transfer and prevents the delamination of the photoresist mask layer compared to an HF:H₂O solution.[25][26] While BOE does not react with silicon, it is important to note that contamination with highly electronegative metallic ions can create pitting corrosion on the silicon surface.[26] For this reason, a new batch of BOE was used for device testing and fabrication. The dissolution of silica in HF solution is shown in the following reactions:[27]

\[ SiO₂ + 4HF \rightarrow SiF₄ + 2H₂O \]

\[ SiF₄ + 2HF \rightarrow H₂SiF₆ \]

3.5.1: Characterizing the Etch Rate

The etch rate of the buffered oxide etchant (BOE) was characterized to determine an appropriate etch time to remove the exposed oxide. An oxidized test wafer was vertically suspended in BOE at room temperature (Figure 3.9). Every two minutes it was removed from the solution, rinsed in
DI water, and returned to the solution at a raised level. This process exposed different regions to different etch times.

Figure 3.9: Method for testing the oxide etch rate in BOE. A) shows the wafer suspended on the single wafer holder before etching, b) shows the wafer in the BOE solution.

After 10 minutes, the wafer was removed and the oxide measured with the Filmetrics thin-film measurement system. Results are given in Table 3.4. After 8 minutes, the oxide was completely removed. The slowest average etch rate (from 2-4 minutes) is 1124 Å/min. This is very close to the reported .1μm/min etch rate of BOE. [25]

Table 3.4: Oxide etch rates for test wafer in BOE over 10 minutes.

<table>
<thead>
<tr>
<th>Etch Time (minutes)</th>
<th>Oxide Thickness (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>8382.1</td>
</tr>
<tr>
<td>2</td>
<td>3479.1</td>
</tr>
<tr>
<td>4</td>
<td>1030.7</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>0</td>
</tr>
</tbody>
</table>

Using the 1124 Å/min etch rate, 8 min is required to remove the 842 nm oxide layer. To be sure the entire oxide is removed, a 10 min etch time was chosen. BOE does not react with silicon, so over-etching is not a concern.[26]
3.5.2 Device Oxide Etching

The SOI wafer was placed in a single-sided etching apparatus with the handle side up (Figure 3.10). The handle patterned with a photoresist mask was exposed to BOE for 10 minute at room temperature. Single sided oxide patterning can also be accomplished by coating the backside with photoresist and hard-baking without exposure to leave it unpatterned. This method is not ideal for two reasons. First, spin-coating does not cover the edges of the wafer; the exposed oxide around the rim will be etched by the BOE. The exposed silicon on the rim will be etched during deep silicon etching, adding to the silicon contaminants in the TMAH solution. Second, placing a photoresist-coated wafer directly onto the vacuum chuck of the spin-coater can break the vacuum if photoresist is chipped off and sucked through the vacuum chuck. To eliminate these risks, a single-sided etcher was used.

![Figure 3.10: Single-Sided Etcher. The single-sided etcher has two o-rings that seal the wafer between two Teflon wafer holders. Full assembly with BOE is shown (left), and the two halves of the etcher before assembly are shown (right).](image)

Following the oxide etch, the wafer was rinsed with DI water and submerged in a beaker of 1500mL Shipley Microposit Remover 1165 at 60°C for ten minutes to remove the photoresist mask. The wafer was lightly agitated to promote physical removal of the dissolved photoresist. The Microposit Remover is compatible with Si, SiO₂, and Teflon cassettes.[28] It is important to
note that the flash point of Microposit Remover 1165 is 88°C.[28] The device cross-section at this point is shown in Figure 3.11.

![Figure 3.11: Wafer Cross-Section after BOE Etch. The oxide layer (white) has been etched in a buffered oxide etchant (BOE). The photoresist has been removed, leaving exposed silicon (grey) etch windows.](image)

3.6 TMAH 25% Anisotropic Wet Etching

The 20 μm thick diaphragms were created by etching the silicon with 25% tetramethylammonium hydroxide (TMAH). The SOI wafer was covered with a continuous oxide on the device side and a patterned oxide on the handle. The embedded oxide layer in the SOI wafer is positioned 20 μm away from the device side. The patterned handle was etched to a depth of 400 μm where etching terminated at the embedded oxide, leaving 20μm of silicon on the device side. TMAH has an excellent selectivity of silicon dioxide to silicon. SiO$_2$ etches 4 orders of magnitude lower than (100) Si.[20] To etch through 400μm of silicon, 400 angstroms of oxide is needed. This far exceeds the 8420 Å oxide created during oxidation.

TMAH’s etch rate increases with decreasing TMAH concentration. To keep the concentration constant, the etching was performed in a condenser chamber to prevent evaporation during etching. The etching chamber (Figure 3.12) has a two water cooling lines that condense and redeposit evaporated chemical back into the solution. The lid is secured tightly with screws and an o-ring. Two thermocouples access the solution through a glass vent tube; one thermocouple goes to the resistive heating wrap and one goes to a thermometer. The foil wrap heater is controlled by an Omega temperature controller and regulates the temperature of the bulk
solution. To achieve a stable etching temperature of 85°C, the hot plate was set to 130°C and the foil wrap heater was set to 85°C. A stir rod was used at a stir speed of 1 to reduce the formation of bubbles or areas of concentrated etchant. Bubbles on the silicon surface can prevent the transfer of etchant to the surface, causing micromasking and increasing the surface roughness.[20]

Figure 3.12: Condenser Chamber Diagram. This condenser chamber was created in our lab at Cal Poly for deep etching.

TMAH was chosen over other etchants for its many advantages. THAH does not decompose below 130°, is nontoxic, relatively inexpensive, and easily handled.[20] It already exists in the positive photoresist developer in our lab; a system exists for its storage and disposal.

TMAH in low concentrations etches faster, but often leaves hillocks and rough surfaces. A TMAH concentration of 25 wt% was chosen because this was the concentration available in our lab, and therefore the maximum concentration I could work with. A higher concentration would provide a slower etch rate and a less sensitive etch stop time.
The reactant transportation rate is dominated by diffusion and can be increased by solution agitation. Stirring the solution can also reduce bubbles and regions of accumulated reactants. The surface reaction rate is most influenced by the temperature, etched material, and etchant concentration. The reaction sequence is as follows:[29]

\[ Si + 2OH^- + 2H_2O \rightarrow SiO_2^- + 2H_2 \]

TMAH is an anisotropic etchant that creates geometric shapes bound by crystallographic planes. Silicon has a diamond cubic crystal structure with different amounts of atoms aligned along different crystallographic planes. Figure 3.13 shows the structures resulting from a TMAH etch with a square mask pattern. (a) shows a large square opening along the (110) direction that is representative of my mask design, (b) shows the consequence of a smaller square opening, and (c) shows the effect of orienting the square edge along the (100) direction. Silicon etches fastest along the plane parallel to the wafer surface (100) and more slowly along the (111) plane. The (111) plane makes an angle of 54.74° with the (100) plane, as seen in the etch profile.

Figure 3.13: Diagram of geometric profiles formed by various mask designs. The top pictures are the masks and the bottom pictures are the resultant etch profiles [29]

35
Figure 3.13 (b) shows the importance of designing a large enough square mask pattern to avoid the etched side walls from coming in contact to form a tetrahedron. These tetrahedrons eliminate exposure to the (100) plane so that etching occurs only along the (111) planes, greatly slowing the etch rate. Figure 3.13 (c) shows that the mask pattern must be aligned in the [110] direction to maintain a suitable profile.

The SOI wafer was etched for a total of 10 hours in 2000mL of 25% TMAH at 85°C until the embedded oxide was visually exposed on the surface of the diaphragms.

3.7. Membrane Characterization

Sixty silicon diaphragms of five sizes were produced with the previous etching procedure. The devices were inspected and measured with a profilometer to ensure that the proper etch depth had been achieved. The embedded oxide was not removed because the profilometer’s maximum depth measurement is 400 μm, exactly the difference between the top of the wafer and the embedded oxide. The diaphragms and corresponding side lengths are shown in Figure 3.14.

Figure 3.14: Initial fabrication produced diaphragms with five side lengths. a) 1.3 mm, b) 2.2 mm, c) 3.0 mm, d) 3.7 mm, e) 4.4 mm. The embedded oxide can be seen in the green interior.

3.7.1 Profilometry

The etch depth of the cavities were verified with a stylus profilometer. Twenty diaphragms were measured and all had etch depths of 400 ± 1 μm, indicating that the diaphragms are around 20 μm thick (Figure 3.15). It should be noted that the maximum measurement capacity of our profilometer is 400 μm, so this measurement tool would not be useful for measuring larger etch depths.
Figure 3.15: Etch Profile of a Diaphragm. The blue reference lines indicate the 100μm etch depth and 20μm diaphragm thickness. The sloping silicon etch profile is a consequence of the crystallographic planes.

3.7.2 Device Failure

72% of the diaphragms were fabricated without holes or warping. Small etched square holes in the diaphragms were the main cause of device failure (Figure 3.16). This could have been the result of pinholes (holes in the oxide structure) on the device side of the wafer created in the wet oxidation process known to form low density oxide structures. Pinholes would allow TMAH to contact the device side of the wafer and etch through the silicon. These holes act as small masks like in Figure 3.11, creating a pyramidal etch profile with a square base.
Figure 3.16: A hole in a diaphragm likely created by an oxide pinhole. The marked hole is about 32 μm by 32 μm large.

Two of the larger diaphragms (4.4 mm side length) exhibited slight warping. Diaphragm warping was expected due to the 850 nm thick oxide layer. The degree of warping of the diaphragm bilayer was investigated. Solids expand upon heating and contract upon cooling. The degree of expansion is a factor of the material’s thermal expansion coefficient $\alpha$, Young’s Modulus $E$, and the thickness $t$. The radius of curvature, $\rho$ can be calculated by the following equation:[16]

$$\frac{1}{\rho} = \frac{6 \left[ 1 + \frac{t_1}{t_2} \right] \frac{1}{t_2} (\alpha_1 - \alpha_2) \Delta T}{h \left[ 3 \left( 1 + \frac{t_1}{t_2} \right)^2 + 1 + \frac{t_1 E_1}{E_2 t_2} \left( \frac{t_1}{t_2} \right)^2 + \frac{1}{t_2 E_2} \right]}$$  \hspace{1cm} (3.4)

The radius of curvature was calculated to be approximately 1.4 cm with the values in Table 3.5, a total thickness $h$ of 22 microns, and a change in temperature of 1030°C. This is an extremely large radius of curvature. In reality, the backside of the device layer was supported by the embedded oxide layer, which was supported by the handle layer. The actual degree of warping was much less and is a four-layer problem that is much more complicated.

Table 3.5: Values used in calculating the radius of curvature for a bilayer diaphragm

<table>
<thead>
<tr>
<th>Variable</th>
<th>Layer 1 (Oxide)</th>
<th>Layer 2 (Silicon)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t$</td>
<td>2 μm</td>
<td>20 μm</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>0.5E-6 °C</td>
<td>2.33E-6 °C</td>
</tr>
<tr>
<td>$E$</td>
<td>385 GPa</td>
<td>150 GPa</td>
</tr>
</tbody>
</table>
3.8 Conclusions of 20 μm Diaphragm Fabrication

The previous fabrication process was largely successful in fabricating 20 μm thick diaphragms. The same procedure will be used with a second SOI wafer to create 10 μm thick diaphragms to allow for greater deflection. Improvements should be made to the condenser chamber to gain better control of the etch temperature. Removing the lid of the chamber to check the wafer required removal of the thermocouple which turned off the temperature controller. This dropped the temperature by about 5°C each time the lid was removed.
Section 4. Adhesive Testing for Sidewall Fabrication

Previous attempts in our lab to use SU-8 as a bonding agent between silicon and pyrex have been unsuccessful, so other bonding methods were investigated, notably TRA-Bond F112, BCB, and PMMA.

4.1 TRA-Bond F112

The first bonding material investigated was TRA-Bond F112, an adhesive used in our lab for the fabrication of fiberoptic cables. F112 is robust, impact resistant, thermal shock resistant, low in stress, and can be cured at room temperature. Table 4.1 lists relevant material properties.[30]

Table 4.1: Material Properties of TRA-Bond F112

<table>
<thead>
<tr>
<th>Physical Properties</th>
<th>Metric Values</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Viscosity</td>
<td>1800 cP</td>
<td>@ 25°C after mixing</td>
</tr>
<tr>
<td>Hardness, Shore D</td>
<td>86</td>
<td></td>
</tr>
<tr>
<td>Adhesive Bond Strength</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17.2 MPa</td>
<td>Lap shear, cured for 24 hrs @ 25°C</td>
<td></td>
</tr>
<tr>
<td>20.7 MPa</td>
<td>Lap shear, cured for 1 hr @ 65°C</td>
<td></td>
</tr>
<tr>
<td>29.6 MPa</td>
<td>Lap Shear, cured for 15 min @ 90°C</td>
<td></td>
</tr>
</tbody>
</table>

The adhesive was thinly painted onto a glass substrate and a diaphragm was placed on top. The adhesive stayed relatively fixed in its position, but after curing the cavity shape was lost (Figure 4.1).

Figure 4.1: Silicon diaphragm bonded to glass with TRA-Bond F112

In an attempt to physically confine the adhesive, a glass substrate was patterned with a negative image of the desired cavity using 10 μm thick positive photoresist SPR 220. The wafer was baked at 115°C to remove solvents from cleaning, spin coated with spin recipe in Table 4.2 to achieve a
10 μm thickness, soft baked at 115°C for 90 seconds to drive off excess solvents, exposed with the Cannon aligner, post-exposure baked at 115°C for 40 minutes, and developed with Microposit developer.

Table 4.2: Spin recipe used for positive photoresist SPR 220.[31]

<table>
<thead>
<tr>
<th>Step #</th>
<th>Speed (RPM)</th>
<th>Time (seconds)</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>300</td>
<td>30</td>
<td>Spread primer over wafer surface</td>
</tr>
<tr>
<td>2</td>
<td>3000</td>
<td>30</td>
<td>Planarized primer</td>
</tr>
<tr>
<td>3</td>
<td>3000 to 100</td>
<td>30</td>
<td>Slow wafer, pause during this step to apply resist</td>
</tr>
<tr>
<td>4</td>
<td>100 to 1000</td>
<td>60</td>
<td>Spread resist over wafer surface</td>
</tr>
<tr>
<td>5</td>
<td>1000 to 1800</td>
<td>4.6</td>
<td>Planarized resist</td>
</tr>
<tr>
<td>6</td>
<td>1800 to 0</td>
<td>42</td>
<td>Slow to stop</td>
</tr>
</tbody>
</table>

The adhesive was applied around the patterned resist, a glass plate was placed on top, and the device was placed in resist stripper to remove the resist from the interior cavity (Figure 4.2). This method was not successful; the resist could not be developed from the cavity.

![Figure 4.2: Process of confining adhesive to regions outside the patterned cavity. A) shows a silicon wafer patterned SPR 220 resist, b) shows the application of the TRA-Bond F112 adhesive, and c) shows the interior cavity.](image-url)
4.2 BCB

It was evident that a photo-definable adhesive was needed to create a defined interior cavity. A common photo-definable resin, benzocyclobutene (BCB) was investigated for use. BCB Cyclotene is a resin designed for planarization and dielectric applications. [32] Photo-definable BCB (Photo-BCB) can be patterned through lithography. Photo-BCB films can be applied to a substrate with a spin-coater with an adhesion promoter. A soft bake step is required to drive out residual solvents before exposure. Photo-BCB acts like a negative resist; regions exposed to UV light are cross-linked and unexposed regions are left soluble in developer. Typical processing conditions are given in Table 4.3. The doses shown are for UV I-line, 365-nm light exposure, which can be created by the mercury arc lamp in the Cannon aligner. The pattern is developed by immersing the substrate in corresponding developer, and a final hard bake dries the film to maintain vertical sidewalls. The BCB film can be soft-cured to bond multiple BCB layers together and hard cured for final mechanical stabilization. Soft-curing is typically performed at 210°C for 40 min and hard curing at 250°C for 60 min.

Table 4.3: Processing conditions for typical cyclotene resins. [33]

<table>
<thead>
<tr>
<th>Cyclotene Resin Type</th>
<th>Thickness After Soft Bake (μm)</th>
<th>Exposure Dose</th>
<th>Thickness after Hard Bake (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4022</td>
<td>5.2</td>
<td>20</td>
<td>3.8</td>
</tr>
<tr>
<td>4024</td>
<td>7.4</td>
<td>25</td>
<td>5.2</td>
</tr>
<tr>
<td>4026</td>
<td>13.3</td>
<td>60</td>
<td>10.2</td>
</tr>
</tbody>
</table>

BCB can be applied to silicon and glass; an adhesion promoter is recommended for adhesion to glass. This adhesive could be applied to both substrates, soft-cured, and layered together with a final hard-curing step. Unfortunately this material could not be used due to its high cost and short shelf-life (1-2 months in a refrigerator or 1 year in a freezer).[34] If more researchers in our lab were able to use the material, it would be a viable option.
4.3 PMMA

Polymethylmethacrylate (PMMA) is another photodefinable polymer commonly used in microfabrication processing. PMMA can be directly bonded to itself, to silicon, and to silica.[35] It is commonly used as a positive resist for lithography processes but can also be used as a coating to protect wafers during wafer thinning, a bonding adhesive, or as a sacrificial layer. PMMA requires deep UV, x-ray or e-beam exposure for lithography. Standard film thicknesses range from .1 to 5 μm, depending on the resist type and spin coating speed.[36] Lithography requires a clean substrate, spin-coater, hot plate that can reach 180°C, a compatible light source, and an MIBK developer. The thickest available photodefinable PMMA from Microchem is 950 PMMA, which can be coated to a 5 μm thickness. PMMA is relatively inexpensive compared to typical microfabrication chemicals. The biggest concern with using this material is finding a compatible light source. X-ray and E-beam sources are not available in our lab. UV exposure requires a 248nm deep UV light source with a >500mJ/cm² exposure dose. There are two UV light sources in our lab that have potential for use: a Mercury-Arc lamp aligner with a wavelength range from 100 nm to 475 nm, and an Avantes fiberoptic short wave UV Probe Model 11SC-1 OP with a 254 nm wavelength. PMMA and MIBK developer were ordered for experimentation as an adhesive. It is important to note that PMMA must be stored in a dry area at 10°C to 27°C (not refrigerated) and kept away from light, heat, oxidants, acids, and reducers. Any equipment exposed to PMMA can be cleaned with acetone.[36]

4.3.1 PMMA Photolithography

Processing parameters were modified from the recommended processing conditions in the PMMA Microchem Data Sheet to create a 5 μm thick PMMA layer.[36] A silicon test wafer was cleaned in Pirhana at 70°C for 10 minutes and BOE at room temperature for 5 minutes. The wafer was placed on the vacuum chuck of the Laurell spin coater and 5 mL of PMMA was dispensed onto the wafer with a syringe. The wafer was spun at 500 RPM for 5 seconds, 1000 RPM for 45 seconds, and then slowed to stop (Table 4.4).
Table 4.4: Spin recipe for PMMA

<table>
<thead>
<tr>
<th>Step #</th>
<th>Speed (RPM)</th>
<th>Time (s)</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>500</td>
<td>5</td>
<td>Spread PMMA over wafer surface</td>
</tr>
<tr>
<td>2</td>
<td>1000</td>
<td>45</td>
<td>Planarize PMMA</td>
</tr>
<tr>
<td>3</td>
<td>1000 to 0</td>
<td>5</td>
<td>Slow to stop</td>
</tr>
</tbody>
</table>

The wafer was aligned to a mask and exposed by the Cannon aligner with the maximum light integral available. The Cannon aligner uses a mercury arc lamp with a spectrum that ranges from 100 nm to 475 nm (Figure 4.3), however lower wavelengths have extremely low intensities. A high exposure time was chosen to see if this UV source would have any effect on the PMMA. The wafer was developed for 30 seconds in the MIBK developer at room temperature and examined for pattern transfer. No pattern was visible.

Figure 4.3: Mercury arc lamp wavelength spectrum with energy intensity for the Cannon aligner

The wafer was cleaned with acetone, Pirhana, and BOE before coating a second time. The same spin coating procedure was used (Table 4.4) and the wafer was exposed with the Avantes fiberoptic short wave UV Probe light (Figure 4.4). This pen light has a 254 nm wavelength, close to the required exposure light wavelength of 248 nm. The light has a small distribution around the target 254 nm light, so experimentation was done with various exposure times. The wafer was aligned with a mask and exposed with the pen light for ten minutes, examined after each one minute interval for pattern transfer. No pattern was seen. This is not surprising considering the pen light exposure dose is 4,500 μW/cm², or 4.5 mJ/cm², far below the recommended 500 mJ/cm².
Figure 4.4: Avantes fiberoptic short wave UV Probe light with a UV wavelength of 248 nm

It was evident that the available UV sources could not be used for the lithographic patterning of PMMA. The spec sheet indicates that PMMA can be exposed with an E-beam source. Next the test wafer was cleaned, coated, and scored into a piece small enough to fit into a scanning electron microscope (SEM). The piece was focused and imaged with different raster speeds to pattern the PMMA layer. Initial imaging used a voltage of 10 kV, filament current of 2.38 A, and spot size of 6. A reduced area was rastered at the fastest and slowest raster speeds (Fig 4.5) for two minutes. Development can be seen in the change of topography of the PMMA as the polymer is broken down by the E-beam.

Figure 4.5: PMMA exposure with SEM E-beam at a) a slow raster speed and b) a fast raster speed for 2 minutes.

To increase the energy of the E-beam, the voltage was changed to 15 kV for a slow raster at 5 and 10 minutes at 56x magnification (Figure 4.6). Then it was changed to 20 kV, and rastered slowly for 5 and 10 minutes (Figure 4.6).
Figure 4.6: E-beam exposure of PMMA with 15 kV for 5 minutes (top left), 15 kV for 10 minutes (bottom left), 20 kV for 5 minutes (bottom right), and 20 kV for 10 minutes (top right). Image taken at 56x magnification.

It can be seen that patterning was achieved with a slow raster at 20 kV for 10 min. A final exposure was taken at 53x to verify (Figure 4.7) that this lithography technique could be used for a larger device.

Figure 4.7: Lithographic patterning of PMMA with a SEM at 53x magnification. Rectangular image measures 300 microns tall by 550 microns wide.

4.3.2 PMMA Bonding

With a lithographic technique found to pattern PMMA in our lab, bonding was attempted between a glass slide coated with PMMA and a silicon wafer. The slide and wafer were cleaned and the slide was spin-coated with a 10μm thick layer of PMMA (using the spin recipe in Table 4.4). The slide was baked at 180°C for 20 min, brought into contact with the wafer, placed on a second hot
plate at 160°C, and a force applied with a ball point pen by writing over the area to be bonded. The wafers were then annealed at 180°C for 20 min.[37] Bonding was not successful through this process. The reason for unsuccessful bonding is unknown, but recommendations include exposing with a different light source, bonding at higher temperatures, and increasing the pressure. While exposing the PMMA with the SEM, the area surrounding the reduced, completely exposed area might be damaged due to e-beam imaging over the surrounding area. This could prevent bonding at low temperatures.

4.4 SU-8

Another student in our lab had developed a fabrication sequence for SU-8 that was successful in bonding pyrex to silicon. I tried his process sequence with two cleaned test wafers to verify his claims.

A silicon test wafer was cleaned in Piranha for 10 minutes, BOE for 30 seconds, and spin-rinse dried. A glass microscope slide was cleaned in IPA for 10 min in an ultrasonic bath. The silicon wafer was dehydration baked at 100°C for 10 min to remove any water or solvents left over from the cleaning process. The wafer was placed in the Laurell spin coater which was lined with Al foil to prevent SU-8 from sticking to the inside of the spin-coater. SU-8 2050 was applied to the wafer straight from the bottle in a continuous stream to prevent bubbles. The SU-8 2050 is very viscous; caution must be used in pouring it from the bottle. A quarter-sized amount was applied to the wafer, and the spin coater tilted to move the SU-8 to the center of the wafer. The wafer and SU-8 sat for two min until the SU-8 settled to a flat profile. The spin recipe in Table 4.5 was used to coat the wafer to a 30μm thick layer of SU-8. The sample was carefully taken out of the spin coater to prevent SU-8 from dripping from the spin coater lid onto the wafer. The wafer was soft-baked on a hot plate at 65°C for 5 minutes, 95°C for 15 minutes, and stepped down to 65°C for 30 seconds. The wafer was left to cool and thicken for 5 minutes before alignment.
Table 4.5: Spin Recipe used for SU-8 2050

<table>
<thead>
<tr>
<th>Step #</th>
<th>Speed (RPM)</th>
<th>Time (minutes)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>500</td>
<td>60</td>
<td>Coats the wafer with SU-8</td>
</tr>
<tr>
<td>2</td>
<td>2200</td>
<td>60</td>
<td>Planarizes the SU-8 layer</td>
</tr>
<tr>
<td>3</td>
<td>2200-0</td>
<td>30</td>
<td>Slows to a stop</td>
</tr>
</tbody>
</table>

The wafer was aligned to a mask with the Cannon aligner and exposed with a UV filter suspended above the mask. A control wafer was tested at 16 different light integrals to determine the optimum exposure dose, 34.5. The wafer was exposed and post-exposure baked at 65°C for 3 minutes, 95°C for 5 minutes, and 65°C for 30 seconds. Then it was developed in a Petri dish of PGMEA developer at room temperature with agitation. When the development looked complete it was rinsed with IPA. Under-developed soluble regions of Su-8 appear white. The wafer was put back into developer, removed and rinsed with IPA. This process was repeated until no white material remained on the surface.

The clean glass microscope slide was taped to a junk Si wafer with Kapton tape and dehydration baked for 30 seconds at 65°C, 5 minutes at 100°C, and 30 seconds at 65°C. Then it was placed in the Laurell spin coater and SU-8 2007 was applied straight from the bottle. Caution was taken when pouring this resist; it is much less viscous than the 2050. The wafer was spun with the spin recipe in Table 4.6 to produce a 10μm thick layer. The glass slide was removed from the junk wafer and set aside for 5 minutes to thicken.

Table 4.6: Spin recipe for SU-8 2007

<table>
<thead>
<tr>
<th>Step #</th>
<th>Speed (RPM)</th>
<th>Time (minutes)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>500</td>
<td>60</td>
<td>Coats the wafer with SU-8</td>
</tr>
<tr>
<td>2</td>
<td>3500</td>
<td>60</td>
<td>Planarizes the SU-8 layer</td>
</tr>
<tr>
<td>3</td>
<td>3500-0</td>
<td>30</td>
<td>Slows to a stop</td>
</tr>
</tbody>
</table>

The glass slide was then placed on top of the patterned wafer at room temperature with a glass Petri dish as pressure. Bonding could be seen through the glass slide as dark regions spreading over the bonded area. More weight was added (a total of 161.5 g) until the area had been completely bonded. The device was soft baked at 45°C for 15 minutes to continue the bonding.
The interior cavity was visually monitored through the glass slide to ensure that the SU-8 did not flow into the cavity. The device was then placed in the aligner, stacking it between a glass plate and the UV filter plate with hex nuts. A dummy wafer was placed inside the aligner and the device was exposed with a light integral of 24. The device was then post-exposure baked to finish the bonding reaction at 60°C for 30 seconds, 95°C for 20 minutes, and 60°C for 1 minute. The final bonded device was then imaged.

Figure 4.8: Final bonded structure of silicon and glass using SU-8. The macroscopic image (a) shows the dark bonded regions. The microscopic image (b) shows adequate patterning and cracking from thermo-cycling.

The bonding with SU-8 was successful with the exception of tiny bubbles. Cracking occurs during the heating and cooling of processing, but did not seem to affect the bond between the two substrates.

4.5 Conclusions of Adhesive Testing

SU-8 is the adhesive of choice for bonding silicon to glass with a defined pattern. PMMA has potential for use with the scanning electron microscope as an E-beam source. Adhesives that are not photo-definable cannot be used for creating a patterned channel or cavity. BCB would work if it could find more use in our lab.

4.6 Device Dimensions with Fabrication Capabilities

With a process outlined for creating diaphragms and sidewalls, device dimensions can be estimated using the original design equations. There is reasonable certainty that 10 μm thick diaphragms can be created using the same fabrication technique outlined in Section 3.6. The
processing parameters for bonding with SU-8 give a sidewall thickness of 40μm. Using Equation 2.37 and rearranging for the sidewall length gives:

\[
a = \sqrt{\frac{2x^2 Eh^3(x_0 - x)}{0.01303\varepsilon\varepsilon_0 V^2}} \tag{4.1}
\]

The parameters in Table 4.7 were applied to this equation to graph the diaphragm sidewall as a function of diaphragm deflection.

Table 4.7 Values Used in Calculating the Diaphragm Side Length

<table>
<thead>
<tr>
<th>Property</th>
<th>Symbol</th>
<th>Value</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Young's Modulus</td>
<td>E</td>
<td>150 GPa</td>
<td>For Silicon</td>
</tr>
<tr>
<td>Gap Distance at Rest</td>
<td>x_0</td>
<td>40 μm</td>
<td>Determined by SU-8 thickness</td>
</tr>
<tr>
<td>Diaphragm Thickness</td>
<td>h</td>
<td>10 μm</td>
<td>Determined by SOI device layer thickness</td>
</tr>
<tr>
<td>Permittivity of Air</td>
<td>\varepsilon</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Permittivity of Free Space</td>
<td>\varepsilon_0</td>
<td>8.854E-12 s^4 A^-2 m^-3 kg^-1</td>
<td></td>
</tr>
<tr>
<td>Applied Voltage</td>
<td>V</td>
<td>200 V</td>
<td></td>
</tr>
<tr>
<td>Diaphragm Displacement</td>
<td>x</td>
<td>1-12 μm</td>
<td>12 μm was chosen as the maximum displacement to prevent snap-down</td>
</tr>
</tbody>
</table>

Using Equation 4.1 and values from Table 4.7, the relationship between side length and diaphragm displacement were graphed (Figure 4.9).
A devices of side-length 1.5 mm to side-length of 4 mm would be adequate for device actuation given the estimations used in my calculation model. Any device larger than 4 mm is predicted to displace further than a third of the distance between the plates, and would be subject to snap down. Smaller diaphragms are extremely difficult to align and handle and I predicted that the devices would achieve smaller deflections than expected due to the unrealistic assumptions made for my model. Side lengths of 2.5 to 5 μm were then chosen for modeling.
Section 5. COMSOL Modeling

After appropriate device sizes were chosen, devices were modeled with COMSOL Multiphysics 4.3 (2012) to determine the effects of membrane size on the achieved deflection by actuation using finite element analysis (FEA). The results determined what range of diaphragm sizes would be used in the final design before making the photomasks.

5.1 Creating the Model

A two dimensional, symmetric model was created in COMSOL for computational simplicity. 3D COMSOL models are large computational problems that can require multiple computer processors to solve, so any symmetry should be taken advantage of. [38] My device will be tested at the center of the diaphragm where the deflection is the greatest. A 2D analysis of the cross section at the center will be sufficient to show the maximum deflection. The square diaphragms are symmetric about x-axis (Figure 5.1), so only half of the diaphragm cross section was modeled.

![Figure 5.1: Device cross section (red tint) that was modeled in COMSOL](image)

COMSOL modeling starts with determining the appropriate physics to apply to the model. COMSOL has many physics types available and they can be coupled to apply multiple physics problems to the same model. My model used electrostatics and solid mechanics to determine the deflection based on an applied voltage between two parallel conductive plates. A stationary solver was chosen to obtain stationary solutions. The geometry was drawn to mimic the device...
cross section with variables defined in the “Global Definitions” (Table 5.1). Boundary conditions were applied to fix the outer edge of the diaphragm and apply a voltage between the two conductive plates. A rough moving mesh was chosen for solver simplicity. The study was computed and displacement values recorded. A diaphragms of side lengths a=5 mm, 4.5 mm, 4 mm, 3.5 mm, 3 mm, and 2.5 mm were modeled to give the associated deflection shown in Figure 5.2. It was determined that diaphragms of side lengths 2.5 to 5 microns would show deflection adequate enough for device characterization.

Table 5.1: Geometric variables defined for COMSOL model of electrostatically actuated parallel plates.

<table>
<thead>
<tr>
<th>Variable Name</th>
<th>Expression</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>dBP</td>
<td>10 mm</td>
<td>Au backplate side length</td>
</tr>
<tr>
<td>tBP</td>
<td>500 μm</td>
<td>Au backplate thickness</td>
</tr>
<tr>
<td>dDia</td>
<td>2.5-5 mm</td>
<td>Si diaphragm side length</td>
</tr>
<tr>
<td>tDia</td>
<td>10 μm</td>
<td>Si diaphragm thickness</td>
</tr>
<tr>
<td>gap</td>
<td>40 μm</td>
<td>Air cavity gap</td>
</tr>
<tr>
<td>V0</td>
<td>200V</td>
<td>Applied voltage</td>
</tr>
</tbody>
</table>

![Deflection vs. Side Length](image)

Figure 5.2: Deflection as a function of side length for 6 diaphragm sizes.

5.3 Conclusions of COMSOL Modeling

The COMSOL models gave different results than the calculated estimations, but the chosen side lengths should still give enough deflection for characterization. The model can be improved by creating a 3D model, running a finer mesh, and altering the ideal material properties to match the material properties after fabrication. A comparison of the COMSOL model and hand calculations is done in Section 10.1.
Section 6. Final Fabrication of 10 μm Thick Diaphragms

6.1 Summary

After successful membrane fabrication with a 20 μm SOI wafer, a second SOI wafer with a 10 μm device layer was used to create my designed diaphragms (Figure 6.1). Masks were designed in AutoCAD to fabricate the final device diaphragms. The second diaphragm followed similar process steps as the first diaphragms, with notable exceptions. The wafer was oxidized, patterned, and anisotropically etched with 5% TMAH instead of 25% TMAH. This fabrication run was unsuccessful due to the inconsistent etching with 5% TMAH.

![Figure 6.1: Cross section of the SOI wafer used in the second diaphragm fabrication.](image)

6.2 Mask Design in AutoCAD

Lithography masks were created in AutoCAD to pattern the wafers to create square devices of side lengths: 2.5 mm, 3 mm, 4.5 mm, 4 mm, 4.5 mm, and 5 mm. Three masks were created for the entire fabrication process. Mask #1 (Figure 6.2) was designed to pattern the oxide mask on the SOI wafer to create 60 membranes (ten of each size). This mask has 50 μm thick break-lines around each diaphragm. Mask #2 (Figure 6.3) was designed to pattern gold coated glass slides to create the counter electrodes. Mask #3 (Figure 6.4) was designed to pattern the SU-8 for bonding between the glass slides and silicon diaphragms. The masks have different polarities to pattern the wafers in the correct manner. Positive photoresist becomes soluble when exposed to UV light and negative photoresist hardens when exposed to light. The mask used to create the
diaphragms has dark regions around the square membranes to create a mask for oxide etching. The mask used to create the counter electrodes has dark regions over the electrodes to create a mask that can protect the underlying gold electrode from etching. The mask used for SU-8 patterning has light regions where the SU-8 is needed for bonding (around the membranes) and dark regions where the SU-8 needs to be removed (directly below the membranes). Mask #2 and Mask #3 align to ensure correct device alignment. Alignment was done by coping the drawing of Mask #3 into the drawing of Mask #2 and aligning their corners at the origin (0,0).

Figure 6.2: Mask #1 designed for patterning the oxidized SOI wafer for diaphragm fabrication
Figure 6.3: Mask #2 designed to pattern gold electrodes on glass substrates.

Figure 6.4: Mask #3 designed to pattern SU-8 for device bonding.
6.3 Wet Thermal Oxidation

An oxide layer was grown on both sides of the wafer to provide an etch mask during silicon etching with TMAH. The device wafer, two P-type control wafers, and two P-type dummy wafers were cleaned in Piranha at 70°C and dipped in BOE for 5 minutes to remove any existing oxides. Dummy wafers are placed in front of and behind the SOI wafer and control wafers to reduce turbulent gas flow that could create an uneven oxide layer. P-type wafers were chosen to match the device layer, preventing any unwanted diffusing species that could contribute to internal stress or wafer bowing. The oxidation process followed the same steps as in the first diaphragm fabrication run (Table 3.1). The oxidation furnace was preheated to 900°C and flooded with UHP N\textsubscript{2} at a 5 L/min flow rate. The three wafers were placed in a quartz boat and loaded at a rate of 0.5 cm/second to prevent thermal shock. The temperature was increased to 1050°C with UHP N\textsubscript{2} gas flowing through the furnace. Once 1050°C was reached, N\textsubscript{2} was stopped. UHP O\textsubscript{2} was turned on, bubbled through boiling water to create water vapor, and the wafers were oxidized for two hours. After oxidation, the furnace and O\textsubscript{2} were turned off, and the furnace was flooded with UHP N\textsubscript{2}. After the furnace cooled to 900°C, the N\textsubscript{2} was turned off and the furnace cooled to room temperature. It is important to note that the furnace’s UHP oxygen gas flow meter was broken at this time, so the inlet rate was unknown. This created an oxide thickness much different than the first fabrication run.

6.3.1 Oxide Measurement

Filmetrics F20 thin-film measurement software was used to measure the oxide thickness on both sides of the wafer in six places (see Figure 3.4 (a)). The mean measured oxide thickness was 6406 Å on the handle side and 6399Å on the device side (Table 6.1). Using Equation 2.42, the oxide growth into the wafer \( X_{Si} \) is calculated at 294 nm. This leaves a 9.7 μm thick layer of silicon on the device side.
Table 6.1 Oxide measurements for second SOI wafer

<table>
<thead>
<tr>
<th>Position</th>
<th>Device Side Oxide Thickness(Å)</th>
<th>Handle Side Oxide Thickness(Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>6428.0</td>
<td>6437.8</td>
</tr>
<tr>
<td>2</td>
<td>6376.3</td>
<td>6439.8</td>
</tr>
<tr>
<td>3</td>
<td>6384.3</td>
<td>6387.5</td>
</tr>
<tr>
<td>4</td>
<td>6415.1</td>
<td>6383.5</td>
</tr>
<tr>
<td>5</td>
<td>6444.4</td>
<td>6384.7</td>
</tr>
<tr>
<td>6</td>
<td>6390.6</td>
<td>6362.9</td>
</tr>
<tr>
<td>Average</td>
<td>6406.5</td>
<td>6399.4</td>
</tr>
</tbody>
</table>

6.4 Lithography

Before lithography, the SOI wafer was cleaned again in 70°C Piranha for 10 minutes, 25°C BOE for 5 minutes, and spin-rinse dried.

The SOI wafer and two control wafers were processed through the positive photoresist lithography procedure used in Section 3.4, but with a Brewer 200X spin coater.

Each wafer was baked at 100°C for 5 minutes to evaporate solvents or water left from the cleaning process. Then they were placed in a Brewer 200X spin coater (the SOI wafer with the handle side up). 2.5mL of an adhesion promoter, Microchem MCC Primer 80/40, was applied to the surface and the wafer spun at 300 RPM for 30 seconds to coat the wafer and 3000 RPM for 30 seconds to planarize the primer. 5 mL of Shipley S1813 positive photoresist was dispensed in a continuous stream onto the center of the wafer. The wafer was spun at 500 RPM for 10 seconds, 4000 RPM for 20 sec, and 300 RPM for 5 seconds. Further discussion of the importance of these spin coating steps is in Section 3.4.

The wafer was placed in a Canon PLA-501FA aligner for mask alignment and exposure. One control wafer was exposed at 16 different light integrals ranging from 3.5 to 5 to determine the best light integral. The optimum integral 4.4 was chosen (Figure 6.5). The second control wafer and SOI wafer were aligned to Mask #1 and exposed by the aligner’s mercury arc lamp. The wafers were developed in Rohm Hass CD-26 resist developer for 2 minutes at room temperature, and finally inspected to ensure proper pattern transfer.
Figure 6.5: Examination of light integrals that resulted in a) under exposed light integral 4.1 b) adequate exposure with light integral 4.5, and c) over exposure with light integral 4.5.

The wafers were hard baked for one minute at 150°C to drive off remaining solvents and complete reactions initiated by exposure had completed. The photoresist mask pattern transfer was examined under a microscope (Figure 6.6)

Figure 6.6: Micrographs of the pattern transfer shown on a) the edge of the diaphragm and b) the break-lines. The break lines were designed to be 50 microns thick, actual patterning reduced their thickness.

6.5 Oxide Etch and Resist Strip

The wafers were placed in the single sided etcher and etched with BOE for 10 min at room temperature to remove the exposed oxide (discussed in Section 3.5.2). The etch time was based on the previously found etch rate (found in Section 3.5.1). After oxide etching, the wafers were rinsed with DI water and submerged in 1500 mL of Shipley Microposit Remover 1165 at 60°C for
10 minutes to remove the photoresist mask. The wafers were inspected under a microscope to ensure adequate patterning of the oxide layer (Figures 6.7 and 6.8).

![Figure 6.7: Oxide patterning of the control wafer shown a) at the square corner and b) at the break lines.](image1)

![Figure 6.8: Oxide patterning of the SOI wafer shown a) at the square corner and b) at the break lines](image2)

6.6 Anisotropic Wet Etching

6.6.1 Condenser Chamber Improvements

Deep silicon etching was performed in the condenser chamber described in Section 3.6 with two notable improvements to the system. A second foil wrap heater was added and controlled by the same Omega temperature controller controlling the original foil wrap heater. The thermocouple
was moved from the vent tube and inserted through the side of the bottom half of the lid. The second foil wrap increased the system's temperature control, eliminating the need of hot plate heating. A stable temperature of 85°C with a 0.2°C temperature variance was achieved by setting the temperature controller to 85°C. The repositioning of the thermocouple also improved temperature control because it did not need to be removed each time the lid was removed. The placement also made it easy for the thermocouple to be positioned underneath the inserted wafer cassette, instead of needing to be fed through the vent tube into the solution above the wafer cassette. The hot plate was kept to control the speed of the stir rod.

6.6.2 Change in Available Etchants

Before using the provided 25% TMAH etchant, it was noticed that the expiration date of the etchant had past two months prior. The etchant was tested with a patterned test wafer to observe etching with the expired etchant. The wafer was placed in the condenser chamber with 2000 mL of TMAH at 85°C. The wafer was taken out at hour intervals and the etch depth measured with a profilometer. After measurement, the wafer was placed in BOE for 30 seconds at room temperature to remove the formed native oxide before being placed back into the TMAH etchant. After the first hour the silicon etch depth was 60μm, slow for typical TMAH etching values.[39] After the second hour, the etch depth was measured to be 61μm. After the third hour, the etch depth was constant at 61μm. The used expired etchant was then disposed of.

A new bottle of 25% TMAH was ordered but the company that provides our lab with TMAH will no longer ship TMAH in that concentration due to the risk associated with shipping the high concentration. 5% TMAH was purchased instead. While waiting for the etchant, I tested potassium hydroxide (KOH) to be potentially used as a silicon etchant.
6.6.3 KOH Testing

KOH is a common etchant used for silicon etching. It has an adequate selectivity of silicon to silicon dioxide, but is not as good as TMAH. The selectivity improves with decreasing temperatures, so a relatively low temperature of 70°C was chosen for testing. Etch rates increase with decreasing concentration. With a low etch temperature, a low concentration is ideal. Experiments show that solutions less than 30% KOH give a rough etch surface, so initial testing started with solution of 30% KOH and water. 30% KOH at 70°C etches silicon dioxide at 150 nm/hr and (100) silicon at 45 μm/hr. [40] Using these etch rates, 400 microns of silicon and would be etched in nine hours, requiring an 1.35 SiO₂ layer. An oxide layer that thick would likely cause significant warping in the membrane, but lower temperatures would necessitate an unreasonably long etch time. Two test wafers were oxidized and patterned by photolithography. The first wafer was cleaned with Pirahana for 10 min at 70°C and then dipped in BOE at room temperature for 30 seconds before testing. The wafer was placed in a 30% KOH bath at 70°C in the condenser chamber. The wafer was taken out after one hour to measure the etch depth. When the wafer was removed, it was apparent that the surface was far too rough to use the low concentration as an etchant. Etch pits were visible to the naked eye (Figure 6.9).

![Etch pits created during 30% KOH etching.](image)

If this etchant were used for the SOI wafer, the embedded oxide would be etched through before the silicon was completely removed from the handle. The profile was measured with a profilometer (Figure 6.10).
Figure 6.10: Profilometer measurement of 30% KOH surface. This profile reading shows a surface that varies by 6 μm.

It is possible that surface contamination contributed to the uneven etching. A second test wafer was cleaned with Piranha solution at 70°C for 10 min, dipped in BOE for 30 seconds, and then placed in a 6:1:1 ratio mixture of DI water: HCL: Hydrogen Peroxide in an ultrasonic cleaner for 10 minutes. The final cleaning step was taken from the RCA cleaning process, a commonly used cleaning sequence that was first developed at the RCA laboratories.[41] The 6:1:1 ratio mixture removes ionic and metal surface contamination. The wafer was rinsed with DI water between each chemical treatment.

The second test wafer was placed in a 40% KOH solution at 80°C to investigate the surface roughness created by a higher temperature and KOH concentration. The wafer was taken out after one hour and the surface examined. As seen in Figures 6.11 and 6.12, the surface roughness was greatly improved. However, the high SiO₂ etch rate prevents this etch technique from being used for silicon deep etching. It would however be effective for a shallow etch.
Figure 6.11: Silicon etching with 40% KOH at 80°C. The surface has a mirror finish, but etched through the oxide mask.

A profile measurement was taken with the profilometer (Figure 6.12). The 0.2 μm surface variation is a vast improvement from the previous KOH etch.

Figure 6.12: Profile taken of silicon surface after etching with 40% KOH at 80°C. The surface varies by 0.2 μm.
6.6.4 5% TMAH Etching

Without any other etching options available, the SOI wafer was etched using the 5% TMAH solution at 85°C. The wafer was placed in the condenser chamber with the etchant for an hour, then removed for a profilometry measurement. After the first hour, the etch depth measured 60μm, which is slow for 5% TMAH etchant. The wafer was cleaned with Pirhana and a BOE dip before being placed back in the TMAH for another hour. The second Profilometry measurement showed an additional micron of etching. The wafer was cleaned, placed back in the solution, and etched for an additional hour. The third Profilometry measurement showed an etch depth of 61 microns, indicating that no etching had occurred. At this point, it was evident that removing the wafer from solution every hour was simply decreasing the oxide mask thickness during each BOE dip, so the wafer was placed vertically in the TMAH solution in an attempt to reduce surface bubbles and left for three hours (Figure 6.13).

Figure 6.13: SOI wafer suspended vertically in the 5% TMAH solution in the condenser chamber
6.6.5 Membrane Fabrication Failure

After three hours, the wafer appeared to be stripped of its oxide. The wafer was removed from the solution and the TMAH had etched through the silicon and silicon dioxide, leaving thin membranes with holes (Figure 6.14). The membranes were heavily warped, perhaps due to their 10 micron thickness (Figure 6.14).

Figure 6.14: Diaphragms resulting from a 6 hour etch in 5% TMAH at 85°C. a) shows diaphragm warping, b) shows holes through the diaphragm, c) shows the entire wafer.
Section 7. Final Device Fabrication

7.1 Summary

Due to the high cost of SOI wafers and unknown etching characteristics of 5% TMAH, the previously fabricated 20 μm thick membranes were used for the rest of the fabrication process. The diaphragms were matched with designed devices, glass substrates were coated with gold and patterned to create electrodes, and the devices were bonded with SU-8.

7.2 Diaphragm Matching with Designed Devices

The previously fabricated membranes do not exactly match my designed devices, so larger membranes were matched with smaller cavities to create the designed cavity size. The 4.4 mm side length diaphragms were matched with the 4.5 mm device cavities because they are so similar in size (Table 7.1).

Table 7.1: Diaphragm matching with designed device cavities

<table>
<thead>
<tr>
<th>Device Size</th>
<th>Diaphragm Side Length (mm)</th>
<th>Cavity Side Length (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Small</td>
<td>3.0</td>
<td>3.0</td>
</tr>
<tr>
<td>Medium</td>
<td>3.7</td>
<td>3.5</td>
</tr>
<tr>
<td>Large</td>
<td>4.4</td>
<td>4.5</td>
</tr>
</tbody>
</table>

7.3 Embedded Oxide Etch

The diaphragms that survived the initial fabrication run were scored into individual pieces and placed in a buffered oxide etchant (BOE) to etch the exposed embedded oxide. BOE is a wet etchant used to etch silicon dioxide or silicon nitride without compromising the silicon surface. The etch rate was previously characterized in Section 3.3.2. The diaphragms were placed in the BOE for 10 min to completely remove the oxide, leaving the 20μm silicon membranes.

7.4 Glass Scoring

Two microscope slides were scored into 12 pieces approximately 1.5 cm by 2.5 cm to accommodate two devices on each piece (Figure 7.1). This scoring step was done before
counterelectrode fabrication to allow the individual pieces to be reworked in case of fabrication issues.

![Figure 7.1: Glass slides scored to accommodate two devices on each piece.](image)

7.5 Mechanical Hole Drilling for Pressure Outlet

The pieces were then aligned to the SU-8 bonding mask and locations were marked for drilling pressure outlet holes (Figure 7.2 a). The glass pieces were covered in tape to prevent cracking during drilling and placed in a micro-abrasive sand blaster, Vaniman Problast-80008 (Figure 7.2 b). This machine shoots air and alumina beads out of a carbide tipped gun. The pressurized mixture drills through the glass to create a small hole for air pressure to be released during device actuation.
Figure 7.2: Mechanical hole drilling began by a) aligning glass slides aligned to Mask #3 and then b) drilling holes with the Vaniman Problast-80008.

7.6 Glass Substrate Cleaning

The glass substrates require cleaning to minimize contamination and improve contact between the sputtered gold and glass substrate. Dust particles can prevent adhesion or create a non-uniform electrode layer. The glass slides were placed in a 250 mL beaker full of electronic grade, 99.7% isopropanol and placed in an ultrasonic cleaner full of water. The isopropanol removes surface particles. The ultrasonic bath uses ultrasound to agitate the solvent and increase the energy of the cleaning reaction. Bubbles formed due to agitation release contaminants from the substrate surface. The isopropanol was then drained and the substrates dried with compressed nitrogen. The nitrogen aids evaporation and prevents further contamination.

7.7 Sputtering Gold

The substrates were taped to a silicon wafer with double sided tape and placed in the Denton V sputtering system. During sputtering, a gold disk (target) given a high negative potential is bombarded with a plasma of positive argon ions. The gold atoms on the surface of the target are ejected by momentum transfer and deposited onto the glass substrate placed on a rotating anode.
Physical vapor deposition (PVD) was performed for 5 minutes at a pressure of 9 mTorr and a power level of 50 watts to achieve a 300 nm gold film (Figure 7.3 b).

Positive photoresist Shipley S1813 was spin coated onto the gold coated glass substrates with a Brewer 200X spin coater. Table 7.2 outlines the spin recipe.
Table 7.2: Spin Recipe for positive photoresist spin coating in Brewer 200X spin coater

<table>
<thead>
<tr>
<th>Step #</th>
<th>Speed (RPM)</th>
<th>Time (s)</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>300</td>
<td>30</td>
<td>Spread primer over wafer surface</td>
</tr>
<tr>
<td>2</td>
<td>3000</td>
<td>30</td>
<td>Planarized primer</td>
</tr>
<tr>
<td>3</td>
<td>3000 to 200</td>
<td>20</td>
<td>Slow wafer, pause during this step to apply resist</td>
</tr>
<tr>
<td>4</td>
<td>200 to 500</td>
<td>10</td>
<td>Spread resist over wafer surface</td>
</tr>
<tr>
<td>5</td>
<td>4000</td>
<td>20</td>
<td>Planarized resist</td>
</tr>
<tr>
<td>6</td>
<td>4000 to 300</td>
<td>5</td>
<td>Slow to stop</td>
</tr>
</tbody>
</table>

The substrates were soft baked at 65°C for 30 seconds, 95°C for 60 seconds, and 65°C for 30 seconds. The 95° soft bake step drives out any remaining solvents. The two 65° steps were done to slowly heat and cool the substrates in an attempt to prevent thermal shock.

After they had cooled, the substrates were removed from the wafer with tweezers and a razor blade. The double sided tape used to attach the substrates to the wafer surface made it extremely difficult to remove the substrates. Many were cracked in the process. Kapton tape should be used instead.

The coated substrates were aligned underneath the mask created for electrode patterning. The Canon PLA-501FA aligner is designed for wafer substrates, so a stacking method was used to expose the glass slides. The substrates were visually aligned between two glass plates with the mask taped on the bottom of the upper plate (Figure 7.4). The plates were separated by four hex huts to keep the resist from sticking to the mask. A dummy wafer was put through the aligner and the substrates were exposed with a light integral of 4.5. The substrates were placed in a Microposit developer (MF-CD-26) at room temperature for three minutes with mild agitation. The regions previously exposed to light were soluble and removed from the surface. The substrates were then rinsed in DI water and dried with N₂.
Figure 7.4: Patterning of positive photoresist to be used as a mask during gold etching. A) shows the stacking method used to put the substrates into the aligner and b) shows the manually aligned substrates.

The substrates were inspected for accurate pattern transfer and then hard baked at 150°C for 60 seconds to polymerize the photoresist mask. They were stepped up and down from 65°C.

The substrates were placed in a small Petri dish with gold etchant (Transene GE-8148) at room temperature for 60 seconds with light agitation. This etchant is a potassium iodine solution (KI/I₂). The iodine reacts with the gold to form gold iodide AuI. KI is added to improve the solubility of AuI. [43] GE-8148 is compatible with both negative and positive resist. The specified etch rate at room temperature is 50Å/sec. [44] Following etching the substrates were thoroughly rinsed with DI water and dried with N₂.

The substrates were placed in a Petri dish of positive resist stripper Microposit Remover 1165 at 60°C for 10 minutes. This step removes the positive resist mask that was previously protecting the gold electrodes, leaving the final electrode pattern. The gold patterning process is shown in Figure 7.5.
Figure 7.5: Process flow chart for gold patterning. a) The substrate was coated with positive resist, aligned to a mask, and exposed to UV light; b) the substrate was developed to remove the soluble photoresist, c) etched with gold etchant, d) and placed in resist stripper to remove the resist mask.

The seventeen patterned glass substrates survived the removal process from the silicon wafer, shown in Figure 7.6.

Figure 7.6: Glass substrates coated with gold and patterned to create electrodes.
7.9 SU-8 Devices Bonding

The 20 μm thick diaphragms and patterned glass slides were bonded with SU-8 to create the device side walls. The bonding procedure followed the steps outlined in Section 4.4, except the diaphragms were patterned with the 30 μm thick 2050 SU-8 and the glass slides coated with the 2007 μm thick SU-8. The glass stacking technique described in Section 7.8 was used to suspend the mask over the devices for alignment and exposure. When the two pieces were placed together for bonding, smaller dark regions appeared than before indicating poor bonding at the interface (Figure 7.7). The devices were placed on a hot plate at 80°C and heavy weights were added in an attempt to promote bonding. A flow chart of the SU-8 side wall fabrication steps is shown in Figure 7.8. Eight devices were fabricated with bonding adequate enough to test the devices. None were fabricated with bonding around the entire perimeter of the device.

![Incomplete Bonding](image)

Figure 7.7: Incomplete bonding of glass to silicon with SU-8
Figure 7.8: Processing steps used to fabricate the device cavity side walls and bond the silicon diaphragms to the glass substrates.  
a) the silicon diaphragms were coated with 2050 SU-8 and aligned with a mask and UV-filter, using hex nuts to prevent the resist coated surface from contacting the mask slide.  
b) The silicon membrane was placed in developer to remove the unexposed SU-8.  
c) the glass substrates patterned with gold electrodes were coated with SU-8 2007 and finally 
d) the two device halves were bonded and exposed with the aligner.
Section 8. Device Testing

8.1 Summary

Three diaphragms were chosen for device testing with a MEMS voltage driver and a Micro Force Displacement System (MFDS): a small device with a side length of 3.0 mm, a medium device with side length of 3.5 mm, and a large device with a side length of 4.5 mm.

8.2 Micro Force Displacement System

The MFDS was created by Evan Cate to measure the change in force (in the micron range) with an applied deflection (in the nm range).[45] Previous research projects have used the surface profilometer for mechanical testing, but the displacement measurements given by the profilometer are only reliable in the micron range. The newly developed MFDS was designed to have a much higher resolution. The MFDS is best summarized in Figure 8.1. The sample is mounted with tape onto the sample stage, which is controlled by two motion controllers. The amplifier amplifies the current signal from a piezoelectric force transducer (Figure 8.2). The signal is read by a voltmeter and data is collected by a computer. A camera is used to align the sample with the micro-prober. The two motion controllers control the x, y, and z axis of the stage.
Figure 8.1: Micro Force Displacement System with labeled components.

The sample was taped onto a glass microscope slide with Kapton tape and the glass slide edge was aligned with the stage edge to square the device with the stage. Copper tape was used to connect the top diaphragm and the gold electrode to two 22-guage lead-wires (Figure 8.2). The wires were taped to the sample stage with masking tape to prevent them from moving during testing.
Figure 8.2: Sample mounted and aligned with a micro-prober controlled by a Piezo transducer.

The two copper wires were connected by alligator clips to the AdvancedMEMS 2-channel high-voltage MEMS Driver.

8.3 MEMS Driver Program

The MEMS driver came with a LabView graphical user interface designed to apply controlled static DC voltage. After installing the necessary software and connecting the driver to a laptop with LabView, the program was unable to recognize the driver. The driver was instead connected to the computer running the MFDS and a new program was created in LabView to run the driver. The user interface is shown in Figure 8.3 and the corresponding block diagram used to create this program is in Appendix II. The program can create a DC or AC voltage from 0V to 300V. For my testing purposes, DC voltage was used. It is important to note that the “enable output” switch will turn on or off the applied voltage, while the “STOP” switch will terminate the entire program.
Figure 8.3: User interface of a LabView program created to control the MEMS driver
8.4 Testing

Three devices were selected for testing with a static DC voltage bias. Each device was positioned using the camera crosshairs (Figure 8.4) and backtrack function on the MFDS software. To use the backtrack function, the camera is first aligned to the center of the device with the cross hairs. Then the “backtrack” button is pushed which moves the MFDS the calibrated distance between the camera and the micro-prober so that the micro-prober is positioned exactly where the center of the cross hairs was previously positioned.

![Figure 8.4: Micro-prober positioning using the MSDF camera and backtrack function. Camera crosshairs were aligned with a) the large device, b) the medium device and c) the small device.](image)

The micro-prober was lowered until it was in contact with the surface of the diaphragm and the z-stage was locked. A voltage was applied using the MEMS Driver program and the force was measured by the transducer for 30 second intervals. 30 second test periods were chosen to allow enough time for data acquisition from an entire set of test runs before hysteresis starts to alter the measurements (which occurs after about seven minutes). The medium diaphragm was tested at 0V, 150V, and 300V three times. The force measurements increase over time, so the measurements were taken in the following order: 0V, 150V, 300V, 0V, 150V, 300V, 0V, 150V, 300V. The small diaphragm was tested six times and the large device was tested ten times in order to gain a better statistical analysis. Figure 8.5 gives the parameters input into the the MFDS program.
Figure 8.5: Parameters input into the MFDS. A stop value of 10V was chosen to prevent the micro-prober from breaking through the diaphragms. 1000 ms was chosen to provide one measurement per second. The step size was brought down to 1 encoder unit (23 nm), this value is not significant because the z-axis was locked.
Section 9. Results

The MFDF graphs voltage as a function of displacement. The displacement was constant, so the data collected graphed voltage as a function of time. The data was manipulated to obtain force measurements as a function of time. These force measurements were examined as a function of the applied voltages over the test period.

9.1: Preliminary Test Results

An initial test using the medium sized diaphragm was performed at 0V and 300V to determine whether or not there was a decrease in the mean force after device actuation. The individual test runs are shown in Figures 9.1 and 9.2. R² values were calculated to see if there was a trend between the increasing force with time that could be subtracted from the test results. As seen by the low R² values, the force measurements did not follow a linear relationship.

![Test 1: Force vs. Time with 0V](image)

Figure 9.1: Test 1: Force vs. Time with 0V plots force measurements of the medium device at rest over three 30 second intervals.
Figure 9.2: Test 1: Force vs. Time with 300V plots force measurements of the medium device after actuation at 300V over three 30 second intervals.

The average force measurements between the two three trials were plotted in Figure 9.3 to compare the change in force between the actuated device (at 300V) and the at-rest device (at 0V). As expected, the force decreased with actuation, indicating that the device had been electrostatically actuated.
Figure 9.3: Test 1: Average Force vs. Time. Averages between the three runs at each voltage were plotted to prove device actuation.

A paired t-Test was performed to determine the statistical difference between the collected data sets at 0V and 300V (Table 9.1). The Pearson correlation is about equal to 0, indicating that there is no linear correlation between the two variables. The p-value is the probability of obtaining a data point greater than or equal to the results obtained in the test data, given that the null hypothesis $H_0$ is true. The null hypothesis $H_0$ is that the two means from the separate data sets are equal ($H_0: \mu_1=\mu_2$). If the p-value is less than the confidence coefficient $\alpha_c$, then the null hypothesis can be rejected. A common confidence coefficient of $\alpha_c=0.05$ gives a 95% confidence interval. The p-values is less than .05, indicating that the means are statistically different with 95% confidence ($H_0$ can be rejected). [46] [47]
A Single Factor ANOVA (analysis of variance) test was performed to detect the strength of the “signal”, a statistical variance between the two groups, compared to the “noise”, statistical variance created by the individual groups. If the difference between groups is greater than the differences within groups, there is a strong “signal-to-noise”. The p-value given by the ANOVA test is less than 0.05; the null hypothesis is rejected with 95% confidence.[46] The sum of squares SS shows the total variation between groups and within groups. SS between the groups is greater than within groups, indicating a strong “signal-to-noise”. Further, the null hypothesis $H_0: \mu_1 = \mu_2$ can be rejected if $F > F_{\text{crit}}$. Table 9.2 gives results for Test #1. The null hypothesis is rejected because $F > F_{\text{crit}}$ and the p-value is low, and the SS (variance) between groups is greater than within groups, indicating good signal to noise.

Table 9.2: ANOVA Test for Test #1

<table>
<thead>
<tr>
<th>Source of Variation</th>
<th>SS</th>
<th>F</th>
<th>P-value</th>
<th>F crit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Between Groups</td>
<td>9.552009</td>
<td>660.318</td>
<td>2.2E-33</td>
<td>4.006873</td>
</tr>
<tr>
<td>Within Groups</td>
<td>0.839015</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td>10.39102</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
9.2 Test Results: Medium Device

A second test was performed with the medium device at 0V, 150V, and 300V for three 30 second time periods. The individual test results are shown in Figures 9.4, 9.5, and 9.6. The $R^2$ values show a poor linear trend, but improved from the preliminary test.

![Test 2: Force vs. Time with 0V](image)

Figure 9.4: Test 2: Force vs. Time with 0V plots force measurements of the medium device at rest over three 30 second intervals.
Figure 9.5: Test 2: Force vs. Time with 150V plots force measurements of the medium device at 150V over three 30 second intervals.

Figure 9.6: Test 2: Force vs. Time with 300V plots force measurements of the medium device at 300V over three 30 second intervals.

The average force measurements between the three data sets were plotted in Figure 9.7 to compare the change in force between the device actuated at 300V, 150V, and at rest. The
observed force decreases with actuation, but overlapping between the 150V and 0V requires statistical analysis to prove a statistically significant difference between the two.

![Test 2: Average Force vs. Time](image)

Figure 9.7: Test 2: Average Force vs. Time plotted for three voltages, 0V, 150V, and 300V.

Two two paired t-Test was performed to determine the statistical differences between the three forces (Table 9.3 and 9.4). The Pearson correlations are about equal to 1, indicating that there is a positive linear correlation between the two variables in both cases. The p-values are less than 0.05, proving a statistically significant difference between the data sets with a 95% confidence interval. The mean force decreases with higher actuation.

Table 9.3: Paired Two Sample t-Test for Means between 0V and 150V for Test #2

<table>
<thead>
<tr>
<th></th>
<th>0V average</th>
<th>150V average</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mean</td>
<td>14.61762154</td>
<td>14.36805091</td>
</tr>
<tr>
<td>Variance</td>
<td>0.310038016</td>
<td>0.102993886</td>
</tr>
<tr>
<td>Observations</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>Pearson Correlation</td>
<td>0.925439324</td>
<td></td>
</tr>
<tr>
<td>P(T&lt;=t) one-tail</td>
<td>2.43489E-05</td>
<td></td>
</tr>
<tr>
<td>P(T&lt;=t) two-tail</td>
<td>4.86977E-05</td>
<td></td>
</tr>
</tbody>
</table>
Table 9.4: Paired Two Sample t-Test for Means between 150V and 300V for Test #2

<table>
<thead>
<tr>
<th></th>
<th>150V average</th>
<th>300V average</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mean</td>
<td>14.36805091</td>
<td>14.09423224</td>
</tr>
<tr>
<td>Variance</td>
<td>0.102993886</td>
<td>0.119240916</td>
</tr>
<tr>
<td>Observations</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>Pearson Correlation</td>
<td>0.937987657</td>
<td></td>
</tr>
<tr>
<td>P(T&lt;=t) one-tail</td>
<td>1.59098E-13</td>
<td></td>
</tr>
<tr>
<td>P(T&lt;=t) two-tail</td>
<td>3.18196E-13</td>
<td></td>
</tr>
</tbody>
</table>

Two ANOVA single factor tests were performed to further examine statistically significant differences between the data sets (Tables 9.5 and 9.6). The p-values are less than 0.05, indicating a rejection of the null hypothesis with 95% confidence. The null hypothesis is further rejected because F>F crit in both cases. The SS variance is lower between groups than within groups. These tests prove a statistically significant decrease in force with device actuation at higher voltages.

Table 9.5: ANOVA Test between 0V and 150V for Test #2

<table>
<thead>
<tr>
<th>Source of Variation</th>
<th>SS</th>
<th>F</th>
<th>P-value</th>
<th>F crit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Between Groups</td>
<td>0.934282</td>
<td>4.524021</td>
<td>0.037687</td>
<td>4.006873</td>
</tr>
<tr>
<td>Within Groups</td>
<td>11.97793</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td>12.91221</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 9.6: ANOVA Test between 150V and 300V for Test #2

<table>
<thead>
<tr>
<th>Source of Variation</th>
<th>SS</th>
<th>F</th>
<th>P-value</th>
<th>F crit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Between Groups</td>
<td>1.12465</td>
<td>10.12128</td>
<td>0.002355</td>
<td>4.006873</td>
</tr>
<tr>
<td>Within Groups</td>
<td>6.444809</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td>7.569459</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
9.3 Test Results: Small Device

The third test was taken of a small diaphragm with five iterations of 0V, 150V, and 300V. The voltage change was alternated to compensate for the increase in voltage with time. Raw data is given in Appendix V. The average forces were plotted against each other in Figure 9.8 for comparison. As seen, the force increased with applied voltage. The average force at 300V is 14.355 mg, which is higher than the average force at 150V, 14.325 mg and much higher than the average force for 0V. This is not characteristic of electrostatic actuation; the device is not functioning.

![Test 3: Average Force vs. Time](image)

Figure 9.8: Test 3: Average Force vs. Time for the small device at rest, actuated at 150V, and actuated at 300V. The force increases with increasing voltage, therefore the device is not actuating.

9.4: Test Results: Large Device

The fourth test characterized a large diaphragm at 0V, 150V, and 300V with 10 testing iterations. The individual test runs are shown in Appendix V. The average forces were plotted as a function of time for the ten runs (Figure 9.9). The device was not actuated at 150V (shown by the increase in average force), but was actuated at 300V (shown by the decrease in average force).
Figure 9.9: Test 4: Average Force vs. Time of large device at rest (0V), actuated at 150V, and actuated at 300V. The force decreases with an applied 300V, but increases slightly with 150V.

A paired t-Test (Table 9.7) was performed to determine the statistical difference between the device at rest and 300V actuation. The Pearson correlation shows a moderately linear correlation between the two variables. The p-values are less than 0.05, indicating a statistically significant difference between the two data sets with 95% confidence.

Table 9.7: Paired t-Test between 150V and 300V for Test #4

<table>
<thead>
<tr>
<th></th>
<th>150V Averages</th>
<th>300V Averages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mean</td>
<td>21.27290251</td>
<td>18.47668261</td>
</tr>
<tr>
<td>Variance</td>
<td>0.043855713</td>
<td>0.191751512</td>
</tr>
<tr>
<td>Observations</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>Pearson Correlation</td>
<td>0.698689357</td>
<td></td>
</tr>
<tr>
<td>P(T&lt;=t) one-tail</td>
<td>3.75642E-29</td>
<td></td>
</tr>
<tr>
<td>P(T&lt;=t) two-tail</td>
<td>7.51284E-29</td>
<td></td>
</tr>
</tbody>
</table>

A single factor ANOVA test was performed to further prove the statistical difference between the two data sets (Table 9.8). The SS between groups is greater than within groups, showing greater variance between the data sets than within them (good signal to noise). The F>F crit and P-
value < 0.05, so the null hypothesis is rejected. The two data sets are statistically different with a 95% confidence interval.

Table 9.8: Single Factor ANOVA test between 150V and 300V for Test #4

<table>
<thead>
<tr>
<th>Source of Variation</th>
<th>SS</th>
<th>F</th>
<th>P-value</th>
<th>F crit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Between Groups</td>
<td>117.2827</td>
<td>995.578</td>
<td>3.25E-38</td>
<td>4.006873</td>
</tr>
<tr>
<td>Within Groups</td>
<td>6.83261</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td>124.1153</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

9.5 Conclusions from Test Results

The medium device was successfully actuated at both 150 V and 300 V. The small device was not actuated at either voltage. The large device was actuated at 300 V, but not at 150 V.
Section 10. Discussion of Characterization Techniques

10.1 Comparison of calculations, modeling, and test results

The achieved deflection can be found by using Equation 2.29 and rearranging to solve for the deflection, $x$:

$$F_{elec} = \frac{Eh^3x}{0.01303a^2}$$  \hspace{1cm} (10.1)

The change in deflection can be estimated by this equation using the average forces from each test to determine the difference in force between the device at rest and actuated. This assumes that the difference in force is due solely to the electrostatic force.

The small device showed no actuation, despite a 0.67 μm deflection predicted by COMSOL modeling.

The mean force of the medium device at 300V was 14.09 mg. At 0V it was 14.62 (data taken from Test #2). This gives a change in force of .53 mg, or 5.2 μN. Given the side length of 3.5 mm, the total calculated deflection is 0.7 nm, far below the modeled deflection of 1.3 microns estimated by COMSOL modeling (Appendix IV).

The mean force of the large device at 300V was 18.8 mg, and at rest 20.66 mg. The change in force is 1.89 mg or 18 μN. Using Equation 10.1, the achieved deflection was 4 nm, far below the modeled deflection of 3.8 microns estimated by COMSOL modeling (Appendix IV).

The model used to derive Equation 10.1 used estimations that do not accurately represent the fabricated devices. The COMSOL models assumed perfectly fabricated devices.

10.2 Influence of Fabrication Procedures on Devices

The modeled and calculated deflection values assumed perfect materials and geometries. In reality, the materials had accumulated stresses during processing conditions and the fabrication tolerances were large. Stresses in the diaphragms could increase the diaphragm stiffness, leading to a lowered deflection with the applied electrostatic force. The designed side length $a$ is
larger than the actual side length due to anisotropic etching. A sensitivity analysis was done to determine the effect of each variable on the calculated deflection. The partial derivative with respect to each variable was taken of Equation 10.1:

\[
\frac{\partial x}{\partial E} = \frac{-0.01303a^2F}{E^2h^3} = -1.47 \times 10^{-15} \tag{10.2}
\]

\[
\frac{\partial x}{\partial h} = \frac{-3 \times 0.01303a^2F}{Eh^4} = -1.72 \times 10^{-4} \tag{10.3}
\]

\[
\frac{\partial x}{\partial a} = \frac{2 \times 0.01303aF}{Eh^3} = 5.08 \times 10^{-7} \tag{10.4}
\]

This shows that the thickness of the diaphragm has the biggest effect on the calculated displacement, while the young’s modulus has the least effect. The side length of the diaphragm has a large effect on the distance but would actually increase the deflection distance, so this does not explain the extremely low calculated distance values. The calculations and COMSOL modeling also do not account for the 10 micron layer of SU-8 between the two electrodes. However, polymers typically have a higher permittivity which would increase the electrostatic force and promote deflection.

10.3 Influence of Test Equipment on Test Results

The micro force displacement system has been recently created to test MEMS devices in our lab. The measured forces with a steady deflection was variable over time, and changed significantly with people moving around the lab or building. Vibrations during operation contribute to noise and changes in the data collected by the force transducer. The system would be improved with isolation and a higher resolution analytical balance. This piece of equipment is not fully characterized, so the force measurements are probably not accurate. Also, the voltage applied to the device could be less than the voltage measured by the multimeter due to the resistance in the lead wires, alligator clips, and copper conductive tape.
Section 11. Conclusions and Continuation of the Project

11.1 Summary

A theoretical analysis of membrane mechanics and finite element analysis provided a device design that could be fabricated and characterized in our lab. Device design began with a study of diaphragm mechanics to predict the membrane displacement based on the pressure induced by electrostatic actuation. Materials and dimensions were selected based on our lab’s fabrication capabilities and available materials. COMSOL models were created to provide a better estimation of device actuation. Eight devices were fabricated but none of them had sealed cavities. Finally a test set-up was created for mechanical testing.

11.2 Fabrication Processes Improved

This thesis advanced the research of the fabrication processes available in our lab. Appropriate spin-recipes and light integrals were found for SPR-220 and PMMA that did not previously exist. A method of patterning PMMA with a SEM was found. Experimentation with KOH and 5% TMAH showed processing parameters that were not successful. I developed a standard operating procedure for the condenser chamber and a cleaning method to remove metal contaminants from the surface of silicon. I proved the use of SOI wafers in the fabrication of thin membranes. These processing notes can be used for any project in our lab.

I also developed a test set-up for mechanically testing actuated MEMS devices with the MEMS driver and micro-force displacement system. This can be used to test micromirrors, electrostatically actuated pumps, or any MEMS sensing device. The MEMS driver can be used to actuate devices with a DC or AC voltage.

11.3 Recommendations for Improvement

Research should be done to improve silicon deep etching by characterizing the 5% TMAH etchant. A stable etch rate is needed to achieve predictable etching and prevent over etching. The processing parameters used to fabricate the diaphragm should be experimented with in an
attempt to reduce the high temperatures that contribute to thermal cycling. This would reduce the degree of warping in the thin diaphragms. The devices would be improved with thinner membranes or side-walls to allow for a reduced actuation voltage and device size. The deflection needs to be maximized to create a pressure wave large enough to produce a sound wave. The test set-up can be further characterized to determine the effects of vibration on the transducer measurements to reduce noise associated with data acquisition.

11.4 Project Continuation

This project can be continued for the development of a microspeaker, pressure sensor, or microfluidics pump. Improvements can be made to the fabrication process and test set-up. This thesis proved that diaphragms can be electrostatically actuated at very small distances. Eventually, this project could result in the fabrication of a functioning device, but the process steps must be improved.

For the device to be tested as a microspeaker, an AC voltage should be applied with the MEMS driver. The LabView program was created to allow for AC voltage and can be easily applied by clicking the "AC/DC" button on the program interface.
References


5. Lecture#7. Informally published manuscript, Yale EAS, Retrieved from


32. Xu071918.30-cyclotene advanced electronic resin technical processing guide for flat panel


Appendix I: Initial COMSOL Modeling of 10 μm Thick Diaphragms at 200V

Total Surface Displacement (microns)

Parameters:
- diaphragm side length: 2.5mm
- diaphragm thickness: 10 microns
- gap thickness: 40 microns
- applied voltage: 200V

Total Surface Displacement (microns)

Parameters:
- diaphragm side length: 3 mm
- diaphragm thickness: 10 microns
- gap thickness: 40 microns
- applied voltage: 200V
Total Surface Displacement (microns)

Parameters:
- diaphragm side length: 3.5 mm
- diaphragm thickness: 10 microns
- gap thickness: 40 microns
- applied voltage: 200V

Total Surface Displacement (microns)

Parameters:
- diaphragm side length: 4 mm
- diaphragm thickness: 10 microns
- gap thickness: 40 microns
- applied voltage: 200V
Total Surface Displacement (microns)

Parameters:
diaphragm side length: 4.5 mm
diaphragm thickness: 10 microns
gap thickness: 40 microns
applied voltage: 200V

Total Surface Displacement (microns)

Parameters:
diaphragm side length: 5 mm
diaphragm thickness: 10 microns
gap thickness: 40 microns
applied voltage: 200V
Appendix II: Lab View Program Block Diagram
Appendix III: Modified COMSOL Models with 20 μm Thickness and 150V

**Total Surface Displacement (microns)**

Parameters:
- Diaphragm side length: 2.5 mm
- Diaphragm thickness: 20 microns
- Gap thickness: 40 microns
- Applied voltage: 150V

**Total Surface Displacement (microns)**

Parameters:
- Diaphragm side length: 3 mm
- Diaphragm thickness: 20 microns
- Gap thickness: 40 microns
- Applied voltage: 150V
Total Surface Displacement (microns)

Parameters:
- diaphragm side length: 3.5 mm
- diaphragm thickness: 20 microns
- gap thickness: 40 microns
- applied voltage: 150V

Total Surface Displacement (microns)

Parameters:
- diaphragm side length: 4 mm
- diaphragm thickness: 20 microns
- gap thickness: 40 microns
- applied voltage: 150V
Total Surface Displacement (microns)

Parameters:
diaphragm side length: 4.5 mm
diaphragm thickness: 20 microns
gap thickness: 40 microns
applied voltage: 150V

Total Surface Displacement (microns)

Parameters:
diaphragm side length: 5 mm
diaphragm thickness: 20 microns
gap thickness: 40 microns
applied voltage: 150 microns
Appendix IV: Modified COMSOL Models with 20 μm Thickness and 300V

Total Surface Displacement (microns)

Parameters:
diaphragm side length: 2.5 mm
diaphragm thickness: 20 microns
gap thickness: 40 microns
applied voltage: 300V

Total Surface Displacement (microns)

Parameters:
diaphragm side length: 3 mm
diaphragm thickness: 20 microns
gap thickness: 40 microns
applied voltage: 300V
Parameters:
diaphragm side length: 3.5 mm
diaphragm thickness: 20 microns
gap thickness: 40 microns
applied voltage: 300V

Parameters:
diaphragm side length: 4 mm
diaphragm thickness: 20 microns
gap thickness: 40 microns
applied voltage: 300V
Total Surface Displacement (microns)

Parameters:
- diaphragm side length: 4.5 mm
- diaphragm thickness: 20 microns
- gap thickness: 40 microns
- applied voltage: 300V

Total Surface Displacement (microns)

Parameters:
- diaphragm side length: 5 mm
- diaphragm thickness: 20 microns
- gap thickness: 40 microns
- applied voltage: 300V
Appendix V: Test Data

Test 3: Force vs. Time with 0V

Test 3: Force vs. Time with 150V
Test 3: Force vs. Time with 300V

Test 4: Force vs. Time with 0V