Development of a CubeSat Instrument for
Microgravity Particle Damper Performance Analysis

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Abstract

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Spacecraft pointing accuracy and structural longevity requirements often necessitate auxiliary vibration dissipation mechanisms. However, temperature sensitivity and material degradation limit the effectiveness of traditional damping techniques in space. Robust particle damping technology offers a potential solution, driving the need for microgravity characterization. A 1U cubesat satellite presents a low cost, low risk platform for the acquisition of data needed for this evaluation, but severely restricts available mass, volume, power and bandwidth resources. This paper details the development of an instrument subject to these constraints that is capable of capturing high resolution frequency response measurements of highly nonlinear particle damper dynamics.
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Table of Contents

LIST OF FIGURES ......................................................................................................................... IX
LIST OF TABLES ............................................................................................................................. XIV
LIST OF EQUATIONS ........................................................................................................................ XV
SCOPE OF WORK ........................................................................................................................... 1

1 CUBESAT SATELLITES ......................................................................................................................... 3
  1.0 THE CUBESat STANDARD ........................................................................................................ 3
  1.1 CUBEsats TODAY & TOMORROW ....................................................................................... 5
  1.2 CUBEsats AT CAL POLY ...................................................................................................... 7
  1.3 INTRODUCTION TO THE CP7 MISSION ........................................................................ 7

2 PARTICLE DAMPING ........................................................................................................................ 9
  2.0 AN INTRODUCTION TO PARTICLE DAMPING .................................................................... 9
     2.0.0 Impact Damping Origins ............................................................................................... 9
     2.0.1 Particle Damping Overview ......................................................................................... 10
     2.0.2 Particle Damping Analysis ......................................................................................... 11
  2.1 PREDICTING MICROGRAVITY PARTICLE DAMPER DYNAMICS ........................................ 12
  2.2 SPACE SYSTEM MECHANICAL DAMPING REQUIREMENTS .................................................. 15
     2.2.0 Modal Attenuation ....................................................................................................... 15
     2.2.1 Jitter Reduction .......................................................................................................... 16
  2.3 THE POTENTIAL OF PARTICLE DAMPING WITHIN SPACE SYSTEMS .................................. 16
     2.3.0 Comparison to Active Damping Approaches ............................................................. 17
     2.3.1 Comparison to Traditional Passive Damping Approaches ........................................ 17
     2.3.2 Particle Damping Compared to Viscoelastic Damping ................................................ 18
     2.3.3 Space System Obstacles ............................................................................................ 19

3 SYSTEM REQUIREMENTS .............................................................................................................. 20
  3.0 REQUIREMENT ORIGINS ........................................................................................................ 20
  3.1 SCIENCE REQUIREMENTS ..................................................................................................... 20
     3.1.0 Baseline Mechanical System ..................................................................................... 20
     3.1.1 System Input & Output ............................................................................................... 21
  3.2 CUBEsats PLATFORM REQUIREMENTS ............................................................................ 22

4 HIGH LEVEL DESIGN ..................................................................................................................... 24
  4.0 PRIMARY MECHANICAL SYSTEM .......................................................................................... 24
  4.1 PARTICLE DAMPER ................................................................................................................. 25
  4.2 CUBEsats STRUCTURE .......................................................................................................... 26
  4.3 CANTILEVER BEAM ACTUATORS .......................................................................................... 29
     4.3.0 Actuator Requirements ............................................................................................... 29
     4.3.1 Actuator Selection ....................................................................................................... 29
     4.3.2 Piezoelectric Ceramic Selection .................................................................................. 30
  4.4 CANTILEVER BEAM LOCKING MECHANISM ACTUATORS .................................................. 31
     4.4.0 Actuator Requirements ............................................................................................... 31
     4.4.1 Actuator Selection ....................................................................................................... 32
     4.4.2 Locking Mechanism Overview ................................................................................... 33
  4.5 SENSOR SELECTION CRITERIA ............................................................................................... 34
     4.5.0 Criteria Overview ......................................................................................................... 34
     4.5.1 Relative Accuracy ....................................................................................................... 35
     4.5.2 Absolute Accuracy ...................................................................................................... 36
     4.5.2 Measurement Noise .................................................................................................... 37
  4.6 SENSOR SELECTION ................................................................................................................. 38
# EXPERIMENT DATA ANALYSIS

- Initial Technology Considerations .................................................. 38
- Ratiometric Hall Sensor Consideration ........................................... 38
- Accelerometer Selection ................................................................. 42

# LOW LEVEL DESIGN ........................................................................ 52

## SENSOR MODULE ........................................................................... 52
- Sensor Module Overview ................................................................. 52
- Power Rails ..................................................................................... 53
- Analog Front End ............................................................................ 57
- Peak Detectors ............................................................................... 62
- Digital Circuitry ............................................................................... 65
- Calibration ..................................................................................... 69

## PIEZOELECTRIC ACTUATOR DRIVER ........................................... 70
- System Overview ............................................................................ 70
- Excitation Signal Generation ......................................................... 72
- High Voltage Amplification ............................................................ 77
- Output Measurement ....................................................................... 81
- Piezoelectric Actuator Multiplexing ............................................... 82
- Calibration ...................................................................................... 83

## FREQUENCY & PHASE DETECTION ............................................. 84
- System Overview ............................................................................ 84
- Trigger Circuitry ............................................................................. 86
- Counter Circuitry ............................................................................ 90
- Digital Interface ............................................................................. 92
- Calibration ...................................................................................... 93

## PAYLOAD COMMAND & DATA HANDLING ................................ 94
- System Overview ............................................................................ 94
- Microcontroller and Supporting Peripherals .................................. 97
- Avionics Interface .......................................................................... 101
- Power Regulation .......................................................................... 103
- SMA Actuator Drivers ................................................................... 105

## INSTRUMENT CONTROL ALGORITHMS .................................. 106
- Wait and Read Algorithm ............................................................... 107
- Sensor Module Automatic Gain Control Algorithm ...................... 108
- Sensor Module Steady State Detection Algorithm ......................... 112
- Beam Locking Mechanism Control .............................................. 118
- Phase and Frequency Measurement Procedure ............................ 118

# EXPERIMENT DATA ANALYSIS ...................................................... 121

## DATA POST PROCESSING ............................................................. 121
- Basic Data Analysis ...................................................................... 121
- Advanced Data Analysis ............................................................... 122

# CONCLUSION .................................................................................. 126

## MISSION STATUS ........................................................................... 126

## REMAINING WORK ....................................................................... 127
- Complete in the Loop System Testing ........................................... 127
- Environmental Testing ................................................................. 127
- Fault Testing .................................................................................. 128
- Operation Plan Definition ............................................................ 128

REFERENCES ..................................................................................... 129
APPENDIX A: PIEZOELECTRIC FORCE-VOLTAGE RELATION ................................................................. 134
APPENDIX B: SENSOR MODULE SCHEMATIC ................................................................................. 135
APPENDIX D: PAYLOAD COMMAND & DATA HANDLING SCHEMATIC ........................................ 148
APPENDIX E: AUTOMATIC GAIN CONTROL LOOK UP TABLE ....................................................... 155
APPENDIX F: FREQUENCY DETECTOR OPERATION INSTRUCTIONS .............................................. 156
APPENDIX G: DATA PROCESSING MATLAB SCRIPT ................................................................. 158
List of Figures

Figure 1 - A photograph of CP6, a one unit, or 1U, cubesat built by Cal Poly’s PolySat program. ............... 4
Figure 2 - A rendering of the P-POD Mark II. The exploded view, right, exposes the spring plunger mechanism used to expel internal cubesat(s) after the door is released......................................................... 4
Figure 3 - A rendering of an impact damper attached to a second order spring dashpot model. Here, a ball bearing is constrained within a cylindrical cavity................................................................. 9
Figure 4 - A rendering of a particle damper. While shown attached to a second order spring dashpot model, particle damping has been demonstrated to be effective for multimodal, multidirectional vibration attenuation......................................................................................... 10
Figure 5 - A photograph of the International Space Station. The low mass, cantilevered structural components, typical of spacecraft configurations, present concerns related to destructive resonant modes. Photo Credit: NASA JSC [39] .......................................................................................................................... 16
Figure 6 - An annotated photograph of a cantilever beam within CP7’s payload. An aluminum cantilever beam serving as a baseline mechanical system for particle damper evaluation is machined as a single piece along the diagonal of a structural cross section. A stainless steel tip mass containing a particle damper is screwed onto the free end of the beam. Three such beams are stacked on top of each other within CP7’s payload..................................................................................................................... 25
Figure 7 - A photograph of the tip mass particle damper cavity used within CP7. This stainless steel piece bolts to the cantilever beam free end, serving to increase the mechanical system’s effective mass to a favorable level. Fine tungsten powder (not shown) fills the cavity, forming the particle damper........................................................................................................................................... 26
Figure 8 - A computer rendering of CP7. Three similar structural crosspieces, shown in red, make up the payload mechanical system. This configuration is designed to control the physical experiment variables within the constraints of a cubesat........................................................................................................... 28
Figure 9 - A dual view photograph of the assembled CP7 structure. Individual cross sections are machined out of aluminum, anodized and joined together with alignment pins and bolts. The completed satellite will include side panels housing solar cells and magnetorquers affixed to each face................................................................................................................................................... 28
Figure 10 - A photograph of the piezoelectric actuator selected for actuating the cantilever beams within CP7’s payload. The actuator consists of rectangular PZT5A3 ceramic plated with silver electrodes on each face. The dimensions of the unit are 1.75” long by .50” wide by .10” thick. ...................................... 31
Figure 11 - An annotated photograph of an SMA actuator used within CP7’s payload. Three such modified Dash-4 actuators are used to lock the three cantilever beams, a fourth operates as a release mechanism such that each beam can be selectively locked and unlocked through a sequence of operations ........................................................................................................................................... 33
Figure 12 - An annotated photo of the CP7 beam locking mechanism. In the locked state the lever arm deflects the cantilever beam such that mechanical coupling to adjacent beams is reduced. In the unlocked state (shown) the cantilever beam is free to oscillate. The lever clasp holds the lever arm in either state without the need for continuous actuation power........................................................................... 34
Figure 13 - Estimates of damped natural frequency and 3dB frequencies are invariant to a constant offset error term or a scaling error term. Therefore bandwidth, damping factor and quality factor performance metrics are insensitive to linear measurement errors.......................................................................................... 36
Figure 14 - A rendering of a Hall Effect sensor based displacement measurement configuration. The blue arrows designate the magnet polarization and hall sensor sensitivity. As the cantilever beam oscillates the incident magnetic field varies linearly, the hall sensor transduces this into a voltage proportionate to the beam’s displacement........................................................................................................ 39
Figure 15 - An annotated photograph of the interferometer used to calibrate the Hall sensor. Hall sensor output is compared to the laser fringe pattern to measure sensor linearity and determine the voltage over displacement scale factor................................................................................................................................. 40
Figure 16 - A plot of displacement over Hall sensor output. Data points are generated from a Michelson interferometer and a test beam. The slope of a line fit to this plot demonstrates a 300 nanometer per millivolt linear sensitivity over a 400 micrometer full scale range......................................................................................... 41
Figure 17 - A photograph of the accelerometer selected for CP7 instrumentation. This analog output MEMS device offers sensitivity in the µg range over two axes............................................................................................................ 45
Figure 18 - A representation of a sampled random output signal. A Discrete Fourier Transform of these data points gives the system's frequency response. ................................................................. 46

Figure 19 - A representation of a sinusoidal waveform overlaid with a sampled peak detector. This data acquisition process performed over a sine dwell gives the means to directly measure a system's magnitude frequency response. ........................................................................................................ 47

Figure 20 - An annotated photograph of the Sensor Module. This PCB is designed to mount to the tip of a cantilever beam. An accelerometer and supporting circuitry is capable of directly measuring the system's magnitude response for a given input function. The board fits within a 1.25” square geometry. ................................................................................................................................. 57

Figure 21 - Schematic of Sensor Module power regulators. Separate LDO’s provide isolated analog and digital power rails. U9, a precision low drift voltage reference provides a stable output onto which the accelerometer output can be referenced. ....................................................................................... 58

Figure 22 - Layout of Sensor Module power planes. Separate analog and digital planes help isolate digital switching noise from the sensitive analog signal chain. A third power plane sources the accelerometer reference voltage. ......................................................................................................................... 59

Figure 23 - Layout of Sensor Module ground planes. Separate analog and digital planes help isolate digital switching noise from the sensitive analog signal chain. Each plane is shunted to the header’s ground through zero ohm resistors, providing a single point return path. ......................... 60

Figure 24 - Schematic of the Sensor Module offset voltage source. A buffered resistor divider produces a 2.2V reference used to offset the accelerometer output. This offset is referred to an A/D converter’s differential input, reducing the systems sensitivity to component temperature drift................. 61

Figure 25 - Schematic of the first stage of the Sensor Module analog front end. The accelerometer output is filtered through a first order filter formed by the device’s resistive output and external capacitors. Analog switch, U1, selects the accelerometer axis to measure. ........................................ 62

Figure 26 - Schematic of the second stage of the Sensor Module analog front end. The filtered accelerometer output is buffered by U2B. The signal is then AC coupled and referred to a known DC offset provided by U2A. Instrumentation amplifier U10 and digital potentiometer form a variable gain stage capable of amplifying the signal between a factor of 1 and 257. ......................... 63

Figure 27 - Schematic of the final stage of the Sensor Module analog front end. The amplified signal is inverted, enabling valley detection in a single supply system. ...................................................... 64

Figure 28 - Schematic of Sensor Module Schmitt trigger. A comparator with added hysteresis is used to convert the accelerometer’s sinusoidal waveform into a square wave that lends itself to frequency and phase measurements. ................................................................................................. 65

Figure 29 - Schematic of Sensor Module peak detector. This circuit captures and holds the highest value of the amplified accelerometer signal. MOSFET’s Q2(1,2) provide the means in which the peak detector can be reset. An identical circuit block captures the peak of the inverted accelerometer signal, forming a valley detector. ................................................................. 66

Figure 30 - Schematic of Sensor Module digital interface. An I²C GPIO expander, U5, provides the means in which the peak detectors can be reset among other Sensor Module functionality. ...................................................... 67

Figure 31 - Schematic of Sensor Module analog to digital converters. A dual channel differential input A/D, U6, provides high resolution conversion of peak detector output. Additional A/D’s including temperature sensor U7 provide the means to confirm proper Sensor Module operation. ...................................................... 68

Figure 32 - Annotated photograph of the payload electronics stack. The top board houses the Piezoelectric Actuator Driver circuitry. The lower board houses the payload Command and Data Handling PCB. This configuration helps isolate high and low voltage circuitry. The combined stack height is approximately .61”; the larger PC&DH PCB measures 3.25” on its side................. 69

Figure 33 - Annotated photograph of the reverse side of the Piezoelectric Actuator Driver PCB. This square PCB measures 2.6875” on its side. The high voltage DC-DC converters protrude .5”. .................... 70

Figure 34 - Schematic of DDS signal generator used in the Piezo Actuator Driver. DDS U8 generates a high resolution sine wave approximation based on clock U11. ................................................................. 71

Figure 35 - Schematic of DDS output buffer. This circuit buffers and AC couples the DDS output, which is incident on U7A’s input. ...................................................................................... 72

Figure 36 - Schematic of DDS output filter. A 4th order cascade of Sallen-Key filters with a 1kHz cut off frequency performs anti-imaging filtering of the DDS sampled sine wave approximation. .......................... 73

Figure 37 - Schematic of signal attenuation stage. A resistor divider attenuates the filtered DDS output which is incident on R5. Analog switch U4 enables or disable the resistor divider to toggle
between normal and low voltage modes................................................................. 76

Figure 38 - Schematic of signal fine gain stage. The filtered signal is applied to a cascade of gain stages, a fixed 1.5 amplification and a variable gain stage formed around digital potentiometer U1. Together this cascade achieves gains between 3 and 16 over 256....................................................... 77

Figure 39 - Schematic of high voltage converters. Two high voltage DC/DC converters supply high voltage rails needed for the high voltage amplification stage. The magnitude of this voltage is proportional to the input, up to +/-400V for a 5V input................................................................. 78

Figure 40 - Schematic of high voltage gain stage. High voltage Op-Amp U25 configured as an inverting amplifier amplifies the sine wave up to 740Vpp in conjunction with the variable input resistor course gain stage........................................................................................................ 79

Figure 41 - Schematic of coarse gain stage. Analog switch U5 shorts segments of the resistor cascade to alter the input resistance value and gain of the high voltage amplifier......................................................... 80

Figure 42 - Plot of input signal dynamic range. Through the selection of fine and course gain values within either the low or normal voltage mode allows the input signal to be amplified between 5Vpp to 740Vpp within 2.66%................................................................. 81

Figure 43 - Schematic of output voltage divider. A high impedance resistor divider and buffer produce a divided output that can be measured using low voltage electronics .................................................. 82

Figure 44 - Schematic of high voltage multiplexer. Opto-isolaters controlled by an I2C GPIO expander route the high voltage input signal to one of three piezoelectric actuators........................................... 83

Figure 45 - Schematic of frequency signal multiplexer. Control lines select the Sensor Module waveform to feed through. 5V waveforms are level converted to 3.3V suitable for the PC&DH logic........ 87

Figure 46 - Schematic of input frequency counter trigger block. This circuitry generates a single pulse of duration proportionate to the input frequency period; this is later used to gate in a high frequency clock to a counter................................................................. 89

Figure 47 - Schematic of phase counter trigger block. This circuitry generates a single pulse of duration equal to delay between rising edges of the input and output frequency; this is later used to gate in a high frequency clock to a counter................................................................. 90

Figure 48 - Schematic of counter circuitry. A buffered 32 MHz clock is gated to three 32-bit counters through the logic generated from the trigger circuit blocks. The resulting count can be used to determine frequency and phase shift of the input and output waveforms................................. 91

Figure 49 - Schematic of counter circuitry digital interface. Two 16-bit I2C GPIO expanders are used to read in the counter registers as well as control the various counter parameters........................................... 92

Figure 50 - Annotated photograph of the PC&DH PCB, top layer. The 3.25” square board houses the slightly smaller Piezo Driver PCB. Ribbon cable headers along the perimeter are exposed for easy access. A rectangular cut out allows the high voltage DC-DC converters to pass through to minimize stack height......................................................................................... 96

Figure 51 - Annotated photograph of the PC&DH PCB, bottom layer. The high voltage DC-DC converters from the mated Piezo Driver Board can be seen protruding from the cut out........................................ 97

Figure 52 - Schematic of microcontroller on PC&DH. An 8-bit microcontroller configured for a 25 MHz clock rate controls the payload operations and communicates with the satellite avionics...................... 98

Figure 53 - Schematic of I2C multiplexer. By multiplexing the I2C lines the payload microcontroller can address identical components on the Sensor Modules and Piezo Driver. Separate sets of pull up resistors level convert the I2C logic................................................................. 99

Figure 54 - Schematic of payload nonvolatile memory. Four I2C EEPROM IC’s are daisy chained for a total capacity of 4-Mbits. A switch, U31 multiplexes the I2C lines so that the payload and avionics can share master control................................................................. 101

Figure 55 - Schematic of payload to avionics parallel port. An I2C GPIO expander, U37, interfaces with a parallel port on the PC&DH microcontroller for status byte updates. An array of LEDs assists in software development and troubleshooting................................................................. 102

Figure 56 - Schematic of payload switching regulators. Buck Boost converter, U1 and inverting charge pump, U2 cascaded with LDOs provide the required 3.3V, 5V and -5V power rails used throughout the payload................................................................. 104

Figure 57 - Schematic of SMA driver. Power MOSFETs Q(1-4) are configured as low side switches to sink current through selected SMA actuators. U34 monitors current and voltage to confirm proper operation................................................................. 105
Figure 58 - Schematic of SMA position switch logic feed through. Pull up resistors convert the open and closed states of mechanical switches to logic states that can be read in by the microcontroller........................................................................................................................................... 106

Figure 59 - Wait & Read algorithm. This algorithm is used to toggle the peak detectors and read in a waveform magnitude value after a sufficient delay........................................................................................................................................... 107

Figure 60 - Adjust gain algorithm. This algorithm is used within the automatic gain control to approach an optimal signal amplitude........................................................................................................................................... 109

Figure 61 - An overlay of signal amplitude and beam magnitude frequency response. Data points are achieved from an experiment run of a baseline beam system. The automatic gain algorithm amplifies the accelerometer amplitude to a relatively constant level. Normalizing the signal amplitude by the gain and converting voltage units to acceleration achieves the magnitude frequency response plot. ........................................................................................................................................... 110

Figure 62 - Automatic Gain Control Algorithm. This algorithm approaches an optimal signal level, while tolerating transients and rail conditions. Loop counters insure the algorithm does not enter an infinite loop. Various parameters of the algorithm can be updated remotely to adjust for unknown particle damper dynamics........................................................................................................................................... 111

Figure 63 - An overlay of gain factor and beam magnitude frequency response. Data points are achieved from an experiment run of a baseline beam system. The automatic gain algorithm amplifies the accelerometer amplitude to a relatively constant level by adjusting the signal chains dynamic gain. As can be observed from the plot, the gain is reduces as the beam’s response increases. A discontinuity near the resonant frequency indicates a transition from the accelerometer’s 2g full scale to 6g full scale........................................................................................................................................... 112

Figure 64 - Find Steady State Algorithm. This algorithm detects a steady state condition by comparing past and present magnitude levels. The tolerance of the steady state determination is iteratively increased to tolerate beat frequencies that may be present in the particle damper’s response................. 113

Figure 65 - An overlay of steady state tolerance and a systems magnitude frequency response. Data points are achieved from an experiment run of a baseline beam system. As can be observed from the plot, a steady state is typically identified within a few milli-g’s. A spike in the tolerance level is present near the resonant frequency owing to the long lasting transients of the underdamped baseline system. Increasing the loop limits within the find steady state algorithm can reduce this spike, but comes at the cost of increased experiment run time. ........................................................................................................................................... 114

Figure 66 - Initialize Input Algorithm. This algorithm takes a successive approximation approach to converge on a desired amplitude. The order of operations is designed to minimize the amplitude error........................................................................................................................................... 116

Figure 67 - Update Input Algorithm. This perturb and observe algorithm is executed successively throughout the experiment run to correct for non flatness in the driving electronics frequency response. ........................................................................................................................................... 117

Figure 68 - An overlay of input fine gain level and input amplitude. Data points are achieved from an experiment run of a baseline beam system. An inspection of this plot demonstrates the Update Input Amplitude Algorithm’s effect on the input amplitude. Noise in the measured amplitude can be observed in the distribution of data points; occasionally this causes a glitch in the amplitude setting as annotated. A discontinuity near the systems resonant frequency is caused by a minimum in the system’s impedance; the update amplitude algorithm can overshoot in its correction causing the observed effect. Both problems may be remedied by averaging readings and performing the update input algorithm more frequently at the cost of longer experiment run time. ........................................................................................................................................... 118

Figure 69 - An overlay of the percent error between nominal frequency and measured frequency. Data points are achieved from an experiment run of a baseline beam system. The divergence of measured output frequency is a result of lower signal to noise ratio as the system’s magnitude response dies off. ........................................................................................................................................... 119

Figure 70 - A plot of a beams phase frequency response. Data points are achieved from an experiment run of a baseline beam system........................................................................................................................................... 120

Figure 71 - An overlay of various data interpolation steps. Data points are achieved from an experiment run of a particle damped beam system. A SHO model is first fit to the measured data points. This physical model is then used to develop a GRNN to interpolate a continuous frequency response curve........................................................................................................................................... 123
Figure 72 - A 3D overlay of a particle damped system’s magnitude response for increasing input amplitude. An inspection of the plot demonstrates a particle damper’s amplitude dependent nonlinearity. Points of interest are highlighted for visualization. ..................................................... 124

Figure 73 - A 3D overlay of a particle damped system’s phase response for increasing input amplitude. An inspection of the plot demonstrates a particle damper’s amplitude dependent nonlinearity. Points of interest are highlighted for visualization................................................................. 125

Figure 74 - A plot set demonstrating a particle damped systems amplitude dependent nonlinearities. Particle mass participation, as determined from the systems natural frequency can be correlated with damping trends. A local maximum in damper efficiency can be observed. ................................................. 125
List of Tables

Table 1 - A trade study of two accelerometer devices considered. These devices are selected as the best representatives of two technology groups separated by a large price discrepancy ........................................ 43

Table 2 - Automatic Gain Control Look Up Table. The PC&DH µcontroller uses this LUT to adjust the gain of a Sensor Module based on the previous amplitude measurement in an effort to maximize the system's signal to noise ratio within the system rails. ......................................................... 155

Table 3 - Initialization state of the frequency and phase hardware .............................................................. 157
List of Equations

Equation 1 – Peak attenuation parameter sensitivity to offset and scale errors ............................................. 36
Equation 2 – Acceleration measurement noise floor ................................................................................... 44
Equation 3 – Determination of signal level needed to resolve minimum acceleration ................................. 44
Equation 4 – DFT frequency resolution sensitivity to windowing function mainlobe width ......................... 49
Equation 5 – Acceleration magnitude sensitivity to output impedance tolerance ........................................ 58
Equation 6 – Cantilever beam natural frequency relation to system mass .................................................... 85
Equation 7 – Period adjustment for Schmitt trigger hysteresis based phase measurement ........................... 94
Equation 8 – Force to voltage piezoelectric transducer general relation ..................................................... 134
Equation 9 – Force to voltage relation for chosen piezoelectric transducer .................................................. 134
Scope of Work

This paper overviews the development of a CubeSat instrument capable of evaluating particle damped systems in orbit. As project manager and principal hardware design engineer, the author attempts to address both system engineering and low level electronic design aspects of the instrument. To accomplish this, the organization of the paper is intended to first motivate high level requirements and then follow these requirements down to low level design, with emphasis on electrical systems.

Chapter 1 provides background on the CubeSat standard. The availability of this standard enables the possibility of this academic particle damper investigation, but places severe restrictions on payload resources, driving much of the instrument design methodology.

Chapter 2 begins with an overview of particle damper theory, applications, and modeling attempts. Subsequent sections focus on particle dampers within a microgravity environment, offering behavior predictions and an explanation of the potential space applications that justify this mission.

Chapter 3 outlines high level instrument requirements as defined by supporting industry engineers and the hard requirements of the CubeSat platform.

Chapter 4 describes high level design decisions driven by the requirements outlined in Chapter 3 and cost versus performance tradeoff considerations.

Chapter 5 provides a comprehensive description of the low level electronics system built to support the high level design decisions identified in Chapter 4. Supporting software algorithms are outlined to lend to the understanding of the electronics functionality.
Chapter 6 introduces a post processing data analysis process to give the reader perspective of the complete system functionality. Example data plots are provided to show the type of particle damper evaluation the developed instrument can provide.

Chapter 7 concludes the paper with a summary of mission status and remaining work.
1 CubeSat Satellites

1.0 The CubeSat Standard

In 1999, Dr. Jordi Puig-Suari of California Polytechnic State University and Professor Robert Twiggs of Stanford University cofounded the CubeSat standard in an effort to facilitate student satellite programs. Two primary elements of the standard accomplish this goal: first, the definition of a standardized satellite geometry, made small enough to both reduce cost and expedite satellite development time, yet large enough to provide useful payload volume and sufficient surface area for solar power generation\(^1\); second, the production of a deployment mechanism designed to allow cubesats to harmlessly occupy unused volume within a launch vehicle paid for in bulk by a primary commercial or government customer\(^1,2\).

A one unit, or 1U, cubesat occupies the volume of a cube with an edge dimension of 10cm; a photograph of a 1U cubesat is provided in Figure 1. Expansion or contraction of this geometry is possible as long as a 10cm square cross section is maintained. This universal cross section dimension allows developers to leverage previously designed subsystems, enabling students to build upon the work of alumni or collaborate with external sources; providing the means in which a CubeSat program can continuously advance despite the coming and going of student generations.
Figure 1 - A photograph of CP6, a one unit, or 1U, cubesat built by Cal Poly’s PolySat program.

Complementing the CubeSat standard is the P-POD, or Poly PicoSatellite Orbital Deployer. When integrated, a P-POD houses up to three 1U cubesats, (or equivalent configuration). An electrical impulse provided by a launch vehicle sequencer triggers the P-POD door to open causing the cubesat(s) to deploy under force from a spring loaded plunger. A rendering of a P-POD is provided in Figure 2.

Figure 2 - A rendering of the P-POD Mark II. The exploded view, right, exposes the spring plunger mechanism used to expel internal cubesat(s) after the door is released.

While the P-POD is instrumental to successful deployment of cubesats, its primary role is to shield the launch vehicle’s primary payload from any physical or electromagnetic damage a cubesat may otherwise inflict[2]. Demonstration of this capability gives launch providers the insurance needed to allow cubesats to share a
vehicle with the payload responsible for funding the vast majority of the launch. Such confidence allows P-PODs to piggy back on pre-existing launches, occupying either unused volume or taking the place of ballast mass. This gives potential for cubesat flight opportunities on nearly every launch; a goal that has made great strides with the NASA ELANA cubesat launch initiative, which offers P-POD positions on several upcoming NASA launches[^3].

### 1.1 CubeSats Today & Tomorrow

Since the inception of the CubeSat standard, over 90 universities, both domestic and abroad, have founded CubeSat based programs[^4]. Together, these programs have developed over 50 unique cubesats, and to date, over 25 of these satellites have been successfully deployed in orbit[^5]. The multidisciplinary engineering experience involved in these cubesat programs gives students a unique skill set scalable to large spacecraft missions. This experience advances students well into the steep learning curve of space system development prior to entering the professional aerospace field, positioning them to make immediate contributions to the industry.

The capabilities of cubesat satellites are continuously being expanded through technological advances in low power, high performance microelectronics, solar cell efficiency and miniature electromechanical systems. This increased performance coupled with the low fiscal risk inherent with cubesat development and deployment has begun to attract the attention of government and commercial institutions.

Beginning with a successful biological experiment conducted on the NASA Ames GeneSat-1 cubesat in 2006, six branches of NASA have entered the CubeSat
community\textsuperscript{[4]}. As many as 40 different government and commercial organizations across the globe have followed suit\textsuperscript{[4]}. Working either independently, or in collaboration with university CubeSat programs, these institutions have implemented missions varying from technology demonstrations to fundamental scientific research. Such missions serve to further accelerate the popularity of the CubeSat standard as well as advance the field of space technology in its entirety.

In the near future, two advancements are poised to provide a quantum leap in cubesat satellite potential. First, The Global Educational Network for Satellite Operations (GENSO) holds promise to provide nearly continuous communication to cubesats while over land through a network of small ground stations sharing an internet database\textsuperscript{[2]}. This system will effectively increase the rate and amount of data linked in ground-satellite communication, allowing cubesats to compete with larger satellite concepts with power budgets affording higher downlink bandwidth.

Second, with the increase in launch opportunities for cubesats, the formation of cubesat to cubesat networking is becoming feasible. These networks would enable cubesats to share computational, sensor and communication resources while providing mission redundancy. This resource sharing would not only allow a cubesat constellation to achieve the functionality of some larger satellites, but through the dispersion of instrumentation in orbit, surpass the capability of any single satellite in performing various scientific data acquisition missions.
1.2 CubeSat at Cal Poly

Under leadership from Dr. Jordi Puig-Suari, a cofounder of the CubeSat standard, two sister cubesat based programs have been founded at California Polytechnic State University.

The Cal Poly CubeSat program operates as the core of the international CubeSat community. Students and staff within this organization are responsible for the development, construction and revision of the P-POD, definition and maintenance of the CubeSat standard, and the procurement of flight opportunities. These duties involve extensive collaboration with government, commercial and academic institutions to insure flight hardware qualification and integration compatibility.

The student run PolySat program serves primarily as a cubesat developer. To benefit both student education and the advancement of cubesat technology, PolySat operates under a philosophy that stresses custom system development. Despite this low level approach, the PolySat program averages production of one cubesat per two years. This is facilitated largely through collaboration with commercial and government organizations which contribute both financial and engineering resources. An overview of prior and current missions can be found in Reference 6.

1.3 Introduction to the CP7 Mission

The CP7 mission exists as a collaboration between Northrop Grumman Aerospace Systems and Cal Poly State University’s PolySat student research group. Northrop Grumman serves to define minimum mission requirements and provide scientific advisory; PolySat performs design and development of satellite systems with deliverables
of a complete flight ready unit. These efforts are funded by an educational grant gifted from Northrop Grumman.

Minimum requirements of the CP7 mission entail delivery of a 1U cubesat with payload instrumentation capable of providing data for the evaluation of a particle damped system in orbit. The satellite must also include an avionics system providing basic support of payload operations including power generation/regulation and command and data handling with radio link to a supporting ground station.

The payload instrumentation must excite a well characterized baseline mechanical system with an attached particle damper, and measure steady state magnitude response of the system over a range of frequency and amplitude. At a minimum, the frequency range of interest should encompass a 100Hz bandwidth centered at the first mode resonant frequency of the baseline system with frequency resolution of $1/8^{th}$ Hz. Input amplitude must be capable of producing a peak velocity response of the baseline system within a range of 2.54e-4 m/s to 1.27e-1 m/s over five discrete amplitude steps.

Successful acquisition and downlink of this data will allow an analysis to be conducted to determine particle damper performance metrics in microgravity. If performance levels demonstrate the technology’s viability in space, further study of the data achieved from the CP7 mission will facilitate the design of particle dampers configured to meet spacecraft vibration mitigation requirements. Such implementation holds promise of providing superior performance at a reduced cost to existing technologies.
2 Particle Damping

2.0 An Introduction to Particle Damping

2.0.0 Impact Damping Origins

Particle damping technology has evolved from a single particle configuration known as an impact damper. An impact damper typically consists of a ball bearing constrained within a cylindrical cavity terminated by a wall on each side. When the cylinder is oriented in the direction of incident vibration, energy is dissipated through the momentum exchanges that occur as the ball bearing reciprocates between cavity walls[7]. A rendering of this configuration is provided in Figure 3.

Figure 3 - A rendering of an impact damper attached to a second order spring dashpot model. Here, a ball bearing is constrained within a cylindrical cavity.

While nonlinear, the dynamics of an impact damped system can be modeled with satisfactory accuracy[32]. This allows parameters such as cavity dimension and particle mass to be analytically optimized to provide maximum damping for a given forcing function.

The effectiveness of impact damping quickly drops off as the excitation frequency, amplitude or direction varies from the optimized value[7,8]. This limitation severely
narrow the viability of impact damping in applications requiring broadband, multi-axis vibration attenuation.

2.0.1 Particle Damping Overview

A particle damper is conceptually similar to an impact damper, but expands cavity dimensions to allow free particle motion and divides total particle mass among multiple smaller particles. A rendering of this configuration is provided in Figure 4.

![Figure 4 - A rendering of a particle damper. While shown attached to a second order spring dashpot model, particle damping has been demonstrated to be effective for multimodal, multidirectional vibration attenuation.](image)

The particle-wall and particle-particle interactions within the damper architecture involve energy dissipation mechanisms including multi-axis momentum transfer and several forms of frictional forces. The combined dynamics of this system can provide high attenuation of a broad range of input excitation frequency, amplitude and direction[8,9,10,15].

The intrinsically simple and robust construction of particle dampers combined with versatile effectiveness has compelled their use in a verity of applications. In the
automotive industry, particle dampers are used to attenuate vibration in vehicles to increase passenger comfort\textsuperscript{[11]}. An insensitivity to extreme temperatures and high cycling have made particle dampers particularly suitable for damping vibration in turbomachinery\textsuperscript{[12,13]}. In spacecraft, particle dampers have been used to eliminate destructive structural resonant modes that would otherwise damage components during launch\textsuperscript{[14,15,16]}.

2.0.2 Particle Damping Analysis

The same mechanisms that give particle damping advantage over impact damping introduce highly nonlinear system dynamics that complicate modeling attempts\textsuperscript{[8,9,13]}. Researchers have addressed this added complexity using a number of methods.

S. Simonian \textit{et al.}\textsuperscript{[18]} developed an analytical expression which accounts for velocity dependent dynamics. This equation is dependent on empirically derived constants unique to system parameters including particle-cavity volumetric fill ratios, particle and cavity material properties, orientation with gravity and cavity and particle geometry.

K. Mao \textit{et al.}\textsuperscript{[19]} have attempted to develop a more general model using an event driven discrete element numerical simulation which calculates the state of each particle as a function of time, updating initial conditions every instant a collision occurs and calculating the resulting energy dissipation. This method is limited by computational resources, which generally restricts studies to transient response analysis of systems with up to a few hundred particles\textsuperscript{[20]}.
C. Wu et al.\textsuperscript{[20]} propose an alternative to discrete element models using fluid
dynamics theory, equating particle-particle friction to drag forces. This methodology
reduces computational requirements, allowing for the study of granular particle systems.

C. Salueña et al.\textsuperscript{[21]} leverage molecular dynamics simulations to correlate granular
particle damper performance trends to vibration velocity dependent phase changes
observed to occur in granular media. These phase changes mark transitions of solid like
to liquid like to gas like behavior of granular systems and the bifurcation of various
convection cell topologies.

These models show promise for predicting particle damper behavior for a
restricted set of operational conditions, however a global solution to particle damper
analysis has not been achieved. The lack of a universal model is a barrier in the
development of particle dampers, one that is generally overcome through successive fine
tuning of design parameters until an optimal response is achieved for a desired
environment. In the case of microgravity application, this type of procedure is not
possible in terrestrial laboratories, as gravity plays an important role in the system
dynamics\textsuperscript{[9,13,19]}.

\section*{2.1 Predicting Microgravity Particle Damper Dynamics}

Knowledge gaps in our understanding of ground based particle damper dynamics
compounds the uncertainty of microgravity behavior. A particle damper energy
dissipation mechanism that plays a small role under the influence of gravity may
transition to a dominant source of damping in the absence of gravity; similarly a
mechanism that plays a large role within gravity’s influence may become negligible
outside of it. This nonlinearity emphasizes a need for experimentally derived data, rather than extrapolated predictions.

While researchers can not entirely escape the effects of gravity in the laboratory, experimentation of particle dampers forced to high amplitude, where the significance of gravity’s contribution to the system is reduced, may provide insight into microgravity particle damper dynamics.

Particle damper amplitude dependent nonlinearities are particularly pronounced in the case of granular particle dampers. Researchers have demonstrated that as a granular particle damper is forced to higher amplitudes, a local maximum in energy dissipation occurs\cite{22}. The shape of this curve has been attributed to the fluidization of the granular particles, where the energy of the particles, or so called mechanical temperature, causes a transition from solid like behavior to liquid like behavior\cite{21,22}.

The onset of this liquefaction corresponds to the peak in particle damper effectiveness. C. Wong et al.\cite{22,25} have hypothesized that this is due to a transition from a maximum in shear type friction to a less dissipative rolling type friction. Indeed, C. Salueña et al.\cite{21} using molecular dynamics simulations have correlated maximum damping to a glass like state, and minimal particle damper effectiveness to the bifurcation of organized convection cells. Furthermore, the beginning of this fluidization regime can be correlated with the mechanical temperature of the particles surpassing the force exerted on them by gravity\cite{21,22,23}.

The link between static force exerted on the system and damper performance was further explored in experiments conducted by J. Rongong et al.\cite{23} where the force due to gravity was supplemented by a uniform magnetic field acting on ferrous particles. The
result of this experiment indicates that the fluidization of the granular medium occurs at higher levels of amplitude, seemingly verifying the ultimate correlation between the magnitude of gravity and particle damper effectiveness.

At first consideration this indicates that in an absence of gravity, the mechanical temperature needed to enter the fluid state will be minimal and damper performance will be low relative to damping performance on the ground. However, research in granular particle physics indicates that for a high enough mechanical temperature, a third, gas-like, phase exists[24,25]. Intuitively, one can envision such a state occurring in the absence of gravity, without the need of particle energy, where particles are dispersed uniformly within the cavity volume.

In this gas state, the contribution of friction to total energy dissipation will be negligible. Instead, particle-particle and particle-cavity momentum exchanges will account for nearly all energy dissipation. Due to the high amplitude levels needed to achieve this state on the ground, experimental data in this regime is sparse. However, the molecular dynamics simulations conducted by C. Salueña et al.[21] indicate that damping increases once more in this state, giving hope that particle damper performance in microgravity may reach levels comparable to that of the glass like state achieved under force from gravity.

This prediction of microgravity particle damper performance in a complete gas like state relies on extrapolation of simulation results, which does not come with a high degree of confidence. However, the correlation experimentally observed between gravity, particle states and damper performance in these studies does allow the conclusion to be drawn that in an absence of pressure due to gravity, only a gas like state
will exist, and damping performance will behave more linearly due to the lack of phase transitions. If this conjecture is demonstrated to hold true, it suggests that designing particle dampers for use in space may be a less complicated task then designing particle dampers for terrestrial applications.

2.2 Space System Mechanical Damping Requirements

2.2.0 Modal Attenuation

Launch vehicle limitations and expense drives the miniaturization of spacecraft volume and mass; a process that results in light weight structures, often involving cantilevered deployable antennas, instrumentation and solar arrays\textsuperscript{[26,27]}.

Left uncompensated, these configurations present serious mission hazards related to underdamped structural resonant modes. In space, vibration does not dissipate as it would on Earth for lack of parasitic coupling and viscous atmospheric drag. Therefore concerns related to structural resonant modes become especially significant, where impulses from thrusters or deployment mechanisms may cause long lasting transients manifesting problems varying from degradation of pointing accuracy to structural damage.

A photograph of the International Space Station (ISS), presented in Figure 5, offers an example of a space structure presenting potentially serious vibrational hazards. Indeed, a recent event demonstrated the severity of an underdamped structural mode during an ISS orbit adjustment in 2009. A faulty thruster command sequence resulted in a periodic force that excited a one half Hz mode in the ISS, reaching an amplitude speculated to have exceeded the rated limit by a factor of five\textsuperscript{[28]}. While no damage was
detected after this event, serious concerns arose causing delays effecting ISS operations and resupply missions\textsuperscript{[29]}.

![Figure 5 - A photograph of the International Space Station. The low mass, cantilevered structural components, typical of spacecraft configurations, present concerns related to destructive resonant modes. Photo Credit: NASA JSC \textsuperscript{[39]}](image)

2.2.1 Jitter Reduction

Miniaturization of spacecraft volume often necessitates colocating sensitive instrumentation with reaction wheels, cryocoolers and other sources of mechanical noise. This can significantly distort sensor readings. In the case of earth observation, camera jitter on the order of ten thousandths of a degree results in a field of view displacement on the order of tens of meters\textsuperscript{[30]}. Similarly, mechanical noise can restrict the range of satellite to satellite communication among other systems requiring ultra-stable pointing accuracy\textsuperscript{[30]}.

2.3 The Potential of Particle Damping within Space Systems

Ground and launch applications of particle damping have demonstrated an attractive performance cost trade off for both the attenuation of resonant modes\textsuperscript{[11,15]} and
jitter reduction\textsuperscript{[9]}. If this performance is demonstrated to hold in microgravity, particle
damper technology promises competitive advantage over damping mechanisms currently
used in space environments.

2.3.0 Comparison to Active Damping Approaches

As a passive technology, particle damping holds several inherent advantages over
active damping mechanisms. Active damping typically involves closed loop noise
cancelation algorithms controlling either piezoelectric or electromagnetic actuators.
Unlike passive techniques, this implementation requires constant current draw that must
be deducted from a spacecraft’s power budget. Furthermore, bandwidth limitations
restrict active damping effectiveness to lower order modes, where as passive technologies
may be configured for broadband vibration attenuation\textsuperscript{[31]}. These factors combined with
a high development cost and a sizable increase in system complexity usually restrict
active damping to applications presenting severe low frequency resonant modes or
having precision or adaptable dynamic response control requirements.

2.3.1 Comparison to Traditional Passive Damping Approaches

Within the category of passive damping, the robust and simple configuration of
particle damping avoids many of the shortcomings traditional mechanisms present. A
brief overview of these advantages follows.

- Particle damper architecture lends itself to nearly unlimited lifespan, offering distinct
  advantage over friction based dashpot mechanisms which degrade over high
cycling\textsuperscript{[32]}. 
• Particle dampers may be incorporated within cavities machined into existing structural components thereby avoiding mass penalties\textsuperscript{[11,22,33]}. 

• Particle dampers may be bolted onto structures as a need for additional damping is recognized, thereby reducing the severity and cost of system redesign\textsuperscript{[15]}. 

• Particle dampers demonstrate performance independent of temperature\textsuperscript{[12,13,19,22]}, a unique property that is especially attractive for implementation in a space environment. 

• An avoidance of ferrous materials in particle damper design eliminates magnetic interference concerns that can become a complication in the implementation of eddy current dampers\textsuperscript{[34]}. 

• Particle dampers can be constructed from low cost metallic or ceramic materials\textsuperscript{[19,22,35]}, giving economical edge over exotic polymeric viscoelastic or tuned circuit piezoelectric dampers. 

2.3.2 Particle Damping Compared to Viscoelastic Damping

Viscoelastic damping is perhaps the most predominant space system damping technology that particle damping is poised to disrupt. Viscoelastic dampers are commonly formed by layering polymeric sheets between rigid boundaries\textsuperscript{[36]}. During optimal conditions, material losses in this composite can contribute high multimodal vibration attenuation over a broad frequency spectrum, a quality that has driven the popularity of viscoelastic damping within space applications\textsuperscript{[37]}. However, this performance peaks within a narrow temperature band, on the order of 10°C\textsuperscript{[38]}. Temperatures below this optimum range cause polymeric materials to enter a glassy state.
and temperatures above this range cause a transition to a rubbery state. In either phase, effective damping drops off\cite{38}. Furthermore, exposure to radiation, high vacuum, atomic oxygen, micrometeorites and high cycling have been attributed to gradual degradation in polymeric materials and damping characteristics\cite{19,37}. These limitations may largely be circumvented through the use of particle dampers, which have negligible dependence on such environmental elements.

2.3.3 Space System Obstacles

Despite these numerous qualities, an uncertainty of particle damper dynamics in microgravity inhibits their use in space applications. A particle damper configuration optimized to attenuate a vibration profile on the ground will likely become suboptimal once the system is free from the Earth’s gravitational pull. Without a clear understanding of how exactly the system dynamics shift in the 1g to 0g transition, designers can not predict or compensate for particle damper characteristics in space. The CP7 mission will do much to fill this knowledge gap, providing orbital frequency response data that can be directly compared to preflight ground data. Generalizations made from this overlay will contribute to the development of models that may someday allow engineers to fine tune particle damper configurations for microgravity operation.
3 System Requirements

3.0 Requirement Origins

Collaboration between Northrop Grumman Aerospace Systems and PolySat on a cubesat based particle damping evaluation system began during the summer of 2008. During initial meetings, desired science was weighed against the constraints of a cubesat payload in an effort to find an optimal compromise between system capability and system complexity. A one unit cubesat capable of evaluating the steady state dynamics of two particle damper configurations and one experiment control system was agreed upon. The name CP7, designating Cal Poly’s seventh cubesat mission, was allocated to the project. A student led CP7 team was organized within PolySat and began working closely with Northrop Grumman system dynamics engineers to identify and define mission requirements.

3.1 Science Requirements

3.1.0 Baseline Mechanical System

In order to experimentally evaluate the performance of a particle damper, the damper must be integrated within a primary mechanical system with known baseline dynamics. The contribution of the particle damper to the total system response can then be assessed by deducting these baseline dynamics. The accuracy of this analysis is dependent on how well the primary system is understood. This drives the design requirement of a simple linear primary system that can be closely approximated by an analytical model.
Because it is desired to test two different particle damper configurations within the cubesat, the satellite structure must accommodate three of these primary mechanical systems; two containing different particle damper volumetric fill ratios and a third containing an unfilled damper cavity. This empty particle cavity provides the means in which the baseline system response can be directly measured. The structure must also be designed to minimize parasitic damping and coupling so that each primary system is mechanically isolated and control over the experiment variables is maintained.

### 3.1.1 System Input & Output

In order for the CP7 payload to collect data necessary for the analysis of a particle damped system response it must be capable of forcing each system and measuring the resulting motion. For a linear system this requires a signal generator and actuator with a bandwidth that encompasses the spectrum of interest. However, the amplitude dependent nonlinearities of particle dampers also necessitate the ability to vary the forcing function magnitude. Additionally, the implementation of the sensing and actuating transducers must have minimal effect on the linearity and predictability of the baseline systems so as not to interfere with the evaluation of the particle dampers contribution to the system dynamics.

The signal generator and actuator must support the dynamic range and fidelity specified by a 100Hz bandwidth centered at the first mode resonant frequency of the baseline system with frequency resolution of $1/8^{th}$ Hz. Input amplitude must be capable of producing a peak velocity response of the baseline system within a range of $2.54e-4$ m/s to $1.27e-1$ m/s over five discrete amplitude steps. The sensor and data acquisition
algorithm must be capable of the recording either displacement or acceleration magnitude response at the physical location of the particle damper with a resolution and bandwidth capable of sensing this dynamic range. These parameters are selected based on Northrop Grumman’s prior experience with particle damper performance analysis.

3.2 CubeSat Platform Requirements

All payload requirements are further restricted by cubesat limitations. Subtracting PolySat’s avionics package mass and volume from available 1U cubesat resources allows approximately 750cm$^3$ and 1kg for the payload which is defined here to include batteries.

The payload must be able to survive launch vibrations which are qualified to 14.1 GRMS random vibes per the NASA GEVS standard$^{[17]}$. The payload must be capable of operating within a space environment which involves a hard vacuum and -60°C to 70°C external temperature range. When possible, ferrous and magnetic material is to be avoided in order to minimize interactions between the cubesat and the Earth’s magnetic field, which can result in undesirable tumbling.

While exact power and downlink figures are dependent on orbit, telemetry from previous PolySat missions including CP3 and CP6, which are in polar and 40.5° inclination low earth orbits respectively, gives bases for estimation. Average power production can be expected to be about 1.5 watts over the course of an orbit. After deducting the requirements of PolySat’s new avionics system, this leaves approximately .43 average watts available to the payload per orbit in order to remain power positive. This figure assumes a 1/3 duty cycle beacon rate which has been found to be a great asset to cubesat position determination and telemetry download. PolySat’s new avionics
system is expected to support 9600 baud communication; scaling CP6’s downlink accordingly suggests that as much as 960kb may be downlinked per day under an aggressive operations plan. Assuming a 10% packet overhead, this amounts to a maximum daily downlink of 864kb of experiment data.
4 High Level Design

4.0 Primary Mechanical System

In the conceptual stage of CP7, structural dynamics engineers within Northrop Grumman recommended an approximate single degree of freedom cantilever beam to serve as the primary mechanical system onto which to integrate a particle damper. The first mode small displacement motion at the tip of a cantilever beam can be closely approximated by the equation for a simple harmonic oscillator with viscous damping. This well understood model can be fit to cantilever beam based experiment data to accurately estimate the performance of auxiliary damping mechanisms.

Furthermore, cantilever beam natural frequency and quality factor can be accurately related to material properties and dimensions. These parameters can be selected to achieve a very low damping ratio, an advantageous quality for auxiliary damping technology evaluation where damping contribution becomes more apparent. Indeed, previous efforts have demonstrated the effectiveness of a cantilever beam configuration as an effective baseline system from which to experimentally quantify particle damper properties\cite{13,16,19,20,32,35}.

A cantilever beam system is also suitable for implementation within a cubesat. A beam fitted with a tip mass aligned along the diagonal cross section of a cubesat can be made long enough to achieve a resonant frequency within a 60Hz to 100Hz band of interest, and can be made with enough mass to achieve a desirable primary system effective mass to particle damper mass ratio. A photo of cantilever beam machined for the CP7 payload is presented in Figure 6.
Figure 6 An annotated photograph of a cantilever beam within CP7’s payload. An aluminum cantilever beam serving as a baseline mechanical system for particle damper evaluation is machined as a single piece along the diagonal of a structural cross section. A stainless steel tip mass containing a particle damper is screwed onto the free end of the beam. Three such beams are stacked on top of each other within CP7’s payload.

4.1 Particle Damper

Within CP7, the free end of each cantilever beam has an affixed tip mass containing an enclosed cubic cavity with an edge dimension of approximately 9mm. In one beam, this cavity is empty, serving as the undamped system baseline. The remaining two cavities are partially filled with tungsten crystalline powder; a particle damping configuration demonstrated to have high damping performance\textsuperscript{[9]}. A photo of this tip mass is presented in Figure 7. Two unique volumetric fill ratios of 90% and 95% are chosen to evaluate performance sensitivity to fill ratio.
Figure 7 - A photograph of the tip mass particle damper cavity used within CP7. This stainless steel piece bolts to the cantilever beam free end, serving to increase the mechanical system’s effective mass to a favorable level. Fine tungsten powder (not shown) fills the cavity, forming the particle damper.

Care is taken to maintain the purity of the tungsten powder. Foreign debris and moisture can have significant effect on particle damper behavior. Therefore before integration, the tungsten is baked out in a thermal vacuum chamber to evaporate any residual moisture. Once the particle damper cavities are filled, a bead of epoxy is applied along the seam of the cavity to beam interface to produce a hermetic seal.

4.2 Cubesat Structure

The design of a structure capable of housing three cantilever beams within the volume and mass constraints of a cubesat while simultaneously minimizing parasitic damping and mechanical coupling between the individual beams is a significant engineering challenge. Not only must this structure meet these requirements but it also must be designed to house supporting electronics, wiring, batteries, and solar cells in a form factor that is machinable and conducive to assembly. Several design techniques were employed to achieve such a structure.
In order to minimize parasitic damping, the cantilever beams are machined as a single piece with structural cross sections. This eliminates damping that would otherwise occur at a bolted interface between the cantilever beam’s base and the structure. The individual cross sections are left as separate pieces to reduce machining complexity and to aid in assembly. Large bolts and alignment pens allow the cross section components to be tightly joined under enough compression to negate the effects of parasitic interface damping.

Next, to reduce mechanical coupling the structure is overbuilt such that its resonant frequency is several orders of magnitude greater than that of the beams. This maximizes the amplitude response of the beams while helping to isolate each of the three beam systems. To further reduce mechanical coupling between the cantilever beams a system of locking mechanisms enable the structure to selectively lock and unlock cantilever beams so that at any given time only one beam is allowed to oscillate. While this significantly increases system complexity, no additional risk is presented to minimum mission success through an operations plan that evaluates all beams in an unlocked state before attempting any lock commands. Additional low level details of CP7’s structural development are documented in the thesis work of John Brown in Reference 42. A rendering of the CP7 structure with integrated systems is presented in Figure 8; a photo complement is presented in Figure 9.
Figure 8 - A computer rendering of CP7. Three similar structural crosspieces, shown in red, make up the payload mechanical system. This configuration is designed to control the physical experiment variables within the constraints of a cubesat.

Figure 9 - A dual view photograph of the assembled CP7 structure. Individual cross sections are machined out of aluminum, anodized and joined together with alignment pins and bolts. The completed satellite will include side panels housing solar cells and magnetorquers affixed to each face.
4.3 Cantilever Beam Actuators

4.3.0 Actuator Requirements

An independent forcing function must be applied to each cantilever beam in order to excite a system response that can be measured. This necessitates the need for three independent actuators. These actuators must be capable of delivering a known force to the cantilever beam system proportional to a controlled electrical signal while providing minimal interference to the beam dynamics. This force must be dynamic with a spectral bandwidth of at least 100Hz while maintaining a flat amplitude profile. The force exerted by the actuator must also be controllable in magnitude, achieving a peak velocity in the baseline beam tip over a range of several orders of magnitude. The actuators must be small, lightweight, power efficient and have minimal ferrous or magnetic material such that they are suitable for a 1U cubesat. These stringent requirements point to a single technology, piezoelectric actuators.

4.3.1 Actuator Selection

A piezoelectric actuator typically consists of a ceramic material containing small crystals that can be polarized through the application of a high DC potential. This poling process gives the ceramic the ability to linearly transduce mechanical and electrical energy\textsuperscript{[40]}. This phenomenon does not involve magnetic fields and the commonly available piezoelectric crystal materials are nonferrous.

Piezoelectric ceramics operated in the electric to mechanical conversion mode produce high forces over small displacements. This property makes them suitable for a so called unimorph configuration where a piezoelectric plate is bonded along the base of
a passive elastic material, such as that of an aluminum cantilever beam [41]. Within this configuration, an electric potential applied across the piezoelectric plate produces an approximately linearly proportional force incident on the cantilever beam; this relationship is quantified in Appendix A, as developed in Reference 40.

This piezoelectric unimorph configuration is well suited to CP7’s actuator requirements. Within CP7 a single plate piezoelectric ceramic actuator is bonded to the base of each cantilever beam using a thin layer of high strength aerospace grade epoxy. Applying a sinusoidal electric signal across a piezoelectric actuator induces a proportional sinusoidal force incident on the respective beam. This forcing function can be directly controlled by varying the amplitude and frequency of the incident electric signal.

### 4.3.2 Piezoelectric Ceramic Selection

The piezoelectric ceramic material and dimensions chosen for the beam actuators is driven by the availability of device samples. A piezoelectric plate of lead zirconate titanate material designated PZT-5A3, with a length of 1.75”, width of .5” and thickness of .10” was sampled from Morgan Electro Ceramics. With a mass of 10.5 grams, this plate was deemed to be sufficiently light and small enough for the CP7 payload. In proof of concept testing, this plate was found to produce sufficient motion at the free end of a test beam for an achievable voltage magnitude, indicating that the stated velocity requirements could be met. A photograph of this actuator is provided in Figure 10.

It should be noted that the addition of a ceramic plate to the aluminum cantilever beam effects system dynamics and complicates optimal beam design. While linearity is
largely maintained, the addition of the plate increases average beam stiffness and subsequently increases the beam’s resonant frequency for a given aluminum thickness. This problem was addressed using finite element analysis software and the specified material properties of the aluminum and the PZT-5A3 ceramic. An optimal beam response could then be approached through an analysis of simulation results versus aluminum thickness. These efforts are detailed within the thesis work of John Brown in Reference 42.

Figure 10 - A photograph of the piezoelectric actuator selected for actuating the cantilever beams within CP7’s payload. The actuator consists of rectangular PZT5A3 ceramic plated with silver electrodes on each face. The dimensions of the unit are 1.75” long by .50” wide by .10” thick.

4.4 Cantilever Beam Locking Mechanism Actuators

4.4.0 Actuator Requirements

In order to simplify analysis and control experiment variables it is desirable to mechanically isolate each cantilever beam from surrounding systems. Left unchecked, the forced motion of one beam would couple into surrounding beams, effectively increasing non particle damper energy dissipation and degrading analysis accuracy. This drives the need for an active locking mechanism capable of altering a selected cantilever beam’s dynamics sufficiently such that mechanical coupling becomes negligible. Just as with the cantilever beam actuator selection, 1U cubesat volume, mass and material constraints severally limit the locking mechanism’s actuator options. However, through
the application of a bistable locking mechanism, power limitations become more relaxed, as locking commands will be infrequent within mission operations. This set of requirements points to shape memory alloy actuators.

4.4.1 Actuator Selection

A shape memory alloy (SMA) actuator operates by passing current through a specialized alloy, often nickel titanium, also known as nitinol. Ohmic resistance in the alloy produces thermal energy causing the SMA to deform. When the current is removed the SMA cools and returns to an original shape. The stroke and force of this action can be compounded using a system of SMA wires and can be made to be much greater than a solenoid actuator of comparable volume and mass.

In order to reduce development cost, a commercial off the shelf (COTS) SMA actuator was selected as the bases for the locking mechanism design. The Dash-4 SMA actuator developed by Miga Motor Company is rated to produce 906 newtons (or 1.75 pounds) of force over a 5.8mm stroke\(^{[43]}\). A single actuator consumes less than 10 grams and 6.3 \(\text{cm}^3\) of volume within a low profile package that is particularly suitable for integration within each cantilever beam structural cross section. The Dash-4 is built from nonferrous material and flight hardening involves simply replacing stock lubricant with a low outgassing aerospace lubricant. The Dash-4 can be powered from the unregulated CP7 battery rail. At a nominal 3.7V, the actuator draws just over one amp, requiring approximately three seconds under load to complete its stroke. This energy requirement is well within the CP7 power budget given the low anticipated locking duty cycle. A photo of a Dash-4 modified for use within the CP7 payload is presented in Figure 11.
4.4.2 Locking Mechanism Overview

The CP7 bistable locking mechanism implementation consists of a configuration in which each beam is accompanied by a lever arm actuated by a Dash-4. In the unlocked state the lever arm is held back under spring tension such that the cantilever beam may oscillate freely. In the locked state the lever arm is pushed past a spring loaded clasp, holding the lever arm against a cantilever beam in a slightly deflected state. This raises the natural frequency of the beam such that it will present minimal interference to the evaluation of the neighboring cantilever beam systems. In this way, by locking two beams, the third is effectively mechanically isolated. A photograph of this mechanism is presented in Figure 12.

To reselect a beam system to test, all beams are first unlocked using a fourth actuator attached to a common drive shaft that releases the lever clasps such that all locking levers return to the unlocked positions. Then the two neighboring beams are
independently locked one by one. Further information on this locking mechanism is available in the thesis work of John Brown in Reference 42.

![An annotated photo of the CP7 beam locking mechanism. In the locked state the lever arm deflects the cantilever beam such that mechanical coupling to adjacent beams is reduced. In the unlocked state (shown) the cantilever beam is free to oscillate. The lever clasp holds the lever arm in either state without the need for continuous actuation power.](image)

4.5 Sensor Selection Criteria

4.5.0 Criteria Overview

The magnitude of a cantilever beam’s response to a given excitation force must be measured to complete the output over input magnitude transfer function needed in the particle damping analysis. This calls for three independent sensors capable of measuring either the displacement or acceleration of each beam at the location of the particle damper within the stated frequency and magnitude range of interest. These sensors must be selected such that their mass, volume and power consumption is conducive to integration within a 1U cubesat and their implementation must not complicate the dynamics of the
system under measurement. Several technologies exist that satisfy these criteria, therefore complexity versus performance must be considered.

Sensor complexity is defined by the cost of system development as measured in time, manpower and monetary resources; it generally also reflects the number of failure modes in the system. Sensor performance is defined by absolute accuracy, relative accuracy and measurement noise. Absolute accuracy is here defined as the deviation of a measurement from the true state of the system under measurement. Relative accuracy is here defined as the deviation of the shape of a curve formed by a vector of measurements from that of a vector of the corresponding true physical states; this is influenced by sensor linearity and drift and is insensitive to an error offset term or an error scaling factor. Measurement noise is here defined as the random deviation of one measurement from another given a constant physical state in the system as caused by the combined contribution of environmental and internal noise sources.

### 4.5.1 Relative Accuracy

A sensor’s relative accuracy is the most important performance metric for damping technology evaluation. Estimates of bandwidth, natural frequency and damping factor rely on an accurate representation of the frequency response curve, but are insensitive to absolute accuracy; this is illustrated in Figure 13.
Figure 13 - Estimates of damped natural frequency and 3dB frequencies are invariant to a constant offset error term or a scaling error term. Therefore bandwidth, damping factor and quality factor performance metrics are insensitive to linear measurement errors.

4.5.2 Absolute Accuracy

Absolute accuracy contributes to the precision of peak attenuation measurements. Within CP7, this measurement requires a comparison of the peak response of the beam with the unfilled damper cavity to that of a particle damped beam. Unlike damping factor, this performance metric is sensitive to how closely two sensor systems are matched. As can be noted from Equation 1, differences in an error offset term or error scale factor will contribute inaccuracy in peak attenuation measurements.

\[
\alpha_{ERROR} = \frac{\max|H_1|}{\max|H_2|} \times \left(\max(e_{OFFSET,1} + e_{SCALE,1} \times |H_1(f)|) - \max(e_{OFFSET,2} + e_{SCALE,2} \times |H_2(f)|)\right)
\]

Equation 1 – Peak attenuation parameter sensitivity to offset and scale errors
Where $\alpha$ is attenuation, $e_{OFFSET}$ is an offset error, $e_{SCALE}$ is an error in scale term, $H(f)$ is the true system transfer function and subscripts 1 and 2 denote the terms associated with the undamped system and a particle damped system respectively.

It should be noted that peak attenuation measurement precision also relies on how closely each baseline cantilever beam system is matched. While considerable efforts are undertaken to minimize dissimilarities in the physical systems, the constraints of a cubesat require the beams to be positioned differently with respect to the satellite’s center of gravity. This results in variance in moment of inertia for each beam system, ultimately causing irregularities in baseline system dynamics. Furthermore, minute differences in beam dimension, epoxy thickness and screw torque contribute further dissimilarities. While characterization of this variance helps to control experiment variables, some imperfection in the experiment results must be anticipated. The complexity versus performance trade off of the sensor system should take into account this imperfection. Choosing a sensor system capable of resolving measurements beyond what is controlled by the physical experiment creates complexity with no overall performance benefit.

4.5.2 Measurement Noise

Measurement noise contributes error to both absolute and relative accuracy. The magnitude of this contribution can be reduced either by directly minimizing the level of noise or by invoking stochastic properties to reduce noise through techniques such as oversampling; the later of which assumes the noise is uncorrelated, an assumption that is generally accurate.
4.6 Sensor Selection

4.6.0 Initial Technology Considerations

The sensor technologies identified as being suitable for measuring cantilever beam motion within CP7 include laser vibrometry, capacitive sensing, hall effect sensing and accelerometers.

While laser vibrometry or capacitive sensing presents the most accurate measurement options, offering resolutions within the nanometer range, they also present the most complexity. No COTS solutions for these technologies are found to be available in a form factor suitable for a 1U cubesat. Therefore a custom build would be required, both cases requiring significant manpower and financial resources. Furthermore, the accuracy offered by these technologies is deemed to surpass the physical system’s degree of control over variables, rendering much of the performance superfluous. This unfavorable complexity versus performance trade off rules out their viability in CP7.

4.6.1 Ratiometric Hall Sensor Consideration

Ratiometric Hall effect sensors, capable of outputting a voltage linearly proportional to an incident magnetic field, are readily available as small, low power, COTS integrated circuits. When positioned such that the sensitive axis of the sensor is perpendicular to the magnetized axis of a permanent magnet, the magnitude of the magnetic moment incident on the Hall sensor is approximately linear in the region halfway between the north and south pole when the distance separating the magnet and hall sensor is small. This configuration, as illustrated in Figure 14, offers a potential contactless solution to measuring cantilever beam displacement. By choosing small
magnets and alternating their orientation, it is thought that stray magnetic fields could be mitigated and this implementation could be made suitable for a cubesat.

![Cantilever Beam With Tip Mass](image)

**Figure 14 -** A rendering of a Hall Effect sensor based displacement measurement configuration. The blue arrows designate the magnet polarization and hall sensor sensitivity. As the cantilever beam oscillates the incident magnetic field varies linearly, the hall sensor transduces this into a voltage proportionate to the beam’s displacement.

A proof of concept system is built to evaluate this Hall sensor configuration. A Samarium Cobalt (SmCo) permanent magnet affixed to a cantilever beam is positioned in proximity to an Allegro A1392 ratiometric linear Hall effect sensor mounted to a printed circuit board (PCB). The cantilever beam is actuated using the piezo actuator described in Section 4.3. A Michelson interferometer is set up to measure the displacement of the beam through the use of a small retro reflector in the same planer position as the hall sensor. This serves as a “true” measurement of position, ideally accurate to 316.4 nm, or one half of the wavelength of the Helium Neon (HeNe) laser used. Over the course of one half cycle of the beams displacement, an oscilloscope is used to simultaneously capture the Hall sensor’s output and the interferometers fringe pattern as transduced by a photodetector. An annotated photograph of this set up is presented in Figure 15.
Figure 15 - An annotated photograph of the interferometer used to calibrate the Hall sensor. Hall sensor output is compared to the laser fringe pattern to measure sensor linearity and determine the voltage over displacement scale factor.

A plot of displacement as measured by the interferometer versus the Hall sensor voltage, reproduced in Figure 16, confirms a high degree of linearity. The plot suggests this configuration is capable of micrometer resolution over a range of approximately half a millimeter, indicating a range sufficient to achieve the specified sensitivity requirements.
Further testing of the Hall sensor configuration reveals a serious design weakness. The neutral position of the cantilever beam relative to the hall sensor would come out of alignment with no apparent cause. Left uncompensated, this drift introduces significant error in the relative accuracy of sensor measurements. Worst yet, this offset misalignment reaches such a severity as to cause the measured response of the cantilever beam to hit the Hall sensor’s rail, rendering the collected data useless. It is thought that this alignment drift is a product of different thermal expansion properties in the aluminum beam and the bonded piezo ceramic causing the beam to bend as environmental temperature varies, similar to how a bimetallic strip operates within a thermostat. This indicates the design flaw would become more serious in orbital environments.
Potential solutions to the Hall sensor alignment drift involve dynamically correcting the alignment through mechanical means. This could be accomplished either through a micro positioning stage capable of shifting the hall sensor, or the application of a DC bias voltage to the piezo actuator such that the static position of the cantilever beam could be adjusted. Either approach significantly increases system complexity and introduces additional failure modes, rendering the Hall sensor solution complexity versus performance unfavorable for CP7 instrumentation.

4.6.2 Accelerometer Selection

The final technology identified as a potentially viable sensor solution is an accelerometer. This sensing method was first considered unfavorable, as it requires trailing wires from the cantilever beam tip which pose the risk of interfering with beam dynamics. However, because an accelerometer is insensitive to neutral position, it would not suffer the alignment drift shortcomings of the Hall sensor implementation. This performance advantage is deemed worth the added complexity of a low interference wiring harness design.

Two different accelerometer types suitable for vibration analysis are available. Piezoelectric based accelerometers are widely used for industrial monitoring. As such the COTS versions are available in sturdy hermetically sealed packages which are deemed too large and massive for implementation within CP7. Instead, a survey of suitable devices focuses on microelectromechanical system (MEMS) capacitive sense type accelerometers which are available in small integrated circuit packages suitable for integration on CP7 cantilever beams.
The category of MEMS capacitive sense type accelerometers can be subdivided into two different grades identified by a large price discontinuity, here designated by the nomenclature high end and low end. Silicon Designs, Inc model number 1221-010\textsuperscript{[44]} is identified as the most suitable high end option and STMicroelectronics model number LIS244ALH\textsuperscript{[45]} is identified as the most suitable low end device. In small quantities these options have a price discrepancy factor of approximately 23.

The key accelerometer performance metrics considered in the comparison of these two devices include nonlinearity, bandwidth, full scale range, power consumption, sensitivity and acceleration noise density; these values, as specified in the respective data sheets, are presented in Table 1.

<table>
<thead>
<tr>
<th>Performance Metric</th>
<th>STMicroelectronics LIS244ALH (low end device)</th>
<th>Silicon Designs, Inc 1221-010 (high end device)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical Nonlinearity ($NL$)</td>
<td>.5</td>
<td>.4</td>
<td>%</td>
</tr>
<tr>
<td>Bandwidth ($BW$)</td>
<td>1000</td>
<td>1000</td>
<td>Hz</td>
</tr>
<tr>
<td>Full Scale Range ($FS$)</td>
<td>6</td>
<td>10</td>
<td>g</td>
</tr>
<tr>
<td>Power Consumption ($P$)</td>
<td>2.24</td>
<td>40</td>
<td>mW</td>
</tr>
<tr>
<td>Sensitivity at Full Scale ($S$)</td>
<td>220</td>
<td>400</td>
<td>mV/g</td>
</tr>
<tr>
<td>Noise Density ($e$)</td>
<td>50</td>
<td>7</td>
<td>$\mu g/\sqrt{Hz}$ RMS</td>
</tr>
</tbody>
</table>

Table 1 - A trade study of two accelerometer devices considered. These devices are selected as the best representatives of two technology groups separated by a large price discrepancy.

An inspection of Table 1 reveals the high end device provides significantly higher sensitivity at a greater full scale range with a much lower noise density then the low end device. This comes with the cost of higher power consumption.

Before making a selection, it is important to understand the involved performance versus cost trade offs. Noise Density can be equated to the minimum peak acceleration that can be detected by the device:
\[ g_{\text{min}} = e \times \sqrt{BW} \times \sqrt{2} \]

Equation 2 – Acceleration measurement noise floor

This gives 313.1µg and 2236.1µg for the high and low end devices respectively. By equating device sensitivity, the signal chain performance needed to resolve these g levels can be derived:

\[ V_{\text{MIN, SIGNAL}} = g_{\text{min}} \times S \]

Equation 3 – Determination of signal level needed to resolve minimum acceleration

Giving 125.24µV and 491.94µV as the minimum signal level for the high and low end devices respectively. This means the high end device theoretically can resolve acceleration levels approximately seven times smaller than the low end device but requires an overhead of a supporting signal chain approximately four times more sensitive to achieve this performance.

Weighing the price and power requirement difference with signal chain complexity, it is decided the added performance of the high end device is not worth the added system complexity and cost. Therefore the low end option, the STMicroelectronics LIS244ALH is selected for CP7. This device has additional features outside the requirements of CP7 instrumentation that can be considered a bonus. These include a self test feature, dual axis sensitivity and a selectable full scale range of 2g and 6g. Most noteworthy, the selectable full scale range allows the signal to noise ratio to be increased by a factor of three for low level accelerations.
Figure 17 - A photograph of the accelerometer selected for CP7 instrumentation. This analog output MEMS device offers sensitivity in the $\mu$g range over two axes.

### 4.7 Data Acquisition System

#### 4.7.0 Overview of Data Acquisition Options

The data acquisition system within CP7’s instrumentation consists of two major subsystems, the generation of a forcing function for the system input and the method of collecting the raw data needed to determine the system’s magnitude output. While several possible implementations are valid for the analysis of a linear system, the nonlinearity of a particle damped system restricts options\[46].

Particle damper dynamics include hysteresis and sensitivity to initial conditions. Therefore a particle damped system’s frequency response to a transient force, such as an impulse function, will be dissimilar to that achieved from a sine dwell or a random input. For this investigation, steady state response is of greater interest than transient response.

For a particle damped system, a stationary random input consisting of white noise band limited to the frequency range of interest can be assumed to produce a steady state, stationary random output after enough time has passed for transients to die off. Therefore, a viable data acquisition technique would involve applying a band limited random input to a cantilever beam’s piezoelectric actuator and recording a time history of
the output. The discrete time Fourier transform (DFT) could then be used to compute the cantilever beams output spectral magnitude. If a DFT is also performed on the random input, or if the random input is well characterized, the magnitude frequency response of the system could then be computed by taking output over input.

![Figure 18 - A representation of a sampled random output signal. A Discrete Fourier Transform of these data points gives the system’s frequency response.](image)

An alternative approach to analyzing the steady state response of a particle damped system involves a procedure in which a constant amplitude spectrally pure sinusoid stepped in frequency is applied to a cantilever beam’s piezoelectric actuator. For each frequency increment the system response is measured and recorded after transients are allowed to die off. The analysis conducted for each measured response can be a simple peak detection operation or a DFT. The DFT analysis option combines the complexity of each data acquisition approach, but gives knowledge of harmonic and intermodulation frequencies present in the nonlinear systems\cite{46}, where as the accuracy of the peak detection operation assumes that the contribution of the first order frequency response function (FRF) is much greater than the higher order functions.
Figure 19 - A representation of a sinusoidal waveform overlaid with a sampled peak detector. This data acquisition process performed over a sine dwell gives the means to directly measure a system’s magnitude frequency response.

The availability of multiple analysis techniques necessitates an investigation of complexity versus performance. A commonality within the majority of the options is the assumption of the ability to perform a DFT computation. Therefore, a determination of the feasibility of performing a DFT is prudent.

4.7.1 Discrete Fourier Transform Feasibility

The first consideration to performing DFT analysis is a selection of sampling frequency. If a cantilever beam’s baseline first mode frequency is 80Hz, then the stated requirements specify a 30 Hz to 130 Hz bandwidth of interest. From the Nyquist theorem it follows that a sampling frequency of at least 260 Hz is required to prevent aliasing. This however assumes an ideal brickwall anti-aliasing filter, which is not achievable. If a Butterworth anti-aliasing filter is selected for maximum passband flatness then a 20 dB per decade roll off can be achieved for every filter order\(^{[47]}\). A 4\(^{th}\) order cascade of Sallen Key filters can be achieved using a dual op-amp package, which is a reasonable investment in power and printed circuit board area. By selecting a cut off frequency of 150 Hz, to give overhead from the maximum 130 Hz signal of interest, 80 dB attenuation
of noise can be expected at 1.15 kHz. Choosing a sampling rate twice this, of 2.3 kHz, guarantees no noise above this level will alias, assuming circuit ideality. This is a reasonable rate for a low power 12bit A/D converter, which can achieve a maximum signal to noise ratio of 74 dB\(^{[47]}\). To further increase signal to noise ratio, a digital filter with a more ideal brickwall characteristic can be implemented after A/D conversion. At this stage the signal stream can then be digitally decimated to an equivalent sample rate of \(2 \times 150 \text{ Hz} = 300 \text{ Hz}\) to reduce future computational or downlink requirements.

The next consideration is DFT window selection. Because microgravity particle damped dynamics are unknown, the experiment must produce data suitable for system identification; it follows that the DFT should have a high frequency resolution\(^{[48]}\). However, because the experiment is also an evaluation of particle damper efficiency, accurate peak attenuation figures are also desired; this drives requirements for DFT amplitude accuracy. Conflicting requirements therefore exist for the chosen windowing function, specifically both a narrow mainlobe and small sidelobe\(^{[49]}\).

A compromise to conflicting window requirements is the selection of a flat top window for maximum amplitude accuracy and then compensating for poor sidelobe attenuation by increasing the amount of samples available for the DFT\(^{[50]}\). The HFT90D window developed in Reference 50 offers a maximum amplitude flatness of 0.0450%. This comes at the expense of a mainlobe width of five frequency bins. Frequency resolution as related to mainlobe width \(W_{f, \text{bin}}\) and sampling rate \(f_s\) can be computed as follows\(^{[49]}\):
\[ f_{\text{resolution}} = \frac{f_s \times W_{f_{\text{bin}}}}{N_{\text{samples}}} = \frac{300 \text{Hz} \times 5}{N} \]

Equation 4 – DFT frequency resolution sensitivity to windowing function mainlobe width

To achieve a frequency resolution of the stated 1/8Hz requirement, this amounts to 12,000 samples. Increasing the number of samples does not increase the dynamic range resolution, which is limited to the specified -90.2dB peak side lobe of the HFT90D filter. It should be noted that increasing the number of samples to a power of two may be advantageous to optimize the eventual fast Fourier transform (FFT) computation.

The next consideration of a DFT computation is the reduction of the variance in the frequency bins. This can be accomplished by applying the window function to overlapping segments of the data stream, performing a DFT on each result and averaging the results. This is a process known as the Welch method. In order to maintain frequency resolution, each overlapped segment must have a length of 12,000 samples. In this process standard deviation is reduced by a factor of \(1/\sqrt{M}\) where \(M\) is the number of segments\(^{[50]}\). A factor of five reduction requires 25 segments. Assuming the ideal overlap percentage of 76.0% for the HFT90D, this amounts to \(12,000 + 25 \times (12000 \times .76) = 240,000\) samples required.

At 12 bit A/D resolution the 240,000 samples required for each DFT amounts to 352 kilobytes of data. Compounding this by five amplitude levels and three beam systems for input and output gives a total data requirement of 10.5 megabytes for minimum mission success. Given an expected downlink of 864 kilobytes per day, this amount of data would require 12.2 days to achieve minimum mission success. Based on previous mission experience, where risk scales with required functional in orbit time, it is decided this is an unacceptable data collection process.
An alternative approach to DFT computations within the CP7 mission would involve performing FFT computations on board the satellite and downlinking only the key parameters of each spectrum. This would significantly compress the relevant data allowing a much faster mission. This however comes at two costs.

The first cost to such compression is a loss of information. Inaccessibility to raw data reduces investigator’s ability to confirm findings or explain anomalies. While this is a significant cost, given the current data limitations of a cubesat, it must be accepted. The second cost involves the complexity of performing the DFT computations onboard. The accurate computation and multiplication of window function values as well as the actual FFT process requires a system that can support floating point computation or the careful design of a scaled integer digital signal processing system.

4.7.2 Discrete Fourier Transform versus Magnitude Detection

Given the inevitable loss of raw information, the DFT data acquisition approaches can be directly compared to the sine dwell, magnitude peak detection approach. Through the use an analog peak detector, a low power, low complexity microcontroller can directly measure a system’s amplitude response at iterated 1/8\textsuperscript{th} Hz steps without strict sampling rate or timing requirements. The raw data from this process can be directly downlinked without any need for further onboard compression. This represents a significant decrease in system complexity.

A comparison of system performance is less straight forward. For a linear system a sine dwell approach offers greater frequency response measurement resolution than a DFT approach which is intrinsically limited in resolution by spectral leakage. However,
because a particle damped system is nonlinear, one can not assume the system’s response
to a tone is spectrally pure, therefore a peak detection method suffers inaccuracy related
to the nature of the system’s nonlinearity. Discussion of this complexity versus
performance trade off with supporting system’s dynamics engineers resulted in a
compromise involving a system capable of measuring both signal peak and valley
magnitude as well as the detection of the system’s primary frequency component.
5 Low Level Design

The following section includes an overview of the design methodology and development of CP7’s payload electronics on the component level. To aid in the reader’s comprehension, segments of the related schematics are included within the text. Complete schematics are available in Appendices B, C and D.

5.0 Sensor Module

5.0.0 Sensor Module Overview

The small size of the MEMS accelerometer selected for measuring cantilever beam motion enables supporting signal processing circuitry to be integrated within a PCB affixed to each cantilever beam tip. This allows analog front end processing and D/A conversion to be performed local to the sensor, negating the need for shielded cabling trailing from the beam tip. Instead, small gauge single strand wire can be used with minimal effect to a cantilever beam’s dynamics. The resulting PCB, here designated Sensor Module (SM), takes on a unique geometry driven by the physical constraints of the cantilever beam and structure configuration. A photo of the sensor module is presented in Figure 20.
The required SM functionality involves peak and valley detection of the output of an accelerometer and the D/A conversion thereof. It also must output a signal suitable for frequency measurements. Under this basic functionality, the primary focus of the SM design is maximal signal integrity. This involves a combination of special considerations in power supply, signal chain, component choice and layout. Secondary design efforts include the addition of non required functionality that is deemed to have a low implementation cost but significant performance contribution.

5.0.1 Power Rails

One of the first considerations in the SM design is the supply rails. The LIS244ALH accelerometer (U8) output is ratiometric with the device’s power supply, which has a nominal value of 3.3V. This means any noise, temperature drift or load dependence in the supply rail will directly effect the accuracy of the accelerometer’s output. U9, A LTC6652 precision low drift, low noise buffered reference IC is selected.
to provide an isolated voltage supply to the accelerometer. This gives a rated +/-0.05% 3.3V accuracy and a temperature drift of less than 5ppm.

Figure 21 - Schematic of Sensor Module power regulators. Separate LDO’s provide isolated analog and digital power rails. U9, a precision low drift voltage reference provides a stable output onto which the accelerometer output can be referenced.

The LTC6652 has a voltage dropout requirement of .3V, requiring a supply of at least 3.6V. In order for this circuitry to operate independently of battery levels, (within limits) a buck/boost converter is required. Due to switching noise concerns this is located on the Payload Command and Data Handling (PC&DH) board to minimize conducted and radiated interference to the sensitive analog signals within the SM. To provide a low
ripple, low noise supply to both the LTC6652 voltage reference as well as the remaining components on the SM, the output of the switching supply is applied to two low dropout regulators (LDO) located on the SM. Separate LDO’s, U15 and U16, are used in a technique to isolate analog and digital power supplies to reduce conducted noise sourced from high frequency digital data lines[51]. Similarly, separate analog and digital ground planes are employed. The layout of these power and ground planes is arranged in a geometry intended to reduce current loops that can cause inductively coupled noise[52]; a screen shot of this layout is provided in Figure 22 and Figure 23 respectively. Power supply decoupling capacitors of various values are located near the supply pins of each component to further reduce current spikes and to filter supply rail noise[51].

![Figure 22 - Layout of Sensor Module power planes. Separate analog and digital planes help isolate digital switching noise from the sensitive analog signal chain. A third power plane sources the accelerometer reference voltage.](image-url)
Figure 23 - Layout of Sensor Module ground planes. Separate analog and digital planes help isolate digital switching noise from the sensitive analog signal chain. Each plane is shunted to the header’s ground through zero ohm resistors, providing a single point return path.

The output of the LDO’s is selected for 5V. This allows low power components to be utilized in the SM design, yet gives sufficient overhead for signal dynamic range and peak detector operation. A single ended supply is chosen to reduce the required amount of LDO’s, power supply decoupling capacitors and power planes within the restricted layout area of the SM. This however requires the generation of a mid supply reference voltage, so the accelerometer’s AC signal can be offset from the ground. A 2.2V offset voltage (V_OFFSET) is produced by the filtered resistor divider formed by R15, R14 and C33 and buffered by U2A, an Analog Devices AD8572 Op-Amp chosen in part for favorable 1/f (flicker) noise characteristics. Using large, low impedance trace width and applying V_OFFSET to a differential input A/D converter at the end of the analog signal chain relaxes temperature drift and precision requirements of V_OFFSET.
Figure 24 - Schematic of the Sensor Module offset voltage source. A buffered resistor divider produces a 2.2V reference used to offset the accelerometer output. This offset is referred to an A/D converter’s differential input, reducing the system’s sensitivity to component temperature drift.

5.0.2 Analog Front End

The next consideration in the SM design is the front end analog stage. The LIS244ALH accelerometer uses a technique to reduce low frequency noise called correlated double sampling which involves a switched capacitor topology similar to that used for autocorrecting offset nulling in precision operation amplifiers\cite{45,53}. The high frequency noise contribution of the associated clock as well as the resonant frequency of the MEMS mechanism necessitates the need for low pass filtering in the first stage of the analog front end. Per the LIS244ALH data sheet recommendations, this is performed by a simple first order RC filter formed by the resistive output impedance of the LIS244ALH and an external capacitor. The nominal output resistance of the LIS244ALH is 110kΩ with an unfortunate tolerance of +/-20%. This reduces the effectiveness of any attempt to analytically account for magnitude and phase distortion of the filter. By choosing a 1.5nF capacitor, a nominal 1kHz cutoff frequency is selected with sufficient headroom such that the deviation in the magnitude response over the
frequency range of interest is minimal. Per Equation 5, this gives a magnitude uncertainty of .7% for the worst case frequency of 130Hz.

\[ |H_{FILT}| = \left| \frac{1}{1 + j \cdot 2\pi f \cdot 110k\Omega \cdot (1 \pm .2) \cdot 1.5nF} \right| \]

Equation 5 – Acceleration magnitude sensitivity to output impedance tolerance

Past this initial filtering, more aggressive filter stages are not pursued. This reduces the need for magnitude and phase characterization and reduces the overall group delay, which adversely slows steady state detection and increases overall experiment time.

Figure 25 - Schematic of the first stage of the Sensor Module analog front end. The accelerometer output is filtered through a first order filter formed by the device’s resistive output and external capacitors. Analog switch, U1, selects the accelerometer axis to measure.

The next stage in the front end analog circuitry is an analog switch, U1, used to change the axis of the acceleration measurement. While this is not a required feature, by
choosing a device with low harmonic distortion characteristics it adds considerable
capability to the SM with minimal cost.

The common terminal of U1 is then fed to a buffering Op-Amp. This Op-Amp, U2B, which shares a package with the reference voltage buffer, offers key characteristics including low flicker noise and high input impedance. The output of the U2B is fed to an AC coupling capacitor C31 and summed with the V_OFFSET voltage through R13. This gives the signal a known offset voltage which can later be removed precisely through the use of a differential input A/D. The impedance of this network can be assumed to act as a simple first order high pass filter by assuming sufficiently low output impedance of both U2A and U2B and sufficiently high input impedance of the next stage formed by an instrumentation amplifier, U10. By choosing 10uF and 100kΩ for C31 and R13 respectively, a cut off frequency of .16Hz is achieved. Therefore the magnitude and phase effect of the filter on the 30Hz to 130Hz bandwidth of interest can be negated.
Figure 26 - Schematic of the second stage of the Sensor Module analog front end. The filtered accelerometer output is buffered by U2B. The signal is then AC coupled and referred to a known DC offset provided by U2A. Instrumentation amplifier U10 and digital potentiometer form a variable gain stage capable of amplifying the signal between a factor of 1 and 257.

The accelerometer signal, now referred to V\_OFFSET is fed to U10, a Texas Instrument INA333 instrumentation amplifier. Combined with U3, a 256 stage digital potentiometer with low temperature drift characteristics, this circuitry is capable of low noise precision dynamic signal amplification within a range of 1 and 257 multiplication. Closing the loop with a microcontroller housed on the Payload Command and Data Handling (PC\&DH) board allows an automatic gain control algorithm to be implemented. This serves two purposes. First, the amplification allows signal to noise ratio in the remaining portion of the signal chain to be maximized. Second, by controlling the amplitude of the signal, it reduces the dynamic range that the peak detection stage must resolve, allowing the peak detector’s response to be better optimized. Further details of the automatic gain control algorithm are provided in Section 5.4.1.
The final stage of the analog front end circuitry, formed by C16, R2 and U14 provides a 180 degree phase shifted replica of the amplified signal. This inversion allows peak detection circuitry to measure signal valley crests within a single supply system.

A Schmitt trigger formed by R4, R3, R6 and a comparator U4 converts the amplified accelerometer sinusoidal waveform into a square wave of an identical primary frequency. This is used in frequency and phase detection circuitry located on the PC&DH board, which is described further in Section 5.2. A hysteresis width of .75V is chosen for two reasons. First, it gives the circuit noise immunity; it is found that too small of a hysteresis band results in instability caused by a positive feedback loop formed by the comparator’s switching noise coupled into the V_OFFSET line. Second, it gives measurements of the primary frequency component immunity from signal distortion expected to exist as a result of particle damper nonlinearities.
5.0.3 Peak Detectors

The next signal chain stage in the SM is the peak detection circuitry. The design goal of this stage is to accurately capture the magnitude of the accelerometer’s amplified output over a single cycle. Any delay in this measurement is compounded through the shear number of experiment iterations, resulting in a significantly slower experiment. For this reason, slower magnitude measurement techniques such as RMS or heating power detectors were disqualified.

The peak and valley detectors differ only in the relative inversion of their respective input signal. These identical circuit blocks are built around U13, an AD8574 quad Op-Amp package. The peak detector using U13A and U13B will be described; the design of the second peak detector using U13C and U13D can be directly compared.

An ideal peak detector is a nonlinear circuit capable of tracking and holding a signal’s maximum value until the circuit is reset. A design based on the “Overall Feedback Peak Detector” presented in Reference 54 is used to approach this ideality. The first stage of the peak detector is U13A, an Op-Amp that operates much like a
comparator, where the inverting input of the Op-Amp is connected to the peak detectors output. When the input signal applied to the positive input is higher than the peak detectors output, U13A swings upwards. In the reverse condition U13A swings low and is clamped to the peak detector output minus a voltage drop of the Schottky diode D4A (about .1V). This clamping prevents U13A from saturating; this reduces recovery time and improves system speed. Configuring the signals automatic gain control such that the maximum signal value is no more than 4.1V gives U13A plenty of headroom to prevent positive rail saturation.

Figure 29 - Schematic of Sensor Module peak detector. This circuit captures and holds the highest value of the amplified accelerometer signal. MOSFET’s Q2(1,2) provide the means in which the peak detector can be reset. An identical circuit block captures the peak of the inverted accelerometer signal, forming a valley detector.

The next stage in the peak detector signal chain is the half wave rectification action provided by D4B and D6. The midpoint of this cascade is bootstrapped to the peak detector output through R19. This means the voltage drop across D6 is nearly zero,
which reduces leakage current in the peak detector and improves droop performance. This is further decreased through the selection of, D6 a very low current leakage diode.
Choosing a Schottky diode for D4B reduces the combined voltage drop of the diode cascade.

The voltage hold operation is enabled by C17, which retains the signal level after the rectifying diodes switch off. It is found that the capacitive load this presents to the signal chain causes poor overshoot performance resulting in artificially high peak detection levels. This is resolved by the addition of R17, which isolates the capacitive load in a manner similar to the “Out Of the Loop Compensation Method” described in Reference 55. The value of R17 is selected empirically, providing a nearly ideal deadbeat response in the peak acquisition operation within the signal level restricted by the automatic gain control. To improve droop performance, C17 is a Polyethylene Naphthalate film type capacitor selected for very low parasitic leakage current. A fairly large capacitance value of 0.1\(\mu\)F is selected to reduce the effect of any leakage current on droop performance. While this significantly slows the peak detector speed, the circuit is found to operate sufficiently fast to capture one cycle amplitude levels within the signal bandwidth of interest.

The peak detector feedback loop is completed by U13B, which provides a high impedance buffer to the voltage stored on C17. U13B’s output is fed back to U13A to complete the loop, and is made available as the peak detector output.

To reset the peak detector, the charge stored on C17 must be drained. This is accomplished by the MOSFET cascade formed by Q2-1 and Q2-2. Application of a logic high signal on the RST line causes the MOSFET’s to switch on, quickly shunting C17 to
the ground. Similar to the diode cascade, leakage current is minimized through a bootstrap resistor, R18, such that the voltage drop across Q2-1 is minimal. The resistance provided by R17 and an internal short circuit current limit within U13A prevents overcurrent conditions during the reset pulse.

Peak detector Op-Amp selection requires careful consideration of several performance metrics. Because the output of the peak detector is a DC signal with high accuracy requirements, the Op-Amp should not contribute excessive flicker noise and Op-Amp offset voltages should be suitably low. The built in autocorrection stages of the AD8574 provide notably low DC noise levels, contributing only 2.0μVpp, as well as a low offset voltages, typically only 1.0μV. Peak detection related Op-Amps must also have very low input bias current, such that the hold capacitor can maintain its charge with low droop. The AD8574 requires only 10pA (typical rating) of input bias current. Op-Amp dynamic performance must also be considered. While the signal to be detected is relatively low in frequency, the Op-Amp should have a suitable slew rate for the fast acquisition of peaks and fast slope reversal such that the true signal peak can be captured. The AD8574 nominal slew rate of .5V/µs is empirically deemed to provide sufficient performance.

5.0.4 Digital Circuitry

Within the SM, digital circuitry is required to support the analog signal chain functionality. This includes amplifier gain selection, A/D conversion, and the generation of various logic levels needed to select measurement operations. To minimize the
amount of data lines, all digital components are selected to operate on an I²C two wire bus.

Figure 30 - Schematic of Sensor Module digital interface. An I²C GPIO expander, U5, provides the means in which the peak detectors can be reset among other Sensor Module functionality.

U5, a 4 bit I²C GPIO expander is configured as output only and is employed to control SM measurement operations. Logic signal AXIS_SEL controls the analog switch U1, ultimately choosing which axis of acceleration to measure. The RST signal controls the reset of the peak detectors. This signal is pulled down by R20, such that the SM enters the more power conservative peak hold state upon power up. FS_SEL and ST signals interface with the LIS244ALH accelerometer after being level shifted through the action of R5, R16 and D3. FS_SEL, selects the accelerometer full scale; either 2g with a 33/50 V/g nominal sensitivity or 6g with an 11/50 V/g nominal sensitivity. Assertion of the ST logic level causes the accelerometer to enter a self test mode where an electrostatic force is internally generated, deflecting the MEM’s component to produce a predictable output. If this output is found to be outside an acceptable range then it can be determined the accelerometer is out of specification. This feature can be used to
contribute to measurement quality insurance during the course of payload operations. C41, in conjunction with R16 creates a low pass filter that limits the logic slew rate to a level specified by the LIS244ALH data sheet. A/D converter, U11, taps into the accelerometer output before AC coupling, such that this static signal can be measured.

A 16 bit A/D converter, U6, is the primary means in which the sensor module measurements are converted to the digital domain. This integrated circuit, a Texas Instrument’s ADS1115, provides two separate differential inputs. This allows both peak detectors to be read with respect to the 2.2V offset voltage, which each signal is referred to. Within the SM, the ADS1115 is configured to apply a factor of two gain to the differential input, providing a full scale differential signal range of +/-2.048V. This equates to a maximum peak detector value of $2.2V + 2.048V = 4.248V$, a limit observed in the parameters of the automatic gain control algorithm. For this +2.048 full scale range, a quantization level of $2.048/2^{15}$ V or $62.5\mu V$ is achieved. The acceleration quantization level this achieves is dependent on the gain setting in the analog front end and the full scale setting of the accelerometer; for a worst case gain of one, and the 6g full scale accelerometer setting, this equates to acceleration quantization levels of $284\mu g$. This is considerably reduced for the measurement of small acceleration signals which are measured under the 2g scale and amplified in the analog front end.

Supplementing the ADS1115, is U12, and U11. U12 is a 12 bit A/D capable of higher sampling rates. This A/D taps into the amplified acceleration signal prior to the peak detector such that the acceleration waveform can be quantized. Within the selected data acquisition scheme this is not a required feature, but offers the ability to collect time history data that can contribute to confirmation of proper experiment operation. U11 is a
low speed 16 bit A/D that taps into the accelerometer output before the signal is AC coupled, this allows the system to measure the accelerometer self test output for diagnostic purposes.

The final digital component on the SM is an I²C temperature sensor. This contributes knowledge of the operating conditions of the experiment, which may be useful for explaining anomalies in either the mechanical baseline system or the particle damper.

Figure 31 - Schematic of Sensor Module analog to digital converters. A dual channel differential input A/D, U6, provides high resolution conversion of peak detector output. Additional A/D’s including temperature sensor U7 provide the means to confirm proper Sensor Module operation.
5.0.5 Calibration

While the sensitivity of the LIS244ALH accelerometer is relatively invariant over time and temperature, its nominal value can only be guaranteed to within +/-5%[^45]. Similarly, the AD5245 digital potentiometer used to set the gain of the analog front end offers low temperature sensitivity but a high resistor tolerance of +/-30%. Therefore it becomes necessary to measure the true values of these components such that measurements can be scaled accordingly.

To calibrate the digital potentiometer, U1 is left unpopulated so that the accelerometer is isolated from the rest of the signal chain. A test lead is soldered to the noninverting input of U2B and the output of U10. A sinusoidal signal with a DC offset is applied to the first test lead and a high accuracy benchtop multimeter is used to measure the RMS voltage at each test lead. Dividing the output measurement over the input measurement gives the true gain accomplished by the digital potentiometer, U3, and the instrumentation amplifier, U10. This process is repeated for every digital potentiometer setting of interest, forming a look up table that can be used in raw data processing performed on the ground.

Calibration of the accelerometer sensitivity requires the application of at least two known acceleration values. The linearity between these points and through the full scale of the accelerometer is guaranteed to within .5% by the LIS244ALH data sheet, which is accepted as being sufficient for the purposes of this mission. Therefore, a simple calibration process is performed by aligning the accelerometer’s axis of interest parallel to the direction of gravity. This gives a positive 1g data point. Inverting the alignment gives a negative 1g data point. An accurate benchtop multimeter is used to measure the
DC output of the accelerometer for each orientation. Proper alignment of each orientation is confirmed by rotating the accelerometer along the sensitive axis and observing consistent output values; this demonstrates that the surface used for alignment is level. Calculating the slope between the +1g measurement and the -1g measurement gives the accelerometers’ true sensitivity. This can then be applied to the data post processing to accurately relate measured voltages to acceleration.

The final SM calibration step involves the measurement of the hysteresis of the Schmitt trigger formed around the comparator U4. This is necessary to accurately analyze the frequency dependent phase shift of the cantilever beam system. This process is covered more completely in Section 5.2.4.

5.1 Piezoelectric Actuator Driver

5.1.0 System Overview

The Piezoelectric Actuator Driver circuitry must produce a spectrally pure excitation signal suitable for the data acquisition process selected in Section 4.7 and amplify this signal to a level suitable for the piezoelectric actuators selected in Section 4.3. To confirm proper operation and implement closed loop amplitude control necessary to maintain a flat frequency response, the Piezoelectric Actuator Driver must also be capable of measuring its output. This circuitry is laid out on a PCB which mates with the Payload Command & Data Handling (PC&DH) board. This configuration is represented in Figure 32.
Figure 32 - Annotated photograph of the payload electronics stack. The top board houses the Piezoelectric Actuator Driver circuitry. The lower board houses the payload Command and Data Handling PCB. This configuration helps isolate high and low voltage circuitry. The combined stack height is approximately .61”; the larger PC&DH PCB measures 3.25” on its side.
5.1.1 Excitation Signal Generation

The selected frequency response acquisition strategy requires the generation of a spectrally pure sinusoid with finely controlled frequency. This requirement is satisfied through circuitry centered on U8, an AD9833 SPI Direct Digital Synthesis (DDS) integrated circuit developed by Analog Devices. The AD9833 DDS contains a 28 bit phase accumulator which approximates a waveform in $2^{28}$ steps, meaning that over one period, a signal’s phase is quantized in $2\pi / 2^{28}$ levels, providing extremely fine frequency
The AD9833 then maps these phase values into sinusoidal amplitude values, ultimately outputting an analog signal with 10 bit resolution.

Figure 34 - Schematic of DDS signal generator used in the Piezo Actuator Driver. DDS U8 generates a high resolution sine wave approximation based on clock U11.

Supporting the AD9833 is a crystal controlled oscillator, U11, which provides the clock frequency of the DDS. A TXC 7W-16.000MBB-T 16Mhz CMOS output oscillator is selected for low phase jitter and high frequency stability. While a 1MHz clock is the rated minimum of the AD9833, choosing an oscillator frequency (F_{CLK}) larger than this improves phase jitter in the output signal, where phase noise is attenuated by a factor of

$$20\log(F_{OUT}/F_{CLK})$$

This sacrifices minimum frequency step size, which for the AD9833 is determined by $F_{CLK}/2^{28}$. For $F_{CLK} = 16$MHz, this equates to a minimum frequency step size of approximately .06Hz, which is well below the .125Hz frequency resolution specified in the mission requirements. A 3.3V LDO is dedicated to power the oscillator and the DDS through an isolated power and ground plane to help minimize conducted clock noise to surrounding analog circuitry.
Figure 35 - Schematic of DDS output buffer. This circuit buffers and AC couples the DDS output, which is incident on U7A’s input.

The DDS output is followed by analog circuitry that performs anti-imaging filtering and fine gain control. To simplify these operations and provide sufficient dynamic range, +/- 5V rails are supplied. A +5.4V source is produced by a buck boost power regulator located on the PC&DH board and further regulated to a clean 5.0V supply through LDO. A -5.36V source, also located on the PC&DH board, is produced by an inverting charge pump and further regulated to a clean -5.0V through LDO, U3.

The first stage of the analog circuitry is an AC coupling stage formed by the buffers U7A, U7B and C18. This centers the DDS signal on ground for further signal processing. This is followed by a 4th order low pass Butterworth filter chosen to attenuate DDS sampling frequency components while providing a maximally flat passband response. A 1 kHz cutoff frequency is chosen to provide a bandwidth much larger than the specified max frequency, yet gives sufficient headroom for sampling frequency attenuation. In the case of the AD9833, the sampling frequency ($F_S$) varies
with the primary output frequency \( F_{\text{OUT}} \) through a scale factor of \( 2^{10} \), or \( F_S = F_{\text{OUT}} \times 1024 \). For the worst case lowest frequency of interest at 30Hz, this gives a 30.72kHz sampling frequency. Assuming circuit ideality, this gives approximately 120dB of sampling frequency attenuation. A Sallen-Key filter topology is selected to implement the filter, based off of Op-Amps U7D and U7C. The quad Op-Amp package, U7, a Texas Instruments OPA4244, is selected for suitable bandwidth and low power operation.

![Figure 36 - Schematic of DDS output filter. A 4\textsuperscript{th} order cascade of Sallen-Key filters with a 1kHz cut off frequency performs anti-imaging filtering of the DDS sampled sine wave approximation.](image)

The DDS signal, now filtered, is applied to a fine gain stage. The first component of this stage is a resistor divider that can be enabled or disabled through the analog switch U4. Enabling U4 causes the initial signal to be attenuated by a factor of 2/5, as determined by R5 and R8. This low voltage mode allows the high voltage amplifier, which has a minimum gain of approximately 10.42, to output signals under 10Vpp. This is useful for the analysis of the undamped cantilever beam.
Figure 37 - Schematic of signal attenuation stage. A resistor divider attenuates the filtered DDS output which is incident on R5. Analog switch U4 enables or disable the resistor divider to toggle between normal and low voltage modes.

The next component of the fine gain stage is a fixed 1.5 gain formed by U23A and a variable gain amplifier formed by U23B and the 50kΩ 256 stage digital potentiometer U1. Cascaded, this gives a linearly variable pre-gain with an amplification factor between approximately 3 and 16 with 256 intermediate steps. Given an AD9833 nominal output of .612 Vpp, the fine gain circuitry can deliver an amplitude of approximately .49 Vpp to 3.92 Vpp over 256 steps in low voltage mode, or approximately 1.84 Vpp to 9.79 Vpp over 256 steps in normal mode.
Figure 38 - Schematic of signal fine gain stage. The filtered signal is applied to a cascade of gain stages, a fixed 1.5 amplification and a variable gain stage formed around digital potentiometer U1. Together this cascade achieves gains between 3 and 16 over 256.

5.1.1 High Voltage Amplification

The piezoelectric actuators are high voltage, low current devices. Bench experimentation has found amplitudes as high as 700Vpp are needed to excite 6g acceleration in a damped beam. Therefore a high voltage stage is needed to amplify the output of the fine gain stage.

The first consideration in the High Voltage Amplification stage is the source of the high voltage rails. The EMCO Q-Series regulators are identified as the sole source for small high voltage regulators suitable for implementation with the constraints of CP7. These regulators take on a cubic form factor with an edge dimension of .5”. The Q0-4 variation offers an output that is proportional to the input up to a 5V input and 400V output relation, sourcing as much as 1.250mA. Through the combination of two of these regulators, U29 and U30, +/- 400 volt rails are achieved.
Figure 39 - Schematic of high voltage converters. Two high voltage DC/DC converters supply high voltage rails needed for the high voltage amplification stage. The magnitude of this voltage is proportional to the input, up to +/-400V for a 5V input.

The next consideration in the High Voltage Amplification stage is the amplifier itself. In particular, this amplifier should have sufficiently high supply limits and small quiescent current. An APEX PA97 high voltage Op-Amp is identified as the only viable option, with a maximum supply voltage of +/-450 V and a typical quiescent current of .6mA. The implementation of the high voltage amplifier, U25, requires several special considerations. U25 is externally compensated with C57, a 10pF capacitor giving a gain bandwidth product of 1 MHz and a specified minimum gain of 10. Transient voltage suppression diodes, D6 and D7, are placed to protect the rails from power supply voltage spikes, and fast acting high voltage clamping diodes D9 and D8 protect the output from over voltage conditions that may result from any inductance on the load. Fast acting low voltage diodes D1 and D2 are placed to protect the amplifier from excessive differential input voltages. R17 serves a dual purpose of both decoupling the piezoelectric actuator’s capacitive load and offering a layer of protection against over current conditions caused by accidental shorts in testing. Feedback resistor R51 is fixed at 10MΩ, this high value is selected to conserve current resources in the high voltage circuitry. The physical form
factor of R51 is found to be an important parameter as well. R51 is selected as a quarter watt through-hole component, such that the body of the device can be physically separated from the PCB. This was found necessary, as a surface mount resistor cascade complement on a previous revision was subject to parasitic conduction through the PCB causing instability in the op-amp feedback loop. Low pass filters formed by R24 and the parallel combination of C20, C18, C26, C8, and their complements on the negative supply, help to reduce high voltage supply ripple, which can be significant under load.

![Schematic of high voltage gain stage](image)

**Figure 40 - Schematic of high voltage gain stage.** High voltage Op-Amp U25 configured as an inverting amplifier amplifies the sine wave up to 740Vpp in conjunction with the variable input resistor coarse gain stage.

The gain of the PA97 can take on three values, set by feedback resistor R51 and the input network formed by R5, R7, R9, R12, R14 and the two channel analog switch U5. Enabling various channels on U5 shorts out segments of the input resistor chain, effectively changing equivalent input resistance. Input resistor values are chosen such
that gains of approximately 10.42, 25 and 90.91 can be achieved; this forms the coarse gain stage.

Figure 41 - Schematic of coarse gain stage. Analog switch U5 shorts segments of the resistor cascade to alter the input resistance value and gain of the high voltage amplifier.

Cascading the coarse and fine gain stages gives high signal dynamic range as well as fine control over signal output. An inspection of Figure 42 reveals for a nominal DDS output of .612Vpp, high voltage amplification can vary from approximately 5Vpp to the maximum output of the PA97, which is approximately 30V less than the top rail. This equates to a maximum amplitude of approximately 740Vpp. Throughout this range an arbitrary output can be selected such that a maximum amplitude error of 2.66% occurs. This can generally be reduced by selecting the smallest possible coarse gain setting.
Figure 42 - Plot of input signal dynamic range. Through the selection of fine and course gain values within either the low or normal voltage mode allows the input signal to be amplified between 5Vpp to 740Vpp within 2.66%.

5.1.2 Output Measurement

Measuring the output of the high voltage amplifier serves two purposes. First it contributes to proper circuit operation confirmation and secondly allows for closed loop control of the output amplitude. Closed loop control largely eliminates component drift concerns, compensates for curvature in the magnitude frequency response, and through proper design of the control algorithm, minimizes the maximum error of the selected output amplitude.

The first stage of the circuitry responsible for measuring the high voltage output is a high impedance resistor divider formed by R16, R20, R23, R26, R27 and R28. The cascade of multiple components is implemented to minimize the voltage drop across each resistor, alleviating voltage rating requirements for the resistors. Values of this network are chosen to provide a voltage division factor of 200, such that the maximum output voltage of 740Vpp is reduced to 3.7Vpp. This divided signal is buffered by U15, a Texas Instruments INA118 instrumentation amplifier selected for dual supply capability and
high input impedance. The buffered signal is then fed into an analog front end and peak
detection stage nearly identical to that implemented on the Sensor Module. The principle
difference is the omission of the AD5245 potentiometer based variable gain stage. In all
other aspects, circuit functionality can be compared to the description found in Section
5.0.2 and 5.0.3.

Figure 43 - Schematic of output voltage divider. A high impedance resistor divider and buffer
produce a divided output that can be measured using low voltage electronics.

5.1.3 Piezoelectric Actuator Multiplexing

The final component of the Piezoelectric Actuator Driver circuitry is a high
voltage multiplexing stage capable of routing the high voltage signal to one of the three
cantilever beams. This is accomplished using a network of opto-isolator switches. U2,
U6 and U9 are normally closed devices, which shunt the piezoelectric actuator terminals
to ground. This prevents charge build up caused by the potential generated across the
piezoelectric transducers when under mechanical stress, such as launch vehicle vibration.
U24, U26, and U27 are normally open devices, which gate the high voltage signal to the desired piezoelectric actuator via the through-hole terminals J3, J4, J5.

The sequence required for selecting a piezoelectric actuator involves first enabling the respective normally closed opto-isolator such that the actuator terminals are no longer shorted to ground, then enabling the respective normally open opto-isolater such that the high voltage signal is applied to the desired piezoelectric actuator. This logic is achieved through U14, an I²C GPIO expander which is controlled by the microcontroller present on the PC&DH board.

![Figure 44 - Schematic of high voltage multiplexer. Opto-isolaters controlled by an I²C GPIO expander route the high voltage input signal to one of three piezoelectric actuators.](image)

### 5.1.4 Calibration

Because the Piezoelectric Actuator Driver is closed loop controlled, calibration of the gain stage is not required. Instead, absolute amplitude measurement accuracy is dependent on the accuracy of the high voltage resistor divider described in Section 5.1.2.
This involves removing R17 and applying a test sinusoidal signal generated by a function generator to the HV_SINE line. A high accuracy bench top multimeter is used to measure the RMS voltage at both this terminal and at the output of U15. The ratio of the two measurements gives the true voltage division factor. Knowledge of this division factor can then be used to adjust output amplitude settings accordingly. The ratiometric nature of the voltage divider coupled with the selection of low drift components contributes to consistent accuracy of this calibration as temperature varies.

The final calibration step involves the accurate measurement of the hysteresis band of the Schmitt trigger formed around U22. Just as with its counterpart on the Sensor Module, knowledge of the hysteresis trigger points is required for accurate phase measurements. This system and the calibration thereof is described in detail in Section 5.2.

5.2  Frequency & Phase Detection

5.2.0  System Overview

While the Direct Digital Synthesis (DDS) system on the Piezoelectric Actuator Driver board offers high frequency accuracy and the closed loop amplitude control gives knowledge of signal peak and valley values, direct measurement of the experiment input frequency contributes to the confirmation of proper system operation. Simultaneous measurement of the experiment output frequency similarly confirms the legitimacy of the magnitude response measurements, but also serves as an indicator of nonlinear frequency distortion.
Within the design process of the frequency counter circuitry, a method of measuring input to output phase shift is identified that presents minimal development investment. While system phase measurement is not a required feature in the CP7 mission, it offers a significant performance enhancement. System natural frequency can accurately be measured by identifying the inflection point within the phase response curve. Unlike estimates from magnitude response curves, this technique holds accurate for both viscous and hysteretic types of damping\textsuperscript{[57]}. Natural frequency can then be related to system mass through Hooke’s law:

$$f_{\text{natural}} = \frac{1}{2\pi} \sqrt{\frac{k}{m}}$$

\textbf{Equation 6 – Cantilever beam natural frequency relation to system mass}

Where $k$ is the system’s spring constant and $m$ is the system’s effective mass. This gives a method to estimate particle participation within a particle damper, where the percent of particles free to reciprocate between cavity walls is inversely related to mass offloading that can be observed by a shift in the system’s natural frequency. Therefore, the availability of phase data is deemed worth the implementation cost.

Both the frequency and phase measurement circuits are based off a frequency counter design in which rising edges of a high frequency clock are counted between rising edges of the signal to be measured. Knowledge of the clock frequency and the count allows the period and frequency of the signal of interest to be measured. A similar process in which the time between rising edges of the input and output signal is measured allows phase shift to be calculated.

This circuitry is placed on the Payload Command & Data Handling (PC&DH) board. While a programmable logic device (PLD) may provide a simple, compact and
power efficient implementation, concerns related to PLD configuration corruption caused by orbital radiation led to a design based instead on discrete logic, counter and multiplexing integrated circuits.

5.2.1 Trigger Circuitry

The input and output waveforms within the experiment are converted to square waves using Schmitt triggers located on the Piezoelectric Actuator Driver Board and the Sensor Modules such that rising edges are better defined. These square wave signals are fed to U8, which is the beginning of the signal chain on the PC&DH board. U8 multiplexes the various Sensor Module signals such that the beam system of interest can be selected for frequency and phase measurements. U8 also level converts the 0-5V waveforms to a 0-3.3V signal suitable for the PC&DH electronics.
Figure 45 - Schematic of frequency signal multiplexer. Control lines select the Sensor Module waveform to feed through. 5V waveforms are level converted to 3.3V suitable for the PC&DH logic.

The output of U8 is the input frequency waveform and the selected output frequency waveform. These signals are split to three similar circuit blocks, which respectively generate a single pulse proportionate to the input period, output period and the delay between rising edges of the input and output. These pulses are later used to gate in a high frequency clock to a counter such that the pulse durations can be measured to determine frequency and phase. This counter circuit block is covered in Section 5.2.2.

The signal path beginning with U14, which serves as a trigger for input frequency measurement, can be compared directly with that starting at U19, which serves as a trigger for output frequency measurement. The following component by component
description of the trigger circuitry operation will follow the signal chain beginning with U14.

The trigger circuit block performs three sequential operations: Arm, Count and Hold. The Arm state readies the circuitry such that the next rising edge event on the signal of interest will trigger the measurement process. The Count state begins after the rising edge occurs and asserts a signal that starts a high frequency counter. The Hold state begins after a desired number of periods of the signal of interest occurs and halts the high frequency counter, holding the circuitry in an inert state until another Arm event occurs.

The Arm state is initiated by a high-low-high pulse on the /ARM signal, controlled by the PC&DH microcontroller. This presets U14, a D flip-flop, such that the /Q output goes low. After the /ARM signal returns to the high logic level, XNOR gate U10B passes /Q’s low logic to the active low clear input of U15, a 4-bit counter. This clear function is synchronous to U15’s clock input which is tied to the signal to be measured, FREQ_IN_3V3. This means the trigger is now armed such that a rising edge of the FREQ_IN_3V3 signal will clear U15, causing the circuit block to enter the Count state. The rising edge event that initiates the Count state simultaneously (after some propagation delay) causes U14’s /Q output to go high, ultimately leading to U15’s clear line to deassert. This process automatically de-arms the circuit block such that only one trigger event occurs per measurement.
Figure 46 - Schematic of input frequency counter trigger block. This circuitry generates a single pulse of duration proportionate to the input frequency period; this is later used to gate in a high frequency clock to a counter.

The count state begins after the first rising edge of FREQ_IN_3V3 after the /ARM signal is deasserted. This rising edge clears U15, causing the 4-bit output to go low. One of these bits is passed through multiplexer U16, to the input of inverter U13. The output of U13, an active high signal designated FREQ_IN_CNT_GATE, starts the high frequency counter described in Section 5.2.2. As additional rising edges of FREQ_IN_3V3 occur, U15’s binary output counts up accordingly; when the bit selected by U16 flips (goes high), the FREQ_IN_CNT_GATE signal goes low, halting the high frequency counter. This same signal pulls the count enable pin of U15 low, effectively freezing U15’s 4-bit output. This is the Hold state, which is held until another /ARM signal occurs to restart the trigger process.

Changing the state of multiplexer U16 alters the number of periods to be counted between 1 and 8. Increasing the number of periods counted increases the accuracy of the frequency measurement, but at the cost of longer required data acquisition time. Making this setting variable, through lines SEL_DIV0 and SEL_DIV1, controlled by the PC&DH microcontroller, gives the ability to quickly acquire lower accuracy data to achieve
minimum mission success, and then later capture full resolution measurements throughout the remainder of CP7’s orbital lifespan.

The phase measurement trigger circuitry operates very similarly to the input and output frequency measurement trigger previously described. One of two key differences is the inclusion of U6, a single pull double throw (SPDT) switch. In the U6 configuration, tying the channel select line to the clear line of the 4-bit counter, U9, ensures that the phase measurement will always begin with a rising edge of the excitation input signal and end with a rising edge of the system’s output signal. This gives consistency in phase measurements, removing ambiguity as to which signal leads which. The second key difference is the exclusion of a multiplexer stage after the 4-bit counter, since this phase measurement technique is limited to timing only a single phase lag duration at a time.

Figure 47 - Schematic of phase counter trigger block. This circuitry generates a single pulse of duration equal to delay between rising edges of the input and output frequency; this is later used to gate in a high frequency clock to a counter.

5.2.2 Counter Circuitry

Each of the three gate control lines that originate from the trigger circuitry described in Section 5.2.1 are applied as an input to separate two channel NAND logic gates, U2(A-C). The second input of each respective NAND gate is tied to a 32MHz clock signal. An intermediate component, U22, buffers a 32MHz crystal oscillator, U21,
such that the combined capacitive load of all three NAND gates can be driven. This configuration allows the high frequency clock to be gated through the signal chain for a duration controlled by the gate control lines.

The output of each NAND gate is tied to the clock input of a 32-bit counter, U24, U25, and U26. These counters increment for each rising edge of the 32MHz clock, such that signal period can be ideally measured within 1/32MHz or 312.5 microseconds within a period of 312.5µs × 2^{32} or 134.2 seconds. High speed NAND gates and a high stability crystal oscillator are chosen to approach this ideality. A 32MHz clock signal is chosen to provide high accuracy, yet give sufficient headroom for the 40MHz rated maximum clock of the 32bit counters.
5.2.3 Digital Interface

A digital interface is required to control and read the phase and frequency measurement circuitry. This is accomplished by the PC&DH microcontroller in conjunction with 16-bit I²C GPIO expanders U27 and U28. The hardware trigger circuitry described in Section 5.2.1 eliminates the need for strict timing requirements allowing a simple procedure based software algorithm to perform the required operations. This procedure is described in Section 5.4.5.

Figure 49 - Schematic of counter circuitry digital interface. Two 16-bit I²C GPIO expanders are used to read in the counter registers as well as control the various counter parameters.

The 32 bit counters, U25, U26 and U27 offer a tri-state 8-bit parallel output that is multiplexed by 4-bit one cold encoded select lines such that all three 8-bit ports can be combined into a single 8-bit bus CNTB(0-7). These lines are applied to the P0(0-7) port of U27. The three 4-bit control groups are applied to output ports on U28. The GPIO expanders also control the select division logic required to select the amount of periods to be counted (a function accomplished by the multiplexers described in Section 5.2.1). The UPDATE_CNT and CLR_CNT signals on U28 allows the microcontroller to update the
32-bit counter registers prior to reading, and clear the count in preparation for a new measurement respectively.

By monitoring the high frequency counter gate control lines (FREQ_OUT_CNT_GATE, FREQ_IN_CNT_GATE and PHASE_CNT_GATE) the GPIO expanders are capable of conveying the state of the frequency measurements to the microcontroller. This gives the system knowledge of when a measurement is complete.

The final output control signal, /ARM, needed for initiating a new measurement was omitted from the GPIO expander’s control as a result of a schematic capture oversight. This is rectified through a wire mod added between the trigger circuitry and the RH2, A18 pin (pin # 1) on the PC&DH microcontroller.

5.2.4 Calibration

Within the accuracy requirements of this investigation, the specified U21 crystal oscillator tolerance and drift parameters are determined to be sufficient such that further characterization of the clock is unnecessary. Therefore the frequency measurement circuitry does require any characterization steps. The accuracy of the phase measurement circuitry is however largely dependent on the rising edge hysteresis point of the Schmitt triggers used for generating the frequency measurement signals.

The chosen phase detector design assumes that the timed interval between input and output rising edges begins and ends at the same relative position on the respective sinusoids. Because the hysteresis bands of the Sensor Module and Piezoelectric Actuator Driver Schmitt triggers are nominally different, and uniquely dependent on resistor tolerances, this assumption fails. To correct for this, Equation 7 is applied in post
processing to estimate the delay ($t_{delay}$) between a sinusoid’s zero crossing and the rising edge of the respective Schmitt trigger such that the measured phase delay can be adjusted accordingly.

$$t_{delay} = \frac{1}{2\pi f \cdot \sin^{-1}\left(\frac{V_{HR}}{A}\right)}$$

Equation 7 – Period adjustment for Schmitt trigger hysteresis based phase measurement

Where $V_{HR}$ is the rising edge level of the hysteresis band, $A$ is the signal amplitude and $f$ is the signal frequency. All the variables of Equation 7 are known for each frequency iteration through the data acquisition measurements except $V_{HR}$, which must be measured using external equipment in a calibration process.

It should be noted that the value of $V_{HR}$ may drift with component temperature dependence. Also, Equation 7 assumes the waveforms in question are ideal sinusoids, which does not always hold true, especially in the case of nonlinear particle damper based measurements. However, because phase measurement is not a defined system requirement, this potential inaccuracy is tolerated.

5.3 Payload Command & Data Handling

5.3.0 System Overview

The Payload Command & Data Handling (PC&DH) board houses a microcontroller, peripherals and interconnects needed to implement data acquisition algorithms, store measured data and communicate with CP7’s avionics system. Due to layout availability this board also houses drivers for the SMA actuator mechanisms.
(required for the locking mechanism described in Section 4.4), the frequency and phase measurement circuitry (described in Section 5.2) and various power regulators.

The PC&DH board mates directly to the Piezoelectric Actuator Driver board as shown in Figure 32. A special cutout exists such that the large EMCO high voltage converters can protrude outside the sandwich configuration (see Figure 50). This minimizes the combined thickness of the boards, such that they can more easily be fit within the physical constraints of CP7.

A number of ribbon cable connectors are aligned along the parameter of the PC&DH board. This gives easy access to the Sensor Module cabling, avionics interface cabling and the locking mechanism feedback cabling. Through-hole terminals, similarly located, provide a high current capability interface for driving the SMA actuators. Finally, small holes are drilled near the high voltage output terminals of the Piezoelectric Actuator Driver board such that high voltage cabling can be fed through to the piezo actuators.
Figure 50 - Annotated photograph of the PC&DH PCB, top layer. The 3.25” square board houses the slightly smaller Piezo Driver PCB. Ribbon cable headers along the perimeter are exposed for easy access. A rectangular cut out allows the high voltage DC-DC converters to pass through to minimize stack height.
Figure 51 - Annotated photograph of the PC&DH PCB, bottom layer. The high voltage DC-DC converters from the mated Piezo Driver Board can be seen protruding from the cut out.

5.3.1 Microcontroller and Supporting Peripherals

A PIC18LF8722 8-bit microcontroller is selected to control the CP7 payload instrumentation. The greatest driving factor for this selection is the PolySat lab’s familiarity with the device and the supporting MPLAB development environment. This experience also allows existing drivers and other low level routines to be leveraged to reduce software development time.
Figure 52 - Schematic of microcontroller on PC&DH. An 8-bit microcontroller configured for a 25 MHz clock rate controls the payload operations and communicates with the satellite avionics.

As configured on the PC&DH board, the PIC18LF8722, or U30, runs at a clock rate of 25MHz. This clock is set by an internal oscillator in conjunction with external crystal, Y1. At this speed, U8 exhibits an attractive power and speed trade off; suitable to reduce data acquisition computational and communication related delays, yet appropriate to take advantage of the time insensitive steady state peak detection measurement.
technique. Additionally, the availability of dual \( \text{I}^2\text{C} \) modules enable the PIC to be used as both a master to payload related components, and as a slave to the avionics system.

A 100kHz \( \text{I}^2\text{C} \) communication protocol is the primary means in which U30 interfaces with peripheral systems. \( \text{I}^2\text{C} \) addressing limitations are alleviated through the use of a four channel \( \text{I}^2\text{C} \) multiplexer, U29. This allows all three Sensor Modules and the Piezoelectric Actuator board to share \( \text{I}^2\text{C} \) devices with similar addresses. It also performs the level converting needed to interface the 3.3V logic of the PC&DH board with the 5.0V logic needed to drive these peripherals. U29 features a reset line that allows the microcontroller, through the use of a dedicated GPIO, to disconnect all such peripherals in the event of a fault that pulls the \( \text{I}^2\text{C} \) lines low. This would otherwise disable the entire \( \text{I}^2\text{C} \) bus, potentially resulting in a non-recoverable condition.

![Figure 53 - Schematic of \( \text{I}^2\text{C} \) multiplexer. By multiplexing the \( \text{I}^2\text{C} \) lines the payload microcontroller can address identical components on the Sensor Modules and Piezo Driver. Separate sets of pull up resistors level convert the \( \text{I}^2\text{C} \) logic.](image)

Data storage local to the PC&DH board is achieved through four separate 1-Mbit capacity, 8-bit word size \( \text{I}^2\text{C} \) EEPROM’s: U32, U33, U35 and U36. In the current data handling configuration only two of these devices are used. Two additional devices are daisy-chained to provide flexibility in future development, giving the ability to store
more data local to the PC&DH or provide memory redundancy. The EEPROM devices are selected based on flight heritage and the availability of preexisting drivers developed for past PolySat missions.

I\textsuperscript{2}C communication to the external EEPROM memory is multiplexed between U28 and the avionics system, through U31. This allows the memory to have two masters, allowing U30 to make direct write operations, and the avionics to make direct read operations. This greatly simplifies the data handling on the software level, removing the need for U30 to operate as an intermediary for data transfer. U30 is given sole control of the multiplexing through a dedicated GPIO such that EEPROM access conflicts do not occur. In this configuration, the avionics systems must first request access to the EEPROM’s or wait for U30 to transfer access at the end of an experiment procedure.

Supplementing U30’s I\textsuperscript{2}C bus control over payload operations are several GPIO ports. The purpose of these lines will be addressed in subsequent sections.
Figure 54 - Schematic of payload nonvolatile memory. Four I2C EEPROM IC’s are daisy chained for a total capacity of 4-Mbits. A switch, U31 multiplexes the I2C lines so that the payload and avionics can share master control.

5.3.2 Avionics Interface

The avionics interface, which ultimately links experiment data to a ground station, has two primary means of communicating with the PC&DH board. First, is an I2C bus connected to U30. The respective I2C port on U30 is configured as a slave, allowing the avionics system to command or interrupt payload operations. This hierarchy is designed such that the avionics can run payload operations based on considerations of system power level and uplinked commands. This I2C bus is supplemented by the I2C_IGNORE line which links GPIOs of U30 (input only) and the avionics computer (output only). The logic value of this signal tells U30 to enable or disable the avionics linked I2C port such
that address bytes intended for other components on the shared bus do not cause U30 to pause experiment operations.

The second means in which the avionics may communicate with U30 is through an I²C GPIO expander, U37, connected to the avionics’ I²C bus and an 8-bit parallel port of U30. This configuration allows the avionics to communicate non time critical values with U30 without interrupting the experiment.

![Figure 55 - Schematic of payload to avionics parallel port. An I²C GPIO expander, U37, interfaces with a parallel port on the PC&DH microcontroller for status byte updates. An array of LEDs assists in software development and troubleshooting.](image)

The intended use of this interface is to allow U30 to communicate sequential status bytes to the avionics system. The avionics system can monitor this status byte to give knowledge of the state of the experiment progress. This serves two purposes; first it gives the avionics indication of when the payload is finished with an experiment and
ready for data to be read. The avionics may then decide to pass new experiment parameters or turn off the payload to conserve power. The second purpose of the status byte is to give means in which the avionics can detect a payload fault. By comparing payload progress against predefined maximum time limits, the avionics can perform a watchdog function. If a fault is detected, the avionics can then power cycle the payload in an attempt to clear the fault. LED’s D(10-17) are connected to give a visual indication of the status byte. This assists in bench testing and debugging efforts. To conserve power, these LED’s are not populated on the flight unit PC&DH board.

Payload to avionics signal and power lines are interfaced via the ribbon connector JP4. Signal lines include programming lines for U30, which are routed through the avionics to CP7’s umbilical connection. This allows the payload to be reprogrammed while integrated within the cubesat. A payload power enable signal is also made available through this connection such that the avionics can turn the payload off to conserve power. A power fault logic line gives the avionics the ability to diagnose an over-current condition within the payload. Lines within this 24 pin header are duplicated to meet current carrying requirements.

5.3.3 Power Regulation

The CP7 high level Electrical Power System (EPS) is similar to that used in previous missions. Depending on temperature, state of charge and orbital orientation this EPS produces an unregulated voltage that can vary between approximately 5.0V and 3.2V. To desensitize payload functionality to the variability of the unregulated supply, DC/DC buck boost converters are implemented to provide steady regulated outputs.
The PC&DH board consists mostly of digital circuitry, making proper operation relatively unaffected by switching noise. This, coupled with the availability of PCB real-estate makes the PC&DH a suitable candidate for housing the payload specific DC/DC converters.

The voltage values of the converter outputs must be selected to give headroom to the cascaded point of load LDO regulators implemented throughout the payload. A 5.4V rail is selected to accommodate +5V and +3.3V LDOs and a -5.36V rail is selected to accommodate the -5.0V LDO. This type of cascade configuration combines the inefficiency of the DC/DC converters and the LDO’s and is not power optimal; rather simplicity and noise reduction drove this design selection.

These respective outputs are produced by U1 and U2. U1 is a high efficiency Texas Instruments TPS63000 buck boost regulator and U2 is a Linear Technology LT3483 inverting charge pump. The external inductor and input / output capacitor selection for each regulator are selected based on design guidelines within the respective data sheets.

Figure 56 - Schematic of payload switching regulators. Buck Boost converter, U1 and inverting charge pump, U2 cascaded with LDOs provide the required 3.3V, 5V and -5V power rails used throughout the payload.
5.3.4 SMA Actuator Drivers

The final component of the PC&DH is the driver needed to control the SMA Actuators used to selectively lock and unlock the cantilever beams. A simple on-off control solution is selected for simplicity and efficiency. Low-side MOSFET switches Q(1-4) sink current through a desired actuator as selected by the SMA_LATCH and SMA_RELEASE logic signals routed from the PC&DH’s microcontroller. Current is sourced through the satellites unregulated supply, and sensed by the current and voltage I\(^2\)C sensor U34. This sensor provides confirmation of expected current draw to verify proper actuator operation.

![Schematic of SMA driver](image)

**Figure 57 - Schematic of SMA driver.** Power MOSFETs Q(1-4) are configured as low side switches to sink current through selected SMA actuators. U34 monitors current and voltage to confirm proper operation.

The amount of time needed for an SMA actuator to complete its required stroke is dependent on the value of the unregulated rail and the thermal dissipation properties of the SMA within the space environment; therefore a simple open loop control solution is
insufficient. Closed loop control is instead accomplished through locking mechanism position sensing switches integrated throughout the payload. Feedback from these switches is routed through header JP5 to the PC&DH microcontroller. Pull up resistors R(45-R48) accomplish a simple two state logic indicating whether a locking mechanism is engaged or released.

Figure 58 - Schematic of SMA position switch logic feed through. Pull up resistors convert the open and closed states of mechanical switches to logic states that can be read in by the microcontroller.

5.4 Instrument Control Algorithms

Automated control of the CP7 experiment is not a trivial task. The nonlinear and unknown behavior of the particle damped systems drive a data acquisition scheme that is tolerant of unknown system dynamics. However, in order to reduce net power and time requirements the algorithms must converge to solutions in minimal time.

In this section, an overview of the high level algorithms is provided. More detailed implementation descriptions can be found in the Senior Project work conducted by Daniel Walker in Reference 58.
5.4.0 Wait and Read Algorithm

The peak detection scheme used in both the Sensor Module and the Piezoelectric Actuator Driver requires at least one sinusoidal crest to occur in between reset and read operations. A crest is guaranteed to occur in at least one period of the sinusoid, which can be estimated based on the nominal input frequency selected. This period, plus sufficient margin defines the PK_CAPT_DELAY value.

By delaying a peak detector A/D conversion read by at least the PK_CAPT_DELAY value insures that a crest has occurred and the peak detector is outputting the signals true amplitude. This operation is accomplished in the Wait & Read algorithm, presented in Figure 59.

Figure 59 - Wait & Read algorithm. This algorithm is used to toggle the peak detectors and read in a waveform magnitude value after a sufficient delay.
5.4.1 Sensor Module Automatic Gain Control Algorithm

The automated gain control implemented on the Sensor Module is designed to maximize the signal chain’s signal to noise ratio within the dynamic range constraints of the Sensor Module. This means that a gain factor must be chosen to amplify the accelerometer output to an optimal level. Taking in considerations of peak detector diode drop out, 5V supply rail and 2.2V DC offset voltage, a maximum signal amplitude of 1.9V is selected.

The Adjust Gain flow diagram of Figure 60 is designed to select a gain factor by comparing the normalized signal level to a Look Up Table (LUT) and selecting the corresponding gain to achieve a new signal amplitude just below the 1.9V limit. To reduce fixed point computation errors in the normalization the signal amplitude output code and gain factor is augmented by three decimal places. The LUT table referenced in this operation is reproduced in Appendix E; it is designed to provide some overlap or hysteresis between gain settings to reduce spurious oscillations. An example of the adjust gain algorithm’s effectiveness is presented in Figure 61.
Figure 60 - Adjust gain algorithm. This algorithm is used within the automatic gain control to approach an optimal signal amplitude.
Figure 61 - An overlay of signal amplitude and beam magnitude frequency response. Data points are achieved from an experiment run of a baseline beam system. The automatic gain algorithm amplifies the accelerometer amplitude to a relatively constant level. Normalizing the signal amplitude by the gain and converting voltage units to acceleration achieves the magnitude frequency response plot.

Because the accelerometer signal can not be assumed to be at steady state, the Adjust Gain algorithm is not sufficient in itself to converge to an optimal solution. The Automatic Gain Control (AGC) algorithm of Figure 62 is implemented to tolerate signal transients, voltage rail conditions and to select the appropriate accelerometer full scale range settings. Loop count limits are used to insure the AGC does not enter an infinite loop caused by failure of the system to enter a steady state. These loop limits can be adjusted through remote operations in the case that particle damper zero gravity transients are found to be significantly different then those observed during ground tests.
Figure 62 - Automatic Gain Control Algorithm. This algorithm approaches an optimal signal level, while tolerating transients and rail conditions. Loop counters insure the algorithm does not enter an infinite loop. Various parameters of the algorithm can be updated remotely to adjust for unknown particle damper dynamics.

A sample of the gains returned for an experiment run is provided in Figure 63, which overlays the corresponding measured system magnitude response. This shows that the gain is decreased in the vicinity of the systems resonant frequency, where the output response magnitude is high. A discontinuity at the peak response, occurring in the
frequency range of 91-92 Hz, can be observed due to the algorithm switching the full scale sensitivity of the accelerometer from 2g to 6g.

![Sensor Module Automatic Gain Control](image)

**Figure 63** - An overlay of gain factor and beam magnitude frequency response. Data points are achieved from an experiment run of a baseline beam system. The automatic gain algorithm amplifies the accelerometer amplitude to a relatively constant level by adjusting the signal chains dynamic gain. As can be observed from the plot, the gain is reduces as the beam’s response increases. A discontinuity near the resonant frequency indicates a transition from the accelerometer’s 2g full scale to 6g full scale.

### 5.4.2 Sensor Module Steady State Detection Algorithm

The Automatic Gain Control algorithm provides some inherent steady state detection, as it will not converge to a gain until the signal is sufficiently stable. This however is a coarse steady state detection and is succeeded by the Find Steady State algorithm, presented in Figure 64.
Figure 64 - Find Steady State Algorithm. This algorithm detects a steady state condition by comparing past and present magnitude levels. The tolerance of the steady state determination is iteratively increased to tolerate beat frequencies that may be present in the particle damper’s response.

The Find Steady State algorithm successively compares past and present signal values until the difference between the signals is within some predetermined margin. This margin is initially set low, but gradually increases if a steady state is not detected within a loop limit. This allows the system to return a measurement even if the system does not settle to a true steady state; a condition that may occur due to a beat response caused by intermodulation frequencies in the nonlinear particle damper dynamics.
An inspection of the steady state margin selection through the course of an experiment run provides indicators of the systems frequency dependent nonlinearity. An example of such a plot is provided in Figure 65.

Figure 65 - An overlay of steady state tolerance and a systems magnitude frequency response. Data points are achieved from an experiment run of a baseline beam system. As can be observed from the plot, a steady state is typically identified within a few milli-g’s. A spike in the tolerance level is present near the resonant frequency owing to the long lasting transients of the underdamped baseline system. Increasing the loop limits within the find steady state algorithm can reduce this spike, but comes at the cost of increased experiment run time.

5.4.3 Piezo Driver Closed Loop Amplitude Control Algorithm

The closed loop amplitude control of a piezoelectric actuator is accomplished through two algorithms. The first algorithm initializes the input, and is conducted once per experiment run. The second algorithm updates the amplitude successively throughout the experiment to correct for imperfections in the amplitude flatness over the Piezoelectric Actuator Driver’s frequency response.

The Initialize Input Amplitude algorithm, of Figure 66, takes a successive approximation approach to converging on the desired amplitude. First, the fine gain
stage is set to maximum gain and the coarse gain stage is adjusted from low to high until
the output amplitude is higher than the desired value. Next the fine gain stage is
decreased and increased in successively smaller steps until the output amplitude
converges to a value that is as close to the desired output as possible.

The Update Input Amplitude algorithm, of Figure 67, is implemented
immediately after frequency is incremented a predefined amount. The algorithm uses a
“perturb and observe” method, where the gain is decremented or incremented based on
the sign of the error between desired amplitude and actual amplitude. If the magnitude of
the error decreases, the algorithm continues to step through gain until a minimum in error
magnitude is found. Because this algorithm must be repeated throughout the experiment,
and can contribute transients in the system, it adds significant amount of time to the total
experiment run time. To compromise between input amplitude accuracy and experiment
run time, the Update Input Amplitude algorithm is only implemented when the frequency
has been changed by some set amount. An example plot of the input amplitude
controlled in this way over the course of an experiment run is provided in Figure 68;
several phenomenon are annotated in this plot.
Figure 66 - Initialize Input Algorithm. This algorithm takes a successive approximation approach to converge on a desired amplitude. The order of operations is designed to minimize the amplitude error.
Figure 67 - Update Input Algorithm. This perturb and observe algorithm is executed successively throughout the experiment run to correct for non-flatness in the driving electronics frequency response.
Figure 68 - An overlay of input fine gain level and input amplitude. Data points are achieved from an experiment run of a baseline beam system. An inspection of this plot demonstrates the Update Input Amplitude Algorithm’s effect on the input amplitude. Noise in the measured amplitude can be observed in the distribution of data points; occasionally this causes a glitch in the amplitude setting as annotated. A discontinuity near the system’s resonant frequency is caused by a minimum in the system’s impedance; the update amplitude algorithm can overshoot in its correction causing the observed effect. Both problems may be remedied by averaging readings and performing the update input algorithm more frequently at the cost of longer experiment run time.

5.4.4 Beam Locking Mechanism Control

The beam locking mechanism control algorithm is developed in Daniel Walker’s Senior Project work, and is described in Reference 58. It is mentioned here for completeness.

5.4.5 Phase and Frequency Measurement Procedure

The phase and frequency measurement control is implemented mainly through the hardware described in Section 5.2. The PC&DH microcontroller must simply select
measurement parameters including the selection of the Sensor Module of interest and the desired number of periods to measure; then clear the previous count and arm the trigger circuitry. By monitoring the high frequency clock gate lines the PC&DH microcontroller can determine a measurement has been made, and then read in the desired data after updating the counter output registers. This process is detailed in Appendix F.

Figure 69 - An overlay of the percent error between nominal frequency and measured frequency. Data points are achieved from an experiment run of a baseline beam system. The divergence of measured output frequency is a result of lower signal to noise ratio as the system’s magnitude response dies off.
Figure 70 - A plot of a beams phase frequency response. Data points are achieved from an experiment run of a baseline beam system.
6  Experiment Data Analysis

6.0  Data Post processing

The final low level design consideration is the post processing of the data achieved from the CP7 instrumentation. To simplify development, raw data is stored and transmitted from the satellite such that post processing algorithms can be implemented using the computing resources available on the ground.

The structure of downlinked packets and the parsing thereof is out of the scope of this paper. Rather this section will focus on the processing of data that has been made available in a decimal comma separated value (CSV) or similar format.

6.0.0  Basic Data Analysis

A Matlab script is developed to read in data from an XLS formatted file consisting of the raw output codes achieved in the CP7 data acquisition process. This script also reads in data acquisition characterization parameters stored locally. These parameters are unique for each hardware system derived previous to system integration through the characterization procedures described in the above sections.

After loading the raw data into a matrix, the script applies the various scaling operations to the data such that it can ultimately be represented in units understandable to analysts; principally acceleration in g’s, frequency in Hz and phase in degrees. An estimate of pound force (lbf) transduced by a piezo actuator for a given input amplitude is used to derive the system’s magnitude transfer function in the common g/lbf accelerance units. The analytical derivation of the linear lbf/V relation is provided in Appendix A.
The final function of the script is to produce plots of the system transfer function as well as plots of input amplitude over frequency, a comparison of input, output and nominal frequency values, steady state tolerance and other visuals that can give an operator the ability to quickly confirm proper system operation. Examples of these plots can be found throughout Section 5.4.

A version of this script is made available in Appendix G.

6.0.1 Advanced Data Analysis

The frequency stepped data acquisition process used in CP7 instrumentation is discrete in nature, necessitating the use of an interpolation technique to derive continuous curves from which system bandwidth, damping factor and natural frequency can be estimated. A comprehensive description of the interpolation technique developed for CP7 data analysis is out of the scope of this work, however a brief overview of the approach is provided.

Data interpolation accuracy can often be enhanced through the application of a mathematical model of the system being measured\[^{[59]}\]. While a satisfactory model for particle damper behavior does not exist, the underlying cantilever beam baseline behavior can be approximated closely by the transfer function of a simple harmonic oscillator (SHO) with viscous damping. Employing a data fitting algorithm to this transfer function produces estimates of SHO parameters including damping factor, natural frequency and spring constants.

The difference between the data points and the SHO model evaluated at the respective frequency points is then applied to a General Regression Neural Network
(GRNN) algorithm. This algorithm leverages the stochastic properties of radial basis functions to interpolate a continuous curve fitted to the data set in a manner that is tolerant to measurement noise\textsuperscript{[59]}. A magnitude plot overlaying these different steps is provided in Figure 71.

![Data Interpolation](image)

**Figure 71 - An overlay of various data interpolation steps.** Data points are achieved from an experiment run of a particle damped beam system. A SHO model is first fit to the measured data points. This physical model is then used to develop a GRNN to interpolate a continuous frequency response curve.

Applying this process to both phase and magnitude data over various data sets corresponding to different input amplitudes allows the particle damper amplitude dependent dynamics to be visualized. Such nonlinearities are one of the principal interests in particle damper dynamics. Figure 72 and 73 are developed by applying this interpolation over data sets acquired from CP7 system testing.

The points of interest identified on the plots of Figure 72 and 73 can be plotted against input amplitude two dimensionally to provide a clearer representation of the nonlinearities. Additionally, by relating natural frequency to system effective mass in the method outlined in Section 5.2.0, particle mass participation can similarly be represented. Figure 74 provides these plots.

An inspection of Figure 74 reveals a peak in damping efficiency as particle mass reaches maximum offloading. This behavior is typical of previous experimental findings.
discussed in Section 2.1. This type of plot set may demonstrate the most dramatic changes between a 1g and 0g particle damped system.

\[ \text{Magnitude Frequency Response} \]

\[ \text{Interpolated Magnitude Response Curve} \]
\[ \text{Peak Magnitude near Fn} \]
\[ -3dB Point \]

Figure 72 - A 3D overlay of a particle damped system’s magnitude response for increasing input amplitude. An inspection of the plot demonstrates a particle damper’s amplitude dependent nonlinearity. Points of interest are highlighted for visualization.
Figure 73 - A 3D overlay of a particle damped system’s phase response for increasing input amplitude. An inspection of the plot demonstrates a particle damper’s amplitude dependent nonlinearity. Points of interest are highlighted for visualization.

Figure 74 - A plot set demonstrating a particle damped systems amplitude dependent nonlinearities. Particle mass participation, as determined from the systems natural frequency can be correlated with damping trends. A local maximum in damper efficiency can be observed.
7 Conclusion

7.0 Mission Status

Testing of the payload instrumentation has demonstrated functionality and accuracy, as confirmed through the oversight of supporting System Dynamics Engineers and through data comparison with published works. Development of the CP7 payload is finalized and assembly of flight and engineering units is in progress. An assembled bench unit, depicted in Figure 9, has successfully passed a P-POD fit check and launch vehicle vibrations profile test to demonstrate preliminary flight qualification. A tap (impulse) test has verified target structural dynamic properties. More information on this test and the structural dynamic analysis can be found in John Brown’s thesis work in Reference 42.

Piezoelectric actuators have been bonded to the flight and engineering unit cantilever beams and baseline beam frequency response has been measured and documented. Following this benchmarking, the top and bottom beam in each unit has been integrated with a 95% and 90% respective volumetric fill ratio of crystalline tungsten powder to form the particle dampers of interest. An epoxy bead has been applied to hermetically seal the tungsten, which had been baked out to remove moisture prior to integration.

Six pick-and-placed Sensor Modules have been fully calibrated and allotted for the flight and engineering units. Population and testing of flight and engineering PC&DH boards and Piezoelectric Actuator Drivers will begin shortly. Final assembly of the payload mechanical components will follow the conformal coating of the sensor modules.
The remaining assembly and complete system testing, as overviewed in subsequent sections, support a December 2011 integration date. Efforts are currently underway in securing a launch position.

7.1 Remaining Work

7.1.0 Complete in the Loop System Testing

At the time of this writing, the new PolySat integrated communication, electrical power and data handling avionics hardware demonstrates basic functionality. Development of the embedded software required to support these systems as well as the CP7 unique payload driver is an ongoing process.

Upon completion of this software, the CP7 instrumentation can and should be tested as part of the complete satellite system. These tests should verify that CP7 can reliably receive instructions to set payload parameters, command experiment runs and request experiment data; in turn the satellite should reliably downlink confirmation of the respective commands and packets of experiment data. The satellite should be shown to be capable of autonomously executing said commands in a manner that guarantees the system will average a power positive state. Demonstration of this functionality entails a successful reliance on radio uplink and downlink, battery and solar cell power, payload operation scheduling and other satellite specific constraints.

7.1.1 Environmental Testing

After complete hardware in the loop functionality is demonstrated within the laboratory, system verification should be repeated under the stress anticipated to occur
throughout the mission. Successful operation within a vacuum over extreme temperature
cycles can be confirmed within thermal vacuum (TVAC) chamber testing and resilience
to launch vehicle vibration levels can be confirmed using a vibrations table. The
definition of the intricacies of such testing can leverage the PolySat and CubeSat lab’s
prior satellite qualification experience.

7.1.2 Fault Testing

Further stress testing should be conducted to demonstrate system fault tolerance.
Low power scenarios should be simulated to test the systems ability to hibernate until
batteries are charged to sufficient levels. Payload and avionics processor hard resets
should be forced at various stages of payload and avionics operations to insure proper
recovery. Finally, operations within the CP7 bench unit should be tested to failure to
understand life cycle limitations and failure modes.

7.1.3 Operation Plan Definition

Following complete hardware in the loop testing and verification, an operations
plan leveraging knowledge of the system behavior can be defined. Considerations
including communication data rate adjusted for packet overhead, fully integrated system
power draw and experiment run time should be weighed in the design of an operations
plan that minimizes mission risk.
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<td>Noise in Analog Circuits.</td>
<td>Tech. Hamers Research Group, University of Wisconsin-Madison</td>
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Appendix A: Piezo Force Voltage Relation

A piezoelectric transducer (PZT) bonded at the base of each beam is used to provide the actuation force. The PZT expands and contracts in a manner proportional to the amplitude and sign of an applied electrical potential. This allows a sinusoidal forcing function of variable frequency and amplitude to be applied to the cantilever beam by varying the parameters of an electrical signal applied across the PZT.

The force that the piezo exerts on the cantilever beam as a function of applied electrical potential can be approximated analytically. A derivation of this relationship is developed in Reference 40. The resulting equation is reproduced here:

\[ F = \frac{A \cdot E_b \cdot d_{31}}{4 \cdot t_c \cdot l_c} \cdot V \]

Equation 8 – Force to voltage piezoelectric transducer general relation

Values for the parameters of the Navy Type II PZTA3 used in this experiment are supplied by the manufacture’s data sheet. Applying these values:

\[ \frac{F}{V} = \frac{A \cdot E_b \cdot d_{31}}{4 \cdot t_c \cdot l_c} = \frac{(3.2258 \times 10^{-5} \text{ m}^2)(6.1 \times 10^{10} \text{ N/m})}{4 \times (2.54 \times 10^{-3} \text{ m})(44.45 \times 10^{-3} \text{ m})} \]

\[ \Rightarrow \frac{F}{V} = .7451 \text{ N/V} \]

Equation 9 – Force to voltage relation for chosen piezoelectric transducer

\[ A = \text{Area of PZT cross section} \]
\[ d_{31} = \text{PZT transverse piezoelectric charge constant} \]
\[ E_b = \text{Longitudinal Youngs Modules of PZT} \]
\[ t_c = \text{PZT thickness} \]
\[ l_c = \text{PZT length} \]
\[ V = \text{Applied electrical potential} \]
Appendix B: Sensor Module Schematic
RC TIME CONSTANT OF 22μs
EXPERIMENTALLY FOUND TO
HAVE DEADBEAT RESPONSE.

FILM TYPE CAPACITOR USED TO
MINIMIZE DROPOFF
USE DAUGHTER BOARD REGULATOR FOR V_ADJ.
VOLTAGE SHOULD BE RAMPED GRADUALLY TO REDUCE INRUSH CURRENT (SOFT START).

HV DC/DC OUTPUT VOLTAGE & POWER CONSUMPTION PROPORTIONAL TO SUPPLY VOLTAGE.
5V 3A REGULATOR CONFIGURED FOR 5.4V OUTPUT.
SUPPLIES ALL PAYLOAD 3V3 LOOPS. 1.5V GIVES SUFFICIENT DROP OUT VOLTAGE TO REDUCE.
VIN RANGE: 3.6V TO 5.6V (7V ABS MAX)
3.5A OUTPUT CURRENT

HIGH SIDE SWITCH SOURCES POWER TO PAYLOAD.
VIN HIGH = 2.7V
VIN LOW = 1.8V (7V ABS MAX)
ADJUSTABLE OF LIMIT FEATURE WITH OVERLOAD POWER CYCLE.

PULL UP TO ENABLE PAYLOAD
SEE DATA SHEET TABLE 1 FOR SELECTING CURRENT LIMIT RESISTOR.
FILL SMA LINES HIGH TO ACTIVATE MECHANISM.
ONLY ONE SMA SHOULD BE ACTIVATED AT A TIME AND DURATION SHOULD BE LIMITED TO PREVENT OVERHEATING.

SMA POSITION LOGIC SENSED BY OFFBOARD DIGITAL I/F SWITCHES.
LOGIC LOW INDICATES ENGAGED STATE.

CAL POLY PICSATELITE PROJECT (POLYSAT)
1 GRAND AVE., BUILDING 13-300, SAN LUIS OBISPO, CA 93407

Title
PAYLOAD C&H - SMA SWITCH

Sheet Document Number
 Created by
Rev
Date: Friday, October 08, 2010
Sheet 7 of 7
Appendix E: Automatic Gain Control Look Up Table

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Table 2 - Automatic Gain Control Look Up Table. The PC&DH µcontroller uses this LUT to adjust the gain of a Sensor Module based on the previous amplitude measurement in an effort to maximize the system's signal to noise ratio within the system rails.
Appendix F: Frequency Detector Operation Instructions

Much of the frequency and phase measurement steps are achieved automatically within hardware. The remaining steps are implemented via the PC&DH microcontroller and I²C GPIO expanders U27 and U30. This eleven step procedure is as follows.

1. Initialize according to settings on Table 2.
2. Choose sensor module with FREQ_SEL lines:
   - 0 0 – FREQ_OUT_1
   - 0 1 – FREQ_OUT_2
   - 1 0 – FREQ_OUT_3
3. Choose # of periods to count with SEL_DIV lines:
   - 0 0 – 1 period
   - 0 1 – 2 periods
   - 1 0 – 4 periods
   - 1 1 – 8 periods
4. Pull CLR high
5. Toggle /ARM low (bring back to high)
6. Pole FREQ_OUT_CNT_GATE, when low go to step 5; if TMAX expires record F_IN_ERROR, go to step 6
7. Toggle UPDATE_CNT high (bring back to low)
   - Pull F_IN_SB0 low, record CNTB(0-7) as F_IN byte 0 (LSB); return F_IN_SB0 to high
   - Pull F_IN_SB1 low, record CNTB(0-7) as F_IN byte 1; return F_IN_SB1 to high
   - Pull F_IN_SB2 low, record CNTB(0-7) as F_IN byte 2; return F_IN_SB2 to high
   - Pull F_IN_SB3 low, record CNTB(0-7) as F_IN byte 3 (MSB); return F_IN_SB3 to high
8. Pole FREQ_IN_CNT_GATE, when low go to step 7; if TMAX expires record F_OUT_ERROR, go to step 8
9. Toggle UPDATE_CNT high (bring back to low)
   - Pull F_OUT_SB0 low, record CNTB(0-7) as F_OUT byte 0 (LSB); return F_OUT_SB0 to high
   - Pull F_OUT_SB1 low, record CNTB(0-7) as F_OUT byte 1; return F_OUT_SB1 to high
   - Pull F_OUT_SB2 low, record CNTB(0-7) as F_OUT byte 2; return F_OUT_SB2 to high
   - Pull F_OUT_SB3 low, record CNTB(0-7) as F_OUT byte 3 (MSB); return F_OUT_SB3 to high
10. Pole PHASE_CNT_GATE, when low go to step 9; if TMAX expires record PHASE_ERROR, end procedure
11. Toggle UPDATE_CNT low (bring back to low)
    - Pull PHASE_SB0 low, record CNTB(0-7) as PHASE byte 0 (LSB); return PHASE_SB0 to high
    - Pull PHASE_SB1 low, record CNTB(0-7) as PHASE byte 1; return PHASE_SB1 to high
    - Pull PHASE_SB2 low, record CNTB(0-7) as PHASE byte 2; return PHASE_SB2 to high
    - Pull PHASE_SB3 low, record CNTB(0-7) as PHASE byte 3 (MSB); return PHASE_SB3 to high
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Table 3 - Initialization state of the frequency and phase hardware.
Appendix G: Data Processing Matlab Script

A simple Matlab script can be used to process the raw data into understandable units and display the results in a graphical format. This is useful for quickly confirming proper instrument operation. A version of such a script is provided here.

% Data acq constants
AD_CONST = 6.25*10^-5; % ADS1115 A/D constant
TWO_G_VTOA = 1.527; % Accelerometer 2g conversion. (SM ET)
SIX_G_VTOA = 4.573; % Accelerometer 6g conversion. (SM ET)
DDS_CLK = 16; % Frequency of DDS CLK in MHZ
V_div = 50; % Voltage division factor for high voltage measurement
FREQ_DIV = 4; % Number of cycles used in frequency measurement
CNTR_CLK = 32*10^6; % Frequency measurement clock
VH_OUT = .3912; % Output frequency comparator rising trip point (SM ET)
VH_IN = .0527; % Input frequency comparator rising trip point (PD_BENCH)
v2lbf = .1675; % Piezo input force to voltage

% Read data file
SENSOR = 'ET';
BEAM = 'Flight Unit Bottom Beam Baseline';
FILE = ['FLT_BOTTOM2_50VDIV.xls'];

% Get raw data
raw = xlsread(FILE,'A2:R7000');
NOM_IN_FREQ_RAW = raw(:,2);
VPK_RAW = raw(:,12);
VVL_RAW = raw(:,13);
SS_MRGN_RAW = raw(:,14);
DVAL = raw(:,10);
ACCEL_STATE = raw(:,9);
IN_AMP_RAW = raw(:,7);
MEAS_FREQ_IN_RAW = raw(:,16);
MEAS_FREQ_OUT_RAW = raw(:,17);
PHASE_RAW = raw(:,18);
IN_AMP_DVAL = raw(:,6);

% Get measured gains
GAIN_TABLE(:,1) = xlsread(['CALIBRATION_SM_',SENSOR,'A5:A53']);
GAIN_TABLE(:,2) = xlsread(['CALIBRATION_SM_',SENSOR,'G5:G53']);
SD_BIT = xlsread(['CALIBRATION_SM_',SENSOR,'G4:G4']);

% Apply acq constants

% Input nominal input frequency to the beam
FREQ = NOM_IN_FREQ_RAW./(2^28).*(DDS_CLK * 10^6);

% Measured input frequency to the beam
MEAS_FREQ_IN = 1./(MEAS_FREQ_IN_RAW./FREQ_DIV.*(1/CNTR_CLK));

% Measured output frequency to the beam
MEAS_FREQ_OUT = 1./(MEAS_FREQ_OUT_RAW./FREQ_DIV.*(1/CNTR_CLK));

% Calculate delay caused by sine to square wave comparator
HYST_DELAY_IN = 1./(2*pi*MEAS_FREQ_IN).*asin(VH_IN./(IN_AMP_RAW*AD_CONST));
HYST_DELAY_OUT = 1./(2*pi*MEAS_FREQ_OUT).*asin(VH_OUT./(VPK_RAW*AD_CONST));

if max(PHASE_RAW) == 0
    % if input amplitude is too low, phase can not be read, this assigns all zeros to this case
    PHASE(:,1) = zeros(numel(NOM_IN_FREQ_RAW),1);
else
    PHASE(:,1) = (PHASE_RAW.*(1./CNTR_CLK)-HYST_DELAY_OUT +
     HYST_DELAY_IN)./(1./MEAS_FREQ_IN) * 360;
endif
end

i = 1;
while i <= numel(NOM_IN_FREQ_RAW)
    % find gain of each measurement
    if DVAL(i) == 1
        GAIN(i,1) = GAIN_TABLE(find(GAIN_TABLE(:,1) == DVAL(i)),2);
    else
        GAIN(i,1) = SD_BIT;
    end

    % find acceleration value
    if ACCEL_STATE(i) == 2 || ACCEL_STATE(i) == 4
        PK_ACCEL(i,1) = ((VPK_RAW(i)*AD_CONST)/GAIN(i,1))* SIX_G_VTOA;
        VL_ACCEL(i,1) = ((VVL_RAW(i)*AD_CONST)/GAIN(i,1))* SIX_G_VTOA;
        SS_MRGN(i,1) = ((SS_MRGN_RAW(i)*AD_CONST)/GAIN(i,1))* SIX_G_VTOA;
    else
        PK_ACCEL(i,1) = ((VPK_RAW(i)*AD_CONST)/GAIN(i,1))* TWO_G_VTOA;
        VL_ACCEL(i,1) = ((VVL_RAW(i)*AD_CONST)/GAIN(i,1))* TWO_G_VTOA;
        SS_MRGN(i,1) = ((SS_MRGN_RAW(i)*AD_CONST)/GAIN(i,1))* TWO_G_VTOA;
    end

    % shift phase 360 degrees after asymptote crossing; adjustments to the
    % parameters within this function may need to be modified on a case by
    % case basis.
    if PHASE(i,1) < 9;
        PHASE(i,1) = PHASE(i,1) + 180;
    else
        PHASE(i,1) = PHASE(i,1);
    end

    % get rid of outliers
    if i > 1 && PHASE(i,1) > 100 + PHASE(i-1,1)
        PHASE(i,1) = PHASE(i-1,1);
    end

    i = i + 1;
end

% correct for glitches
PHASE(:,1) = real(PHASE(:,1));

% calculate average input force
INPUT_LBF = v2lbf.*IN_AMP;
% calculate accelerance transfer magnitude
ACCELERANCE(:,1) = PK_ACCEL(:,1)./(INPUT_LBF);
VL_ACCELERANCE = VL_ACCEL(:,1)./(INPUT_LBF);
% calculate input fine gain setting
IN_AMP_FINE_GAIN = 1.5*((IN_AMP_DVAL./256*50000)+5760)./5760+1;

%% plot phase response data points
figure('Name','phase response data points','NumberTitle','off')
clf
hold on
plot(FREQ,PHASE, '.b')
title({['Phase Angle by which AccelerationLAGS Force ','BEAM']},'Fontweight','bold')
xlabel('Frequency (Hz)')
ylabel('Phase (deg.)')
hold off

%% plot accelerance data points
figure('Name','accelerance data points','NumberTitle','off')
clf
hold on
plot(FREQ,ACCELERANCE, '.r')
plot(FREQ,VL_ACCELERANCE, '.b')
title({['Accerlance Data points ','BEAM']})
legend('As calculated from Peak Acceleration','As calculated from Valley Acceleration')
xlabel('Nominal Frequency (Hz)')
ylabel('Accelerance (g/lbf)')
hold off
%% plot acceleration data points
figure('Name','acceleration data points','NumberTitle','off')
clf
hold on
plot(FREQ,PK_ACCEL,'.r')
plot(FREQ,VL_ACCEL,'.b')
title(['Acceleration Data Points ','BEAM'])
legend('Peak Acceleration', 'Valley Acceleration')
xlabel('Nominal Frequency (Hz)')
ylabel('Acceleration (g)')
hold off

%% plot percent difference between input and output frequency
figure('Name','Frequency % Diff','NumberTitle','off')
clf
hold on
plot(FREQ(2:end), (MEAS_FREQ_IN(2:end)-FREQ(2:end))./MEAS_FREQ_IN(2:end).*100,'.b')
plot(FREQ(2:end), (MEAS_FREQ_OUT(2:end)-FREQ(2:end))./MEAS_FREQ_OUT(2:end).*100,'.r')
legend('Measured Input Frequency', 'Measured Output Frequency')
title(['Nominal Frequency % Difference ','BEAM'])
xlabel('Nominal Frequency (Hz)')
ylabel('%Difference')
hold off

%% plot Input Amplitude
figure('Name','Input Amplitude','NumberTitle','off')
clf
hold on
plot(FREQ,IN_AMP,'.b')
title(['Input Amplitude ','BEAM'])
xlabel('Nominal Frequency (Hz)')
ylabel('Amplitude (Vp)')
hold off

%% plot steady state tolerance
figure('Name','Steady State Tolerance','NumberTitle','off')
clf
hold on
plot(FREQ,SS_MRGN,'.b')
title(['Steady State Tolerance ','BEAM'])
xlabel('Nominal Frequency (Hz)')
ylabel('Acceleration (g)')
hold off

%% plot gain factor
figure('Name','Measurement Gain Factor','NumberTitle','off')
clf
hold on
plot(FREQ,GAIN,'.b')
title(['Measurement Gain Factor ','BEAM'])
xlabel('Nominal Frequency (Hz)')
ylabel('Gain Factor')
hold off

%% plot input amplitude gain setting
figure('Name','Input Gain Setting','NumberTitle','off')
clf
hold on
plot(FREQ,IN_AMP_FINE_GAIN,'.b')
title(['Input Fine Gain Factor ','BEAM'])
xlabel('Nominal Frequency (Hz)')
ylabel('Fine Gain Factor')
hold off

%% plot % difference between valley and peak acceleration
figure('Name','magnitude percent difference','NumberTitle','off')
clf
hold on
plot(FREQ,(PK_ACCEL-VL_ACCEL)./PK_ACCEL*100,'.b')
title(['Valley and Peak acceleration % Difference ','BEAM'])
xlabel('Nominal Frequency (Hz)')
ylabel('Valley and Peak acceleration % Difference')
hold off