Empirical Model for the Transconductance-Current Dependence of Short-Channel MOSFETs

Vladimir I. Prodanov

***Abstract*— this work is concerned with the g_m-I dependence of sub-micrometer MOSFETs. The transconductance-current expression given by the Advanced Compact Model (ACM) is reviewed and simple modification is proposed. The modification yields an expression which (with proper parametrization) captures the g_m-I dependence of short-channel MOSFETs. The proposed expression is "universal" in the sense that it is capable of modeling the g_m-I dependence of long-channel MOSFETs, short-channel MOSFETs, and resistively-degenerated BJTs.**

I. INTRODUCTION

Transconductance, commonly denoted g_m, is the slope of the transfer characteristic of a transistor evaluated at the "operating point". For a MOSFET, this is:

$$g_m \equiv \left.\frac{di_D}{dv_{GS}}\right|_{o.p.} \tag{1}$$

The importance of the device transconductance is best understood in regard to an amplifier design. Here we will state several related facts that are very well-known.

1. The voltage gain of single-transistor amplifier cannot exceed the product $g_m R_{Load}$.
2. The mean-squared thermal noise of transistors can be written in terms of their g_m [1]. Therefore, the value of the device transconductance has direct impact upon the noise performance of the circuits implemented.
3. The input linear range of a Common-Source amplifier with no source degeneration is approximately 40% of the I_D / g_m ratio. Similar "rule" applies to Common-Emitter amplifiers: BJT-dictated input linear range is approximately 20% of I_C / g_m, [2].
4. Strong correlation exists between the transconductance value of the device and the power dissipation of the circuit (for Class-A circuits). This is related to the fact that the bias current determines both the g_m of the device and the DC power consumption of the circuit.

The last two facts suggest that the g_m-I dependence of a transistor has an important role in the design of analog circuits. Indeed, there are many publications that teach optimization of CMOS circuits based upon transistor g_m / I ratio [3]-[7]. Most of these publications make use the Advanced Compact MOS Model. The g_m-I relation of a MOSFET in saturation, according to the ACM [3], [8] is:

$$g_m \approx \frac{2}{1+\sqrt{1+\frac{I_D}{I_S}}} \times \frac{I_D}{nU_T} \tag{2}$$

The normalization current, I_S, is defined as follows:

$$I_S \equiv \frac{1}{2} n\mu C_{ox} \frac{W}{L} U_T^2 \tag{3}$$

U_T in (2) and (3) denotes the thermal voltage kT/q and n is the so-called "slope factor" – a dimensionless quantity with value ranging from 1 to 2. More information regarding the slope factor and the origin of expression (2) can be found elsewhere [3], [8]. The rest of the parameters in (3) have their usual meaning.

The ratio of the bias current I_D to the normalization current I_S determines the "inversion level" of the MOS channel. When I_D is much smaller than I_S, the device is in weak inversion and its gate transconductance is proportional to the bias current , $g_m \approx I_D/(nU_T)$; the g_m-I relation resembles that of a BJT. When I_D is much larger than I_S , the device is said to operate in strong inversion. The transconductance of a "long-channel" MOSFET in strong inversion is proportional to the square-root of the bias current. This is consistent with the Shichman-Hodges (Spice Level 1) MOSFET model [9].

Expression (2) is relatively simple and in theory, valid in weak, moderate and strong inversion. This makes it useful for design of analog circuits. The shortcoming of the ACM g_m-I expression is that it fails to capture the g_m-I relation of "short-channel" MOSFETs operated in strong inversion. This shortcoming is related to the fact that the model does not account for the reduction of the carrier mobility with lateral field. A brute-force attempt to include such dependence will complicate the model, diminishing significantly its usefulness for circuit design.

An alternative strategy for improving the accuracy of the model while preserving its simplicity is presented here. The approach is based upon two important observations. Those are discussed in Section II.

II. ONE FUNCTION , TWO DISTINCTLY-DIFFERENT CASES

The "long-channel" MOSFET model (2) belongs to the following general class of functions:

$$g_m = \frac{2}{1+\left(1+ I/I_{norm}\right)^m} \times \frac{I}{V_{norm}} \qquad (4)$$

Here V_{norm} and I_{norm} are "normalization" quantities. They ensure the correctness of the transconductance dimensions (Ampere/Volt).

The impact of the dimension-less exponent m is best understood by examining the behavior of expression (4) for extreme values of the bias current . When $I << I_{norm}$, expression (4) reduces to $g_m = I/V_{norm}$. This means that m has no impact upon the g_m-I behavior for small values of I. When $I>>I_{norm}$, the transconductance becomes proportional to I^{1-m}. If the exponent m has value ½, the g_m will have square-root dependence upon the bias current. If m is 1, the g_m will not be a function of the bias current. Increasing the value of m from ½ to 1 "flattens" the *gm-I* curve. This is illustrated in Fig. 1. Also illustrated, is that making m larger than unity leads to a curve with a non-monotonic behavior.

In the following we will show that the *gm-I* expression of a resistively-degenerated BJT also belongs to the same family of functions. Hence, expression (4) is not specific to a "long-channel" MOSFET.

The effective transconductance of a resistively degenerated BJT, see Fig. 2, can formally be defined as:

$$g_{m(eff)} \equiv \left.\frac{di_C}{dv_{BE'}}\right|_{i_C=I} \qquad (5)$$

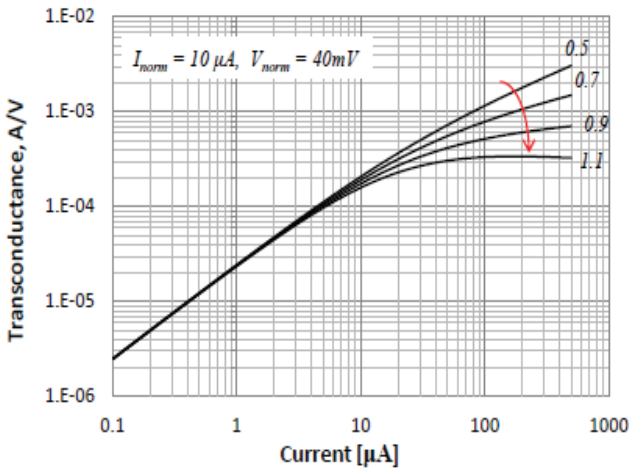

Figure 1. A log-log plot of a family of g_m-*I* curves with fixed I_{norm} , fixed V_{norm} and m varied from *0.5* to *1.1* in steps of *0.2*.

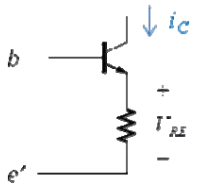

Figure 2. Schematic of an emitter-degenerated Bipolar Junction Transistor

Using "small-signal" analysis and/or the concept of feedback and loop gain, the $g_{m(eff)}$ can be expressed in terms of the collector bias current I and the voltage drop V_{RE} as follows:

$$g_{m(eff)} = \frac{I}{U_T + V_{RE}} \qquad (6)$$

Expression (6) can also be rewritten as:

$$g_{m(eff)} = \frac{2}{1+\left(1+ I/I_{norm}\right)^1} \times \frac{I}{U_T} \qquad (7)$$

Expression (7) clearly shows that the *gm-I* dependence of Fig. 2 circuit is of the general form (4) where m has value *1*. The normalization current here is given by $I_{norm}=V_T/(2\alpha R_E)$ where α is the common-base current gain of the BJT.

One wonders whether the g_m-I relation of a short-channel MOSFET is also member of the same family of functions. In Section III we argue that this is indeed the case. We show that it is possible to find a set of values for I_{norm}, V_{norm} and m to accurately curve-fit the g_m-I dependence of sub-micrometer MOSFETs.

III. CURVE-FITTING OF SPICE-DERIVED DATA

The g_m-I dependence of N-channel and P-channel devices from 6 different sub-micrometer CMOS processes were extracted using Spice. The transconductance was obtained by performing "operating point" analysis upon transistors connected in a "diode" configuration. Diode connection was used because it ensures active mode of operation irrespective of the value of the bias current and allows for a comparison of processes with different nominal supply voltages.

All six processes are available via MOSIS [10] and have feature size of 0.35μm, 0.25 μm and 180nm. The W/L of the devices studied is 10 and the drawn length L is the minimum one allowed by the respective technology. BSIM3v3 (HSPICE Level-49) models, found on MOSIS parametric datasheets [11], were used. Data were curve-fitted by adjusting I_{norm}, V_{norm} and m to minimize the maximum percent error.

A maximum error of less than 6% was achieved in all but one of the cases. Exemplary, Spice-extracted data and their corresponding curve-fitting functions are presented in Fig. 3, Fig. 4 and Fig. 5. The results for all cases considered here are summarized in Table I and Table II.

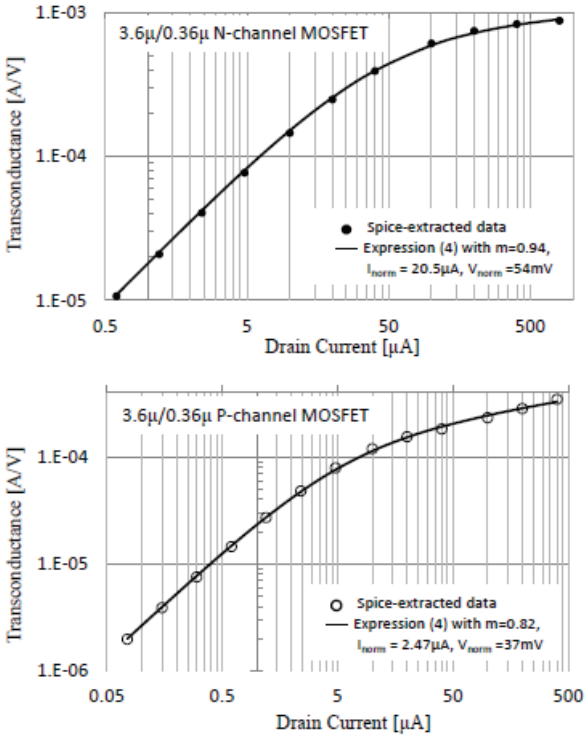

Figure 3. Spice-extracted gm-I data of an N-channel and a P-channel MOSFET from a representative 0.35µm process fitted using expression (4).

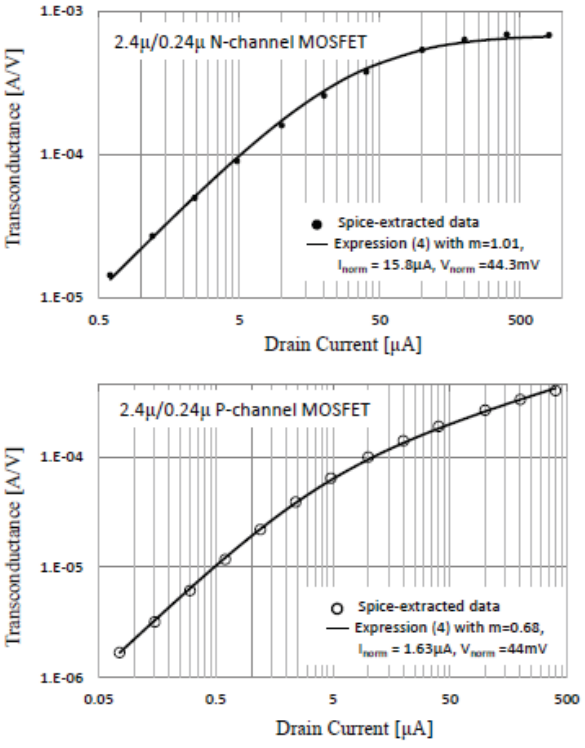

Figure 4. Spice-extracted gm-I data of an N-channel and a P-channel MOSFET from a representative 0.25µm process fitted using expression (4)

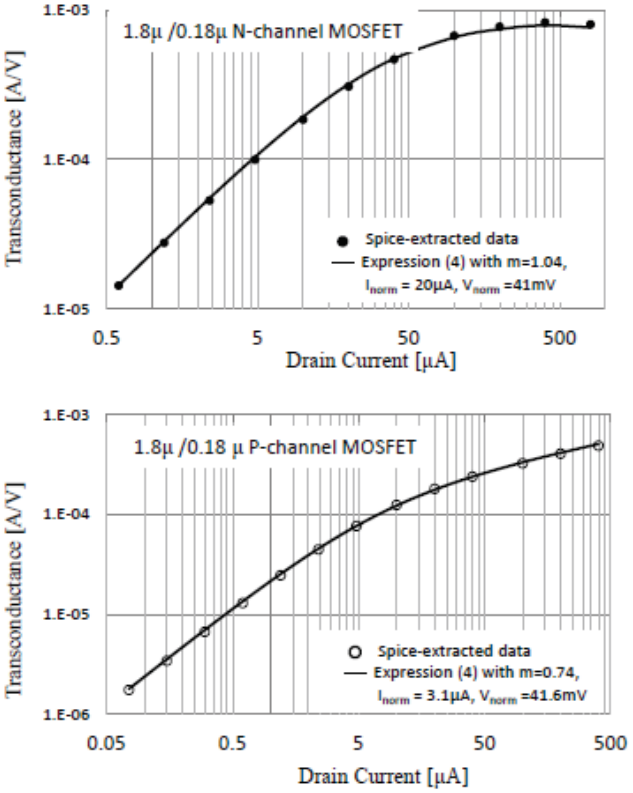

Figure 5. Spice-extracted gm-I data of an N-channel and a P-channel MOSFET from a representative 180nm process fitted using expression (4).

TABLE I. FITTING PARAMETERS AND MAXIMUM ERORR FOR SIX N-CHANNEL MOSFETS. ALL W/L = 10.

Process	Vendor	Drawn L_{min}	Fitting Parameters			Max. Error
			m	I_{norm}	V_{norm}	
0.35µm	# 1	0.4µm	0.91	14.0µA	52.0mV	4.7%
	# 2	0.36µm	0.94	20.5µA	54.0mV	4.2%
0.25 µm	# 1	0.24µm	0.87	9.9µA	43.5mV	6.0%
	# 2	0.24µm	1.01	15.8µA	44.3mV	7.5%
0.18 µm	# 1	0.18 µm	1.04	20.0µA	41.0mV	4.7%
	# 2	0.18 µm	0.98	16.6µA	43.9mV	6.0%

TABLE II. FITTING PARAMETERS AND MAXIMUM ERROR FOR SIX P-CHANNEL MOSFETS. ALL W/L=10.

Process	Vendor	Drawn L_{min}	Fitting Parameters			Max. Error
			m	I_{norm}	V_{norm}	
0.35µm	#1	0.4µm	0.71	1.65µA	44.5mV	4.3%
	# 2	0.36µm	0.82	2.47µA	37.0mV	5.2%
0.25 µm	# 1	0.24µm	0.70	1.81µA	44.0mV	4.4%
	# 2	0.24µm	0.68	1.63µA	44.0mV	5.2%
0.18 µm	# 1	0.18 µm	0.74	3.1µA	41.0mV	4.7%
	# 2	0.18 µm	0.77	2.82µA	43.9mV	6.0%

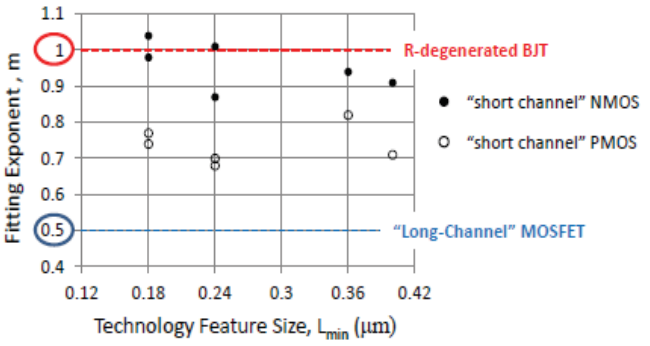

Figure 6. Exponents *m* as a function of technology feature size and device type.

As shown in Table I, modeling the g_m-*I* dependence of N-channel devices (operated in strong inversion) requires exponents with values ranging from 0.9 to approximately 1.05. This implies that modern N-channel MOSFETs have g_m-I dependence that resembles the gm-I dependence of an emitter-degenerated BJT! The results presented in Table II demonstrate that modern P-channel MOSFETs are neither "long-channel" devices nor "degenerated BJTs". Their exponents range from 0.7 to 0.8 – nearly equidistant from 0.5 and 1.0. These observations are depicted graphically in Fig. 6.

IV. Conclussions

"Universal" g_m-I expression is presented. The proposed model was shown capable of capturing the transconductance-current dependence of "long-channel" MOSFETs, "short-channel" MOSFETs and BJTs with resistive emitter degeneration. The presented model was validated by curve-fitting of gm-I data obtain from Spice simulations. Despite its non-physical nature, the g_m-*I* model has been found invaluable for classroom instruction, by-hand design of analog circuits and comparison of CMOS technologies having different supply voltages and feature size.

Acknowledgment

The author would like to thank his former student Mr. Michael Spahn for collecting the Spice data used in this study.

References

[1] P.R. Gray, P.J. Hurst, S.H. Lewis and R.G. Meyer, Analysis and Design of Analog Integrated Circuits, 4th ed., John Wiley & Sons, 2001, pp.758-759

[2] R. C.Jaeger and T. N. Blalock, Microelectronics Circuit Design, 4th ed., McGraw Hill, 2011, pp. 817-818.

[3] F. Silveira, D. Flandre, and P. G. A. Jespers, "A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *IEEE J. Solid-State Circuits,* vol. 31, pp. 1314–1319, Sept. 1996.

[4] A. I. A. Cunha, M. C. Schneider, and C. Galup-Montoro, "An MOS transistor model for analog circuit design", *IEEE J. Solid-State Circuits*, vol. 33, no 10, pp. 1510-1519, October 1998.

[5] S. Yan and E. Sánchez-Sinencio, "Low voltage analog circuit design techniques: A tutorial," *IEICE Trans. Fund.*, vol. E83, no. 2, pp. 1–17, Feb. 2000.

[6] A. Girardi, and S. Bampi, "Power Constrained Design Optimization of Analog Circuits Based on Physical gm/ID Characteristics", *Journal of Integrated Circuits and Systems*, Vol. 2, No. 1, pp. 22-28, 2007.

[7] P. Jespers, The gm/ID Methodology, A Sizing Tool for Low-Voltage Analog Cmos Circuits, Springer, New York, NY, USA, 2009.

[8] O. C. F. Gouveia, A. I. A. Cunha, M. C. Schneider, and C. Galup-Montoro. The ACM model for circuit simulation and equations for SMASH. [Online], available from http://www.dolphin.fr

[9] H. Shichman and D. A. Hodges. "Modeling and simulation of insulated-gate field-effect transistor switching circuits." *IEEE J. Solid State Circuits*, SC-3, pp. 285-289, Sept. 1968.

[10] MOSIS Fabrication Precesses, http://www.mosis.com/products/fab-processes

[11] Wafer Wafer Electrical Test Data and SPICE Model Parameters, http://www.mosis.com/pages/Technical/Testdata/index