Modeling and Simulation of Paralleled Series-Loaded-Resonant Converter

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Abstract

This paper presents the development of a circuit modeling for paralleled Series Loaded Resonant (SLR) converter used in an experimental power supply to drive high voltage and high frequency medical equipment. The circuit model for each individual converter is first described. Once the complete model of an individual converter is achieved, the model is then extended to include the parallel connection. To verify the validity of model, the design of paralleled SLR using the model is explained. The component values obtained are then being used in Pspice simulations to further prove the validity of the model.

1. Introduction

One of the trends in the Power Electronics field is the pursuit of highly efficient power supplies. This has motivated engineers to come up with new designs that drastically improve power conversion. Switching power supplies have an efficiency of up to 90% compared to the 30% to 60% of regular linear power supplies making them highly efficient. These power supplies transform energy by basically turning on and off the input voltage very fast, so the output voltage is the average of the switched input voltage over a period of time.

The efficiency of a converter is determined by how well the input power is being processed to deliver the desired output power to the load. Efficiency then is the ratio of the average output power over the average input power. As previously stated, switching power supplies provide an efficiency of up to 90%, and the remaining 10% or more is the power that "stays" in the power converter in the form of semiconductor forward drop loss, AC switching loss, and DC conduction loss, among others.

A resonant converter is a power supply topology that enables improved efficiency by introducing sinusoidal switching waveforms instead of the more commonly used square switching waveforms [1]. This causes the provision of Zero Current Switching (ZCS) and the Zero Voltage Switching (ZVS) modes. With these modes, the switch in the converter is turned on or off when the current or voltage across it is zero, thus switching losses are minimized [2].

To produce the sinusoidal waveforms, the resonant converter utilizes an LC resonant tank circuit. Another main advantage of having sinusoidal switching besides efficiency is that the total harmonic distortion and electromagnetic interference will also be reduced which are important in many applications that require a "quiet" power supply.

Due to the aforementioned advantages, resonant converter is an obvious choice for high-voltage high-frequency power supplies commonly found in medical equipment [3]. This paper presents one type of resonant converter called the Series Loaded Resonant (SLR) converter. In order to achieve adjustable output power while keeping the size of the converter relatively small, two SLR circuits are connected in parallel. The output is then adjusted by phasing the output of one converter with respect to the other. Although references for designing individual series loaded resonant converter can be found in many power electronic text books; however, unfortunately, due to the relatively new approach, there is not any design reference for parallel connected SLR.

In this paper, the derivation of a circuit model for paralleled SLR converter will be presented. To do so, circuit model of individual SLR is first derived by breaking the converter down into its functional blocks. Once completed, the paralleled SLR model can then be achieved by expanding the individual SLR circuit model.

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2. SLR Circuit Characteristics

One simple method to understand the characteristics of resonant topologies is by looking at their gain curve plot. Figure 1 shows the gain curves for the series resonant tank when excited by a square waveform generated by a half-bridge converter [4].

The curves show that if the resonant converter operates above the resonant frequency (the right side of the gain curve), then the controller won't be able to regulate the output voltage. The same is true when the opposite condition occurs. The curves also suggest that as the load increases, Q decreases. The gain curve becomes flat, and thus to maintain the desired output voltage, significant frequency changes are needed. Therefore, regulation at open circuit is impossible since there is no resonant peak or selectivity. This means, to achieve a better control in series resonant converter, a high Q value is desirable. However, the trade-off is that if Q is too high, then the process of controlling the output becomes very non-linear. This implies that a small change in the switching frequency could generate a big change in the output voltage and the controller could even move the operating frequency too close to the resonant peak. This would in turn completely destabilize the power supply.

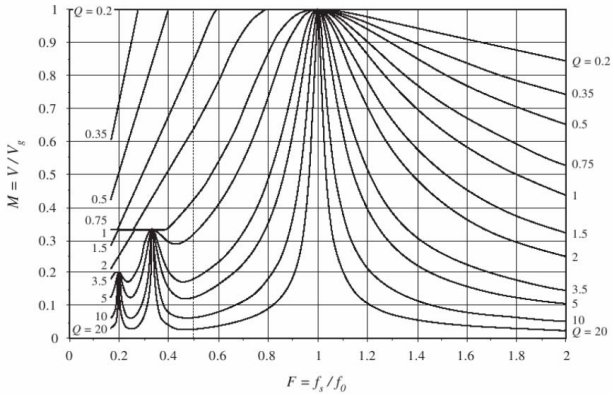

Figure 1. Series resonant gain curves

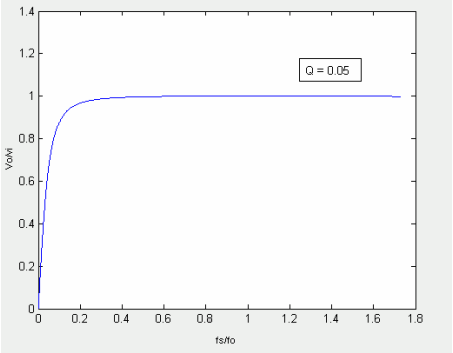

Figure 2. Series Converter's Gain Curve at very low Q

To avoid the nonlinear gain curve characteristics, the converter will be operated with a very low Q so the curve will be flat at virtually any frequency as seen in Figure 2. Further observation of Figure 2 raises a problem of controlling the output voltage; how can the output be controlled when at any frequency the voltage remains the same? The proposed architecture solves this problem, it consists of two regular series resonant loaded converters placed in parallel where the output voltage is the sum of both converters. So to control the output voltage, the phase of the resonant current in one of the converters is changed. For example, since the waveforms are sinusoidal, to obtain a zero output voltage, the waves will have to be 180 degrees apart. On the other hand, to increase the output voltage, the phase difference will be decreased until it reaches zero where the maximum output voltage occurs.

3. Individual SLR Model

A simple half-bridge series resonant loaded converter is depicted on Figure 3. It consists of five blocks: the switches, resonant tank, transformer, rectifier and filter network. To model the converter, the sinusoidal analysis will be applied since the small ripple approximation is not applicable due to the nature of the converter's currents and voltages, i.e. they are sinusoidal and therefore their variations are large. To obtain the mathematical model, the converter will be analyzed block by block and at the end the final gain equation will be presented.

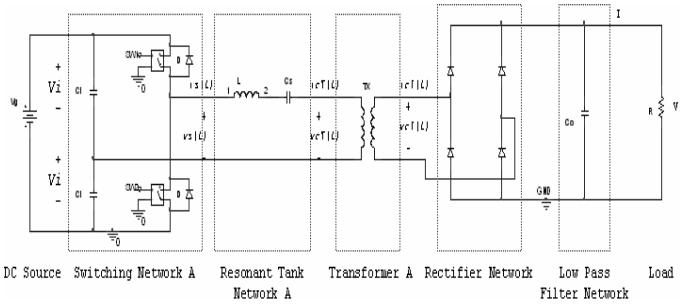

Figure 3. Basic SLR circuit

The switch network converts the DC input voltage into a square wave voltage. Equation (1) shows the square wave in the form of the Fourier series:

$$V_{s1}(t) = \frac{V_i \cdot 2}{\pi}\left[\cos(n\omega_o t) + \sin(n\omega_o t)\right], n = 1 \quad (1)$$

The input current can be expressed as the average current that circulates through the switches when they are turned on and off, as shown in equation (2). Since

this current is fed to the resonant tank circuit, it can be well approximated to a half-sinusoidal form.

$$\left\langle i_g(t)\right\rangle_{T_s} = \frac{1}{T_s}\int_0^{T/2} I_{s1}\sin(\omega_s t-\varphi_s)\partial t = \frac{I_{s1}\cos(\varphi_s)}{\pi} \quad (2)$$

where I_{S1} is the peak amplitude, and φ_S is the phase introduced from the LC components of the circuit. The circuit model for the switching network is shown in Figure 4.

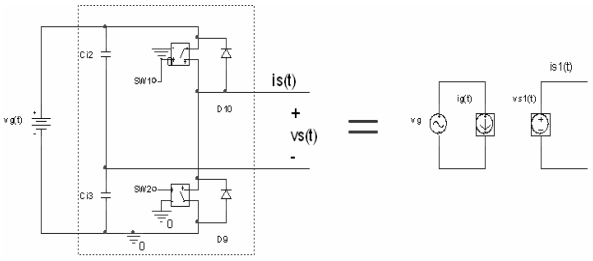

Figure 4. Switching network model

Rectifier and capacitive filter blocks convert the square wave voltage from the resonant tank network into a dc voltage. The large output capacitor filters the signal, and since the ac component is very small we can make the small-ripple approximation that the output voltage and current are considered dc. The rectifier input current is a sinusoidal current coming from the tank network and it can be represented as in equation (3).

$$i_r(t) = I_{r1}\sin(\omega_o t-\varphi_r) \quad (3)$$

where ω_o is the resonant frequency and φ_r is a phase shift in the current. Then, the current that circulates through the load is a dc current and it is actually the average of the rectified current:

$$I = \frac{2}{T}\int_0^{T_s/2} I_{r1}\cdot\left|\sin(\omega_s t-\varphi_r)\right|\partial t = \frac{2}{\pi}I_{r1} \quad (4)$$

Since the resonant tank network mainly responds to the fundamental component of its input voltage, the fundamental component can be represented as:

$$v_{r1} = V_{r1}\sin(\omega_s t-\varphi_r) \quad (5)$$

where,

$$V_{r1} = \frac{4V}{\pi} \quad (6)$$

Finally, the rectifier's effective resistive load presented to the transformer is:

$$R_{e1} = \frac{v_{r1}(t)}{i_{r1}(t)} = \frac{V_{r1}\sin(\omega_o t-\varphi_r)}{I_{r1}\sin(\omega_o t-\varphi_r)} = \frac{8V\sin(\omega_o t-\varphi_r)}{\pi^2 I\sin(\omega_o t-\varphi_r)} \quad (7)$$

which can be simplified to:

$$R_{e1} = 0.8106R \quad (8)$$

The equivalent circuit for the rectifier and filter network is shown in Figure 5.

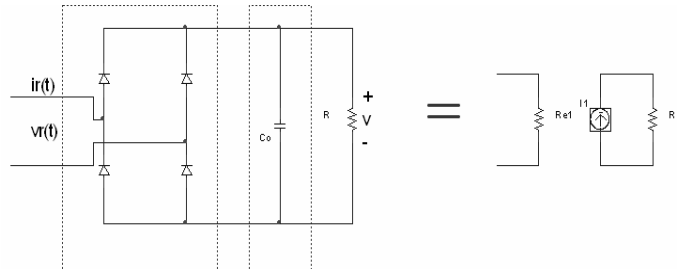

Figure 5. Rectifier and output filter model

The purpose of the transformer is to amplify the voltage coming out of the tank network and a simple model of this block is the transformer turns ratio. To include this amplification in the resonant tank network model, the effective resistance found previously has to be reflected into the transformer primary side:

$$R_T = \frac{R_{e1}}{B^2} \quad (9)$$

where B is the secondary winding turns. The circuit model for the transformer with the LC tank is shown in Figure 5.

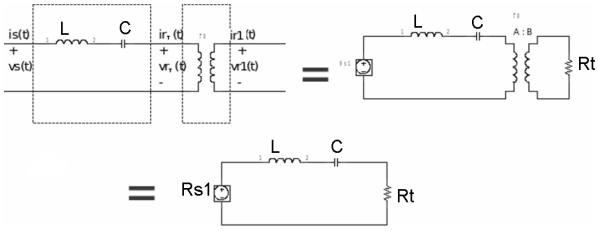

Figure 5. Rectifier and output filter model

Now that we have all the circuit blocks modeled, we can then cascade them together as shown in Figure 6.

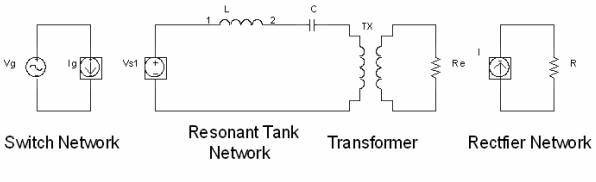

Figure 6. The complete model of individual SLR

4. Paralleled SLR Model

The previously obtained model for individual SLR converter can now be expanded to model the paralleled series loaded converters. As before, the sinusoidal analysis is being used again with minor changes. The transformer model and the controlled switch network model remain the same for each of the series converter (where the top converter will be named A, and the bottom one B). Figure 7 illustrates a model based on two series loaded resonant converter in parallel in which the output voltage is the sum of both before the voltage is rectified. This is done by adding the voltages and currents from the transformers' secondary winding.

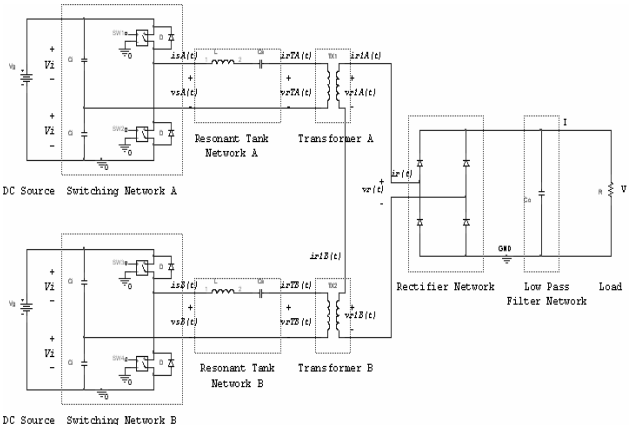

Figure 7. The complete model of parallel SLR

Converter A generates a sinusoidal current whose average current is shown in equation (4). As for converter B, the current generated has a controlled change of phase α and this will control the output of the paralleled SLR converter. The average value of this current is shown in equation (10).

$$I_B = \frac{2}{T_s}\int_0^{T_s/2} I_{r1B}\left|\sin\left(\omega_s t-\varphi_r-\alpha\right)\right|\partial t = I_{r1B}\Lambda \qquad (10)$$

where:

$$\Lambda = \int_0^{T_s/2}\left|\sin\left(\omega_s t-\varphi_r-\alpha\right)\right|\partial t \qquad (11)$$

The input current to the rectifier is the sum of the output currents from each of the transformers and its average current is shown in equation (12).

$$I = \frac{2}{T_s}\int_0^{T_s/2} I_{r1A}\left|\sin\left(\omega_s t-\varphi_r\right)\right| + I_{r1B}\left|\sin\left(\omega_s t-\varphi_r-\alpha\right)\right|\partial t \qquad (12)$$

I_{r1A} and I_{r1B} have the same peak to peak current value with a phase difference α, so that:

$$I = \frac{I_{r1}2}{T_s}\int_0^{T_s/2}\left|\sin\left(\omega_s t-\varphi_s\right)\right| + \left|\sin\left(\omega_s t-\varphi_s-\alpha\right)\right|\partial t \qquad (13)$$

The value of I varies with α and it has to be recalculated every time α changes to obtain the right average value.

The input voltage to the rectifier is the sum of the output voltages from each of the transformers as expressed in equation (14), neglecting any harmonics that these voltages may have.

$$v_{r1}(t) = \frac{4V}{\pi}\left(\sin\left(\omega_s t-\varphi_r\right)+\sin\left(\omega_s t-\varphi_r-\alpha\right)\right) \qquad (14)$$

Finally, the effective resistance to the transformers may be expressed in equation (15)

$$\frac{v_{r1}(t)}{i_{r1}(t)} = R_{e1} = \frac{\frac{4V}{\pi}\left(\sin\left(\omega_s t-\varphi_r\right)+\sin\left(\omega_s t-\varphi_r-\alpha\right)\right)}{\frac{I}{\lambda}\left(\sin\left(\omega_s t-\varphi_s\right)+\sin\left(\omega_s t-\varphi_s-\alpha\right)\right)} \qquad (15)$$

The resonant tank networks are the same as for the individual SLR converter. The effective resistance can be calculated for each of the converters by applying the superposition theorem. The effective resistance presented to the tank networks previously has to be reflected to the primary of the transformer. Equations (16) and (17) show these resistances after properly being reflected.

$$R_{TA} = \frac{R_{e1A}}{B^2} \qquad (16)$$

$$R_{TB} = \frac{R_{e1B}}{B^2} \qquad (17)$$

where:

$$R_{e1A} = \frac{\frac{4V}{\pi}\sin\left(\omega_s t-\varphi_r\right)}{\frac{I_A\pi}{2}\sin\left(\omega_s t-\varphi_s\right)} \qquad (18)$$

$$R_{e1B} = \frac{\frac{4V}{\pi}\sin\left(\omega_s t-\varphi_r-\alpha\right)}{\frac{I_B 2}{\pi}\sin\left(\omega_s t-\varphi_s-\alpha\right)} \qquad (19)$$

Figure 8 illustrates the complete model of the paralleled SLR converter. Using this complete model, nominal values for the main components may now be calculated. After the values are obtained, computer simulation may then be performed which will be described in the following section.

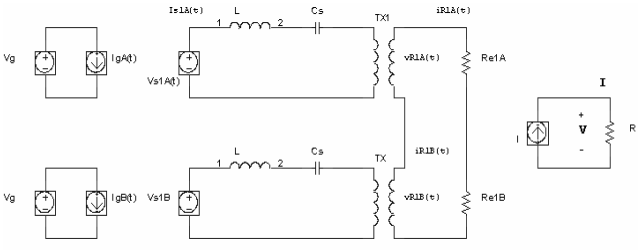

Figure 8. The complete model of parallel SLR

5. Component Selections and Computer Simulation

To verify the validity of the model, a 550V output paralleled SLR converter is designed and explained in this section. To avoid audible noise coming from the converter, the switching frequency will be set at 25 kHz. The resonant tank network will be tuned to resonate a little bit higher than 50 kHz. Based on these parameters, and using the equations previously derived in the modeling of paralleled SLR converter, the values of main components are obtained as shown in table 1.

Table 1. The complete model of parallel SLR

Components	Electrical Characteristics
MOSFET IRF740A	V_{dds} = 400V I_d = 10A
Recovery Diodes D RURP8100	V_{rrm},V_{rwm},V_r = 1000V I_f = 8A
Diode Bridge	1000V @ 1A
Transformers TX1 and TX2	Tx ratio 1:6 , Lp =28uH Ls = 1004uH
Tank Inductor L	L = 10uH
Tank Capacitor	Cs = 200nF @ 300V
Input Capacitors Ci	470uF @ 300V
Filter Capacitor Co	1uF @ 1000V

These component values are then incorporated into Pspice schematic to simulate the circuit to prove the validity of the model and to exhibit the performance of the paralleled SLR converter. Figure 9 shows the Pspice schematic used for the computer simulation of paralleled SLR. Figure 10 shows the output voltages at different phase delays from the simulation results. It can be noted that even if the phase delays have been equally spaced, the output voltage is not linear and this is due to the nonlinearity of the sum of two sinusoidal waveforms. It was also observed that as the output voltage increases, the less time it takes for the converter to reach steady state, in the same way when the output filter capacitor increases the settling time increases too. For example, when the phase delay is zero and a capacitor of 1uF is used, the converter reaches steady state at 530V in 3.5ms and 563V in 2.6ms. When a capacitor value of 100nF is used the converter reaches steady state at 530V in 340us and 563V in 200us. This is something very important to note because it introduces longer or shorter dead times than expected into the control system which in turn may lead to instability.

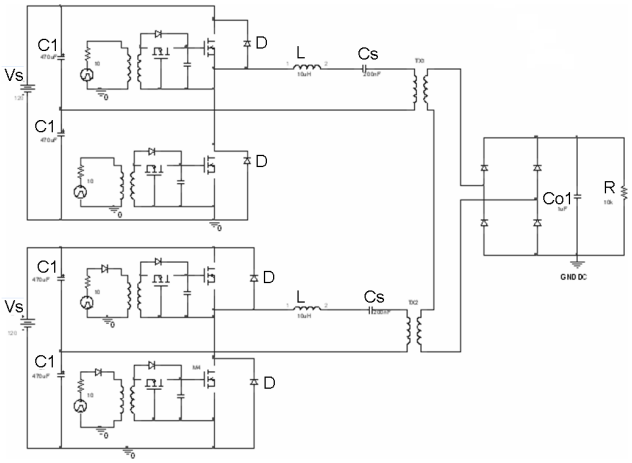

Figure 9. Pspice schematic of parallel SLR

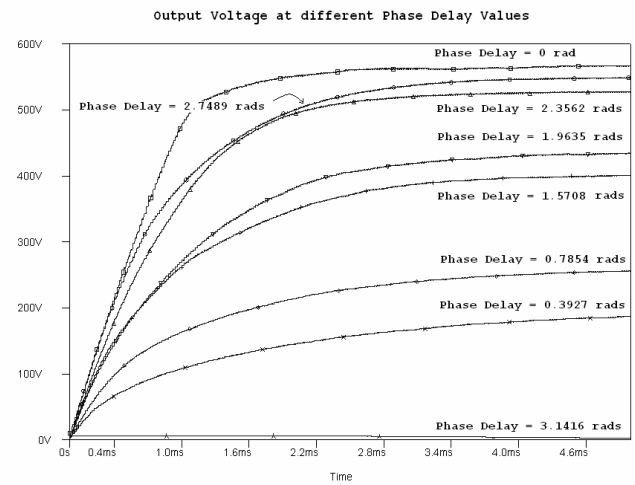

Figure 10. Output voltage with varying phase delays

Table 2 and Figure 11 show the efficiency obtained from the simulation results of the converter as a function of phase delays. As shown, with the phase

delay increases, the efficiency decreases because both converters are always running at their maximum regardless what value the output voltage has. When the phase delay is zero, both voltages will be in phase and all the energy will be delivered to the load. On the other hand, when the phase delay is set higher than 0 μs, the sum will partially cancel both voltages. The output will decrease but the series converters will still use as much energy as if the output voltage was set to 720 or a phase delay of zero.

Phase Delay / Efficiency	Input Power Watts rms	Output Power Watts rms	Efficiency %
0 sec	37.43	31.01	82.85
4 μsec	26.86	19.57	72.86
8 μsec	23.61	17.02	72.08
12 μsec	31.87	23.25	72.95
16 μsec	25.67	16.47	64.16
20 μsec	8.40	3x10-3	0.36

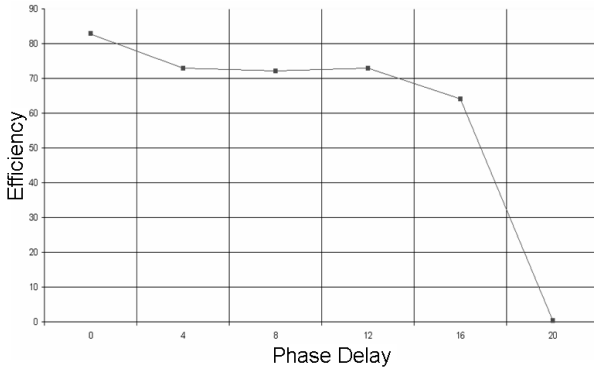

Figure 11. Efficiency with varying phase delays

6. Conclusion

The derivation of circuit modeling for individual series loaded resonant converter was presented. The model was developed by breaking down the converter circuit into several functional blocks. Results from each block were then cascaded to form the complete model a single series loaded resonant converter. The complete model was then used with slight modifications to expand the model to include two series loaded resonant converter connected in parallel.

To verify the validity of the model, a paralleled SLR converter was designed. The main components of the converter were computed by using the derived model. Computer simulations were then performed as a means to further prove the validity of paralleled SLR converter using the obtained component values. The results showed that the model indeed yielded the expected results. Hence, the derived model is useful not only in gaining more insight into designing the converter, but also particularly useful in helping to select main components of the paralleled SLR converter.

In addition to the computer simulations already performed to provide the proof of the validity of the model; however, further verification through hardware implementation will be best. Lab prototype of the paralleled SLR is currently being developed and results from these hardware measurements will be presented in a future paper.

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