California Polytechnic State University

Broadband PIN Diode Attenuator

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Abstract

Keywords: PIN Diode, Pi Network, Variable Attenuator, RF electronics

The design and implementation of a high power (+28dBm) broadband attenuator is explored in this senior project paper. The attenuator is a current controlled variable PIN Diode attenuator in the balanced Pi network configuration. The advantages of this implementation are shown versus other circuit configurations. Circuit limitations are given and the document includes areas for further research and information on improvements should this design be productized.

Acknowledgments

I would like to thank Dr. Paul Greiling for providing his expertise on semiconductor device physics and his knowledge of industry practices.

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I. Introduction

RF Systems are an integral part of life for a large portion of the world. Most of us would be hard pressed to go a day without using an RF device; cell phones, digital cable, even cordless land lines phones are all examples of RF devices. Almost all communication devices have RF components (transmitters, receivers, mixers, multiplexers, attenuators, amplifiers, modulators, demodulators, VCO's, PLL's, etc.) and some require specific power levels to run correctly. These power levels differ from one component to the next in a system, thus the need for amplifiers and attenuators. This senior project focuses on a specific type of attenuator, the balanced Pi network PIN Diode Attenuator.

PIN Diode Attenuators are a subset of variable RF attenuators and are useful for circuits requiring continuously changing attenuation levels [1]. PIN diodes have advantages over resistive networks and are the ideal RF component for these types of attenuators. Resistive network attenuators provide a theoretically unlimited bandwidth (resistor construction ultimately limits this ideal) but require many stages to provide good attenuation accuracy [1]. Each successive stage in these resistive networks introduces another source of impedance mismatch and the switches used can introduce noise to these systems [1]. PIN diode attenuators can provide excellent dynamic range and accuracy in as little as one stage; which eliminates the inherent problems with resistive network attenuators.

II. Background

A. PIN Diode Physics

PIN Diodes differ from their PN diode counterparts in the basic construction of the diode. A PIN Diode is designed with **P**- and **N**- type doped layers separated by a thick **I**ntrinsic layer (literally stacked with **P-I-N** regions). This intrinsic layer creates the effect of a diode with a wide depletion region. It is this I-region that gives the PIN Diode its specific properties. For proper performance it is critical that the I-region be free of impurities since impurities degrade the frequency performance and limit the RF loss in reverse bias. The ideal PIN diode is free of impurities in the I-region, however, a truly intrinsic layer, free of impurities, is impractical. Typical I-region resistivities are in the range of 8,000 to 12,000 Ohm-cm [1].

At zero-bias, the diode behaves as an open circuit to RF signals, provided that the signal is of sufficient frequency [1]. The specific frequency that a PIN diode becomes an open circuit is strongly dependent on the I-region of the diode. However, the I-region contains minute space charges capable of transmitting a signal. These space charges introduce extra noise and loss in the RF system. In order to remove these space charges, a small reverse bias is required to deplete the I-region and must be considered in the design of properly functioning RF circuits. This reverse bias voltage level is commonly referred to as the “punch-through” voltage.

Minority carrier lifetime is the low frequency limiting factor of PIN Diodes. It is defined as the interval between the creation and recombination of minority carriers. The two types of recombination are bulk recombination and surface recombination. Bulk recombination is the electron-hole recombination that occurs within a particular region of a semiconductor device. This recombination is largely dependent on the thermal equilibrium condition

$$pn = n_i^2 \qquad \text{Eq. 1}$$

Where n_i is the carrier density of the bulk substrate, p is the concentration of hole carriers and n is the concentration of electron carriers. In the ideal I-region p = n and the recombination time would be infinite because each recombination would create another electron-hole pair. However, p ≠ n in real PIN diodes so the recombination does not always result in another

electron-hole pair. This gives PIN diodes a finite bulk recombination time. As a general rule of thumb, the more heavily doped the majority carrier the higher the rate of recombination (PN junction diodes have recombination times on the order of 10ns, whereas PIN diode recombination times are on the order of 1000ns).

The other type of recombination is surface recombination. Surface recombination occurs at the surface between two substrates as well as the edge of a given PIN diode wafer. The recombination at the edge of the wafer occurs because cutting the wafer causes a deformation of the crystalline structure and creates "traps" for recombination [1]. The surface recombination at the interface between P- and I- regions as well as I- and N-regions is due to the diffusion lengths between the two layers. These impurities cause the recombination at the surfaces to occur at a higher rate than the bulk recombination. The effective recombination lifetime is

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{surface}} + \frac{1}{\tau_{bulk}} \qquad \text{Eq. 2}$$

Chip geometry is an important factor in determining the minority carrier lifetime. Figure 1 shows the typical PIN diode construction on a wafer. The width of the I-region and its direct effect on the effective minority carrier lifetime is shown in Figure 2.

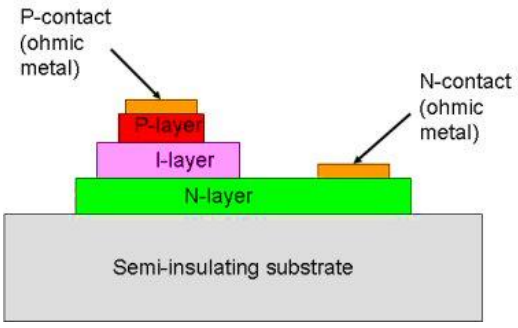

Figure 1 - Typical PIN wafer construction. The diode can also be stacked in reverse (NIP construction), P and N layers may also be stacked upon a long I-region. The latter is the configuration that allows for the greatest resistance variation.

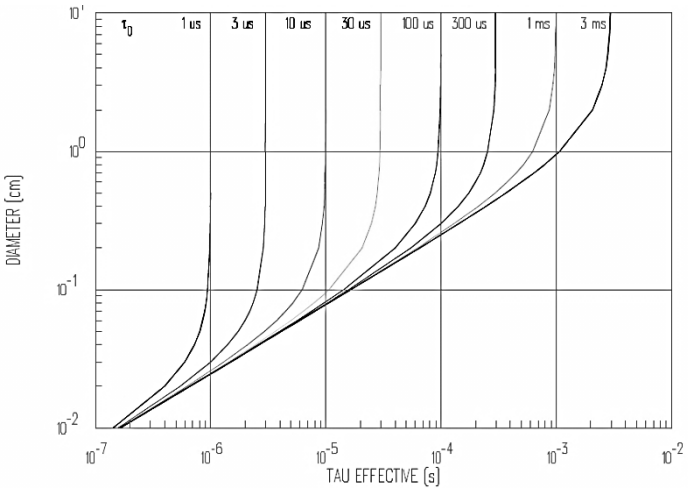

Figure 2 - Tau effective vs. I-region width. The graph shows that as the width of the I-region is decreased the minority carrier lifetime increases. This is due to the changing ratio of surface to bulk recombination.

When a PIN Diode is forward biased, charge carriers are injected into the I-region and they have a finite time before they recombine in accordance with the minority carrier lifetime. The charge density and volume of the I-region determine the effective resistance of the device. At higher forward bias levels, more charge carriers are injected into the I-region giving the PIN Diode a low effective resistance and higher current. The forward current of the diode is related to the total stored charge in the I-region by

$$I_f = \frac{dQ}{dt} + \frac{Q}{\tau_{eff}} \qquad \text{Eq. 3}$$

where Q is the total charge stored. At frequencies well below the carrier frequency ($1/\tau_{eff}$) a PIN Diode behaves the same as a PN junction diode. At high frequencies, approximately $10f_c$, the resistance of the I-region becomes linear given by

$$R_f = \frac{W^2}{2d\tau I_f} \qquad \text{Eq. 4}$$

where *d* is the diffusion constant of the substrate, W is the width of the I-region, τ is the effective recombination time and I_f is the forward current. This implies, as expected, that the resistance of the PIN Diode is only dependent on the I-region geometry and the forward current of the diode. An example of PIN Diode resistance vs. forward current is shown in Figure 3.

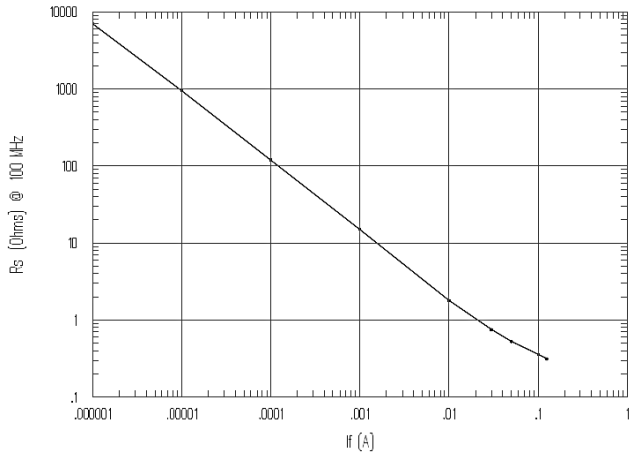

Figure 3 - The RF resistance vs. Current for a sample PIN Diode. Notice that there is a 5 octave change in resistance for a 5 octave change in current, indicating a linear relationship.

High frequency limitations of PIN diodes are dependent on I-region geometry. The I-region effectively sets the reverse bias capacitance of the diode. This capacitance is modeled as parallel to the variable RF resistance of the diode, and for high frequency operation it is desirable to have this capacitance minimized. Typical values for this junction capacitance are in the range of 20 – 50pF. As frequency is increased this capacitance begins to look

like a short circuit and will allow bypassing of the signal without attenuation.

B. PIN Diode Attenuators

As mentioned in the introduction, PIN Diode attenuators are useful for circuits involving continuously changing attenuation levels. These attenuators come in a variety of configurations, TEE and PI configurations are the most common. Resistive network models of TEE and PI attenuators and the equations for calculating resistor values are shown in Figures 4 and 5 respectively. These models are for specific attenuation levels; to create a variable attenuator, variable resistors must be used.

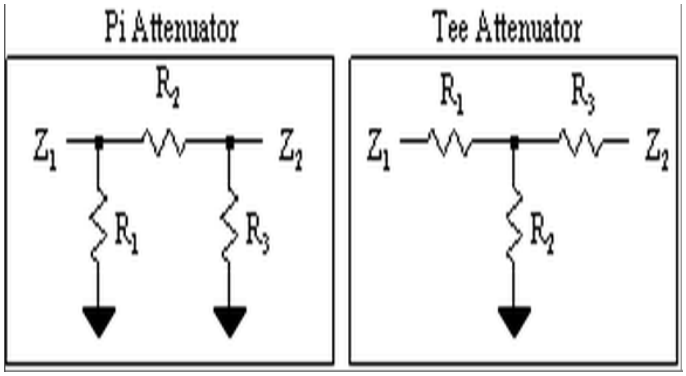

Figure 4 - Resistive network TEE and PI attenuators. These provide constant attenuation. [7]

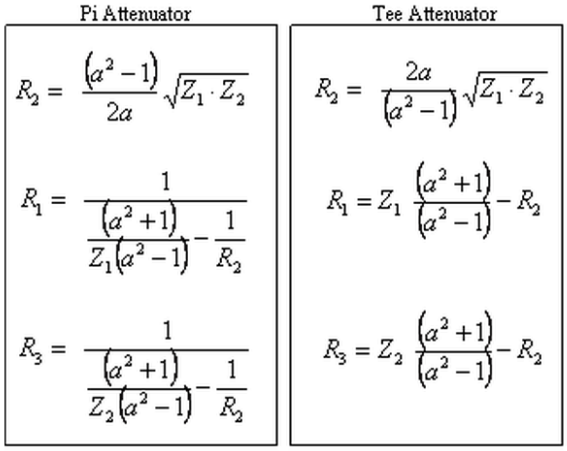

Figure 5 - Equations to determine the attenuation of TEE and Pi resistive attenuators. Z_1 is the input characteristic impedance, Z_2 is the output characteristic impedance, and a is the desired attenuation level. [7]

It has been shown in the previous section that a PIN Diode acts as a current controlled resistor at RF frequencies, so it makes sense to use a PIN diode in RF attenuators. The TEE network proves to be difficult to bias with PIN Diodes, so a modified bridged TEE network is used in its place [1]. Typical configurations for bridged TEE model and standard PI model PIN Diode attenuators are shown in Figures 6 and 7. There is a complex biasing circuit involved with both of these configurations because both circuits are inherently unbalanced. To simplify this unbalanced nature of PIN Attenuators, Ray Waugh created the balanced-Pi Attenuator [2]. Because Waugh was anti-patent (his design was never patented) his attenuator quickly became the industry standard in broadband PIN Diode Attenuators [2].

This senior project uses the balanced Pi network as a basis for PIN attenuator design; a model is shown in Figure 8. The Waugh balanced PI network has multiple advantages over the standard Pi model. The anti-parallel series diodes self cancel even order distortion products. The use of two diodes in series also doubles the useful frequency of the attenuator because it effectively cuts the series diode capacitance in half. It also creates a symmetrical network with 2 IN/OUT ports instead of specified in and out ports. Finally, the balanced configuration doubles the

effective power dissipation of the device because each diode is dissipating half the power. The one disadvantage of the Waugh attenuator is its increase in insertion loss. The circuit used in this senior project had an insertion loss of ~2.5dBc (explained further in Testing).

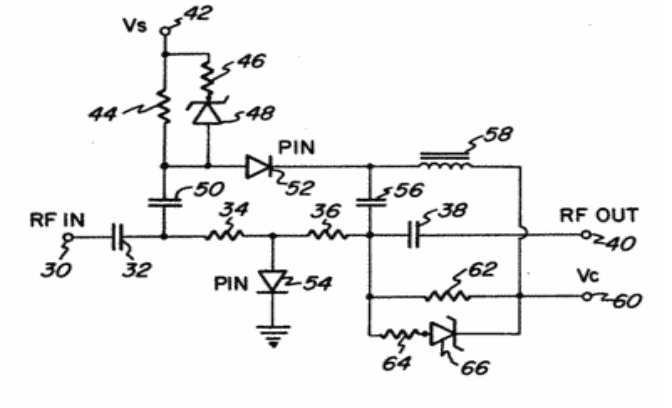

Figure 6 - Bridged TEE PIN Attenuator circuit. This particular circuit uses Zener diodes to clamp control and bias voltages to some maximum value.

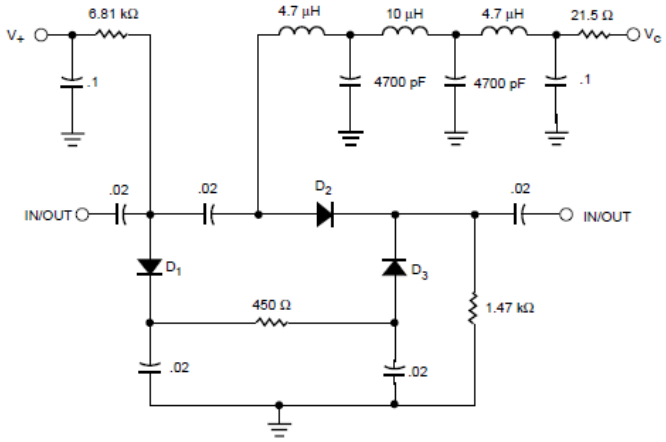

Figure 7 - The Standard Pi model PIN Attenuator. Heavy filtering is required to reduce noise on the control voltage.

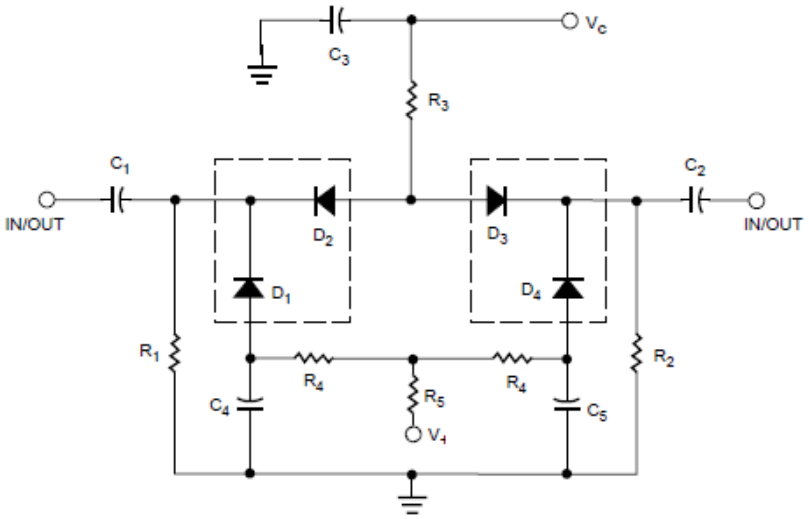

Figure 8 - Balanced Pi network PIN Diode attenuator. The biasing network is simplified and circuit operation can be more readily visualized in this configuration over the standard Pi model network.

III. Requirements and Specifications

A list of the specific device characteristics is listed in Table 1 below. It is worth noting that these specs represent a state of the art combination of power handling and bandwidth. There are devices on the market that have 8+ octave bandwidths but limited power handling capability (+17dBm)[].

Table 1 - Senior project device specifications

Device Specifications	
Minimum Frequency	30Mhz
Maximum Frequency	6GHz
Peak RF Power dissipation	+28dBm
Insertion Loss	<2dB
Maximum Attenuation	-30dBc
Attenuation Slope	<2dB
Return Loss	>15dB
IP3 intercept	>+50dBm

IV. Design

It has been shown that the balanced Pi model is the most desirable circuit configuration for a broadband high power variable attenuator. Component selection to provide the proper bandwidth and power handling is the main objective of the design phase. First diodes must be selected to operate over the proper frequency range. The lower cutoff frequency is determined by the effective recombination time and the high cutoff frequency is determined by the effective device capacitance (in truth, the high frequency limit is determined by the desired attenuation level at the high frequency end of the device spectrum). Avago Technologies HSMP-381x PIN Diode specification sheet is included in Appendix E. Using this information:

$$f_{low} = 10f_c = \frac{10}{\tau_{eff}} = \frac{10}{1500ns} = 6.67MHz \quad \text{Eq. 5}$$

$$R_{effhigh} = \frac{1}{wC_{eff}} = \frac{1}{6GHZ*.18pF} = 147.4\Omega \quad \text{Eq. 6}$$

$R_{effhigh}$ is the effective capacitive resistance at the 6GHz upper limit of the diode. In the high attenuation state the I-region resistance will be >>$R_{effhigh}$ so the total resistance is approximately equal to the capacitive resistance. Using this number it is possible to obtain 25dB of loss at 6GHz. This falls short of the required 30dB of attenuation range, but for time constraints this diode was selected for further testing. The bias circuitry was designed around Agilent HSMP – 3814 PIN Diode packages.

The selection of resistors is important in obtaining a correctly functioning and feasible attenuator. Resistors R_1 and R_2 are the bias resistors for the series diodes. The resistance of each of these resistors must be high enough to ensure good impedance match with the in/out ports, but not so high that the circuit requires a large control voltage. The resistor R_3 also provides biasing for series diodes and serves the additional purpose of limiting the amount of RF power transmitted through capacitor C_3. Again, R_3 cannot be set too high or a large control will be required. Resistors R_4 and R_5 are the bias resistors for the parallel diodes. The parallel

diodes carry less current on average than the series diodes so these resistors will typically be higher value resistors. In practice, resistors R_1 – R_5 are all chosen empirically and simulated for results. Figure 9 shows the final simulation circuit used in the design process.

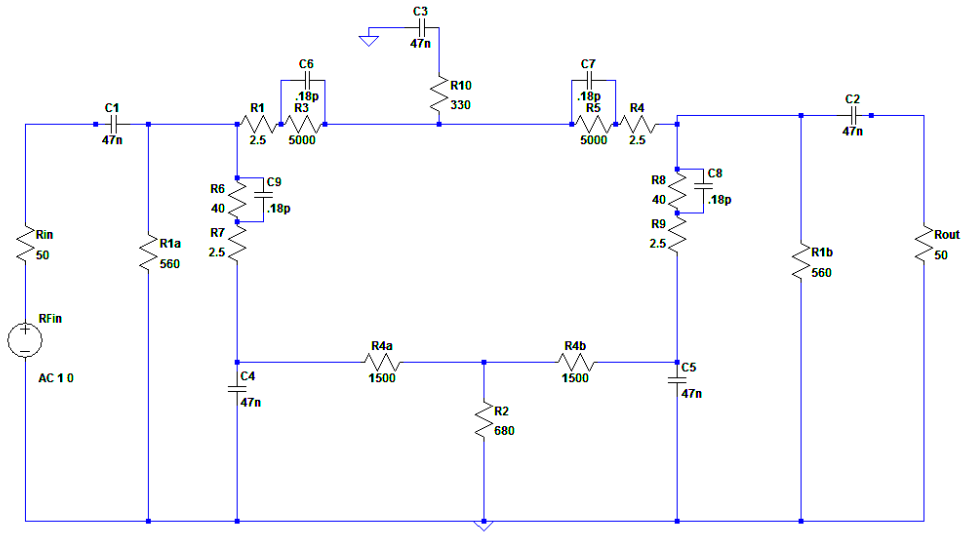

Figure 9 - Simulation circuit used to determine feasibility of HSMP-3814 diodes. The diode model is taken from the datasheet (Appendix E)

The diode resistances are dynamically changing with respect the series current and it is difficult to run one simulation that changes all 4 diode variable resistances correctly. It is for this reason that a small and simple java program was made to determine all 4 diode resistances for a given series current. The program takes the series current and, using the PIN Diode model in the datasheet, finds the series diode resistance and calculates the control voltage required to create that diode resistance. It then iteratively determines the parallel diode current and resistance from the voltage at the cathode of each diode (where resistors R_1 and R_6 meet as well as R_4 and R_8 in the above simulation SPICE program). The program output is shown in figure 10 and code is given in Appendix D.

```
----jGRASP exec: java ResistanceCalc

Enter desired series diode current (mA):
2
Series Resistance = 42.87
Control Voltage (V)= 1.87
Parallel Current (mA)= 1.56
Parallel Resistance = 53.73

----jGRASP: operation complete.
```

Figure 10 - Output for small java program used to determine diode resistances

It is important to note that this program is not overly precise, but rather gives estimates based on datasheet information. There is a small discrepancy between the voltage drop of the diode and the current through it. Still, it provides a solid basis for simulation and helps to determine feasibility. Using this program a forward current of 17mA can be generated in the series Diodes with a control voltage of ~15V. This program can also be used to show when the series and parallel diodes turn on or off. Figures 11 – 16 show program output for these states as well as simulated attenuation of the device in Figure 8.

```
----jGRASP exec: java ResistanceCalc

Enter desired series diode current (mA):
17
Series Resistance = 6.25
Control Voltage (V)= 15.28
Parallel Current (mA)= 0.00
Parallel Resistance = 10000.00

----jGRASP: operation complete.
```

Figure 11 - Calculated resistance at the maximum available current. These values will categorize the insertion loss of the attenuator.

```
----jGRASP exec: java ResistanceCalc

Enter desired series diode current (mA):
.5
Series Resistance = 149.29
Control Voltage (V)= 0.52
Parallel Current (mA)= 1.94
Parallel Resistance = 44.06

----jGRASP: operation complete.
```

Figure 12 - Resistance values at a predetermined minimum current. These values will be used to help categorize the attenuation maximum of the attenuator.

```
----jGRASP exec: java ResistanceCalc

Enter desired series diode current (mA):
.005
Series Resistance = 9419.26
Control Voltage (V)= 0.05
Parallel Current (mA)= 2.07
Parallel Resistance = 41.62

----jGRASP: operation complete.
```

```
----jGRASP exec: java ResistanceCalc

Enter desired series diode current (mA):
7.68
Series Resistance = 12.77
Control Voltage (V)= 6.95
Parallel Current (mA)= 0.00
Parallel Resistance = 10000.00

----jGRASP: operation complete.
```

Figure 14 - Current value and control voltage value to turn off the parallel diodes. It makes sense that the parallel diodes are off in lower attenuation states as all the RF power is transmitted through the series diodes to the output.

Figure 13 - Series current effectively turned off the series diodes. This value is lower than the predetermined minimum current state; the attenuator should avoid any unwanted characteristics of having the series diodes turned off.

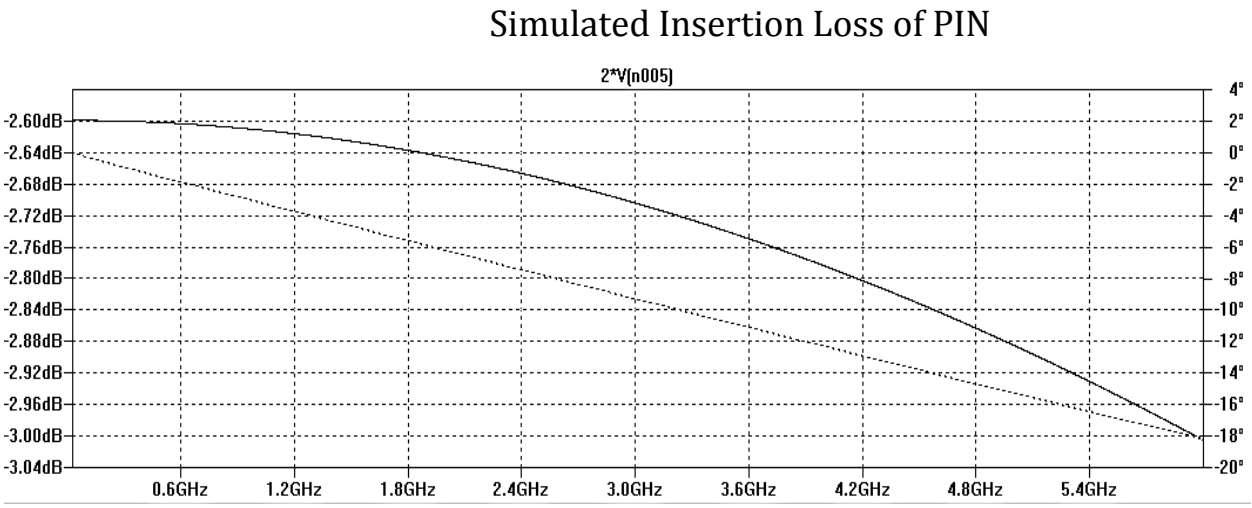

Figure 15 - Simulated results for the minimum attenuation setting. The solid line represents the attenuation and the dashed line represents the phase shift.

Attenuator

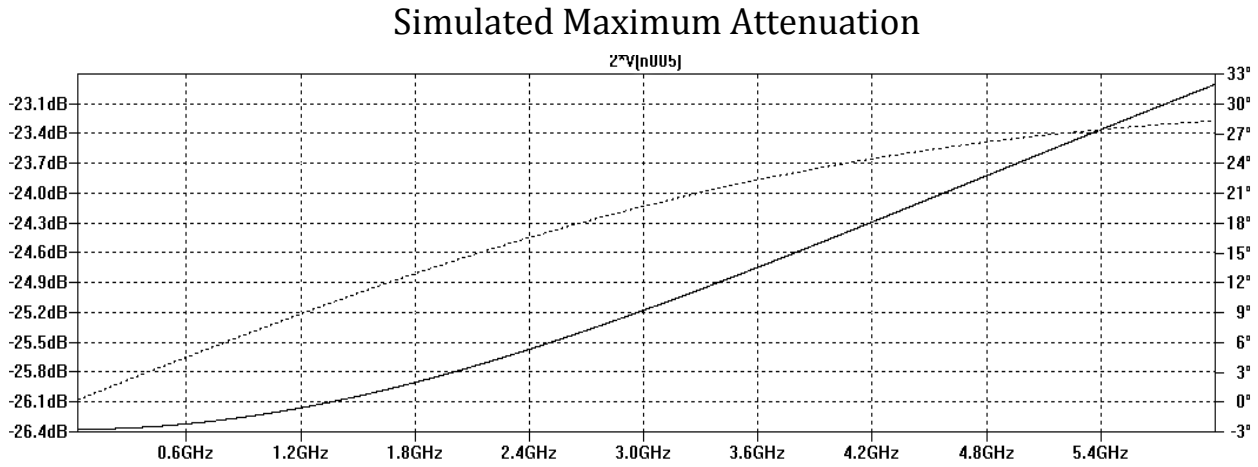

Figure 16 - Simulated results for the maximum attenuation setting. Solid line represents the attenuation curve and the dashed line shows the phase shift. The graph indicates, as expected, that the attenuator becomes increasingly capacitive at high frequencies. It also shows that the device will have undesirable attenuation slope across the frequency spectrum

The only design consideration that cannot be taken into account is the power handling capability of the device. The gain expansion will be used as a measure of the devices power handling capability (in Testing section).

V. Construction

The final product in this design uses .063" FR4 PCB material with .070" trace widths. The entire PIN attenuator is laid on 1.9in^2 section of the FR4 material. FR4 is not designed for high frequency devices and is not recommended to use for this device, but it is mechanically stable and very cost effective. HT-2 is a higher performance PCB material with a better controlled dielectric and can be used in circuits operating in the EHF band (~40GHz). The performance of the device will increase if placed on proper PCB substrate. The silkscreen and trace layouts are in Appendix C.

Attenuators are typically small subcircuits of larger systems. It is therefore desirable for the attenuator to be as small as possible while maintaining all of its properties. Surface mount components should be used whenever possible because of their reduced footprint size. Thin film resistors are used in this design, but thick film resistors may be used as well. The capacitor type is more important than the resistor type. A capacitor with a small footprint as well as a low ESR will help with circuit function. Ceramic capacitors can be used up to 10GHz or so with reasonably reliable operation. Ceramic capacitors were chosen for this design because of the cost benefits. Use only capacitors with NP0 temperature ratings. These capacitors are more reliable and stable than differently rated capacitors. All 2 pin components in this design are 0805SMT parts. These parts are large enough to be easily soldered; smaller parts may be used with increased performance. The smaller components offer better performance because they afford even smaller trace widths and lengths, leading to less signal leakage.

Complete parts list and cost information is available in Appendix A.

VI. Testing

The device was tested using an Anritsu 10MHz – 3GHz network analyzer. The analyzer provides a 0dBm signal and was used to measure S_{11} and S_{21} parameters of the PIN Diode Attenuator. The attenuation level was changed with a DC voltage supply. Figures 17 – 21 show the results of the PIN Diode Attenuator built. The device did not meet the requirements for attenuation slope. This is due to having large solder joints on the board. These large solder joints make the device inductive at low attenuation states (Fig. 17) and capacitive at high attenuation states (Fig. 19 and 20)

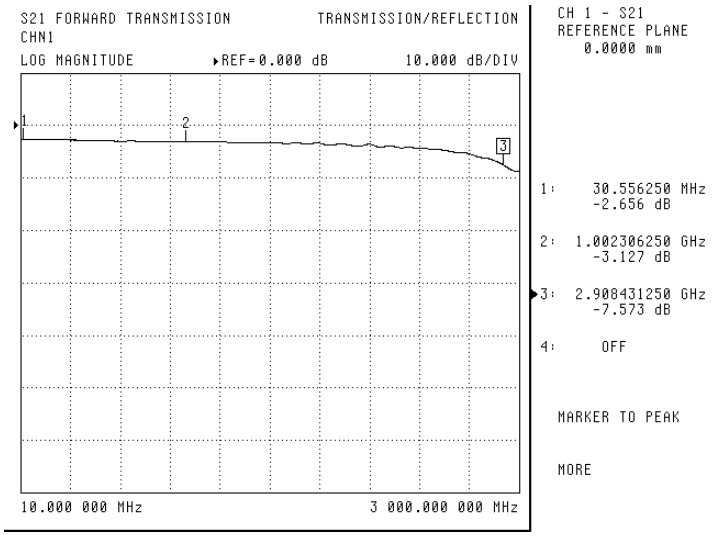

Figure 17 - Insertion loss of the PIN Diode attenuator. Control voltage = +15V

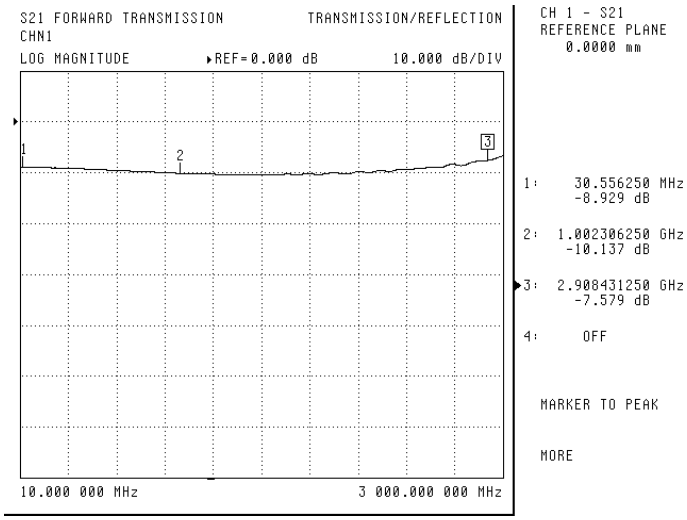

Figure 18 - Attenuation of 10dB. Control voltage set +5.8V

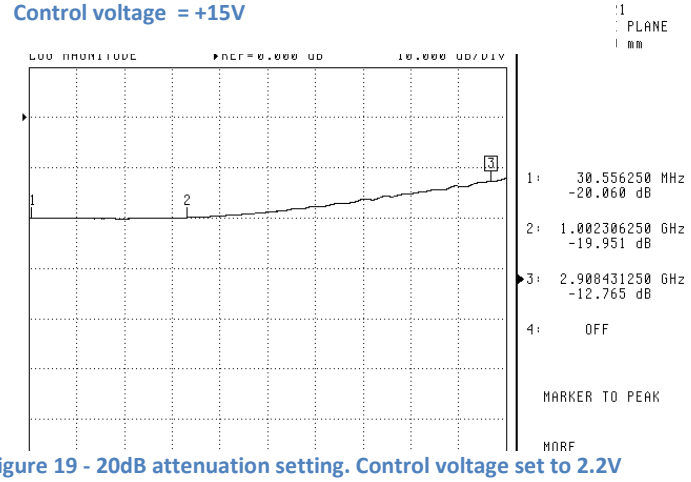

Figure 19 - 20dB attenuation setting. Control voltage set to 2.2V

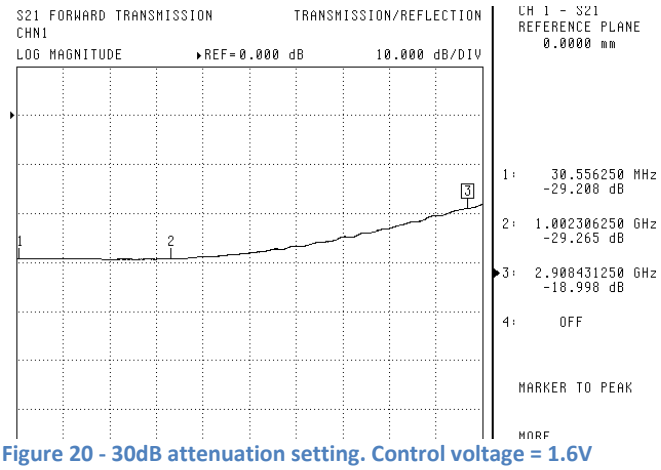

Figure 20 - 30dB attenuation setting. Control voltage = 1.6V

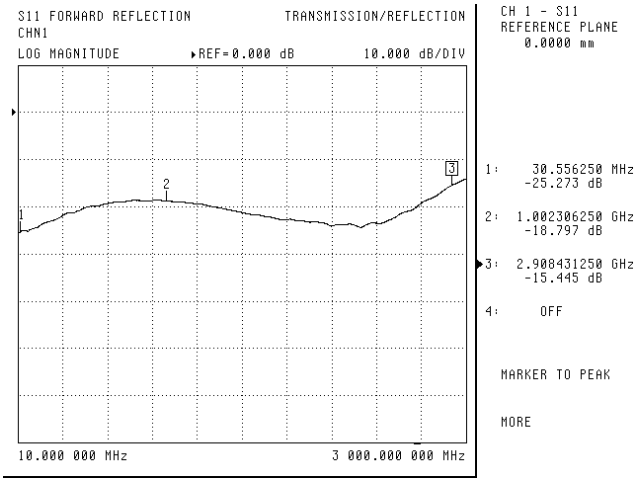

Figure 21 - Return losses in the worst case (series diodes turned off)

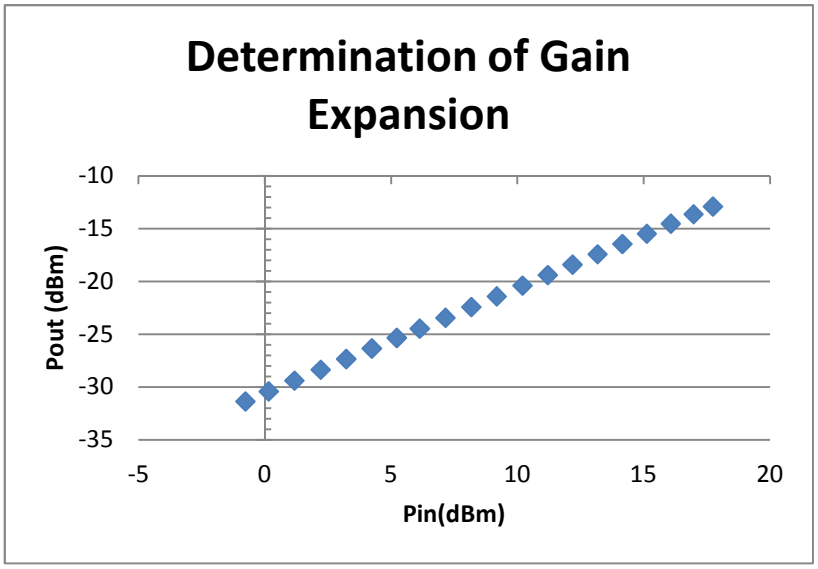

Figure 22 - Graph depicting the input and output power in an attempt to find the 1-dB gain expansion point. F = 100MHz

Three tests were done on the Attenuator. A transmission test (determining S_{21}) to sweep across the attenuation range. A reflection test (determining S_{11}) to find the minimum reflection losses. The final test was a power handling test. All RF devices have a finite power handling capability above which device performance begins to degrade and below which the device can be expected to behave linearly. There are two different ways to find the power handling capability of a given device; gain compression and gain expansion. The vast majority of devices are tested using a gain compression method; however, attenuators are tested using the gain expansion method. Gain expansion is the condition when the input signal reaches a power level that causes the device to have a boost in output gain. This logically makes sense for testing an attenuator, because the gain is negative. To perform this test the attenuator is set to its maximum attenuation state and the signal power is increased until the device can no longer provide its full attenuation setting. The broadband PIN Diode in this design requires a gain expansion point of +28dBm, which was unable to obtain with the equipment. However, figure 22 shows a linear relationship up to +18dBm (the maximum power level of the signal generator available) which is expected.

VII. Conclusions and Recommendations

A. Limitations of Device

This senior project represents a proof of concept for a high power broadband pin diode attenuator. In order to help productize it, several additions can be made to improve upon the design. The board components can be downsized from 0805SMT parts to 0402SMT parts, this will allow for thinner traces while maintaining product reliability. The smaller SMT parts also require less solder, which improves the bonding capacitance and inductance characteristics of the PIN Diode Attenuator. Also, the current design requires multiple voltage levels, not a desirable trait for industry. A DC/DC buck/boost converter can be used to take the control voltage and regulate it to 5V for the bias voltage. This would require extensive testing to ensure voltage ripple was kept to a minimum (multiple LPF's would be required). It would also be desirable to have a GUI interface with this device. A Flash or successive approximation DAC can be driven by a microprocessor to run the DC voltages of the board. The DAC will need to be able to source approximately 150mA to correctly drive the DC/DC converter and the control voltage of the board.

B. Test Equipment required for full characterization of attenuator.

The design of an 8 octave, 1Watt PIN Diode Attenuator represents state of the art technology. The combination of power and bandwidth is unrepresented in the industry. That being said, it requires specific test equipment to fully quantify and qualify its properties. The EE dept. does an excellent job of providing students with the necessary equipment, however better equipment would have allowed for better classification of this device.

Several test equipment items would allow student access to higher quality test devices. The need for a higher frequency VNA would enable testing of this particular PIN Attenuator to the full 6-GHz upper bandwidth limit. Agilent Technologies makes such a device, model number N5230C – a network analyzer in their PNA line of devices. This device has two built in sources and can supply +5dBm signal out to 10GHz and a 122dB dynamic range receiver. The 4-channel version is shown in Figure 1 below. A higher power signal generator is needed to test high

power RF devices. The current signal generator is calibrated up to +13dBm and will output a fairly reliable signal to +19dBm, however this is insufficient to test this PIN Diode attenuator. Similar models are available from a variety of companies. Anritsu makes a vector signal generator, model number MG3710A, which can sweep
from 100kHz – 2.7GHz or higher and output up to +30dBm up to 1GHz with noise suppression of -131dBc/Hz. Finally, and possibly the most important piece of equipment is a power splitter. Most RF devices carry multiple signals at once and an Inter Modulation Distortion (IMD) test is necessary to check the harmonic suppression of the device. Power splitters are an effective way of running multiple tones through a device. Mini-Circuits model number Z99SC-62+ is a cost effective device that operates in good frequency range (.5 – 600MHz) to test most every device used in RF classes at Cal Poly.

VIII. References

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5. "HSMP-381x." Avago Technologies, Web. 5 Jun 2012. <http://www.avagotech.com/docs/AV02-0402EN>.
6. "Types of Capacitors." *Electronics Tutorials*. N.p., June 2012. Web. 5 Jun 2012. <http://www.electronics-tutorials.ws/capacitor/cap_2.html>.
7. "Pi and Tee Attenuator Pad Calculator." Multi-Teknik, n.d. Web. 5 Jun 2012. <http://www.multek.se/engelska/engineering/signal-management-2/pi-and-tee-attenuator-pad-calculator-2>.
8. "PIN Diodes." . Microwaves 101, 04 Jan 2010. Web. 5 Jun 2012. <http://www.microwaves101.com/encyclopedia/diodes_PIN.cfm>
9. "PIN Diode Attenuator." . Stanton, 1 July 1990. Web. 5 Jun 2012. <http://www.patentgenius.com/patent/5140200.html>.
10.

Appendix A – Parts list and Costs

Table 2 - Parts Purchased for Senior Project

Part	Cost
PCB	$50.85
SMA Connectors, End Launch, .187"	$45.42
Capacitor, Ceramic, .047uF, 50V, NP0, 0805	$9.92
Capacitor, Tantalum, 47uF, 26V, EIA7343	$7.30
Kit, Chip resistors, Thin film, 61 Values, 0805	$79.95
Resistors, assorted, Thick Film, 1206	$1.23
PIN Diode, HSMP-3814	$6.70
Total	$201.37

Appendix B – Schedule and Time Estimates

Table 3 - Schedule and Time Allocation

Schedule Item	Date(s)	Estimated Time (Hours)
Project Kick Off	Oct 2011	xx
Backgound Information	Oct - Dec 2011	50
Circuit Design, Simulation	Dec 2011 - Mar 2012	50
PCB Design	Mar 2012	8
Construction	Apr 2012	10
Testing	Apr - May 2012	10
Documentation	May - June 2012	40

Appendix C – PC Board Layout and Component location

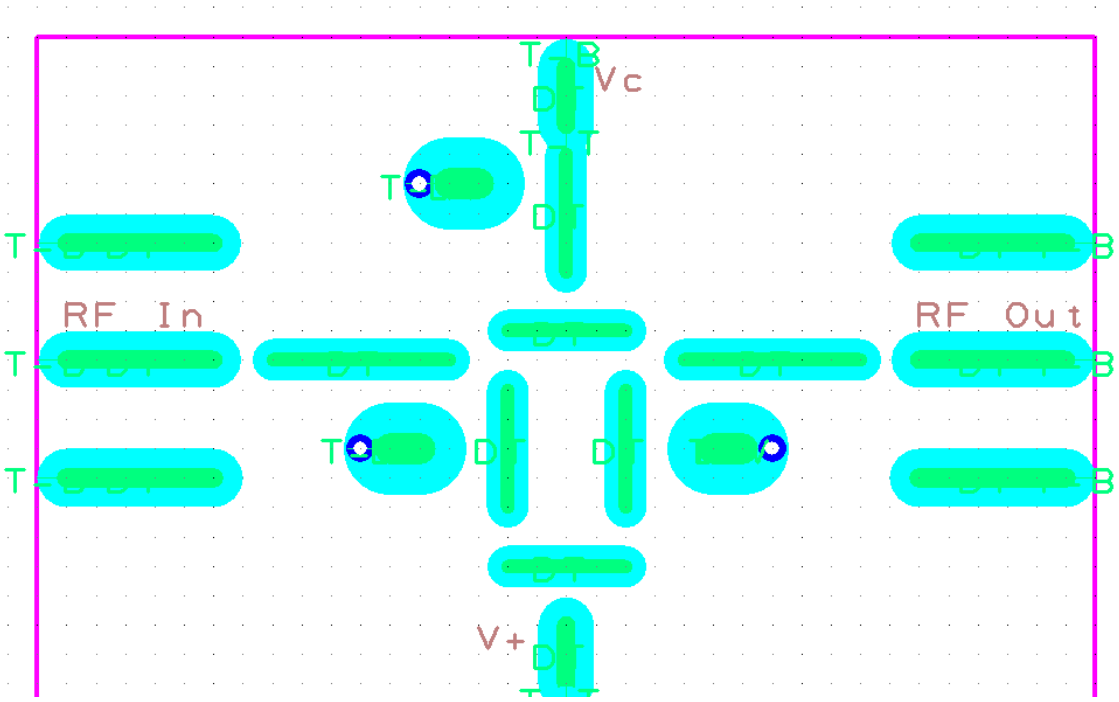


Figure 23 - Trace layout

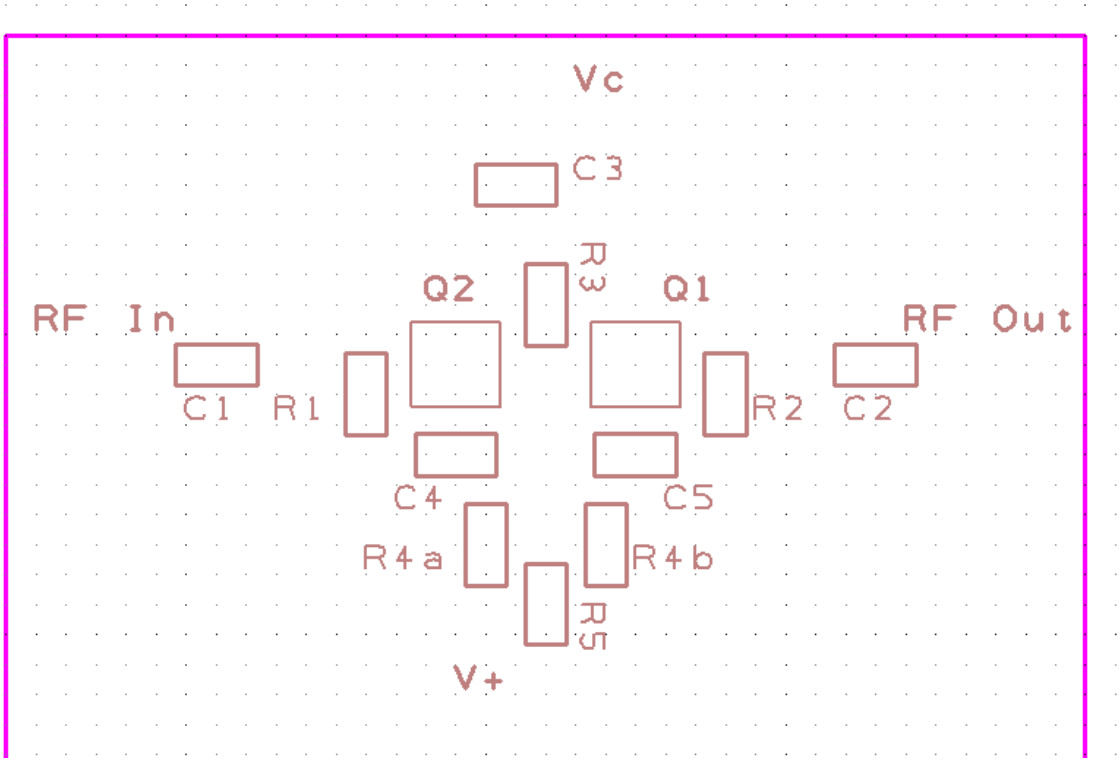


Figure 24 - Component Location

Appendix D – Software code

```
import java.util.Scanner;
import java.lang.*;


public class ResistanceCalc{
   public static void main(String[] args){
        System.out.println("Enter desired series diode current
(mA): ");
        System.out.flush();
        Scanner inputStream = new Scanner(System.in);
        findResValues(inputStream);

        return;
    }

    private static void findResValues(Scanner inputStream){

        double seriesCurrent = inputStream.nextDouble();
        double seriesResistance = 80/Math.pow(seriesCurrent,
.9);
        double Vcathode = .560*seriesCurrent;
        double Vcontrol =
(.560+.330+.0025+seriesResistance/1000)*seriesCurrent;
        double parallelCurrent = 0;
        double parallelResistance = 0;

        if(Vcathode > 4.3){
            parallelCurrent = 0.00;
            parallelResistance = 10000;
        }
       else{
            for(int i=0; i<10; i++){
                parallelCurrent = (5 - .4 -
Vcathode)/(.680+1.5+.0025+parallelResistance/1000);
                parallelResistance =
80/Math.pow(parallelCurrent, .9);
            }
```

```
            if(parallelCurrent < 0.009){
               parallelResistance = 10000;
            }
        }

        System.out.format("Series Resistance = %.2f\n" +
"Control Voltage (V)= %.2f\n" + "Parallel Current (mA)= %.2f\n"
+ "Parallel Resistance = %.2f\n", seriesResistance,Vcontrol,
parallelCurrent, parallelResistance);

        return;
    }
}
```

Appendix E – PIN Diode Specifications

HSMP-381x, 481x

Surface Mount RF PIN
Low Distortion Attenuator Diodes

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully
compliant

Description/Applications

The HSMP-381x series is specifically designed for low distortion attenuator applications. The HSMP-481x products feature ultra low parasitic inductance in the SOT-23 and SOT-323 packages. They are specifically designed for use at frequencies which are much higher than the upper limit for conventional diodes.

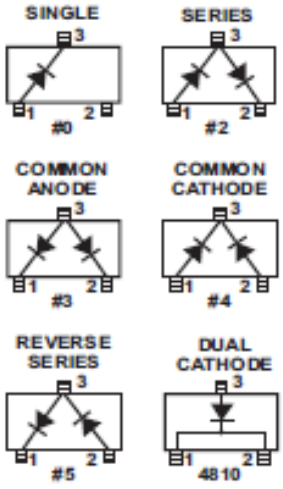
A SPICE model is not available for PIN diodes as SPICE does not provide for a key PIN diode characteristic, carrier lifetime.

Features

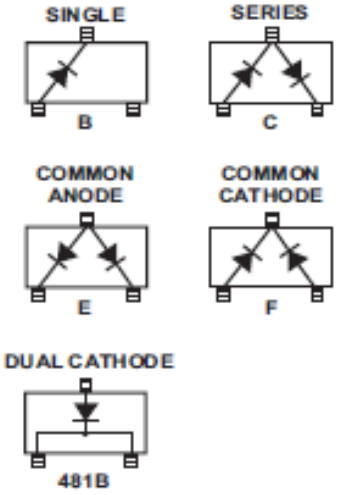
- Diodes Optimized for:
  - Low Distortion Attenuating
  - Microwave Frequency Operation
- Surface Mount Packages
  - Single and Dual Versions
  - Tape and Reel Options Available
- Low Failure in Time (FIT) Rate[1]
- Lead free

Note:
1. For more information see the Surface Mount PIN Reliability Data Sheet.

Package Lead Code Identification, SOT-23 (Top View)



Package Lead Code Identification, SOT-323 (Top View)



Absolute Maximum Ratings[1] $T_C = +25°C$

Symbol	Parameter	Unit	SOT-23	SOT-323
I_F	Forward Current (1 µs Pulse)	Amp	1	1
P_{IV}	Peak Inverse Voltage	V	Same as V_{BR}	Same as V_{BR}
T_J	Junction Temperature	°C	150	150
T_{stg}	Storage Temperature	°C	-65 to 150	-65 to 150
θ_{jc}	Thermal Resistance[2]	°C/W	500	150

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. $T_C = +25°C$, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.

Electrical Specifications $T_C = +25°C$ (Each Diode)

Conventional Diodes

Part Number HSMP-	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Total Capacitance C_T (pF)	Minimum Resistance at $I_F = 0.01mA$, RH (Ω)	Maximum Resistance at $I_F = 20mA$, R_L (Ω)	Maximum Resistance at $I_F = 100mA$, RT (Ω)	Resistance at $I_F = 1mA$, R_M (Ω)
3810	E0	0	Single	100	0.35	1500	10	3.0	48 to 70
3812	E2	2	Series						
3813	E3	3	Common Anode						
3814	E4	4	Common Cathode						
3815	E5	5	Reverse Series						
381B	E0	B	Single						
381C	E2	C	Series						
381E	E3	E	Common Anode						
381F	E4	F	Common Cathode						
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10uA$	$V_R = 50V$ f = 1MHz	$I_F = 0.01mA$ f = 100MHz	$I_F = 20mA$ f = 100MHz	$I_F = 100mA$ f = 100MHz	$I_F = 1mA$ f = 100MHz

High Frequency (Low Inductance, 500 MHz – 3 GHz) PIN Diodes

Part Number HSMP-	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Series Resistance R_S (Ω)	Series Resistance $I_F = 1mA$, R_M (Ω)	Typical Total Capacitance C_T (pF)	Maximum Total Capacitance C_T (pF)	Typical Total Inductance L_T (nH)
4810	EB	B	Dual Cathode	100	3	48 - 70	0.35	0.4	1
481B	EB	B	Dual Cathode						
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10\mu A$	$I_F = 100mA$ f = 100MHz	$I_F = 1mA$ f = 100MHz	$V_R = 50V$ f = 1MHz	$V_R = 50V$ f = 1MHz	f = 500MHz - 3GHz

Typical Parameters at $T_C = 25°C$

Part Number	Series Resistance	Carrier Lifetime	Reverse Recovery Time	Total Capacitance
HSMP-	R_S (Ω)	τ (ns)	T_{rr} (ns)	C_T (pF)
381x	53	1500	300	0.27 @ 50 V
Test Conditions	I_F = 1 mA f = 100 MHz	I_F = 50 mA I_R = 250 mA	V_R = 10 V I_F = 20 mA 90% Recovery	f = 1 MHz

Typical Parameters at $T_C = 25°C$ (unless otherwise noted), Single Diode

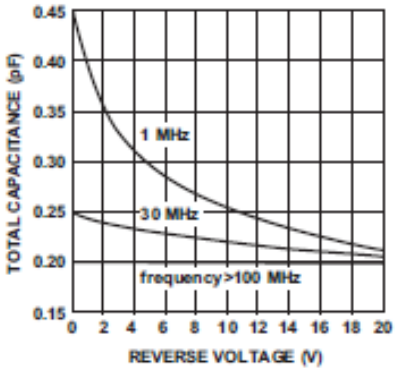


Figure 1. RF Capacitance vs. Reverse Bias.

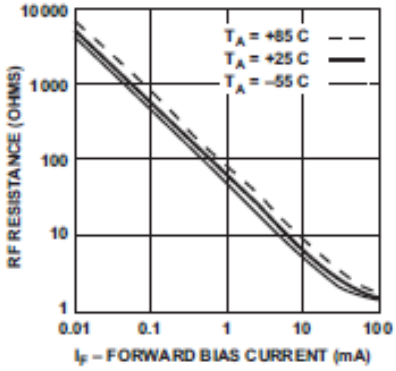


Figure 2. RF Resistance vs. Forward Bias Current, f = 100MHz

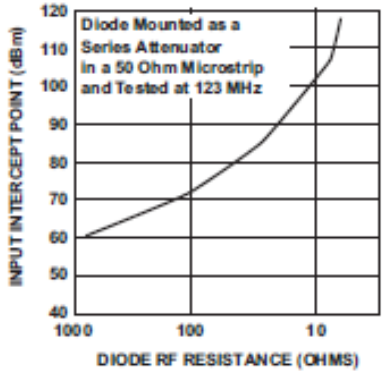


Figure 3. 2nd Harmonic Input Intercept Point vs. Diode RF Resistance.

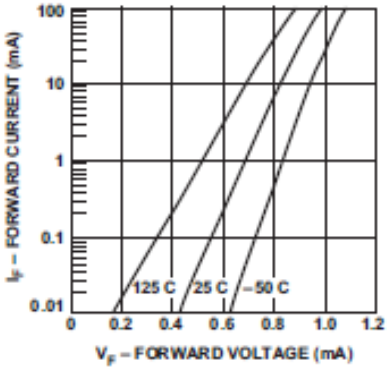


Figure 4. Forward Current vs. Forward Voltage.

Typical Applications for Multiple Diode Products

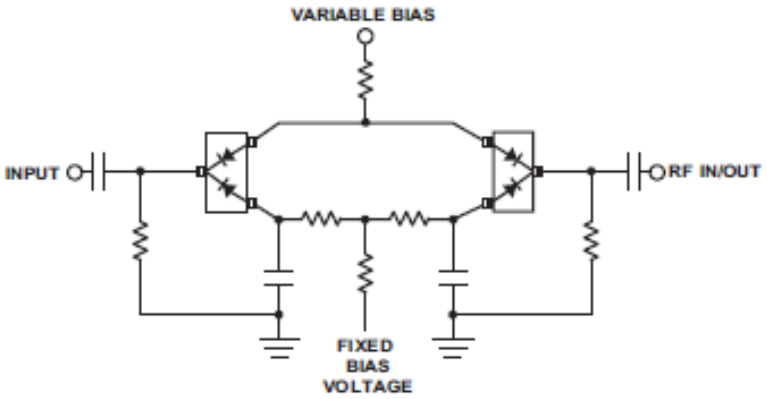


Figure 5. Four Diode π Attenuator. See Application Note 1048 for Details.

Notes:
3. Typical values were derived using limited samples during initial product characterization and may not be representative of the overall distribution.

Typical Applications for HSMP-481x Low Inductance Series (continued)

Co-Planar Waveguide Shunt Connection for HSMP-481x Series

Co-Planar waveguide, with ground on the top side of the printed circuit board, is shown in Figure 10. Since it eliminates the need for via holes to ground, it offers lower shunt parasitic inductance and higher maximum attenuation when compared to microstrip circuit.

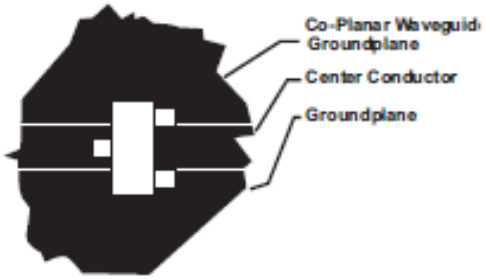


Figure 10. Circuit Layout.

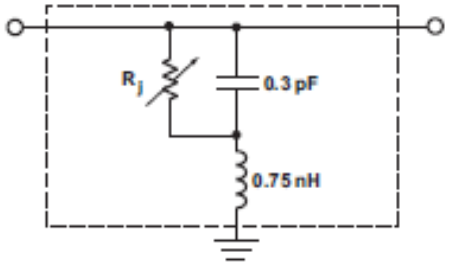
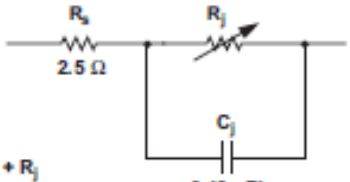


Figure 11. Equivalent Circuit.

Equivalent Circuit Model HSMP-381x Chip*



$R_T = 2.5 + R_j$

$C_T = C_P + C_j$

$R_j = \frac{80}{I^{0.9}}\ \Omega$

I = Forward Bias Current in mA

*See AN1124 for package models.