

A CMOS AGC-less IF Strip for Bluetooth

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Abstract

This paper presents an IF chain suitable for Low-IF fully-integrated GFSK receivers. The circuit performs amplification and channel selection (including image rejection). A five-pole Gm-C polyphase filter forms the core of the IF strip. The filter is current driven and has transimpedance gain of $\simeq 120 \text{ k}\Omega$. The filter is architected so that GFSK signals with dynamic range exceeding 50dB can be decoded without the need of any automatic gain control. This AGC-less IF strip was fabricated in standard $0.25 \mu\text{m}$ CMOS process. It draws 6.2 mA from a 2.5 V supply and has better than 4.8 nA rms input referred noise. Input signals (compliant with Bluetooth) were applied and the output signal was collected for "software decoding". Generated BER plots meet Bluetooth specifications.

1. Receiver Topology

In this paper we will discuss the implementation of an IF chain for a fully integrated Bluetooth receiver. There are three receiver architectures that are amenable to full integration: direct conversion, single low-IF down-conversion and poly-phase filtering, and wideband-IF double down-conversion (Weaver architecture). The Bluetooth signal is approximately 1MHz wide with most of its energy concentrated in the middle of the band. Thus, direct conversion receiver would be difficult to implement, especially in CMOS because of $1/f$ noise. The Bluetooth standard has a relaxed image requirement; therefore, a low-IF architecture seems to be the best choice [1]. The selection of the IF is a trade-off between the $1/f$ noise and the filter quality factor. We have selected an IF of 2MHz. It gives good "immunity" to $1/f$ noise and dc offsets, while the required Q factors are still practical (< 20). To perform channel selection a 5-pole active poly-phase filter was deemed necessary and an image rejection better than 30dB was sought; this number is easily achievable without resorting to complicated I/Q-mismatch correcting schemes. Since the amplitude of the signal carries no information (GFSK modulation), no harm is done if the filter I/Q outputs are limited. The final data detection is done in a differential FM detector. For successful decoding of a Bluetooth signal, our decoder circuit [2] calls for an SNR of about 15 dB, and SDR of 11 dB or better.

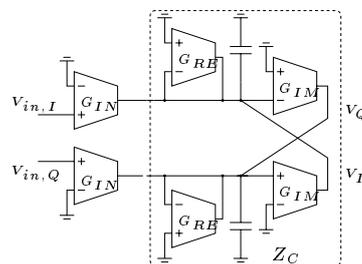


Figure 1. One pole of the complex filter.

2. Topology of the IF Strip

The core of the IF strip is a 5-th order Butterworth polyphase filter. In this section we will decide upon the architecture of this filter, its gain distribution, as well as the interface between the filter and the I/Q mixers.

2.1. Architecture

The most power-efficient way of reducing the filter's input referred noise is to implement it as a chain of alternating filter/gain sections. When properly done, the input referred noise contribution of successive filter sections will be reduced. Each section implements a single "complex pole". We decided upon a "plain" Gm-C implementation with *no internal nodes*, because of the high quality factors of the poles ($Q_{max} \simeq 20$). Due to the high Q 's the parasitic poles of the integrators should be located above 400 MHz.

The topology of a complex pole section is shown in Fig 1. Transconductor G_{in} performs V-I conversion, while the rest of the circuit forms a "complex impedance", Z_C . The transconductance of G_{in} can be adjusted to achieve the desired gain. The overall filter is a cascade of 5 stages like the one in Fig. 1, and it can be regarded as a "complex transimpedance" driven by a G_m element.

The input transconductor and the load of the mixer form a current amplifier. The sole purpose of this amplifier is to "align" the compression point of the filter transimpedance with that of the mixer. We disposed of this current amplifier by co-designing the mixer and the filter, and injected the output current of the Gilbert-type mixer directly into the filter transimpedance stage. Portion of the blocker-induced current is shunted to ground through the filter capacitors of the first node. Thus, the blocker

is filtered somewhat before it gets a chance to develop a voltage and produce distortion. This gives a 10 dB improvement in the DR at no extra cost (a similar principle is presented in [3]). In order to avoid loading of the filter, it might be necessary to inject the input current via a folded cascode.

2.2. Stage Ordering and Gain Distribution

Since sections implementing higher Q 's are noisier, we placed the filter sections in ascending order with respect to their Q 's. Transconductance values relative to one another are determined as follows. Those setting the real part of the first three complex poles, G_{RE} in Fig. 1, were assumed unity, while the G_{RE} 's of the last two, high Q , poles were taken $1/4$ to conserve power. The transconductors that determine the imaginary part of the poles, G_{IM} in Fig. 1, were calculated from the corresponding G_{RE} 's and the desired Q 's. The transconductors that determine the gains, G_{in} 's, are set so that the worst case blocker develops the same voltage swings across the first three nodes of the filter. No gain was applied in the last two stages to conserve power. When propagating through the filter chain the in-band, desired, signal will be amplified. With this gain distribution, strong in-channel signals will cause compression in the filter. If we are to keep the chain linear we would have to apply some type of AGC-ing. As discussed in the preceding section the signals coming out of the poly-phase filter are intentionally limited before decoding. Naturally, one wonders whether or not it is possible to limit earlier, inside the filter, and still extract decodable signal. This question will be answered in the next subsection.

2.3. Soft-Limiting in Presence of a Blocker

Consider a soft limiter, a circuit that is linear up to an input signal of S_{max} and saturates for larger signals. A blocker with magnitude S_{max} is applied to its input. For this signal alone the circuit is perfectly linear. Now, if a desired signal having large dynamic range is added to the input, the soft limiter becomes highly non-linear. Intermodulation tones are produced. Some of these spurious responses would fall on top of the desired signal and even if filtering is applied they can not be removed. If the strength of this interference, however, is sufficiently small compared to that of the desired signal, decoding could still be possible. Analysis and simulation show that the minimum signal-to-interference ratio is about 16 dB with the *only* requirement that the blocker alone does not overload the soft limiter. This minimum signal-to-interference value is observed when the magnitude of the desired signal is approximately $2S_{max}$. The signal-to-interference ratio improves fast around this minimum. Due to space limitations the detailed analysis will not be presented here.

Limiting of the output current of the gain transconductors, G_{in} in Fig. 1, would make these circuits behave as soft limiters. Assume that the maximum current, when G_{in} clips, does not overload the impedance it drives, Z_C

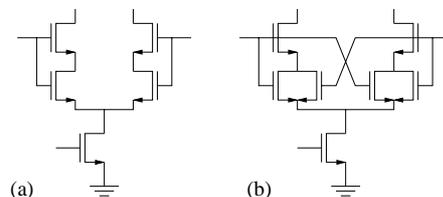


Figure 2. (a) A differential pair transconductor, (b) Modified differential pair with improved DR .

in Fig. 1. Then, the voltages that will develop, V_I and V_Q , will have a signal-to-interference of at least 16 dB. At the same time the filtering operation that this stage performs remains unaltered. It can be shown that the minimum signal-to-interference ratio at the output of the overall filter will be about the same, 16 dB, which is good enough at least for decoding of a Bluetooth signal. This was verified with matlab simulations.

Because we were not able to find a sufficiently robust circuit technique to implement the desired current limiting, we opted for voltage limiting. In parallel to Z_C in Fig. 1 we placed a non-linear conductance, such as back-to-back diodes or a MOSFET, biased so that it would conduct heavily whenever the voltage swing exceeds certain level. This level is chosen slightly lower than the linear range of the transconductors used.

Using voltage clipping instead of current clipping, gives rise to an undesired effect. For certain input levels, the nonlinear operation of the circuit causes distortion similar to intersymbol interference, which is particularly pronounced for fast (0,1,0,1,...) data sequences. This distortion causes the Bit Error Rate to increase. However, by using FM demodulation with post-correction [2], the circuit still meets the required specifications, see Sec. 4.

3. Circuit Implementation

In this section we will discuss the transconductor used and the common-mode feedback approach.

3.1. The Transconductor

Since in this design we are dealing with the implementation of high Q poles, a transconductor with virtually no parasitic poles is needed. The simplest such transconductor is the MOS differential pair. Linearization is helpful *only* if it results in larger dynamic range (with respect to simple diff. pair) with the same power dissipation and no frequency degradation. There are very few such transconductors and one of them is shown in Fig. 2(b). This circuit is derived from the stacked-transistor diff. pair shown in Fig.2(a) by splitting the bottom transistor in two and cross-connecting the gates, in a way similar to [4]. The regular diff. pair and the new circuit have exactly the same power consumption and output current noise. The cross-connection trades transconductance for larger input linear range. The DR of the new circuit is improved because

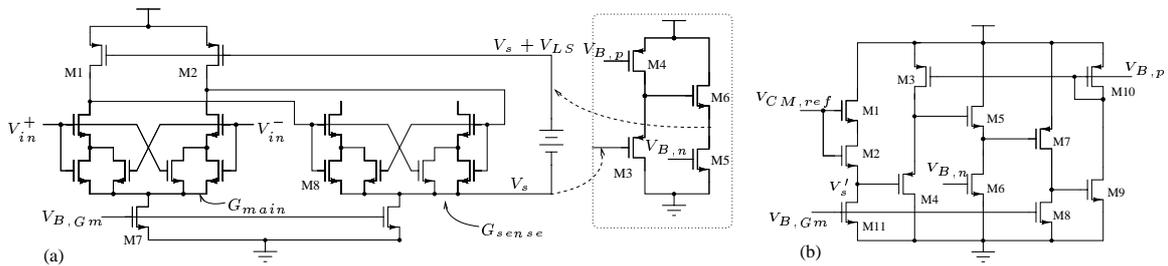


Figure 3. (a) The common mode feedback circuit, (b) The biasing arrangement for the common mode feedback.

the percent increase in input linear range is larger than the percent decrease in transconductance value.

3.2. The CMFB Circuit

The common-mode feedback circuit we used is shown in Fig. 3(a). The common-mode voltage at the output of transconductor G_{main} is sensed at the common-source node, S, of an identical transconductor G_{sense} . It can be shown that the voltage at node S follows the common-mode component of the voltage at the input of G_{sense} , while it is unaffected by the differential component. Instead of using an extra transconductor for common-mode sensing, we used transconductors which are already connected to the nodes whose common-mode voltage we try to sense. This approach to common-mode voltage sensing has been quite popular recently, see for example [5].

The voltage at the common-source node, V_s , is subsequently fed-back at the gates of M1 and M2 in Fig. 3(a) through a level shifter V_{LS} . The reader can verify that this configuration indeed establishes a negative feedback for the common-mode voltage. The common-mode feedback loop depicted in Fig. 3(a) has a dominant pole located at the drains of M1 and M2, which is the only high impedance point in the loop and, moreover, the integrating capacitors are connected there; no frequency compensation is therefore needed.

Fig. 3(b) shows a scheme that adjusts V_{LS} so that the output common-mode voltage equals certain reference value, $V_{CM,ref}$, over process and temperature variations. This scheme is conceptually similar to the common-mode feedback used in [6]. The desired common-mode voltage $V_{CM,ref}$ is applied at the input of a common-mode sensing circuit, identical to the one used in Fig. 3(a). The voltage developed at node S' is level shifted by V_{LS} and is then applied to the gate of transistor M7. This transistor is matched to the active load of the transconductor. The current that develops should be identical to the bias current of the transconductor. The corresponding error is amplified by M9 and fed back to the gate of M3 to adjust V_{LS} , so that the two current are equal. The bias voltage $V_{B,p}$ is used to bias *all* common-mode feedback circuits in the filter.

The p-MOS accumulation capacitors we used have an accuracy of $\pm 5\%$ over process and temperature. The filter transconductors were referenced to an external resistor. The achieved accuracy (simulated 3σ variation) was

$\pm 2\%$. The resulting absolute frequency accuracy of the filter transfer function was sufficient for our application.

4. Measurement Results

This section presents the measured results for the IF chain. The test setup is composed of an off-chip downconversion mixer which produces the desired I and Q inputs for the filter, and appropriate amplification stages. Frequencies above the LO frequency of the mixer are perceived as positive, and below it as negative. Since the filter should be driven by a current, on-chip buffers were included to convert the output voltage of the mixer to an input current. Fig. 4 shows the measured frequency response of the filter which closely matches the desired Butterworth response.

The measured image rejection is about 45 dB. This number includes contribution from the mixer, which can either improve or deteriorate the image rejection, depending on whether the mismatches of the mixer and the filter tend to cancel or reinforce each other. The number given above was a worst case measurement, and it is consistent with the expected image rejection from a circuit with a good layout at this frequency.

Because of the fairly unconventional architecture employed in the filter, it was decided to perform BER tests instead of spurious analyses in the spectral domain. A GFSK modulated signal was applied to the filter together with the appropriate interferers as described in the Bluetooth specifications. The output of the filter was sampled and decoded off-line to estimate the achieved BER. The technique presented in [2] was used to improve the BER of the detected signal. Fig. 6 shows the BER measurements corresponding to the Bluetooth tests. For each data point 41 kbits of data were processed. The input signal is swept across the required dynamic range while the blockers were set to the levels shown on the side of the plots. For each test the upper/lower curve corresponds to BER before/after the post-detection algorithm is applied.

The filter satisfies all tests dictated by the Bluetooth standard. Due to space limitations we didn't show the intermodulation test which is easily passed by virtue of the current-input filtering, the co-channel interference test, and the +3 MHz blocker test, which are also satisfied. The input referred noise current of the filter integrated over the passband is 4.8 nA rms.

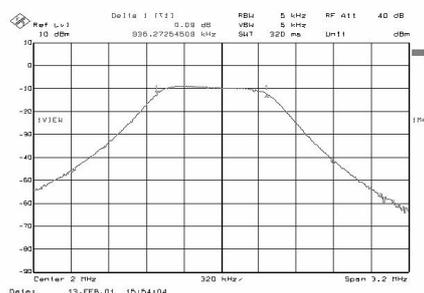


Figure 4. The frequency response of the filter.

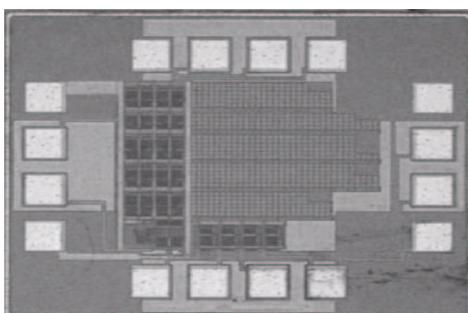


Figure 5. Microphotograph of the fabricated chip.

Fig. 5 shows a microphotograph of the fabricated chip. The chip occupies about 0.3 mm^2 .

5. Conclusion

A standard CMOS, 6.2 mA, IF strip for a fully integrated GFSK receiver has been presented. The proposed architecture operates in a nonlinear fashion by taking advantage of the angular modulation of the input. Although the circuit uses no Automatic Gain Control the resulting performance is compliant with the Bluetooth standard specifications.

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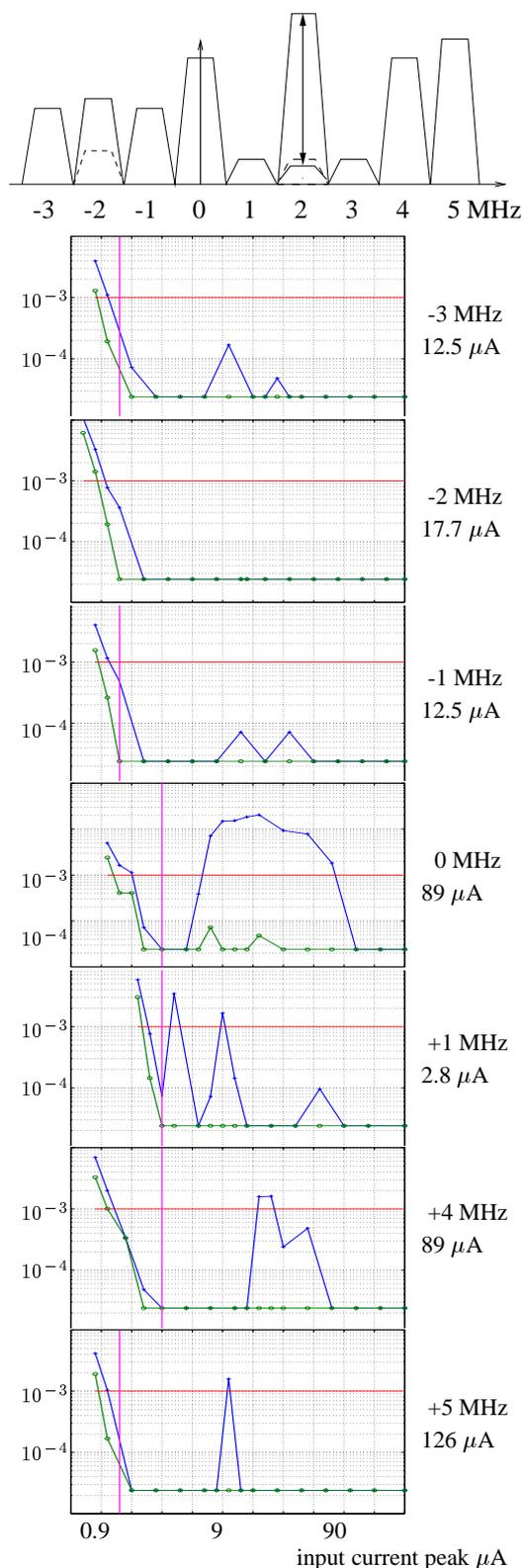


Figure 6. Bit Error Rate measurements for the complex filter. The numbers to the right of the plots give the level and the frequency of the blocker for each test. The two curves in each plot correspond to the measured BER before and after post-correction. The horizontal lines at 10^{-3} give the maximum allowed BER for Bluetooth, 0.1%.