An up to 3x breakdown voltage tristate capable integrated circuit CMOS buffer includes a level shifter circuit and a driver circuit. The driver stage includes a series connected n-channel and p-channel cascode stacks, each including at least three transistors. Dynamic gate biasing is provided for the third n-channel and p-channel cascode transistors to prevent voltage overstress of the cascode transistors. The level shifter circuit includes at least one pseudo N-MOS inverter including an input transistor, a protective cascode stack including at least one n-channel cascode transistor, and a load transistor. The level shifter provides at least one voltage shifted input signal to the driver.
FIG. 1B

Prior Art

1/2V_High

20

Dynamic Bulk Bias

Dynamic Gate Bias

P1

n2

n1

IN

OEN

GND
FIG. 2A

FIG. 2B

ACTIVE MODE

FIG. 2C

TRISTATE MODE
**FIG. 3A**

100

3V\(_{\text{max}}\) (V\(_{\text{HIGH}}\))

2V\(_{\text{max}}\)

S\(_2\)

S\(_1\)

V\(_{\text{max}}\)

V\(_n\)

(V\(_{\text{GROUND}}\))

**FIG. 3B**

100

3V\(_{\text{max}}\) (V\(_{\text{HIGH}}\))

2V\(_{\text{max}}\)

S\(_2\)

S\(_1\)

V\(_{\text{max}}\)

V\(_n\)

(V\(_{\text{GROUND}}\))
FIG. 3F

3V_{\text{max}} (V_{\text{HIGH}})

P_1

P_2

2V_{\text{max}}

N_4

P_6

108

P_5

P_3

P_7

V_{\text{pad}}

V_{\text{max}}

N_1

N_2

N_3

N_5

N_6

N_7

104

104

106

102

V_{\text{GROUND}}
FIG. 4

200

2V_{\text{max}} (V_{\text{HIGH}})

2V_{\text{max}} V_{\text{max}}

P_1

P_2

206

G_n

V_{\text{pad}}

2V_{\text{max}}

0

2V_{\text{max}}

\text{PAD}

V_{\text{GROUND}}

FIG. 5A

300

3V_{\text{max}} (V_{\text{HIGH}})

D

N_{11}

G

P_{11}

V_p

D

N_{10}

S

V_{\text{GROUND}}

V_{\text{max}}

G

N_{9}

S

IN

D

N_{8}

S

V_{\text{GROUND}}
FIG. 5B
FIG. 7

500

2V_{max}

\begin{align*}
\text{N}_4 & \quad \text{N}_5 \\
\text{P}_5 & \quad \text{P}_6 \\
\text{P}_7 & \quad \text{P}_8 \\
\text{N}_3 & \quad \text{N}_2 \\
\text{N}_1 & \quad \text{V}_{\text{ground}} \\
\text{V}_{\text{max}} & \quad \text{V}_{\text{max}} \\
\text{0 TO V}_{\text{max}} & \quad \text{0 TO 2V}_{\text{max}} \\
\end{align*}

502

102

IN

3V_{\text{max}}

\begin{align*}
\text{P}_1 & \\
\text{P}_2 & \\
\text{P}_3 & \\
\text{P}_4 & \\
\text{P}_5 & \\
\text{P}_6 & \\
\text{P}_7 & \\
\text{P}_8 & \\
\end{align*}

508

\begin{align*}
\text{OUT} & \\
\text{V}_{\text{max}} & \\
\text{V}_{\text{max}} & \\
\text{0 TO 3V}_{\text{max}} & \\
\text{0 TO 3V}_{\text{max}} & \\
\end{align*}

\begin{align*}
\text{d} & \quad \text{g} \\
\text{d} & \quad \text{g} \\
\text{d} & \quad \text{g} \\
\text{d} & \quad \text{g} \\
\text{d} & \quad \text{g} \\
\text{d} & \quad \text{g} \\
\text{d} & \quad \text{g} \\
\end{align*}
BUFFER INTERFACE ARCHITECTURE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from U.S. provisional application serial No. 60/287,674, filed May 1, 2001 and entitled “Buffer Interface Architecture.”

FIELD OF THE INVENTION

[0002] The present invention relates to integrated circuits, generally, and more specifically to a buffer for interfacing a low-voltage technology with a relatively high-voltage technology.

DESCRIPTION OF THE RELATED ART

[0003] Advances in the semiconductor arts have driven devices to decreasing sizes operating at increasing speeds. This continuous effort to maximize the performance of integrated circuits (“ICs”) has produced several additional benefits, including decreased operating voltages and reductions in power consumption.

[0004] As MOS technology scales below 0.2 μm, acceptable supply voltages have lowered below the previous 3.3V and 5V standards. As lower and lower operating voltage IC technology is developed and commercialized, however, a distinct problem has arisen. Mostly because of economic reasons, electronic systems often use ICs that span several technology generations, each generation having different supply voltage requirements. The ability to interface newer low power ICs with their predecessors where each IC has a different range of operating voltages is of concern, particularly as it relates to metal oxide semiconductors (“MOS”). Interfacing an older higher operating voltage IC with a lower operating voltage technology may cause reliability issues and/or temporary or even permanent damage. For example, the buffer circuits of a 1.5V IC can neither provide nor sustain (when in a high impedance state) a 3.3V drive.

[0005] To overcome this interface problem, several solutions have been proposed. One approach entails the development of MOS devices capable of handling both low and high voltages on the same semiconductor substrate. While this “dual supply” approach is simple in circuit implementation, presently, it is substantially more expensive than the traditionally known MOS technology because of the additional processing steps required to fabricate the high-voltage devices. Currently, many 0.2 μm technologies utilize this “dual supply” approach.

[0006] Alternatively, several buffer interface architectures are also known in the art for providing high voltage drive capability using low voltage MOS technology. Using this methodology, the incremental costs associated with the additional circuitry required to realize an interface having high voltage drive capability while implemented in low voltage MOS technology are negligible.

[0007] Prior approaches to high-voltage drive buffers with low-voltage transistors (HV/BLVT) can be classified into two basic groups. FIG. 1A illustrates a circuit with both high-voltage tolerance and high-voltage drive. Such a circuit is proposed in U.S. Pat. No. 5,663,917 to Oka et al., the entirety of which is hereby incorporated by reference herein.

FIG. 1B illustrates a circuit with high-voltage tolerance and low-voltage drive, such as may be found in M. Pelgrom and E. Dijkmans, “A 3/5V compatible I/O Buffer,” IEEE J. of Solid-State Circuits, vol. 30, No. 7, p.p. 823-825, July, 1995, the entirety of which is hereby incorporated by reference herein.

[0008] For purposes of circuit 10 of FIG. 1A, it is assumed that the breakdown voltage of the transistors used in the circuit is only slightly higher than ½ V_{HIGH}—the voltage swing of the input signal. The circuit 10 of FIG. 1A includes a pad driver 12 which includes p-channel and n-channel cascode stacks, which include MOS devices P1, P2, N1, N2, respectively. The cascode transistors P1 and N2 allow the output to pad node 14 to traverse between 0V and V_{HIGH} while the V_{GS}S (voltage gate to source) and V_{GO}S (voltage gate to drain) of all four transistors P1, P2, N1, N2 remain lower than ½ V_{HIGH} and thus lower than the breakdown voltage of the transistors. The voltage capability of the pad driver 12, therefore, is twice times larger than the voltage capability of the MOSFETs used in the driver. Such a circuit may be referred to as a “2x driver.”

[0009] For proper operation, the cascode pad driver 12 requires two in-phase input signals at nodes 18 and 20. Both signals must have a voltage swing that does not exceed ½ V_{HIGH} in order to avoid exceeding the voltage capability of the transistors used therein. These signals are provided from the level shifter 16 to the driver 12 through two conventional inverter chains. The level shifter 16 takes a 0 to ½ V_{HIGH} swing input data signal and produces a data signal that swings between ½ V_{HIGH} and V_{HIGH} at node 18. Naturally, the level shifter 16 should be implemented in such a way that none of its transistors experience voltage overstress.

[0010] Unlike the circuit 10 of FIG. 1A, the circuit 20 of FIG. 1B is a high voltage buffer with low voltage transistors that is biased from a lower supply voltage ½ V_{HIGH} and is characterized by high voltage tolerance but low voltage drive. As a result, its output drive is only between 0 and ½ V_{HIGH}. The structure, however, allows the pad voltage to exceed the supply voltage when the buffer is in the tristate mode, i.e., the circuit can be driven by a voltage of approximately V_{HIGH} without damaging the components. The circuit, therefore, may be characterized as having a “2x tolerance.” The circuit 10 of FIG. 1A may also be characterized as a “2x tolerance” circuit.

[0011] Three problems are eliminated to achieve the 2x tolerance of the circuit 20: (a) V_{DD} (voltage drain to gate) overstress of the n-channel transistor N2; (b) conduction of the dynamic gate and bulk biasing (conceptually illustrated using two pairs of switches).

[0012] Recently, two HV/BLVT’s with beyond-2x voltage capabilities have been reported. A first circuit has a 3.3V drive and 5V tolerance using 2V transistors and is proposed in L. Clark, “High-Voltage Output Buffer Fabricated on a 2V CMOS Technology,” Digest of Technical Papers, 1999 VLSI Symposium, p.p. 61-62. A circuit that extends the stress free range of a cascode stack beyond the difference between
While the above referenced circuits address some of the issues involved with interfacing an older higher operating voltage IC with a lower operating voltage technology, the circuits possess significant long term shortcomings. Presently, there is a movement within the semiconductor industry to migrate to sub-0.2 μm sizes towards 0.16 μm, and even 0.13 μm technology powered by sub-1.5V sources. It is expected that within the next four years, the supply voltages may even be in the sub-1V range. As the industry moves below the sub-0.2 μm area and the technologies is powered by sub-1.5V sources, interface buffers will be required to handle greater than the 2x multiples of the known art in order to function with older 0.24-0.35 μm powered devices. Thus, the known art is limited as a long term solution due to the migration towards increasingly smaller MOS transistor technologies in view of the continuing commercial viability of older IC components operating at voltages more than twice that of the breakdown voltages of the smaller devices.

As such, there is a need for an improved output buffer capable of interfacing at least two ICs having operating voltages which are multiples equal to or greater than 2x and which provides no gate-to-source, gate-to-drain, and drain-to-source stresses while providing at least 2x tolerance. Still further, there is a need for a tristate capable high voltage buffer implemented with low voltage transistors that approaches 3x voltage capabilities or better.

SUMMARY OF THE INVENTION

An integrated circuit includes an output buffer having a maximum voltage that approximates the highest voltage V_{MAX} applicable across at least one pair of nodes of a transistor. The output buffer is capable of delivering an output signal having a voltage swing V_{HIGH} of up to approximately three times the magnitude of V_{MAX}. The output buffer includes at least a first and a second transistor cascode stack, each of the stacks having a driver transistor and at least one cascode transistor. The output buffer also includes a biasing circuit for biasing at least one of the cascode transistors of each of the cascode stacks in response to said output signal such that the magnitude of the voltage applicable across each pair of nodes of each transistor in each cascode stack is less than or equal to V_{MAX}.

The buffer may be utilized to provide a tristate capable buffer circuit with up to 3x voltage capabilities, including 3x drive and 3x tolerance.

The above and other features of the present invention will be better understood from the following detailed description of the preferred embodiments of the invention that is provided in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings illustrate preferred embodiments of the invention, as well as other information pertinent to the disclosure, in which:

FIG. 1A is a circuit diagram of a known high voltage tolerance and high voltage driver buffer interface circuit;

FIG. 1B is a circuit diagram of a known high voltage tolerance and low voltage driver buffer interface circuit;

FIGS. 2A-2C are a schematic representation of a tristate capable high voltage buffer and accompanying active mode and tristate mode waveforms;

FIGS. 3A-3F are circuit diagrams of an exemplary driver for a 3x tristate capable buffer;

FIG. 4 is a circuit diagram of an exemplary driver for a 2x tristate capable buffer;

FIGS. 5A-5C are circuit diagrams of an exemplary level shifter circuit for a 3x tristate capable buffer;

FIG. 6 is a circuit diagram of an exemplary 3x tristate capable output buffer; and

FIG. 7 is a circuit diagram of a 3x tristate capable input buffer.

DETAILED DESCRIPTION

FIGS. 2A is a conceptual diagram of a tristate capable CMOS buffer 30 for interfacing a low supply voltage IC chip and a high supply voltage IC chip. The buffer 30 receives an input data signal from the low voltage supply at an input and produces an output data signal which corresponds to the input data signal but has a voltage swing between ground and the higher supply voltage V_{DD}. The buffer 30 includes a level shifter 32 and a driver stage 34. The level shifter produces data waveforms V_{p} and V_{n} shown in FIGS. 2B and 2C, depending upon whether the circuit is operated in the “Active Mode” or the “Tristate Mode.” As is conventional, the tristate mode is enabled via the OEN (output enable) input. In the “Active Mode,” V_{n} is typically the input data signal and V_{p} corresponds to V_{p} with a DC offset as shown in FIG. 2B. It is assumed, but not required, that the input data signal received from the low operating voltage IC has a voltage swing with a peak of V_{MAX}, V_{MAX} approaching the maximum voltage a transistor in the buffer circuitry can withstand, i.e. \( N_{GS}, N_{GD}, \) and \( N_{DS} \leq V_{MAX}. \)

FIG. 3A is a conceptual schematic of an exemplary embodiment of a pad driver 100 having stress-free range of 3x, i.e., the driver 100 is capable of driving an output signal V_{pad} at output node 102 having a voltage swing V_{HIGH} which is up to approximately three times the break-down voltage of any transistor used in the driver 100. Driver 100 includes a p-channel cascode stack and an n-channel cascode stack connected in series at output node 102. The p-channel cascode stack includes at least three p-channel MOS transistors P_{1}, P_{2}, P_{3} connected in series between the supply voltage V_{HIGH} and the output node 102. The n-channel cascode stack includes at least three n-channel MOS transistors N_{1}, N_{2}, N_{3} connected in series between the output node 102 and a relative ground V_{GROUND}.

The gate terminal of N_{1} is coupled to an input data signal V_{in} (FIG. 2A) and the gate terminal of P_{1} is coupled to a level shifted data signal V_{out} (FIG. 2A). These signals may be supplied by a level shifter circuit. The gate terminal...
of n-channel transistor $N_2$ is coupled to a first constant voltage such that the difference between the first constant voltage and $V_{\text{GROUND}}$ does not exceed $V_{\text{MAX}}$. For a true 3x buffer, this first constant voltage value equals approximately $V_{\text{MAX}}$ as shown in FIG. 3A. The gate terminal of p-channel transistor $P_2$ is coupled to a second constant voltage such that the difference between $V_{\text{HIGH}}$ and the second constant voltage does not exceed $V_{\text{MAX}}$. For a true 3x buffer, the second constant voltage is set to $2V_{\text{MAX}}$ as shown in FIG. 3A. The first constant voltage may be obtained from the low voltage supply IC. The second constant voltage may be generated internally within the buffer by conventional techniques.

In FIG. 3A, the pad voltage at output node 102 controls switches $S_1$ and $S_2$, which thereby provide dynamic gate biasing for cascode transistors $P_3$ and $N_3$. None of the six transistors $N_1$, $N_2$, $N_3$, $P_1$, $P_2$, and $P_3$ experience $V_{\text{GS}}$ or $V_{\text{DS}}$ voltage overstress if the following conditions are satisfied: (1) $S_1$ is closed when $V_{\text{pad}}$ falls below the first constant voltage (e.g., $V_{\text{MAX}}$), (2) $S_2$ is closed when $V_{\text{pad}}$ rises above the second constant voltage (e.g., $2V_{\text{MAX}}$), and (3) $S_1$ and $S_2$ maintain the gate voltage of $N_3$ and $P_3$ at or between the first or second constant voltages when $V_{\text{pad}}$ is at or above the first and second constant voltages. Of course, both $S_1$ and $S_2$ are never both closed.

The fact that $S_1$ must be closed or “on” when its control voltage (i.e., $V_{\text{pad}}$) is lower than its terminal voltage suggests that $S_1$ should be implemented using a p-channel transistor. $S_2$ on the other hand should be implemented using n-channel transistor because it must be closed or “on” when its control voltage is higher than its terminal voltages. This configuration is shown in FIG. 3B with the addition of n-channel transistor $N_4$ and p-channel transistor $P_4$. The drain terminals of each transistor are coupled at node 104 to the gate terminals of transistors $N_3$ and $P_3$.

The gates of both switch transistors $N_4$ and $P_4$ should be controlled by $V_{\text{pad}}$ but preferably are not directly connected to the pad node 102. A direct connection would result in voltage overstress of the switch transistors $N_4$ and $P_4$. For stress-free operation, the gate voltage of $P_4$ should follow $V_{\text{pad}}$ but it should not exceed $1/3V_{\text{HIGH}}$ or $2V_{\text{MAX}}$. Similarly, the gate voltage of $N_4$ should follow $V_{\text{pad}}$ but it should not go below $1/3V_{\text{HIGH}}$ or $V_{\text{MAX}}$. When the driver 100 of FIG. 3A is in tristate mode, nodes 110 and 112 have the required voltage excursions. The voltage at node 112 follows $V_{\text{pad}}$ down to $V_{\text{GROUND}}$, but it would not increase much beyond $1/3V_{\text{HIGH}}$. The voltage at node 110 on the other hand, follows $V_{\text{pad}}$ to the supply rail, but it would not decrease significantly below $1/3V_{\text{HIGH}}$. Note that “Vtn” is the threshold voltage of the n-channel devices, and $V_{\text{IP}}$ is the threshold voltage of the p-channel devices.

A driver 100 as shown in FIG. 3B has the gate terminals of $N_3$ and $P_3$ coupled directly to node 110 and 112, respectively, was simulated using 0.25 um 2.5V breakdown voltage technology and a $V_{\text{HIGH}}$ of 7.5V. The driver was placed in tristate mode (i.e., both $N_3$ and $P_3$ were OFF) and the pad voltage was varied between 0 and 7.5 V. As expected, the gate-source and gate-drain voltages of all eight transistors ($N_1$-$N_4$ and $P_1$-$P_4$) remained bounded to $2.5V$ (i.e., the voltages did not exceed $V_{\text{MAX}}$). In active mode, however, the voltage at node 112 is not only a function of both $V_{\text{pad}}$ (i.e., $V_{\text{pad}}$) but it is also a function of the gate voltage of transistor $N_1$. Similarly, the voltage at node 110 is a function of both $V_{\text{pad}}$ and the gate voltage of transistor $P_1$. As a result, immediately after each input transition, both $P_3$ ($S_3$) and $N_3$ ($S_2$) are ON and conducting a large “shunt through” current. More importantly, during the same time frame, the gate oxides of both $N_3$ and $P_3$ are subjected to voltage overstress. This issue is addressed in the circuit of FIG. 3C.

In FIG. 3C, the triple cascode is split into two separate circuits, one of which is always operated in tristate mode, and the switching transistors are shared. The controls for the switching transistors are derived from the “always-tristate” circuit. Switch transistors $P_3$ and $N_3$ respond only to changes in $V_{\text{pad}}$ at node 102 and provide dynamic protection for added transistors $N_4$ and $P_4$. Transistors $N_4$ and $P_4$ have gate terminals coupled to node 104, and drain terminals coupled to output node 102. The source terminal of $P_4$ is coupled to the gate terminal of $N_4$, and the source terminal of $N_4$ is coupled to the gate terminal of $P_4$. Since the drain and gate nodes of these two transistors $P_4$ and $N_4$ are coupled respectively to the gate and drain nodes of $N_3$ and $P_3$ (also referred to as nodes 104 and 102, respectively), the switches $N_4$ and $P_4$ also provide protection for $N_3$ and $P_3$. An exemplary high voltage buffer, low voltage transistor circuit is therefore achieved.

The gate-source and gate-drain voltages of all ten transistors ($N_1$-$N_4$, $P_1$-$P_4$) are always limited to $1/3V_{\text{HIGH}}$ or $V_{\text{MAX}}$. Drain-source (DS) voltages of transistors $N_5$, $P_5$, $N_3$ and $P_3$ can, however, exceed $V_{\text{MAX}}$ by at least one threshold voltage ($V_{\text{Th}}$). This may be addressed by extending the length of devices in the driver, but this may not be a viable option with increasing area constraints on ICs.

In order to keep $V_{\text{DS}}$ of $N_3\leq 1/3V_{\text{HIGH}}$ or $V_{\text{MAX}}$, node 106 may be pulled up to $1/3V_{\text{HIGH}}$. This is accomplished in the exemplary circuit configurations of FIGS. 3D and 3E via transistor $N_5$. Similarly, to keep $V_{\text{DS}}$ of $P_3\geq 1/3V_{\text{HIGH}}$ or $V_{\text{MAX}}$, node 106 may be pulled down to $1/3V_{\text{HIGH}}$ which is accomplished via transistor $P_5$. Note that when activated, $N_5$ does not connect node 106 directly to $1/3V_{\text{HIGH}}$; instead, it connects it to node 104, which for high pad voltages acquires the desired $1/3V_{\text{HIGH}}$ value. Similarly, node 108 is brought down to $1/3V_{\text{HIGH}}$ indirectly via node 104. This feature guarantees that transistors $N_3$ and $P_3$ are not overstressed.

The final issue that should be addressed is the potential drain-source overstress of transistors $N_4$ and $P_4$. Below is a brief description of the causes of the drain-source overstress of transistor $N_4$, and a circuit approach to resolve this issue is shown in FIG. 3F. The cause of overstress of $P_4$ is analogous to that of $N_4$ and is not described.

When the pad voltage at node 102 equals $V_{\text{HIGH}}$, the drain-source voltages of transistors $N_2$ and $N_3$ are as follows: $V_{\text{DS}}$ of $N_2=1/3V_{\text{HIGH}}+(V_{\text{GS}}$ of $N_2-V_{\text{DS}}$ of $N_3$) and $V_{\text{DS}}$ of $N_3=1/3V_{\text{HIGH}}+V_{\text{DS}}$ of $N_3$, respectively. Immediately after input transition of the input data signal at the gate terminal of $N_1$, both $V_{\text{GS}}$ of $N_1$ and $V_{\text{DS}}$ of $N_1$ can increase so that the cascode transistors $N_2$ and $N_3$ can carry the current consequently. These changes alter $V_{\text{DS}}$ of $N_2$ and $V_{\text{DS}}$ of $N_3$. According to the first equation, the change in $V_{\text{DS}}$ of $N_1$ can be kept low at approximately constant and equal to $1/3V_{\text{HIGH}}$ by making $N_4$ and $N_2$ identical in size. The second equation reveals that $N_3$ would experience a drain-source overstress.
This overstress could be prevented by connecting an additional cascode transistor \(N_5\) between the drain of \(N_3\) and node 102 as shown in FIG. 3F. With the addition of transistor \(N_5\) in FIG. 3F to the n-channel cascode stack, the drain-source voltage of \(N_3\) becomes \(V_{\text{DS}} = \frac{1}{3} V_{\text{HIGH}} \) due to the addition of \(V_{\text{GS}}\) of \(N_5\). This drain-source voltage can now be kept constant and equal to \(\frac{1}{3} V_{\text{HIGH}}\) by simply making \(N_5\) and \(N_3\) approximately equal in size. This drain-source overstress protection requires the gate terminal of \(N_5\) to have a potential of \(V_{\text{HIGH}}\) whenever the pad node has potential \(V_{\text{HIGH}}\). The gate terminal potential of transistor \(N_5\) should, however, be lowered to \(\frac{1}{3} V_{\text{HIGH}}\) as pad node 102 traverses toward \(V_{\text{GROUND}}\), i.e., \(N_5\) requires a \(V_{\text{HIGH}}\)-to-\(\frac{1}{3} V_{\text{HIGH}}\) dynamic gate biasing. Such biasing is readily available at node 108.

Similarly, the drain-source overstress of \(P_3\) is eliminated by the addition of the \(P_2\) cascode transistor coupled between the drain terminal of \(P_3\) and output node 102. As shown in FIG. 3F, required dynamic biasing (0-to-\(\frac{1}{3} V_{\text{HIGH}}\)) is obtained by connecting the gate terminal of transistor \(P_2\) to node 106.

FIG. 4 is provided to show that the same basic approach as described above in achieving a 3x driver with no gate-source, gate-drain, and drain-source overvoltage may be utilized to provide a 2x driver 200 that exhibits no gate-source, gate-drain, and drain-source overstress. Note that the driver 200 of FIG. 4 includes n-channel and p-channel cascode stacks connected at an output node 202 as shown in FIGS. 3A-3E. The supply rail is set to \(2V_{\text{MAX}}\) in the 2x driver 200 instead of \(3V_{\text{MAX}}\). Also, the gate terminals of \(P_3\) and \(N_2\) are coupled to a single constant voltage at node 204 (shown as \(V_{\text{MAX}}\)), such that the difference between \(V_{\text{GS}}\) and node 204 is not greater than \(V_{\text{MAX}}\) and the difference between node 204 and \(V_{\text{GROUND}}\) is not greater than \(V_{\text{MAX}}\). The input data signal at the gate terminal of \(N_2\) may have a maximum voltage swing of \(2V_{\text{MAX}}\), and the input data signal at the gate terminal of \(P_3\) is the input data signal of \(N_2\) level shifted by the DC value at node 204, i.e., the data signal traverses between \(V_{\text{MAX}}\) and \(2V_{\text{MAX}}\). Control circuits 206 and 208 provide dynamic gate biasing signals \(Gn\) and \(Gp\) to n-channel transistor \(N_4\) and p-channel transistor \(P_3\), respectively.

Both signals \(Gn\) and \(Gp\) are in-phase with the output signal produced at node 202 and have a voltage swing of \(V_{\text{MAX}}\). With \(Gn\) traversing between \(V_{\text{MAX}}\) and \(V_{\text{HIGH}}\) and \(Gp\) traversing between \(V_{\text{GROUND}}\) and \(V_{\text{MAX}}\). To understand how the circuit 200 of FIG. 4 provides stress-free operation, the behavior of the circuit before and after input transition may be considered. Assuming that the initial condition is as follows: input is low (the gate of \(N_1\) is \(0V\) and the gate of \(P_1\) is \(V_{\text{MAX}}\)), and the output is \(V_{\text{HIGH}}\). Due to the action of the biasing circuits 206, 208, \(Gn\) and \(Gp\) respectively are \(V_{\text{HIGH}}\) and \(V_{\text{GROUND}}\). Under these stated conditions, it can be shown that the potential difference between any two transistor terminals does not exceed \(V_{\text{MAX}}\).

As the input signal at the gate terminal of \(N_1\) goes high, the current carried by \(N_1\) increases. In order for this current to be conducted by \(N_0\) and \(N_1\), the transistor source potentials of \(N_0\) and \(N_1\) decrease from their initial values of \(V_{\text{MAX}}\) and \(V_{\text{GROUND}}\). If \(N_0\) and \(N_1\) are matched, the source decrement for both transistors is the same and \(V_{\text{DS}}\) of \(N_1\) remains initially constant and approximately equal to \(V_{\text{MAX}}\). The drain-source voltage of \(N_3\) also is less than \(V_{\text{MAX}}\). As the load capacitance is being discharged, the drain voltage of \(N_3\) decreases. At some point, the biasing circuit 206 is activated and it lowers the voltage of \(N_3\) to prevent \(V_{\text{GS}}\) of transistor \(N_3\) from becoming too large. The output node 202 keeps discharging until it reaches \(V_{\text{GROUND}}\) where it settles.

It can be shown that for output “low” or \(V_{\text{GROUND}}\) and input of \(V_{\text{MAX}}\), no terminal-to-terminal voltages exceed \(V_{\text{MAX}}\). The circuit 200 exhibits similar behavior when the input transitions from “high” to “low” (and output transitions from “low” to “high”). During this transition, the presence of \(P_3\) prevents transistor \(P_3\) from developing large drain-source voltages while the control circuit 208 provides gate-source and gate-drain overvoltage protection for \(P_3\).

Biasing circuits 206 and 208 may be implemented as shown in FIG. 4 with p-channel transistors \(P_3\) and \(P_1\) and n-channel transistors \(N_0\) and \(N_2\). P-channel transistor \(P_1\) has its gate terminal coupled to \(V_{\text{pad}}\) at output node 202, a drain terminal coupled to the constant voltage at node 204, and a source terminal coupled to the gate terminal of \(N_3\). Transistor \(P_3\) has its gate terminal coupled to node 204, a drain terminal coupled to output node 202, and its source terminal coupled to the gate terminal of \(N_3\). Likewise, biasing circuit 208 may be implemented with n-channel transistor \(N_3\) having its gate terminal coupled to output node 202, its source terminal coupled to the gate terminal of \(P_3\), and its drain terminal coupled to the constant voltage at node 204. N-channel transistor \(N_2\) has its gate terminal coupled to the constant voltage at node 204, its source terminal coupled to the gate terminal of \(P_3\), and its drain terminal coupled to output node 202. The biasing circuits provide the advantage of not dissipating static power.

FIGS. 5A-5C are circuit schematics of an exemplary level shifter circuit 300 for use in a 3x tristate capable buffer. This circuit may be used to provide signal \(V_s\) to driver 100. A level shifter circuit comprises an input n-channel transistor, a cascode stack for protecting the input transistor from voltage overstress and including at least one n-channel cascode transistor, and a load transistor coupled to the cascode stack at an output node. As shown in FIG. 5A, the level shifter 300 for providing a signal to a driver as described above may generally be illustrated as a modified N-MOS inverter comprising at least four n-channel transistors \(N_8\), \(N_9\), \(N_{10}\), and \(N_{11}\), coupled in series. A source terminal of input transistor \(N_8\) is coupled to \(V_{\text{GROUND}}\) a source terminal of cascode transistor \(N_9\) is coupled to a drain terminal of \(N_5\), a source terminal of cascode transistor \(N_{10}\) is coupled to a drain terminal of \(N_7\), and a drain and gate terminals of load transistor \(N_{11}\) are both coupled to supply \(V_{\text{HIGH}}\) or \(3V_{\text{MAX}}\). Transistors \(N_5\) and \(N_{10}\) are connected together at first output node 302. A gate terminal of \(N_9\) is coupled to an input data signal with a maximum voltage swing which does not exceed \(V_{\text{MAX}}\). This input data signal may be provided by the low voltage IC. The gate terminals of \(N_9\) and \(N_{10}\) are coupled to a first constant voltage and a second constant voltages, respectively, such that a difference between \(V_{\text{HIGH}}\) and the second constant voltage does not exceed \(V_{\text{MAX}}\) and a difference between the first constant voltage and \(V_{\text{GROUND}}\) does not exceed \(V_{\text{MAX}}\). For a true 3x level shifter stage, the first and second constant voltages are \(V_{\text{MAX}}\) (1/3 \(V_{\text{HIGH}}\)) and 2 \(V_{\text{MAX}}\).
The circuit 300 provides a very robust output signal at node 302, but can dissipate static power. To reduce this static power dissipation, the duty cycle of the input data signal can be reduced. If the input data signal duty cycle is reduced, the output duty cycle must still be preserved. Therefore, an exemplary level shifter may further include a second inverter stage driven out-of-phase with the input inverter by one half cycle and an RS (reset-set) latch connecting the two inverter stages. This exemplary embodiment of a level shifter is shown in FIG. 5B.

The level-shifter of FIG. 5B includes inverter 300a and inverter 300b (N12, N13, N14, and N15) coupled to an RS latch 306. The level shifter also optionally includes cross-coupled p-channel transistors P1 and P2 and added series n-channel transistors N16 and N17. These devices (P1, P2, N16, and N17) are not required but help the level shifter produce smooth output waveforms at outputs 308 and 310. Each inverter 300a, 300b comprises an input transistor coupled to input signals IN1 and IN2 at their gate terminals, a cascode stack and load transistor. Input signals IN1 and IN2 are shown as having reduced duty cycles below 50%. The “dashed” wave forms illustrate input waveforms with 50% duty cycles. The cascode transistors provide overstress protection for all of the devices. For effective overstress protection all devices preferably are the same size. With equally sized input and load transistors, the level shifter of FIG. 5B exhibits a gain of near-unity for large inverters. Inverter gain is on the first order insensitive to process and temperature variations. The level-shifter of FIG. 5B, however, dissipates static power if input signals IN1 and IN2 have normal duty cycles of 50% (as shown by the dashed input signals of FIG. 5B).

Since the inverter stages 300a, 300b dissipate static power whenever their inputs are “high,” the static power dissipation could be reduced if the two inverters are impulse driven. Impulse duration, however, should be sufficiently large so that the latch 306 can change its state. If the two inverter structure are pulse driven, both inverter outputs are “high” most of the time. In order to be able to retain its state, the RS latch 306 should be implemented using NAND gates (as opposed to NOR gates).

The circuit of FIG. 5C illustrates one means of generating the modified pulse signals IN1 and IN2. The circuit of FIG. 5C also provides the additional advantage of producing two additional signals at outputs 316 and 318 having voltage swings between 0 and 3V_{MAX}. One of these signals may be used to provide signal V106 to drive the n-channel transistor N12 of the driver stage 200. Transistors N8, N9, N12 and N13 are also part of the one-shot circuit. P-channel transistors P10 and P11 may be included for smoother waveform generation. A pulse is produced at the gate of the transistors N12 whenever there is a positive input transition and at the gate of input transistor N12 whenever there is a negative input transistor. The duration of the produced pulse is approximately equal to t_mos+t_{NS,N9}+t_{RS} where t_mos is the delay of the MOS inverter, t_{NS,N9} is the delay of the N9/N8 inverter and t_{RS} is the switching delay of the RS latch 312. As long as RS latch 308 and RS latch 312 are equally loaded and present minor loading to their corresponding driving circuits, the duration of the generated driving pulses would be sufficient to guarantee switching of RS latch 308.

FIG. 6 is an exemplary embodiment of a 3x tristate capable output buffer circuit 400 including a level shifter circuit 300 described above coupled to a driver stage 200 described above. The tristate-capable 7V output buffer 400 was fabricated with a 0.25 μm 2.5V CMOS process. The circuit was designed to drive a 10 pF load capacitance at 200MHz. The transistor sizes (width/length in μm) were as follows:

<table>
<thead>
<tr>
<th>Name</th>
<th>Width/Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>N1</td>
<td>3.7/0.24</td>
</tr>
<tr>
<td>N2</td>
<td>3.7/0.24</td>
</tr>
<tr>
<td>N3</td>
<td>7.4/0.24</td>
</tr>
<tr>
<td>N4</td>
<td>6.6/0.24</td>
</tr>
<tr>
<td>P1</td>
<td>2.1/0.24</td>
</tr>
<tr>
<td>P2</td>
<td>3.8/0.24</td>
</tr>
<tr>
<td>P3</td>
<td>7.4/0.28</td>
</tr>
<tr>
<td>P4</td>
<td>7.4/0.28</td>
</tr>
<tr>
<td>P5</td>
<td>13.0/0.28</td>
</tr>
<tr>
<td>P6</td>
<td>13.0/0.28</td>
</tr>
</tbody>
</table>

The above designed circuit was tested, and “on-wafer” probing was performed successfully. To verify high-voltage capability, internal nodes 104, 106 and 108 were monitored while the buffer was operated in a “package-like environment.” This was done by bonding a bare die directly on a PCB (printed circuit board) and using active probes. The obtained waveforms were then compared to the output waveform generated at node 102. The potential differences V102-V106, V102-V108 and V102-V104 are indicative of the presence or absence of GS and GD voltage overstress. These differences remained bounded to approximately ±2.5 V. Therefore, the voltage drive and tolerance of the developed buffer circuit is nearly three times larger than the breakdown voltage of the MOS devices used in the circuit.

FIG. 7 illustrates that the circuit approach described in FIGS. 3D-3F may be used to form an input buffer circuit which receives an input signal at node 102 which swings between 0 and $3V_{MAX}$ and produces an output data which swings between 0 and $V_{MAX}$ at output node 506. Of course the output signal can be amplified by an inverter 510 or chain of inverters as is conventional. The n-channel and p-channel cascode stacks of FIGS. 3D-3F are not required for the function of an exemplary input driver. This circuitry is shown within the dashed box 508. These cascode stacks may be disabled by coupling the gate of P1 to the supply voltage and the gate of N1 to VGROUND.

An input stage 502 may be designed as shown in FIGS. 3D-3F from transistors N9 and P9 particularly those circuit configuration introduced in FIGS. 3D and 3E. Likewise, the biasing circuit 208 of FIG. 4 including n-channel transistors N9a and N9b may be coupled to the input stage 502 as shown. An input data signal from a high voltage IC presented at node 102 and having a voltage swing between 0 and $3V_{MAX}$ produces a data signal at node 506 which is appropriate for safely driving a low voltage IC. The
We claim:
1. An integrated circuit comprising an output buffer having a maximum voltage that approximates the highest voltage \( V_{\text{MAX}} \) applicable across at least one pair of nodes of a transistor, the output buffer for delivering an output signal having a voltage swing \( V_{\text{HIGH}} \) of up to about three times the magnitude of \( V_{\text{MAX}} \), said output buffer comprising:
   (a) at least a first and a second transistor cascode stack, each of said stacks having a driver transistor and at least one cascode transistor; and
   (b) a biasing circuit for biasing said at least one cascode transistor of each of said cascode stacks in response to said output signal such that the magnitude of the voltage applicable across each pair of nodes of each transistor in each cascode stack is less than or equal to \( V_{\text{MAX}} \).

2. The integrated circuit of claim 1, wherein said biasing circuit comprises switching means for applying to a biasing node of a cascode transistor of each of said first and second cascode stacks a first voltage having a magnitude of about \( V_{\text{HIGH}}-V_{\text{MAX}} \) when the output signal voltage is greater than or equal to about \( V_{\text{HIGH}}-V_{\text{MAX}} \) and a second voltage having a magnitude of about \( V_{\text{HIGH}}-2V_{\text{MAX}} \) when the output signal voltage is less than or equal to about \( V_{\text{HIGH}}-2V_{\text{MAX}} \).

3. The integrated circuit of claim 2, wherein said first transistor cascode stack includes transistors of a first conduction type and said second cascode stack includes transistors of a second conduction type.

4. The integrated circuit of claim 3 wherein each of said at least first and second transistor cascode stacks includes at least two cascode transistors, wherein said first voltage is coupled to a biasing node of one of said cascode transistors in said first cascode stack, said second voltage is coupled to a biasing node of at least one of said cascode transistors in said second cascode stack, and wherein said switching means applies, to the biasing node of said other cascode transistor of each of said first and second cascode stacks, said first voltage when the output signal voltage is greater than or equal to about \( V_{\text{HIGH}}-V_{\text{MAX}} \) and said second voltage when the output signal voltage is less than or equal to about \( V_{\text{HIGH}}-V_{\text{MAX}} \).

5. The integrated circuit of claim 4, wherein said switching means comprises a fourth transistor of said second conduction type coupling said first voltage to said biasing nodes of said other cascode transistors and a fourth transistor of said first conduction type coupling said second voltage to said biasing nodes of said other cascode transistors.

6. The integrated circuit of claim 5, wherein said fourth transistors are coupled together at a first node coupled to said biasing nodes of said other transistors of said cascode stacks, said switching means further comprising a fifth transistor of said second conduction type coupling said biasing node of said fourth transistor of said first conduction type to an output node and a fifth transistor of said first conduction type coupling said biasing node of said fourth transistor of said second conduction type to said output node, said fifth transistors having respective biasing nodes coupled to said first node.

7. The integrated circuit of claim 6, further comprising a sixth transistor of said second conduction type and a sixth transistor of said first conduction type coupled between said biasing nodes of said fourth transistors at said first node, said sixth transistors having biasing nodes coupled to said output node.

8. The integrated circuit of claim 6, further comprising a sixth transistor of said second conduction type and a sixth transistor of said first conduction type coupled between said biasing nodes of said fourth transistors, wherein said sixth transistors are coupled together at said first node, and wherein a biasing terminal of said sixth transistor of said first conduction type is coupled to a biasing terminal of said fourth transistor of said first conduction type and a biasing terminal of said sixth transistor of said second conduction type is coupled to a biasing terminal of said fourth transistor of said second conduction type.

9. The integrated circuit of claim 8, wherein said first cascode stack further comprises a seventh transistor of said first conduction type coupled between said other cascode transistor of said first cascode stack and said output node, and said second cascode stack further comprises a seventh cascode transistor of said second conduction type coupled between said other cascode transistor of said second cascode stack and said output node and wherein a biasing node of said seventh transistor of said second conduction type is coupled to a biasing node of said fourth transistor of said second conduction type, and a biasing node of said seventh transistor of said second conduction type is coupled to a biasing node of said fourth transistor of said second conduction type.

10. An integrated circuit comprising a tristate capable output buffer having a maximum voltage that approximates the highest voltage \( V_{\text{MAX}} \) applicable across at least one pair of nodes of a transistor, the output buffer for delivering an output signal having a voltage swing \( V_{\text{HIGH}} \) of up to about three times the magnitude of \( V_{\text{MAX}} \) having a maximum voltage that approximates the highest voltage \( V_{\text{MAX}} \) applicable across at least one pair of nodes of each transistor in each cascode stack.

(a) a voltage driver, comprising:
   (i) at least a first and a second transistor cascode stack, each of said stacks having a driver transistor and at least one cascode transistor; and
   (ii) a biasing circuit for biasing said at least one cascode transistor of each of said cascode stacks in response to said output signal such that the magnitude of the voltage applicable across each pair of nodes of each transistor in each cascode stack is less than or equal to \( V_{\text{MAX}} \).

(b) a level shifter circuit, said level shifter circuit providing at least one voltage shifted data signal to a driver transistor of said voltage driver in response to an input data signal when said buffer is in an active mode, said circuit further configured to place said buffer in a tristate mode in response to an enable signal.

11. The integrated circuit of claim 10, wherein said level shifter circuit comprises:
   a first inverter for providing a first voltage shifted data signal comprising at least an input transistor having a voltage applicable across each pair of nodes of each transistor in each cascode stack.
biasing node for receiving a first input data signal, a cascode stack connected in series with said input transistor and a load transistor.

12. The integrated circuit of claim 11, wherein said level shifter further comprises:

(a) a second inverter for providing a second voltage shifted data signal comprising at least an input transistor having a biasing node for receiving a second input data signal, a cascode stack connected in series with said input transistor and a load transistor; and

(b) a first latch for producing said at least one voltage shifted data signal in response to said first and second voltage shifted data signals when said input transistors of said inverters are driven with a first and second modified input data signals, respectively, corresponding to said input data signals.

13. The integrated circuit of claim 12, wherein said latch is a RS latch and said level shifter further comprises a one-shot circuit for generating said first and second modified input data signals.

14. The integrated circuit of claim 12, wherein said biasing circuit comprises switching means for applying to a biasing node of a cascode transistor of each of said first and second cascode stacks a first voltage having a magnitude of about \( V_{\text{HIGH}} - V_{\text{MAX}} \) when the output signal voltage is greater than or equal to about \( V_{\text{HIGH}} - 2V_{\text{MAX}} \) and said second voltage coupled to a biasing node of at least one of said cascode transistors in said first cascode stack further comprises a seventh transistor of said second conduction type coupling said first voltage to said biasing nodes of said other cascode transistors.

15. The integrated circuit of claim 14, wherein said first transistor cascode stack includes transistors of a first conduction type and said second cascode stack includes transistors of a second conduction type.

16. The integrated circuit of claim 15 wherein each of said at least first and second transistor cascode stacks includes at least two cascode transistors, wherein said first voltage is coupled to a biasing node of one of said cascode transistors in said first cascode stack, said second voltage is coupled to a biasing node of at least one of said cascode transistors in said second cascode stack, and wherein said switching means includes, to the biasing node of said other cascode transistor of each of said first and second cascode stacks, said first voltage when the output signal voltage is greater than or equal to about \( V_{\text{HIGH}} - V_{\text{MAX}} \) and said second voltage when the output signal voltage is less than or equal to about \( V_{\text{HIGH}} - 2V_{\text{MAX}} \).

17. The integrated circuit of claim 16, wherein said switching means comprises a fourth transistor of said second conduction type coupling said first voltage to said biasing nodes of said other cascode transistors and a fourth transistor of said first conduction type coupling said second voltage to said biasing nodes of said other cascode transistors.

18. The integrated circuit of claim 17, wherein said fourth transistors are coupled together at a first node coupled to said biasing nodes of said other transistors of said cascode stacks, said switching means further comprising a fifth transistor of said second conduction type coupling said biasing node of said fourth transistor of said first conduction type to an output node and a fifth transistor of said first conduction type coupling said biasing node of said fourth transistor of said second conduction type to said output node, said fifth transistors having respective biasing nodes coupled to said first node.

19. The integrated circuit of claim 18, further comprising a sixth transistor of said second conduction type and a sixth transistor of said first conduction type coupled between said biasing nodes of said fourth transistors at said first node, said sixth transistors having biasing nodes coupled to said output node.

20. The integrated circuit of claim 18, further comprising a sixth transistor of said second conduction type and a sixth transistor of said first conduction type coupled between said biasing nodes of said fourth transistors, wherein said sixth transistors are coupled together at said first node, and wherein a biasing terminal of said sixth transistor of said first conduction type is coupled to a biasing terminal of said fourth transistor of said second conduction type.

21. The integrated circuit of claim 20, wherein said first cascode stack further comprises a seventh transistor of said first conduction type coupled between said other cascode transistor of said first cascode stack and said output node, and said second cascode stack further comprises a seventh cascode transistor of said second conduction type coupled between said other cascode transistor of said second cascode stack and said output node and wherein a biasing node of said seventh transistor of said second conduction type is coupled to a biasing node of said fourth transistor of said second conduction type, and a biasing node of said seventh transistor of said first conduction type is coupled to a biasing node of said fourth transistor of said first conduction type.