Simple Rail-to-Rail Constant-Transconductance Input Stage Operating in Strong Inversion

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***Abstract*— A CMOS op-amp input and gain stage suitable for low voltage operation are introduced. The input stage operates in strong inversion and has common-mode range beyond rail-to-rail. It uses two complementary differential pairs connected in parallel. The common-mode dependent current biasing employs only four transistors, does not require additional voltage references, current switches and/or current mirrors and does not increase the minimum required supply voltage. The variation of the net transconductance is approximately 15% over the entire common-mode range. The gain-stage has constant output resistance. In addition it reduces the variation of the net transconductance due to variations in μ_n/μ_p ratio.**

I. Introduction

A widely used technique for obtaining a rail-to-rail input range, when designing low-voltage op-amps, is to connect two complementary differential pairs in parallel as shown in Fig. 1(a). In this way one guarantees that for any common-mode input voltage at least one of the differential pairs will operate properly. This simple topology is rarely used, however, because its net transconductance g_{m_T} varies by a factor of two over the common-mode input range. In mid-supply range, where both pairs operate, the net transconductance is given by:

$$g_{m_T} = g_{m_n} + g_{m_p} \tag{1}$$

However, when the input common-mode voltage approaches the positive (negative) rail g_{m_T} reduces to $g_{m_n}(g_{m_p})$ respectively. This variation does not allow optimal frequency compensation of multi-stage op-amps and also increases their distortion.

Since the individual differential-pair transconductances g_{m_n} and g_{m_p} are well-defined functions of the of the tail currents I_n and I_p, respectively, a general method for obtaining common-mode–*independent* net transconductance is to employ common-mode - *dependent* current biasing. In other words, we balance the reduction in $g_{m_n}(g_{m_p})$ (caused by the reduction of $I_n(I_p)$ when $V_{in_{CM}}$ approaches $V_{ss}(V_{dd})$) by increasing $I_p(I_n)$ (e.g. Fig. 1(b)).

In the case of an input stage using BJT's or MOS transistors in weak inversion the requirement that g_{m_T} be independent of $V_{in_{CM}}$ translates into the following, simple to implement, current-biasing requirement:

$$I_n + I_p = const. \tag{2}$$

If MOS transistors in strong inversion are to be used in such a rail-to-rail input stage the current biasing requirement is:

$$\sqrt{I_n} + \sqrt{I_p} = const. \quad \text{for} \quad \beta_n = \beta_p \tag{3}$$

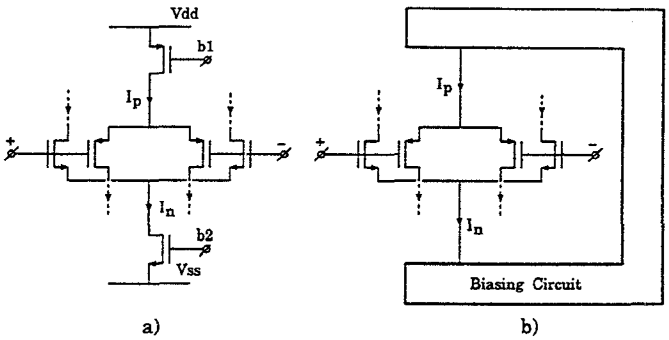

Figure 1: (a) Simple rail-to-rail input stage; (b) Conceptual schematic of constant-g_m rail-to-rail input stage.

and, more general:

$$\sqrt{(2/\beta_n)I_n} + \sqrt{(2/\beta_p)I_p} = const. \quad \text{for} \quad \beta_n \neq \beta_p \tag{4}$$

The main differences between various rail-to-rail input stage topologies reported in the literature is the employed biasing scheme. Those schemes targeting the MOS-strong inversion case can loosely be classified as either exact or approximate. All schemes realizing equations (3) or (4) [1], [2], [3] are considered exact, because under ideal conditions (perfect matching and no second order effects) they result in a constant net transconductance. The approximate schemes are based on the assumption that the tail currents I_n, I_p take either their nominal value or are completely turned off. Those schemes are usually implemented by use of a simple 1 : 3 current mirrors [3], [4] and can reduce the g_{m_T}-variation to within 15%. Unfortunately, most of the reported strong inversion biasing circuits have high complexity.

In Section II we present a simple approximate scheme which requires only four additional transistors and has a g_{m_T} variation of approximately 15%. In Section III a gain stage which has constant output resistance is introduced. Also, it reduces the variations of the effective net transconductance caused by variations in the mobility ratio μ_n/μ_p.

II. The Proposed Rail-to-Rail Input Stage

The input stage, shown in Fig. 2(a), is topologically identical to that reported in [5]. However, the aspect ratios of the four additional transistors in the Fig. 2(a) circuit is three times that of the corresponding differential-pair transistors. The nominal value of the tail currents I_{S_n} and

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I_{S_p} is $4I_0$ and must be selected sufficiently large to ensure strong-inversion operation. The aspect ratios of the n and p-channel transitory are selected such that $\beta_n = \beta_p = \beta$. Under this conditions the Fig. 2(a) circuit guarantees rail-to-rail operation with a 15% variation in g_{m_T}. To show this let us first consider the operation of the $M_5 - M_8$ quartet. As discussed in [5] if a CMOS current source ($M_5 - M_6$) is connected in series with a current sink ($M_7 - M_8$), the pair which must carry the higher current is forced into the triode region and thus the smaller of the two currents is conducted. For our case:

$$I_x = \min\left(\frac{3}{4}I_{S_n}, \frac{3}{4}I_{S_p}\right) = \frac{3}{4}\min(I_{S_n}, I_{S_p}) \qquad (5)$$

Hence, the current I_x and the currents $I_p = I_{S_p} - I_x$ ($I_n = I_{S_n} - I_x$) conducted by the differential-pair transistors $M_{1,2}(M_{3,4})$ of the Fig. 2(a) stage are,

1) $V_{in_{CM}}$ close to V_{ss}:
$$I_x = 3/4 I_{S_n} = 0$$
$$I_n = 1/4 I_{S_n} = 0$$
$$I_p = I_{S_p} - I_x = 4I_0 - I_x = 4I_0$$

2) $V_{in_{CM}}$ near mid-supply:
$$I_x = 3I_0$$
$$I_n = I_{S_n} - I_x = 4I_0 - 3I_0 = I_0$$
$$I_p = I_{S_p} - I_x = 4I_0 - 3I_0 = I_0$$

3) $V_{in_{CM}}$ close to V_{dd}:
$$I_x = 3/4 I_{S_p} = 0$$
$$I_n = I_{S_n} - I_x = 4I_0$$
$$I_p = 1/4 I_{S_p} = 0$$

Thus for the above three regions of operation, where the tail currents I_{S_n}, I_{S_p} have their nominal ($4I_0$) value or have zero value, the total transconductance (see equation (1)) is the same and given by:

$$g_{m_T} = 2\sqrt{(2/\beta)I_0} \quad when \quad \beta_n = \beta_p = \beta \qquad (6)$$

For the transition regions, where $0 < I_{S_{n,p}} < 4I_0$, g_{m_T} is not constant and slightly higher than the above value. The maximum g_{m_T} deviation can be calculated and is approximately 15%.

The Fig. 2(a) rail-to-rail input stage was simulated using HSPICE and BSIM2 (level 13) models for MOSIS 2-micron ORBIT Analog Process. The size of the transistors and the value of the constant bias current $4I_0$ were as indicated on the schematic. Fig. 2(b) shows the variation of I_n and I_p bias currents as the $V_{in_{CM}}$ is swept from V_{SS} to V_{dd}. The three regions (near-V_{SS}, mid-supply and near-V_{dd}) where I_n and I_p must remain constant are evident. The non-zero slope of those regions is due to the finite output resistance of the used transistors. In Fig. 2(c) the simulated individual (g_{m_n}, g_{m_p}) and net transconductance (g_{m_T}) are plotted v.s. the input common-mode voltage. As expected, there are two "bumps" in the g_{m_T} plot corresponding to the two transition regions. The small "glitch" present within each "bump" can not be predicted if the simple square-law relation is used to model the voltage-current behavior of the MOS transistor. Since "glitches" occur when one of the bias currents (I_n or I_p) has relatively low value, they are most likely due to one of the differential pairs entering moderate and then weak inversion region of operation.

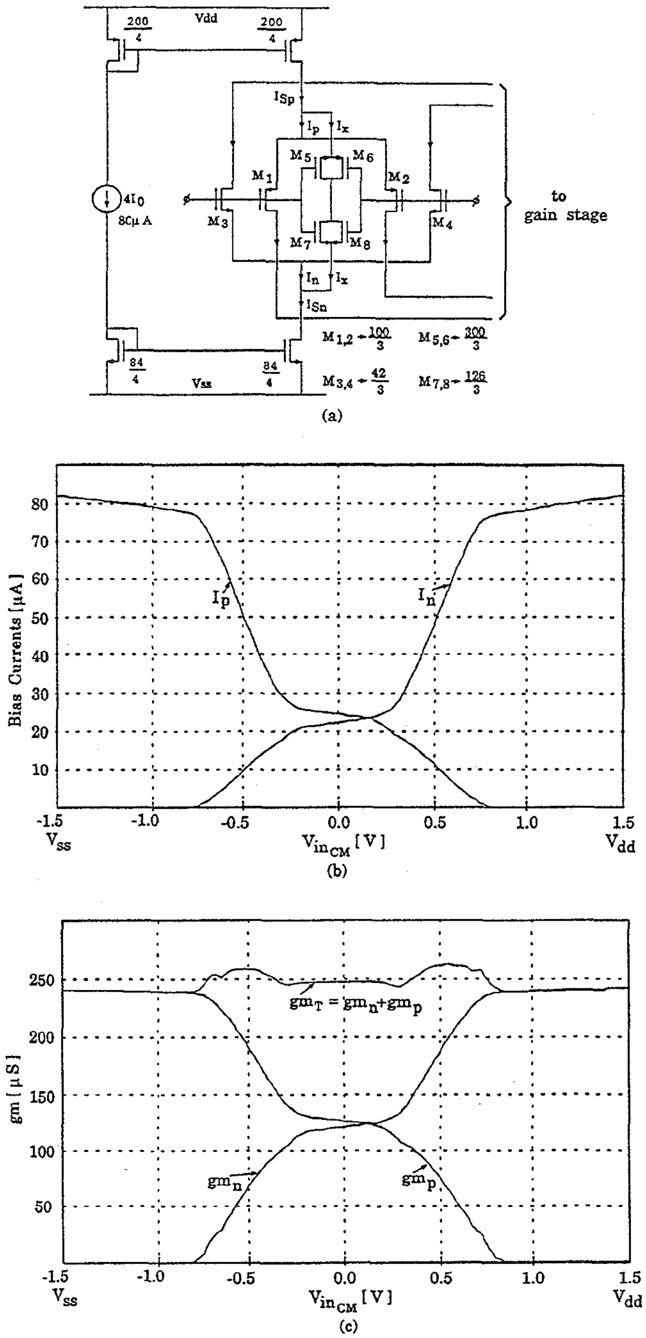

Figure 2: Proposed Rail-to-Rail Input Stage: (a) Schematic; (b) Bias Currents v.s. $V_{in_{CM}}$; (c) Individual and Net Transconductance v.s. $V_{in_{CM}}$;

Because of finite r_o effects, I_n and I_p are slightly larger than 20μA in the mid-supply region. For this reason the net transconductance in this region is slightly higher than that in the near-rail regions. As is the case with many other rail-to-rail input stages, the one presented in this

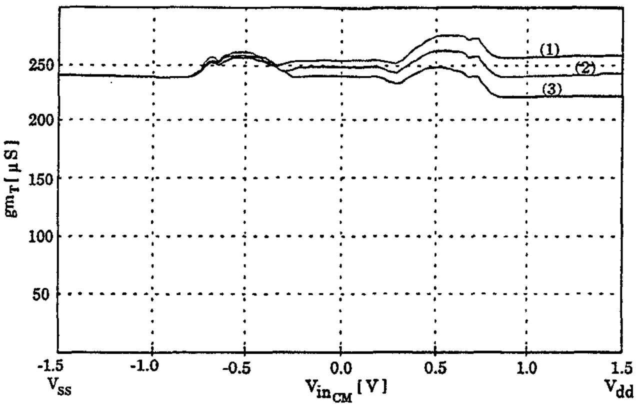

Figure 3: Net transconductance v.s. $V_{in_{CM}}$ for three different values of $\frac{\mu_n}{\mu_p}$: (1) "actual" $\frac{\mu_n}{\mu_p}$ is 15% higher than the one used in the design; (2) "actual" $\frac{\mu_n}{\mu_p}$ = used $\frac{\mu_n}{\mu_p}$; (3) "actual" $\frac{\mu_n}{\mu_p}$ is 15% less than the used one;

paper relies on matching the transconductance parameter (β) of the used n-channel transistors to that of the used p-channel transistors. If the ratio between the mobility of the n-channel transistors and the mobility of the p-channel transistors μ_n/μ_p is exactly known then β_n can be made very close to β_p by simply sizing the transistors whose β's are to be matched in accordance with: $W_n = W_p \frac{\mu_p}{\mu_n}$ for $L_n = L_p$. Unfortunately, for a given process from one run to another the ratio of the mobilities could vary as much as 30% from its nominal value [1] used to determine "the best" n-channel and p-channel aspect ratios. To illustrate the effect this variation would have on the net transconductance of the proposed input stage two additional simulations were performed. The width of the n-channel devices was changed to 48μ and 36μ — that is, a change of +15% and −15% from its nominal 42μ width. Since β-equality is achieved for $\frac{W_n}{W_p} = \frac{42}{100}$, transistor having W_n equal to $48\mu(36\mu)$ would be equivalent to transistor having $W = 42$(the nominal value) and μ increased (decreased) by 15%. Fig. 3 shows the results from the simulations.

III. The Gain Stage

Fig. 4 shows single-stage unbuffered op-amp which uses the input stage described in the previous section. The gain stage consists of two MOS-R current mirrors and a floating current source. Here, as in many other reported in the literature rail-to-rail topologies, in addition to providing voltage gain the gain stage is used to sum the small signal (differential) currents generated by the two input-stage differential pairs. However, there are some unique properties possessed by this gain stage. First, its output resistance — and thus the op-amp's gain — is independent of the level of the injected by the input stage common-mode currents (I_n, I_p). As a result the distortion caused by common-mode dependent gain is kept at its minimum. To show that the output resistance is constant it is sufficient to show that the output resistance of each current mirror is constant.

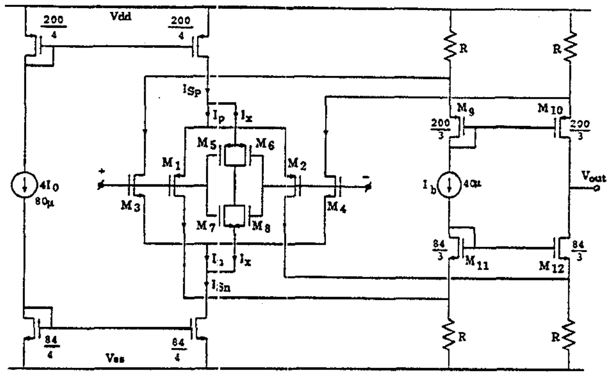

Figure 4: Single-stage unbuffered op-amp.

The output resistance of the Fig. 5 current mirror, given by:

$$r_{out_n} = (1 + g_{m_{12}} R) r_{o_{12}} \tag{7}$$

would be constant if both the transconductance and the output resistance ($g_{m_{12}}$ and $r_{o_{12}}$) of M_{12} transistor are constant. The latter is guaranteed when the current conducted by M_{12} ($I_{M_{12}}$) is constant. The KVL equation written for the Fig. 5 MOS-R current mirror:

$$R\left(\frac{1}{2}I_p + I_b\right) + \sqrt{\frac{2}{\beta}I_b} = R\left(\frac{1}{2}I_p + I_{M_{12}}\right) + \sqrt{\frac{2}{\beta}I_{M_{12}}} \tag{8}$$

where $\beta = \beta_{11} = \beta_{12}$, shows that indeed:

$$I_{M_{12}} = I_b = const. \tag{9}$$

Second, due to the finite $g_{m_{11,12}}$ and R only a portion of the differential input current will be transferred to the output (see the equivalent circuit shown in Fig. 5(b)):

$$i_{out} = \frac{g_{m_{11,12}} R}{1 + g_{m_{11,12}} R} i_{in} \tag{10}$$

This property seems undesirable because it reduces the effective transconductance g'_{m_T} of this single-stage op-amp (e.g. Fig. 6). More importantly, if the factors $\frac{g_{m_{9,10}} R}{1+g_{m_{9,10}} R}$ and $\frac{g_{m_{11,12}} R}{1+g_{m_{11,12}} R}$ are not equal, g'_{m_T} will not be constant

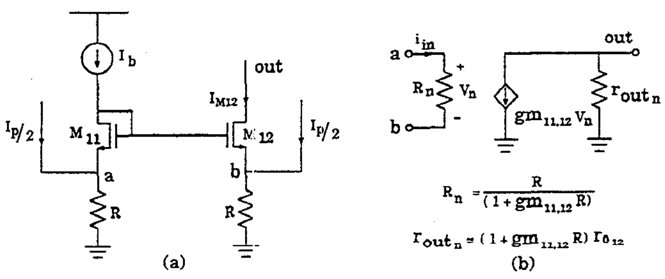

Figure 5: (a) n-channel R-MOS current mirror; (b) small differential signal equivalent of (a).

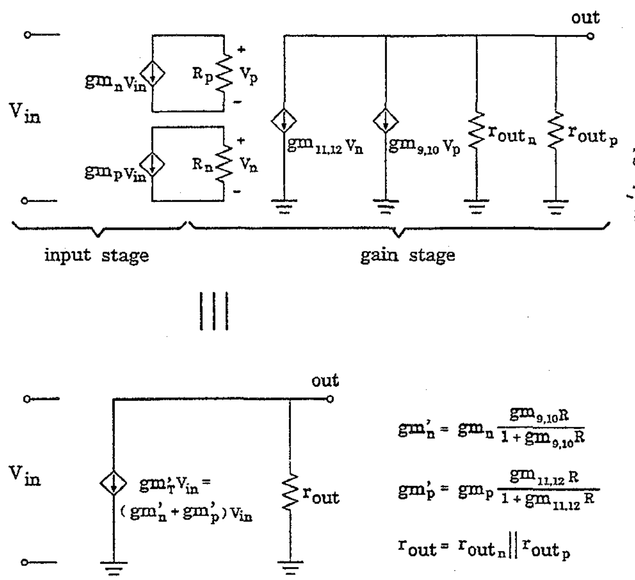

Figure 6: Simplified equivalent circuits of Fig. 4 single-stage op-amp.

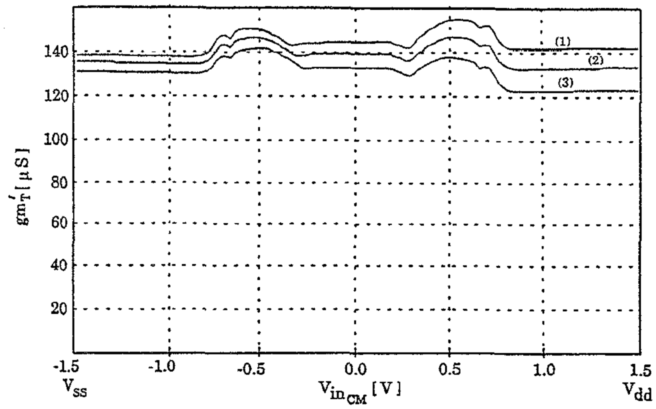

Figure 7: Effective net transconductance v.s. $V_{in_{CM}}$ for three different values of $\frac{\mu_n}{\mu_p}$: (1) "actual" $\frac{\mu_n}{\mu_p}$ is 15% higher than the one used in the design; (2) "actual" $\frac{\mu_n}{\mu_p}$ = used $\frac{\mu_n}{\mu_p}$; (3) "actual" $\frac{\mu_n}{\mu_p}$ is 15% less than the used one;

over the common-mode input range. Achieving equality of the above current gain expressions can be accomplished be making $g_{m_{9,10}} = g_{m_{11,12}} = g_m$. This is done as in the input stage by sizing M_9, M_{10} and M_{11}, M_{12} so their β's are identical.

The advantage of this gain stage over others becomes obvious only when the variations in g_{m_T} and g'_{m_T} due to differences between the actual ratio of the mobilities and the one used to carry out the design are compared. The smaller the product $g_m R$ the lower the g'_{m_T}-variation. However, this product should not be made lower than unity in order to retain a sufficiently large overall op-amp gain. As can be seen from the plots shown in Fig. 7, the change of μ_n effects the transconductance of both the near-V_{ss} and near-V_{dd} range in same direction which results in lower relative variation within each curve. This can be explained with the fact that now each individual g'_{m_n} and g'_{m_p} is determined by the transconductances of both n-channel and p-channel transistors.

If higher output resistance is desired the simple M_9,M_{10} and M_{11},M_{12} current mirrors can be replaced by high-swing cascoded current mirrors without altering the properties of the gain stage.

IV. Conclusions

A simple rail-to-rail input stage operating in strong inversion was presented. Its net transconductance variation is approximately 15% over the entire common-mode range. A new gain stage was introduced. It was shown that the transconductance variation in this gain stage caused by imperfect β-matching is reduced as compared to previous techniques.

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