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A Method for Reducing the Variation in "On" Resistance of a MOS Sampling Switch

A. K. Ong, V. I. Prodanov, M. Tarsia
Bell Laboratories, Lucent Technologies
600 Mountain Avenue, Murray Hill, NJ 07974, USA

Abstract

Variation in the "on" resistance of a MOS sampling switch can introduce distortion into the front end of a switched-capacitor filter or analog-to-digital converter. We review three methods commonly used to linearize the resistance of a MOS switch and propose a new technique that addresses their limitations. A practical method for implementation is also suggested.

I. Introduction

Variation in the "on" resistance, R_{on}, of a MOS sampling switch can introduce distortion into the front-end of a switched-capacitor filter or analog-to-digital converter. This variation can be easily seen by considering the simple sample-and-hold circuit depicted in Figure 1. The circuit is comprised of an NMOS device, M_1, and a sampling capacitor, C_s. The gate of M_1 is driven between *Gnd* and V_{dd}. If square-law behavior in M_1 is assumed, and V_{ds} is small, R_{on} can be written as

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_t)} \quad . \tag{1}$$

Thus, during the conduction phase, when the gate voltage, Φ_s, is held at the supply voltage, R_{on} will be a function of the input signal level, V_{in}, in two manners. First, V_{gs} is equal to $V_{dd} - V_{in}$. Second, the threshold voltage, V_t, is dependent on V_{in} through the source-bulk voltage, V_{sb}:

$$V_t = V_{to} + \gamma[\sqrt{2|\phi_f| + V_{sb}} - \sqrt{2|\phi_f|}] \quad . \tag{2}$$

First-order variations in V_t can be eliminated if the source and body of M_1 are tied together. However, this is only possible if device M_1 is implemented in its own separate well. Even so, shorting the body and source may not be desirable due to the large parasitic capacitance associated with that well. In applications that demand high-speed sampling, parasitic capacitances should be minimized whenever possible.

A typical design practice is simply to size device M_1 large enough such that at extreme ranges of the input signal, V_{in}, the value of R_{on} remains acceptably small. The f_{-3dB} bandwidth of the sampling circuit in Figure 1 is

$$f_{-3dB} = \frac{1}{2\pi R_{on} C_s} = \frac{1}{2\pi} \times \frac{\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_t)}{C_s} \quad . \tag{3}$$

If the input signal has a bandwidth of f_b, it is generally considered sufficient for most low- to medium-resolution applications to size M_1 such that the minimum –3 dB cutoff frequency is approximately 5x to 10x larger than f_b. However, this rule-of-thumb becomes problematic as the feature size of the technology continues to shrink along with the supply voltage. Since V_t does not scale as rapidly as V_{dd}, the resulting gate-source overdrive on M_1 becomes smaller. Therefore, from (1), it follows that the size of M_1 must be increased in order to keep R_{on} at the same previously acceptable small level. At some point, self loading from the capacitance contributed by M_1 will reduce the –3 dB bandwidth of the circuit by an unacceptable amount. Furthermore,

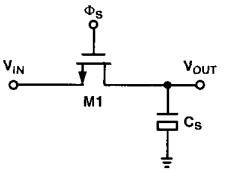


Figure 1 Simple MOS sample-and-hold.

charge injection errors and clock driver loading increase commensurately with larger switches.

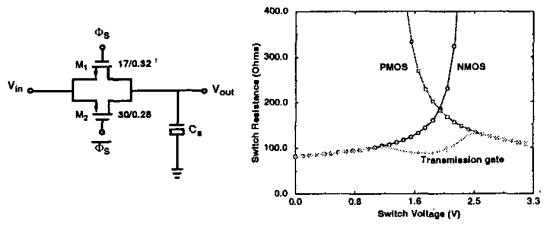
Given constraints on parasitic capacitance and charge injection, it can be difficult to guarantee a sufficiently low value for R_{on} over an entire input signal range simply by using large device sizes. This difficulty is compounded by the fact that although the supply voltage may shrink with technology, the input signal range should remain relatively constant in order to prevent a loss in dynamic range.

Brute force voltage boosting can be used to reduce the value of R_{on} for a given device size. With voltage boosting, a specialized switch driver pumps the gate voltage of M_1 beyond the supply voltage. A typical voltage doubler such as that described in [1] is used to drive the gate of M_1 between *Gnd* and $2V_{dd} - V_t$. Under such conditions, it follows from (1) that R_{on} of M_1 will be reduced commensurately. However, device reliability becomes a concern as the gate voltage is driven beyond V_{dd}. In many cases, destructive breakdown mechanisms are greatly accelerated when the voltage across the gate oxide exceeds V_{dd} by some small margin [2].

It would be preferable if a switch's "on" resistance could be decoupled from the signal that it must pass. Then, once the MOS device has been sized to have an adequately low "on" resistance at the midpoint of the input signal excursion, additional circuitry would guarantee that R_{on} remains relatively constant over some specified range of the input signal. In the following sections of this paper, three common methods that accomplish this goal are reviewed and their limitations are discussed. In Section V, we propose a new technique that addresses shortcomings in these existing methods, and we suggest a practical means of implementation.

II. CMOS Switch

If the sampling switch in Figure 1 is implemented as a transmission gate comprised of *n*- and *p*-transistors in parallel, then the switch resistance exhibits improved linearity over the input signal swing range. Figure 2(a) shows a CMOS switch that has been designed for a nominal small-signal resistance of approximately 100Ω. The gates of the devices are tied to *Gnd* and 3.3V. The aspect ratios of M_1 and M_2 are chosen such that the "on" resistance of the *n*- and *p*-transistors are roughly equal to 100Ω at input common mode voltages of 1.1V and 2.1V, respectively. Figure 2(b) illustrates how as V_{in} approaches V_{dd}, the NMOS device turns off, but the PMOS device remains conducting. Similarly, as V_{in} approaches *Gnd*, the PMOS device enters a high-resistance region while the NMOS device remains conducting. As seen, the parallel combination of M_1 and M_2 ensures conduction over a large input signal range with a somewhat linear resistance characteristic.



(a) (b)

Figure 2 (a) CMOS switch designed for a nominal resistance of 100Ω and (b) its equivalent resistance as a function of V_{in}.

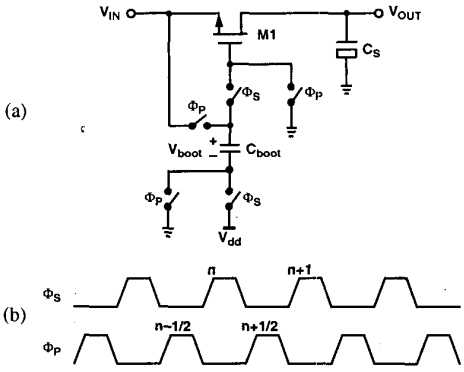


Figure 3 (a) Brooks switch driver and (b) its timing diagram.

However, despite improvement in the linearization of R_{on}, the corresponding nonlinearities in the *n*- and *p*-transistors are not matched, and substantial variations in R_{on} still occur. This variation becomes more extreme if devices M_1 and M_2 are chosen to have equal *W/L* ratios, which is often done to cancel clock feedthrough and, to a lesser extent, switch charge injection.

III. Brooks Switch Driver

The linearity of the sampling switch in Figure 1 can be improved if the gate-source voltage, V_{gs}, of M_1 remains constant when the switch is conducting, despite any variations in the input signal. This can be accomplished by sampling the input voltage when the switch is nonconducting, and then bootstrapping the gate of the switch to $V_{dd} + V_{in}$ during conduction. A simplified schematic of such a bootstrap driver is illustrated in Figure 3(a). This circuit was first described in [3]. The operation of this circuit is as follows. On the precharge phase, Φ_p, the gate of M_1 is grounded, and the voltage sampled across the boot capacitor is

$$V_{boot}\left[n-\frac{1}{2}\right] = V_{in}\left[n-\frac{1}{2}\right] \quad . \tag{4}$$

On the conduction phase, Φ_s, the boot capacitor acts like a floating battery, and the gate of M_1 is driven to

$$V_{gM1}[n] = V_{dd} + V_{in}\left[n-\frac{1}{2}\right] \quad . \tag{5}$$

Therefore, the "on" resistance of M_1 can be written as

$$R_{on} = \frac{1}{\mu_n C_{ox}\frac{W}{L}\left(V_{dd} + V_{in}\left[n-\frac{1}{2}\right] - V_{in}[n] - V_t\right)} \quad . \tag{6}$$

If the input signal varies slowly with respect to the sampling frequency, then $V_{in}[n - 1/2] \approx V_{in}[n]$. However, R_{on} is still not completely independent of V_{in} because V_t is a function of V_{in}. Furthermore, if the input signal frequency, f_{in}, were to approach 1/2 of the sampling

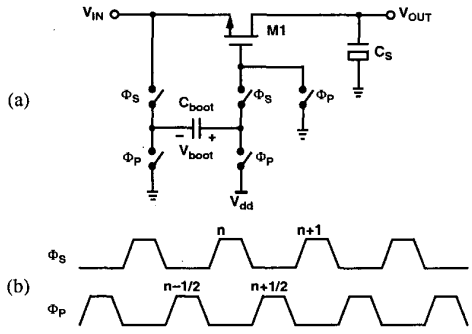


Figure 4 (a) Abo switch driver and (b) its timing diagram.

frequency, f_s, the discrepancy between $V_{in}[n - 1/2]$ and $V_{in}[n]$ would be maximized. Consequently, this technique is only suitable in cases where $f_{in} << f_s$.

IV. Abo Switch Driver

The technique proposed by Abo in [4] is not limited to the same constraints on $f_{in}<<f_s$ as the Brooks switch driver. A simplified diagram of the Abo switch driver is shown in Figure 4(a). On the precharge phase, Φ_p, the gate of M_1 is grounded, and the boot capacitor is charged to V_{dd}. Then on the conduction phase, Φ_s, the gate of the switch transistor, M_1, is bootstrapped to $V_{dd} + V_{in}$. Thus the "on" resistance of M_1 is

$$R_{on} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{dd} - V_t)} \quad . \tag{7}$$

Since the input signal is sampled on the conduction phase instead of the precharge phase, this linearization technique is not limited to cases where $f_{in}<<f_s$. However, the dependence of R_{on} upon V_{in} through the threshold voltage persists.

V. Proposed Compensation Technique

The dependence of R_{on} on the threshold voltage can be removed if the gate of the switch device is bootstrapped to a value that includes the threshold voltage. In other words, with reference to Figure 1, it is desirable to bootstrap the gate of M_1 to $V_{dd} + V_{in} + V_t$. This can be accomplished using the proposed switch driver illustrated in Figure 5(a). During the precharge phase, switch M_1 is grounded, and the boot capacitor is charged to V_{dd}. Then, during the conduction phase, the operational amplifier forces node *A* to be equal to the input voltage, V_{in}, which implies that the voltage on node *B* is

$$V_B = V_{in} + V_{tM2} + \sqrt{\frac{2I_{bias}}{\mu_n C_{ox}(W/L)_{M2}}} \quad . \tag{8}$$

Transistors M_1 and M_2 are matched, and their source nodes are at the same potential. Therefore, their threshold voltages are nominally equal, notwithstanding the influence of drain-induced barrier lowering. Thus, during conduction when the gate of M_1 is bootstrapped to $V_{dd} + V_B$, the "on" resistance of M_1 is

$$R_{on} = \frac{1}{\mu_n C_{ox}\frac{W}{L}\left(V_{dd} + \sqrt{\frac{2I_{bias}}{\mu_n C_{ox}(W/L)_{M2}}}\right)} \quad . \tag{9}$$

In principle, R_{on} of M_1 is now dependent only on technology parameters, the aspect ratio of the device, and a signal-independent bias current, I_{bias}. In practice, however, the differing drain-source voltages of M_1 and M_2 will cause their threshold voltages to be slightly unequal, so some small dependence of R_{on} on the input signal will remain.

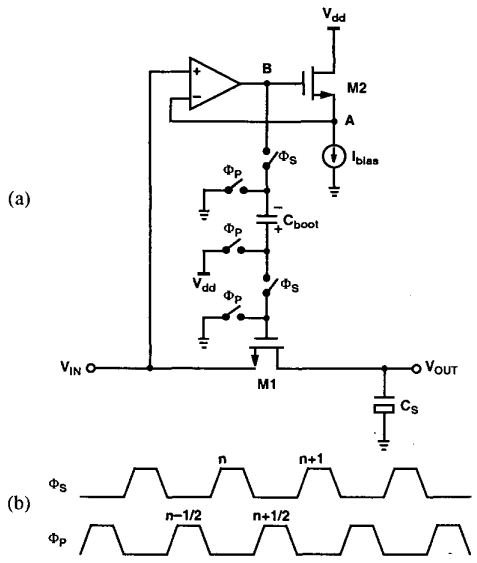


Figure 5 (a) Proposed switch driver and (b) its timing diagram.

A relative measure of the improvement in the distortion performance using the proposed technique can be estimated using the test network shown in Figure 6. A 91-MHz sinusoidal input is applied to four circuits, each with a nominal –3 dB bandwidth of approximately 1 GHz when the input common-mode voltage is 1.6V. The reference circuit is an ideal *RC* network with R = 100Ω and C_s = 1500fF. The output of this circuit, V_{outa}, is expected to be free of distortion, within the limits of the simulation environment. The subsequent three circuits are: 1) a transmission gate, 2) an NMOS switch with a floating battery charged to V_{dd} connected between the input and the gate of the switch, and 3) an NMOS switch with its gate driven by the proposed closed-loop controller. Models from Lucent's MBIC 0.25-µm process have been used in these simulations. Since these circuits approximate the sampling phase of a full sample-and-hold amplifier, any distortion introduced by nonlinearity in these networks is also expected to be present in the outputs of the full sample-and-hold circuits. The Brooks switch driver of Figure 3 is not included because it is assumed to have similar or slightly worse performance than the Abo driver with the primary difference arising from the 1/2 period delay in sampling V_{in}, as discussed in Section III.

The simulation results shown in Figure 7 indicate that use of the proposed technique reduces in less harmonic distortion compared with existing techniques. As simulation check, the benchmark RC network shows no measurable distortion in Figure 7(a). Figures 7(b), (c), and (d) show that both the switch driver of [4] and the proposed technique suppress harmonic distortion by a large margin compared to the use of a transmission gate switch. Comparing the Abo driver with the proposed technique, we see that by decoupling R_{on} from V_t, the signal-to-distortion ratio is improved by approximately three additional dB.

In actual practice, fully-differential circuit topologies and bottom-plate sampling techniques would also be used to reduce the influence of charge-injection and clock feedthrough in any sample-and-hold circuit. Fully-differential operation also results in the cancellation of odd-order harmonics. In principle, these circuit techniques are fully compatible with the proposed switch driver.

In a practical implementation of the proposed switch driver, it is possible to merge the matched sensing transistor, M_5 of Figure 6, into the operational amplifier itself. In Figure 8, this is illustrated using a

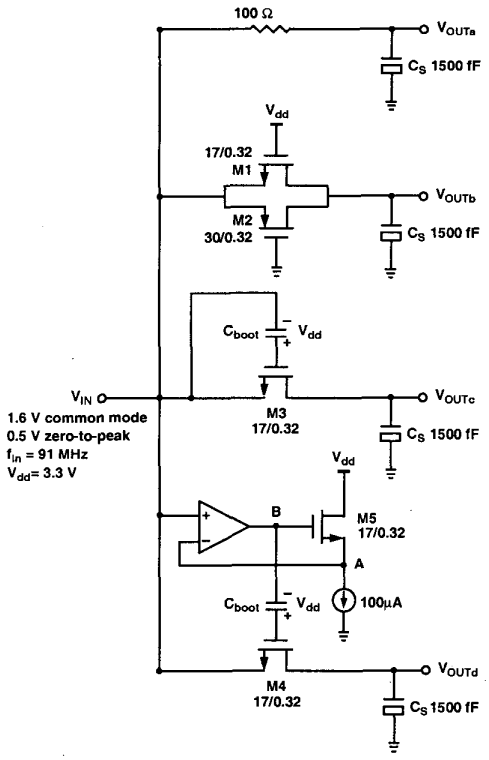


Figure 6 (a) Test network to evaluate relative distortion performance.

folded-cascode amplifier. Comparing Figures 6 and 8, we see that feedback forces the output of this amplifier to equal the input voltage, V_{in}, meaning that node B then equals the desired voltage, $V_{in} + V_t + V_{ov}$, where V_{ov} is the gate-source overdrive voltage of M_5, which is only dependent on technology parameters and I_{bias}, not on V_{in}.

VI. Conclusions

A new method for linearizing the resistance of a MOS sampling switch has been described. The proposed technique desensitizes the value of switch "on" resistance to the input signal that it must pass. It also reduces the influence of switch threshold voltage, which in general is also a function of V_{in}. Simulation results using Lucent's 0.25-µm MBIC process show that the new technique can suppress R_{on}-related harmonic distortion in a sample-and-hold circuit by an additional 3 dB compared with existing methods that do not compensate for the dependence of V_t on V_{in}.

VII. Acknowledgments

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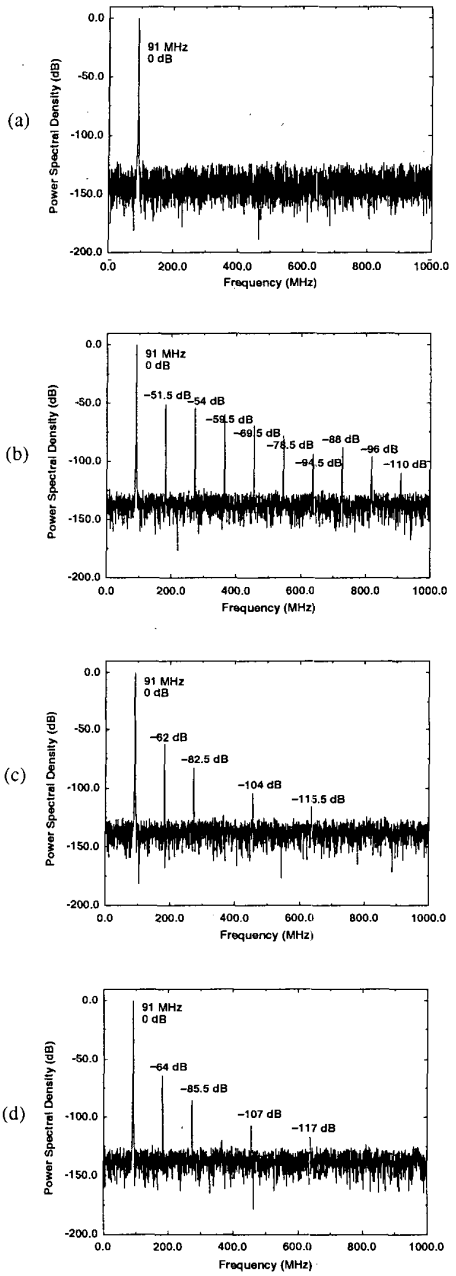

Figure 7 Output spectral content of (a) RC network, (b) transmission gate, (c) switch bootstrapped with Abo driver, and (c) switch bootstrapped using the proposed technique.

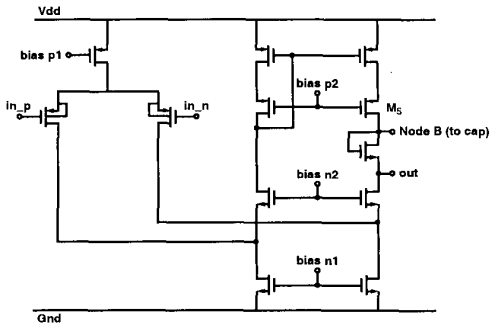

Figure 8 A practical implementation of the amplifier and sensing transistor required in the proposed switch driver.