ROBUST HIGH-PASS AND NOTCH Gm – (grounded) C BIQUADS: HOW MANY DIFFERENT TOPOLOGIES ARE THERE?

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ABSTRACT

This paper deals with Gm–C biquadratic filters that use grounded capacitors. We derive all practical HP and notch filter topologies that do not require critical component matching. The aim of this derivation was to discover new architectures. The result of this derivation is quite unexpected: there are only three distinct topologies (one notch and two high-pass). None of them is particularly new because all reported in the literature biquad circuits are their embodiments.

1. INTRODUCTION

In general there are two analog filter synthesis techniques: the prototype-based technique and the biquad-based technique. Active filters based upon a passive prototype have lower sensitivity to component mismatch than their biquad counterparts. Biquad-based filters, on the other hand, allow for easier on-chip automatic tuning[1]. Both filter structures can be implemented using op-amp based integrators or Gm–C integrators.

Because of their "open-loop" nature Gm-C integrators exhibit lower phase "errors" at higher frequency; thus they are better suited for implementation of high-frequency filters. Gm–C filter architectures that use only grounded capacitors are of special interest, because standard (digital) CMOS process does not provide high-density linear floating capacitors.

It is well known that low-pass and band-pass filter characteristics can be obtained (simultaneously) from a set of integrators[2] connected in a loop. This is also true if the integrators are of the type Gm–(grounded) C. Hence, the implementation of LP and BP biquadratic filters using only grounded capacitors does not present a problem.

Second order transfer functions having pair of finite transmission zeroes (in theory) can be obtained from the same architecture by taking weighted sum of the input signal and the produced LP and BP output signals [5], i.e.

$$H_{general}(s) = k_1 + k_2 H_{LP}(s) + k_3 H_{BP}(s)$$

[1] "master-slave" or VCO-based tuning

[2] One integrator is "lossy" while the other one is "lossless"

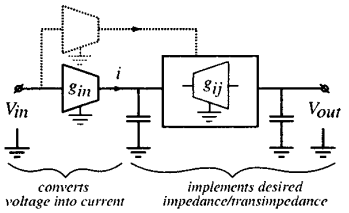

Figure 1: Conceptual schematic of Gm-(grounded)C biquad.

In practice however this approach fails to produce robust high-pass and notch filter characteristics. The reason is that here the "missing" numerator terms are obtained via cancellation. Thus, the attainable attenuation is determined by component matching and it is limited to $35 - 40dB$.

Alternative high-pass architectures with no requirements for critical component matching can be found in [1], [2], [3], [4], [5], [6] and probably many other publications. Gm – (grounded) C notch architectures with no component matching requirements have been reported in at least two papers [5], [6].

While each of these fine publications provides a "good set" of filter topologies none of them seems to clearly identify the "complete set".

The aim of this paper is to derive *the complete set* of practical HP and notch filter topologies that do not require critical component matching.

2. PRELIMINARY CONSIDERATIONS

Here will we assume that single-input/single-output (SI/SO) transconductors are to be used. Once the filter topology is determined, constraints related to a specific transconductor topology could then be taken into account. For example, two SI/SO transconductors whose outputs are coupled could be replaced by a single differential-input/SO transconductor after imposing the following two requirements:

$$|gm_1| = |gm_2| \quad \& \quad sign[gm_1] = -sign[gm_2]$$

Such considerations are *not* required when implementing fully-differential filters[3]. A fully-differential design is

[3] In products, fully-differential designs are usually used.

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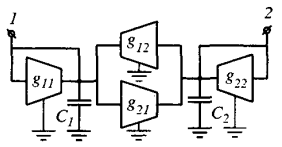

Figure 2: A general two-node Gm-(grounded)C network.

obtained directly from the single-ended filter topology if each SI/SO transconductor is replaced by a DI/DO transconductor and the number of capacitors is doubled.

Biquads must be implemented in such a way that their natural frequencies are not affected by the cascading. This suggests that a cascadable Gm-(grounded)C biquad must have high input impedance, i.e. it must have the topology shown in Fig. 1. The input transconductor(s) in Fig. 1 architecture converts the applied input voltage into current(s). The produced current(s) is(are) then injected into a network comprised of two grounded capacitors and several transconductor blocks. The network converts the injected current(s) into voltages. Any of these voltages[4] can than be taken as an output voltage. We see that for a given $Gm-(grounded)C$ network (mathematically described by either its admittance matrix $[Y(s)]$ or its impedance matrix $[Z(s)]$) many but finite number of transfer functions can be implemented. Thus, the study of only few Gm-C networks can yield information about large number of biquad configurations.

In the next two section several Gm-(grounded)C networks will be derived and studied.

3. THE TWO-NODE NETWORK

Among all networks that can exhibit second-order response Fig. 2 is the one with minimum number of nodes - only two. The admittance matrix of this circuit, i.e.

$$Y_{Fig.2}(s) = \begin{bmatrix} g_{11}+sC_1 & g_{12} \\ g_{21} & g_{22}+sC_2 \end{bmatrix} \quad (1)$$

can be inverted to obtain circuit's impedance matrix:

$$Z_{Fig.2}(s) = \begin{bmatrix} z_{11}(s) & z_{12}(s) \\ z_{21}(s) & z_{22}(s) \end{bmatrix} \quad (2)$$

This matrix tells us how Fig. 2 "converts" injected currents into voltages. Thus, it shows the type of transfer functions that one can implement.

It can be easily verified that the above four entries are:

$$z_{11} = \frac{g_{22}+sC_2}{D(s)} \qquad z_{12} = \frac{-g_{12}}{D(s)}$$
$$z_{21} = \frac{-g_{21}}{D(s)} \qquad z_{22} = \frac{g_{11}+sC_1}{D(s)}$$

where: $D(s) = s^2C_1C_2 + s(C_1g_{22} + C_2g_{11}) + g_{11}g_{22} - g_{12}g_{21}$

Since none of the four numerators contains an s^2 term *Fig. 2 circuit can not be used to implement high-pass, notch or any other transfer function that has a pair of transmission zeroes.*

[4]Circuit terminal potentials "measured" with respect to ground

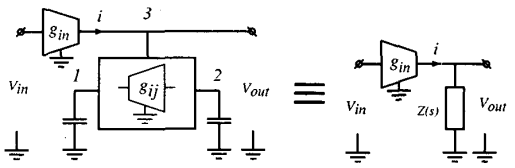

Figure 3: Conceptual schematic of Gm-(grounded)C biquad capable of implementing transfer functions with second-order numerator.

4. THE THREE-NODE NETWORK

The next in complexity network is the three-node network. Since we are concerned with circuits that exhibit a second-order response, only two of the three nodes (say nodes "1" and "2") should be capacitively loaded. The admittance matrix of such a circuit is thus given by:

$$Y(s) = \begin{bmatrix} g_{11}+sC_1 & g_{12} & g_{13} \\ g_{21} & g_{22}+sC_2 & g_{23} \\ g_{31} & g_{32} & g_{33} \end{bmatrix} \quad (3)$$

Inverting the above matrix we obtain circuit's impedance matrix, i.e.

$$Z(s) = \begin{bmatrix} z_{11}(s) & z_{12}(s) & z_{13}(s) \\ z_{21}(s) & z_{22}(s) & z_{23}(s) \\ z_{31}(s) & z_{32}(s) & z_{33}(s) \end{bmatrix} \quad (4)$$

Only z_{33} entry of the Z matrix has second-order numerator.

$$N_{z_{33}} = g_{33}[s^2C_1C_2 + s(C_2g_{11} + C_1g_{22}) + g_{11}g_{22} - g_{12}g_{21}] \quad (5)$$

Thus, using a three-node network one can implement transfer functions with second-order numerators. *All such implementations however will have the same topology - the one shown in Fig. 3.*

The denominators of all $z_{ij}(s)$ entries are the same and equal to the determinant of $Y(s)$.

4.1. Robust Notch Topologies

Since the zeroes of an ideal notch transfer function are located on the imaginary axes, both g_{11} and g_{22} must be 0. With this restriction the numerator of z_{33} becomes:

$$N_{z_{33}}(s) = s^2C_1C_2g_{33} - g_{12}g_{21}g_{33}$$

and the denominator becomes:

$$D(s) = s^2C_1C_2g_{33} - s\,(C_1g_{23}g_{32} + C_2g_{31}g_{13}) + g_{21}g_{13}g_{32} + \\ + g_{12}g_{31}g_{23} - g_{12}g_{21}g_{33}$$

The poles and the zeroes of a robust notch filter must have the same imaginary parts. Hence, the pole and the zero imaginary part must be set by the same circuit elements. This suggests that the first two zero-order terms of $D(s)$ must equal zero, i.e.

$$g_{13}g_{32} = 0 \quad \& \quad g_{31}g_{23} = 0 \quad (6)$$

One might be tempted to set all four transconductances g_{13}, g_{32}, g_{31} and g_{23} to zero. This however would also nullify

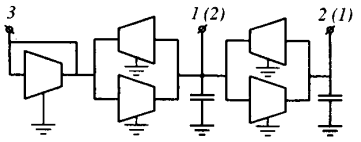

Figure 4: The only minimal three-node network (with grounded capacitors) that can be used to implement a robust notch filter.

denominator's first-order term. Hence, we have to choose g_{13}, g_{32}, g_{31} and g_{23} in such a way that either (7) or (8) is satisfied.

$$g_{23}g_{32} = 0 \quad \& \quad g_{31}g_{13} \neq 0 \tag{7}$$

$$g_{23}g_{32} \neq 0 \quad \& \quad g_{31}g_{13} = 0 \tag{8}$$

Restrictions (6) and (7) are simultaneously satisfied when $g_{23} = g_{32} = 0$ while restrictions (6) and (8) are satisfied when $g_{13} = g_{31} = 0$. In both cases we obtain the same minimal network[5] (e.g. Fig. 4). Thus, there is only one three-node network that can be used to implement notch transfer function. The impedance matrix $Z_{Fig.5}(s)$ of this network is:

$$\frac{1}{D_{Fig.5}(s)} \begin{bmatrix} sC_2g_{33} & -g_{12}g_{33} & -sC_2g_{13} \\ -g_{21}g_{33} & sC_1g_{33} & g_{13}g_{21} \\ -sC_2g_{31} & g_{12}g_{31} & s^2C_1C_2 - g_{12}g_{21} \end{bmatrix} \tag{9}$$

where $D_{Fig.5}(s) = s^2C_1C_2g_{33} - sC_2g_{31}g_{13} - g_{21}g_{12}g_{33}$. Such derived impedance matrix shows that total of six SI/SO transconductors are needed to realize Fig. 4-based biquad.

4.2. Robust High-Pass Topologies

To obtain network that has high-pass response we have to make the zero-order and the first-order terms of (5) zero. This can be done by setting g_{11}, g_{22} and g_{12} to zero or by

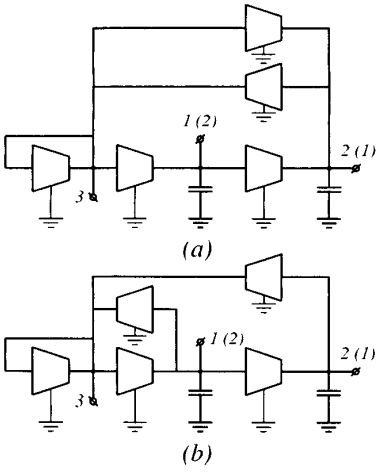

Figure 5: The only minimal three-node networks that can be used to implement high-pass transfer function.

[5]The difference is in the node labeling not the network connectivity.

setting g_{11}, g_{22} and g_{21} to zero. After considering the determinants of the resulting admittance matrices we find that in each case one additional transconductor can be removed[6]. Thus, after relatively straightforward considerations we find that total of four transconductances can be eliminated. The possibilities are:

1) $g_{11} = g_{22} = g_{12} = g_{31} = 0$;
2) $g_{11} = g_{22} = g_{12} = g_{23} = 0$;
3) $g_{11} = g_{22} = g_{21} = g_{13} = 0$;
4) $g_{11} = g_{22} = g_{21} = g_{32} = 0$;

These four possibilities lead to two distinct networks[7]. The networks have the following impedance matrices:

Fig. 5(a)

$$\frac{1}{D(s)} \begin{bmatrix} sC_2g_{33} - g_{23}g_{32} & g_{13}g_{32} & -sC_2g_{13} \\ -g_{21}g_{33} & sC_1g_{33} & -sC_1g_{23} + g_{13}g_{21} \\ g_{21}g_{32} & -sC_1g_{32} & s^2C_1C_2 \end{bmatrix} \tag{10}$$

where $D(s) = s^2C_1C_2g_{33} - sC_1g_{23}g_{32} + g_{21}g_{13}g_{32}$

Fig. 5(b)

$$\frac{1}{D(s)} \begin{bmatrix} sC_2g_{33} & g_{13}g_{32} & -sC_2g_{13} \\ -g_{21}g_{33} & sC_1g_{33} - g_{13}g_{31} & g_{13}g_{21} \\ -sC_2g_{31} + g_{21}g_{32} & -sC_1g_{32} & s^2C_1C_2 \end{bmatrix} \tag{11}$$

where $D(s) = s^2C_1C_2g_{33} - sC_2g_{31}g_{13} + g_{21}g_{13}g_{32}$.

Again, total of six SI/SO transconductors will be needed to realize Fig. 5(a) or Fig. 5(b) based HP biquads. Thus, a practical fully-differential HP biquad filter requires no less than six fully-differential transconductance elements.

Naturally, the sign of the transconductors used must be chosen in such a way that a stable network is achieved. Such sign selection is not unique. The sign selection however is trivial and for that reason it will not be discussed here.

The identification of the basic high-pass and notch topologies allows for a classification of previously reported $Gm - (grounded)C$ architectures. The classification of the cited in this paper architectures is given on the next page.

Parasitic capacitive loading of node "3" affects all three-node architectures. This situation becomes even more problematic if more "additional" nodes are introduced. For this reason, we believe that quad-node (see Fig. 4(a) in [3]) and other higher-order architectures are not worth considering.

5. AN ALTERNATIVE VIEW

The implementation of a transfer function that has finite transmission zeroes calls for an implementation of a suitable impedance (see Fig. 3). The impedances required for the implementation of notch and high-pass characteristics are respectively:

$$Z_{notch} = \frac{R(s^2 + a_0)}{s^2 + a_1s + a_0} \quad \& \quad Z_{HP} = \frac{Rs^2}{s^2 + a_1s + a_0} \tag{12}$$

Using long division these two expressions yield Fig. 6 canonical forms. As illustrated in Fig. 7 the previously introduced

[6]For the case where $g_{12} = 0$ either g_{31} or g_{23} can be set to zero. For the case where $g_{21} = 0$ either g_{13} or g_{32} can be set to zero.

[7]Conditions 1) and 4) yield Fig. 5(a) network while conditions 2) and 3) yield Fig. 5(b).

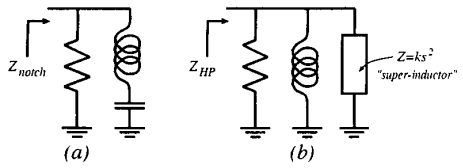

Figure 6: Impedances that must be realized to implement notch and high-pass transfer functions.

Fig. 4 topology implements the required impedance.

Fig. 6 high-pass canonical form contains a non-physical element: an inductive type frequency dependent negative resistance. Its implementation is shown in Fig. 8(a). There are two different ways to emulate the required inductor. As a result we obtain two different high-pass impedance topologies: Fig. 8(b) and Fig. 8(c). These are identical to the previously derived Fig. 5(a) and Fig. 5(b) topologies.

6. CONCLUSIONS

We have shown that circuits with grounded capacitors that implement transfer functions with second-order numerator have at least three distinct nodes (four nodes if input node is counted).

We have shown that there is only one architecture that implements robust notch transfer function and only two distinct architectures that implement robust high-pass transfer function[8].

We have argued that if only grounded capacitors are used, at least six transconductors will be needed to implement high-pass and notch transfer functions.

Implementation	Transfer Function	Topology
Fig. 6(b) in [5]	notch	Fig. 4
Fig. 1 in [6]	notch	Fig. 4
Fig. 4(b) in [3]	high-pass	Fig. 5(a)
Fig. 4 in [6]	high-pass	Fig. 5(a)
Fig. 12(b) in [1]	high-pass	Fig. 5(b)
[2]	high-pass	Fig. 5(b)
Fig. 3 in [4]	high-pass	Fig. 5(b)
Fig. 6 (c) in [5]	high-pass	Fig. 5(b)
Fig. 2 in [6]	high-pass	Fig. 5(b)

Table 1: Classification of previously reported high-pass and notch biquadratic filters.

7. REFERENCES

[1] E. Sánchez-Sinencio, R. L. Geiger and H. Nevarez-Lozano, "Generation of continuous-time two integrator loop OTA filter structures,"*IEEE Transactions on Circuits and Systems,* vol. 35, no. 8, pp. 936-945, 1988.

[8]These implementations also yield (as a biproduct) a large number of different low-pass and band-pass architectures. All of which allow independent frequency and Q tuning.

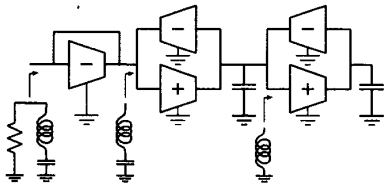

Figure 7: Emulation of Fig. 6(a) canonical form.

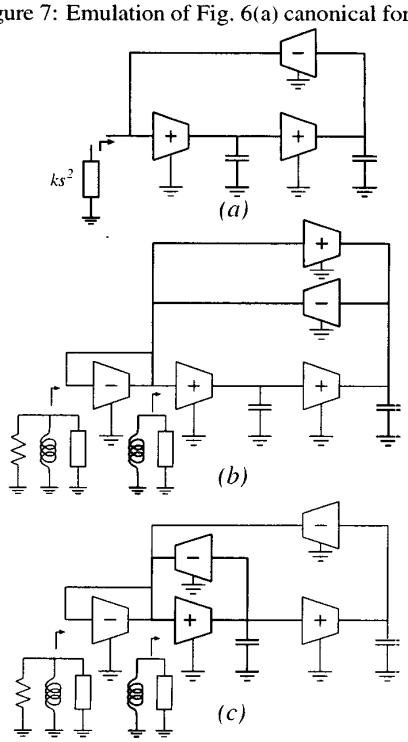

Figure 8: Emulation of Fig. 6(b) canonical form.

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