7V Tristate-Capable Output Buffer Implemented in Standard 2.5V CMOS Process

Vladimir Prodanov and Vito Boccuzzi
Bell Laboratories/ Lucent Technologies
600 Mountain Ave., Murray Hill, NJ 07974

Abstract
This paper describes high-voltage CMOS buffer architecture that uses low-voltage transistors. The voltage capability of presented architecture is nearly three times larger than the voltage capability of used MOSFET's. This buffer topology could be used to provide 3.3V compatibility of 1.2V and 1.5V digital ICs implemented in standard CMOS technology. A 7V circuit-prototype was fabricated in 0.25μm 2.5V CMOS technology. Performed measurements demonstrate stress-free operation in both active and high-impedance mode.

Introduction
As CMOS technology scales below 0.2μm, allowed supply voltages become significantly lower than previous 3.3V and 5V standards [1]. Because of economic reasons, systems usually use chips spanning several technology generations. As a result, a 3.3V IC might need to interface with another IC designed to operate from lower supply voltage (such as 1.5V). This scenario presents a serious problem: The buffer circuits of the 1.5V IC neither can provide nor sustain (when in high-impedance state) a 3.3V drive.

One could solve the above problem in two ways. The first approach is to use "dual-supply" technology. However, the use of technology that has two types of transistors such as 1.5V(low-voltage) and 3.3V(high-voltage) devices, increases production cost.

The second approach is to develop buffer architectures that have high-voltage capabilities and use only low-voltage transistors. Reported to date high-voltage buffers with low-voltage transistors (HVB/LVT) can be classified into two basic groups: 1) circuits with both high-voltage tolerance and high-voltage drive; 2) circuits with high-voltage tolerance and low-voltage drive. The conceptual schematics of these two types of HVB/LVT's are shown in Fig. 1. The pad driver in Fig. 1(a) consists of n-channel and p-channel cascode stacks. The cascodes allow output to transfer between 0 and Vhigh, while the Vgs's and Vgd's of all four transistors remain lower than 1/2Vhigh [2]. Thus, the voltage capability of Fig. 1(a) pad driver is two times larger than the voltage capability of used MOSFET's. For proper operation the cascode pad driver requires two in-phase input signals. Both signals must have low-voltage (1/2Vhigh) swing. These signals are provided through two "regular" inverter chains and are generated by the level-shifter circuit. The level-shifter takes a 0-to-1/2Vhigh input and produces signal that swings between 1/2Vhigh and Vhigh. Naturally, the level-shifter must be implemented in such a way that none of its transistors experiences voltage overstress.

Unlike previously discussed HVB/LVT the circuit shown in Fig. 1(b) is biased from the lower supply voltage. As a result its output drive is only 0-to-1/2Vhigh . The structure however allows pad voltage to exceed supply (when the buffer is in tristate mode), i.e. the circuit has high-voltage tolerance (≈ Vhigh). Three problems have been eliminated to achieve this 2X tolerance [3]: 1) Vgs over-stress of n-channel transistor; 2) conduction of p-channel transistor; 3) forward biasing of the drain-bulk pn junction of p-channel transistor. The first problem is resolved by using an n-channel cascode, while the second and the third are eliminated by using dynamic gate and bulk biasing (conceptually illustrated using two pairs of switches).

Recently, two HVB/LVT's with beyond-2X voltage capabilities have been reported. Clark [4] has developed circuit with 3.3V drive and 5V tolerance using 2V transistors, while Singh and Salem [5] have extended the stress-free range of a cascode stack beyond supply and ground with approximately one threshold voltage. Both circuits use dynamic gate biasing.

In the next two Sections we will describe an HVB/LVT that has a stress-free range of nearly 3X. Its high-voltage

---

1Many sub-0.2μm technologies are "dual-supply" technologies.
2This increase could be as much as 20%.

---

23-4-1

IEEE 2001 CUSTOM INTEGRATED CIRCUITS CONFERENCE

497
capability is achieved by means of suitable dynamic gate biasing.

**High-Voltage Pad Driver**

The conceptual schematic of pad driver having stress-free range of 3X is shown in Fig. 2(a). In this circuit the pad voltage controls $S_1$ and $S_2$ switches which provide dynamic gate biasing for the triple cascode. None of the used six transistors will experience $V_{ds}$ or $V_{tg}$ voltage overstress if the following conditions are satisfied:

- Transistors are shared. The controls of the triple cascode is split into two separate circuits, one of them is always operated in tristate and the switching transistors are shared. The controls for the switching transistors are derived from the "always-tristate" circuit. Switch transistors $P3$ and $n2$ respond only to changes in $V_{pad}$ and provide dynamic protection for transistors $n3A$ and $P3A$. However, since the drain and gate nodes of these two

- Direct connection would result in voltage overstress of switch transistors.

- Transistors are coupled respectively to the gate and drain nodes of $n3B$ and $P3B$. The switches also provide protection for $n3B$ and $P3B$. Eliminating the "unused" $n1A$, $n2A$, $P1A$, and $P2A$ we obtain the HVB/LVT shown in Fig. 2(d).

The gate-source (GS) and gate-drain (GD) voltages of all ten transistors are always limited to $\pm 1/3V_{high}$. Unfortunately, drain-source (DS) voltages of transistors $n3A$, $n3B$, and $P3B$ exceeds $1/3V_{high}$ by at least one threshold voltage.

To keep $V_{ds}$ of $n3A \leq 1/3V_{high}$ we have to pull node "1A" up to $2/3V_{high}$. This is accomplished in Fig. 2(e) via transistor $n_{up}$. Similarly, to keep $V_{ds}$ of $n3B \leq 1/3V_{high}$ we have to pull node "2A" down to $1/3V_{high}$ which is accomplished via transistor $p_{down}$. Note that when activated $n_{up}$ does not connect "1A" directly to $2/3V_{high}$. Instead, it connects it to node "G" which for high pad voltages acquire desired $2/3V_{high}$ value. Similarly, node "2A" is brought down to $1/3V_{high}$ via node "G", i.e. indirectly. This is intentionally done in order to guarantee that transistors $n_{up}$ and $p_{down}$ are not stressed.

The final problem that needs to be addressed is the drain-source overstress of transistors $n3B$ and $P3B$. We will briefly discuss what causes the drain-source overstress of transistor $n3B$ and we will provide circuit solution to this problem.

When the pad voltage equals $V_{high}$ the drain-source...
voltage of transistors $n_2B$ and $n_3B$ (see Fig. 3(a)) are: $V_{DSn2B} = 1/3V_{high} + (V_{GSn2B} - V_{GSn3B})$ and $V_{DSn3B} = 1/3V_{high} + V_{GSn3B}$ respectively. Immediately after input transition both $V_{GSn2B}$ and $V_{GSn3B}$ increase so that cascode transistors could carry the current conducted by $n_1B$. These changes would alter $V_{DSn2B}$ and $V_{DSn3B}$. According to the first equation, the change in $V_{DSn2B}$ can be kept low (thus $V_{DSn2B}$ could be kept approximately constant and equal to $1/3V_{high}$) by making $n_2B$ and $n_3B$ identical in size. The second equation reveals that $n_3B$ would experience an overstress of $V_{GSn3B}$. This overstress could be prevented by connecting an additional cascode transistor as shown in Fig. 3(b). With $n_4B$ in place, drain-source voltage of $n_3B$ becomes $V_{DSn3B} = 1/3V_{high} + (V_{GSn3B} - V_{GSn4B})$. This drain-source voltage can now be kept nearly constant and equal to $1/3V_{high}$ by simply making $n_2B$ and $n_3B$ identical in size. This drain-source overstress protection requires gate of $n_4B$ to have potential of $V_{GSn4B}$ whenever the pad node has potential $V_{high}$. The gate potential of transistor $n_4B$ should however be lowered to $1/3V_{high}$ as pad nodes traverse toward ground, i.e. $n_4B$ requires a $V_{high} - to- 1/3V_{high}$ dynamic gate biasing. Such biasing is readily available - node “2A” in Fig. 2(e) circuit.

Similarly, the drain-source overstress of $p_{3B}$ is eliminated by the addition of $p_{4B}$ cascode transistor. As shown in Fig. 3(c) required dynamic biasing ($0 - to - 2/3V_{high}$) is obtained by directly connecting the gate of transistor $p_{4B}$ to node “1A”.

The Level-Shifter Circuit
Level-shifter consists of two inverters and an RS latch (see Fig. 4(a)). Each inverter is comprised of input transistor ($n_{iA}$ & $n_{iB}$), a cascode stack (the $n_i$'s) and load transistor ($n_{LA}$ & $n_{LB}$). Cascode transistors provide over-stress protection for the input devices. For effective over-stress protection all devices must have the same size. With equally sized input and load transistors, Fig. 4(a) inverter structures exhibit gain of near-unity for large signals. Inverter gain is on first order insensitive to process and temperature variations. Fig. 4(a) level-shifter architecture however dissipates (static) power.

The static power dissipation could be reduced if the two inverters are impulse driven. To minimize static power consumption we have to minimize input pulse duration$^7$. If the two inverter structure are pulse driven both inverter outputs will be “high” most of the time. In order to be able to retain its state, the latch must be implemented using NAND gates (as opposed to NOR gates).

Schematic of the complete level-shifter circuit is shown in Fig. 4(b). Desired impulse drive is realized using a “one-shot” circuit. This circuit employs three MOS inverters, two NAND gates and a NAND-based RS latch (RSL). Transistors $n_{inA}$, $n_{inB}$, $n_{1A}$ and $n_{2B}$ are also part of the one-shot circuit$^4$. Pulse is produced at the gate of transistor $n_{inA}$ ($n_{inB}$) whenever there is positive (negative) input transition. The duration of the produced pulse is approximately equal to $\tau_{MOS} + \frac{\tau_{in}}{n_{i}} + \tau_{RS}$; where $\tau_{MOS}$ is the delay of the MOS inverter, $\tau_{in}/n_{i}$ is the delay of the $n_{in} - n_{ei}$ inverter and $\tau_{RS}$ is the switching delay of the used RS latch. As long as RS1 and RSL are equally loaded and present minor loading to their corresponding driving circuits, the duration of the generated driving pulses would be sufficient to guarantee switching of latch RS1.

Experimental Results
Tristate-capable 7V output buffer (see Fig. 5) was fabricated with Lucent's 0.25µm 2.5V CMOS process. The circuit was designed to drive 10F of load capacitance at 200MHz. Pad driver transistor sizes (all in µm) are as

$^7$Pulse duration however should be sufficiently large so that RS latch could change its state.

$^4$The two-transistor structures $n_{inA} - n_{e1A}$ and $n_{inB} - n_{e1B}$ can be viewed as inverters.
The circuit was tested extensively. Twenty three packaged parts (out of 25 tested) were functional. On-wafer probing was also performed successfully. To verify high-voltage capability, internal nodes (IA, 2A and G) had to be measured while the buffer was being operated in "package-like environment". The obtained waveforms were then compared to output (pad) waveform. The potential differences \( V_{\text{out}} - V_{\text{IA}}, V_{\text{out}} - V_{\text{2A}} \) and \( V_{\text{out}} - V_{\text{G}} \) are indicative of presence/absence of GS-GD voltage overstress. These differences indeed remain bounded to approximately \( \pm 2.5V \) (see Fig. 6 and Fig. 7).

**Conclusion**

We have presented high-voltage output buffer. The voltage drive and tolerance of the developed circuit is nearly three times larger than that of used MOS devices. The circuit has been experimentally verified in 0.25\( \mu \)m 2.5V CMOS process, but it can be used in any other CMOS process. The use of proposed architecture entails performance-cost trade-off.

**References**


\( ^9 \) This was done by bonding a bare die directly on a PCB and using active (Pico) probes.

\( ^{10} \) No dual-supply technology is required, but the performance is inferior to that of a "regular" buffer implemented with high-voltage devices.