

# 7V Tristate-Capable Output Buffer Implemented in Standard 2.5V CMOS Process

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## Abstract

This paper describes high-voltage CMOS buffer architecture that uses low-voltage transistors. The voltage capability of presented architecture is nearly three times larger than the voltage capability of used MOSFET's. This buffer topology could be used to provide 3.3V compatibility of 1.2V and 1.5V digital ICs implemented in standard CMOS technology. A 7V circuit-prototype was fabricated in 0.25 $\mu\text{m}$  2.5V CMOS technology. Performed measurements demonstrate stress-free operation in both active and high-impedance mode.

## Introduction

As CMOS technology scales below 0.2 $\mu\text{m}$ , allowed supply voltages become significantly lower than previous 3.3V and 5V standards [1]. Because of economic reasons, systems usually use chips spanning several technology generations. As a result, a 3.3V IC might need to interface with another IC designed to operate from lower supply voltage (such as 1.5V). This scenario presents a serious problem: *The buffer circuits of the 1.5V IC neither can provide nor sustain (when in high-impedance state) a 3.3V drive.*

One could solve the above problem in two ways. The first approach is to use "dual-supply" technology. However, the use of technology that has two types of transistors such as 1.5V (low-voltage) and 3.3V (high-voltage) devices, increases production cost<sup>2</sup>.

The second approach is to develop buffer architectures that have high-voltage capabilities and use only low-voltage transistors. Reported to date *high-voltage buffers with low-voltage transistors* (HVB/LVT) can be classified into two basic groups: 1) circuits with both high-voltage tolerance and high-voltage drive; 2) circuits with high-voltage tolerance and low-voltage drive. The conceptual schematics of these two types of HVB/LVT's are shown in Fig. 1. The pad driver in Fig. 1(a) consists of n-channel and p-channel cascode stacks. The cascodes allow output to traverse between 0 and  $V_{high}$  while the  $V_{gs}$ 's and  $V_{gd}$ 's of all four transistors remain lower than  $1/2V_{high}$  [2]. Thus, the voltage capability of Fig. 1(a) pad driver is two times larger than the voltage capability of used MOSFET's. For

<sup>1</sup>Many sub-0.2 $\mu\text{m}$  technologies are "dual-supply" technologies.

<sup>2</sup>This increase could be as much as 20%.

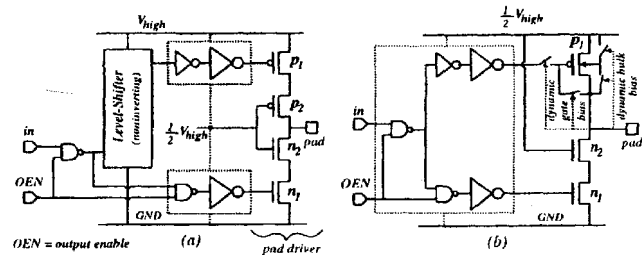


Figure 1: Conceptual schematics of high-voltage tristate-capable output buffers: (a) with 2X drive and 2X tolerance; (b) with "regular" (1X) drive and 2X tolerance;

proper operation the cascode pad driver requires two in-phase input signals. Both signals must have low-voltage ( $1/2V_{high}$ ) swing. These signals are provided through two "regular" inverter chains and are generated by the level-shifter circuit. The level-shifter takes a 0-to- $1/2V_{high}$  input and produces signal that swings between  $1/2V_{high}$  and  $V_{high}$ . Naturally, the level-shifter must be implemented in such a way that none of its transistors experiences voltage overstress.

Unlike previously discussed HVB/LVT the circuit shown in Fig. 1(b) is biased from the lower supply voltage. As a result its output drive is only 0-to- $1/2V_{high}$ . The structure however allows pad voltage to exceed supply (when the buffer is in tristate mode), i.e. the circuit has high-voltage tolerance ( $\approx V_{high}$ ). Three problems have been eliminated to achieve this 2X tolerance [3]: 1)  *$V_{dg}$  overstress of n-channel transistor*; 2) *conduction of p-channel transistor*; 3) *forward biasing of the drain-bulk pn junction of p-channel transistor*. The first problem is resolved by using an n-channel cascode, while the second and the third are eliminated by using dynamic gate and bulk biasing (conceptually illustrated using two pairs of switches).

Recently, two HVB/LVT's with beyond-2X voltage capabilities have been reported. Clark [4] has developed circuit with 3.3V drive and 5V tolerance using 2V transistors, while Singh and Salem [5] have extended the stress-free range of a cascode stack beyond supply and ground with approximately one threshold voltage. Both circuits use dynamic gate biasing.

In the next two Sections we will describe an HVB/LVT that has a stress-free range of nearly 3X. Its high-voltage

capability is achieved by means of suitable dynamic gate biasing.

### High-Voltage Pad Driver

The conceptual schematic of pad driver having stress-free range of  $3X$  is shown in Fig. 2(a). In this circuit the pad voltage controls  $S_1$  and  $S_2$  switches<sup>3</sup> which provide dynamic gate biasing for the triple cascode. None of the used six transistors will experience  $V_{gs}$  or  $V_{ds}$  voltage overstress if the following conditions are satisfied:

	Turns ON/OFF	Stays ON
$S_1$	$1/3V_{high} < V_{pad} < 2/3V_{high}$	$V_{pad} < 1/3V_{high}$
$S_2$	$1/3V_{high} < V_{pad} < 2/3V_{high}$	$V_{pad} > 2/3V_{high}$

The fact that  $S_1$  must be ON when its control voltage (i.e.  $V_{pad}$ ) is lower than the switch terminal voltages suggests that  $S_1$  should be implemented using p-channel transistor.  $S_2$  on the other hand should be implemented using n-channel transistor because it must be ON when its control voltage is higher than its terminal voltages.

The gates of both switch transistors should be controlled by  $V_{pad}$ , but they can not be directly connected to the pad node<sup>4</sup>. For stress-free operation the gate voltage of  $p_{S1}$  must follow  $V_{pad}$  but it should never exceed  $2/3V_{high}$ . Similarly, the gate voltage of  $n_{S2}$  must follow  $V_{pad}$  but it should never go below  $1/3V_{high}$ . When Fig. 2(a) pad driver is in tristate mode, nodes "1" and "2" have the required voltage excursions<sup>5</sup>.

The above observations lead to Fig. 2(b) pad driver. The circuit was simulated using models for Lucent's  $0.25\mu m$   $2.5V$  technology and  $V_{high}$  of  $7.5V$ . It was placed in tristate mode (i.e. both  $n_1$  and  $p_1$  - OFF) and the pad voltage was varied between  $0$  and  $7.5V$ . As expected, the gate-source and gate-drain voltages of all eight transistors remain bounded to  $\pm 2.5V$ . Unfortunately, in active mode  $V_1$  is not only function of  $V_{out}$  (i.e.  $V_{pad}$ ) but it is also function of the gate voltage of transistor  $n_1$  (i.e.  $V_{gn1}$ ). Similarly,  $V_2$  is function of both  $V_{pad}$  and  $V_{gp1}$ . As a result, immediately after each input transition both  $p_{S1}$  and  $n_{S2}$  are ON and conducting large "shot-trough" current. More importantly, during the same time the gate oxides of both  $n_3$  and  $p_3$  are subjected to voltage overstress. This problem is eliminated in the circuit of Fig. 2(c). Here, the triple cascode is split into two separate circuits, one of them is always operated in tristate and the switching transistors are shared. The controls for the switching transistors are derived from the "always-tristate" circuit. Switch transistors  $p_{S1}$  and  $n_{S2}$  respond only to changes in  $V_{pad}$  and provide dynamic protection for transistors  $n_{3A}$  and  $p_{3A}$ . However, since the drain and gate nodes of these two

<sup>3</sup>  $S_1$  and  $S_2$  must not be ON at the same time.

<sup>4</sup> Direct connection would result in voltage overstress of switch transistors.

<sup>5</sup>  $V_1$  follows  $V_{pad}$  down to ground, but it would not increase much beyond  $2/3V_{high} - V_{tn}$ .  $V_2$  on the other hand follows  $V_{pad}$  to supply rail but it would not decrease significantly below  $1/3V_{high} + V_{tp}$ .

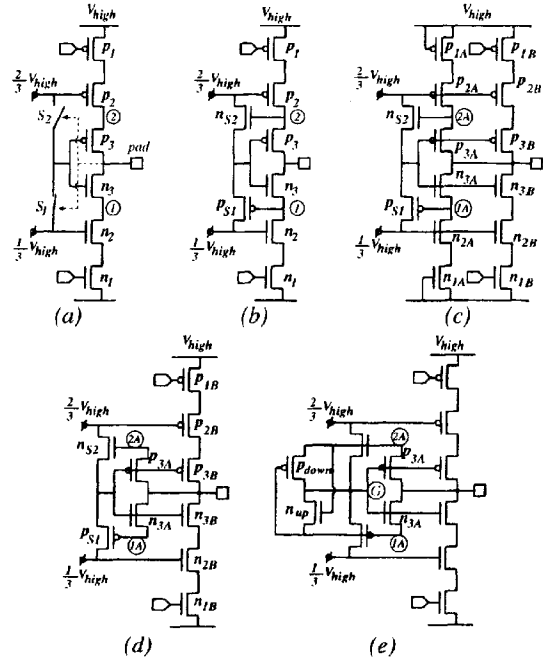


Figure 2: Evolution of  $3X$  pad driver: a) conceptual schematic. b) implementation that works well in tristate mode but fails in active mode. c) implementation that works well both in tristate and active modes. d) reduced topology. e) topology where the DS overstress of transistors  $n_{3A}$  and  $p_{3A}$  has been eliminated.

transistors are coupled respectively to the gate and drain nodes of  $n_{3B}$  and  $p_{3B}$  the switches also provide protection for  $n_{3B}$  and  $p_{3B}$ . Eliminating the "unused"  $n_{1A}$ ,  $n_{2A}$ ,  $p_{1A}$  and  $p_{2A}$  we obtain the HVB/LVT shown in Fig. 2(d)

The gate-source (GS) and gate-drain (GD) voltages of all ten transistors are always limited to  $\pm 1/3V_{high}$ . Unfortunately, drain-source (DS) voltages of transistors  $n_{3A}$ ,  $p_{3A}$ ,  $n_{3B}$  and  $p_{3B}$  exceeds  $1/3V_{high}$  (by at least one threshold voltage).

To keep  $V_{ds}$  of  $n_{3A} \leq 1/3V_{high}$  we have to pull node "1A" up to  $2/3V_{high}$ . This is accomplished in Fig. 2(e) via transistor  $n_{up}$ . Similarly, to keep  $V_{ds}$  of  $n_{3A} \leq 1/3V_{high}$  we have to pull node "2A" down to  $1/3V_{high}$  which is accomplished via transistor  $p_{down}$ . Note that when activated  $n_{up}$  does not connect "1A" directly to  $2/3V_{high}$ . Instead, it connects it to node "G" which for high pad voltages acquire desired  $2/3V_{high}$  value. Similarly, node "2A" is brought down to  $1/3V_{high}$  via node "G", i.e. indirectly. This is intentionally done in order to guarantee that transistors  $n_{up}$  and  $p_{down}$  are not stressed.

The final problem that needs to be addressed is the drain-source overstress of transistors  $n_{3B}$  and  $p_{3B}$ . We will briefly discuss what causes the drain-source overstress of transistor  $n_{3B}$  and we will provide circuit solution to this problem<sup>6</sup>.

When the pad voltage equals  $V_{high}$  the drain-source

<sup>6</sup>The  $p_{3B}$  case is analogous and will not be discussed here.

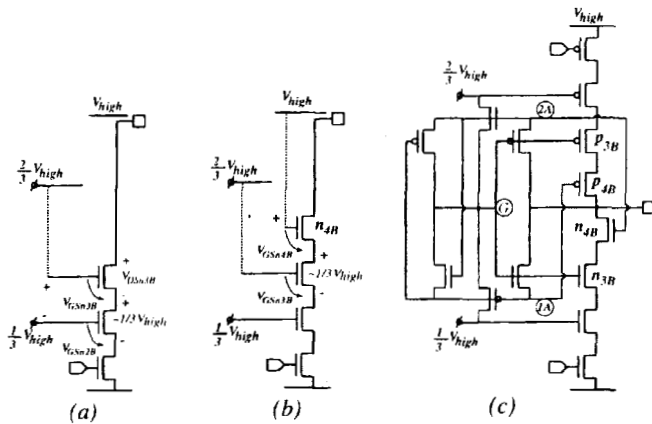


Figure 3: Evolution of 3X pad driver with no DS overstress of transistors  $n_{3B}$  and  $p_{3B}$ .

voltages of transistors  $n_{2B}$  and  $n_{3B}$  (see Fig. 3(a)) are:  $V_{DSn2B} = 1/3V_{high} + (V_{GSn2B} - V_{GSn3B})$  and  $V_{DSn3B} = 1/3V_{high} + V_{GSn3B}$  respectively. Immediately after input transition both  $V_{GSn2B}$  and  $V_{GSn3B}$  increase so that cascode transistors could carry the current conducted by  $n_{1B}$ . These changes would alter  $V_{DSn2B}$  and  $V_{DSn3B}$ . According to the first equation, the change in  $V_{DSn2B}$  can be kept low (thus  $V_{DSn2B}$  could be kept approximately constant and equal to  $1/3V_{high}$ ) by making  $n_{2B}$  and  $n_{3B}$  identical in size. The second equation reveals that  $n_{3B}$  would experience an overstress of  $V_{GSn3B}$ . This overstress could be prevented by connecting an additional cascode transistor as shown in Fig. 3(b). With  $n_{4B}$  in place, drain-source voltage of  $n_{3B}$  becomes  $V_{DSn3B} = 1/3V_{high} + (V_{GSn3B} - V_{GSn4B})$ . This drain-source voltage can now be kept nearly constant and equal to  $1/3V_{high}$  by simply making  $n_{4B}$  and  $n_{3B}$  identical in size. This drain-source overstress protection requires gate of  $n_{4B}$  to have potential of  $V_{high}$  whenever the pad node has potential  $V_{high}$ . The gate potential of transistor  $n_{4B}$  should however be lowered to  $1/3V_{high}$  as pad node traverses toward ground, i.e.  $n_{4B}$  requires a  $V_{high} - to - 1/3V_{high}$  dynamic gate biasing. Such biasing is readily available - node "2A" in Fig. 2(e) circuit.

Similarly, the drain-source overstress of  $p_{3B}$  is eliminated by the addition of  $p_{4B}$  cascode transistor. As shown in Fig. 3(c) required dynamic biasing ( $0 - to - 2/3V_{high}$ ) is obtained by directly connecting the gate of transistor  $p_{4B}$  to node "1A".

### The Level-Shifter Circuit

Level-shifter consists of two inverters and an RS latch (see Fig. 4(a)). Each inverter is comprised of input transistor ( $n_{inA}$  &  $n_{inB}$ ), a cascode stack (the  $n_c$ 's) and load transistor ( $n_{LA}$  &  $n_{LB}$ ). Cascode transistors provide overstress protection for the input devices. For effective overstress protection all devices must have the same size. With

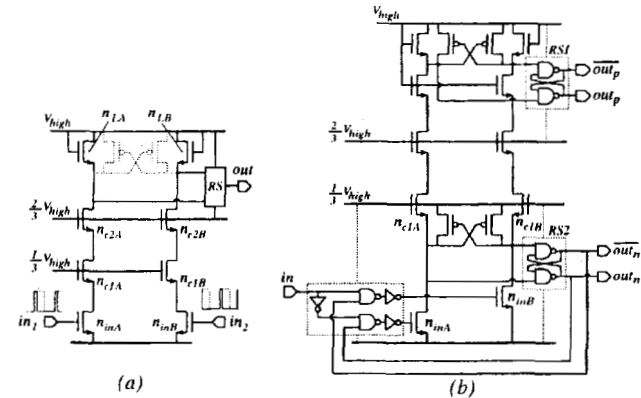


Figure 4: High-voltage level-shifter using impulse-driven RS latch: (a) conceptual schematic; (b) an implementation based upon a "one-shot" circuit;

equally sized input and load transistors, Fig. 4(a) inverter structures exhibit gain of near-unity for large signals. Inverter gain is on first order insensitive to process and temperature variations. Fig. 4(a) level-shifter architecture however dissipates (static) power.

The static power dissipation could be reduced if the two inverters are impulse driven. To minimize static power consumption we have to minimize input pulse duration<sup>7</sup>. If the two inverter structure are pulse driven both inverter outputs will be "high" most of the time. In order to be able to retain its state, the latch must be implemented using NAND gates (as opposed to NOR gates).

Schematic of the complete level-shifter circuit is shown in Fig. 4(b). Desired impulse drive is realized using a "one-shot" circuit. This circuit employs three MOS inverters, two NAND gates and a NAND-based RS latch (RS2). Transistors  $n_{inA}$ ,  $n_{inB}$ ,  $n_{c1A}$  and  $n_{c1B}$  are also part of the one-shot circuit<sup>8</sup>. Pulse is produced at the gate of transistor  $n_{inA}$  ( $n_{inB}$ ) whenever there is positive (negative) input transition. The duration of the produced pulse is approximately equal to  $\tau_{MOS} + \tau_{n_{in}/n_{c1}} + \tau_{RS}$ ; where  $\tau_{MOS}$  is the delay of the MOS inverter,  $\tau_{n_{in}/n_{c1}}$  is the delay of the  $n_{in} - n_{c1}$  inverter and  $\tau_{RS}$  is the switching delay of the used RS latch. As long as RS1 and RS2 are equally loaded and present minor loading to their corresponding driving circuits, the duration of the generated driving pulses would be sufficient to guarantee switching of latch RS1.

### Experimental Results

Tristate-capable 7V output buffer (see Fig. 5) was fabricated with Lucent's  $0.25\mu m$  2.5V CMOS process. The circuit was designed to drive  $10pF$  of load capacitance at  $200MHz$ . Pad driver transistor sizes (all in  $\mu m$ ) are as

<sup>7</sup>Pulse duration however should be sufficiently large so that RS latch could change its state.

<sup>8</sup>The two-transistor structures  $n_{inA} - n_{c1A}$  and  $n_{inB} - n_{c1B}$  can be viewed as inverters.

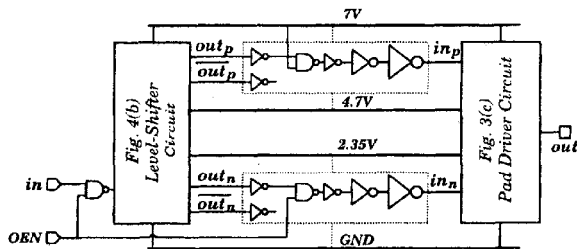


Figure 5: Schematic of complete 7V/2.5V CMOS output buffer.

follows:

$n_{1B-4B}$	370/0.24	$p_{1B-4B}$	1300/0.28
$n_{3A}, n_{up}$	37/0.24	$p_{3A}, p_{down}$	74/0.28
$n_{S2}$	740/0.24	$p_{S1}$	1300/0.28

The circuit was tested extensively. Twenty three packaged parts (out of 25 tested) were functional. On-wafer probing was also performed successfully. To verify high-voltage capability, internal nodes (1A, 2A and G) had to be measured while the buffer was being operated in "package-like environment"<sup>9</sup>. The obtained waveforms were then compared to output (pad) waveform. The potential differences  $V_{out} - V_{1A}$ ,  $V_{out} - V_{2A}$  and  $V_{out} - V_G$  are indicative of presence/absence of GS-GD voltage overstress. These differences indeed remain bounded to approximately  $\pm 2.5V$  (see Fig. 6 and Fig. 7).

### Conclusion

We have presented high-voltage output buffer. The voltage drive and tolerance of the developed circuit is nearly three times larger than that of used MOS devices. The circuit has been experimentally verified in  $0.25\mu m$  2.5V CMOS process, but it can be used in any other CMOS process. The use of proposed architecture entails performance-cost trade-off<sup>10</sup>.

### References

- [1] The 1999 International Technology Roadmap for Semiconductors.
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- [3] M. Pelgrom and E. Dijkmans, "A 3/5V Compatible I/O Buffer," *IEEE J. of Solid-State Circuits*, vol. 30, No. 7, pp. 823-825, Jul. 1995.
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<sup>9</sup>This was done by bonding a bare die directly on a PCB and using active (Pico) probes.

<sup>10</sup>No dual-supply technology is required, but the performance is inferior to that of a "regular" buffer implemented with high-voltage devices.

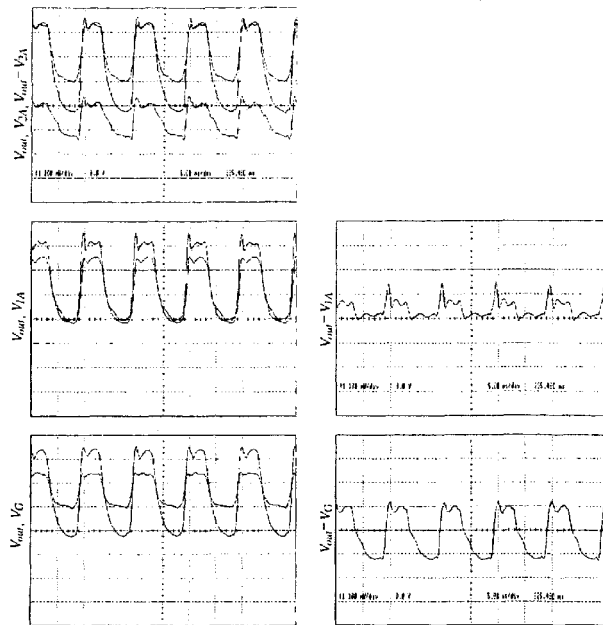


Figure 6: Developed 7V/2.5V output buffer in active mode: Measured waveforms. All figures: 5ns/dev and 2V/dev (100mV/dev with 20 : 1 probes).

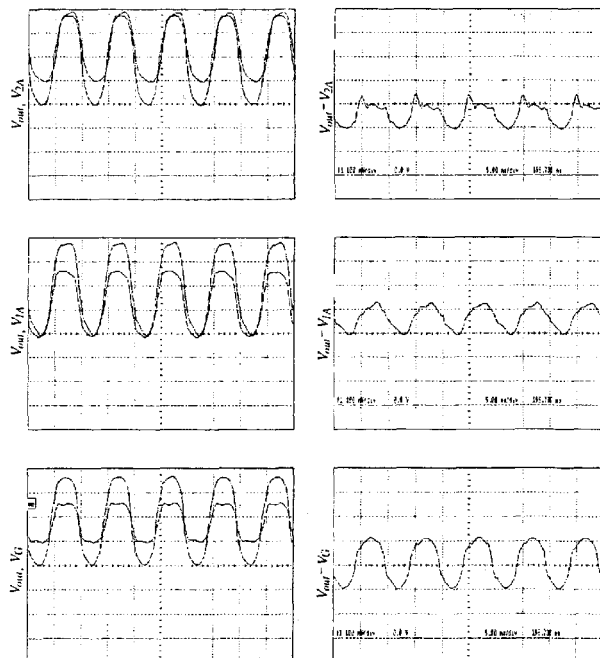


Figure 7: Developed 7V/2.5V output buffer in tristate mode: Measured waveforms. All figures: 5ns/dev and 2V/dev (100mV/dev with 20 : 1 probes).